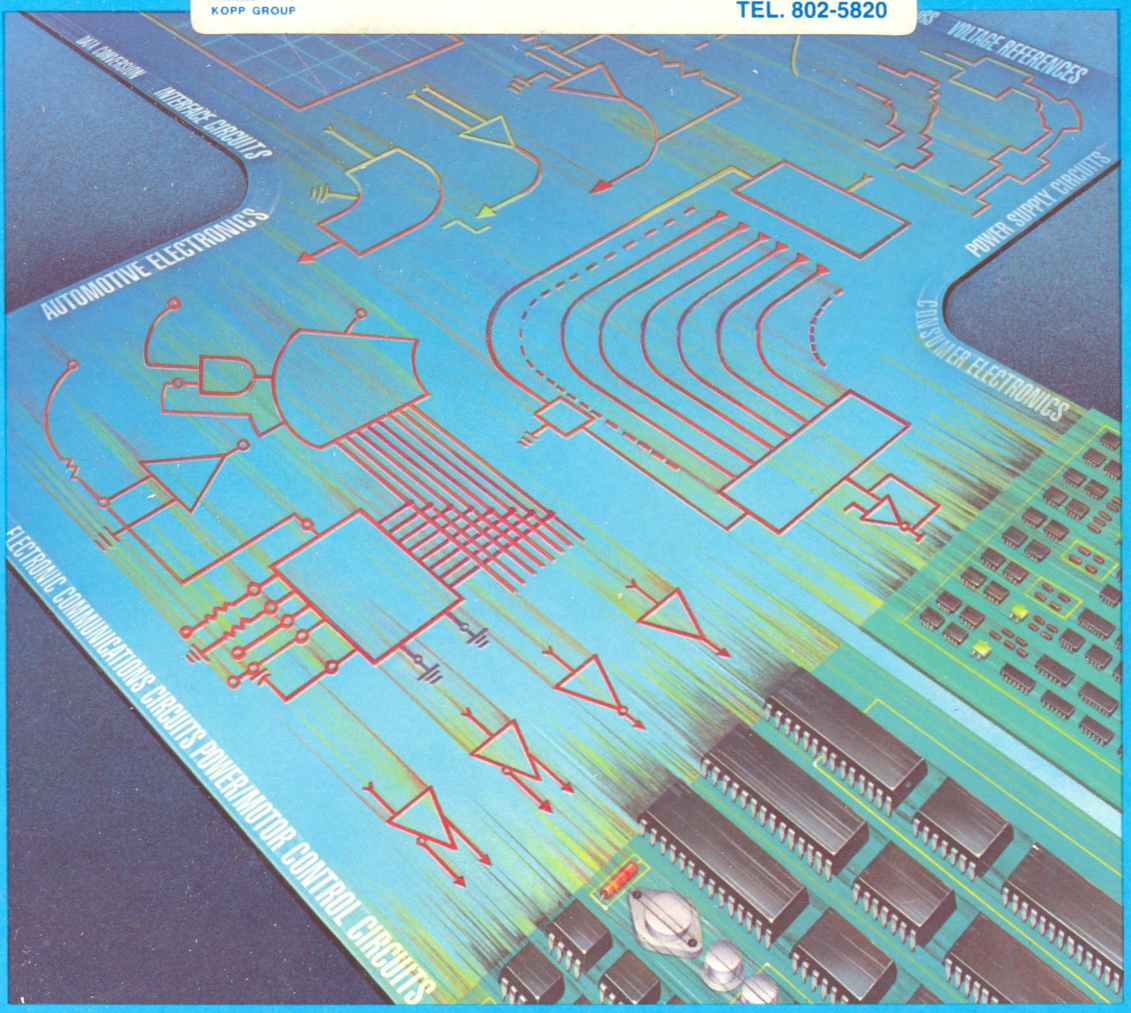
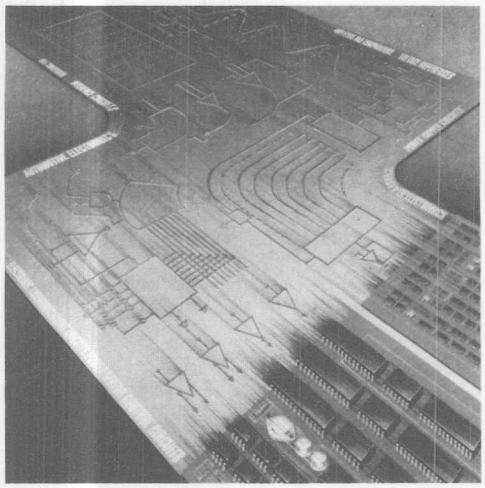
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LINEAR AND INTERFACE INTEGRATED CIRCUITS



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LINEAR AND INTERFACE INTEGRATED CIRCUITS

This publication presents technical information for the broad line of Linear and Interface Integrated Circuit products. Complete device specifications are provided in the form of **Data Sheets** which are categorized by product type into ten chapters for easy reference. **Selector Guides** by product family are provided in the beginning of each Chapter to enable quick comparisons of performance characteristics. A **Cross Reference** chapter lists Motorola direct replacement and functional equivalent part numbers for other industry products.

A chapter is provided to illustrate **Package Outline** and mounting hardware drawings, and includes information on Surface Mount Devices (SMD), and Industry Package Cross Reference Guide.

Additionally, chapters are provided with information on **Quality** program concepts, high-reliability processing, and abstracts of available **Technical Literature.**

The information in this book has been carefully checked and is believed to be accurate; however, no responsibility is assumed for inaccuracies.

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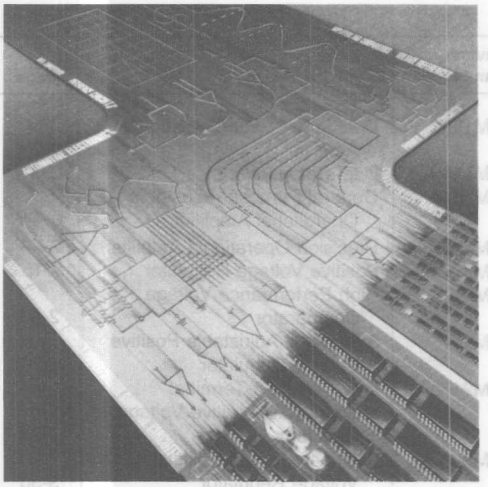
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Index/Cross Reference



In Brief . . .

In the Cross Reference Section of this chapter, a complete interchangeability list linking over 3000 devices is offered by most major Linear Integrated Circuits manufacturers to the nearest equivalent Motorola device. The "Motorola Direct Replacement" column lists devices with identical pin connections and package and the same or better electrical characteristics and temperature range. The "Motorola Similar Replacement" column provides a device which performs the same function but with possible differences in package configurations, pin connections, temperature range or electrical specifications.

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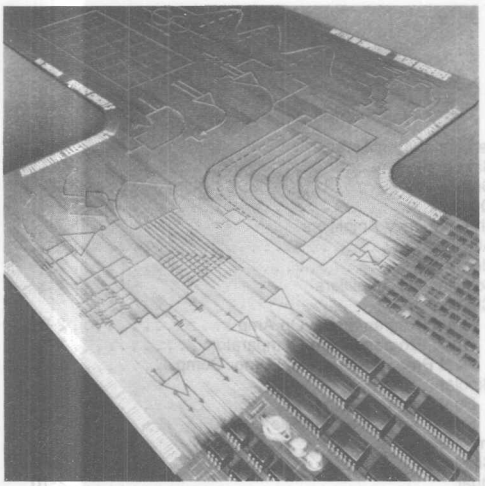
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µA7808KC	MC7808K		3-132
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µA7808UC	MC7808CT		3-132
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µA7815KC	MC7815CK		3-132
µA7815KM	MC7815K		3-132
µA7815UC	MC7815CT		3-132
µA7815UV	MC7815BT		3-132
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Amplifiers and Comparators

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In Brief . . .

For over two decades, Motorola has continually refined and updated integrated circuit technologies, analog circuit design techniques and processes in response to the ever-expanding needs of the market place. The enhanced performance of present day operational amplifiers and comparators have come into being through innovative application of these technologies, designs and processes. Some early designs, though of inferior performance by today's standards, are still available but are rapidly giving way to the new, higher performance operational amplifier and comparator circuits. Motorola has pioneered in JFET inputs, low temperature coefficient input stages, Miller loop compensation, all NPN output stages, dual-doublet frequency compensation and analog "in-the-package" trimming of resistors to produce superior high performance operational amplifiers and comparators, operating in many cases from a single supply, with low input offset, low noise, low power, high output swing, high slew rate and high gain-bandwidth product at reasonable cost to the customer.

Present day operational amplifiers and comparators find application in all segments of society to include motor controls, instrumentation, aerospace, automotive, telecommunication, medical and consumer products.

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Amplifiers and Comparators

Operational Amplifiers

Motorola offers a broad line of bipolar operational amplifiers to meet a wide range of applications. From low-cost industry-standard types to high precision circuits, the span encompasses a large range of performance capabilities. These linear integrated circuits are available as single, dual, and quad monolithic devices in a variety of temperature ranges and package styles. Most devices may be obtained in unencapsulated "chip" form as well. For price and delivery information on chips, please contact your Motorola Sales Representative or Distributor.

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Single Operational Amplifiers

Device	I_{IB} μA Max	V_{IO} mV Max	TC_{VIO} μV/°C Typ	I_{IO} nA Max	A_{vol} V/mV Min	BW (A_V=1) MHz Typ	SR (A_V=1) V/μs Typ	Supply Voltage V Min	Supply Voltage V Max	Description	Package Suffix
Noncompensated											
Commercial Temperature Range (0°C to +70°C)											
LM301A	0.25	7.5	10	50	25	1.0	0.5	±3.0	±18	General Purpose	H, N/626, J/693
LM308	7.0	7.5	15	1.0	25	1.0	0.3	±3.0	±18	Precision	H, N/626
LM308A	7.0	0.5	5.0	1.0	80	1.0	0.3	±3.0	±18	Precision	H, N/626
MC1439	1.0	7.5	15	100	15	2.0	4.2	±6.0	±18	High Slew Rate	G/601, P1
MC1709C	1.5	7.5	15	500	15	1.0	0.3	±3.0	±18	General Purpose	G/601, P1, U
MC1748C	0.5	6.0	15	200	20	1.0	0.5	±3.0	±18	General Purpose	G/601, P1, U
Industrial Temperature Range (−25°C to +85°C)											
LM201A	0.075	2.0	10	10	50	1.0	0.5	±3.0	±22	General Purpose	H, N/626, J/693
LM208	0.002	2.0	3.0	0.2	50	1.0	0.3	±3.0	±20	Precision	H, N/626, J/632, J-8
LM208A	0.002	0.5	1.0	0.2	80	1.0	0.3	±3.0	±20	Precision	H, N/626, J/632, J-8
Military Temperature Range (−55°C to +125°C)											
LM101A	0.075	2.0	10	10	50	1.0	0.5	±3.0	±22	General Purpose	H, J/693
LM108	0.002	2.0	3.0	0.2	50	1.0	0.3	±3.0	±20	Precision	H, J, J-8/693
LM108A	0.002	0.5	1.0	0.2	80	1.0	0.3	±3.0	±20	Precision	H, J, J-8/693
MC1539	0.5	3.0	15	60	50	2.0	4.2	±4.0	±18	High Slew Rate	G/601
MC1709	0.5	5.0	15	200	25	1.0	0.3	±3.0	±18	General Purpose	G/601, U
MC1709A	0.6	3.0	5.0	100	25	1.0	0.5	±3.0	±18	High Performance MC1709	G/601
MC1748	0.5	5.0	15	200	50	1.0	0.5	±3.0	±22	General Purpose	G/601, U

Internally Compensated

Commercial Temperature Range (0°C to +70°C)

Device	I_{IB} μA Max	V_{IO} mV Max	TC_{VIO} μV/°C Typ	I_{IO} nA Max	A_{vol} V/mV Min	BW (A_V = 1) MHz Typ	SR (A_V = 1) V/μs Typ	Supply Voltage V Min	Supply Voltage V Max	Description	Package Suffix
LF351	200 pA	10	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	N/626
LF355	200 pA	10	5.0	50 pA	50	1.0	5.0	±5.0	±18	JFET Input	H/601, J/693
LF355B	100 pA	5.0	5.0	20 pA	50	2.5	5.0	±5.0	±22	JFET Input	H/601, J/693
LF356	200 pA	10	5.0	50 pA	50	2.0	15	±5.0	±18	JFET Input	H/601, J/693
LF356B	100 pA	5.0	5.0	20 pA	50	5.0	12	±5.0	±22	JFET Input	H/601, J/693
LF357	200 pA	10	5.0	50 pA	50	3.0	75	±5.0	±18	Wideband FET Input	H/601, J/693
LF357B	100 pA	5.0	5.0	20 pA	50	20	50	±5.0	±22	JFET Input	H/601, J/693
LF441C	100 pA	5.0	10	50 pA	25	2.0	6.0	±5.0	±18	Low Power JFET Input	N/626
LM11C	100 pA	0.6	2.0	10 pA	250	1.0	0.3	±3.0	±20	Precision	H, N/626, J/632, J-8/693
LM11CL	200 pA	5.0	3.0	25 pA	50	1.0	0.3	±3.0	±20	Precision	H, N/626, J/632, J-8/693
LM307	0.25	7.5	10	50	25	1.0	0.5	±3.0	±18	General Purpose	N/626
MC1436	0.04	10	12	10	70	1.0	2.0	±15	±34	High Voltage	G/601, U
MC1456	0.03	10	12	10	70	1.0	2.5	±3.0	±18	High Performance	G/601, P1, U
MC1733C	30	—	—	5.0 μA	80	90	—	±4.0	±8.0	Differential Wideband Video Amp	G/601, L, P/646
MC1741C	0.5	6.0	15	200	20	1.0	0.5	±3.0	±18	General Purpose	G/601, P1, U
MC1741SC	0.5	6.0	15	200	20	1.0	10	±3.0	±18	High Slew Rate	G/601, P1
MC1776C	0.003	6.0	15	3.0	100	1.0	0.2	±1.2	±18	μPower, Programmable	G/601, P1, U
MC3476	0.05	6.0	15	25	50	1.0	0.2	±1.5	±18	Low Cost μPower, Programmable	G/601, P1, U
MC34001	200 pA	10	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	G/601, P/626, U
MC34001A	100 pA	2.0	10	50 pA	50	4.0	13	±5.0	±18	JFET Input	G/601, P/626, U
MC34001B	200 pA	5.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	G/601, P/626, U
MC34071	0.50	5.0	10	75	25	4.5	10	+3.0	+44	High Performance,	P/626, U
MC34071A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	Single Supply	P/626, U
MC34080	200 pA	1.0	10	100 pA	25	16	55	±5.0	±22	Decompensated	P/626, U
MC34080A	200 pA	0.5	10	100 pA	50	16	55	±5.0	±22	MC34081 for $A_V \geq 2$	P/626, U
MC34081	200 pA	1.0	10	100 pA	25	8.0	30	±5.0	±22	High Speed, JFET Input	P/626, U
MC34081A	200 pA	0.5	10	100 pA	50	8.0	30	±5.0	±22	High Speed, JFET Input	P/626, U
MC34181	0.1 nA	2.0	10	0.05	25	4.0	10	±2.5	±18	Low Power JFET Input	P/626
OP-27E	0.040	0.025	0.2	35	1000	8.0	2.8	±4.0	±22	Low Noise, Precision	P/626
OP-27F	0.055	0.060	0.3	50	1000	8.0	2.8	±4.0	±22	Low Noise, Precision	P/626
OP-27G	0.080	0.100	0.4	75	700	8.0	2.8	±4.0	±22	Low Noise, Precision	P/626
TL061AC	200 pA	6.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power JFET Input	P/626
TL061BC	200 pA	3.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power JFET Input	P/626
TL061C	200 pA	15	10	200 pA	4.0	2.0	6.0	±2.5	±18	Low Power JFET Input	P/626
TL071AC	200 pA	6.0	10	50 pA	50	4.0	13	±5.0	±18	Low Noise, JFET Input	P/626, JG
TL071BC	200 pA	3.0	10	50 pA	50	4.0	13	±5.0	±18	Low Noise, JFET Input	P/626, JG
TL071C	200 pA	10	10	50 pA	25	4.0	13	±5.0	±18	Low Noise, JFET Input	P/626, JG
TL081AC	200 pA	6.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	P/626, JG
TL081BC	200 pA	3.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	P/626, JG
TL081C	400 pA	15	10	200 pA	25	4.0	13	±5.0	±18	JFET Input	P/626, JG

Industrial Temperature Range (−25°C to +85°C)

OP-27E	0.040	0.025	0.2	35	1000	8.0	2.8	±4.0	±22	Low Noise, Precision	Z
OP-27F	0.055	0.060	0.3	50	1000	8.0	2.8	±4.0	±22	Low Noise, Precision	Z
OP-27G	0.080	0.100	0.4	75	700	8.0	2.8	±4.0	±22	Low Noise, Precision	Z

Automotive Temperature Range (−40°C to +85°C)

MC33071	0.50	5.0	10	75	25	4.5	10	+3.0	+44	High Performance,	P/626, U
MC33071A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	Single Supply	P/626, U
MC33171	0.10	4.5	10	20	50	1.8	2.1	+3.0	+44	Low Power, Single Supply	P/626
MC33181	0.1 nA	2.0	10	0.05	25	4.0	10	±2.5	±18	Low Power JFET Input	P/626
TL061V	200 pA	6.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power JFET Input	P/626

Single Operational Amplifiers (continued)

Device	I_{IB} μA Max	V_{IO} mV Max	TC_{VIO} μV/°C Typ	I_{IO} nA Max	A_{vol} V/mV Min	BW (A_V=1) MHz Typ	SR (A_V=1) V/μs Typ	Supply Voltage V Min	Supply Voltage V Max	Description	Package Suffix
Internally Compensated											
Military Temperature Range (−55°C to +125°C)											
LM11	50 pA	0.3	1.0	10 pA	250	1.0	0.3	±3.0	±20	Precision	H, J/632, J-8/693
MC1536	0.02	5.0	10	3.0	100	1.0	2.0	±15	±40	High Voltage	G/601, U
MC1556	0.015	4.0	10	2.0	100	1.0	2.5	±3.0	±22	High Performance	G/601, 693, U
MC1733	0.20	—	—	3.0 μA	90	90	—	±4.0	±8.0	Differential Wideband Video Amp	G/603, L
MC1741	0.5	5.0	15	200	50	1.0	0.5	±3.0	±22	General Purpose	G/601, U
MC1741S	0.5	5.0	15	200	50	1.0	10	±3.0	±22	High Slew Rate	G/601, U
MC1776	0.0075	5.0	15	3.0	200	1.0	0.2	±1.2	±18	μPower, Programmable	G/601, L
MC35001	100 pA	10	10	100 pA	25	4.0	13	±5.0	±22	JFET Input	G/601, U
MC35001A	75 pA	2.0	10	25 pA	50	4.0	13	±5.0	±22	JFET Input	G/601, U
MC35001B	100 pA	5.0	10	50 pA	50	4.0	13	±5.0	±22	JFET Input	G/601, U
MC35071	0.50	5.0	10	75	25	4.5	10	+3.0	+44	High Performance,	U
MC35071A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	Single Supply	U
MC35080	200 pA	1.0	10	100 pA	25	16	55	±5.0	±22	Decompensated	U
MC35080A	200 pA	0.5	10	100 pA	50	16	55	±5.0	±22	MC35081 for $A_V \geq 2$	U
MC35081	200 pA	1.0	10	100 pA	25	8.0	30	±5.0	±22	High Speed, JFET Input	U
MC35081A	200 pA	0.5	10	100 pA	50	8.0	30	±5.0	±22	High Speed, JFET Input	U
MC35171	0.10	4.5	10	20	50	1.8	2.1	+3.0	+44	Low Power, Single Supply	U
MC35181	0.1 nA	2.0	10	0.05	25	4.0	10	±2.5	±18	Low Power JFET Input	U
OP-27A	0.040	0.025	0.2	35	1000	8.0	2.8	±4.0	±22	Low Noise, Precision	Z
OP-27B	0.055	0.060	0.3	50	1000	8.0	2.8	±4.0	±22	Low Noise, Precision	Z
OP-27C	0.080	0.100	0.4	75	700	8.0	2.8	±4.0	±22	Low Noise, Precision	Z
TL061M	200 pA	6.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power JFET Input	JG
TL071M	200 pA	6.0	10	50 pA	35	4.0	13	±5.0	±18	Low Noise, JFET Input	JG
TL081M	200 pA	9.0	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	JG

Dual Operational Amplifiers

Device	I_{IB} μA Max	V_{IO} mV Max	TC_{VIO} μV/°C Typ	I_{IO} nA Max	A_{vol} V/mV Min	BW (A_V=1) MHz Typ	SR (A_V=1) V/μs Typ	Supply Voltage V Min	Supply Voltage V Max	Description	Package Suffix
Noncompensated											
Commercial Temperature Range (0°C to +70°C)											
MC1437	1.5	7.5	10	500	15	1.0	0.25	±3.0	±18	Dual MC1709	L, P/646
Military Temperature Range (−55°C to +125°C)											
MC1537	0.5	5.0	10	200	25	1.0	0.25	±3.0	±18	Dual MC1709	L
Internally Compensated											
Commercial Temperature Range (0°C to +70°C)											
LF353	200 pA	10	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	N/626
LF442C	100 pA	5.0	10	50 pA	25	2.0	6.0	±5.0	±18	Low Power JFET Input	N/626
LM358	0.25	6.0	7.0	50	25	1.0	0.6	±1.5 +3.0	±18 +36	Single Supply (Low Power Consumption)	H, N/626, J/693
LM833	1.0	5.0	2.0	200	31.6	15	7.0	±2.5	±18	Dual, Low Noise, Audio	P/626
MC1458	0.5	6.0	10	200	20	1.1	0.8	±3.0	±18	Dual MC1741	G/601, P1, U
MC1458C	0.70	10	10	300	20	1.1	0.8	±3.0	±18	Dual General Purpose	G/601, P1
MC1458S	0.5	6.0	10	200	20	1.0	10	±3.0	±18	High Slew Rate	G/601, P1, U
MC1747C	0.5	6.0	10	200	25	1.0	0.5	±3.0	±18	Dual MC1741	G/603, L, P2
MC3458	0.5	10	7.0	50	20	1.0	0.6	±1.5 +3.0	±18 +36	Split Supplies Single Supply (Low Crossover Distortion)	G/601, P1, U

Dual Operational Amplifiers (continued)

Device	I_{IB} μA Max	V_{IO} mV Max	TC_{VIO} μV/°C Typ	I_{IO} nA Max	A_{vol} V/mV Min	BW (A_V=1) MHz Typ	SR (A_V=1) V/μs Typ	Supply Voltage V Min	Supply Voltage V Max	Description	Package Suffix
Commercial Temperature Range (0°C to +70°C) (continued)											
MC4558AC	0.5	5.0	10	200	50	2.8	1.6	±3.0	±22	High Frequency	P1
MC4558C	0.5	6.0	10	200	20	2.8	1.6	±3.0	±18	High Frequency	G/601, P1, U
MC34002	100 pA	10	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	G/601, P/626, U
MC34002A	75 pA	2.0	10	50 pA	50	4.0	13	±5.0	±18	JFET Input	G/601, P/626, U
MC34002B	100 pA	5.0	10	70 pA	25	4.0	13	±5.0	±18	JFET Input	G/601, P/626, U
MC34072	0.50	5.0	10	75	25	4.5	10	+3.0	+44	High Performance,	P/626, U
MC34072A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	Single Supply	P/626, U
MC34082	200 pA	3.0	10	100 pA	25	8.0	30	±5.0	±22	High Speed, JFET Input	P/626, U
MC34082A	200 pA	1.0	10	100 pA	50	8.0	30	±5.0	±22	High Speed, JFET Input	P/626, U
MC34083	200 pA	3.0	10	100 pA	25	16	55	±5.0	±22	Decompensated	P/626, U
MC34083A	200 pA	1.0	10	100 pA	50	16	55	±5.0	±22	MC34082 for $A_V \geq 2$	P/626, U
MC34182	0.1 nA	3.0	10	0.05	25	4.0	10	±2.5	±18	Low Power JFET Input	P/626
TL062AC	200 pA	6.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power JFET Input	P/626
TL062BC	200 pA	3.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power JFET Input	P/626
TL062C	200 pA	15	10	200 pA	4.0	2.0	6.0	±2.5	±18	Low Power JFET Input	P/626
TL072AC	200 pA	6.0	10	50 pA	50	4.0	13	±5.0	±18	Low Noise, JFET Input	P/626, JG/693
TL072BC	200 pA	3.0	10	50 pA	50	4.0	13	±5.0	±18	Low Noise, JFET Input	P/626, JG/693
TL072C	200 pA	10	10	50 pA	25	4.0	13	±5.0	±18	Low Noise, JFET Input	P/626, JG/693
TL082AC	200 pA	6.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	P/626, JG/693
TL082BC	200 pA	3.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	P/626, JG/693
TL082C	400 pA	15	10	200 pA	25	4.0	13	±5.0	±18	JFET Input	P/626, JG/693
Industrial Temperature Range (−25°C to +85°C)											
LM258	0.15	5.0	10	30	50	1.0	0.6	±1.5	±18	Split or Single	H, N/626, J/693
								±3.0	±36	Supply Op Amp	
Automotive Temperature Range (−40°C to +85°C)											
LM2904	0.25	7.0	7.0	50	100 typ	1.0	0.6	±1.5	±13	Split or Single	H, N/626, J/693
								±3.0	±26	Supply Op Amp	
MC3358	5.0	8.0	10	75	20	1.0	0.6	±1.5	±18	Split Supplies	P1/626
								±3.0	±36	Single Supply	
MC33072	0.50	5.0	10	75	25	4.5	10	+3.0	+44	High Performance,	P/626, U
MC33072A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	Single Supply	P/626, U
MC33077	1.0	1.0	2.0	180	150	37	11	±2.5	±18	Dual, Low Noise	P/626
MC33078	750 nA	2.0	2.0	150	31.6	16	7.0	±5.0	±18	Low Noise	N/626
MC33172	0.10	4.5	10	20	50	1.8	2.1	+3.0	+44	Low Power, Single Supply	P/626
MC33182	0.1 nA	3.0	10	0.05	25	4.0	10	±2.5	±18	Low Power JFET Input	P/626
MC33282	100 pA	200μV	5.0	50 pA	50	30	12	±2.5	±18	Low Input Offset JFET	P/646
TL062V	200 pA	6.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power JFET Input	P/626
Military Temperature Range (−55°C to +125°C)											
LM158	0.15	5.0	10	30	50	1.0	0.6	±1.5	±18	Split Supplies	H, J/693
								+3.0	+36	Single Supply (Low Power Consumption)	
MC1558	0.5	5.0	10	200	50	1.1	0.8	±3.0	±22	Dual MC1741	G/601, U
MC1558S	0.5	5.0	10	200	50	1.0	10	±3.0	±22	High Slew Rate	G/601, U
MC1747	0.5	5.0	10	200	50	1.0	0.5	±3.0	±22	Dual MC1741	G/601, L
MC3558	0.5	5.0	10	50	50	1.0	0.6	±1.5	±18	Split Supplies	G/601, U
								+3.0	+36	Single Supply	
MC4558	0.5	5.0	10	200	50	2.8	1.6	±3.0	±22	High Frequency	G/601, U
MC35002	100 pA	10	10	100 pA	25	4.0	13	±5.0	±22	JFET Input	G/601, U
MC35002A	75 pA	2.0	10	25 pA	50	4.0	13	±5.0	±22	JFET Input	G/601, U
MC35002B	100 pA	5.0	10	50 pA	50	4.0	13	±5.0	±22	JFET Input	G/601, U
MC35072	0.50	5.0	10	75	25	4.5	10	+3.0	+44	High Performance,	U
MC35072A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	Single Supply	U
MC35082	200 pA	3.0	10	100 pA	25	8.0	30	±5.0	±22	High Speed, JFET Input	U
MC35082A	200 pA	1.0	10	100 pA	50	8.0	30	±5.0	±22	High Speed, JFET Input	U

Dual Operational Amplifiers (continued)

Device	I_{IB} μA Max	V_{IO} mV Max	TC_{VIO} μV/°C Typ	I_{IO} nA Max	A_{vol} V/mV Min	BW (A_V=1) MHz Typ	SR (A_V=1) V/μs Typ	Supply Voltage V Min	Supply Voltage V Max	Description	Package Suffix
Military Temperature Range (−55°C to +125°C)											
MC35083	200 pA	3.0	10	100 pA	25	16	55	±5.0	±22	Decompensated	U
MC35083A	200 pA	1.0	10	100 pA	50	16	55	±5.0	±22	MC35082 for $A_V \geq 2$	U
MC35172	0.10	4.5	10	20	50	1.8	2.1	+3.0	+44	Low Power, Single Supply	U
MC35182	0.1 nA	3.0	10	0.05	25	4.0	10	±2.5	±18	Low Power JFET Input	U
TL062M	200 pA	6.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power JFET Input	JG
TL072M	200 pA	6.0	10	50 pA	35	4.0	13	±5.0	±18	Low Noise, JFET Input	JG
TL082M	200 pA	6.0	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	JG

Quad Operational Amplifiers

Device	I_{IB} μA Max	V_{IO} mV Max	TC_{VIO} μV/°C Typ	I_{IO} nA Max	A_{vol} V/mV Min	BW (A_V=1) MHz Typ	SR (A_V=1) V/μs Typ	Supply Voltage V Min	Supply Voltage V Max	Description	Package Suffix
Internally Compensated											
Commercial Temperature Range (0°C to +70°C)											
LF347	200 pA	10	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	N/646
LF347B	200 pA	5.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	N/646
LF444C	100 pA	10	10	50 pA	25	2.0	6.0	±5.0	±18	Low Power JFET Input	N/646
LM324	0.25	6.0	7.0	50	25	1.0	0.6	±1.5	±16	Low Power	J/632, N/646
								+3.0	+32	Consumption	
LM348	0.20	6.0	—	50	25	1.0	0.5	±3.0	±18	Quad MC1741	J/632, N/646
MC3401/ LM3900	0.3	—	—	—	1.0	5.0	0.6	±1.5	±18	Norton Input	J/632, N/646
								+3.0	+36		
MC3403	0.5	10	7.0	50	20	1.0	0.6	±1.5	±18	No Crossover	L, P/646
								+3.0	+36	Distortion	
MC4741C	0.5	6.0	15	200	20	1.0	0.5	±3.0	±18	Quad MC1741	L, P/646
MC34004	200 pA	10	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	L, P/646
MC34004B	200 pA	5.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	L, P/646
MC34074	0.50	5.0	10	75	25	4.5	10	+3.0	+44	High Performance,	L, P/646
MC34074A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	Single Supply	L, P/646
MC34084	200 pA	12	10	100 pA	25	8.0	30	±5.0	±22	Hi-Speed, JFET Input	P/646
MC34084A	200 pA	6.0	10	100 pA	50	8.0	30	±5.0	±22	Hi-Speed, JFET Input	P/646
MC34085	200 pA	12	10	100 pA	25	16	55	±5.0	±22	Decompensated	P/646
MC34085A	200 pA	6.0	10	100 pA	50	16	55	±5.0	±22	MC34084 for $A_V \geq 2$	P/646
MC34184	0.1 nA	10	10	0.05	25	4.0	10	±2.5	±18	Low Power JFET Input	P/646
TL064AC	200 pA	6.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power JFET Input	N/646
TL064BC	200 pA	3.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power JFET Input	N/646
TL064C	200 pA	15	10	200 pA	4.0	2.0	6.0	±2.5	±18	Low Power JFET Input	N/646
TL074AC	200 pA	6.0	10	50 pA	50	4.0	13	±5.0	±18	Low Noise, JFET Input	J/632, N/646
TL074C	200 pA	10	10	50 pA	25	4.0	13	±5.0	±18	Low Noise, JFET Input	J/632, N/646
TL084AC	200 pA	6.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	J/632, N/646
TL084BC	200 pA	3.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	J/632, N/646
TL084C	400 pA	15	10	200 pA	25	4.0	13	±5.0	±18	JFET Input	J/632, N/646
Industrial Temperature Range (−25°C to +85°C)											
LM224	0.15	5.0	7.0	30	50	1.0	0.6	±1.5	±16	Split or Single	J/632, N/646
								±3.0	±32	Supply OP Amp	
LM248	0.20	6.0	—	50	25	1.0	0.5	±3.0	±18	Quad MC1741	J/632, N/646
Automotive Temperature Range (−40°C to +85°C)											
LM2902	0.5	10	—	50	—	1.0	0.6	±1.5	±13	Differential	N/646
								+3.0	+26	Low Power	

Quad Operational Amplifiers (continued)

Device	I_{IB} μA Max	V_{IO} mV Max	TC_{VIO} μV/°C Typ	I_{IO} nA Max	A_{vol} V/mV Min	BW (A_V=1) MHz Typ	SR (A_V=1) V/μs Typ	Supply Voltage V Min	Supply Voltage V Max	Description	Package Suffix
Automotive Temperature Range (−40°C to +85°C) (continued)											
MC3301/ LM2900	0.3	—	—	—	1.0	4.0	0.6	±2.0 +4.0	±15 +28	Norton Input	P/646 N/646
MC3303	0.5	8.0	10	75	20	1.0	0.6	±1.5 +3.0	±18 +36	Differential General Purpose	P/646
MC33074	0.50	5.0	10	75	25	4.5	10	+3.0	+44	High Performance, Single Supply	L, P/646
MC33074A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	Quad High Performance	L, P/646
MC33079	750 nA	2.5	2.0	150	31.6	16	7.0	±5.0	±18	Quad Low Noise	N/646
MC33174	0.10	4.5	10	20	50	1.8	2.1	+3.0	+44	Low Power, Single Supply	P/646
MC33184	0.1 nA	10	10	0.05	25	4.0	10	±2.5	±18	Low Power JFET Input	P/646
MC33284	100pA	200μV	5.0	50pA	50	30	12	±2.5	±18	Low Input Offset JFET	P/646
TL064V	200 pA	9.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power JFET Input	N/646
Telecommunications Temperature Range (−40°C to +85°C)											
MC143403	1.0 nA	30	—	200 pA	45 dB	0.8	1.5	4.75	12.6	CMOS, Low Power, Drives Low-Impedance Loads	L, P/646
MC143404	1.0 nA	30	—	200 pA	60 dB	0.8	1.0	4.75	12.6	CMOS, Very Low Power	L, P/646
Military Temperature Range (−55°C to +125°C)											
LM124	0.15	5.0	7.0	30	50	1.0	0.6	±1.5 +3.0	±16 +32	Low Power Consumption	J/632, N/646
LM148	0.10	5.0	—	25	50	1.0	0.5	±3.0	±18	Quad MC1741	J/632
MC3503	0.5	5.0	7.0	50	50	1.0	0.6	±1.5 +3.0	±18 +36	General Purpose Low Power	L, P/646
MC4741	0.5	5.0	15	200	50	1.0	0.5	±3.0	±22	Quad MC1741	L
MC35004	100 pA	10	10	100 pA	25	4.0	13	±5.0	±22	JFET Input	L
MC35004B	100 pA	5.0	10	50 pA	50	4.0	13	±5.0	±22	JFET Input	L
MC35074	0.50	5.0	10	75	25	4.5	10	+3.0	+44	High Performance, Single Supply	L
MC35074A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	Quad High Performance	L
MC35084	200 pA	12	10	100 pA	25	8.0	30	±5.0	±22	High Speed, JFET Input	L
MC35084A	200 pA	6.0	10	100 pA	50	8.0	30	±5.0	±22	High Speed, JFET Input	L
MC35085	200 pA	12	10	100 pA	25	16	55	±5.0	±22	Decompensated	L
MC35085A	200 pA	6.0	10	100 pA	50	16	55	±5.0	±22	MC35084 for $A_V \geq 2$	L
MC35174	0.10	4.5	10	20	50	1.8	2.1	+3.0	+44	Low Power, Single Supply	L
MC35184	0.1 nA	10	10	0.05	25	4.0	10	±2.5	±18	Low Power JFET Input	L
TL064M	200 pA	9.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power JFET Input	J/632
TL074M	200 pA	9.0	10	50 pA	35	4.0	13	±5.0	±18	Low Noise, JFET Input	J/632
TL084M	200 pA	9.0	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	J/632

High Frequency Amplifiers

A variety of high frequency circuits with features ranging from low cost simplicity to multi-function versatility marks Motorola's line of integrated amplifiers. Devices described here are intended for industrial and communications applications. For devices especially dedicated to consumer products, i.e., TV and entertainment radio, see the "Consumer Electronics" section.

AGC Amplifiers

MC1590G Family — Wide-Band General Purpose Amplifiers

The MC1590G, MC1490, MC1350 family are basic building blocks — AGC (Automatic Gain Controlled) RF/Video Amplifiers. These parts are recommended for applications up through 70 MHz. The best high frequency performance may be obtained by using the physically smaller SOIC version (shorter leads) — MC1350D. There are currently no other RF IC's like these, because other manufacturers have dropped their copies. Applications include variable gain video and instrumentation amplifiers, IF (Intermediate Frequency) amplifiers for radio and TV receivers, and transmitter power output control. Many uses will be found in medical instrumentation, remote monitoring, video/graphics processing, and a variety of communications equipment. The family of parts using the same basic die (identical circuit with slightly different test parameters) is listed in the following table.

MC1545/1445 — Gated 2-Channel Input

Differential input and output amplifier with gated 2-channel input for a wide variety of switching purposes. Typical 50 MHz bandwidth makes it suitable for high frequency applications such as video switching, FSK circuits, multiplexers, etc. Gating circuit is useful for AGC control.

Non-AGC Amplifiers

SE/NE592 — Differential Two Stage Video Amplifier

A monolithic, two stage differential output, wideband video amplifier. It offers fixed gains of 100 and 400 without external components and adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high pass, low pass, or band pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display and video recorder systems.

MC1733/MC1733C — Video Amplifier

Differential input and output amplifier provides three fixed gain options with bandwidth to 120 MHz. External resistor permits any gain setting from 10 to 400 V/V. Extremely fast rise time (2.5 ns typ) and propagation delay time (3.6 ns typ) makes this unit particularly useful as pulse amplifier in tape, drum, or disc memory read applications.

High-Frequency Amplifier Specifications

Operating Temperature Range			A_V dB	Bandwidth @ MHz	V_{CC}/V_{EE} Vdc		
−55° to +125°C	−40° to +85°C	0° to +70°C	(Typ)		Min	Max	Case/Suffix
MC1590G	—	—	50 35	10 100	+6.0	+18	601
—	—	MC1350	50 50	45 45	+6.0	+18	626/P, 751/D
—	MC1490	—	50 35	10 100	+6.0	+18	626/P
MC1545	—	MC1445	19	50	±4.0	±12	603/G, 632/L
SE592	—	NE592	52 40	40 90	±4.0	±8.0	603/H, 632/F 646/N
MC1733	—	MC1733C	52 40 20	40 90 120	±4.0	±8.0	603/G, 632/L 646/P

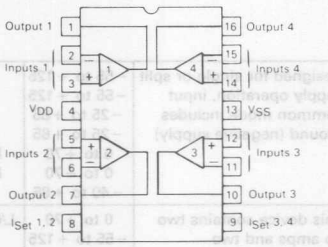
Miscellaneous Amplifiers

Motorola provides several bipolar and CMOS special purpose amplifiers which fill specific needs. These devices range from low power CMOS programmable amplifiers and comparators to variable-gain bipolar power amplifiers.

CMOS

MC14573: Quad Programmable Operational Amplifier
MC14574: Quad Programmable Comparator
MC14575: Dual Programmable Operational Amplifier and Dual Programmable Comparator

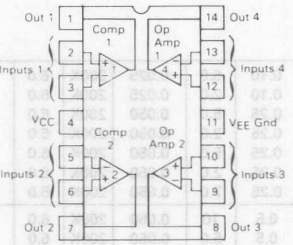
These low power devices are designed for applications such as active filters, voltage reference circuits, function generators, oscillators, and limit set alarms.



Bipolar

MC3505/MC3405: Dual Operational Amplifier and Dual Comparator

This device contains two Differential Input Operational Amplifiers and two Comparators each set capable of single supply operation. This operational amplifier-comparator circuit will find its applications as a general purpose product for automotive circuits and as an industrial "building block."



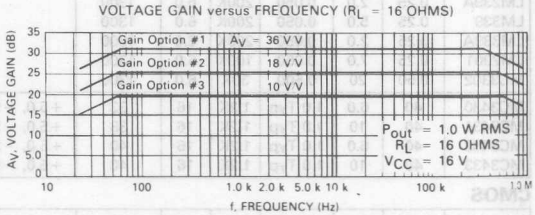
Device	I_{IB} μA Max	V_{IO} mV Max	I_{IO} nA Max	A_{vol} V/mV Min	Response μs Typ	Supply Voltage Single	Supply Voltage Dual	Package Suffix
Bipolar								
MC3505	0.5	5.0	50	20	1.3	3.0 to 36	±1.5 to ±18	L/632
MC3405		10						L/632, P/646
CMOS								
MC14573	50 pA	±30	100 pA	1.0	10*	3.0 to 15	±1.5 to ±7.5	D/751F, P/648
MC14574								
MC14575								

*Propagation Delay

Power Amplifiers Variable Gain

MC1554G—T_A = −55° to +125°C, Case 603C
MC1454G—T_A = 0° to +70°C, Case 603C

One-watt Power Amplifier for single or split supply operation. Typical voltage gain of 10, 18, or 33 V/V with 0.4% THD.



Comparators

Single

BIPOLAR

Device	I_{IB} μA Max	V_{IO} mV Max	I_{IO} μA Max	A_V V/V Typ	I_O mA Min	Response Time ns	Supply Voltage V	Description	Temperature Range (°C)	Package Suffix
LM111	0.10	3.0	0.01	200K	8.0	200	+15, −15	With strobe, will operate from single supply	−55 to +125	H, J-8
LM211	0.10	3.0	0.01	200K	8.0	200	+15, −15		−25 to +85	H, J-8
LM311	0.25	7.5	0.05	200K	8.0	200	+15, −15		0 to +70	H, N/626, J-8

CMOS

MC14578	1.0 pA	50	—	—	1.1	—	+3.5 to +14	Requires only 10 μA from single-ended supply	−30 to +70	D/751B, P/648

Dual

BIPOLAR

LM193	0.10	5.0	0.025	200K	6.0	1300	±1.5 to	Designed for single or split	−55 to +125	H
LM193A	0.10	2.0	0.025	200K	6.0	1300	±18 or	supply operation, input	−55 to +125	H
LM293	0.25	5.0	0.050	200K	6.0	1300	+3.0 to +36	common mode includes	−25 to +85	H
LM293A	0.25	2.0	0.050	200K	6.0	1300		ground (negative supply)	−25 to +85	H
LM393	0.25	5.0	0.050	200K	6.0	1300			0 to +70	H, N/626
LM393A	0.25	2.0	0.050	200K	6.0	1300			0 to +70	H, N/626
LM2903	0.25	7.0	0.050	200K	6.0	1500			−40 to +85	N/626
MC3405	0.5	10	0.050	200K	6.0	1300	±1.5 to	This device contains two	0 to +70	L/632, P/646
MC3505	0.5	5.0	0.050	200K	6.0	1300	±7.5 or +3.0 to 15	op amps and two comparators in a single package	−55 to +125	L/632

CMOS

MC14575	0.001	30	0.0001	20K	3.0	1000	±1.5 to ±7.5 or +3.0 to 15	This device contains two op amps and two comparators in a single package	−40 to +85	P/648

Quad

BIPOLAR

LM139	0.10	5.0	0.025	200K	6.0	1300	±1.5 to	Designed for single or split	−55 to +125	J
LM139A	0.10	2.0	0.025	200K	6.0	1300	±18 or	supply operation, input	−55 to +125	J
LM239	0.25	5.0	0.050	200K	6.0	1300	+3.0 to +36	common mode includes	−25 to +85	J, N/646
LM239A	0.25	2.0	0.050	200K	6.0	1300		ground (negative supply)	−25 to +85	J, N/646
LM339	0.25	5.0	0.050	200K	6.0	1300			0 to +70	J, N/646
LM339A	0.25	2.0	0.050	200K	6.0	1300			0 to +70	J, N/646
LM2901	0.25	7.0	0.050	100K	6.0	1300			−40 to +85	N/646
MC3302	0.50	20	0.500	30K	6.0	1300			−40 to +85	N/646
MC3430	40	6.0	1.0 Typ	1.2K	16	33	+5.0, −5.0	High speed comparator/	0 to +70	L, P
MC3431	40	10	1.0 Typ	1.2K	16	33	+5.0, −5.0	sense-amplifier	0 to +70	L, P
MC3432	40	6.0	1.0 Typ	1.2K	16	40	+5.0, −5.0		0 to +70	L, P
MC3433	40	10	1.0 Typ	1.2K	16	40	+5.0, −5.0		0 to +70	L, P

CMOS

MC14574	0.001	30	0.0001	20K	3.0	10000	±1.5 to ±7.5 or +3.0 to +15	Externally programmable power dissipation with one or two resistors	−40 to +85	L/620

OPERATIONAL AMPLIFIERS

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MC35081	High Speed JFET Input Operational Amplifier	2-302
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MC35083	Dual High Speed Decompensated ($A_{VCL} \geq 2$) JFET Input Operational Amplifier	2-302
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2

HIGH FREQUENCY AMPLIFIERS

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RELATED APPLICATION NOTES

Application Note	Title	Related Device
AN926, AR115	Techniques for Improving the Settling of a DAC and Op. Amp. Combination	**LF357, MC34084, MC34085, MC34087**
AN273A	Getting More Value Out of an Int. Op. Amp. Data Sheet	**MC1439, 1539**
AN513A	A High Gain Int. Circuit RF-IF Amp. with Wide Range AGC	**MC1490P, MC1590G**
AN587, EB20	Analysis and Design of the Op. Amp. Current Source	**MC1741**
EB57	An Economical FM Trans. Voice Proc. from a Single Integrated Circuit	**MC3401**

MOTOROLA

LF347
LF351
LF353

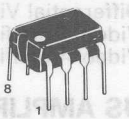
FAMILY OF BIFET OPERATIONAL AMPLIFIERS
SILICON MONOLITHIC INTEGRATED CIRCUITS

JFET INPUT OPERATIONAL AMPLIFIERS

These low cost JFET input operational amplifiers combine two state-of-the-art linear technologies on a single monolithic integrated circuit. Each internally compensated operational amplifier has well matched high voltage JFET input devices for low input offset voltage. The BIFET technology provides wide bandwidths and fast slew rates with low input bias currents, input offset currents, and supply currents.

These devices are available in single, dual and quad operational amplifiers which are pin-compatible with the industry standard MC1741, MC1458, and the MC3403/LM324 bipolar devices.

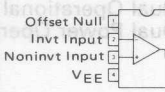
- Input Offset Voltage of 5.0 mV Max (LF347B)
- Low Input Bias Current – 50 pA
- Low Input Noise Voltage – 16 nV/$\sqrt{Hz}$
- Wide Gain Bandwidth – 4.0 MHz
- High Slew Rate – 13 V/μs
- Low Supply Current – 1.8 mA per Amplifier
- High Input Impedance – 10^{12} Ω
- High Common-Mode and Supply Voltage Rejection Ratios – 100 dB



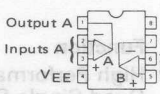
N SUFFIX
PLASTIC PACKAGE
CASE 626-05
(LF351, LF353 Only)

D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SO-8
(LF351, LF353 Only)

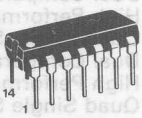




LF351
(Top View)



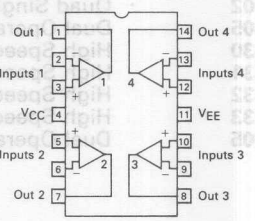
LF353
(Top View)



N SUFFIX
PLASTIC PACKAGE
CASE 646-06
(LF347 Only)

D SUFFIX
PLASTIC PACKAGE
CASE 751A-02
SO-14





(Top View)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC} V_{EE}	+18 −18	V
Differential Input Voltage	V_{ID}	±30	V
Input Voltage Range (Note 1)	V_{IDR}	±15	V
Output Short Circuit Duration (Note 2)	t_S	Continuous	
Power Dissipation at T_A = + 25°C	P_D	900	mW
Derate above T_A = +25°C	$1/\theta JA$	10	mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Operating Junction Temperature Range	T_J	115	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

NOTES:

1. Unless otherwise specified, the absolute maximum negative input voltage is limited to the negative power supply.

2. Any amplifier output can be shorted to ground indefinitely. However, if more than one amplifier output is shorted simultaneously, maximum junction temperature ratings may be exceeded.

ORDERING INFORMATION

Function	Device	Package
Single	LF351D	SO-8
Single	LF351N	Plastic DIP
Dual	LF353D	SO-8
Dual	LF353N	Plastic DIP
Quad	LF347D	SO-14
Quad	LF347BN	Plastic DIP
Quad	LF347N	Plastic DIP

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C unless otherwise noted).

Characteristic	Symbol	LF347B			LF347, LF351, LF353			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq$ 10 k, V_{CM} = 0) T_A = +25°C 0°C ≤ T_A ≤ +70°C	V_{IO}	 — —	 1.0 —	 5.0 8.0	 — —	 5.0 —	 10 13	mV
Average Temperature Coefficient of Input Offset Voltage $R_S \leq$ 10 k, 0°C ≤ T_A ≤ +70°C	$\Delta V_{IO}/\Delta T$	—	10	—	—	10	—	μV/°C
Input Offset Current (V_{CM} = 0, Note 3) T_A = +25°C 0°C ≤ T_A ≤ +70°C	I_{IO}	 — —	 25 —	 100 4.0	 — —	 25 —	 100 4.0	 pA nA
Input Bias Current (V_{CM} = 0, Note 3) T_A = +25°C 0°C ≤ T_A ≤ +70°C	I_{IB}	 — —	 50 —	 200 8.0	 — —	 50 —	 200 8.0	 pA nA
Input Resistance	r_i	—	10^{12}	—	—	10^{12}	—	Ω
Common Mode Input Voltage Range	V_{ICR}	±11	+15 −12	—	±11	+15 −12	—	V
Large-Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 k) T_A = +25°C 0°C ≤ T_A ≤ +70°C	A_{VOL}	 50 25	 100 —	 — —	 25 15	 100 —	 — —	V/mV
Output Voltage Swing (R_L = 10 k)	V_O	±12	±14	—	±12	±14	—	V
Common Mode Rejection Ratio ($R_S \leq$ 10 k)	CMRR	80	100	—	70	100	—	dB
Supply Voltage Rejection Ratio ($R_S \leq$ 10 k)	PSRR	80	100	—	70	100	—	dB
Supply Current LF347 LF351 LF353	I_D	 — — —	 7.2 — —	 11 — —	 — — —	 7.2 1.8 3.6	 11 3.4 6.5	mA
Slew Rate (A_V = +1)	SR	—	13	—	—	13	—	V/μs
Gain-Bandwidth Product	BWp	—	4.0	—	—	4.0	—	MHz
Equivalent Input Noise Voltage (R_S = 100 Ω, f = 1000 Hz)	e_n	—	16	—	—	16	—	nV/√Hz
Equivalent Input Noise Current (f = 1000 Hz)	i_n	—	0.01	—	—	0.01	—	pA/√Hz
Channel Separation (LF347, LF353) 1.0 Hz ≤ f ≤ 20 kHz (Input Referred)	—	—	−120	—	—	−120	—	dB

For Typical Characteristic Performance Curves, refer to MC34001/34002/34004 data sheet.

NOTES: (continued)

3. Input bias currents of JFET input op amps approximately double for every 10°C rise in junction temperature. To maintain junction temperatures as close to ambient as is possible, pulse techniques are utilized during test.

MOTOROLA

LF355, LF356, LF357* LF355B, LF356B, LF357B*

Specifications and Applications Information

MONOLITHIC JFET INPUT OPERATIONAL AMPLIFIERS

These internally compensated operational amplifiers incorporate highly matched JFET devices on the same chip with standard bipolar transistors. The JFET devices enhance the input characteristics of these operational amplifiers by more than an order of magnitude over conventional amplifiers.

This series of op amps combines the low current characteristics typical of FET amplifiers with the low initial offset voltage and offset voltage stability of bipolar amplifiers. Also, nulling the offset voltage does not degrade the drift or common mode rejection.

- Low Input Bias Current – 30 pA
- Low Input Offset Current – 3.0 pA
- Low Input Offset Voltage – 1.0 mV
- Temperature Compensation of Input Offset Voltage – 3.0 $\mu V/^{o}C$
- Low Input Noise Current – 0.01 $pA/\sqrt{Hz}$
- High Input Impedance – $10^{12}\Omega$
- High Common-Mode Rejection Ratio – 100 dB
- High DC Voltage Gain – 106 dB

SERIES FEATURES

- LF355/355B — Low Power Supply Current
- LF356/356B — Wide Bandwidth
- LF357/357B — **Wider** Bandwidth Decompensated (A_{Vmin} = 5)

	LF355/355B	LF356/356B	LF357/357B
Fast Settling Time to 0.01%	4.0 μs	1.5 μs	1.5 μs
Fast Slew Rate	5.0 $V/\mu s$	12 $V/\mu s$	50 $V/\mu s$
Wide Gain Bandwidth	2.5 MHz	5.0 MHz	20 MHz
Low Input Noise Voltage	20 $nV/\sqrt{Hz}$	12 $nV/\sqrt{Hz}$	12 $nV/\sqrt{Hz}$

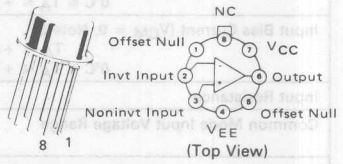
ORDERING INFORMATION

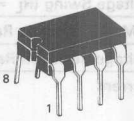
Device	Temperature Range	Package
LF355BH,H LF355BJ,J	0 to +70°C 0 to +70°C	Metal Can Ceramic DIP
LF356BH,H LF356BJ,J	0 to +70°C 0 to +70°C	Metal Can Ceramic DIP
LF357BH,H LF357BJ,J	0 to +70°C 0 to +70°C	Metal Can Ceramic DIP

MONOLITHIC JFET OPERATIONAL AMPLIFIERS

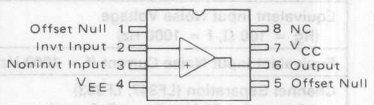
SILICON MONOLITHIC INTEGRATED CIRCUITS

H SUFFIX
METAL PACKAGE
CASE 601-04





J SUFFIX
CERAMIC PACKAGE
CASE 693-02



APPLICATIONS

The LF series is suggested for all general purpose FET input amplifier requirements where precision and frequency response flexibility are of prime importance.

Specific applications include:

- Sample and Hold Circuits
- High Impedance Buffers
- Fast D/A and A/D Converters
- Precision High Speed Integrators
- Wideband, Low Noise, Low Drift Amplifiers

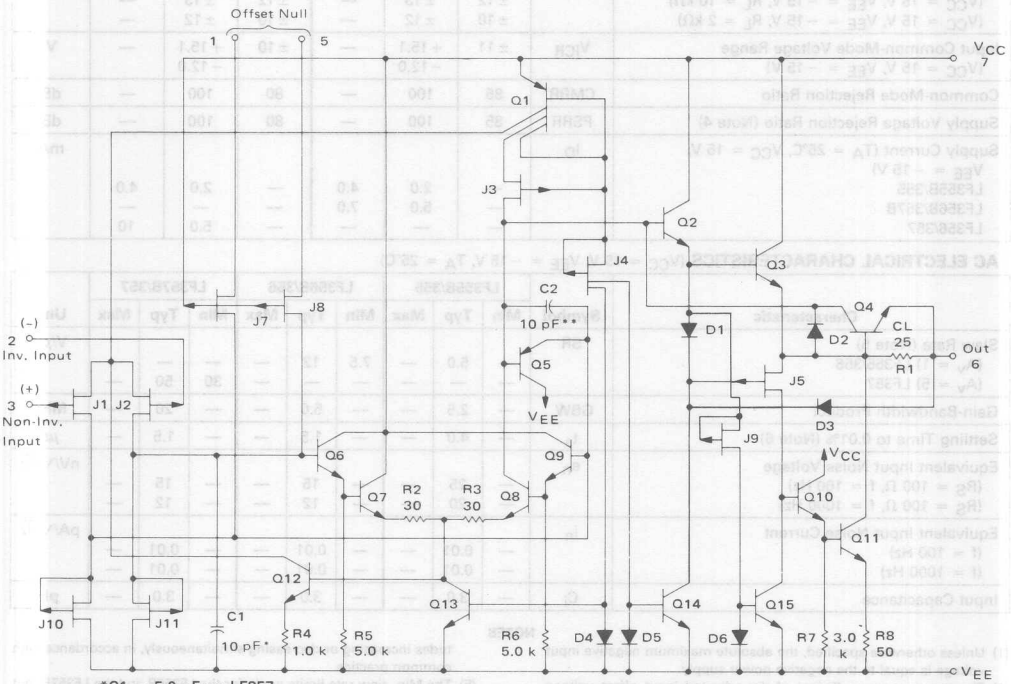
***NOTE:** The LF357/357B are designed for wider bandwidth applications. They are decompensated (A_{Vmin} = 5).

MAXIMUM RATINGS

Rating	Symbol	LF355B/ 356B/357B	LF355/356/357	Unit
Supply Voltage	V_{CC} V_{EE}	+22 −22	+18 −18	V
Differential Input Voltage	V_{ID}	±40	±30	V
Input Voltage Range (Note 1)	V_{IDR}	±20	±16	V
Output Short-Circuit Duration	T_S	Continuous		-
Operating Ambient Temperature Range	T_A	0 to +70		°C
Operating Junction Temperature	T_J	115		°C
Storage Temperature Range	T_{stg}	−65 to +150		°C

Note 1. Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

CIRCUIT SCHEMATIC



*C1 = 5.0 pF on LF357.
**C2 = 2.0 pF on LF357.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 15 to 20 V, V_{EE} = −15 to −20 V for LF355B/356B/357B; V_{CC} = 15 V, V_{EE} = −15 V for LF355/356/357; T_A = 0°C to +70°C unless otherwise noted)

Characteristic	Symbol	LF355B/6B/7B			LF355/6/7			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (R_S = 50 Ω, V_{CM} = 0)	V_{IO}							mV
(T_A = 25°C)		—	3.0	5.0	—	3.0	10	
(Over Temperature)		—	—	6.5	—	—	13	
Average Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω)	$\Delta V_{IO}/\Delta T$	—	5.0	—	—	5.0	—	μV/°C
Change in Average TC with V_{IO} Adjust (R_S = 50 Ω) (Note 2)	$\Delta TC/\Delta V_{IO}$	—	0.5	—	—	0.5	—	μV/°C per mV
Input Offset Current (V_{CM} = 0) (Note 3)	I_{IO}							
(T_J = 25°C)		—	3.0	20	—	3.0	50	pA
($T_J \leq$ 70°C)		—	—	1.0	—	—	2.0	nA
Input Bias Current (V_{CM} = 0) (Note 3)	I_{IB}							
(T_J = 25°C)		—	30	100	—	30	200	pA
($T_J \leq$ 70°C)		—	—	5.0	—	—	8.0	nA
Input Resistance (T_J = 25°C)	r_i	—	10^{12}	—	—	10^{12}	—	Ω
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 k, V_{CC} = 15 V, V_{EE} = −15 V)	A_{VOL}							V/mV
(T_A = 25°C)		50	200	—	25	200	—	
(0°C ≤ T_A ≤ +70°C)		25	—	—	15	—	—	
Output Voltage Swing	V_O							V
(V_{CC} = 15 V, V_{EE} = −15 V, R_L = 10 kΩ)		±12	±13	—	±12	±13	—	
(V_{CC} = 15 V, V_{EE} = −15 V, R_L = 2 kΩ)		±10	±12	—	±10	±12	—	
Input Common-Mode Voltage Range (V_{CC} = 15 V, V_{EE} = −15 V)	V_{ICR}	±11	+15.1 −12.0	—	±10	+15.1 −12.0	—	V
Common-Mode Rejection Ratio	CMRR	85	100	—	80	100	—	dB
Supply Voltage Rejection Ratio (Note 4)	PSRR	85	100	—	80	100	—	dB
Supply Current (T_A = 25°C, V_{CC} = 15 V, V_{EE} = −15 V)	I_D							mA
LF355B/355		—	2.0	4.0	—	2.0	4.0	
LF356B/357B		—	5.0	7.0	—	—	—	
LF356/357		—	—	—	—	5.0	10	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, V_{EE} = −15 V, T_A = 25°C)

Characteristic	Symbol	LF355B/355			LF356B/356			LF357B/357			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Slew Rate (Note 5)	SR										V/μs
(A_V = 1) LF355/356		—	5.0	—	7.5	12	—	—	—	—	
(A_V = 5) LF357		—	—	—	—	—	—	30	50	—	
Gain-Bandwidth Product	GBW	—	2.5	—	—	5.0	—	—	20	—	MHz
Settling Time to 0.01% (Note 6)	t_s	—	4.0	—	—	1.5	—	—	1.5	—	μs
Equivalent Input Noise Voltage	e_n										nV/√Hz
(R_S = 100 Ω, f = 100 Hz)		—	25	—	—	15	—	—	15	—	
(R_S = 100 Ω, f = 1000 Hz)		—	20	—	—	12	—	—	12	—	
Equivalent Input Noise Current	i_n										pA/√Hz
(f = 100 Hz)		—	0.01	—	—	0.01	—	—	0.01	—	
(f = 1000 Hz)		—	0.01	—	—	0.01	—	—	0.01	—	
Input Capacitance	C_i	—	3.0	—	—	3.0	—	—	3.0	—	pF

NOTES

(1) Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply.

(2) The temperature coefficient of the adjusted input offset voltage changes only a small amount (0.5 μV/°C typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.

(3) The input bias currents approximately double for every 10°C rise in junction temperature, T_J. Due to limited test time, the input bias currents are correlated to junction temperature. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

(4) Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

(5) The Min. slew rate limits apply for the LF356B and the LF357B, but do not apply for the LF356 or LF357.

(6) Settling time is defined here, for a unity gain inverter connection using 2.0 k resistors for the LF355/6. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10 V step input is applied to the inverter. For the LF357, A_V = −5.0, the feedback resistor from output to input is 2.0 k and the output step is 10 V (see settling time test circuit).

TYPICAL DC PERFORMANCE CHARACTERISTICS
(Curves are for LF355, LF356, and LF357 series unless otherwise specified)

INPUT BIAS CURRENT versus CASE TEMPERATURE

FIGURE 1 — (LF355 SERIES)

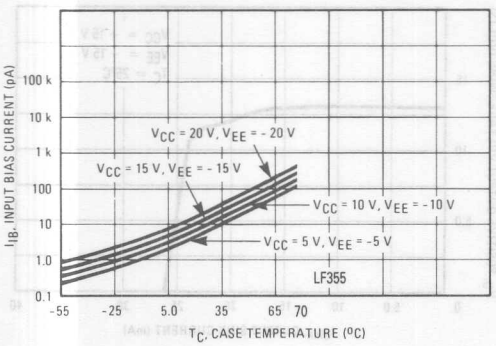


FIGURE 2 — (LF356 AND LF357 SERIES)

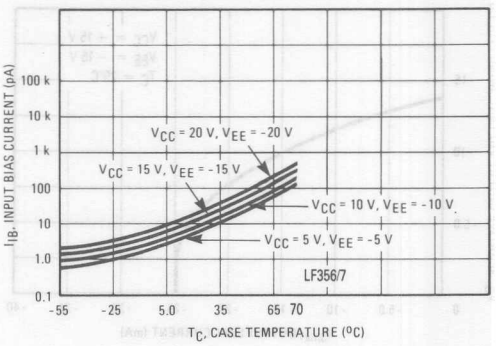


FIGURE 3 — INPUT BIAS CURRENT versus INPUT COMMON-MODE VOLTAGE

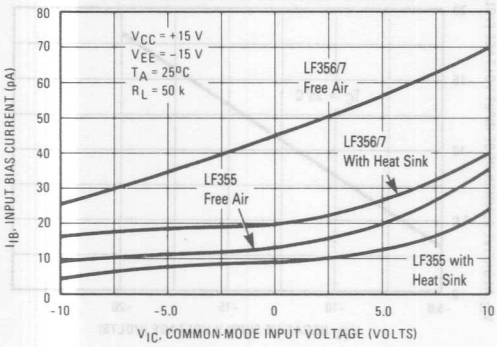
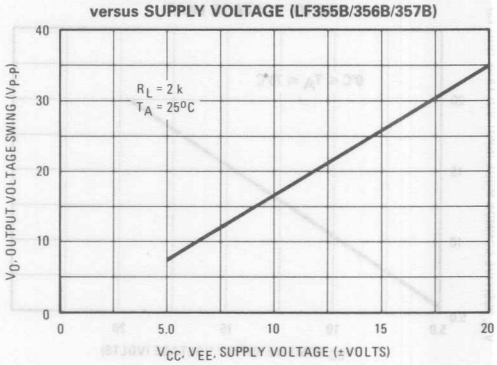


FIGURE 4 — OUTPUT VOLTAGE SWING versus SUPPLY VOLTAGE (LF355B/356B/357B)



SUPPLY CURRENT versus SUPPLY VOLTAGE

FIGURE 5 — (LF355 SERIES)

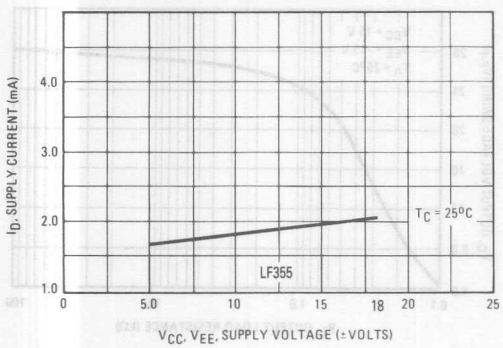
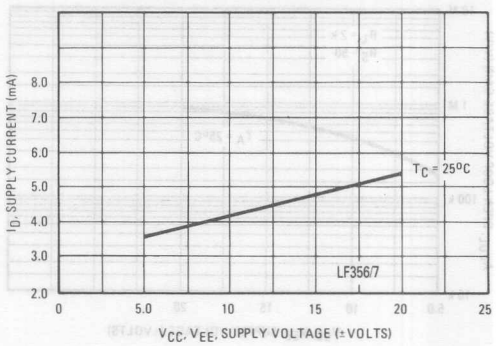


FIGURE 6 — (LF356 AND LF357 SERIES)



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TYPICAL DC PERFORMANCE CHARACTERISTICS (continued)

FIGURE 7 — NEGATIVE CURRENT LIMIT

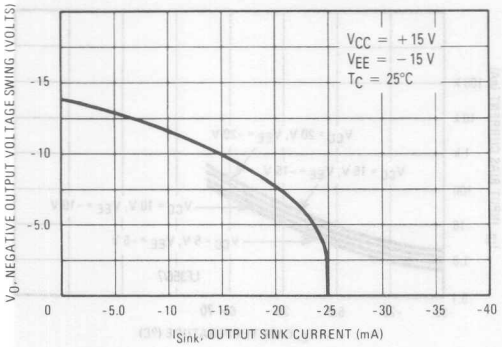


FIGURE 8 — POSITIVE CURRENT LIMIT

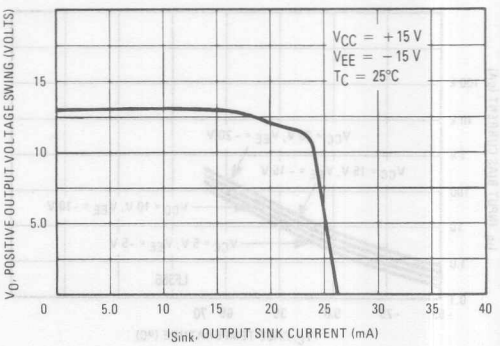


FIGURE 9 — POSITIVE COMMON-MODE INPUT VOLTAGE LIMIT

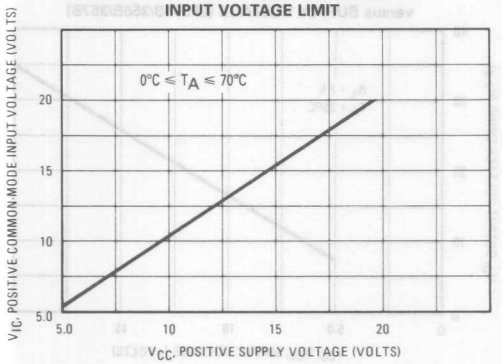


FIGURE 10 — NEGATIVE COMMON-MODE INPUT VOLTAGE LIMIT

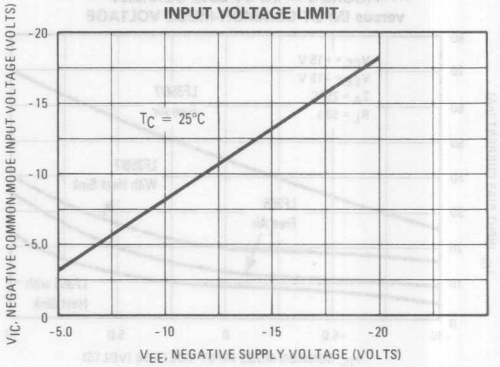


FIGURE 11 — OPEN LOOP VOLTAGE GAIN

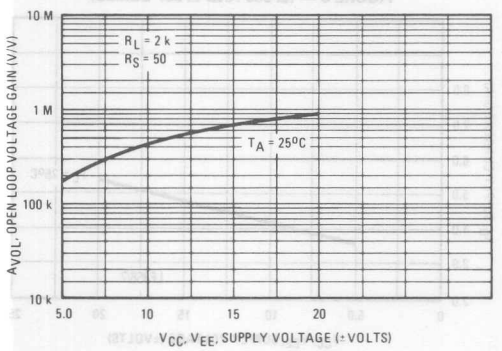
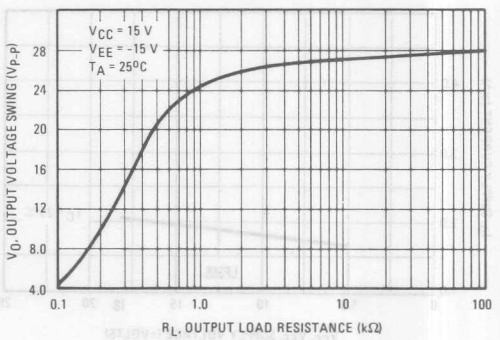


FIGURE 12 — OUTPUT VOLTAGE SWING versus LOAD RESISTANCE



TYPICAL AC PERFORMANCE CHARACTERISTICS

GAIN BANDWIDTH PRODUCT

FIGURE 13 — (LF355 SERIES)

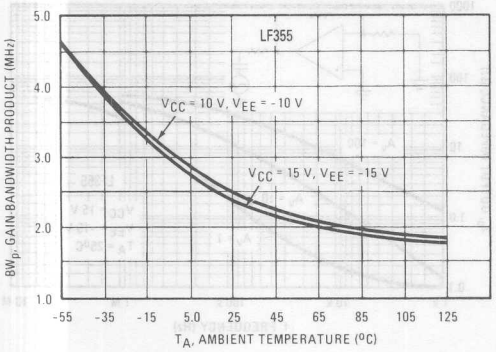
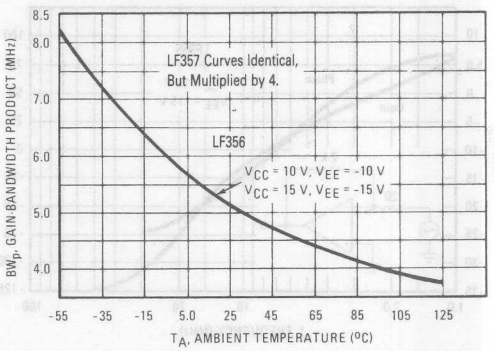


FIGURE 14 — (LF356/357 SERIES)



INVERTER SETTLING TIME

FIGURE 15 — (LF355 SERIES)

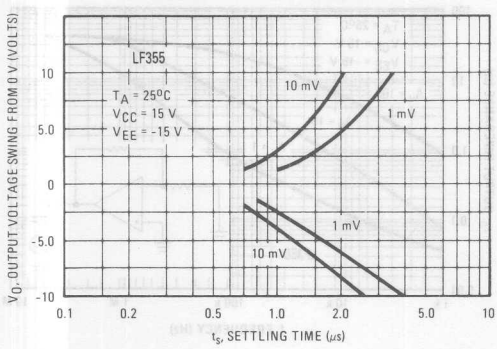


FIGURE 16 — (LF356 AND LF357 SERIES)

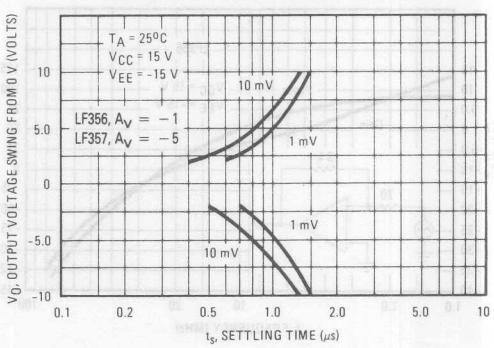


FIGURE 17 — NORMALIZED SLEW RATE

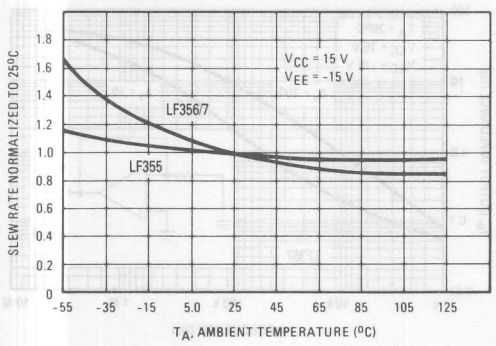
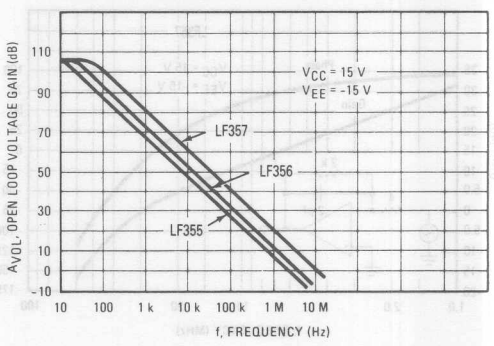


FIGURE 18 — OPEN LOOP FREQUENCY RESPONSE



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TYPICAL AC PERFORMANCE CHARACTERISTICS (continued)

BODE PLOT

FIGURE 19 — (LF355 SERIES)

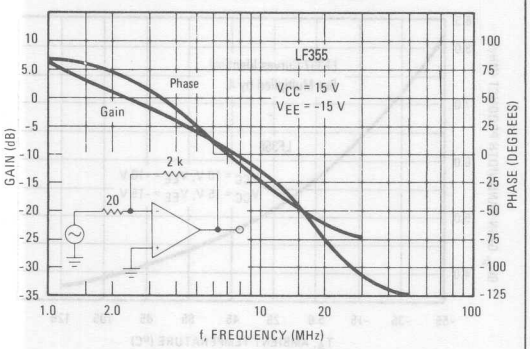


FIGURE 20 — (LF356 SERIES)

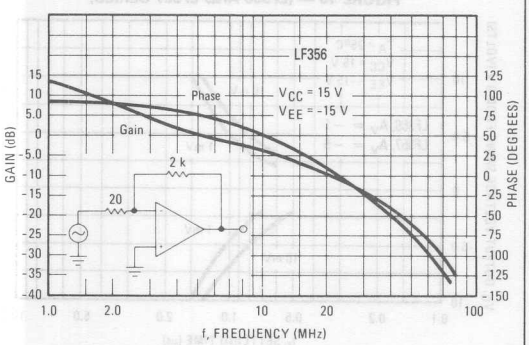
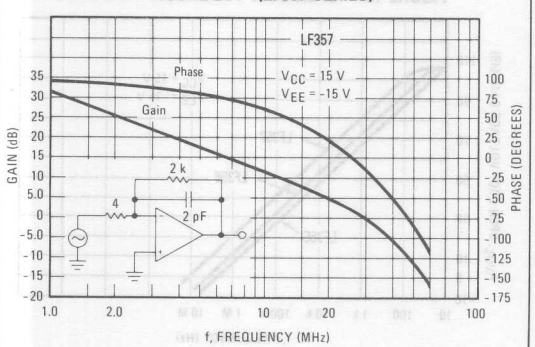


FIGURE 21 — (LF357 SERIES)



OUTPUT IMPEDANCE

FIGURE 22 — (LF355 SERIES)

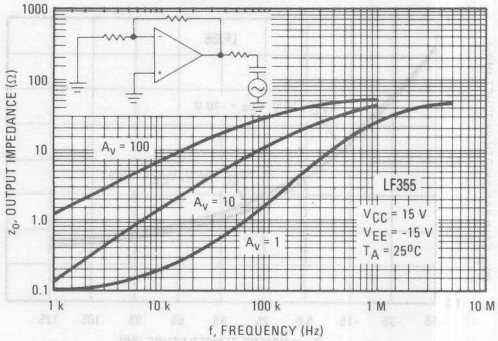


FIGURE 23 — (LF356 SERIES)

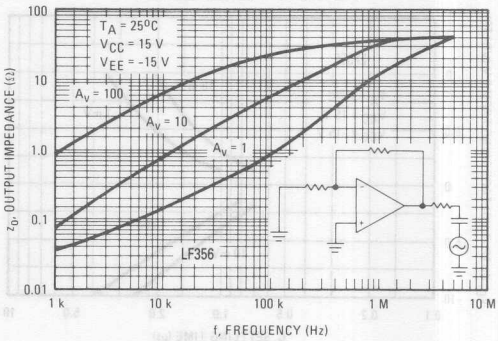
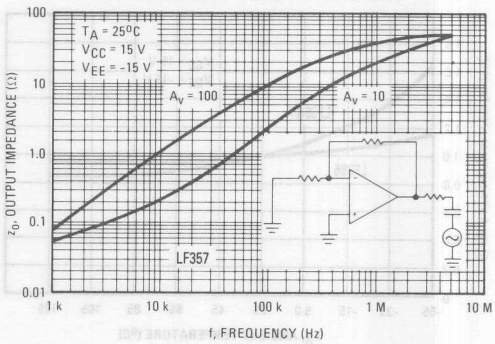


FIGURE 24 — (LF357 SERIES)



TYPICAL AC PERFORMANCE CHARACTERISTICS (continued)

FIGURE 25 — COMMON-MODE REJECTION RATIO

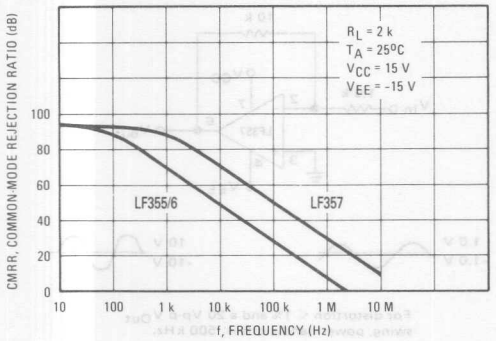
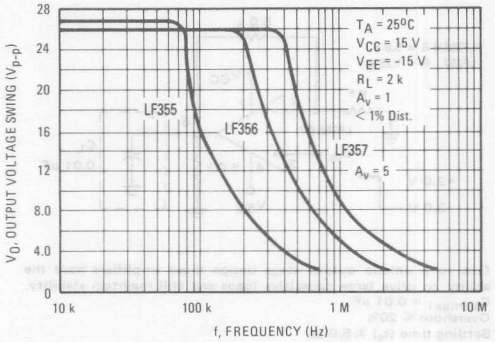


FIGURE 26 — UNDISTORTED OUTPUT VOLTAGE SWING



POWER SUPPLY VOLTAGE REJECTION RATIO

FIGURE 27 — (LF355 SERIES)

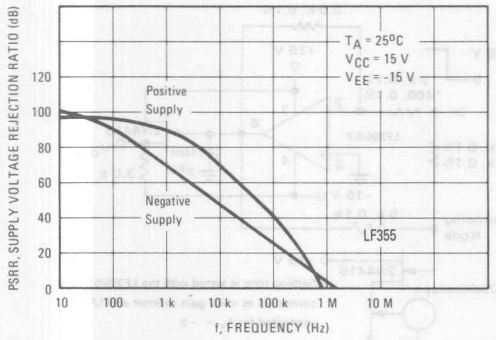
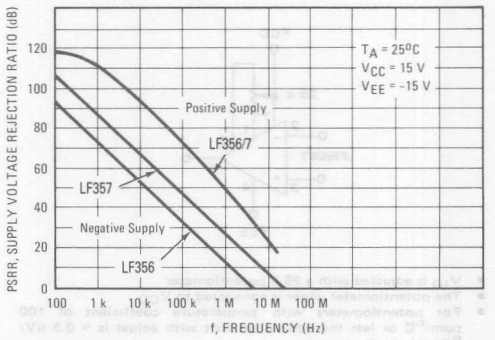


FIGURE 28 — (LF356 AND LF357 SERIES)



EQUIVALENT NOISE VOLTAGE

FIGURE 29 — (LF355/356/357 SERIES)

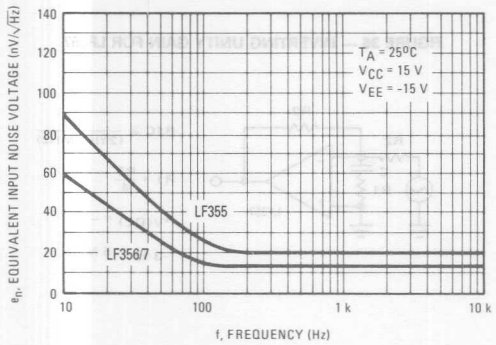
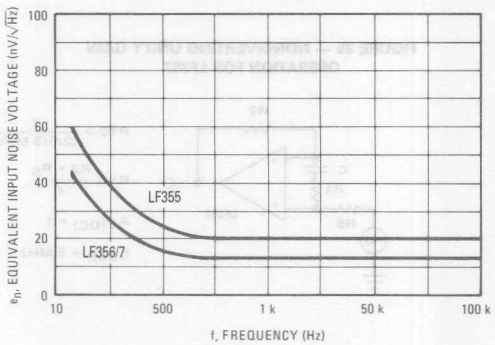


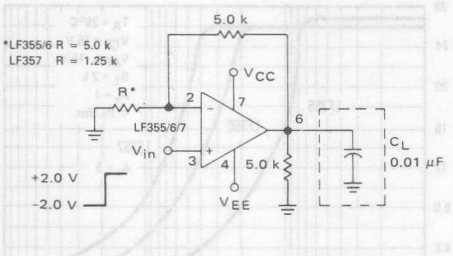
FIGURE 30 (EXPANDED SCALE)



2

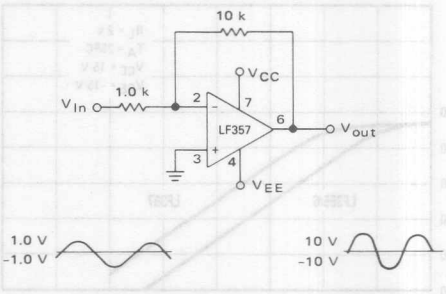
TYPICAL CIRCUIT CONNECTIONS

FIGURE 31 — DRIVING CAPACITIVE LOADS



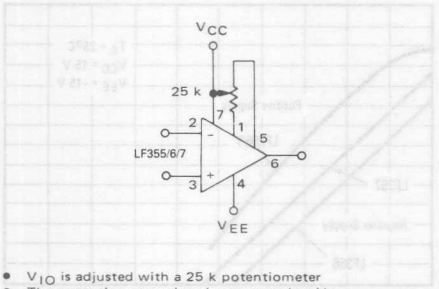
Due to a unique output stage design these amplifiers have the ability to drive large capacitive loads and still maintain stability.
$C_{L(max)} \cong 0.01\ \mu F$.
Overshoot $\leq 20\%$
Settling time (t_s) $\cong 5.0\ \mu s$

FIGURE 32 — LARGE POWER BANDWIDTH AMPLIFIER



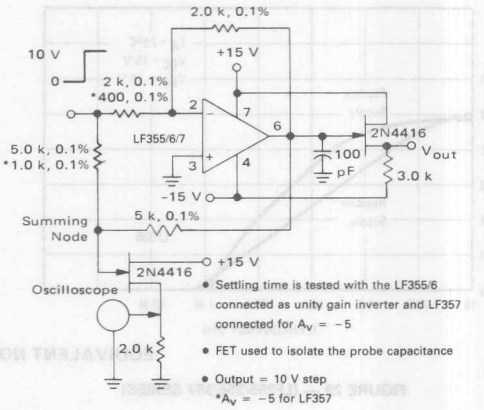
For distortion < 1% and a 20 Vp-p V_{Out} swing, power bandwidth is: 500 kHz.

FIGURE 33 — INPUT OFFSET VOLTAGE ADJUSTMENT



- V_{IO} is adjusted with a 25 k potentiometer
- The potentiometer wiper is connected to V_{CC}
- For potentiometers with temperature coefficient of 100 ppm/°C or less the additional drift with adjust is $\approx 0.5\ \mu V/°C/mV$ of adjustment.
- Typical overall drift: 5.0 μV/°C ±(0.5 μV/°C/mV of adjustment.)

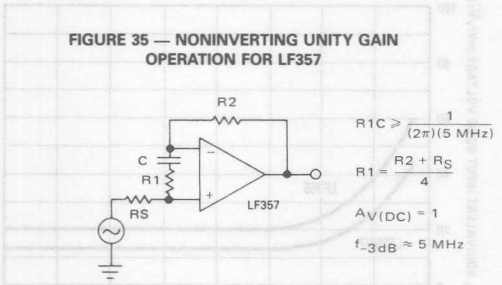
FIGURE 34 — SETTLING TIME TEST CIRCUIT



- Settling time is tested with the LF355/6 connected as unity gain inverter and LF357 connected for $A_V = -5$
- FET used to isolate the probe capacitance
- Output = 10 V step

*$A_V = -5$ for LF357

FIGURE 35 — NONINVERTING UNITY GAIN OPERATION FOR LF357



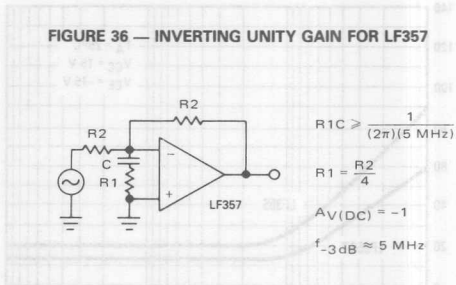
$$R1C \geq \frac{1}{(2\pi)(5\ MHz)}$$

$$R1 = \frac{R2 + R_S}{4}$$

$$A_{V(DC)} = 1$$

$$f_{-3dB} \approx 5\ MHz$$

FIGURE 36 — INVERTING UNITY GAIN FOR LF357



$$R1C \geq \frac{1}{(2\pi)(5\ MHz)}$$

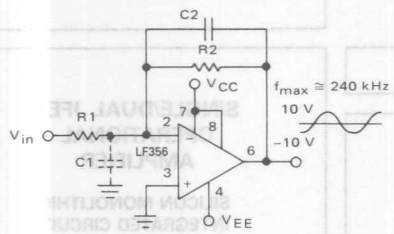
$$R1 = \frac{R2}{4}$$

$$A_{V(DC)} = -1$$

$$f_{-3dB} \approx 5\ MHz$$

TYPICAL APPLICATIONS

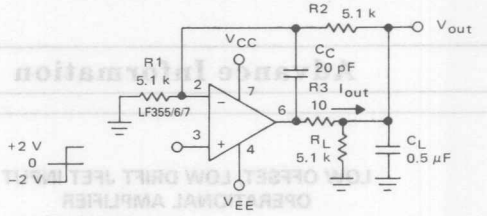
FIGURE 37 — WIDE BW, LOW NOISE, LOW DRIFT AMPLIFIER



- Power BW: $f_{max} = \frac{S_r}{2\pi V_p} \cong 240$ kHz

- Parasitic input capacitance (C1 ≅ 3 pF for LF355, LF356, and LF357 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate add C2 such that: R2C2 ≅ R1C1.

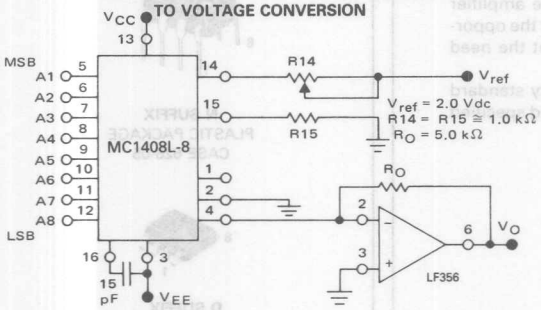
FIGURE 38 — ISOLATING LARGE CAPACITIVE LOADS



- Overshoot 6%
- t_s = 10 μs
- When driving large C_L, the V_{out} slew rate is determined by C_L and $I_{out(max)}$:

$$\frac{\Delta V_{out}}{\Delta t} = \frac{I_{out}}{C_L} \cong \frac{0.02}{0.5} \text{ V/μs} = 0.04 \text{ V/μs (with } C_L \text{ shown)}$$

FIGURE 39 — 8-BIT D/A WITH OUTPUT CURRENT TO VOLTAGE CONVERSION



Theoretical V_O

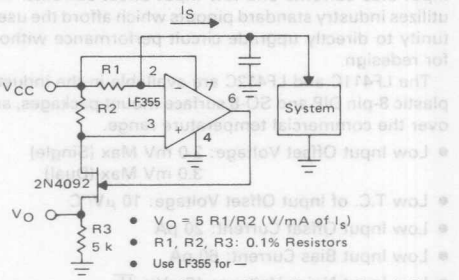
$$V_O = \frac{V_{ref}}{R14}(R_O)\left\{\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right\}$$

Adjust V_{ref}, R14 or R_O so that V_O with all digital inputs at high level is equal to 9.961 volts.

$$V_O = \frac{2V}{1\text{ k}}(5\text{ k})\left\{\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} + \frac{1}{256}\right\}$$

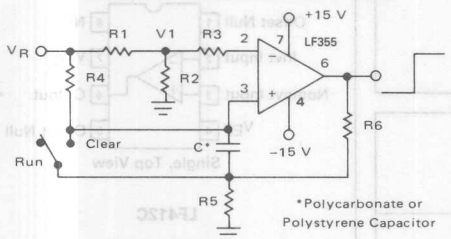
$$= 10\text{ V}\left\{\frac{255}{256}\right\} = 9.961\text{ V}$$

FIGURE 40 — PRECISION CURRENT MONITOR



- V_O = 5 R1/R2 (V/mA of I_s)
- R1, R2, R3: 0.1% Resistors
- Use LF355 for —
  - ▲ Common-Mode Range to Supply Range
  - ▲ Low I_{IB}
  - ▲ Low V_{IO}
  - ▲ Low Supply Current

FIGURE 41 — LONG INTERVAL RC TIMER



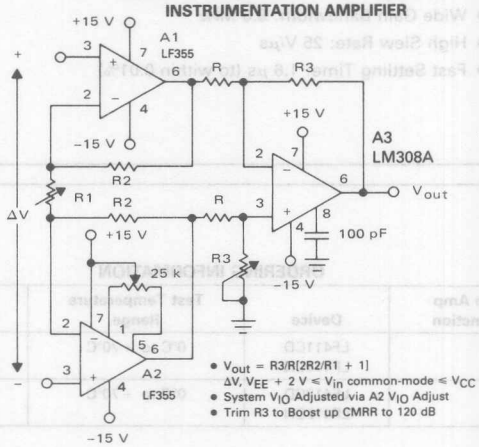
Time (τ) = R4Cℓn($V_R/V_R - V_1$), $R_3 = R_4$, $R_5 = 0.1$ R6

If R1 = R2: t = 0.693 R4C

Design Example: 100 Second Timer

V_R = 10 V	C = 1 μF	R3 = R4 = 144 M
R6 = 20 k	R5 = 2 k	R1 = R2 = 1 k

FIGURE 42 — HIGH IMPEDANCE, LOW DRIFT INSTRUMENTATION AMPLIFIER



- V_{out} = R3/R[2R2/R1 + 1]
  ΔV, V_{EE} + 2 V ≤ V_{in} common-mode ≤ V_{CC}
- System V_{IO} Adjusted via A2 V_{IO} Adjust
- Trim R3 to Boost up CMRR to 120 dB

MOTOROLA

LF411C
LF412C

Advance Information

SINGLE/DUAL JFET OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

LOW OFFSET, LOW DRIFT JFET INPUT OPERATIONAL AMPLIFIER

Through innovative design concepts and precision matching this monolithic high speed JFET input operational amplifier family offers very low input offset voltage as well as low temperature coefficient of input offset voltage. The amplifier requires less than 3.4 mA per amplifier of supply current yet exhibits greater than 2.7 MHz of gain bandwidth product and more than 8.0 V/μs slew rate. Through the use of JFET inputs the amplifier has very low input bias currents and low input offset currents. The amplifier utilizes industry standard pinouts which afford the user the opportunity to directly upgrade circuit performance without the need for redesign.

The LF411C and LF412C are available in the industry standard plastic 8-pin DIP and SO-8 surface mount packages, and specified over the commercial temperature range.

- Low Input Offset Voltage: 2.0 mV Max (Single)
  3.0 mV Max (Dual)
- Low T.C. of Input Offset Voltage: 10 μV/°C
- Low Input Offset Current: 20 pA
- Low Input Bias Current: 60 pA
- Low Input Noise Voltage: 18 nV/$\sqrt{Hz}$
- Low Input Noise Current: 0.01 pA/$\sqrt{Hz}$
- Low Total Harmonic Distortion: 0.05%
- Low Supply Current: 2.5 mA
- High Input Resistance: 10^{12} Ω
- Wide Gain Bandwidth: 8.0 MHz
- High Slew Rate: 25 V/μs
- Fast Settling Time: 1.6 μs (to within 0.01%)

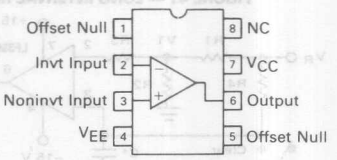


N SUFFIX
PLASTIC PACKAGE
CASE 626-05



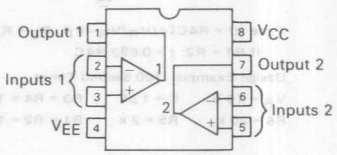
D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SO-8

LF411C



Single, Top View

LF412C



(Dual, Top View)

ORDERING INFORMATION

Op Amp Function	Device	Test Temperature Range	Package
Single	LF411CD LF411CN	0°C to +70°C	SO-8 Plastic DIP
Dual	LF412CD LF412CN	0°C to +70°C	SO-8 Plastic DIP

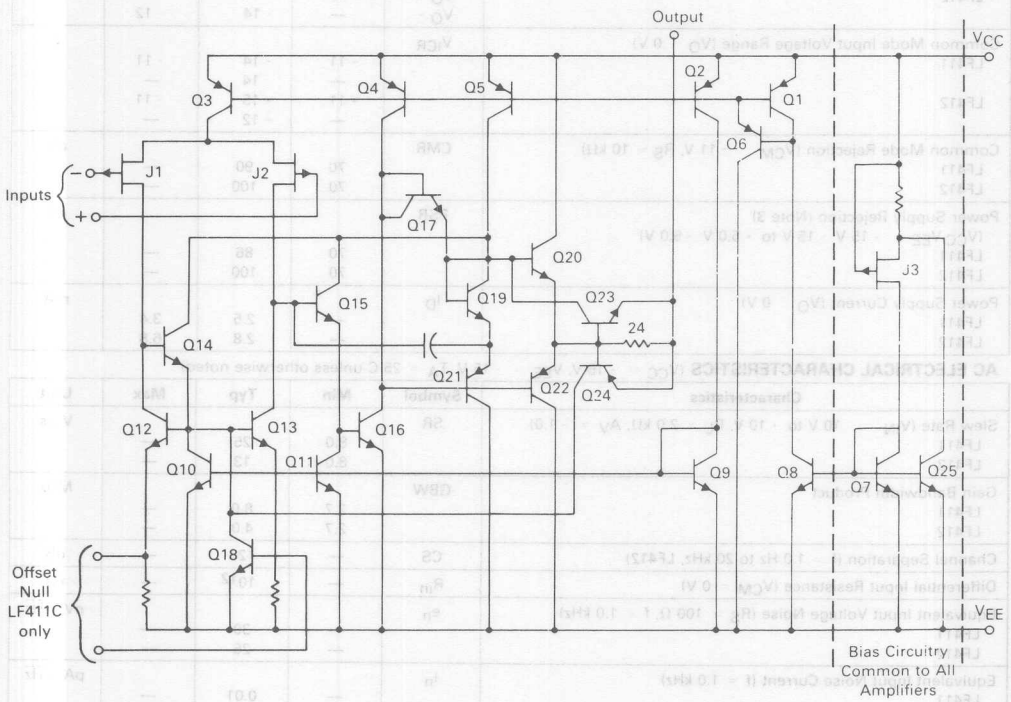
This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Supply Voltages		V_{CC}, $\|V_{EE}\|$	+18	Volts
Input Differential Voltage Range (Note 1)		V_{IDR}	±30	Volts
Input Voltage Range (Note 1)		V_{IR}	±15	Volts
Output Short-Circuit Duration (Note 2)		t_S	Indefinite	Seconds
Maximum Junction Temperature		T_J	+150	C
Operating Ambient Temperature Range		T_A	0 to 70	C
Thermal Resistance (Junction to Ambient)	LF411CN 412CN LF411CD 412CD	$R_{\theta JA}$	100 180	C Watt
Storage Temperature		T_{stg}	−60 to +150	C
Maximum Power Dissipation		P_D	(Note 2)	mW

NOTES:
1. Input voltages should not exceed V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded.
3. Measured with V_{CC} and V_{EE} simultaneously varied.

REPRESENTATIVE CIRCUIT SCHEMATIC
(Each Amplifier)



Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 10 kΩ, V_{CM} = 0 V, V_O = 0 V)	V_{IO}				mV
LF411		—	0.5	2.0	
LF412		—	1.0	3.0	
Average Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$				μV/°C
(R_S = 10 kΩ, V_{CM} = 0 V, V_O = 0 V)		—	10	—	
Input Offset Current (V_{CM} = 0 V, V_O = 0 V)	I_{IO}				
LF411 T_A = 25°C		—	20	100	pA
T_A = 0°C to 70°C		—	—	2.0	nA
LF412 T_A = 25°C		—	25	100	pA
T_A = 0°C to 70°C		—	—	2.0	nA
Input Bias Current (V_{CM} = 0 V)	I_{IB}				
LF411 T_A = 25°C		—	0.6	200	pA
T_A = 0°C to 70°C		—	—	4.0	nA
LF412 T_A = 25°C		—	0.5	200	pA
T_A = 0°C to 70°C		—	—	4.0	nA
Large Signal Voltage Gain (V_O = ± 10 V, R_L = 2.0 kΩ)	A_{VOL}				V/mV
LF411 T_A = 25 C		25	80	—	
T_A = 0 C to 70 C		15	—	—	
LF412 T_A = 25 C		25	150	—	
T_A = 0 C to 70 C		15	—	—	
Output Voltage Swing (V_{ID} = ± 1.0 V, R_L = 10 kΩ)					V
LF411	V_O +	12	13.9	—	
	V_O −	—	− 14.7	− 12	
LF412	V_O +	12	14	—	
	V_O −	—	14	− 12	
Common Mode Input Voltage Range (V_O = 0 V)	V_{ICR}				V
LF411		− 11	− 14	− 11	
		—	14	—	
LF412		− 11	+ 15	− 11	
		—	− 12	—	
Common Mode Rejection (V_{CM} = ± 11 V, R_S = 10 kΩ)	CMR				dB
LF411		70	90	—	
LF412		70	100	—	
Power Supply Rejection (Note 3)	PSR				dB
(V_{CC}/V_{EE} = − 15 V/ 15 V to + 5.0 V/ − 5.0 V)					
LF411		70	86	—	
LF412		70	100	—	
Power Supply Current (V_O = 0 V)	I_D				mA
LF411		—	2.5	3.4	
LF412		—	2.8	6.8	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = + 15 V, V_{EE} = − 15 V, T_A = 25 C unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{IN} = − 10 V to + 10 V, R_L = 2.0 kΩ, A_V = + 1.0)	SR				V/μs
LF411		8.0	25	—	
LF412		8.0	13	—	
Gain Bandwidth Product	GBW				MHz
LF411		2.7	8.0	—	
LF412		2.7	4.0	—	
Channel Separation (f = 1.0 Hz to 20 kHz, LF412)	CS	—	− 120	—	dB
Differential Input Resistance (V_{CM} = 0 V)	R_{in}	—	10^{12}	—	kΩ
Equivalent Input Voltage Noise (R_S = 100 Ω, f = 1.0 kHz)	e_n				nV/√Hz
LF411		—	30	—	
LF412		—	25	—	
Equivalent Input Noise Current (f = 1.0 kHz)	i_n				pA/√Hz
LF411		—	0.01	—	
LF412		—	0.01	—	

LF441C
LF442C
LF444C

LOW POWER JFET INPUT OPERATIONAL AMPLIFIER

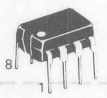
These JFET input operational amplifiers are designed for low power applications. They feature high input impedance, low input bias current and low input offset current. Advanced design techniques allow for higher slew rates, gain bandwidth products and output swing. The LF441C device provides for the external null adjustment of input offset voltage.

These devices are specified over the commercial temperature range. All are available in plastic dual in-line and SOIC packages.

- Low Supply Current — 200 μA/Amplifier
- Low Input Bias Current — 5.0 pA
- High Gain Bandwidth — 2.0 MHz
- High Slew Rate — 6.0 V/μs
- High Input Impedance — 10^{12} Ω
- Large Output Voltage Swing — ± 14 V
- Output Short Circuit Protection

LOW POWER JFET INPUT OPERATIONAL AMPLIFIERS

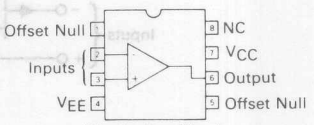
SILICON MONOLITHIC INTEGRATED CIRCUITS



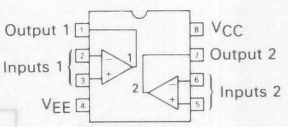
N SUFFIX
PLASTIC PACKAGE
CASE 626-04



D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SO-8



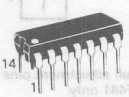
(Single, Top View)



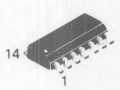
(Dual, Top View)

ORDERING INFORMATION

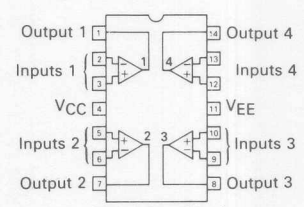
Op Amp Function	Device	Tested Temperature Range	Package
Single	LF441CD LF441CN	0 to +70°C 0 to +70°C	SO-8 Plastic DIP
Dual	LF442CD LF442CN	0 to +70°C 0 to +70°C	SO-8 Plastic DIP
Quad	LF444CD LF444CN	0 to +70°C 0 to +70°C	SO-14 Plastic DIP



N SUFFIX
PLASTIC PACKAGE
CASE 646-06



D SUFFIX
PLASTIC PACKAGE
CASE 751A-02
SO-14



(Quad, Top View)

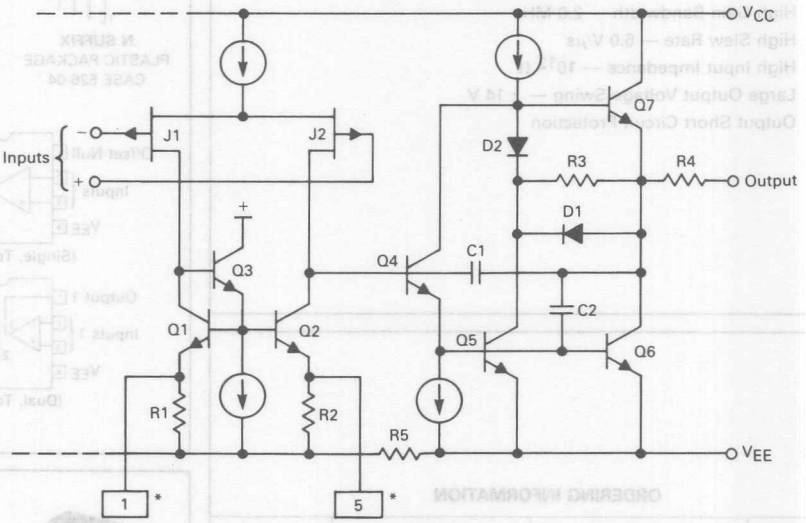
2

MAXIMUM RATINGS

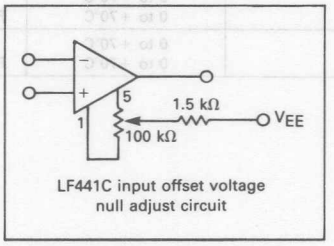
Rating	Symbol	Value	Unit
Supply Voltage (from V_{CC} to V_{EE})	V_S	+36	V
Input Differential Voltage Range (Note 1)	V_{IDR}	±30	V
Input Voltage Range (Notes 1 and 2)	V_{IR}	±15	V
Output Short-Circuit Duration (Note 3)	t_S	Indefinite	Seconds
Operating Junction Temperature (Note 3)	T_J	+150	°C
Storage Temperature Range	T_{stg}	−60 to +150	°C

NOTES:
1. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
2. The magnitude of the input voltage must never exceed the magnitude of the supply or 15 volts, whichever is less.
3. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded. (See Figure 1.)

EQUIVALENT CIRCUIT SCHEMATIC (EACH AMPLIFIER)



*Null adjustment pins for LF441 only.



LF441C input offset voltage null adjust circuit

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 0°C to +70°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 10 kΩ, V_O = 0 V)	V_{IO}				mV
Single					
T_A = +25°C		—	3.0	5.0	
T_A = 0°C to +70°C		—	—	7.5	
Dual					
T_A = +25°C		—	3.0	5.0	
T_A = 0°C to +70°C		—	—	7.5	
Quad					
T_A = +25°C		—	3.0	10	
T_A = 0°C to +70°C		—	—	12	
Average Temperature Coefficient of Offset Voltage (R_S = 10 kΩ, V_O = 0 V)	$\Delta V_{IO}/\Delta T$	—	10	—	μV/°C
Input Offset Current (V_{CM} = 0 V, V_O = 0 V)	I_{IO}				
T_A = +25°C		—	0.5	50	pA
T_A = 0°C to +70°C		—	—	1.5	nA
Input Bias Current (V_{CM} = 0 V, V_O = 0 V)	I_{IB}				
T_A = +25°C		—	3.0	100	pA
T_A = 0°C to +70°C		—	—	3.0	nA
Common Mode Input Voltage Range (T_A = +25°C)	V_{ICR}	— −11	+14.5 −12	+11 —	V
Large Signal Voltage Gain (V_O = ±10 V, R_L = 10 kΩ)	A_{VOL}				V/mV
T_A = +25°C		25	60	—	
T_A = 0°C to +70°C		15	—	—	
Output Voltage Swing (R_L = 10 kΩ)	V_O+ V_O-	+12 —	+14 −14	— −12	V
Common Mode Rejection ($R_S \leq$ 10 kΩ, V_{CM} = V_{ICR}, V_O = 0 V)	CMR	70	86	—	dB
Power Supply Rejection (R_S = 100 Ω, V_{CM} = 0 V, V_O = 0 V)	PSR	70	84	—	dB
Power Supply Current (No Load, V_O = 0 V)	I_D				μA
Single		—	200	250	
Dual		—	400	500	
Quad		—	800	1000	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25°C, unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = −10 V to +10 V, R_L = 10 kΩ, C_L = 10 pF, A_V = +1.0)		SR	0.6	6.0	—	V/μs
Settling Time	To within 10 mV	t_s	—	1.6	—	μs
(A_V = −1.0, R_L = 10 kΩ, V_O = 0 V to +10 V)	To within 1.0 mV		—	2.2	—	
Gain Bandwidth Product (f = 200 kHz)		GBW	0.6	2.0	—	MHz
Equivalent Input Noise Voltage (R_S = 100 Ω, f = 1.0 kHz)		e_n	—	47	—	$nV/\sqrt{Hz}$
Equivalent Input Noise Current (f = 1.0 kHz)		i_n	—	0.01	—	$pA/\sqrt{Hz}$
Input Resistance		R_i	—	10^{12}	—	Ω
Channel Separation (f = 1.0 Hz to 20 kHz)		CS	—	120	—	dB

2

TYPICAL PERFORMANCE CURVES

FIGURE 1 — MAXIMUM POWER DISSIPATION versus TEMPERATURE FOR PACKAGE VARIATIONS

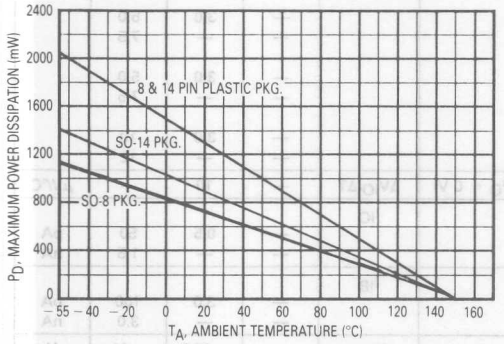


FIGURE 2 — INPUT BIAS CURRENT versus INPUT COMMON-MODE VOLTAGE

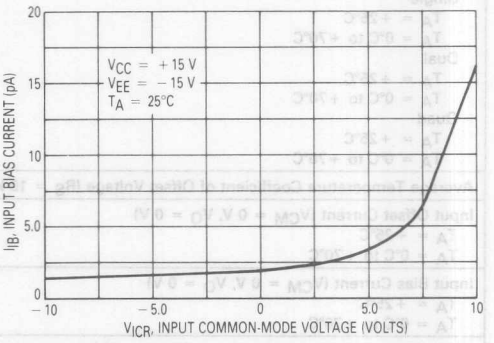


FIGURE 3 — INPUT BIAS CURRENT versus TEMPERATURE

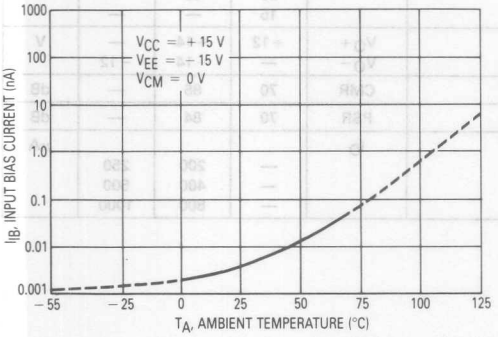


FIGURE 4 — SUPPLY CURRENT versus SUPPLY VOLTAGE

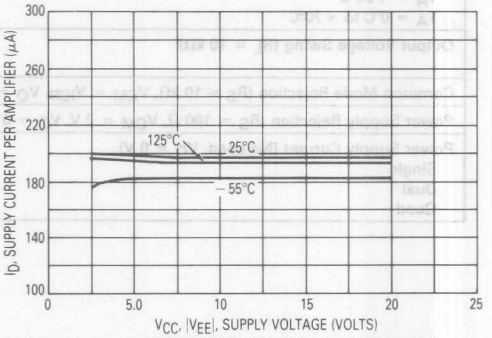


FIGURE 5 — POSITIVE INPUT COMMON-MODE VOLTAGE RANGE versus POSITIVE SUPPLY VOLTAGE

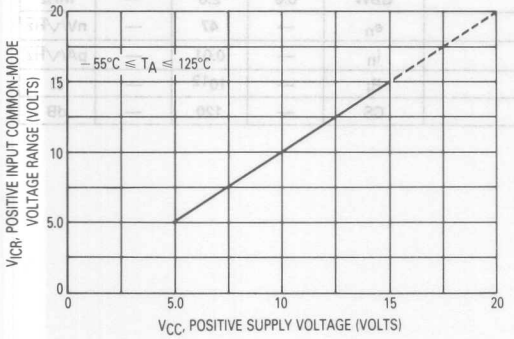


FIGURE 6 — NEGATIVE INPUT COMMON-MODE VOLTAGE RANGE versus NEGATIVE SUPPLY VOLTAGE

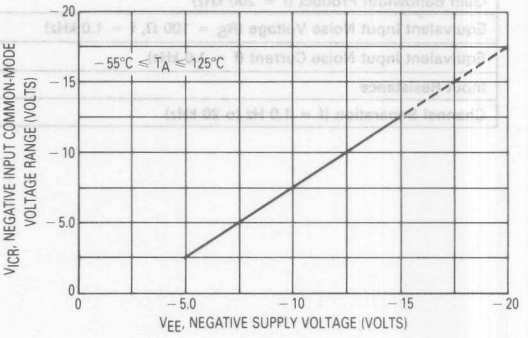


FIGURE 7 — OUTPUT VOLTAGE versus OUTPUT SOURCE CURRENT

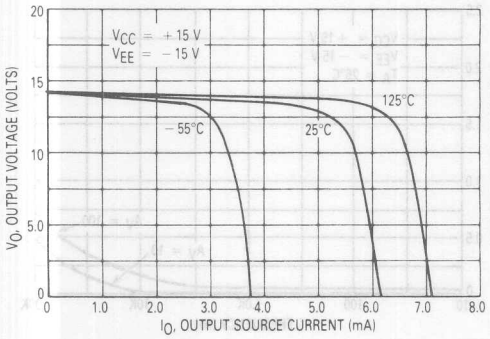


FIGURE 8 — OUTPUT VOLTAGE versus OUTPUT SINK CURRENT

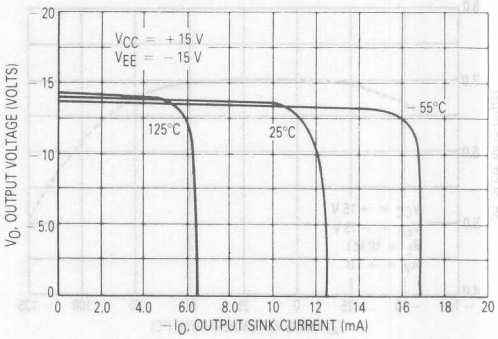


FIGURE 9 — OUTPUT VOLTAGE SWING versus SUPPLY VOLTAGE

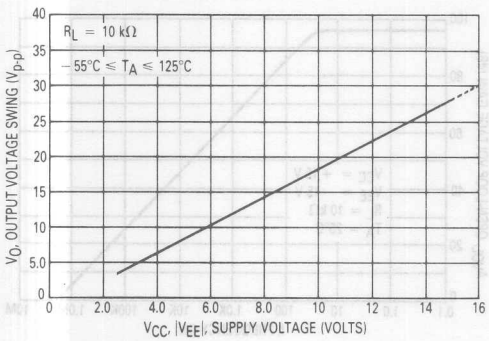


FIGURE 10 — OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

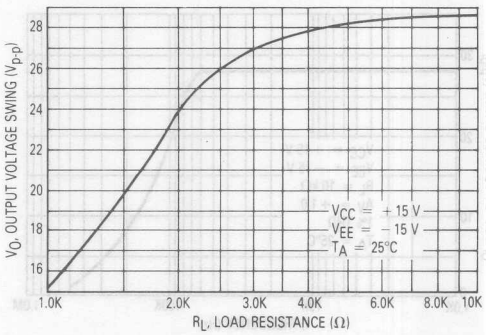


FIGURE 11 — NORMALIZED GAIN BANDWIDTH PRODUCT versus TEMPERATURE

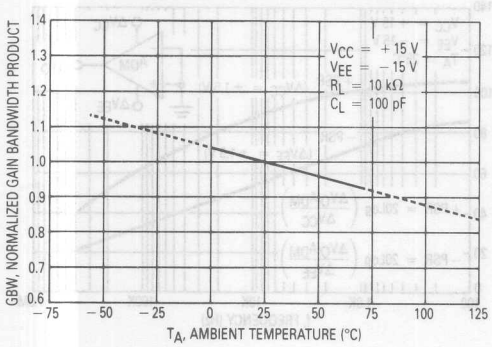
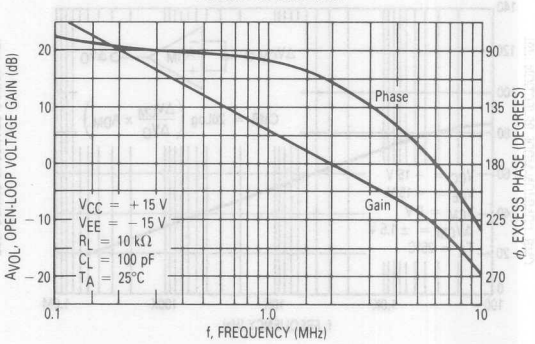


FIGURE 12 — OPEN-LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY



2

FIGURE 13 — SLEW RATE versus TEMPERATURE

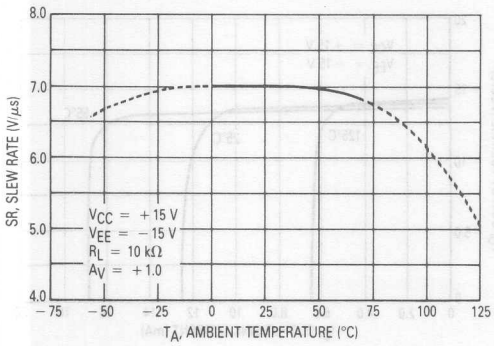


FIGURE 14 — TOTAL OUTPUT DISTORTION versus FREQUENCY

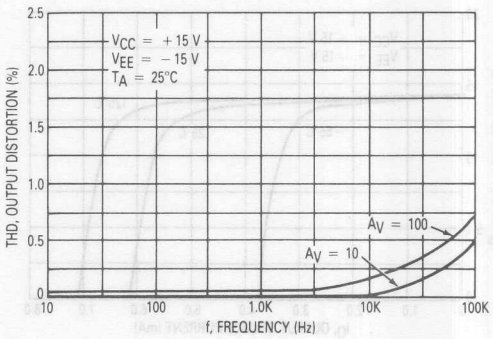


FIGURE 15 — OUTPUT VOLTAGE SWING versus FREQUENCY

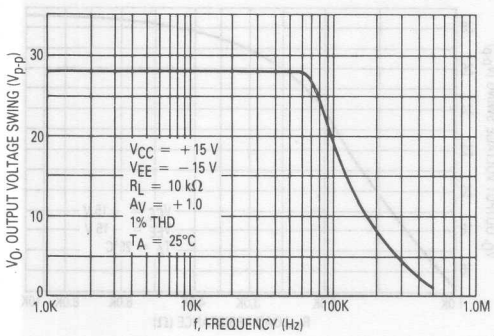


FIGURE 16 — OPEN-LOOP VOLTAGE GAIN versus FREQUENCY

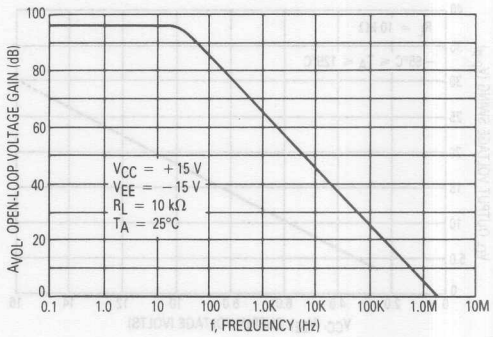


FIGURE 17 — COMMON-MODE REJECTION versus FREQUENCY

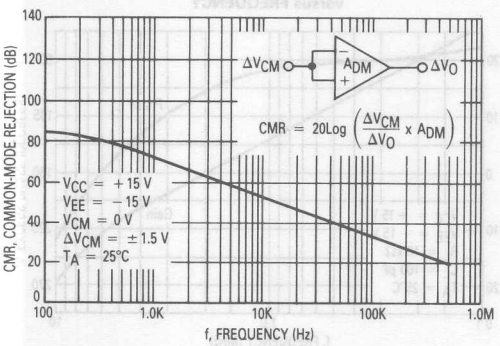


FIGURE 18 — POWER SUPPLY REJECTION versus FREQUENCY

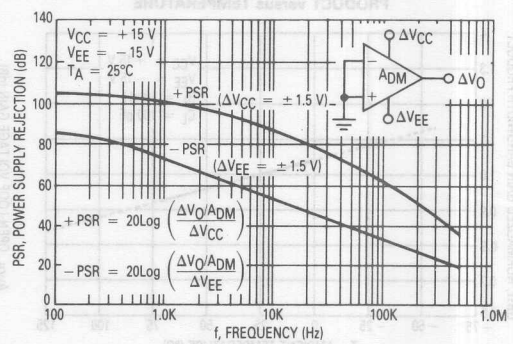


FIGURE 19 — INPUT NOISE VOLTAGE versus FREQUENCY

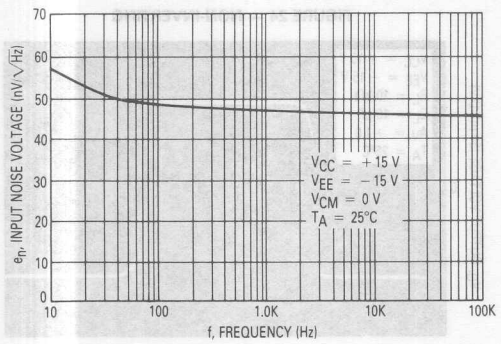


FIGURE 20 — OPEN-LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE

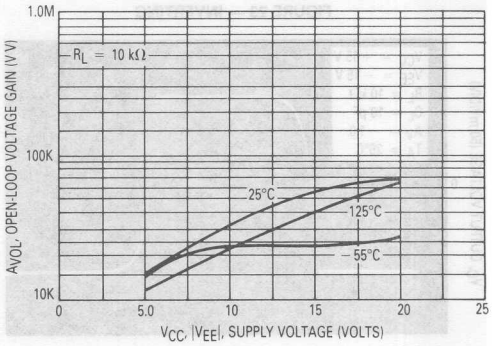


FIGURE 21 — OUTPUT IMPEDANCE versus FREQUENCY

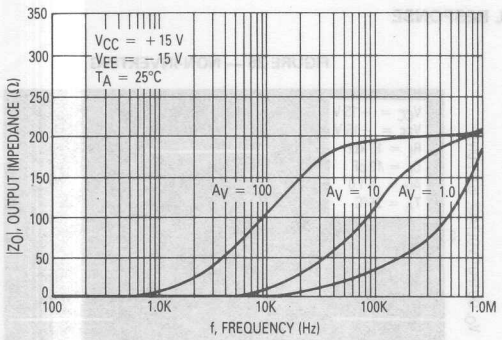
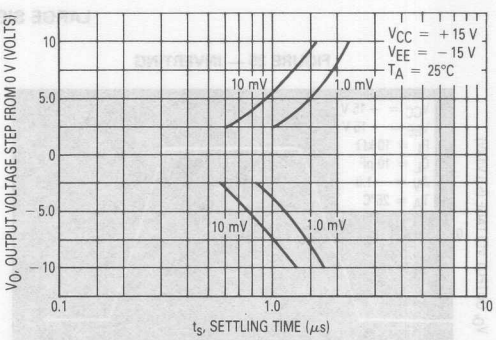


FIGURE 22 — INVERTER SETTLING TIME



2

SMALL SIGNAL RESPONSE

FIGURE 23 — INVERTING

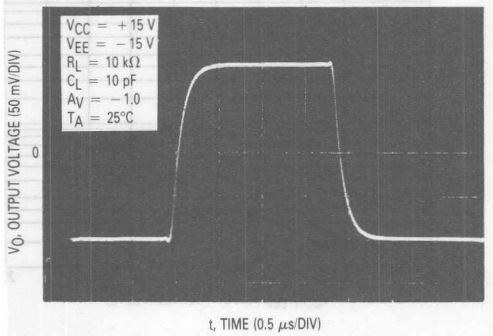
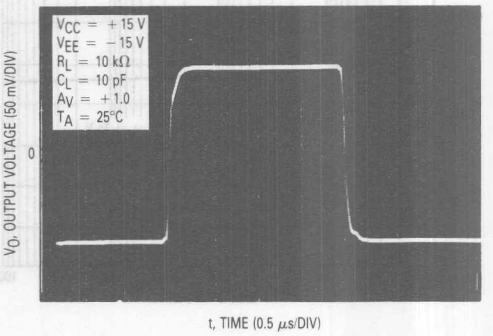


FIGURE 24 — NON-INVERTING



LARGE SIGNAL RESPONSE

FIGURE 25 — INVERTING

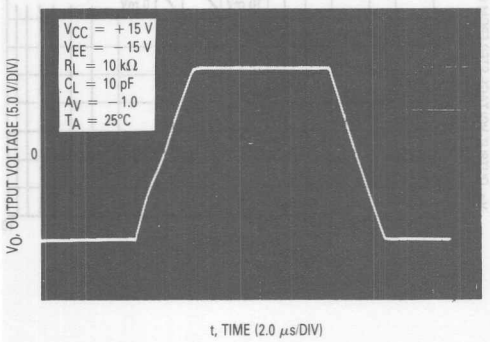
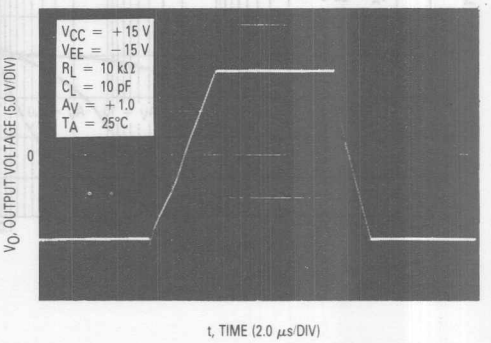


FIGURE 26 — NON-INVERTING



LM11
LM11C
LM11CL

PRECISION OPERATIONAL AMPLIFIERS

The LM11 is a precision, low drift operational amplifier providing the best features of existing FET and Bipolar op amps. Implementation of super gain transistors allows reduction of input bias currents by an order of magnitude over earlier devices such as the LM108A. Offset voltage and drift have also been reduced. Although bandwidth and slew rate are not as great as FET devices, input offset voltage, drift and bias current are inherently lower, particularly over temperature. Power consumption is also much lower, eliminating warm-up stabilization time in critical applications.

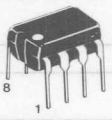
Offset balancing is provided, with the range determined by an external low resistance potentiometer. Compensation is provided internally, but external compensation can be added for improved stability when driving capacitive loads.

The precision characteristics of the LM11 make this device ideal for applications such as charge integrators, analog memories, electrometers, active filters, light meters and logarithmic amplifiers.

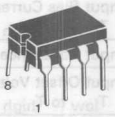
- Low Input Offset Voltage: 100 μV
- Low Input Bias Current: 17 pA
- Low Input Offset Current: 0.5 pA
- Low Input Offset Voltage Drift: 1.0 μV/°C
- Long-Term Stability: 10 μV/year
- High Common Mode Rejection: 130 dB

PRECISION OPERATIONAL AMPLIFIERS

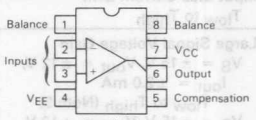
SILICON MONOLITHIC INTEGRATED CIRCUIT

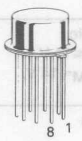


N SUFFIX
PLASTIC PACKAGE
CASE 626-04

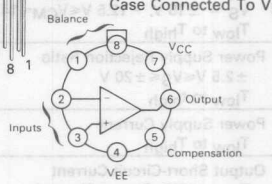


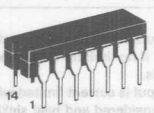
J-8 SUFFIX
CERAMIC PACKAGE
CASE 693-02



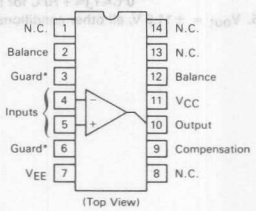


H SUFFIX
METAL CAN
CASE 601-04
Case Connected To V_{EE}





J SUFFIX
CERAMIC PACKAGE
CASE 632-08



*Unused pin (no internal connection) to allow for input anti-leakage guard ring on printed circuit board layout.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} to V_{EE}	40	Vdc
Differential Input Current (Note 1)	I_{ID}	±10	mA
Output Short-Circuit Duration (Note 2)	t_s	Indefinite	
Power Dissipation (Note 3)	P_D	500	mW
Operating Junction Temperature LM11 LM11C/CL	T_J	 150 85	°C
Storage Temperature Range Metal and Ceramic Packages Plastic Package	T_{stg}	 −65 to +150 −55 to +125	°C

ORDERING INFORMATION

Device	Operating Ambient Temperature Range	Package
LM11CLN,CN	0 to +70°C	Plastic 8-Pin DIP
LM11CLJ-8, CJ-8	0 to +70°C	Ceramic 8-Pin DIP
LM11CLJ, CJ	0 to +70°C	Ceramic 14-Pin DIP
LM11CLH, CH	0 to +70°C	Metal Can
LM11J-8	−55 to +125°C	Ceramic 8-Pin DIP
LM11J	−55 to +125°C	Ceramic 14-Pin DIP
LM11H	−55 to +125°C	Metal Can

2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted [Note 4])

Characteristics	Symbol	LM11			LM11C			LM11CL			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	—	0.1	0.3	—	0.2	0.6	—	0.5	5.0	mV
T_{low} to T_{high}		—	—	0.6	—	—	0.8	—	—	6.0	
Input Offset Current	I_{IO}	—	0.5	10	—	1.0	10	—	4.0	25	pA
T_{low} to T_{high}		—	—	30	—	—	20	—	—	50	
Input Bias Current	I_{IB}	—	17	50	—	17	100	—	17	200	pA
T_{low} to T_{high}		—	—	150	—	—	150	—	—	300	
Input Resistance	r_i	—	10^{11}	—	—	10^{11}	—	—	10^{11}	—	Ω
Input Offset Voltage Drift	$\Delta V_{IO}/\Delta T$	—	1.0	3.0	—	2.0	5.0	—	3.0	—	μV/°C
T_{low} to T_{high}											
Input Offset Current Drift	$\Delta I_{IO}/\Delta T$	—	20	—	—	10	—	—	50	—	fA/°C
T_{low} to T_{high}											
Input Bias Current Drift	$\Delta I_{IB}/\Delta T$	—	0.5	1.5	—	0.8	3.0	—	1.4	—	pA/°C
T_{low} to T_{high}											
Large Signal Voltage Gain	A_{VOL}										V/mV
V_S = ±15 V, V_{out} = ±12 V,											
I_{out} = ±2.0 mA		100	300	—	100	300	—	25	300	—	
T_{low} to T_{high} (Note 5)		50	—	—	50	—	—	15	—	—	
V_S = ±15 V, V_{out} = ±12 V,		250	1200	—	250	1200	—	50	800	—	
I_{out} = ±0.5 mA											
T_{low} to T_{high}		100	—	—	100	—	—	30	—	m	
Common Mode Rejection Ratio	CMRR										dB
V_S = ±15 V, −13 V≤V_{CM}≤14 V		110	130	—	110	130	—	96	110	—	
V_S = ±15 V, −12.5 V≤V_{CM}≤14 V,											
T_{low} to T_{high}		100	—	—	100	—	—	90	—	—	
Power Supply Rejection Ratio	PSRR										dB
±2.5 V≤V_S≤±20 V		100	118	—	100	118	—	84	100	—	
T_{low} to t_{high}		96	—	—	96	—	—	80	—	—	
Power Supply Current	I_D	—	0.3	0.6	—	0.3	0.8	—	0.3	0.8	mA
T_{low} to T_{high}		—	—	0.8	—	—	1.0	—	—	1.0	
Output Short-Circuit Current	I_{os}	—	±10	—	—	±10	—	—	±10	—	mA
T_J = 150°C, Output Shorted											
to Ground											

Notes:
1. The inputs are shunted by back-to-back diodes for over-voltage protection. Excessive current will flow if the input differential voltage is in excess of 1.0 V if no limiting resistance is used. Additionally, a 2 kΩ resistance in each input is suggested to prevent possible latch-up initiated by supply reversals.
2. The output is current limited when shorted to ground or any voltages less than the supplies. Continuous overloads will require package dissipation to be considered and heat sinking should be provided when necessary.
3. Devices must be derated based on package thermal resistance (see package outline dimensions).
4. These specifications apply for V_{EE} + 2.0 V≤V_{CM}≤V_{CC} − 1.0 V (V_{EE} + 2.5 V≤V_{CM}≤V_{CC} − 1.0 V for T_{low} to T_{high}) and ±2.5 V≤V_S≤±20 V
   T_{low} to T_{high}: −55°C≤T_J≤+125°C for LM11
   0°C≤T_J≤+70°C for LM11C and LM11CL
5. V_{out} = ±11.5 V, all other conditions unchanged.

SCHEMATIC DIAGRAM

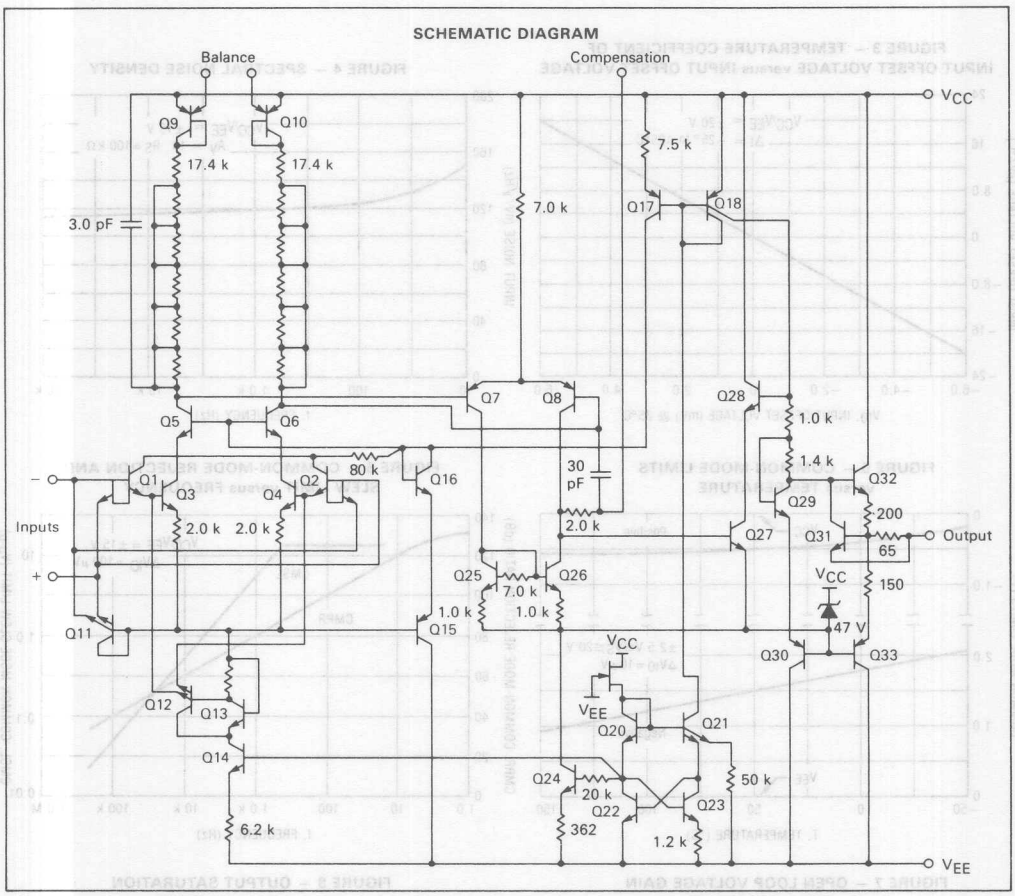


FIGURE 1 — INPUT BIAS CURRENT versus CASE TEMPERATURE

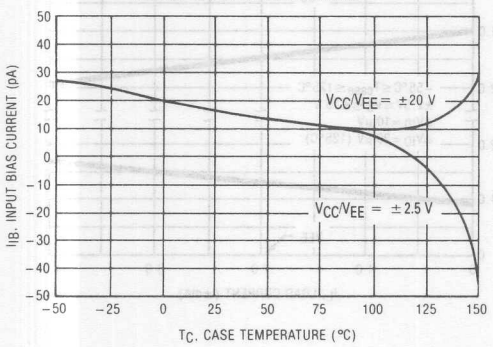
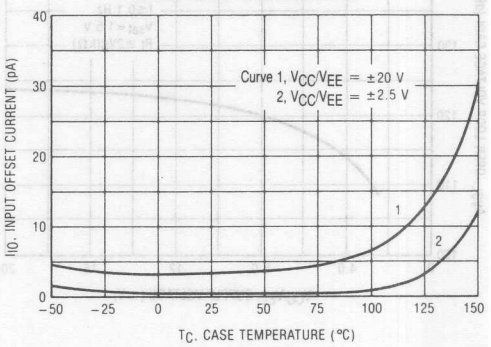


FIGURE 2 — INPUT OFFSET CURRENT versus CASE TEMPERATURE



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FIGURE 3 — TEMPERATURE COEFFICIENT OF INPUT OFFSET VOLTAGE versus INPUT OFFSET VOLTAGE

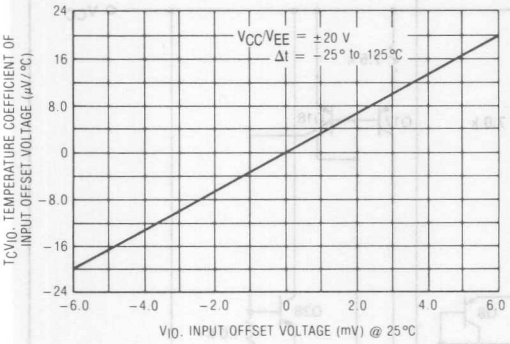


FIGURE 4 — SPECTRAL NOISE DENSITY

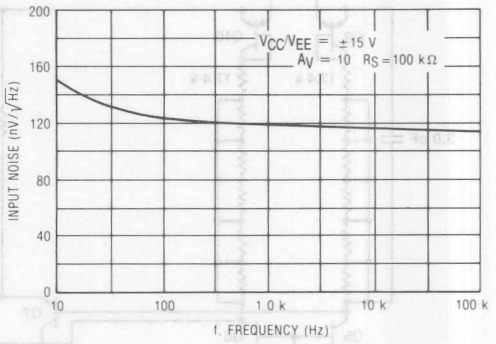


FIGURE 5 — COMMON-MODE LIMITS versus TEMPERATURE

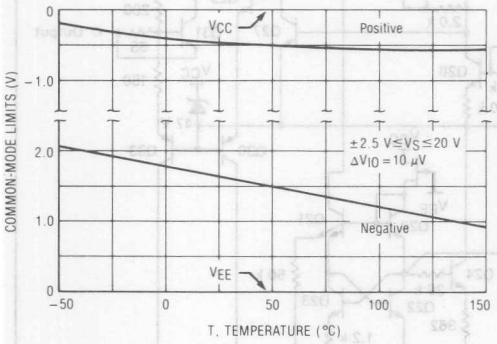


FIGURE 6 — COMMON-MODE REJECTION AND SLEW LIMIT versus FREQUENCY

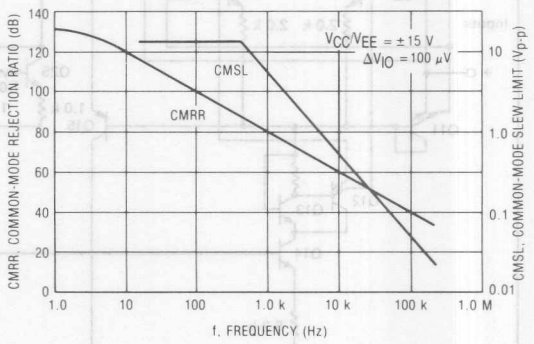


FIGURE 7 — OPEN LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE

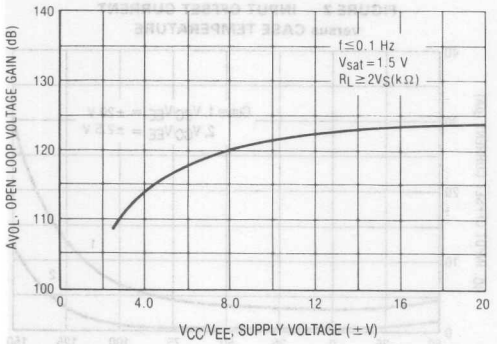


FIGURE 8 — OUTPUT SATURATION versus LOAD CURRENT

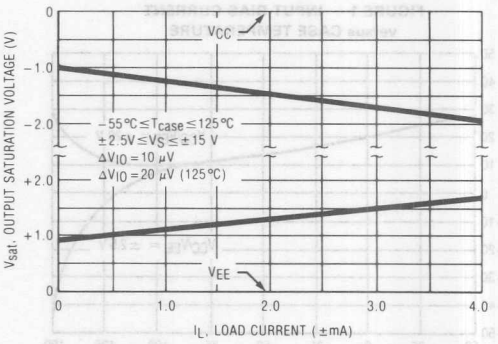


FIGURE 9 — POWER SUPPLY REJECTION RATIO versus FREQUENCY

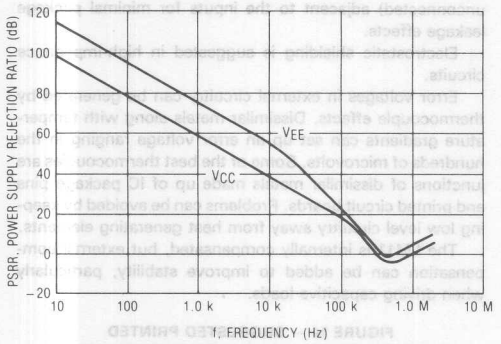


FIGURE 10 — SUPPLY CURRENT versus SUPPLY VOLTAGE

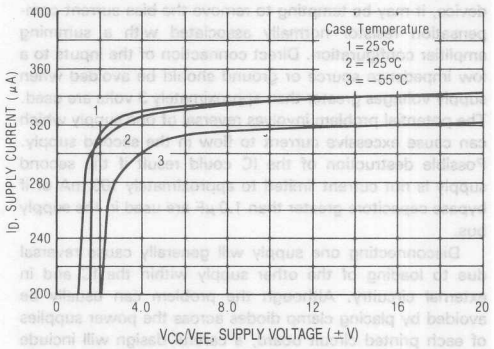


FIGURE 11 — OPEN LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY

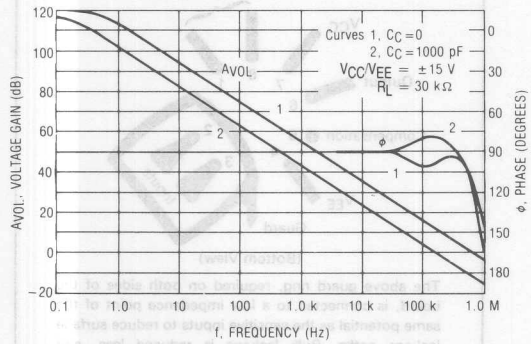


FIGURE 12 — SLEW RATE versus EXTERNAL COMPENSATION CAPACITOR

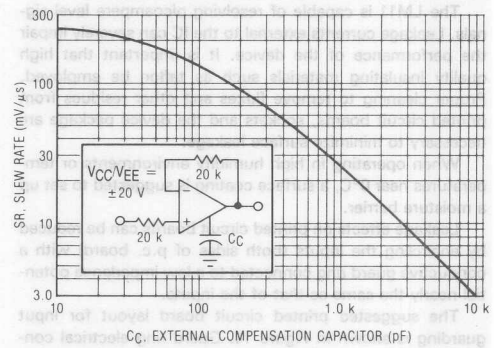
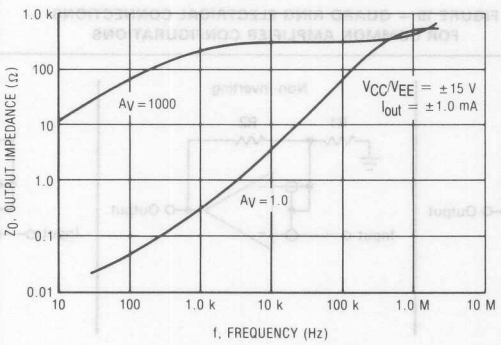


FIGURE 13 — CLOSED LOOP OUTPUT IMPEDANCE versus FREQUENCY



2

APPLICATIONS INFORMATION

Due to the extremely low input bias currents of this device, it may be tempting to remove the bias current compensation resistor normally associated with a summing amplifier configuration. Direct connection of the inputs to a low impedance source or ground should be avoided when supply voltages greater than approximately 3 volts are used. The potential problem involves reversal of one supply which can cause excessive current to flow in the second supply. Possible destruction of the IC could result if the second supply is not current limited to approximately 100 mA or if bypass capacitors greater than 1.0 μF are used in the supply bus.

Disconnecting one supply will generally cause reversal due to loading of the other supply within the IC and in external circuitry. Although the problem can usually be avoided by placing clamp diodes across the power supplies of each printed circuit board, a careful design will include sufficient resistance in the input leads to limit the current to 10 mA if the input leads are pulled to either supply by internal currents. This precaution is not limited to only the LM11.

The LM11 is capable of resolving picoampere level signals. Leakage currents external to the IC can severely impair the performance of the device. It is important that high quality insulating materials such as teflon be employed. Proper cleaning to remove fluxes and other residues from printed circuit boards, sockets and the device package are necessary to minimize surface leakage.

When operating in high humidity environments or temperatures near 0°C, a surface coating is suggested to set up a moisture barrier.

Leakage effects on printed circuit boards can be reduced by encircling the inputs (both sides of p.c. board) with a conductive guard ring connected to a low impedance potential nearly the same as that of the inputs.

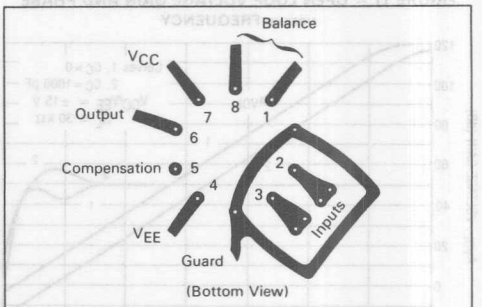
The suggested printed circuit board layout for input guarding is shown in Figure 14. Guard ring electrical connections for common operational amplifier configurations are illustrated in Figure 15. For critical applications, a 14-pin dual in-line package is available with guard pins (internally unconnected) adjacent to the inputs for minimal package leakage effects.

Electrostatic shielding is suggested in high-impedance circuits.

Error voltages in external circuitry can be generated by thermocouple effects. Dissimilar metals along with temperature gradients can set up an error voltage ranging in the hundreds of microvolts. Some of the best thermocouples are junctions of dissimilar metals made up of IC package pins and printed circuit boards. Problems can be avoided by keeping low level circuitry away from heat generating elements.

The LM11 is internally compensated, but external compensation can be added to improve stability, particularly when driving capacitive loads.

FIGURE 14 — SUGGESTED PRINTED CIRCUIT BOARD LAYOUT FOR INPUT GUARDING USING METAL PACKAGED DEVICE



The above guard ring, required on both sides of the board, is connected to a low impedance point of the same potential as the sensitive inputs to reduce surface leakage paths. Bulk leakage is reduced less, and depends more on guard ring width.

FIGURE 15 — GUARD RING ELECTRICAL CONNECTIONS FOR COMMON AMPLIFIER CONFIGURATIONS

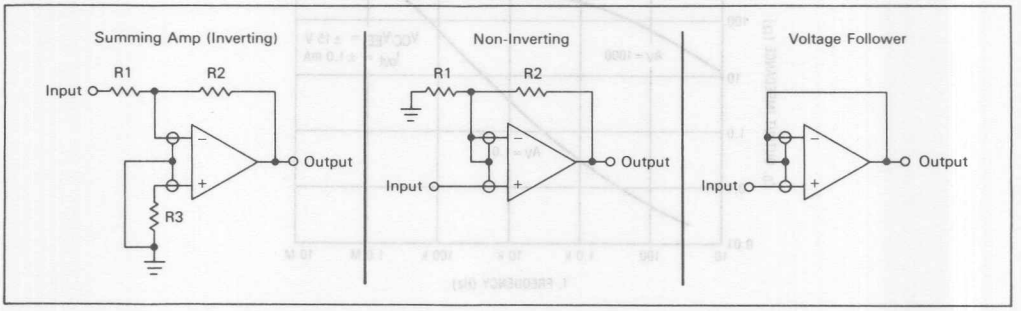
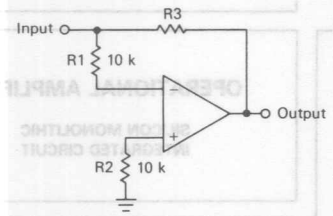
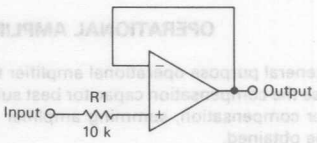


FIGURE 16 — INPUT PROTECTION FOR SUMMING (INVERTING) AMPLIFIER



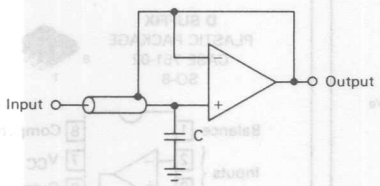
Current is limited by R1 in the event the input is connected to a low impedance source outside the common-mode range of the device. Current is controlled by R2 if one supply reverses. R1 and R2 do not affect normal operation.

FIGURE 17 — INPUT PROTECTION FOR A VOLTAGE FOLLOWER

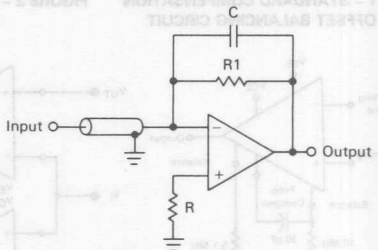


Input current is limited by R1 when the input exceeds supply voltage, power supply is turned off, or output is shorted.

FIGURE 18 — CABLE BOOT STRAPPING AND INPUT SHIELDS

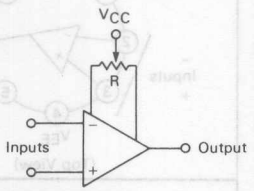


An input shield boot strapped in a voltage follower reduces input capacitance, leakage, and spurious voltages from cable flexing. A small capacitor from the input to ground will prevent any instability.



In a summing amplifier the input is at virtual ground. Therefore the shield can be grounded. A small feedback capacitor will insure stability.

FIGURE 19 — ADJUSTING INPUT OFFSET VOLTAGE WITH BALANCE POTENTIOMETER



Minimum Adjustment Range (mV)	R Ω
±0.4	1.0 k
±1.0	3.0 k
±2.0	10 k
±5.0	100 k

Input offset voltage adjustment range is a function of the Balance Potentiometer Resistance as indicated by the table above. The potentiometer is connected between the two "Balance" pins.

LM301A

OPERATIONAL AMPLIFIER

A general purpose operational amplifier that allows the user to choose the compensation capacitor best suited to his needs. With proper compensation, summing amplifier slew rates to 10 V/μs can be obtained.

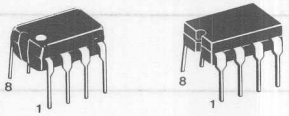
- Low Input Offset Current — 20 nA maximum Over Temperature Range
- External Frequency Compensation for Flexibility
- Class AB Output Provides Excellent Linearity
- Output Short Circuit Protection
- Guaranteed Drift Characteristics

OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

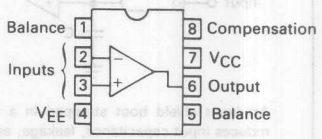
N SUFFIX
PLASTIC PACKAGE
CASE 626-05
(LM201A and LM301A)

J SUFFIX
CERAMIC PACKAGE
CASE 693-02



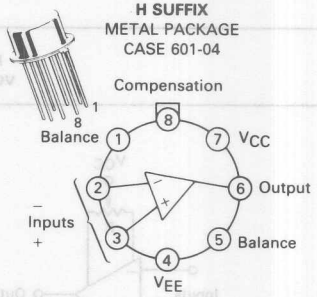
D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SO-8





(Top View)

H SUFFIX
METAL PACKAGE
CASE 601-04



(Top View)

FIGURE 1 – STANDARD COMPENSATION AND OFFSET BALANCING CIRCUIT

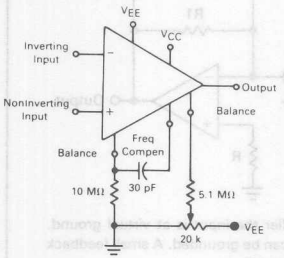
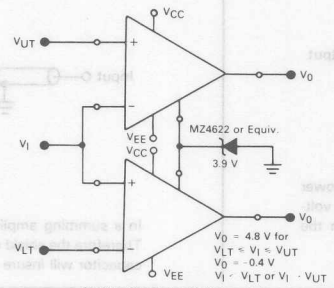
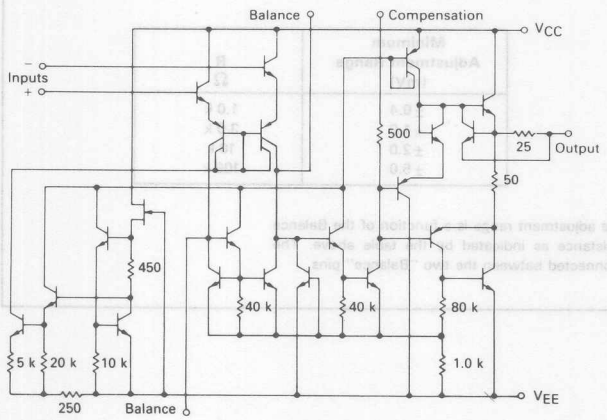


FIGURE 2 – DOUBLE-ENDED LIMIT DETECTOR



Pins Not Shown Are Not Connected

FIGURE 3 – REPRESENTATIVE CIRCUIT SCHEMATIC



ORDERING INFORMATION

Device	Temperature Range	Package
LM101AH	−55°C to +125°C	Metal Can
LM101AJ	−55°C to +125°C	Ceramic DIP
LM201AD	−25°C to +85°C	SO-8
LM201AH	−25°C to +85°C	Metal Can
LM201AN	−25°C to +85°C	Plastic DIP
LM201AJ	−25°C to +85°C	Ceramic Dip
LM301AD	0°C to +70°C	SO-8
LM301AH	0°C to +70°C	Metal Can
LM301AN	0°C to +70°C	Plastic DIP
LM301AJ	0°C to +70°C	Ceramic Dip

MAXIMUM RATINGS

Rating	Symbol	VALUE			Unit
		LM101A	LM201A	LM301A	
Power Supply Voltage	V_{CC}, V_{EE}	±22	±22	±18	Vdc
Input Differential Voltage	V_{ID}	±30			Volts
Input Common-Mode Range (Note 1)	V_{ICR}	±15			Volts
Output Short-Circuit Duration	t_S	Continuous			
Power Dissipation (Package Limitation)	P_D				
Metal Can		500			mW
Derate above T_A = +75°C		6.8			mW/°C
Plastic Dual In-Line Package (LM201A/		—	625	625	mW
Derate above T_A = + 25°C 301A)		—	5.0	5.0	mW/°C
Ceramic Package		750			mW
Derate above 25°C		6.6			mW/°C
Operating Ambient Temperature Range	T_A	−55 to +125	−25 to +85	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150			°C

Note 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted.) Unless otherwise specified, these specifications apply for supply voltages from ±5.0 V to ±20 V for the LM101A and LM201A, and from ±5.0 V to ±15 V for the LM301A.

Characteristics	Symbol	LM101A LM201A			LM301A			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (R_S ≤ 50 kΩ)	V_{IO}	—	0.7	2.0	—	2.0	7.5	mV
Input Offset Current	I_{IO}	—	1.5	10	—	3.0	50	nA
Input Bias Current	I_{IB}	—	30	75	—	70	250	nA
Input Resistance	r_i	1.5	4.0	—	0.5	2.0	—	Megohms
Supply Current	I_{CC},I_{EE}							mA
V_{CC}/V_{EE} = ±20 V		—	1.8	3.0	—	—	—	
V_{CC}/V_{EE} = ±15 V		—	—	—	—	1.8	3.0	
Large Signal Voltage Gain (V_{CC}/V_{EE} = ±15 V, V_O = ±10 V, R_L > 2.0 kΩ)	A_V	50	160	—	25	160	—	V/mV
The following specifications apply over the operating temperature range.								
Input Offset Voltage (R_S ≤ 50 kΩ)	V_{IO}	—	—	3.0	—	—	10	mV
Input Offset Current	I_{IO}	—	—	20	—	—	70	nA
Average Temperature Coefficient of Input Offset Voltage T_A(min) ≤ T_A ≤ T_A(max)	$\Delta V_{IO}/\Delta T$	—	3.0	15	—	6.0	30	µV/°C
Average Temperature Coefficient of Input Offset Current	$\Delta I_{IO}/\Delta T$							nA/°C
+25°C ≤ T_A ≤ T_A(max)		—	0.01	0.1	—	0.01	0.3	
T_A(min) ≤ T_A ≤ 25°C		—	0.02	0.2	—	0.02	0.6	
Input Bias Current	I_{IB}	—	—	100	—	—	300	nA
Large Signal Voltage Gain (V_{CC}/V_{EE} = ±15 V, V_O = ±10 V, R_L > 2.0 kΩ)	A_V	25	—	—	15	—	—	V/mV
Input Voltage Range	V_I							V
V_{CC}/V_{EE} = ±20 V		±15	—	—	—	—	—	
V_{CC}/V_{EE} = ±15 V		—	—	—	±12	—	—	
Common-Mode Rejection Ratio R_S ≤ 50 kΩ	CMRR	80	96	—	70	90	—	dB
Supply Voltage Rejection Ratio R_S ≤ 50 kΩ	PSRR	80	96	—	70	96	—	dB
Output Voltage Swing	V_O							V
V_{CC}/V_{EE} = ±15 V, R_L = 10 kΩ,		±12	±14	—	±12	±14	—	
R_L = 2.0 kΩ		±10	±13	—	±10	±13	—	
Supply Currents (T_A = T_A(max), V_{CC}/V_{EE} = ±20 V)	I_{CC}, I_{EE}	—	1.2	2.5	—	—	—	mA

2

TYPICAL CHARACTERISTICS

(V_{CC} = +15 V, V_{EE} = −15 V, T_A = + 25°C unless otherwise noted.)

FIGURE 4 — MINIMUM INPUT VOLTAGE RANGE

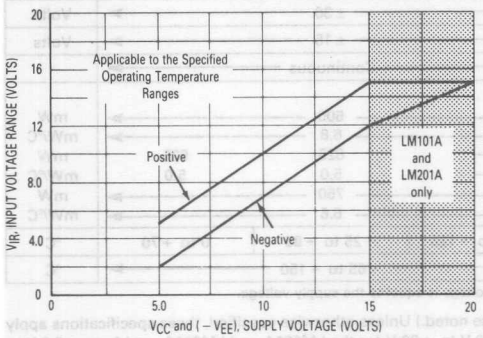


FIGURE 5 — MINIMUM OUTPUT VOLTAGE SWING

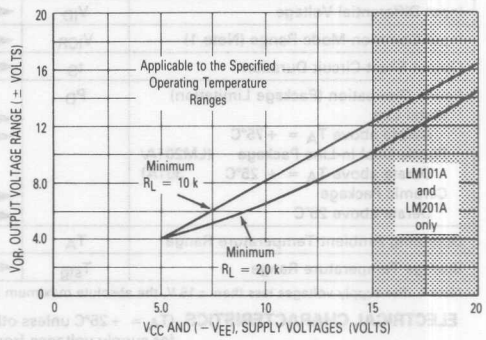


FIGURE 6 — MINIMUM VOLTAGE GAIN

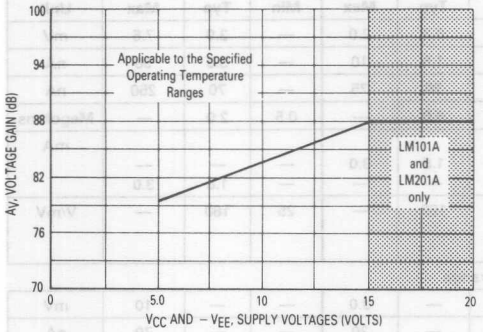


FIGURE 7 — TYPICAL SUPPLY CURRENTS

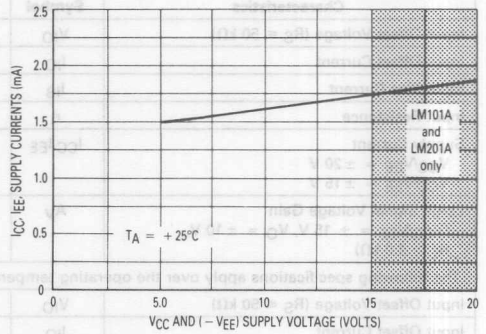


FIGURE 8 — OPEN-LOOP FREQUENCY RESPONSE

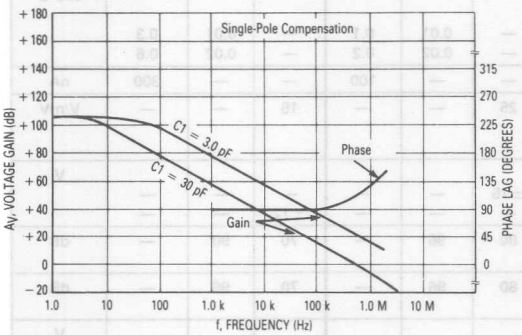
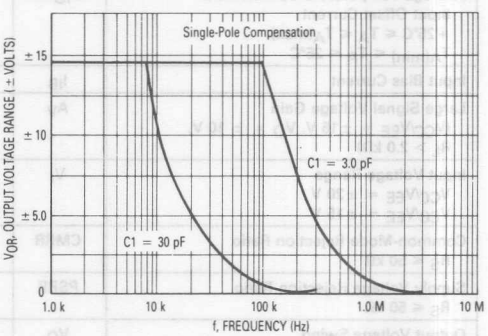


FIGURE 9 — LARGE-SIGNAL FREQUENCY RESPONSE



TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25°C unless otherwise noted.)

FIGURE 10 — VOLTAGE FOLLOWER PULSE RESPONSE

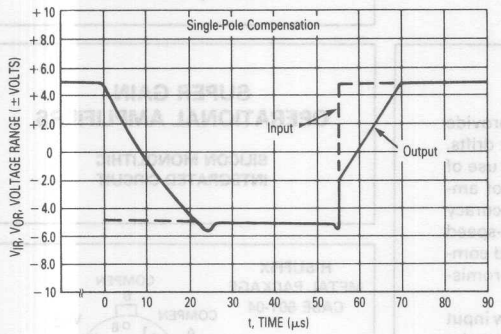


FIGURE 11 — OPEN-LOOP FREQUENCY RESPONSE

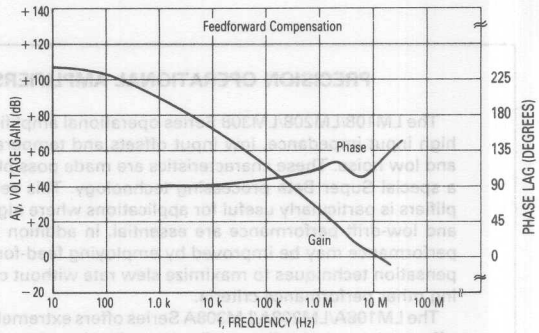


FIGURE 12 — LARGE-SIGNAL FREQUENCY RESPONSE

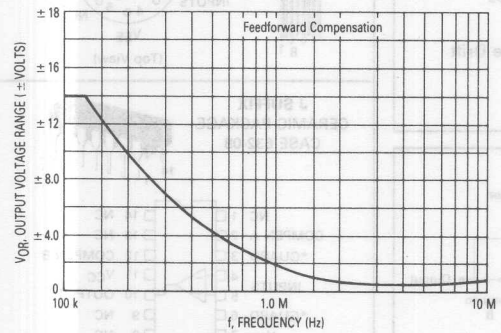
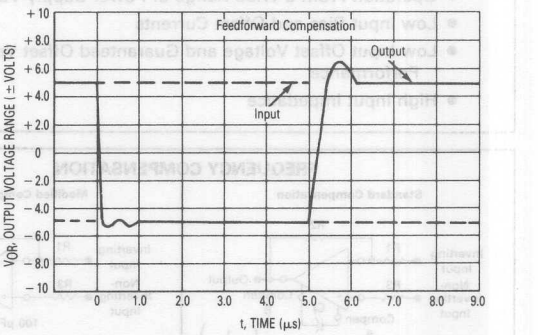
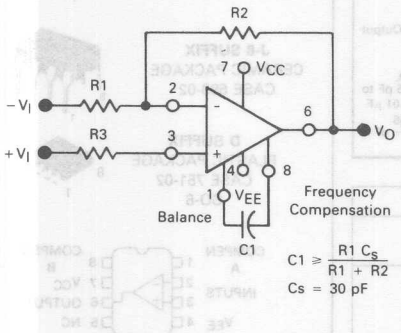


FIGURE 13 — INVERTER PULSE RESPONSE



TYPICAL COMPENSATION CIRCUITS

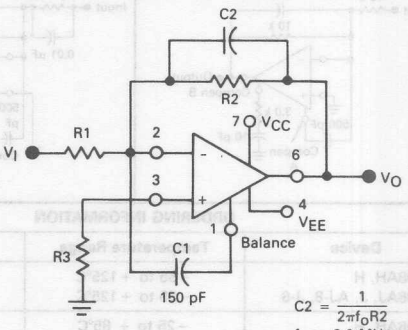
FIGURE 14 — SINGLE-POLE COMPENSATON



$$C1 \geq \frac{R1\ C_S}{R1 + R2}$$

C_S = 30 pF

FIGURE 15 — FEEDFORWARD COMPENSATION



$$C2 = \frac{1}{2\pi f_O R2}$$

f_O = 3.0 MHz

MOTOROLA

LM208, LM208A
LM308, LM308A

PRECISION OPERATIONAL AMPLIFIERS

The LM108/LM208/LM308 Series operational amplifiers provide high input impedance, low input offsets and temperature drifts, and low noise. These characteristics are made possible by use of a special Super Beta processing technology. This series of amplifiers is particularly useful for applications where high-accuracy and low-drift performance are essential. In addition high-speed performance may be improved by employing feed-forward compensation techniques to maximize slew rate without compromising other performance criteria.

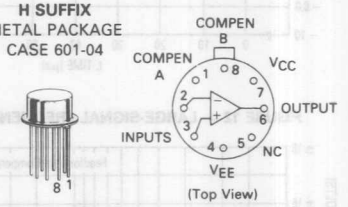
The LM108A/LM208A/LM308A Series offers extremely low input offset voltage and drift specifications allowing usage in even the most critical applications without external offset nulling.

- Operation From a Wide Range of Power Supply Voltages
- Low Input Bias and Offset Currents
- Low Input Offset Voltage and Guaranteed Offset Voltage Drift Performance
- High Input Impedance

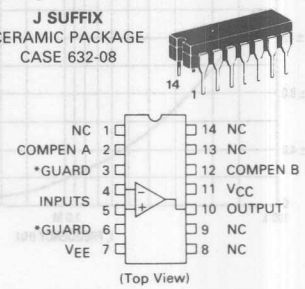
SUPER GAIN OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUIT

H SUFFIX
METAL PACKAGE
CASE 601-04



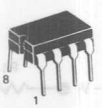
J SUFFIX
CERAMIC PACKAGE
CASE 632-08



N SUFFIX
PLASTIC PACKAGE
CASE 626-05
(LM208, LM208A)
(LM308, LM308A Only)

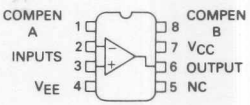


J-8 SUFFIX
CERAMIC PACKAGE
CASE 693-02



D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SO-8

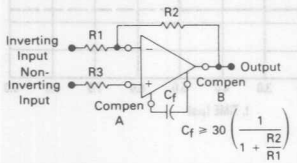




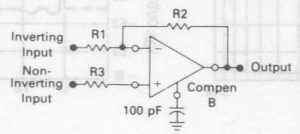
*Unused pin (no internal connection) to allow for input anti-leakage guard ring on printed circuit board layout.

FREQUENCY COMPENSATION

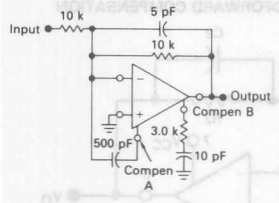
Standard Compensation



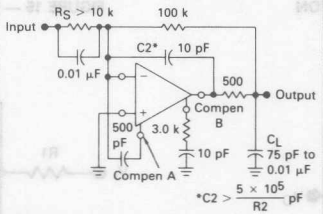
Modified Compensation



Standard Feedforward Compensation



Feedforward Compensations for Decoupling Load Capacitance



ORDERING INFORMATION

Device	Temperature Range	Package
LM108AH, H	−55 to +125°C	Metal Can
LM108AJ, J, AJ-8, J-8	−55 to +125°C	Ceramic DIP
LM208AH, H	−25 to + 85°C	Metal Can
LM208AJ, J, AJ-8, J-8	−25 to +85°C	Ceramic DIP
LM208AN, N	−25 to +85°C	Plastic DIP
LM208AD, D	−25 to +85°C	SO-8
LM308AH, H	0 to +70°C	Metal Can
LM308AJ, J, AJ-8, J-8	0 to +70°C	Ceramic DIP
LM308AN, N	0 to +70°C	Plastic DIP
LM308AD, D	0 to +70°C	SO-8

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value			Unit
		LM108, LM108A	LM208, LM208A	LM308, LM308A	
Power Supply Voltage	V_{CC}, V_{EE}	±20	±20	±18	Vdc
Input Voltage (See Note 1)	V_I	±15			Volts
Input Differential Current (See Note 2)	I_{ID}	±10			mA
Output Short-Circuit Duration	t_S	Indefinite			
Operating Ambient Temperature Range	T_A	−55 to +125	−25 to +85	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150			°C
Junction Temperature Metal, Ceramic Package Plastic Package	T_J	 +175 +150			°C

Note 1. For supply voltages less than ±15 V, the maximum input voltage is equal to the supply voltage.
Note 2. The inputs are shunted with back-to-back diodes for over-voltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1.0 V is applied between the inputs unless some limiting resistance is used.

ELECTRICAL CHARACTERISTICS (Unless otherwise noted these specifications apply for supply voltages of +5.0 V ≤ V_{CC} ≤ +20 V and −5.0 V ≥ V_{EE} ≥ −20 V, T_A = +25°C.)

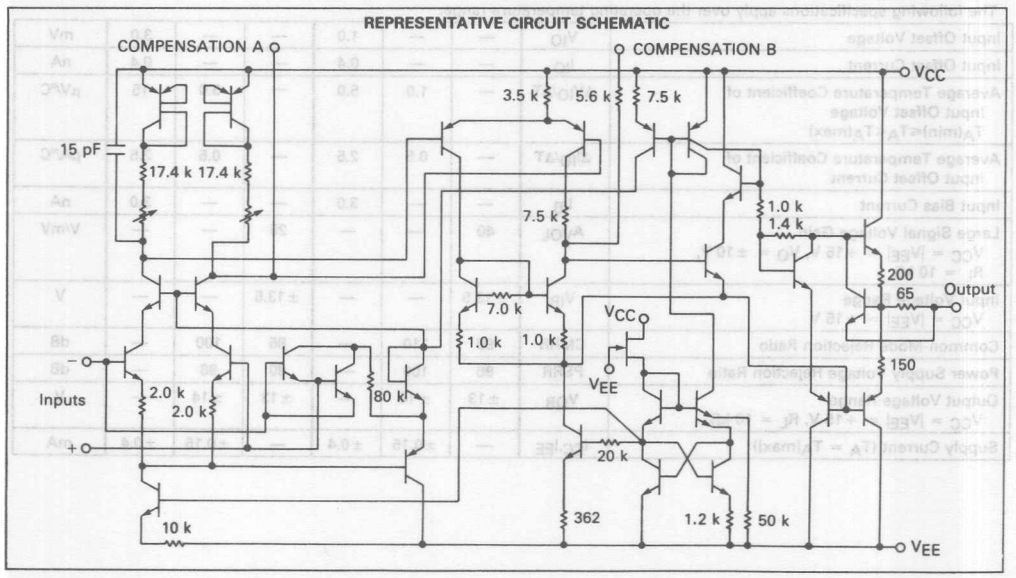
Characteristic	Symbol	LM108A LM208A			LM108 LM208			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	—	0.3	0.5	—	0.7	2.0	mV
Input Offset Current	I_{IO}	—	0.05	0.2	—	0.005	0.2	nA
Input Bias Current	I_{IB}	—	0.8	2.0	—	0.8	2.0	nA
Input Resistance	r_i	30	70	—	30	70	—	Megohms
Power Supply Currents V_{CC} = +20 V, V_{EE} = −20 V	I_{CC},I_{EE}	—	±0.3	±0.6	—	±0.3	±0.6	mA
Large Signal Voltage Gain V_{CC} = $\|V_{EE}\|$ = +15 V, V_O = ±10 V, R_L ≥ 10 kΩ	A_{VOL}	80	300	—	50	300	—	V/mV
The following specifications apply over the operating temperature range.								
Input Offset Voltage	V_{IO}	—	—	1.0	—	—	3.0	mV
Input Offset Current	I_{IO}	—	—	0.4	—	—	0.4	nA
Average Temperature Coefficient of Input Offset Voltage $T_A(min) \leq T_A \leq T_A(max)$	$\Delta V_{IO}/\Delta T$	—	1.0	5.0	—	3.0	15	µV/°C
Average Temperature Coefficient of Input Offset Current	$\Delta I_{IO}/\Delta T$	—	0.5	2.5	—	0.5	2.5	pA/°C
Input Bias Current	I_{IB}	—	—	3.0	—	—	3.0	nA
Large Signal Voltage Gain V_{CC} = $\|V_{EE}\|$ = +15 V, V_O = ±10 V, R_L = 10 kΩ	A_{VOL}	40	—	—	25	—	—	V/mV
Input Voltage Range V_{CC} = $\|V_{EE}\|$ = +15 V	V_{IR}	±13.5	—	—	±13.5	—	—	V
Common-Mode Rejection Ratio	CMRR	96	110	—	85	100	—	dB
Power Supply Voltage Rejection Ratio	PSRR	96	100	—	80	96	—	dB
Output Voltage Range V_{CC} = $\|V_{EE}\|$ = +15 V, R_L = 10 kΩ	V_{OR}	±13	±14	—	±13	±14	—	V
Supply Current (T_A = T_A[max])	I_{CC},I_{EE}	—	±0.15	±0.4	—	±0.15	±0.4	mA

2

ELECTRICAL CHARACTERISTICS (Unless otherwise noted these specifications apply for supply voltages of $+5.0\ V \leq V_{CC} \leq +15\ V$ and $-5.0V \geq V_{EE} \geq -15\ V$, $T_A = +25°C$.)

Characteristic	Symbol	LM308A Min	LM308A Typ	LM308A Max	LM308 Min	LM308 Typ	LM308 Max	Unit
Input Offset Voltage	V_{IO}	—	0.3	0.5	—	2.0	7.5	mV
Input Offset Current	I_{IO}	—	0.2	1.0	—	0.2	1.0	nA
Input Bias Current	I_{IB}	—	1.5	7.0	—	1.5	7.0	nA
Input Resistance	r_i	10	40	—	10	40	—	Megohms
Power Supply Currents $V_{CC} = +15\ V, V_{EE} = -15\ V$	I_{CC}, I_{EE}	—	±0.3	±0.8	—	±0.3	±0.8	mA
Large Signal Voltage Gain $V_{CC} = +15\ V, V_{EE} = -15\ V, V_O = \pm 10\ V, R_L \geq 10\ k\Omega$	A_{VOL}	80	300	—	25	300	—	V/mV
The following specifications apply over the operating temperature range.								
Input Offset Voltage	V_{IO}	—	—	0.73	—	—	10	mV
Input Offset Current	I_{IO}	—	—	1.5	—	—	1.5	nA
Average Temperature Coefficient of Input Offset Voltage $T_A(min) \leq T_A \leq T_A(max)$	$\Delta V_{IO}/\Delta T$	—	1.0	5.0	—	6.0	30	µV/°C
Average Temperature Coefficient of Input Offset Current	$\Delta I_{IO}/\Delta T$	—	2.0	10	—	2.0	10	pA/°C
Input Bias Current	I_{IB}	—	—	10	—	—	10	nA
Large Signal Voltage Gain $V_{CC} = +15\ V, V_{EE} = -15\ V, V_O = \pm 10\ V, R_L \geq 10\ k\Omega$	A_{VOL}	60	—	—	15	—	—	V/mV
Input Voltage Range $V_{CC} = +15\ V, V_{EE} = -15\ V$	V_{IR}	±14	—	—	±14	—	—	V
Common-Mode Rejection Ratio $R_S \leq 50\ k\Omega$	CMRR	96	110	—	80	100	—	dB
Supply Voltage Rejection Ratio $R_S \leq 50\ k\Omega$	PSRR	96	110	—	80	96	—	dB
Output Voltage Range $V_{CC} = +15\ V, V_{EE} = -15\ V, R_L = 10\ k\Omega$	V_{OR}	±13	±14	—	±13	±14	—	V

REPRESENTATIVE CIRCUIT SCHEMATIC



TYPICAL CHARACTERISTICS

FIGURE 1 – INPUT BIAS AND INPUT OFFSET CURRENTS

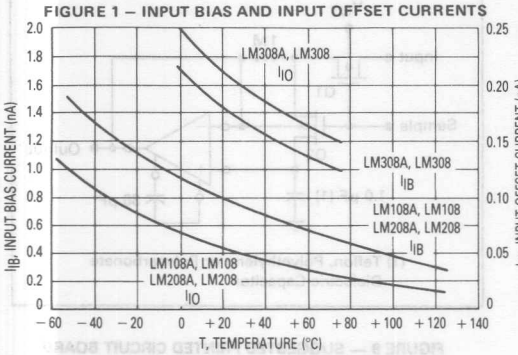


FIGURE 2 – MAXIMUM EQUIVALENT INPUT OFFSET VOLTAGE ERROR versus INPUT RESISTANCE

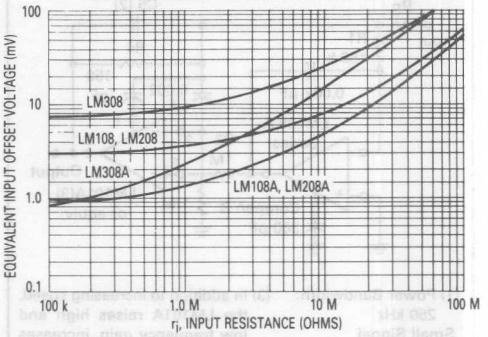


FIGURE 3 – VOLTAGE GAIN versus SUPPLY VOLTAGES

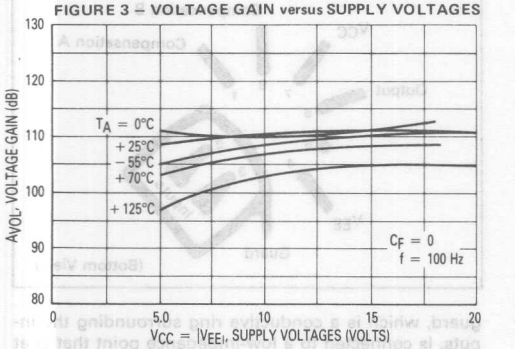


FIGURE 4 – POWER SUPPLY CURRENTS versus POWER SUPPLY VOLTAGE

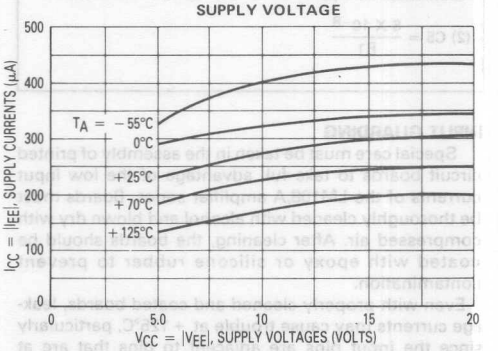


FIGURE 5 – OPEN-LOOP FREQUENCY RESPONSE

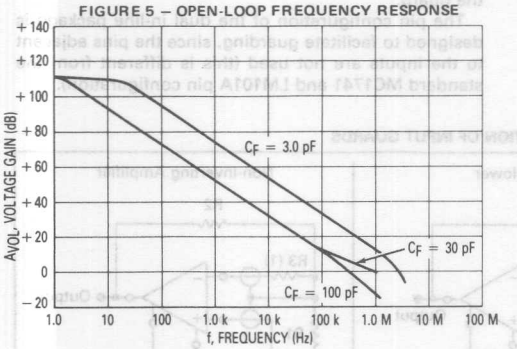
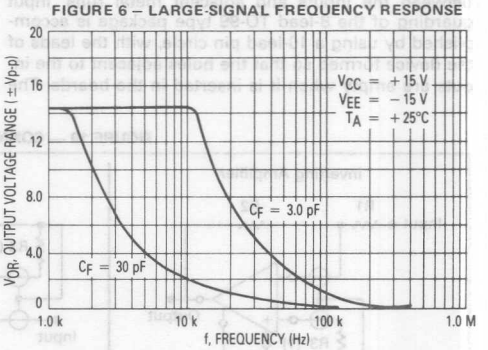
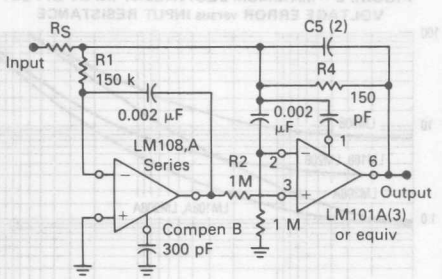


FIGURE 6 – LARGE-SIGNAL FREQUENCY RESPONSE

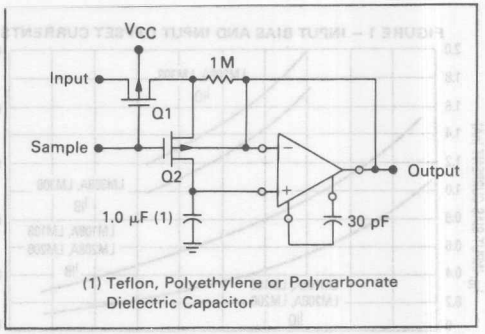




(1) Power Bandwidth: 250 kHz
Small Signal Bandwidth: 3.5 MHz
Slew Rate: 10 V/μs

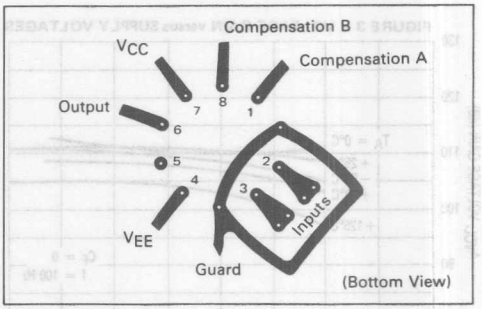
(2) $C5 = \frac{6 \times 10^{-8}}{R1}$

(3) In addition to increasing speed, the LM101A raises high and low frequency gain, increases output drive capability and eliminates thermal feedback.



(1) Teflon, Polyethylene or Polycarbonate Dielectric Capacitor

FIGURE 9 — SUGGESTED PRINTED CIRCUIT BOARD LAYOUT for INPUT GUARDING USING METAL PACKAGED DEVICE



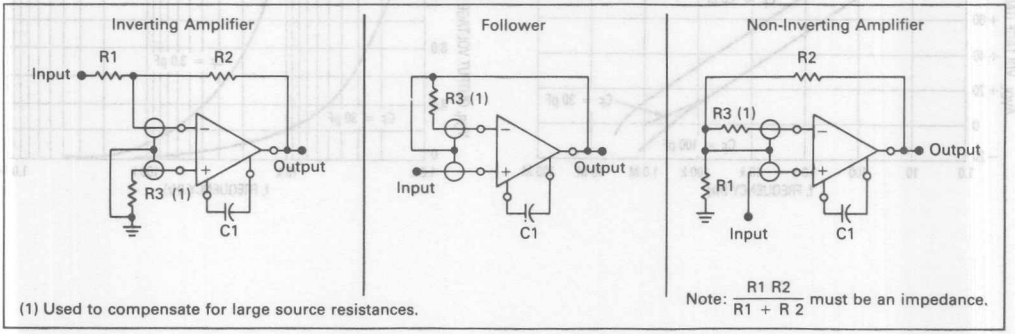
INPUT GUARDING

Special care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the LM108,A amplifier series. Boards must be thoroughly cleaned with alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble at +125°C, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8-lead TO-99 type package is accomplished by using a 10-lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the boards. The guard, which is a conductive ring surrounding the inputs, is connected to a low-impedance point that is at approximately the same voltage as the inputs. Leakage currents from high-voltage pins are then absorbed by the guard.

The pin configuration of the dual in-line package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard MC1741 and LM101A pin configuration).

FIGURE 10 — CONNECTION OF INPUT GUARDS



(1) Used to compensate for large source resistances.

Note: $\frac{R1\ R2}{R1 + R2}$ must be an impedance.

MOTOROLA

LM111
LM211
LM311

2

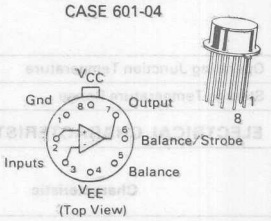
HIGHLY FLEXIBLE VOLTAGE COMPARATORS

The ability to operate from a single power supply of 5.0 to 30 volts or ±15 volt split supplies, as commonly used with operational amplifiers, makes the LM111/LM211/LM311 a truly versatile comparator. Moreover, the inputs of the device can be isolated from system ground while the output can drive loads referenced either to ground, the V_{CC} or the V_{EE} supply. This flexibility makes it possible to drive DTL, RTL, TTL, or MOS logic. The output can also switch voltages to 50 volts at currents to 50 mA. Thus the LM111/LM211/LM311 can be used to drive relays, lamps or solenoids.

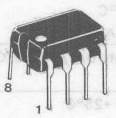
HIGH PERFORMANCE VOLTAGE COMPARATORS

SILICON MONOLITHIC INTEGRATED CIRCUIT

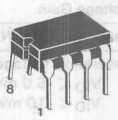
H SUFFIX
METAL PACKAGE
CASE 601-04



N SUFFIX
PLASTIC PACKAGE
CASE 626-05
(LM311 Only)

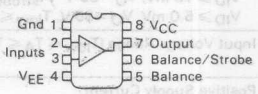


J-8 SUFFIX
CERAMIC PACKAGE
CASE 693-02



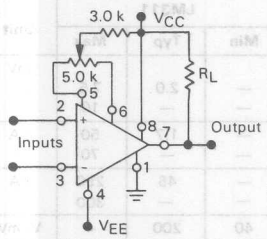
D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SO-8
(LM211/LM311 Only)



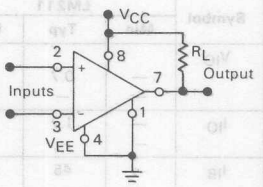


TYPICAL COMPARATOR DESIGN CONFIGURATIONS

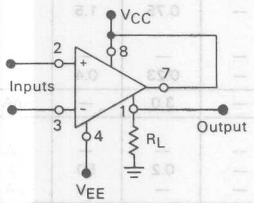
Split Power-Supply with Offset Balance



Single Supply

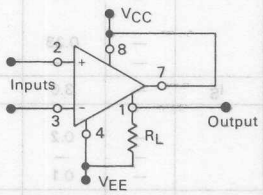


Ground-Referred Load



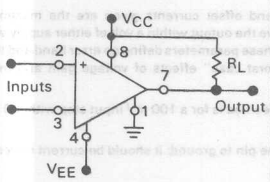
Input polarity is reversed when Gnd pin is used as an output.

Load Referred to Negative Supply

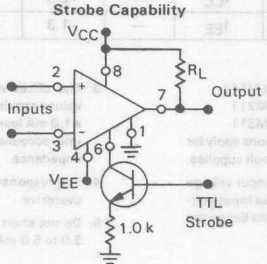


Input polarity is reversed when Gnd pin is used as an output.

Load Referred to Positive Supply



Strobe Capability



ORDERING INFORMATION

Device	Temperature Range	Package
LM111H LM111J-8	−55°C to +125°C	Metal Can Ceramic DIP
LM211D LM211H LM211J-8	−25°C to +85°C	SO-8 Metal Can Ceramic DIP
LM311D LM311J-8 LM311N	0°C to +70°C	SO-8 Ceramic DIP Plastic DIP

2

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value		Unit
		LM111 LM211	LM311	
Total Supply Voltage	$V_{CC}+\lvert V_{EE}\rvert$	36	36	Vdc
Output to Negative Supply Voltage	$V_O - V_{EE}$	50	40	Vdc
Ground to Negative Supply Voltage	V_{EE}	30	30	Vdc
Input Differential Voltage	V_{ID}	±30	±30	Vdc
Input Voltage (Note 2)	V_{in}	±15	±15	Vdc
Voltage at Strobe Pin	—	V_{CC} to V_{CC}-5	V_{CC} to V_{CC}-5	Vdc
Power Dissipation and Thermal Characteristics Metal Package Derate above T_A = +25°C Plastic and Ceramic Dual In-Line Packages Derate above T_A = +25°C	 P_D $1/\theta_{JA}$ P_D $1/\theta_{JA}$	 680 5.5 625 5.0		 mW mW/°C mW mW/°C
Operating Ambient Temperature Range	T_A	−55 to +125 −25 to +85 —	— — 0 to +70	°C
Operating Junction Temperature	$T_{J(max)}$	+150	+150	°C
Storage Temperature Range	T_{stg}	−65 to +150	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25°C unless otherwise noted [Note 1].)

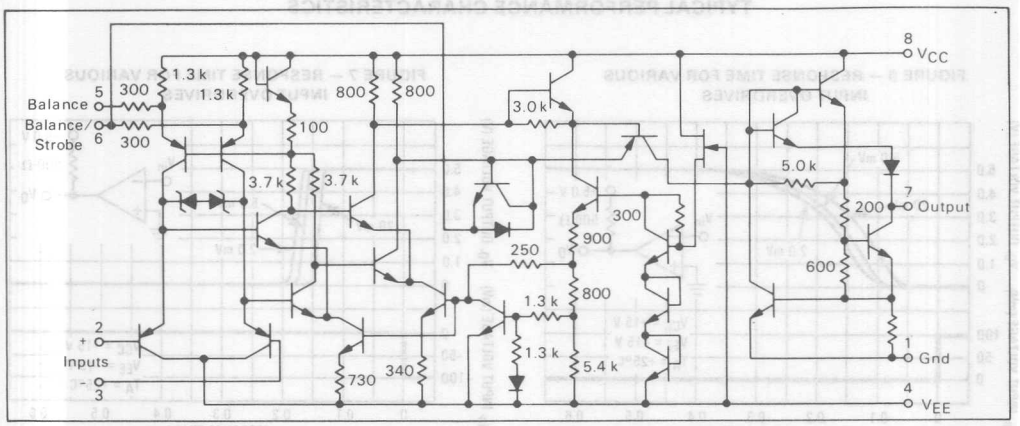
Characteristic	Symbol	LM111 LM211			LM311			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 3) $R_S \leq 50$ kΩ, T_A = +25°C $R_S \leq 50$ kΩ, $T_{low} \leq T_A \leq T_{high}$*	V_{IO}	 —	 0.7	 3.0	 —	 2.0	 7.5	mV
		—	—	4.0	—	—	10	
Input Offset Current (Note 3) T_A = +25°C $T_{low} \leq T_A \leq T_{high}$*	I_{IO}	—	1.7	10	—	1.7	50	nA
		—	—	20	—	—	70	
Input Bias Current, T_A = +25°C $T_{low} \leq T_A \leq T_{high}$*	I_{IB}	—	45	100	—	45	250	nA
		—	—	150	—	—	300	
Voltage Gain	A_V	40	200	—	40	200	—	V/mV
Response Time (Note 4)		—	200	—	—	200	—	ns
Saturation Voltage $V_{ID} \leq -5.0$ mV, I_O = 50 mA, T_A = +25°C $V_{ID} \leq -10$ mV, I_O = 50 mA, T_A = +25°C $V_{CC} \geq 4.5$ V, V_{EE} = 0, $T_{low} \leq T_A \leq T_{high}$* $V_{ID} \leq -6.0$ mV, $I_{sink} \leq 8.0$ mA $V_{ID} \leq -10$ mV, $I_{sink} \leq 8.0$ mA	V_{OL}	 — — — —	 0.75 — 0.23 —	 1.5 — 0.4 —	 — — — —	 — 0.75 — 0.23	 — 1.5 — 0.4	V
Strobe "On" Current (Note 5)	I_S	—	3.0	—	—	3.0	—	mA
Output Leakage Current $V_{ID} \geq 5.0$ mV, V_O = 35 V, T_A = +25°C $V_{ID} \geq 10$ mV, V_O = 35 V, I_{strobe} = 3.0 mA $V_{ID} \geq 5.0$ mV, V_O = 35 V, $T_{low} \leq T_A \leq T_{high}$*		 — — —	 0.2 — 0.1	 10 — 0.5	 — — —	 — 0.2 —	 — 50 —	 nA nA μA
Input Voltage Range ($T_{low} \leq T_A \leq T_{high}$*)	V_{IR}	−14.5	−14.7 to 13.8	13.0	−14.5	−14.7 to 13.8	13.0	V
Positive Supply Current	I_{CC}	—	+2.4	+6.0	—	+2.4	+7.5	mA
Negative Supply Current	I_{EE}	—	−1.3	−5.0	—	−1.3	−5.0	mA

NOTES:

* T_{low} = −55°C for LM111, = −25°C for LM211, = 0°C for LM311; T_{high} = +125°C for LM111, = +85°C for LM211, = +70°C for LM311

1. Offset voltage, offset current and bias current specifications apply for a supply voltage range from a single 5.0 volt supply up to ±15 volt supplies.
2. This rating applies for ±15 volt supplies. The positive input voltage limit is 30 volts above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30 volts below the positive supply, whichever is less.
3. The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1.0 mA load. Thus, these parameters define an error band and take into account the "worst case" effects of voltage gain and input impedance.
4. The response time specified is for a 100 mV input step with 5.0 mV overdrive.
5. Do not short the strobe pin to ground; it should be current driven at 3.0 to 5.0 mA.

FIGURE 1 — CIRCUIT SCHEMATIC



TYPICAL PERFORMANCE CHARACTERISTICS

FIGURE 2 — INPUT BIAS CURRENT versus TEMPERATURE

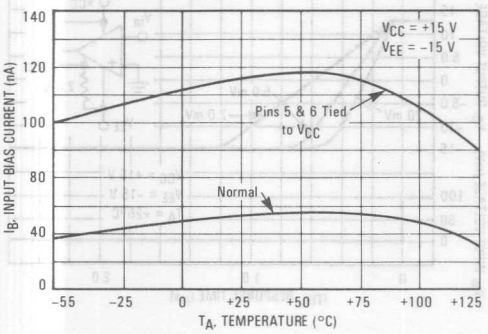


FIGURE 3 — INPUT OFFSET CURRENT versus TEMPERATURE

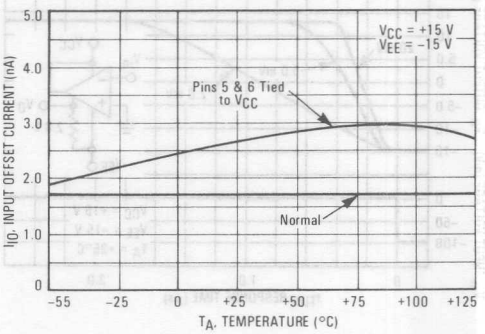


FIGURE 4 — INPUT BIAS CURRENT versus DIFFERENTIAL INPUT VOLTAGE

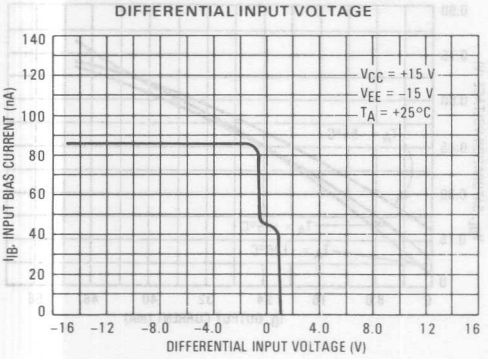
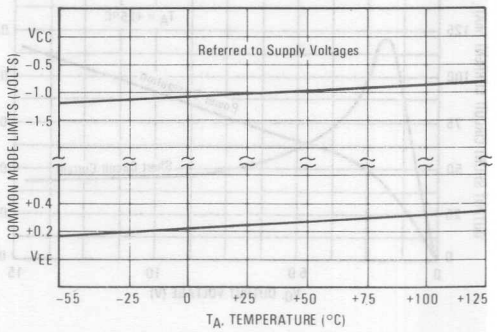


FIGURE 5 — COMMON MODE LIMITS versus TEMPERATURE



TYPICAL PERFORMANCE CHARACTERISTICS

FIGURE 6 — RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

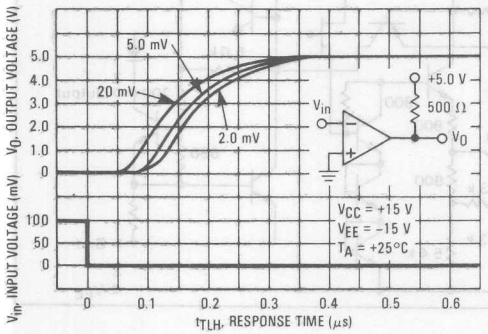


FIGURE 7 — RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

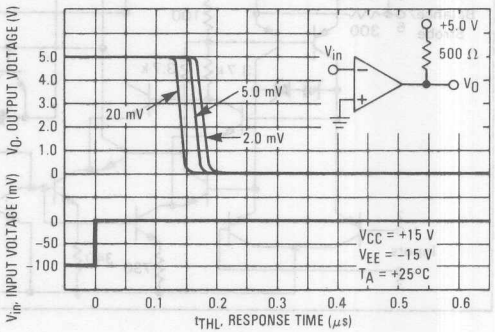


FIGURE 8 — RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

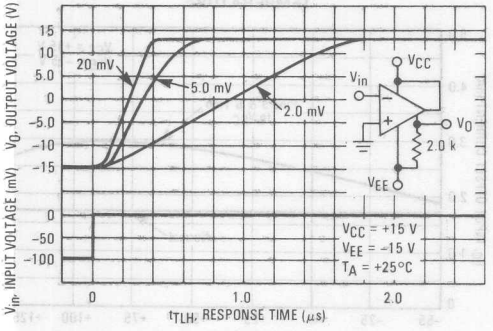


FIGURE 9 — RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

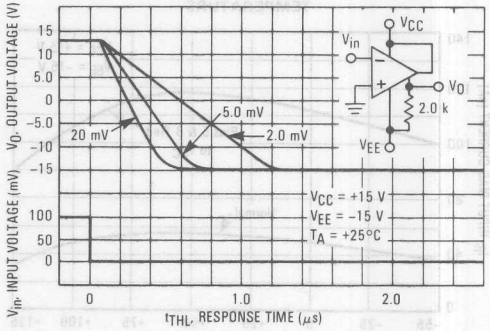


FIGURE 10 — OUTPUT SHORT CIRCUIT CURRENT CHARACTERISTICS AND POWER DISSIPATION

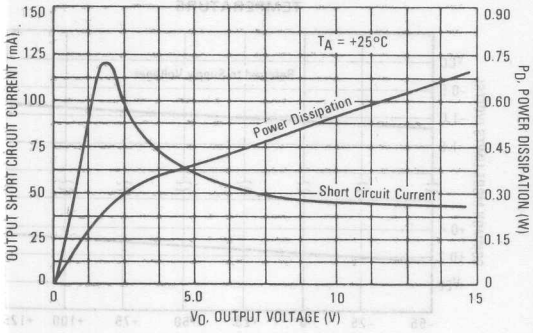
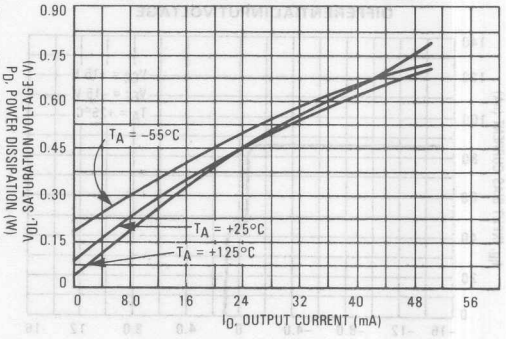


FIGURE 11 — OUTPUT SATURATION VOLTAGE versus OUTPUT CURRENT



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

FIGURE 12 — OUTPUT LEAKAGE CURRENT versus TEMPERATURE

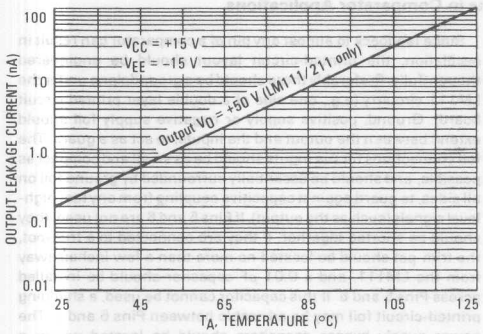


FIGURE 13 — POWER SUPPLY CURRENT versus SUPPLY VOLTAGE

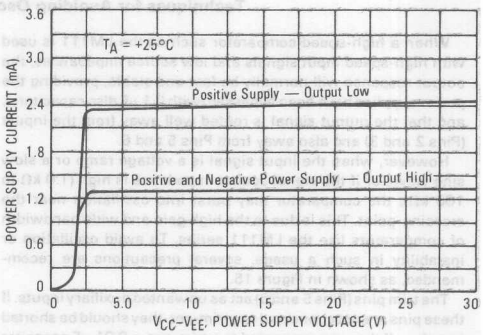
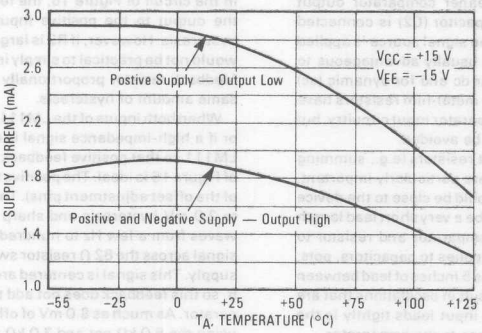


FIGURE 14 — POWER SUPPLY CURRENT versus TEMPERATURE



APPLICATIONS INFORMATION

FIGURE 15 — IMPROVED METHOD OF ADDING HYSTERESIS WITHOUT APPLYING POSITIVE FEEDBACK TO THE INPUTS

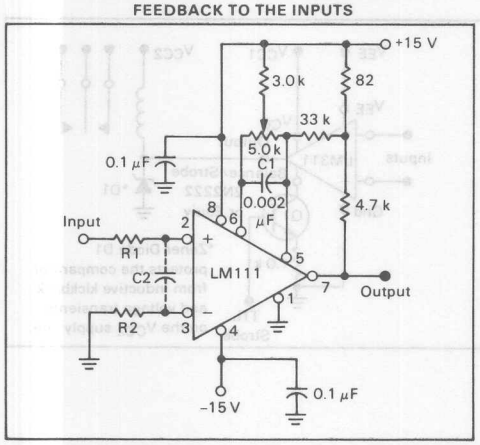
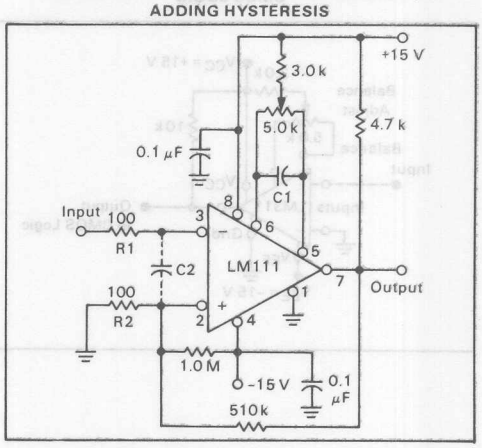


FIGURE 16 — CONVENTIONAL TECHNIQUE FOR ADDING HYSTERESIS



2

APPLICATIONS INFORMATION

Techniques for Avoiding Oscillations in Comparator Applications

When a high-speed comparator such as the LM111 is used with high-speed input signals and low source impedances, the output response will normally be fast and stable, providing the power supplies have been bypassed (with 0.1 μF disc capacitors), and that the output signal is routed well away from the inputs (Pins 2 and 3) and also away from Pins 5 and 6.

However, when the input signal is a voltage ramp or a slow sine wave, or if the signal source impedance is high (1.0 kΩ to 100 kΩ), the comparator may burst into oscillation near the crossing-point. This is due to the high gain and wide bandwidth of comparators like the LM111 series. To avoid oscillation or instability in such a usage, several precautions are recommended, as shown in Figure 15.

The trim pins (Pins 5 and 6) act as unwanted auxiliary inputs. If these pins are not connected to a trim-pot, they should be shorted together. If they are connected to a trim-pot, a 0.01 μF capacitor (C1) between Pins 5 and 6 will minimize the susceptibility to ac coupling. A smaller capacitor is used if Pin 5 is used for positive feedback as in Figure 15.

Certain sources will produce a cleaner comparator output waveform if a 100 pF to 1000 pF capacitor (C2) is connected directly across the input pins. When the signal source is applied through a resistive network, R1, it is usually advantageous to choose R2 of the same value, both for dc and for dynamic (ac) considerations. Carbon, tin-oxide, and metal-film resistors have all been used with good results in comparator input circuitry, but inductive wirewound resistors should be avoided.

When comparator circuits use input resistors (e.g., summing resistors), their value and placement are particularly important. In all cases the body of the resistor should be close to the device or socket. In other words, there should be a very short lead length or printed-circuit foil run between comparator and resistor to radiate or pick up signals. The same applies to capacitors, pots, etc. For example, if R1 = 10 kΩ, as little as 5 inches of lead between the resistors and the input pins can result in oscillations that are very hard to dampen. Twisting these input leads tightly is the best alternative to placing resistors close to the comparator.

Since feedback to almost any pin of a comparator can result in oscillation, the printed-circuit layout should be engineered thoughtfully. Preferably there should be a groundplane under the LM111 circuitry (e.g., one side of a double layer printed circuit board). Ground, positive supply or negative supply foil should extend between the output and the inputs, to act as a guard. The foil connections for the inputs should be as small and compact as possible, and should be essentially surrounded by ground foil on all sides, to guard against capacitive coupling from any fast high-level signals (such as the output). If Pins 5 and 6 are not used, they should be shorted together. If they are connected to a trim-pot, the trim-pot should be located no more than a few inches away from the LM111, and a 0.01 μF capacitor should be installed across Pins 5 and 6. If this capacitor cannot be used, a shielding printed-circuit foil may be advisable between Pins 6 and 7. The power supply bypass capacitors should be located within a couple inches of the LM111.

A standard procedure is to add hysteresis to a comparator to prevent oscillation, and to avoid excessive noise on the output. In the circuit of Figure 16, the feedback resistor of 510 kΩ from the output to the positive input will cause about 3.0 mV of hysteresis. However, if R2 is larger than 100 Ω, such as 50 kΩ, it would not be practical to simply increase the value of the positive feedback resistor proportionally above 510 kΩ to maintain the same amount of hysteresis.

When both inputs of the LM111 are connected to active signals, or if a high-impedance signal is driving the positive input of the LM111 so that positive feedback would be disruptive, the circuit of Figure 15 is ideal. The positive feedback is applied to Pin 5 (one of the offset adjustment pins). This will be sufficient to cause 1.0 to 2.0 mV hysteresis and sharp transitions with input triangle waves from a few Hz to hundreds of kHz. The positive-feedback signal across the 82 Ω resistor swings 240 mV below the positive supply. This signal is centered around the nominal voltage at Pin 5, so this feedback does not add to the offset voltage of the comparator. As much as 8.0 mV of offset voltage can be trimmed out, using the 5.0 kΩ pot and 3.0 kΩ resistor as shown.

FIGURE 17 — ZERO-CROSSING DETECTOR DRIVING CMOS LOGIC

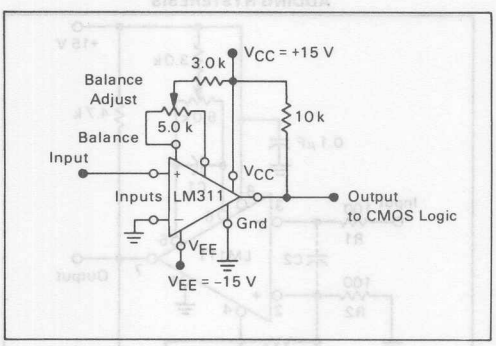
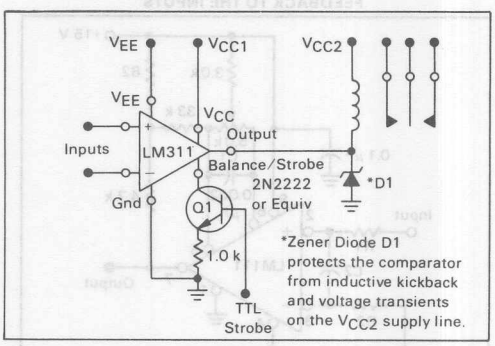


FIGURE 18 — RELAY DRIVER WITH STROBE CAPABILITY



MOTOROLA

LM124, LM224, LM324, LM324A LM2902

2

Specifications and Applications Information

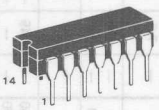
QUAD LOW POWER OPERATIONAL AMPLIFIERS

The LM124 Series are low-cost, quad operational amplifiers with true differential inputs. These have several distinct advantages over standard operational amplifier types in single supply applications. The quad amplifier can operate at supply voltages as low as 3.0 Volts or as high as 32 Volts with quiescent currents about one fifth of those associated with the MC1741 (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

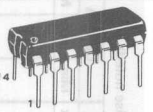
- Short Circuited Protected Outputs
- True Differential Input Stage
- Single Supply Operation: 3.0 to 32 Volts
- Low Input Bias Currents: 100 nA Max (LM324A)
- Four Amplifiers Per Package
- Internally Compensated
- Common Mode Range Extends to Negative Supply
- Industry Standard Pinouts

QUAD DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUIT



J SUFFIX
CERAMIC PACKAGE
CASE 632-08

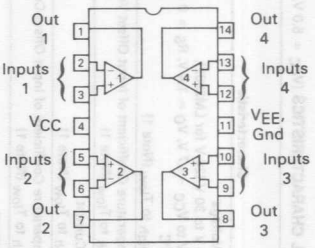


N SUFFIX
PLASTIC PACKAGE
CASE 646-06
(LM224, LM324, LM2902 Only)



D SUFFIX
PLASTIC PACKAGE
CASE 751A-02
SO-14

PIN CONNECTIONS



(Top View)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	LM124 LM224 LM324,A	LM2902	Unit
Power Supply Voltages Single Supply Split Supplies	 V_{CC} V_{CC}, V_{EE}	 32 ±16	 26 ±13	Vdc
Input Differential Voltage Range (1)	V_{IDR}	±32	±26	Vdc
Input Common Mode Voltage Range	V_{ICR}	−0.3 to 32	−0.3 to 26	Vdc
Input Forward Current (2) (V_I < −0.3 V)	I_{IF}	50	—	mA
Output Short Circuit Duration	t_S	Continuous		
Junction Temperature Ceramic Package Plastic Packages	T_J	 175 150		°C
Storage Temperature Range Ceramic Package Plastic Packages	T_{stg}	 −65 to +150 −55 to +125		°C
Operating Ambient Temperature Range LM124 LM224 LM324 LM324A LM2902	T_A	 −55 to +125 −25 to +85 0 to +70 0 to +70 —	 — — — — −40 to +85	°C

(1) Split Power Supplies.
(2) This input current will only exist when the voltage is negative at any of the input leads. Normal output states will reestablish when the input voltage returns to a voltage greater than −0.3 V.

ORDERING INFORMATION

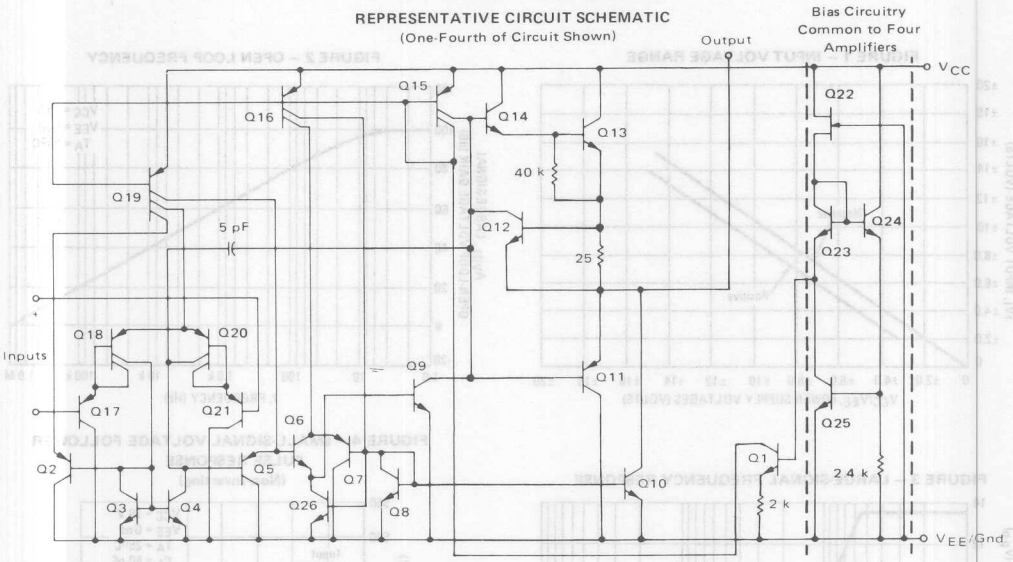
Device	Temperature Range	Package
LM124J	−55 to +125°C	Ceramic DIP
LM2902D	−40 to +85°C	SO-14
LM2902J		Ceramic DIP
LM2902N		Plastic DIP
LM224D	−25 to +85°C	SO-14
LM224J		Ceramic DIP
LM224N		Plastic DIP
LM324AD	0 to +70°C	SO-14
LM324AN		Plastic DIP
LM324D		SO-14
LM324J		Ceramic DIP
LM324N		Plastic DIP

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C unless otherwise noted)

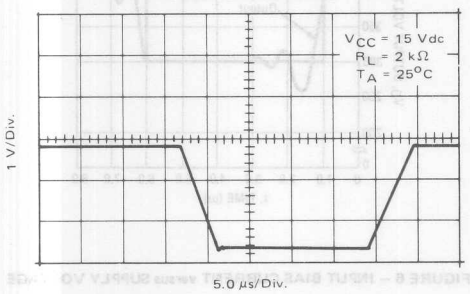
Characteristic	Symbol	LM124/LM224			LM324A			LM324			LM2902		
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
Input Offset Voltage V_{CC} = 5.0 V to 30 V (26 V for LM2902), V_{ICR} = 0 V to V_{CC} − 1.7 V, V_O ≈ 1.4 V, R_S = 0 Ω T_A = 25°C T_A = T_{high} to T_{low} (Note 1)	V_{IO}	— —	2.0 —	5.0 7.0	— —	2.0 —	3.0 5.0	— —	2.0 —	7.0 9.0	— —	2.0 —	7.0 10
Average Temperature Coefficient of Input Offset Voltage T_A = T_{high} to T_{low} (Note 1)	$\Delta V_{IO}/\Delta T$	—	7.0	—	—	7.0	30	—	7.0	—	—	7.0	—
Input Offset Current T_A = T_{high} to T_{low} (Note 1)	I_{IO}	— —	3.0 —	30 100	— —	5.0 —	30 75	— —	5.0 —	50 150	— —	5.0 —	50 200
Average Temperature Coefficient of Input Offset Current T_A = T_{high} to T_{low} (Note 1)	$\Delta I_{IO}/\Delta T$	—	10	—	—	10	300	—	10	—	—	10	—
Input Bias Current T_A = T_{high} to T_{low} (Note 1)	I_{IB}	— —	−90 —	−150 −300	— —	−45 —	−100 −200	— —	−90 —	−250 −500	— —	−90 —	−250 −500
Input Common-Mode Voltage Range (Note 2) V_{CC} = 30 V (26 V for LM2902) V_{CC} = 30 V (26 V for LM2902), T_A = T_{high} to T_{low}	V_{ICR}	0 0	— —	28.3 28	0 0	— —	28.3 28	0 0	— —	28.3 28	0 0	— —	24.3 24
Differential Input Voltage Range	V_{IDR}	—	—	V_{CC}	—	—	V_{CC}	—	—	V_{CC}	—	—	V_{CC}
Large Signal Open-Loop Voltage Gain R_L = 2.0 kΩ, V_{CC} = 15 V, For Large V_O Swing, T_A = T_{high} to T_{low} (Note 1)	A_{VOL}	50 25	100 —	— —	25 15	100 —	— —	25 15	100 —	— —	— —	100 —	— —
Channel Separation 1.0 kHz ≤ f ≤ 20 kHz, Input Referenced	—	—	−120	—	—	−120	—	—	−120	—	—	−120	—
Common-Mode Rejection Ratio R_S ≤ 10 kΩ	CMRR	70	85	—	65	70	—	65	70	—	50	70	—
Power Supply Rejection Ratio	PSRR	65	100	—	65	100	—	65	100	—	50	100	—
Output Voltage Range R_L = 2.0 kΩ (R_L ≥ 10 kΩ for LM2902)	V_{OR}	0	—	3.3	0	—	3.3	0	—	3.3	0	—	3.3
Output Voltage — High Limit (T_A = T_{high} to T_{low}) (Note 1) V_{CC} = 30 V (26 V for LM2902), R_L = 2.0 kΩ V_{CC} = 30 V (26 V for LM2902), R_L = 10 kΩ	V_{OH}	26 27	— 28	— —	26 27	— 28	— —	26 27	— 28	— —	22 23	— 24	— —
Output Voltage — Low Limit V_{CC} = 5.0 V, R_L = 10 kΩ, T_A = T_{high} to T_{low} (Note 1)	V_{OL}	—	5.0	20	—	5.0	20	—	5.0	20	—	5.0	100
Output Source Current (V_{ID} = +1.0 V, V_{CC} = 15 V) T_A = 25°C T_A = T_{high} to T_{low} (Note 1)	I_{O+}	20 10	40 20	— —	20 10	40 20	— —	20 10	40 20	— —	20 10	40 20	— —
Output Sink Current (V_{ID} = −1.0 V, V_{CC} = 15 V T_A = 25°C T_A = T_{high} to T_{low} (Note 1) V_{ID} = −1.0 V, V_O = 200 mV, T_A = 25°C	I_{O-}	10 5.0 12	20 8.0 50	— — —	10 5.0 12	20 8.0 50	— — —	10 5.0 12	20 8.0 50	— — —	10 5.0 —	20 8.0 —	— — —
Output Short Circuit to Ground (Note 3)	I_{os}	—	40	60	—	40	60	—	40	60	—	40	60
Power Supply Current (T_A = T_{high} to T_{low}) (Note 1) V_{CC} = 30 V (26 V for LM2902), V_O = 0 V, R_L = ∞ V_{CC} = 5.0 V, V_O = 0 V, R_L = ∞	I_{CC}	— —	— —	3.0 1.2	— —	1.4 0.7	3.0 1.2	— —	— —	3.0 1.2	— —	— —	3.0 1.2

NOTES:
(1) T_{low} = −55°C for LM124
= −40°C for LM2902
= −25°C for LM224
= 0°C for LM324,A
T_{high} = +125°C for LM124
= +85°C for LM2902 and LM224
= +70°C for LM324,A
(2) The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V_{CC} − 1.7 V, but either or both inputs can go to +32 V without damage (+26 V for LM2902).
(3) Short circuits from the output to V_{CC} can cause excessive heating and eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

REPRESENTATIVE CIRCUIT SCHEMATIC
(One-Fourth of Circuit Shown)



LARGE SIGNAL VOLTAGE
FOLLOWER RESPONSE

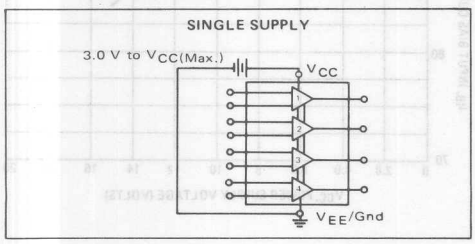


CIRCUIT DESCRIPTION

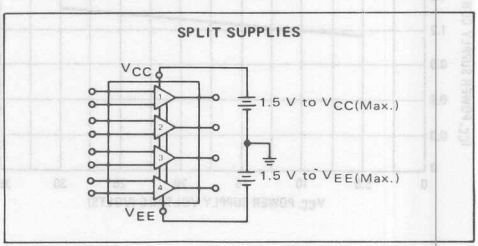
The LM124 Series is made using four internally compensated, two-stage operational amplifiers. The first stage of each consists of differential input devices Q20 and Q18 with input buffer transistors Q21 and Q17 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance a smaller compensation capacitor (only 5 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q20 and Q18. Another feature of this input stage is that the input common-mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single-ended converter. The second stage consists of a standard current source load amplifier stage.

Each amplifier is biased from an internal-voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

SINGLE SUPPLY



SPLIT SUPPLIES



2

TYPICAL PERFORMANCE CURVES

FIGURE 1 – INPUT VOLTAGE RANGE

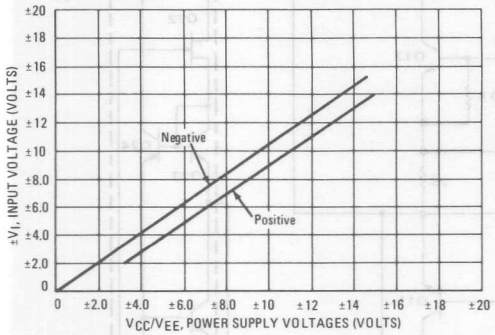


FIGURE 2 – OPEN LOOP FREQUENCY

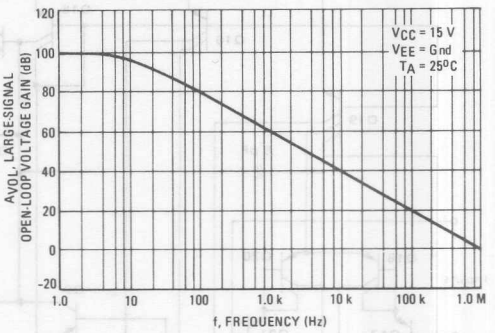


FIGURE 3 – LARGE-SIGNAL FREQUENCY RESPONSE

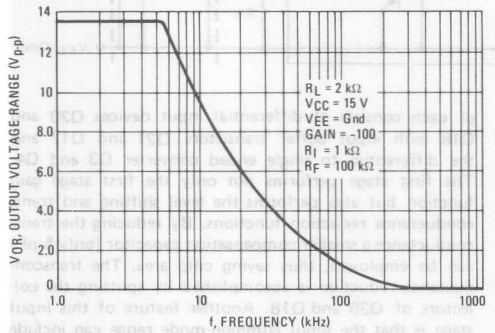


FIGURE 4 – SMALL-SIGNAL VOLTAGE FOLLOWER PULSE RESPONSE (Non-Inverting)

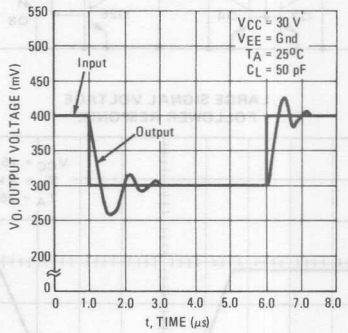


FIGURE 5 – POWER SUPPLY CURRENT versus POWER SUPPLY VOLTAGE

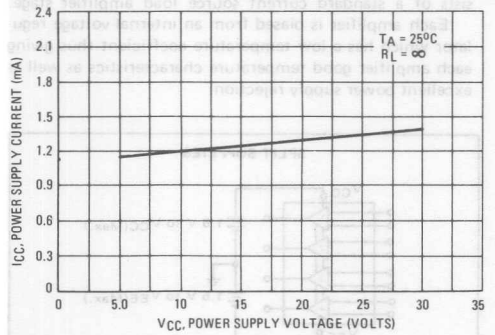
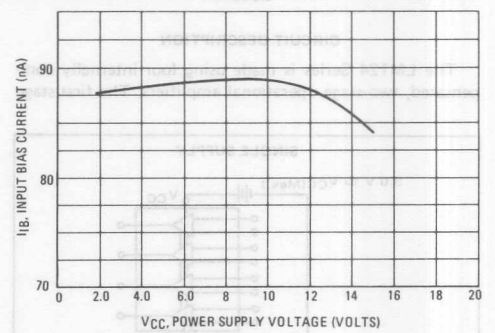
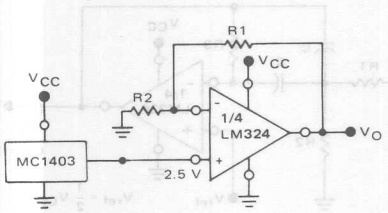


FIGURE 6 – INPUT BIAS CURRENT versus SUPPLY VOLTAGE



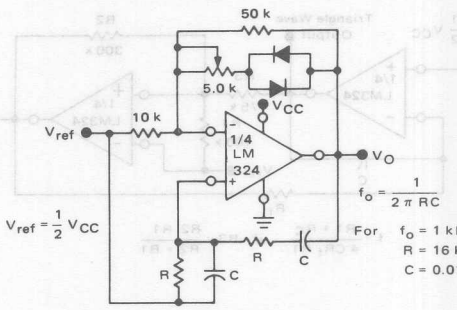
APPLICATIONS INFORMATION

FIGURE 7 – VOLTAGE REFERENCE



$$V_O = 2.5\ V\left(1 + \frac{R1}{R2}\right)$$

FIGURE 8 – WIEN BRIDGE OSCILLATOR

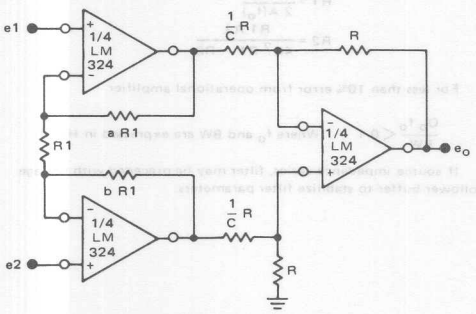


$$f_o = \frac{1}{2\pi RC}$$

$$V_{ref} = \frac{1}{2} V_{CC}$$

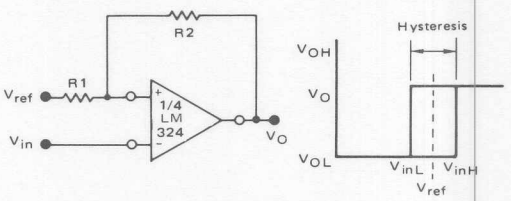
For f_o = 1 kHz
R = 16 kΩ
C = 0.01 μF

FIGURE 9 – HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER



$$e_o = C\ (1 + a + b)\ (e2 - e1)$$

FIGURE 10 – COMPARATOR WITH HYSTERESIS

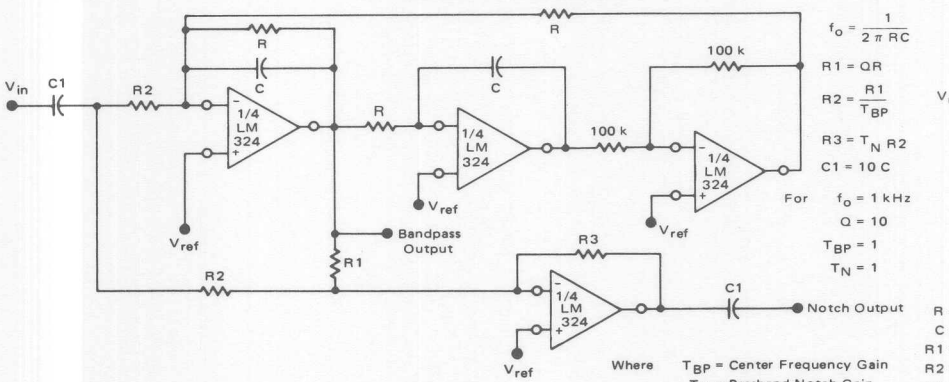


$$V_{inL} = \frac{R1}{R1 + R2}\ (V_{OL} - V_{ref}) + V_{ref}$$

$$V_{inH} = \frac{R1}{R1 + R2}\ (V_{OH} - V_{ref}) + V_{ref}$$

$$H = \frac{R1}{R1 + R2}\ (V_{OH} - V_{OL})$$

FIGURE 11 – BI-QUAD FILTER



$$f_o = \frac{1}{2\pi RC}$$

R1 = QR

$$R2 = \frac{R1}{T_{BP}}$$

$R3 = T_N\ R2$

C1 = 10 C

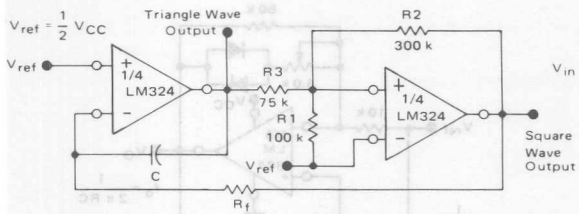
$$V_{ref} = \frac{1}{2} V_{CC}$$

For f_o = 1 kHz
Q = 10
T_{BP} = 1
T_N = 1

R = 160 kΩ
C = 0.001 μF
R1 = 1.6 MΩ
R2 = 1.6 MΩ
R3 = 1.6 MΩ

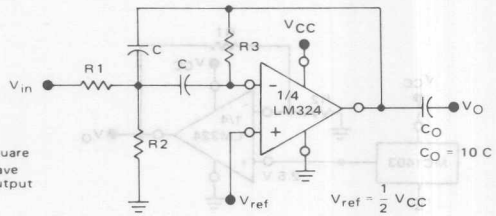
Where T_{BP} = Center Frequency Gain
T_N = Passband Notch Gain

FIGURE 12 – FUNCTION GENERATOR



$$f = \frac{R1 + R_C}{4 C R_f R1} \quad \text{if} \quad R3 = \frac{R2\ R1}{R2 + R1}$$

FIGURE 13 – MULTIPLE FEEDBACK BANDPASS FILTER



Given f_o = Center Frequency
$A(f_o)$ = Gain at Center Frequency

Choose Value f_o, C
Then

$$R3 = \frac{Q}{\pi f_o C}$$

$$R1 = \frac{R3}{2 A(f_o)}$$

$$R2 = \frac{R1\ R3}{4Q^2 R1 - R3}$$

For less than 10% error from operational amplifier

$$\frac{Q_o f_o}{BW} < 0.1$$ Where f_o and BW are expressed in Hz.

If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

MOTOROLA

LM139, A
LM239, A LM2901
LM339, A MC3302

2

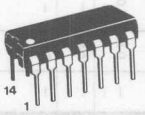
QUAD SINGLE SUPPLY COMPARATORS

These comparators are designed for use in level detection, low-level sensing and memory applications in Consumer Automotive and Industrial electronic applications.

- Single or Split Supply Operation
- Low Input Bias Current — 25 nA (Typ)
- Low Input Offset Current — ±5.0 nA (Typ)
- Low Input Offset Voltage — ±1.0 mV (Typ LM139A Series)
- Input Common-Mode Voltage Range to Gnd
- Low Output Saturation Voltage — 130 mV (Typ) @ 4.0 mA
- TTL and CMOS Compatible

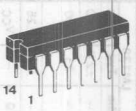
QUAD COMPARATORS

SILICON MONOLITHIC INTEGRATED CIRCUIT



N, P SUFFIX
PLASTIC PACKAGE
CASE 646-06

J, L SUFFIX
CERAMIC PACKAGE
CASE 632-08



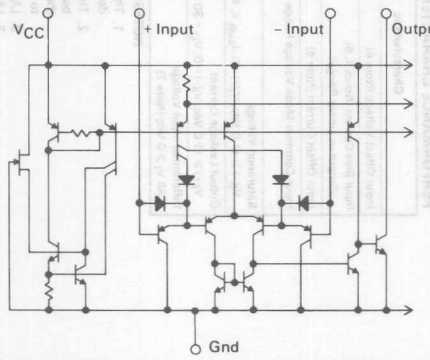


D SUFFIX
PLASTIC PACKAGE
CASE 751A-02
SO-14

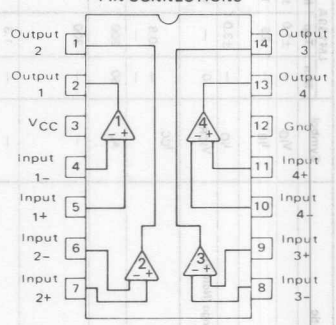
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage LM139, A/LM239, A/ LM339A/LM2901 MC3302	V_{CC}	+36 or ±18 +30 or ±15	Vdc
Input Differential Voltage Range LM139, A/LM239, A/LM339, A/LM2901 MC3302	V_{IDR}	 36 30	Vdc
Input Common Mode Voltage Range	V_{ICR}	-0.3 to V_{CC}	Vdc
Output Short-Circuit to Gnd (Note 1)	I_{SC}	Continuous	
Input Current (V_{in} < -0.3 Vdc) (Note 2)	I_{in}	50	mA
Power Dissipation @ T_A = 25°C Ceramic Package Derate above 25°C Plastic Package Derate above 25°C	P_D	 1.0 8.0 1.0 8.0	 Watts mW/°C Watts mW/°C
Operating Ambient Temperature Range LM139, A LM239, A LM2901/MC3302 LM339, A	T_A	 −55 to +125 −25 to +85 −40 to +85 0 to +70	 °C
Storage Temperature Range	T_{stg}	-65 to +150	°C

FIGURE 1 — CIRCUIT SCHEMATIC (Diagram shown is for 1 comparator)



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
LM139J, AJ	−55°C to +125°C	Ceramic DIP
LM239D, AD LM239J, AJ LM239N, AN	−25°C to +85°C	SO-14 Ceramic DIP Plastic DIP
LM339D, AD LM339J, AJ LM339N, AN	0°C to +70°C	SO-14 Ceramic DIP Plastic DIP
LM2901D LM2901N MC3302L MC3302P	−40°C to +85°C	SO-14 Plastic DIP Ceramic DIP Plastic DIP

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	LM139A			LM239A/339A			LM139			LM239/339			LM2901			MC3302			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 4)	V_{IO}	—	±1.0	±2.0	—	±1.0	±2.0	—	±2.0	±5.0	—	±2.0	±5.0	—	±2.0	±7.0	—	±3.0	±20	mVdc
Input Bias Current (Notes 4, 5) (Output in Linear Range)	I_{IB}	—	25	100	—	25	250	—	25	100	—	25	250	—	25	250	—	25	500	nA
Input Offset Current (Note 4)	I_{IO}	—	±3.0	±25	—	±5.0	±50	—	±3.0	±25	—	±5.0	±50	—	±5.0	±50	—	±3.0	±100	nA
Input Common-Mode Voltage Range (Note 7)	V_{ICR}	0	—	V_{CC} -1.5	0	—	V_{CC} -1.5	0	—	V_{CC} -1.5	0	—	V_{CC} -1.5	0	—	V_{CC} -1.5	0	—	V_{CC} -1.5	V
Supply Current R_L = ∞ (For All Comparators) R_L = ∞, V_{CC} = 30 Vdc	I_{CC}	— —	0.8 —	2.0 —	— —	0.8 —	2.0 —	— —	0.8 —	2.0 —	— —	0.8 —	2.0 —	— —	0.8 1.0	2.0 2.5	— —	0.8 —	2.0 —	mA
Voltage Gain R_L ≥ 15 kΩ, V_{CC} = 15 Vdc	A_V	50	200	—	50	200	—	—	200	—	—	200	—	25	100	—	2	30	—	V/mV
Large Signal Response Time V_I = TTL Logic Swing, V_{ref} = 1.4 Vdc, V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ	—	—	300	—	—	300	—	—	300	—	—	300	—	—	300	—	—	300	—	ns
Response Time (Note 6) V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ	—	—	1.3	—	—	1.3	—	—	1.3	—	—	1.3	—	—	1.3	—	—	1.3	—	μs
Output Sink Current $V_I(-)$ ≥ +1.0 Vdc, $V_I(+)$ = 0, V_O ≤ 1.5 Vdc	I_{sink}	6.0	16	—	6.0	16	—	6.0	16	—	6.0	16	—	6.0	16	—	6.0	16	—	mA
Saturation Voltage $V_I(-)$ ≥ +1.0 Vdc, $V_I(+)$ = 0, I_{sink} ≤ 4.0 mA	V_{sat}	—	130	400	—	130	400	—	130	400	—	130	400	—	130	400	—	130	500	mV
Output Leakage Current $V_I(+)$ ≥ +1.0 Vdc, $V_I(-)$ = 0, V_O = +5.0 Vdc	I_{OL}	—	0.1	—	—	0.1	—	—	0.1	—	—	0.1	—	—	0.1	—	—	0.1	—	nA

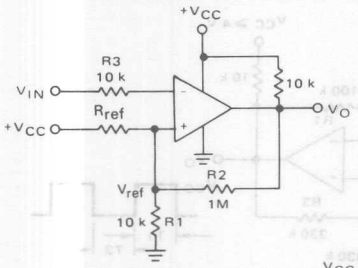
PERFORMANCE CHARACTERISTICS (V_{CC} = +5.0 Vdc, T_A = T_{low} to T_{high} [Note 3])

Characteristic	Symbol	LM139A			LM239A/339A			LM139			LM239/339			LM2901			MC3302			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 4)	V_{IO}	—	—	±4.0	—	—	±4.0	—	—	±9.0	—	—	±9.0	—	—	±15	—	—	±40	mVdc
Input Bias Current (Notes 4, 5) (Output in Linear Range)	I_{IB}	—	—	300	—	—	400	—	—	300	—	—	400	—	—	500	—	—	1000	nA
Input Offset Current (Note 4)	I_{IO}	—	—	±100	—	—	±150	—	—	±100	—	—	±150	—	—	±200	—	—	±300	nA
Input Common-Mode Voltage Range	V_{ICR}	0	—	V_{CC} -2.0	0	—	V_{CC} -2.0	0	—	V_{CC} -2.0	0	—	V_{CC} -2.0	0	—	V_{CC} -2.0	0	—	V_{CC} -2.0	V
Saturation Voltage $V_I(-)$ ≥ +1.0 Vdc, $V_I(+)$ = 0, I_{sink} ≤ 4.0 mA	V_{sat}	—	—	700	—	—	700	—	—	700	—	—	700	—	—	700	—	—	700	mV
Output Leakage Current $V_I(+)$ ≥ +1.0 Vdc, $V_I(-)$ = 0, V_O = 30 Vdc	I_{OL}	—	—	1.0	—	—	1.0	—	—	1.0	—	—	1.0	—	—	1.0	—	—	1.0	μA
Differential Input Voltage All V_I ≥ 0 Vdc (Note 7)	V_{ID}	—	—	V_{CC}	—	—	V_{CC}	—	—	V_{CC}	—	—	V_{CC}	—	—	V_{CC}	—	—	V_{CC}	Vdc

NOTES:

1. The maximum output current may be as high as 20 mA, independent of the magnitude of V_{CC}. Output short circuits to V_{CC} can cause excessive heating and eventual destruction.
2. This magnitude of input current will only occur if the leads are driven more negative than ground or the negative supply voltage. This is due to the input PNP collector-base junction becoming forward biased, acting as an input clamp diode. There is also a lateral PNP parasitic transistor action which can cause the output voltage of the comparators to go to the V_{CC} voltage level (or ground if overdrive is large) during the time that an input is driven negative. This will not destroy the device when limited to the max rating and normal output states will recover when the inputs become ≥ ground or negative supply.
3. LM139/139A — T_{low} = −55°C, T_{high} = +125°C LM339/339A — T_{low} = 0°C, T_{high} = +70°C
   LM239/239A — T_{low} = −25°C, T_{high} = +85°C LM2901/MC3302 — T_{low} = −40°C, T_{high} = +85°C
4. At the output switch point, V_O ≈ 1.4 Vdc, R_S ≤ 100 Ω, 5.0 Vdc ≤ V_{CC} ≤ 30 Vdc, with the inputs over the full common-mode range (0 Vdc to V_{CC} − 1.5 Vdc).
5. The bias current flows out of the inputs due to the PNP input stage. This current is virtually constant, independent of the output state.
6. The response time specified is for a 100 mV input step with 5.0 mV overdrive. For larger signals, 300 ns is typical.
7. Positive excursions of input voltage may exceed the power supply level. As long as one of the inputs remain within the common-mode range, the comparator will provide the proper output state.

FIGURE 2 — INVERTING COMPARATOR WITH HYSTERESIS



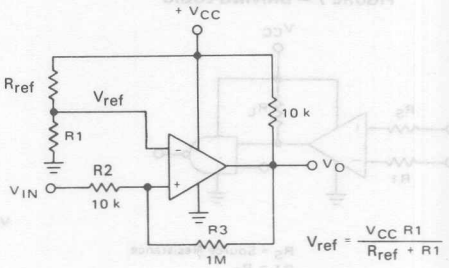
$$V_{ref} \approx \frac{V_{CC}\ R1}{R_{ref} + R1}$$

$$R3 \simeq R1 \,//\, R_{ref}//R2$$

$$V_H = \frac{R1//R_{ref}}{R1//R_{ref} + R2}\ (V_{Omax} - V_{Omin})$$

$$R2 >> R_{ref}//R1$$

FIGURE 3 — NON-INVERTING COMPARATOR WITH HYSTERESIS



$$V_{ref} = \frac{V_{CC}\ R1}{R_{ref} + R1}$$

$$R2 \simeq R1//R_{ref}$$

Amount of Hysteresis V_H

$$V_H = \frac{R2}{R2 + R3}\ (V_{Omax} - V_{Omin})$$

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, T_A = +25°C (each comparator) unless otherwise noted.)

FIGURE 4 — NORMALIZED INPUT OFFSET VOLTAGE

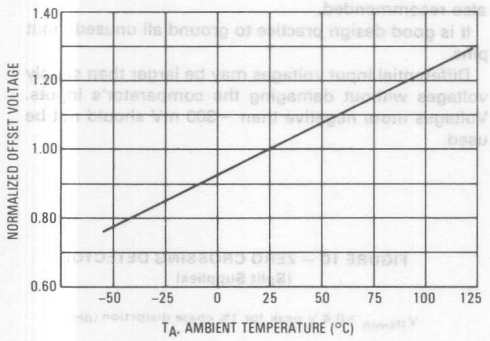


FIGURE 5 — INPUT BIAS CURRENT

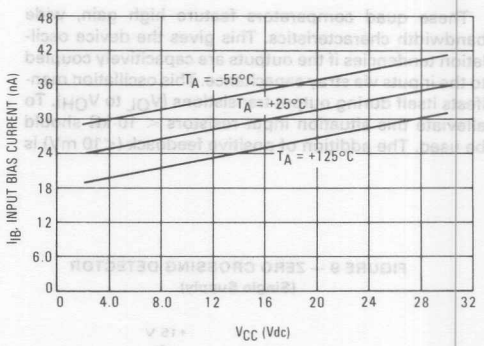


FIGURE 6 — OUTPUT SINK CURRENT versus OUTPUT SATURATION VOLTAGE

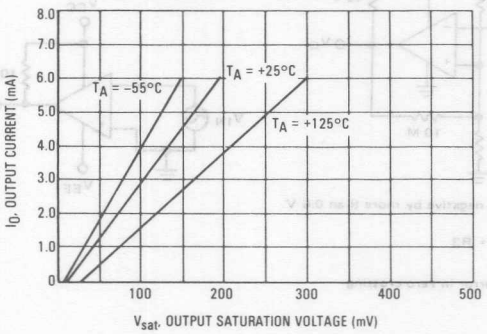
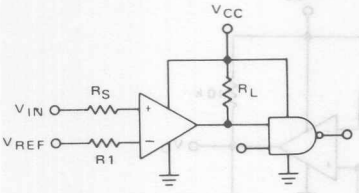


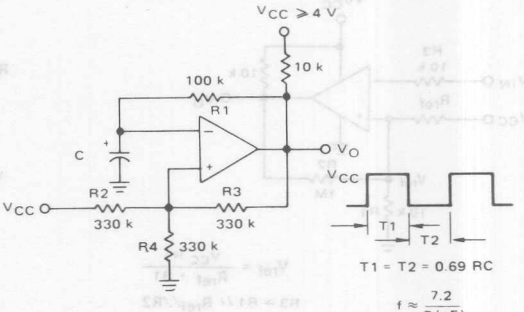
FIGURE 7 — DRIVING LOGIC



R_S = Source Resistance
$R1 \simeq R_S$

LOGIC	DEVICE	V_{CC} Volts	R_L kΩ
CMOS	1/4 MC14001	+15	100
TTL	1/4 MC7400	+5	10

FIGURE 8 — SQUAREWAVE OSCILLATOR



$T1 = T2 = 0.69\ RC$

$f \approx \frac{7.2}{C\,(\mu F)}$

$R2 = R3 = R4$

$R1 \approx R2//R3//R4$

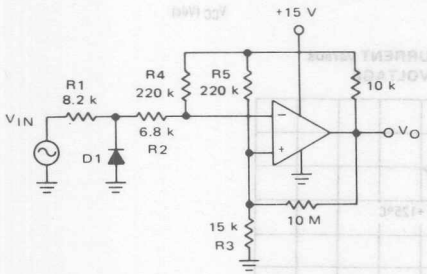
APPLICATIONS INFORMATION

These quad comparators feature high gain, wide bandwidth characteristics. This gives the device oscillation tendencies if the outputs are capacitively coupled to the inputs via stray capacitance. This oscillation manifests itself during output transistions (V_{OL} to V_{OH}). To alleviate this situation input resistors < 10 kΩ should be used. The addition of positive feedback (<10 mV) is also recommended.

It is good design practice to ground all unused input pins.

Differential input voltages may be larger than supply voltages without damaging the comparator's inputs. Voltages more negative than −300 mV should not be used.

FIGURE 9 — ZERO CROSSING DETECTOR (Single Supply)



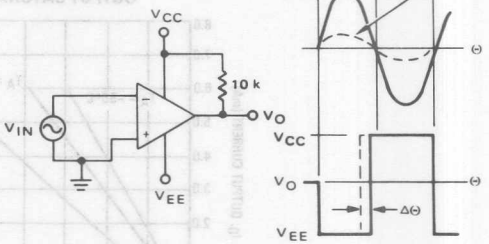
D1 prevents input from going negative by more than 0.6 V.

$R1 + R2 = R3$

$R3 \leq \frac{R5}{10}$ for small error in zero crossing

FIGURE 10 — ZERO CROSSING DETECTOR (Split Supplies)

$V_{INmin} \approx 0.4$ V peak for 1% phase distortion (Δθ).

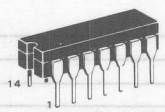


LM148
LM248
LM348

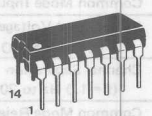
Specifications and Applications Information

(QUAD MC1741)
DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

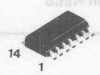
SILICON MONOLITHIC INTEGRATED CIRCUIT



J SUFFIX
CERAMIC PACKAGE
CASE 632-08



N SUFFIX
PLASTIC PACKAGE
CASE 646-06



D SUFFIX
PLASTIC PACKAGE
CASE 751A-02
SO-14

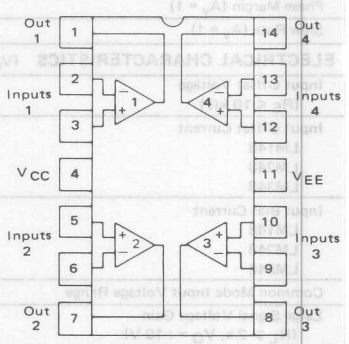
(QUAD MC1741)
OPERATIONAL AMPLIFIERS

The LM148 series is a true quad MC1741. Integrated on a single monolithic chip are four independent, low power operational amplifiers which have been designed to provide operating characteristics identical to those of the industry standard MC1741, and can be applied with no change in circuit performance. In addition, the total supply current for all four amplifiers is comparable to the supply current of a single MC1741. Other features include input offset currents and input bias currents which are much less than the MC1741 industry standard.

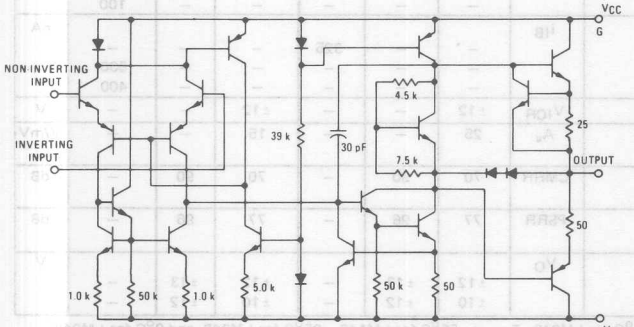
The LM148 can be used in applications where amplifier matching or high packing density is important. Other applications include high impedance buffer amplifiers and active filter amplifiers.

- Each Amplifier is Functionally Equivalent to the MC1741
- Low Input Offset and Input Bias Currents
- Class AB Output Stage Eliminates Crossover Distortion
- Pin Compatible with MC3503 and LM124
- True Differential Inputs
- Internally Frequency Compensated
- Short Circut Protection
- Low Power Supply Current (0.6 mA/Amplifier)

PIN CONNECTIONS



EQUIVALENT CIRCUIT SCHEMATIC
(1/4 of Circuit Shown)



ORDERING INFORMATION

Device	Temperature Range	Package
LM148J	−55 to +125°C	Ceramic DIP
LM248J	−25 to +85°C	Ceramic DIP
LM248N	−25 to +85°C	Plastic DIP
LM348D	0 to +70°C	SO-14
LM348J	0 to +70°C	Ceramic DIP
LM348N	0 to +70°C	Plastic DIP

2

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	LM148	LM248/LM348		Unit
Power Supply Voltage	V_{CC} V_{EE}	+22 −22	+18 −18		Vdc Vdc
Input Differential Voltage	V_{ID}	±44	±36		Volts
Input Common Mode Voltage	V_{ICM}	±22	±18		Volts
Output Short Circuit Duration	t_S	Continuous			
Operating Ambient Temperature Range	T_A	−55 to +125	−25 to +85	0 to +70	°C
Storage Temperature Range Ceramic Package Plastic Package	T_{stg}	−65 to +150 −55 to +125			°C
Junction Temperature Ceramic Package Plastic Package	T_J	175 150			°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	LM148			LM248/348			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (R_S ≤ 10 k)	V_{IO}	–	1.0	5.0	–	1.0	6.0	mV
Input Offset Current	I_{IO}	–	4.0	25	–	4.0	50	nA
Input Bias Current	I_{IB}	–	30	100	–	30	200	nA
Input Resistance	r_i	0.8	2.5	–	0.8	2.5	–	MΩ
Common Mode Input Voltage Range	V_{ICR}	±12	–	–	±12	–	–	V
Large Signal Voltage Gain (R_L ≥ 2.0 k, V_O = ±10 V)	A_v	50	160	–	25	160	–	V/mV
Channel Separation (f = 1.0 Hz to 20 kHz)	–	–	-120	–	–	-120	–	dB
Common Mode Rejection Ratio (R_S ≤ 10 k)	CMRR	70	90	–	70	90	–	dB
Supply Voltage Rejection Ratio (R_S ≤ 10 k)	PSRR	77	96	–	77	96	–	dB
Output Voltage Swing (R_L ≥ 10 k) (R_L ≥ 2 k)	V_O	 ±12 ±10	 ±13 ±12	 – –	 ±12 ±10	 ±13 ±12	 – –	V
Output Short-Circuit Current	I_{os}	–	25	–	–	25	–	mA
Supply Current – (All Amplifiers)	I_D	–	2.4	3.6	–	2.4	4.5	mA
Small Signal Bandwidth (A_v = 1)	BW	–	1.0	–	–	1.0	–	MHz
Phase Margin (A_v = 1)	ϕm	–	60	–	–	60	–	degrees
Slew Rate (A_v = 1)	SR	–	0.5	–	–	0.5	–	V/μs

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = *T_{high} to T_{low} unless otherwise noted)

Input Offset Voltage (R_S ≤ 10 kΩ)	V_{IO}	–	–	6.0	–	–	7.5	mV
Input Offset Current LM148 LM248 LM348	I_{IO}	 – – –	 – – –	 75 – –	 – – –	 – – –	 – 125 100	nA
Input Bias Current LM148 LM248 LM348	I_{IB}	 – – –	 – – –	 325 – –	 – – –	 – – –	 – 500 400	nA
Common Mode Input Voltage Range	V_{ICR}	±12	–	–	±12	–	–	V
Large Signal Voltage Gain (R_L ≥ 2 k, V_O = ±10 V)	A_v	25	–	–	15	–	–	V/mV
Common Mode Rejection Ratio (R_S ≤ 10 k)	CMRR	70	90	–	70	90	–	dB
Supply Voltage Rejection Ratio (R_S ≤ 10 k)	PSRR	77	96	–	77	96	–	dB
Output Voltage Swing (R_L ≥ 10 k) (R_L ≥ 2 k)	V_O	 ±12 ±10	 ±13 ±12	 – –	 ±12 ±10	 ±13 ±12	 – –	V

*T_{high} = 125°C for LM148, 85°C for LM248, and 70°C for LM348. T_{low} = −55°C for LM148, -25°C for LM248, and 0°C for LM348.

NOTE: Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted or the maximum junction temperature will be exceeded.

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted).

FIGURE 1 – POWER BANDWIDTH
(LARGE SIGNAL SWING versus FREQUENCY)

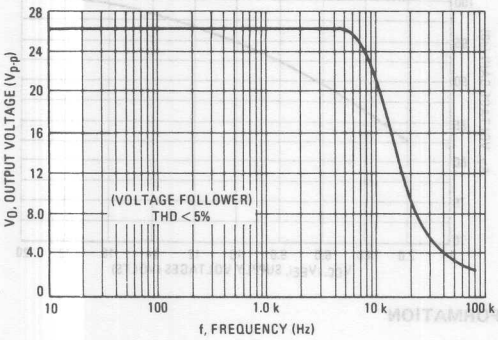


FIGURE 2 – OPEN LOOP FREQUENCY RESPONSE

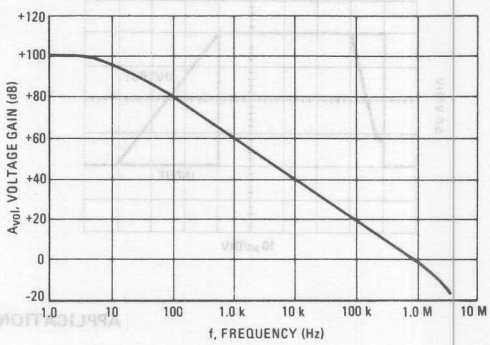


FIGURE 3 – POSITIVE OUTPUT VOLTAGE SWING
versus LOAD RESISTANCE

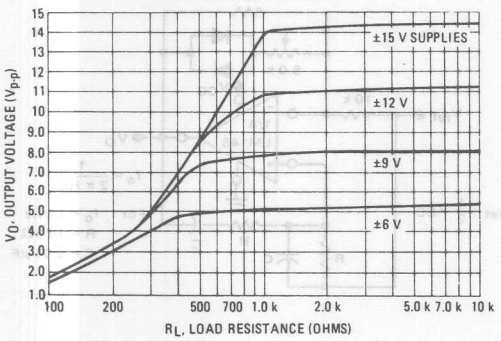


FIGURE 4 – NEGATIVE OUTPUT VOLTAGE SWING
versus LOAD RESISTANCE

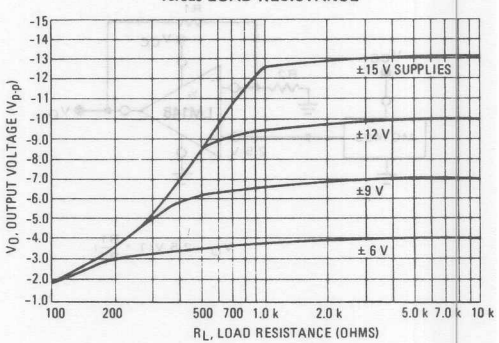


FIGURE 5 – OUTPUT VOLTAGE SWING versus
LOAD RESISTANCE (Single Supply Operation)

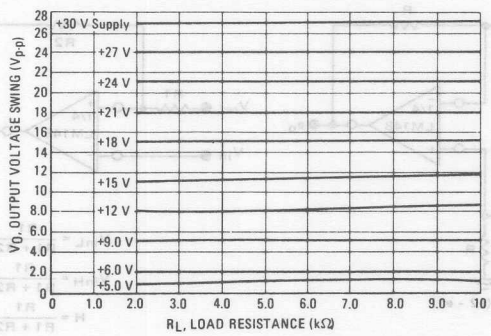


FIGURE 6 — NONINVERTING PULSE RESPONSE

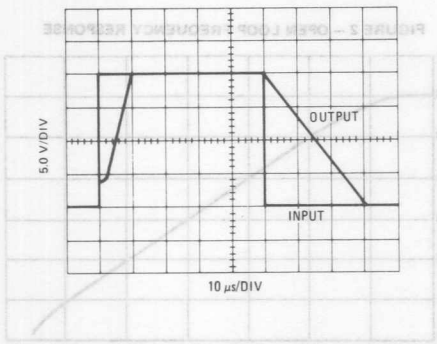
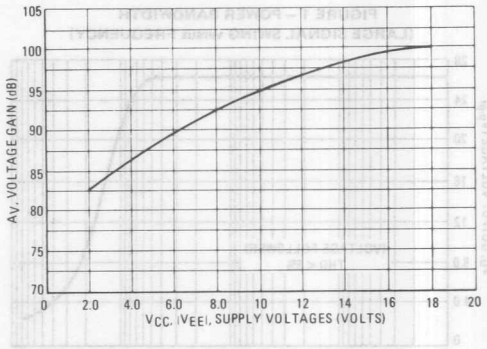


FIGURE 7 — OPEN LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE



APPLICATIONS INFORMATION

FIGURE 8 — VOLTAGE REFERENCE

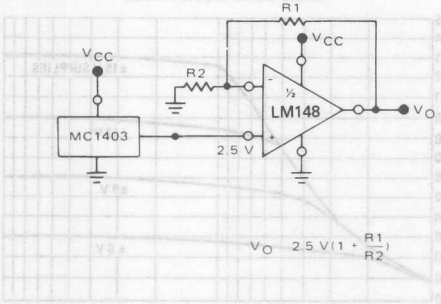


FIGURE 9 — WIEN BRIDGE OSCILLATOR

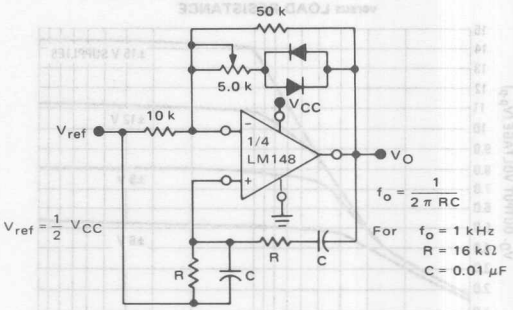


FIGURE 10 — HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER

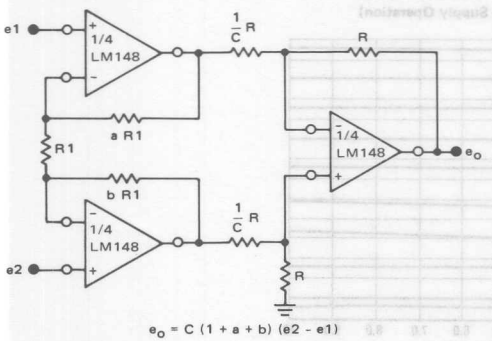


FIGURE 11 — COMPARATOR WITH HYSTERESIS

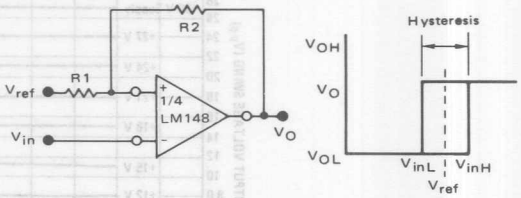


FIGURE 12 – HIGH IMPEDANCE INSTRUMENTATION BUFFER/FILTER

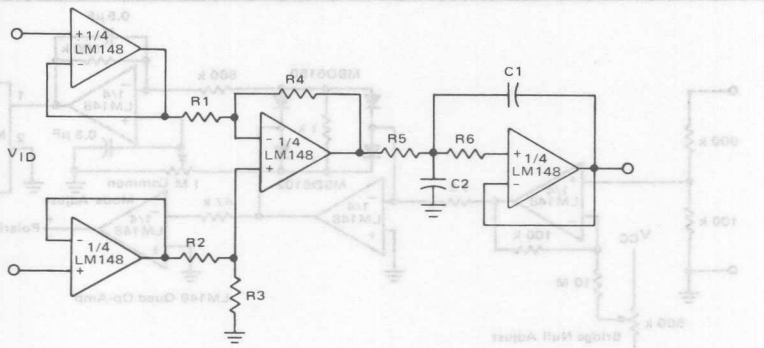
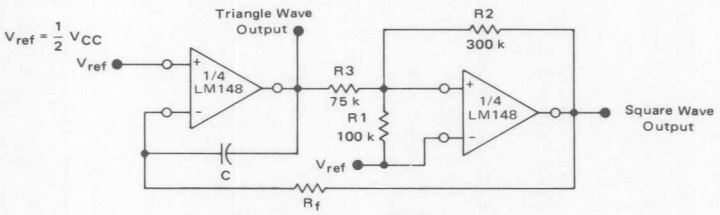
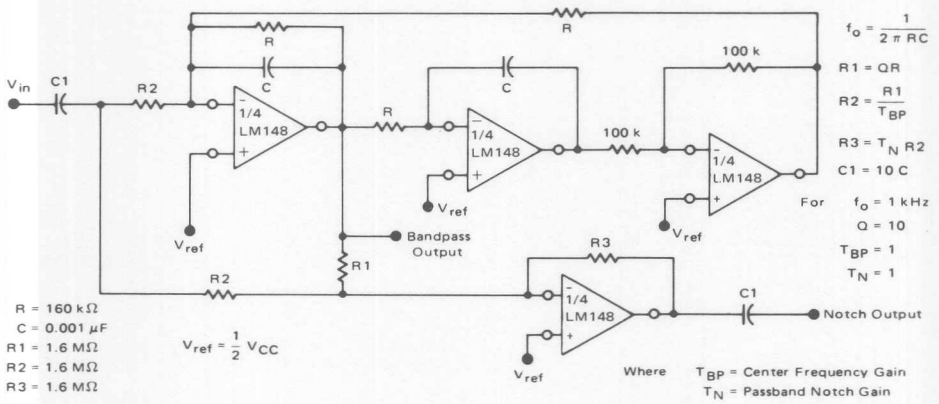


FIGURE 13 – FUNCTION GENERATOR



$$f = \frac{R1 + RC}{4CR_f R1} \quad \text{if} \quad R3 = \frac{R2\,R1}{R2 + R1}$$

FIGURE 14 – BI-QUAD FILTER



$$f_o = \frac{1}{2\pi RC}$$

$$R1 = QR$$

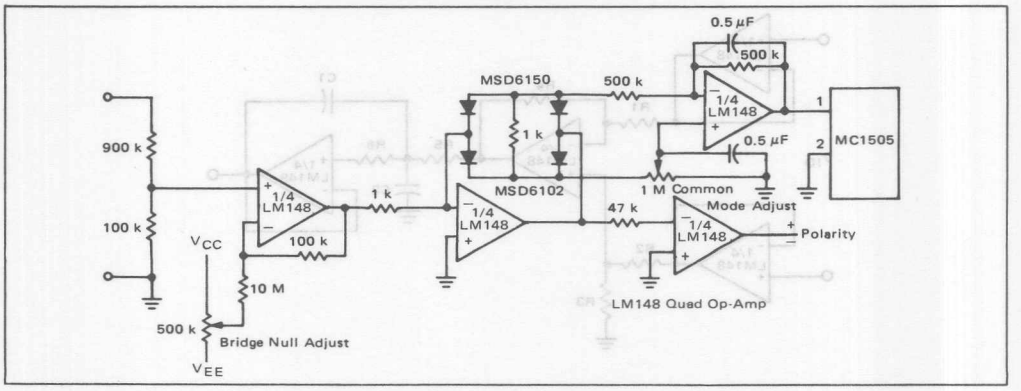
$$R2 = \frac{R1}{T_{BP}}$$

$$R3 = T_N\,R2$$

$$C1 = 10\,C$$

2

FIGURE 15 – ABSOLUTE VALUE DVM FRONT END



MOTOROLA

LM158, LM258, LM358, LM2904

Specifications and Applications Information

DUAL LOW POWER OPERATIONAL AMPLIFIERS

Utilizing the circuit designs perfected for recently introduced Quad Operational Amplifiers, these dual operational amplifiers feature 1) low power drain, 2) a common mode input voltage range extending to ground/V_{EE}, 3) Single Supply or Split Supply operation and 4) pin outs compatible with the popular MC1558 dual operational amplifier. The LM158 Series is equivalent to one-half of an LM124.

These amplifiers have several distinct advantages over standard operational amplifier types in single supply applications. They can operate at supply voltages as low as 3.0 Volts or as high as 32 Volts with quiescent currents about one-fifth of those associated with the MC1741 (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

- Short Circuit Protected Outputs
- True Differential Input Stage
- Single Supply Operation: 3.0 to 32 Volts
- Low Input Bias Currents
- Internally Compensated
- Common Mode Range Extends to Negative Supply
- Single and Split Supply Operation
- Similar Performance to the Popular MC1558

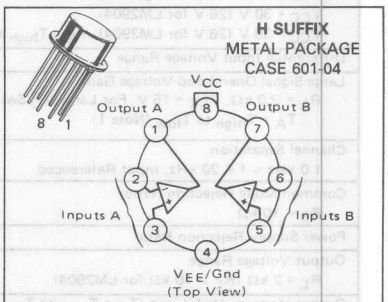
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

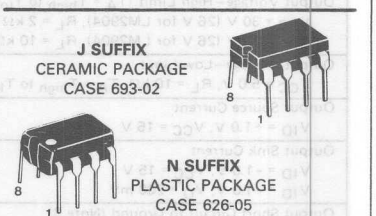
Rating	Symbol	LM158 LM258 LM358	LM2904	Unit
Power Supply Voltages				Vdc
Single Supply	V_{CC}	32	26	
Split Supplies	V_{CC}, V_{EE}	±16	±13	
Input Differential Voltage Range (1)	V_{IDR}	±32	±26	Vdc
Input Common Mode Voltage Range (2)	V_{ICR}	-0.3 to 32	-0.3 to 26	Vdc
Input Forward Current (3) ($V_I \leq -0.3$ V)	I_{IF}	50	–	mA
Output Short Circuit Duration	t_S	Continuous		
Junction Temperature	T_J			°C
Ceramic and Metal Packages		175		
Plastic Package		150		
Storage Temperature Range	T_{stg}			°C
Ceramic and Metal Packages		−65 to +150		
Plastic Package		−55 to +125		
Operating Ambient Temperature Range	T_A			°C
LM158		−55 to +125	–	
LM258		−25 to +85	–	
LM358		0 to +70	–	
LM2904		–	−40 to +85	

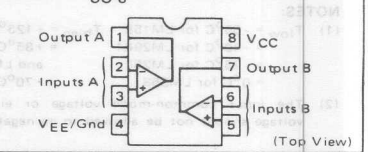
(1) Split Power Supplies.
(2) For Supply Voltages less than 32 V for the LM158/258/358 and 26 V for the LM2904, the absolute maximum input voltage is equal to the supply voltage.
(3) This input current will only exist when the voltage is negative at any of the input leads. Normal output states will reestablish when the input voltage returns to a voltage greater than −0.3 V.

DUAL DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUIT







ORDERING INFORMATION

Device	Temperature Range	Package
LM158H	−55 to +125°C	Metal Can
LM158J		Ceramic DIP
LM2904D	−40 to +85°C	SO-8
LM2904H		Metal Can
LM2904J		Ceramic DIP
LM2904N		Plastic DIP
LM258D	−25 to +85°C	SO-8
LM258H		Metal Can
LM258J		Ceramic DIP
LM258N		Plastic DIP
LM358D	0 to +70°C	SO-8
LM358H		Metal Can
LM358J		Ceramic DIP
LM358N		Plastic DIP

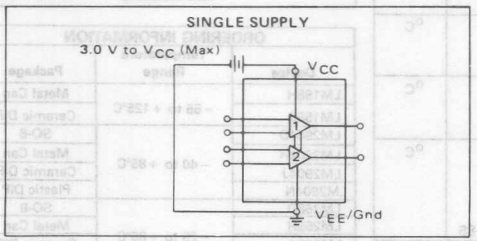
Characteristic	Symbol	LM158/LM258 Min	LM158/LM258 Typ	LM158/LM258 Max	LM358 Min	LM358 Typ	LM358 Max	LM2904 Min	LM2904 Typ	LM2904 Max	Unit
Input Offset Voltage V_{CC} = 5.0 V to 30 V (26 V for LM2904), V_{IC} = 0 V to V_{CC} – 1.7 V, $V_O \simeq$ 1.4 V, R_S = 0 Ω	V_{IO}										mV
$T_A = 25^oC$		–	2.0	5.0	–	2.0	7.0	–	2.0	7.0	
$T_A = T_{high}$ to T_{low} (Note 1)		–	–	7.0	–	–	9.0	–	–	10	
Average Temperature Coefficient of Input Offset Voltage $T_A = T_{high}$ to T_{low} (Note 1)	$\Delta V_{IO}/\Delta T$	–	7.0	–	–	7.0	–	–	7.0	–	μV/°C
Input Offset Current	I_{IO}	–	3.0	30	–	5.0	50	–	5.0	50	nA
$T_A = T_{high}$ to T_{low} (Note 1)		–	–	100	–	–	150	–	45	200	
Average Temperature Coefficient of Input Offset Current $T_A = T_{high}$ to T_{low} (Note 1)	$\Delta I_{IO}/\Delta T$	–	10	–	–	10	–	–	10	–	pA/°C
Input Bias Current	I_{IB}	–	-45	-150	–	-45	-250	–	-45	-250	nA
$T_A = T_{high}$ to T_{low} (Note 1)		–	-50	-300	–	-50	-500	–	-50	-500	
Input Common-Mode Voltage Range (Note 2)	V_{ICR}										V
V_{CC} = 30 V (26 V for LM2904)		0	–	28.3	0	–	28.3	0	–	24.3	
V_{CC} = 30 V (26 V for LM2904), $T_A = T_{high}$ to T_{low}		0	–	28	0	–	28	0	–	24	
Differential Input Voltage Range	V_{IDR}	–	–	V_{CC}	–	–	V_{CC}	–	–	V_{CC}	V
Large Signal Open-Loop Voltage Gain	A_{VOL}										V/mV
R_L = 2.0 kΩ, V_{CC} = 15 V, For Large V_O Swing		50	100	–	25	100	–	–	100	–	
$T_A = T_{high}$ to T_{low} (Note 1)		25	–	–	15	–	–	–	–	–	
Channel Separation 1.0 kHz ≤ f ≤ 20 kHz, Input Referenced	–	–	-120	–	–	-120	–	–	-120	–	dB
Common-Mode Rejection Ratio $R_S \leq$ 10 kΩ	CMRR	70	85	–	65	70	–	50	70	–	dB
Power Supply Rejection Ratio	PSRR	65	100	–	65	100	–	50	100	–	dB
Output Voltage Range R_L = 2 kΩ (R_L > 10 kΩ for LM2904)	V_{OR}	0	–	3.3	0	–	3.3	0	–	3.3	V
Output Voltage–High Limit ($T_A = T_{high}$ to T_{low})(Note 1)	V_{OH}										V
V_{CC} = 30 V (26 V for LM2904), R_L = 2 kΩ		26	–	–	26	–	–	22	–	–	
V_{CC} = 30 V (26 V for LM2904), R_L = 10 kΩ		27	28	–	27	28	–	23	24	–	
Output Voltage–Low Limit V_{CC} = 5.0 V, R_L = 10 kΩ, $T_A = T_{high}$ to T_{low} (Note 1)	V_{OL}	–	5.0	20	–	5.0	20	–	5.0	20	mV
Output Source Current V_{ID} = +1.0 V, V_{CC} = 15 V	I_{O+}	20	40	–	20	40	–	20	40	–	mA
Output Sink Current	I_{O-}										
V_{ID} = -1.0 V, V_{CC} = 15 V		10	20	–	10	20	–	10	20	–	mA
V_{ID} = -1.0 V, V_O = 200 mV		12	50	–	12	50	–	–	–	–	μA
Output Short Circuit to Ground (Note 3)	I_{os}	–	40	60	–	40	60	–	40	60	mA
Power Supply Current ($T_A = T_{high}$ to T_{low})(Note 1)	I_{CC}										mA
V_{CC} = 30 V (26 V for LM2904), V_O = 0 V, $R_L = \infty$		–	1.5	3.0	–	1.5	3.0	–	1.5	3.0	
V_{CC} = 5 V, V_O = 0 V, $R_L = \infty$		–	0.7	1.2	–	0.7	1.2	–	0.7	1.2	

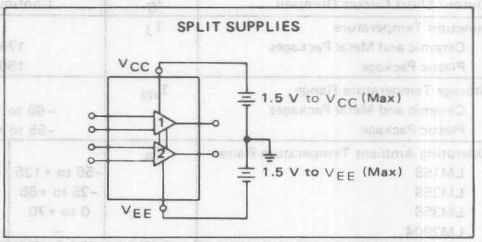
NOTES:

(1) T_{low} = -55°C for LM158, -40°C for LM2904, -25°C for LM258, 0°C for LM358; T_{high} = +125°C for LM158, +85°C for LM2904 and LM258, +70°C for LM358

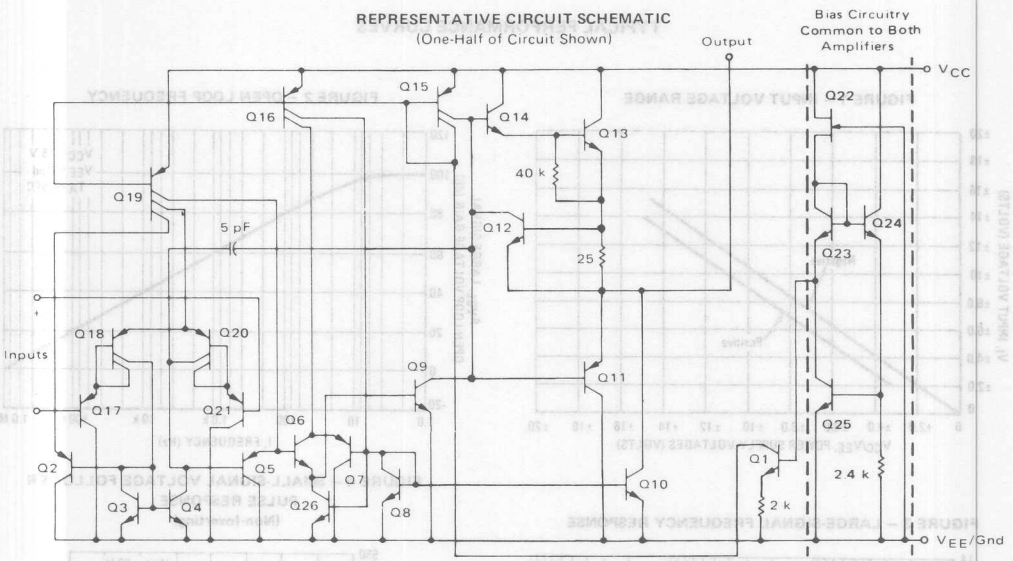
(2) The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V_{CC} - 1.7 V, but either or both inputs can go to +32 V without damage (+26 V for LM2904).

(3) Short circuits from the output to V_{CC} can cause excessive heating and eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

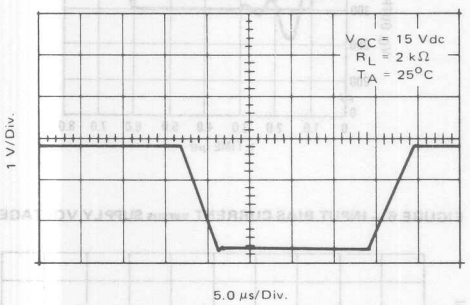




REPRESENTATIVE CIRCUIT SCHEMATIC
(One-Half of Circuit Shown)



LARGE SIGNAL VOLTAGE
FOLLOWER RESPONSE



CIRCUIT DESCRIPTION

The LM158 Series is made using two internally compensated, two-stage operational amplifiers. The first stage of each consists of differential input devices Q20 and Q18 with input buffer transistors Q21 and Q17 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance a smaller compensation capacitor (only 5 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q20 and Q18. Another feature of this input stage is that the input common-mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single-ended converter. The second stage consists of a standard current source load amplifier stage.

Each amplifier is biased from an internal-voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

2

TYPICAL PERFORMANCE CURVES

FIGURE 1 – INPUT VOLTAGE RANGE

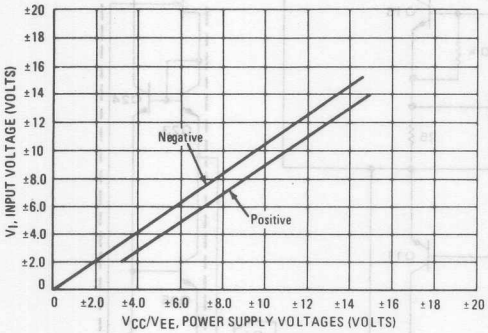


FIGURE 2 – OPEN LOOP FREQUENCY

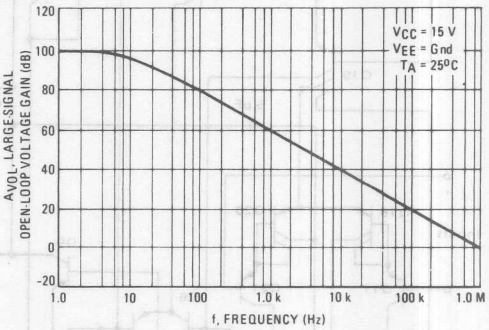


FIGURE 3 – LARGE-SIGNAL FREQUENCY RESPONSE

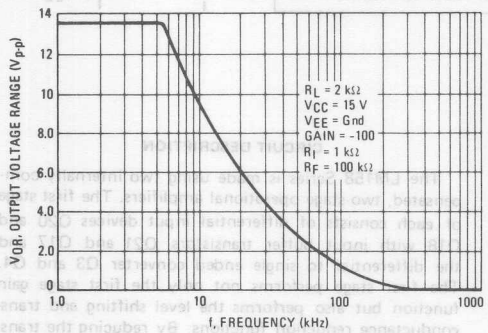


FIGURE 4 – SMALL-SIGNAL VOLTAGE FOLLOWER PULSE RESPONSE (Non-Inverting)

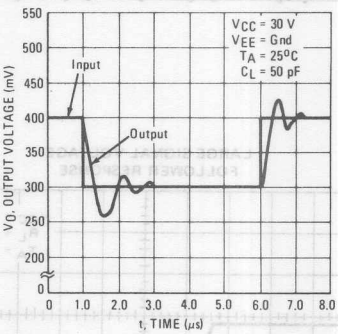


FIGURE 5 – POWER SUPPLY CURRENT versus POWER SUPPLY VOLTAGE

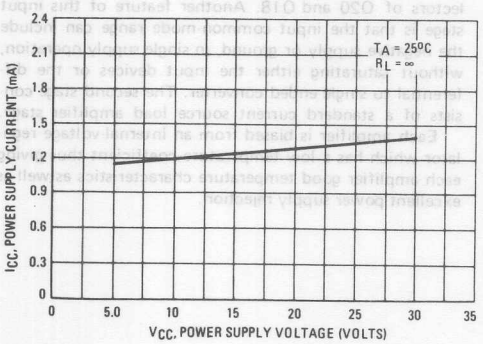
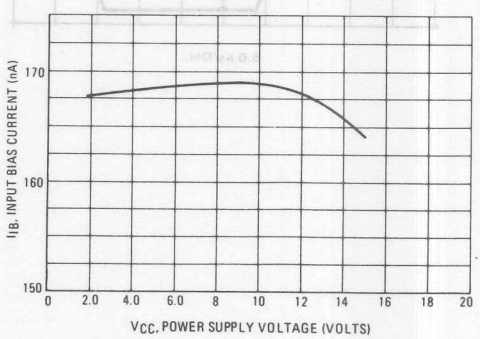


FIGURE 6 – INPUT BIAS CURRENT versus SUPPLY VOLTAGE



APPLICATIONS INFORMATION

FIGURE 7 – VOLTAGE REFERENCE

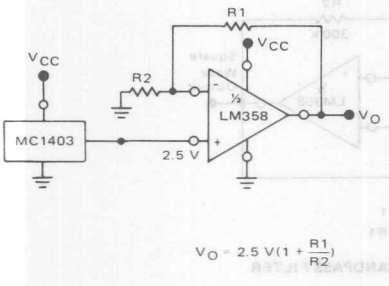


FIGURE 8 – WIEN BRIDGE OSCILLATOR

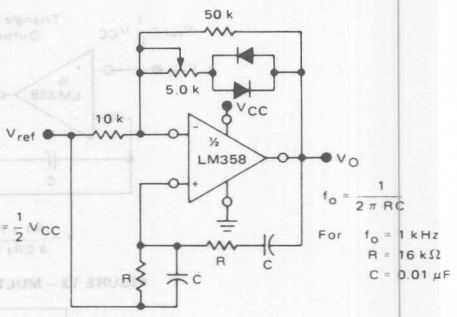


FIGURE 9 – HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER

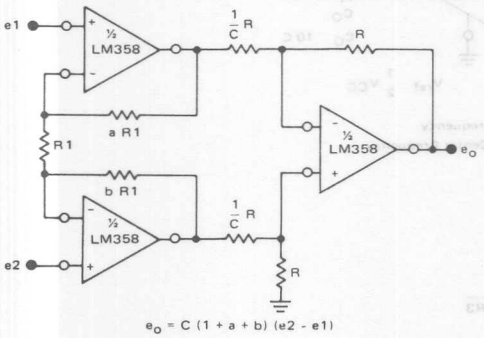


FIGURE 10 – COMPARATOR WITH HYSTERESIS

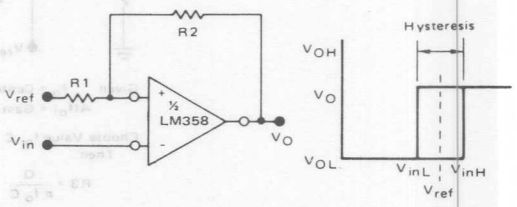


FIGURE 11 – BI-QUAD FILTER

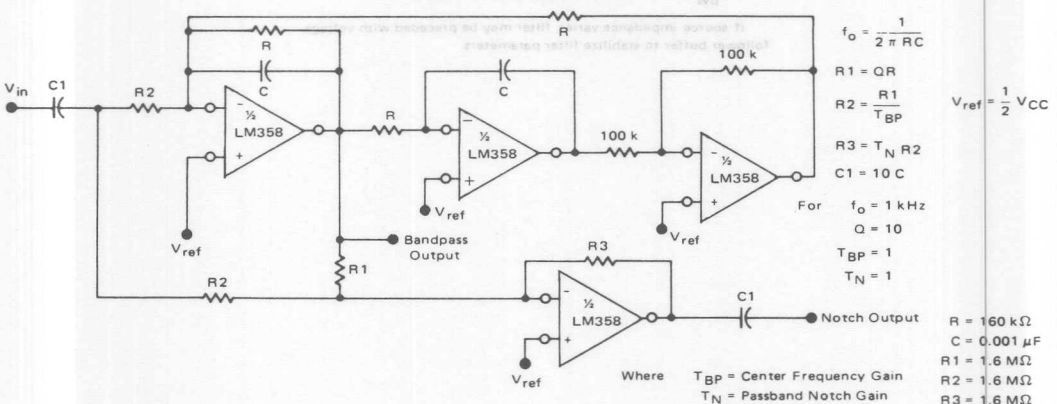
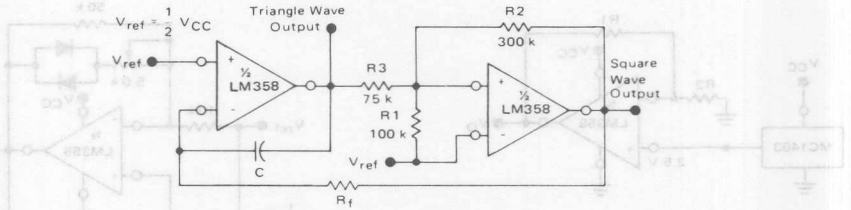
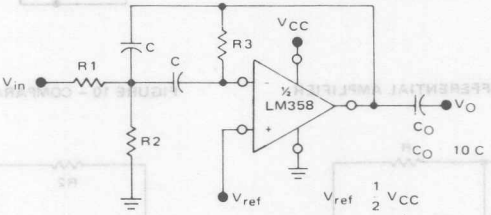


FIGURE 12 – FUNCTION GENERATOR



$$f = \frac{R1 + R_C}{4\,CR_f\,R1} \quad \text{if} \quad R3 = \frac{R2\,R1}{R2 + R1}$$

FIGURE 13 – MULTIPLE FEEDBACK BANDPASS FILTER



Given f_o = Center Frequency
$A(f_o)$ = Gain at Center Frequency

Choose Value f_o, C
Then

$$R3 = \frac{Q}{\pi\, f_o\, C}$$

$$R1 = \frac{R3}{2\,A(f_o)}$$

$$R2 = \frac{R1\,R3}{4Q^2\,R1 - R3}$$

For less than 10% error from operational amplifier

$$\frac{Q_o\, f_o}{BW} < 0.1$$ Where f_o and BW are expressed in Hz.

If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

MOTOROLA

LM193 LM193A
LM293 LM293A
LM393 LM393A
LM2903

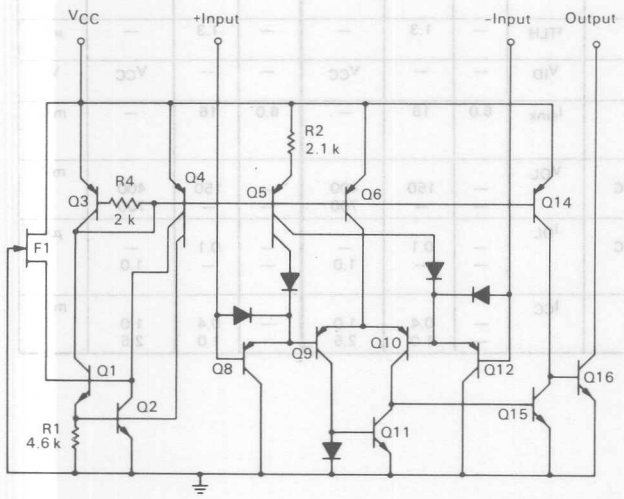
2

SINGLE SUPPLY, LOW POWER, LOW OFFSET VOLTAGE DUAL COMPARATORS

The LM193 series are dual independent precision voltage comparators capable of single-or split-supply operation. These devices are designed to permit a common mode range-to-ground level with single-supply operation. Input offset-voltage specifications as low as 2.0 mV make this device an excellent selection for many applications in consumer automotive, and industrial electronics.

- Wide Single-Supply Range — 2.0 Vdc to 36 Vdc
- Split-Supply Range — ±1.0 Vdc to ±18 Vdc
- Very Low Current Drain Independent of Supply Voltage — 0.4 mA
- Low Input Bias Current — 25 nA
- Low Input Offset Current — 5.0 nA
- Low Input Offset Voltage — 2.0 mV (max) LM193A/293A/393A
  — 5.0 mV (max) LM193/293/393
- Input Common Mode Range to Ground Level
- Differential Input Voltage Range Equal to Power Supply Voltage
- Output Voltage Compatible with DTL, ECL, TTL, MOS and CMOS Logic Levels

FIGURE 1 — CIRCUIT SCHEMATIC
(Diagram shown is for 1 comparator)

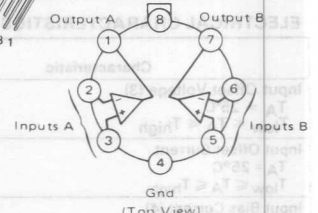


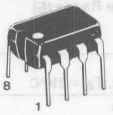
DUAL COMPARATORS

SILICON MONOLITHIC
INTEGRATED CIRCUIT



H SUFFIX
METAL PACKAGE
CASE 601-04

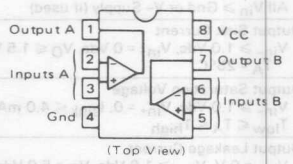




N SUFFIX
PLASTIC PACKAGE
CASE 626-05

D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SO-8





ORDERING INFORMATION

Device	Temperature Range	Package
LM193AH,H	−55 to +125°C	Metal Can
LM293AH,H	−25 to +85°C	Metal Can
LM293D		SO-8
LM393AH,H	0 to +70°C	Metal Can
LM393D		SO-8
LM393AN,N		Plastic DIP
LM2903D	−40 to +85°C	SO-8
LM2903N		Plastic DIP

2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+36 or ±18	Vdc
Input Differential Voltage Range	V_{IDR}	36	Vdc
Input Common Mode Voltage Range	V_{ICR}	-0.3 to +36	Vdc
Input Current (2) (V_{in} < −0.3 Vdc)	I_{in}	50	mA
Output Short Circuit-to-Ground Output Sink Current (1)	I_{SC} I_{sink}	Continuous 20	mA
Power Dissipation @ T_A = 25°C Plastic DIP Derate above 25°C Metal Can Derate above 25°C	 P_D $1/R_{\theta JA}$ P_D $1/R_{\theta JA}$	 570 5.7 830 6.64	 mW mW/°C mW mW/°C
Operating Ambient Temperature Range LM193, 193A LM293, 293A LM393, 393A LM2903	T_A	 -55 to +125 -25 to +85 0 to +70 -40 to +85	°C
Maximum Operating Junction Temperature LM393, 393A, 2903 LM193, 193A, 293, 293A	$T_{J(max)}$	 125 150	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc; *$T_{low} \leq T_A \leq T_{high}$ unless otherwise stated.)

Characteristic	Symbol	LM193A Min	LM193A Typ	LM193A Max	LM293A, LM393A Min	LM293A, LM393A Typ	LM293A, LM393A Max	Unit
Input Offset Voltage (3) T_A = 25°C $T_{low} \leq T_A \leq T_{high}$	V_{IO}	— —	±1.0 —	±2.0 4.0	— —	±1.0 —	±2.0 4.0	mV
Input Offset Current T_A = 25°C $T_{low} \leq T_A \leq T_{high}$	I_{IO}	— —	±3.0 —	±25 ±100	— —	±5.0 —	±50 ±150	nA
Input Bias Current (4) T_A = 25°C $T_{low} \leq T_A \leq T_{high}$	I_{IB}	— —	25 —	100 300	— —	25 —	250 400	nA
Input Common Mode Voltage Range (5) T_A = 25°C $T_{low} \leq T_A \leq T_{high}$	V_{ICR}	0 0	— —	V_{CC} -1.5 V_{CC} -2.0	0 0	— —	V_{CC} -1.5 V_{CC} -2.0	Volts
Voltage Gain $R_L \geq$ 15 kΩ, V_{CC} = 15 Vdc, T_A = 25°C	A_{VOL}	50	200	—	50	200	—	V/mV
Large Signal Response Time V_{in} = TTL Logic Swing, V_{ref} = 1.4 Vdc V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ, T_A = 25°C	—	—	300	—	—	300	—	ns
Response Time (5) V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ, T_A = 25°C	t_{TLH}	—	1.3	—	—	1.3	—	μs
Input Differential Voltage (7) All $V_{in} \geq$ Gnd or V- Supply (if used)	V_{ID}	—	—	V_{CC}	—	—	V_{CC}	V
Output Sink Current $V_{in-} \geq$ 1.0 Vdc, V_{in+} = 0 Vdc, $V_O \leq$ 1.5 Vdc T_A = 25°C	I_{sink}	6.0	16	—	6.0	16	—	mA
Output Saturation Voltage $V_{in-} \geq$ 1.0 Vdc, V_{in+} = 0, $I_{sink} \leq$ 4.0 mA, T_A = 25°C $T_{low} \leq T_A \leq T_{high}$	V_{OL}	— —	150 —	400 700	— —	150 —	400 700	mV
Output Leakage Current V_{in-} = 0 V, $V_{in+} \geq$ 1.0 Vdc, V_O = 5.0 Vdc, T_A = 25°C V_{in-} = 0 V, $V_{in+} \geq$ 1.0 Vdc, V_O = 30 Vdc, $T_{low} \leq T_A \leq T_{high}$	I_{OL}	— —	0.1 —	— 1.0	— —	0.1 —	— 1.0	μA
Supply Current R_L = ∞ Both Comparators, T_A = 25°C R_L = ∞ Both Comparators, V_{CC} = 30 V	I_{CC}	— —	0.4 1.0	1.0 2.5	— —	0.4 1.0	1.0 2.5	mA

*LM193/193A — T_{low} = -55°C, T_{high} = +125°C
LM293/293A — T_{low} = -25°C, T_{high} = +85°C
LM393/393A — T_{low} = 0°C, T_{high} = +70°C
LM2903 — T_{low} = -40°C, T_{high} = +85°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc; *$T_{low} \leq T_A \leq T_{high}$ unless otherwise stated.)

Characteristic	Symbol	LM193 Min	LM193 Typ	LM193 Max	LM293, LM393 Min	LM293, LM393 Typ	LM293, LM393 Max	LM2903 Min	LM2903 Typ	LM2903 Max	Unit
Input Offset Voltage (3)	V_{IO}										mV
T_A = 25°C		—	±1.0	±5.0	—	±1.0	±5.0	—	±2.0	±7.0	
$T_{low} \leq T_A \leq T_{high}$		—	—	9.0	—	—	9.0	—	9.0	15	
Input Offset Current	I_{IO}										nA
T_A = 25°C		—	±3.0	±25	—	±5.0	±50	—	±5.0	±50	
$T_{low} \leq T_A \leq T_{high}$		—	—	±100	—	—	±150	—	±50	±200	
Input Bias Current (4)	I_{IB}										nA
T_A = 25°C		—	25	100	—	25	250	—	25	250	
$T_{low} \leq T_A \leq T_{high}$		—	—	300	—	—	400	—	200	500	
Input Common Mode Voltage Range (4)	V_{ICR}										Volts
T_A = 25°C		0	—	V_{CC} -1.5	0	—	V_{CC} -1.5	0	—	V_{CC} -1.5	
$T_{low} \leq T_A \leq T_{high}$		0	—	V_{CC} -2.0	0	—	V_{CC} -2.0	0	—	V_{CC} -2.0	
Voltage Gain	A_{VOL}	50	200	—	50	200	—	25	200	—	V/mV
$R_L \geq$ 15 kΩ, V_{CC} = 15 Vdc, T_A = 25°C											
Large Signal Response Time	—	—	—	300	—	—	300	—	—	300	—	ns
V_{in} = TTL Logic Swing, V_{ref} = 1.4 Vdc											
V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ, T_A = 25°C											
Response Time (6)	t_{TLH}	—	1.3	—	—	1.3	—	—	1.5	—	μs
V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ, T_A = 25°C											
Input Differential Voltage (7)	V_{ID}	—	—	V_{CC}	—	—	V_{CC}	—	—	V_{CC}	V
All $V_{in} \geq$ Gnd or V- Supply (if used)											
Output Sink Current	I_{sink}	6.0	16	—	6.0	16	—	6.0	16	—	mA
$V_{in-} \geq$ 1.0 Vdc, V_{in+} = 0 Vdc, $V_O \leq$ 1.5 Vdc T_A = 25°C											
Output Saturation Voltage	V_{OL}										mV
$V_{in-} \geq$ 1.0 Vdc, V_{in+} = 0, $I_{sink} \leq$ 4.0 mA, T_A = 25°C		—	150	400	—	150	400	—	—	400	
$T_{low} \leq T_A \leq T_{high}$		—	—	700	—	—	700	—	200	700	
Output Leakage Current	I_{OL}										nA
V_{in-} = 0 V, $V_{in+} \geq$ 1.0 Vdc, V_O = 5.0 Vdc, T_A = 25°C		—	0.1	—	—	0.1	—	—	0.1	—	
V_{in-} = 0 V, $V_{in+} \geq$ 1.0 Vdc, V_O = 30 Vdc, $T_{low} \leq T_A \leq T_{high}$		—	—	1000	—	—	1000	—	—	1000	
Supply Current	I_{CC}										mA
$R_L = \infty$ Both Comparators, T_A = 25°C		—	0.4	1.0	—	0.4	1.0	—	0.4	1.0	
$R_L = \infty$ Both Comparators, V_{CC} = 30 V		—	—	2.5	—	—	2.5	—	—	2.5	

*LM193/193A — T_{low} = -55°C, T_{high} = +125°C
LM293/293A — T_{low} = -25°C, T_{high} = +85°C
LM393/393A — T_{low} = 0°C, T_{high} = +70°C

NOTES:

(1) The max. output current may be as high as 20 mA, independent of the magnitude of V_{CC}, output short circuits to V_{CC} can cause excessive heating and eventual destruction.

(2) This magnitude of input current will only occur if the input leads are driven more negative than ground or the negative supply voltage. This is due to the input PNP collector base junction becoming forward biased, acting as an input clamp diode. There is also a lateral PNP parasitic transistor action on the IC chip. This phenomena can cause the output voltage of the comparators to go to the V_{CC} voltage level (or ground if overdrive is large) during the time the input is driven negative. This will not destroy the device and normal output states will recover when the inputs become > −0.3 V of ground or negative supply.

(3) At output switch point, $V_O \approx$ 1.4 Vdc, R_S = 0 Ω with V_{CC} from 5.0 Vdc to 30 Vdc, and over the full input common-mode range (0 volts to V_{CC} = −1.5 volts)

(4) Due to the PNP transistor inputs, bias current will flow out of the inputs, this current is essentially constant independent of the output state, therefore, no loading changes will exist on the input lines.

(5) Input common mode of either input should not be permitted to go more than 0.3 V negative of ground or minus supply. The upper limit of common mode range is V_{CC} − 1.5 V but either or both inputs can be taken to as high as 30 volts without damage.

(6) Response time is specified with a 100 mV step and 5.0 mV of overdrive. With larger magnitudes of overdrive faster response times are obtainable.

(7) The comparator will exhibit proper output state if one of the inputs become greater than V_{CC}, the other input must remain within the common mode range. The low input state must not be less than −0.3 volts of ground of minus supply.

TYPICAL PERFORMANCE CHARACTERISTICS

LM193,A/293,A/393,A

FIGURE 2 — INPUT BIAS CURRENT versus POWER SUPPLY VOLTAGE

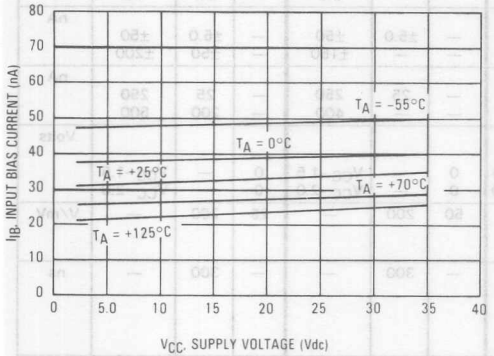


FIGURE 3 — OUTPUT SATURATION VOLTAGE versus OUTPUT SINK CURRENT

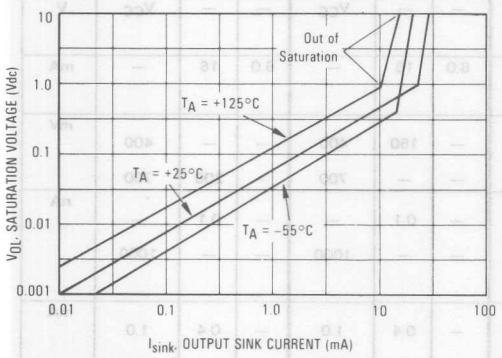
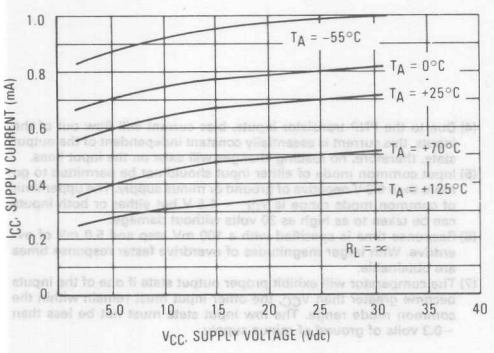


FIGURE 4 — POWER SUPPLY CURRENT versus POWER SUPPLY VOLTAGE



LM2903

FIGURE 5 — INPUT BIAS CURRENT versus POWER SUPPLY VOLTAGE

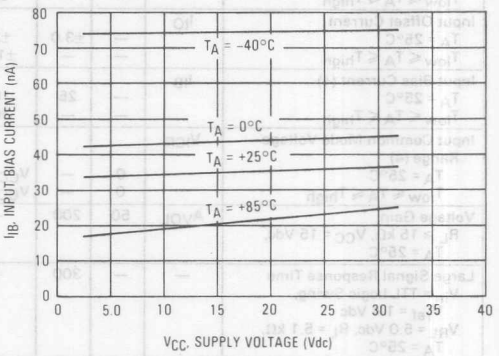


FIGURE 6 — OUTPUT SATURATION VOLTAGE versus OUTPUT SINK CURRENT

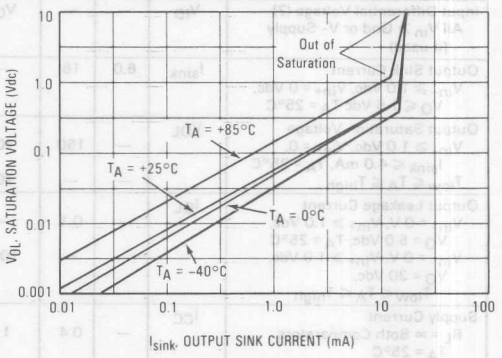
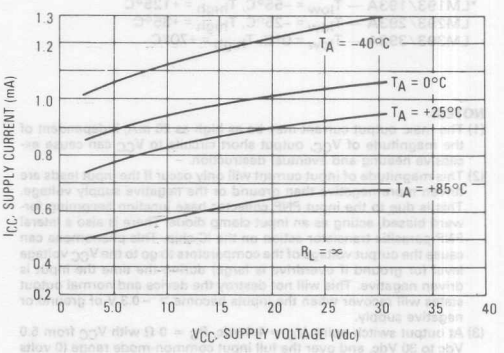


FIGURE 7 — POWER SUPPLY CURRENT versus POWER SUPPLY VOLTAGE



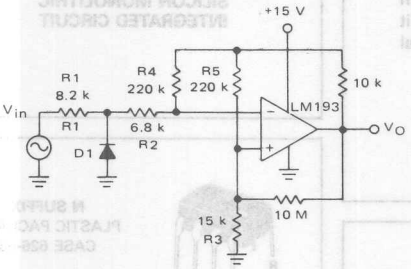
APPLICATIONS INFORMATION

These dual comparators feature high gain, wide bandwidth characteristics. This gives the device oscillation tendencies if the outputs are capacitively coupled to the inputs via stray capacitance. This oscillation manifests itself during output transitions (V_{OL} to V_{OH}). To alleviate this situation input resistors < 10 kΩ should be used. The addition of positive feedback (< 10 mV) is also recommended.

It is good design practice to ground all unused pins.

Differential input voltages may be larger than supply voltage without damaging the comparator's inputs. Voltages more negative than −0.3 V should not be used.

FIGURE 8 – ZERO CROSSING DETECTOR
(Single Supply)



D1 prevents input from going negative by more than 0.6 V.

$$R1 + R2 = R3$$

$$R3 \leq \frac{R5}{10} \text{ for small error in zero crossing}$$

FIGURE 9 – ZERO CROSSING DETECTOR
(Split Supplies)

V_{INmin} ≈0.4 V peak for 1% phase distortion (Θ).

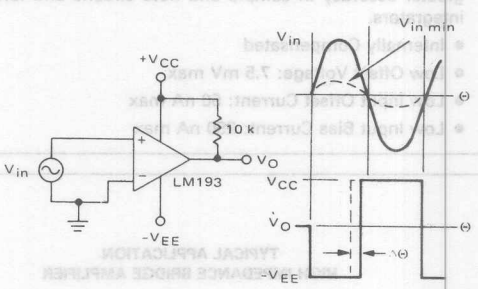


FIGURE 10 – FREE-RUNNING SQUARE-WAVE OSCILLATOR

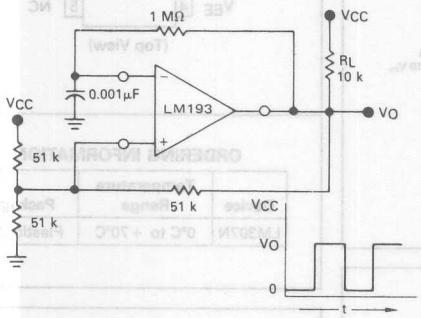
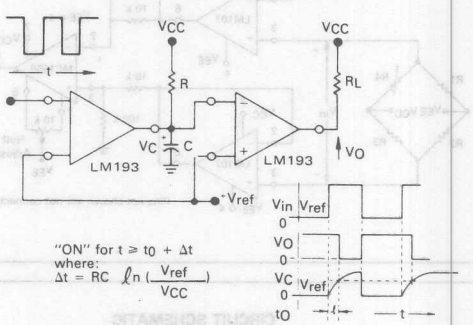
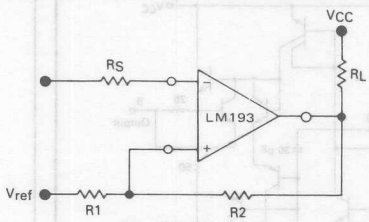


FIGURE 11 – TIME DELAY GENERATOR



"ON" for $t \geq t_0 + \Delta t$
where:
$\Delta t = RC \ln \left(\frac{V_{ref}}{V_{CC}}\right)$

FIGURE 12 – COMPARATOR WITH HYSTERESIS



$$R_S = R1 \parallel R2$$

$$V_{th1} = V_{ref} + \frac{(V_{CC} - V_{ref})\,R1}{R1 + R2 + R_L}$$

$$V_{th2} = V_{ref} - \frac{(V_{ref} - V_{O\,Low})\,R1}{R1 + R2 + R_L}$$

MOTOROLA

LM307

INTERNALLY COMPENSATED MONOLITHIC OPERATIONAL AMPLIFIER

A general purpose operational amplifier series well suited for applications requiring lower input currents than are available with the popular MC1741. These improved input characteristics permit greater accuracy in sample and hold circuits and long interval integrators.

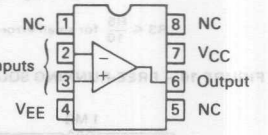
- Internally Compensated
- Low Offset Voltage: 7.5 mV max
- Low Input Offset Current: 50 nA max
- Low Input Bias Current: 250 nA max

OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

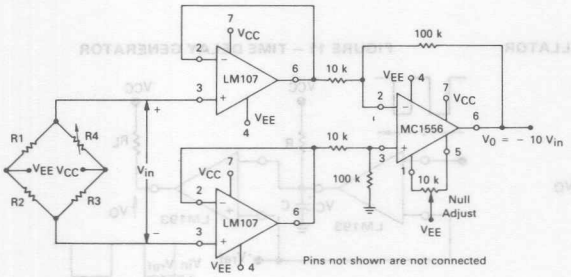


N SUFFIX
PLASTIC PACKAGE
CASE 626-05



(Top View)

TYPICAL APPLICATION
HIGH IMPEDANCE BRIDGE AMPLIFIER

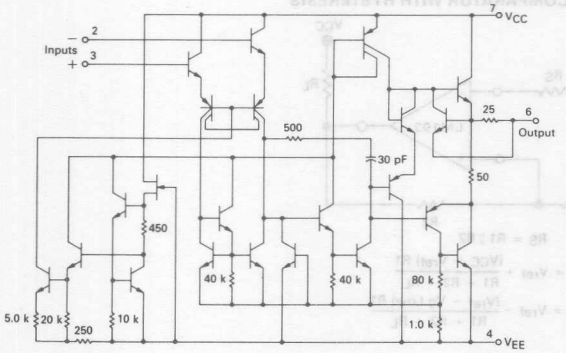


Pins not shown are not connected

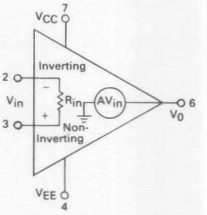
ORDERING INFORMATION

Device	Temperature Range	Package
LM307N	0°C to +70°C	Plastic DIP

CIRCUIT SCHEMATIC



EQUIVALENT CIRCUIT



Pins 1, 5, and 8
no connection.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	LM307	Unit
Power Supply Voltages	V_{CC} V_{EE}	+18 −18	Vdc
Differential Input Signal Voltage	V_{ID}	±30	Volts
Common-Mode Input Swing (Note 1)	V_{ICR}	±15	Volts
Output Short-Circuit Duration	t_s	Indefinite	
Power Dissipation (Package Limitation) (Note 2)	P_D	500	mW
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted, see Note 3.)

Characteristics	Symbol	LM307 Min	LM307 Typ	LM307 Max	Unit
Input Offset Voltage $R_S \leq 50\ k\Omega$, T_A = + 25°C $R_S \leq 50\ k\Omega$, $T_A = T_{low}$ to T_{high}	V_{IO}	 — —	 2.0 —	 7.5 10	mV
Input Offset Current T_A = +25°C $T_A = T_{low}$ to T_{high}	I_{IO}	 — —	 3.0 —	 50 70	nA
Input Bias Current T_A = +25°C $T_A = T_{low}$ to T_{high}	I_{IB}	 — —	 70 —	 250 300	nA
Input Resistance	r_i	0.5	2.0	—	MΩ
Supply Current V_S = ±15 V, T_A = +25°C	I_D	—	1.8	3.0	mA
Large-Signal Voltage Gain V_S = ±15 V, V_O = ±10 V, $R_L > 2.0\ k\Omega$, T_A = +25°C V_S = ±15 V, V_O = ±10 V, $R_L \geq 2.0\ k\Omega$, $T_A = T_{low}$	A_V	 25 15	 160 —	 — —	V/mV
Average Temperature Coefficient of Input Offset Voltage $T_{low} \leq T_A \leq T_{high}$	TCV_{IO}	—	6.0	30	µV/°C
Average Temperature Coefficient of Input Offset Current +25°C ≤ $T_A \leq T_{high}$ $T_{low} \leq T_A \leq$ +25°C	TCI_{IO}	 — —	 0.01 0.02	 0.3 0.6	nA/°C
Output Voltage Swing ($T_A = T_{low}$ to T_{high}) V_S = ±15 V, R_L = 10 kΩ R_L = 2.0 kΩ	V_O	 ±12 ±10	 +14 ±13	 — —	V
Input Voltage Range ($T_A = T_{low}$ to T_{high}) V_S = ±15 V	V_{ICR}	±12	—	—	V
Common-Mode Rejection Ratio ($T_A = T_{low}$ to T_{high}) $R_S \leq 50\ k\Omega$	CMRR	70	90	—	dB
Supply-Voltage Rejection Ratio ($T_A = T_{low}$ to T_{high}) $R_S \leq 50\ k\Omega$	PSRR	70	96	—	dB

Symbols conform to JEDEC Engineering Bulletin No. 1 when applicable.

Note 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

Note 2. For operating at elevated temperatures, the device must be derated based on a maximum junction temperature of 100°C for the LM307. The H package is derated based on a thermal resistance of +150°C/W, junction to ambient, or +45°C/W, junction to case.

Note 3. Unless otherwise noted, these specifications apply for: ±5.0 V ≤ $V_{CC}/V_{EE} \leq$ ±15 V, T_{low} = 0°C, T_{high} = +70°C

TYPICAL CHARACTERISTICS

(V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25°C unless otherwise noted.)

FIGURE 1 — MINIMUM INPUT VOLTAGE RANGE

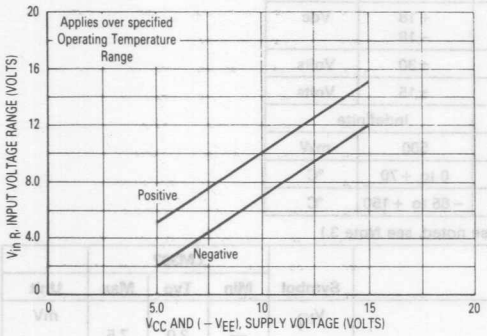


FIGURE 2 — MINIMUM OUTPUT VOLTAGE SWING

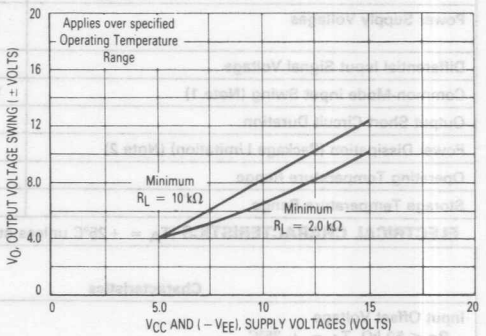


FIGURE 3 — MINIMUM VOLTAGE GAIN

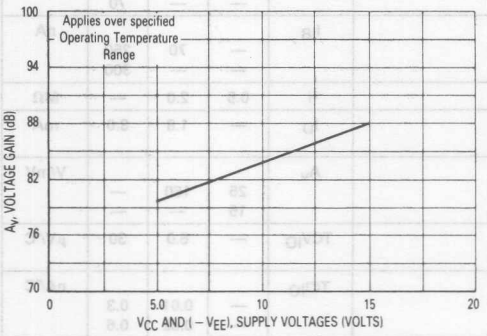


FIGURE 4 — TYPICAL SUPPLY CURRENTS

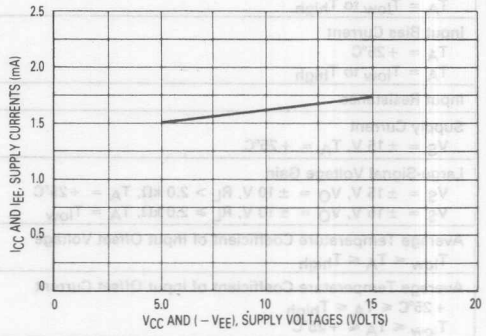


FIGURE 5 — OPEN-LOOP FREQUENCY RESPONSE

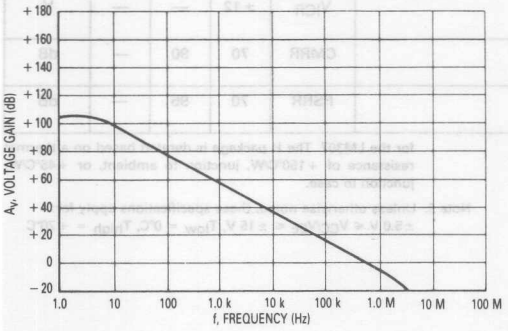
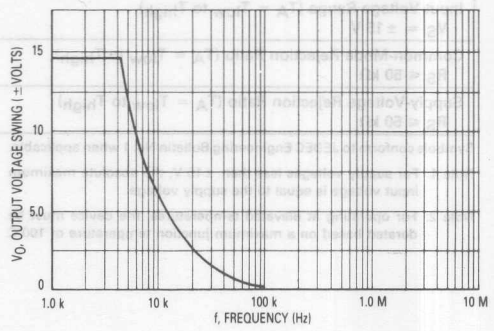
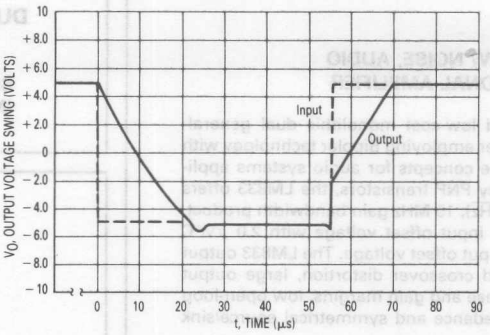


FIGURE 6 — LARGE-SIGNAL FREQUENCY RESPONSE



TYPICAL CHARACTERISTICS (continued)

FIGURE 7 — VOLTAGE FOLLOWER PULSE RESPONSE



MOTOROLA

LM833

DUAL, LOW NOISE, AUDIO OPERATIONAL AMPLIFIER

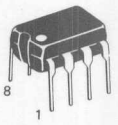
The LM833 is a standard low-cost monolithic dual general-purpose operational amplifier employing Bipolar technology with innovative high-performance concepts for audio systems applications. With high frequency PNP transistors, the LM833 offers low voltage noise (4.5 nV/$\sqrt{Hz}$), 15 MHz gain bandwidth product, 7.0 V/μs slew rate, 0.3 mV input offset voltage with 2.0 μV/°C temperature coefficient of input offset voltage. The LM833 output stage exhibits no deadband crossover distortion, large output voltage swing, excellent phase and gain margins, low open-loop high frequency output impedance and symmetrical source/sink ac frequency response.

The LM833 is specified over the vehicular temperature range and is available in the plastic DIP and SO-8 packages (P and D suffixes). A quad device is available in the MC34079 family.

- Low Voltage Noise: 4.5 nV/$\sqrt{Hz}$
- High Gain Bandwidth Product: 15 MHz
- High Slew Rate: 7.0 V/μs
- Low Input Offset Voltage: 0.3 mV
- Low T.C. of Input Offset Voltage: 2.0 μV/°C
- Low Distortion: 0.002%
- Excellent Frequency Stability
- Dual Supply Operation

DUAL OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

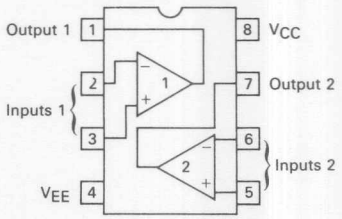


P SUFFIX
PLASTIC PACKAGE
CASE 626-05



D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SO-8

PIN ASSIGNMENTS



Dual, Top View

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	+36	Volts
Input Differential Voltage Range	V_{IDR}	30 NOTE 1	Volts
Input Voltage Range	V_{IR}	±15 NOTE 1	Volts
Output Short-Circuit Duration (NOTE 2)	tS	Indefinite	Seconds
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Operating Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	−60 to +150	°C
Maximum Power Dissipation (NOTE 2)	P_D	500 NOTE 3	mW

NOTES:
1. Either or both input voltages must not exceed the magnitude of V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (See power dissipation performance characteristic).
3. Maximum value at $T_A \leq 85°C$.

ORDERING INFORMATION

Device	Temperature Range	Package
LM833P	−40 to +85°C	Plastic DIP
LM833D	−40 to +85°C	SO-8

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C unless otherwise noted).

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 10 Ω, V_O = 0 V)	V_{IO}	—	0.3	5.0	mV
Average Temperature Coefficient of Input Offset Voltage R_S = 10 Ω, V_O = 0 V, T_A = T_{low} to T_{high}	$\Delta V_{IO}/\Delta T$	—	2.0	—	μV/°C
Input Offset Current (V_{CM} = 0 V, V_O = 0 V)	I_{IO}	—	10	200	nA
Input Bias Current (V_{CM} = 0 V, V_O = 0 V)	I_{IB}	—	300	1000	nA
Common Mode Input Voltage Range	V_{ICR}	— −12	+14 −14	+12 —	V
Large Signal Voltage Gain (R_L = 2.0 kΩ, V_O = ±10 V)	A_{VOL}	90	110	—	dB
Output Voltage Swing: R_L = 2.0 kΩ, V_{ID} = 1.0 V R_L = 2.0 kΩ, V_{ID} = 1.0 V R_L = 10 kΩ, V_{ID} = 1.0 V R_L = 10 kΩ, V_{ID} = 1.0 V	V_{O+} V_{O-} V_{O+} V_{O-}	10 — 12 —	13.7 −14.1 13.9 −14.7	— −10 — −12	V V V V
Common Mode Rejection (V_{IN} = ±12 V)	CMR	80	100	—	dB
Power Supply Rejection (V_S = 15 to 5.0 V, −15 to −5.0 V)	PSR	80	115	—	dB
Power Supply Current (V_O = 0 V, Both Amplifiers)	I_D	—	4.0	8.0	mA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C unless otherwise noted).

Characteristics	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{IN} = −10 V to +10 V, R_L = 2.0 kΩ, A_V = +1.0)	SR	5.0	7.0	—	V/μs
Gain Bandwidth Product (f = 100 kHz)	GBW	10	15	—	MHz
Unity Gain Frequency (Open Loop)	f_U	—	9.0	—	MHz
Unity Gain Phase Margin (Open Loop)	θ_m	—	60	—	Deg
Equivalent Input Noise Voltage (R_S = 100 Ω, f = 1.0 kHz)	e_n	—	4.5	—	nV/√Hz
Equivalent Input Noise Current (f = 1.0 kHz)	i_n	—	0.5	—	pA/√Hz
Power Bandwidth (V_O = 27 V_{p-p}, R_L = 2.0 kΩ, THD ≤ 1.0%)	BWP	—	120	—	kHz
Distortion (R_L = 2.0 kΩ, f = 20 Hz to 20 kHz, V_O = 3.0 V_{rms}, A_V = +1.0)	THD	—	0.002	—	%
Channel Separation (f = 20 Hz to 20 kHz)	—	—	−120	—	dB

FIGURE 1 — MAXIMUM POWER DISSIPATION versus TEMPERATURE

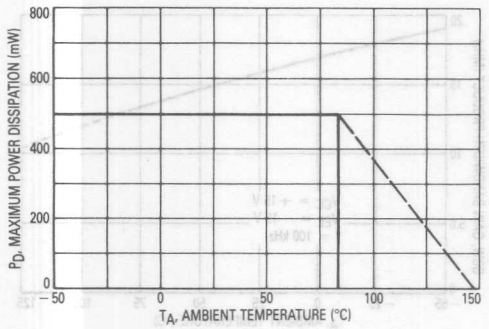


FIGURE 2 — INPUT BIAS CURRENT versus TEMPERATURE

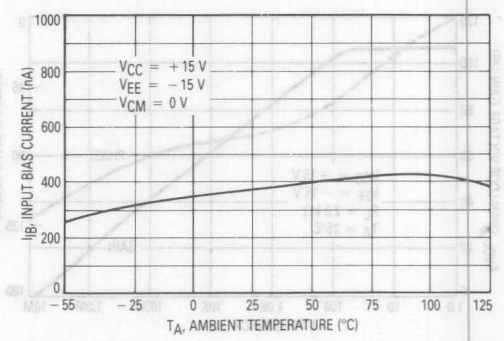


FIGURE 3 — INPUT BIAS CURRENT versus SUPPLY VOLTAGE

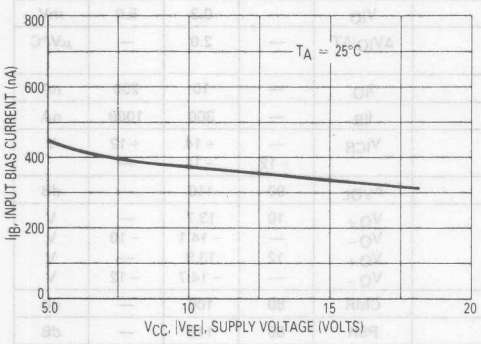


FIGURE 4 — SUPPLY CURRENT versus SUPPLY VOLTAGE

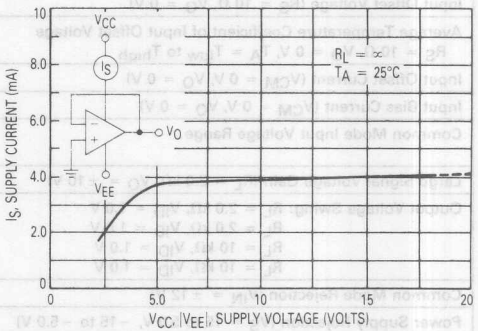


FIGURE 5 — DC VOLTAGE GAIN versus TEMPERATURE

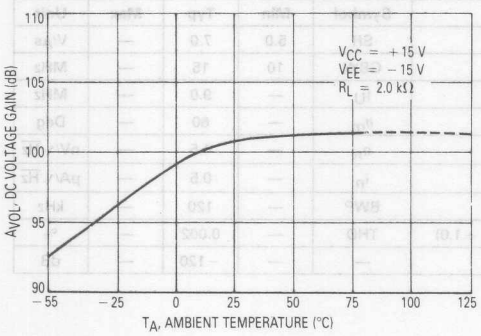


FIGURE 6 — DC VOLTAGE GAIN versus SUPPLY VOLTAGE

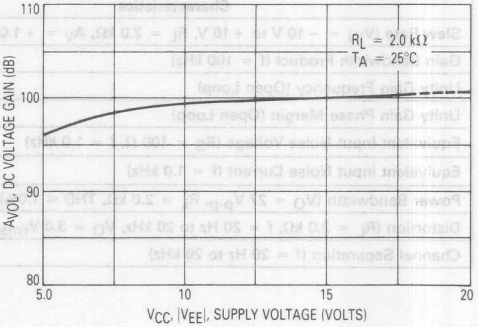


FIGURE 7 — OPEN-LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY

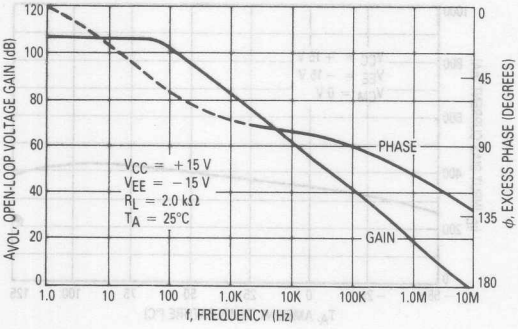


FIGURE 8 — GAIN BANDWIDTH PRODUCT versus TEMPERATURE

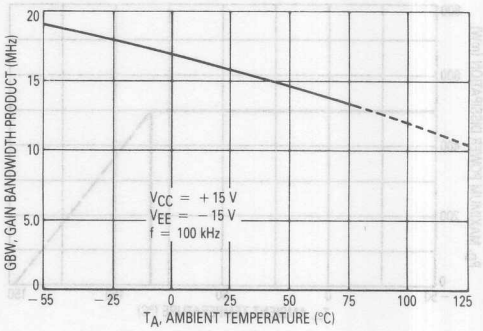


FIGURE 9 — GAIN BANDWIDTH PRODUCT versus SUPPLY VOLTAGE

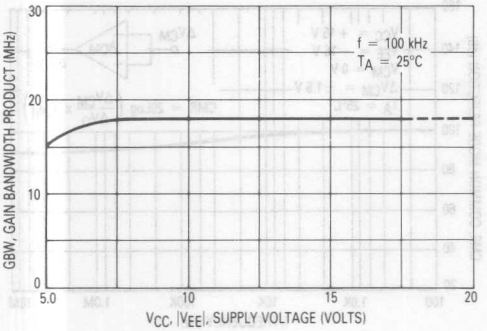


FIGURE 10 — SLEW RATE versus TEMPERATURE

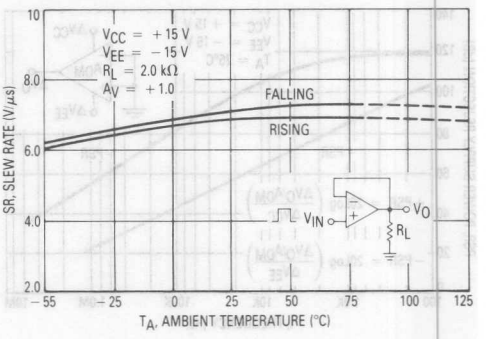


FIGURE 11 — SLEW RATE versus SUPPLY VOLTAGE

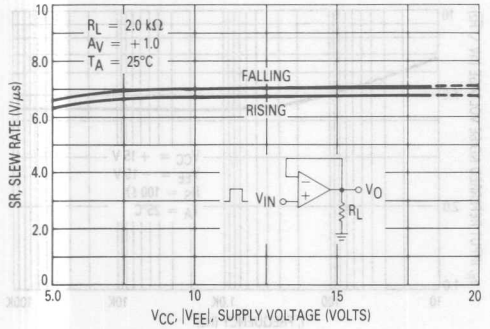


FIGURE 12 — OUTPUT VOLTAGE versus FREQUENCY

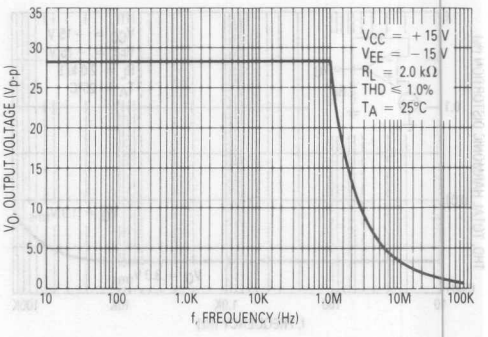


FIGURE 13 — MAXIMUM OUTPUT VOLTAGE versus SUPPLY VOLTAGE

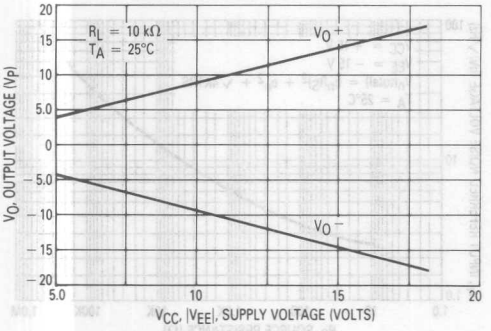
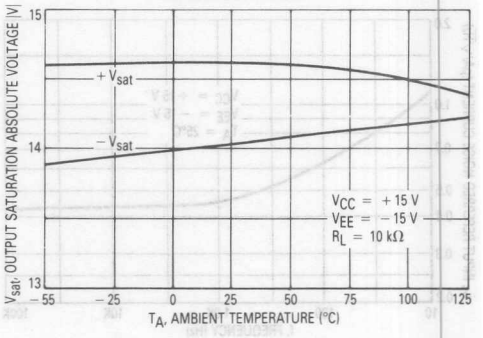


FIGURE 14 — OUTPUT SATURATION VOLTAGE versus TEMPERATURE



2

FIGURE 15 — POWER SUPPLY REJECTION versus FREQUENCY

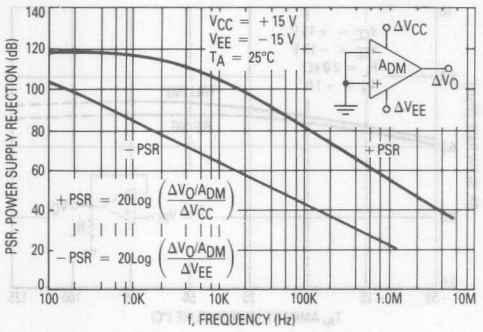


FIGURE 16 — COMMON MODE REJECTION versus FREQUENCY

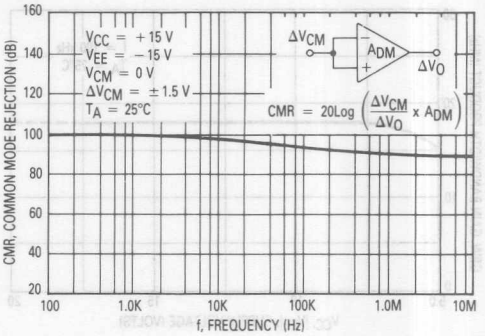


FIGURE 17 — TOTAL HARMONIC DISTORTION versus FREQUENCY

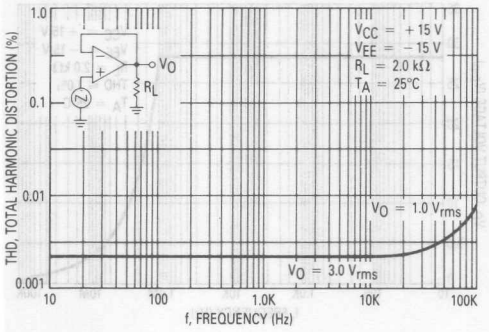


FIGURE 18 — INPUT REFERRED NOISE VOLTAGE versus FREQUENCY

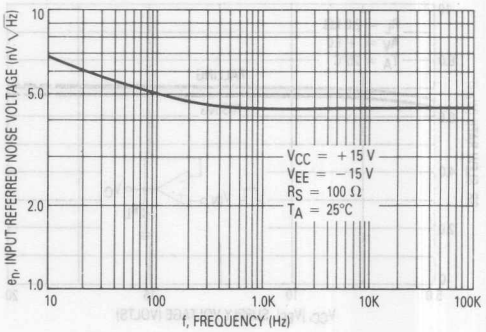


FIGURE 19 — INPUT REFERRED NOISE CURRENT versus FREQUENCY

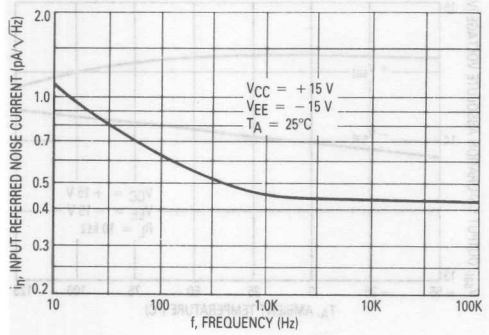


FIGURE 20 — INPUT REFERRED NOISE VOLTAGE versus SOURCE RESISTANCE

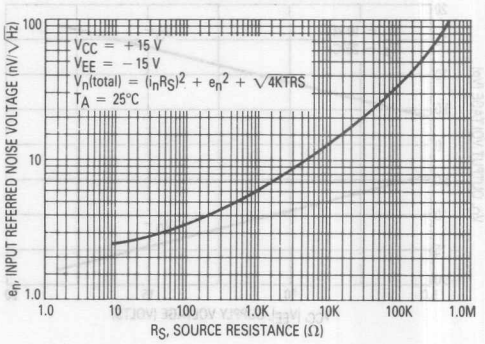


FIGURE 21 — INVERTING AMPLIFIER

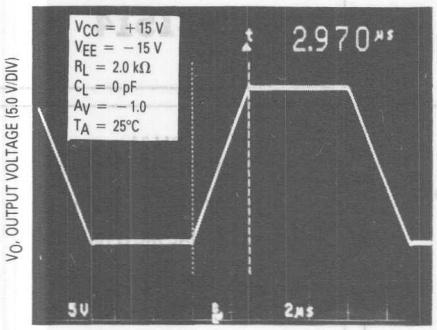


FIGURE 22 — NON-INVERTING AMPLIFIER SLEW RATE

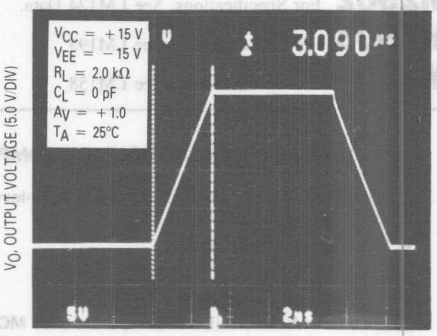
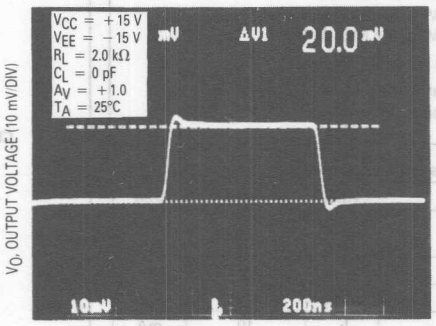


FIGURE 23 — NON-INVERTING AMPLIFIER OVERSHOOT



LM2902 For Specifications, See LM124 Data.
LM2903 For Specifications, See LM193
LM2904 For Specifications, See LM158

MC1514

DUAL DIFFERENTIAL VOLTAGE COMPARATOR

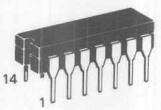
. . . designed for use in level detection, low-level sensing, and memory applications.

- Two Separate Outputs
- Strobe Capability
- High Output Sink Current
  2.8 mA Minimum (Each Comparator) for MC1514
  1.6 mA Minimum (Each Comparator) for MC1414
- Differential Input Characteristics
  Input Offset Voltage = 1.0 mV for MC1514
  = 1.5 mV for MC1414
  Offset Voltage Drift = 3.0 μV/°C for MC1514
  = 5.0 μV/°C for MC1414
- Short Propagation Delay Time — 40 ns Typical
- Output Compatible with All Saturating Logic Forms
  V_O = +3.2 V to −0.5 V Typical

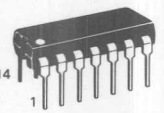
DUAL DIFFERENTIAL COMPARATOR

(DUAL MC1710)

SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 632-08

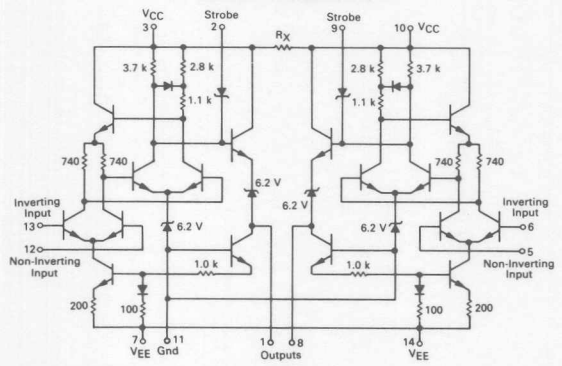


P SUFFIX
PLASTIC PACKAGE
CASE 646-06
(MC1414 Only)

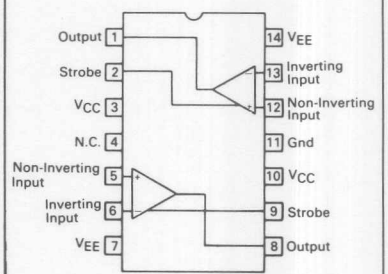
MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC} V_{EE}	+14 −7.0	Vdc
Differential Mode Input Voltage Range	V_{IDR}	±5.0	Vdc
Common Mode Input Voltage Range	V_{ICR}	±7.0	Vdc
Peak Load Current	I_L	10	mA
Power Dissipation (Package Limitation) Ceramic Dual In-Line Package Derate above T_A = 25°C Plastic Dual In-Line Package Derate above T_A = 25°C	P_D	 1000 6.0 625 5.0	 mW mW/°C mW mW/°C
Operating Temperature MC1514 MC1414	T_A	−55 to +125 0 to +75	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

CIRCUIT SCHEMATIC



R_X = Low Resistance Value, usually < 100 Ω, not specified.



ELECTRICAL CHARACTERISTICS (V_{CC} = +12 Vdc, V_{EE} = −6.0 Vdc, T_A = 25°C unless otherwise noted.) (Each Comparator)

Characteristic	Symbol	MC1514 Min	MC1514 Typ	MC1514 Max	MC1414 Min	MC1414 Typ	MC1414 Max	Unit
Input Offset Voltage	V_{IO}							mVdc
(V_O = 1.4 Vdc, T_A = 25°C)		—	1.0	2.0	—	1.5	5.0	
(V_O = 1.8 Vdc, T_A = T_{low}*)		—	—	3.0	—	—	6.5	
(V_O = 1.0 Vdc, T_A = T_{high}*)		—	—	3.0	—	—	6.5	
Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	—	3.0	—	—	5.0	—	μV/°C
Input Offset Current	I_{IO}							μAdc
(V_O = 1.4 Vdc, T_A = 25°C)		—	1.0	3.0	—	1.0	5.0	
(V_O = 1.8 Vdc, T_A = T_{low})		—	—	7.0	—	—	7.5	
(V_O = 1.0 Vdc, T_A = T_{high})		—	—	3.0	—	—	7.5	
Input Bias Current	I_{IB}							μAdc
(V_O = 1.4 Vdc, T_A = 25°C)		—	12	20	—	15	25	
(V_O = 1.8 Vdc, T_A = T_{low})		—	—	45	—	18	40	
(V_O = 1.0 Vdc, T_A = T_{high})		—	—	20	—	—	40	
Open Loop Voltage Gain	A_{vol}							V/V
(T_A = 25°C)		1250	1700	—	1000	1500	—	
(T_A = T_{low} to T_{high})		1000	—	—	800	—	—	
Output Resistance	R_O	—	200	—	—	200	—	Ohms
Differential Voltage Range	V_{IDR}	±5.0	—	—	±5.0	—	—	Vdc
High Level Output Voltage (V_{ID} ≥ 5.0 mV, 0 ≤ I_O ≤ 5.0 mA)	V_{OH}	2.5	3.2	4.0	2.5	3.2	4.0	Vdc
Low Level Output Voltage	V_{OL}							Vdc
(V_{ID} ≥ −5.0 mV, I_{OS} = 2.8 mA)		−1.0	−0.5	0	—	—	—	
(V_{ID} ≥ −5.0 mV, I_{OS} = 1.6 mA)		—	—	—	−1.0	−0.5	0	
Output Sink Current (V_{ID} ≥ −5.0 mV, V_{OL} ≤ 0.4 V, T_A = T_{low} to T_{high})	I_{OS}	2.8	3.4	—	1.6	2.5	—	mAdc
Input Common Mode Voltage Range (V_{EE} = −7.0 Vdc)	V_{ICR}	±5.0	—	—	±5.0	—	—	Vdc
Common-Mode Rejection Ratio (V_{EE} = −7.0 Vdc, R_S ≤ 200 Ω)	CMRR	80	100	—	70	100	—	dB
Strobe Low Level Current (V_{IL} = 0)	I_{IL}	—	—	2.5	—	—	2.5	mA
Strobe High Level Current (V_{IH} = 5.0 Vdc)	I_{IH}	—	—	1.0	—	—	1.0	μA
Strobe Disable Voltage (V_{OL} ≤ 0.4 Vdc)	V_{IL}	—	—	0.4	—	—	0.4	Vdc
Strobe Enable Voltage (V_{OH} ≥ 2.4 Vdc)	V_{IH}	3.5	—	6.0	3.5	—	6.0	Vdc
Propagation Delay Time (Figure 1)	t_{PLH}	—	20	—	—	20	—	ns
	t_{PHL}	—	40	—	—	40	—	
Strobe Response Time (Figure 2)	t_{so}	—	15	—	—	15	—	ns
	t_{sr}	—	6.0	—	—	6.0	—	
Total Power Supply Current, Both Comparators	I_{CC}	—	12.8	18	—	12.8	18	mAdc
(V_O ≤ 0)	I_{EE}	—	11	14	—	11	14	
Total Power Consumption, Both Comparators	P_D	—	230	300	—	230	300	mW

*T_{low} = −55°C for MC1514, 0°C for MC1414
T_{high} = +125°C for MC1514, +75°C for MC1414

FIGURE 1 — PROPAGATION DELAY TIME

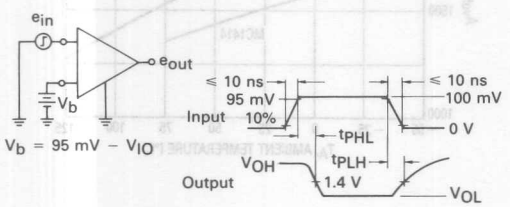
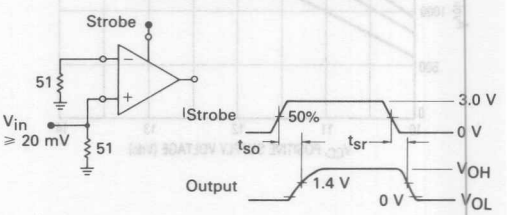


FIGURE 2 — STROBE RESPONSE TIME



2

TYPICAL CHARACTERISTICS
(Each Comparator)

FIGURE 3 — VOLTAGE TRANSFER CHARACTERISTICS

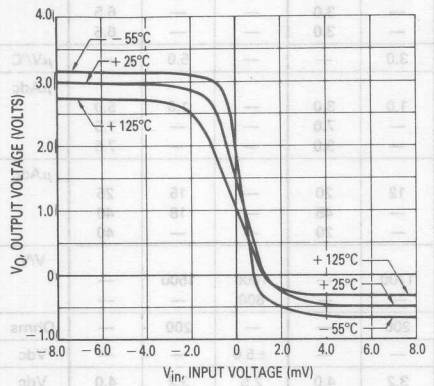


FIGURE 4 — INPUT OFFSET VOLTAGE versus TEMPERATURE

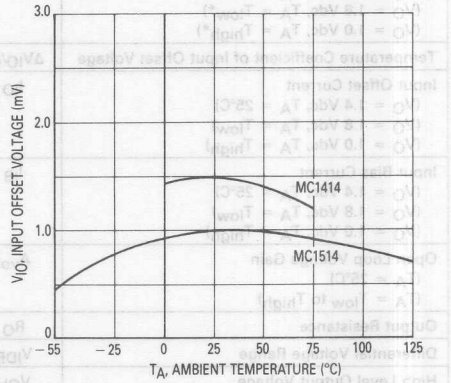


FIGURE 5 — INPUT OFFSET CURRENT versus TEMPERATURE

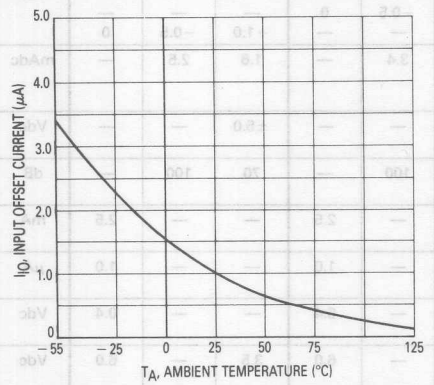


FIGURE 6 — INPUT BIAS CURRENT versus TEMPERATURE

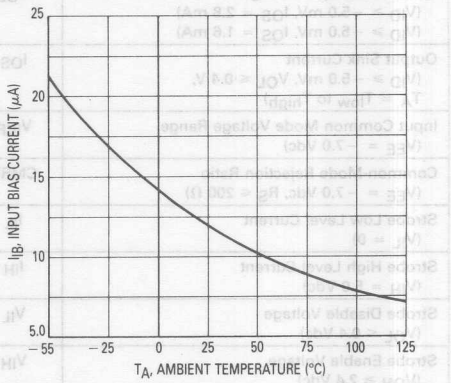


FIGURE 7 — GAIN VARIATION WITH POWER SUPPLY VOLTAGE

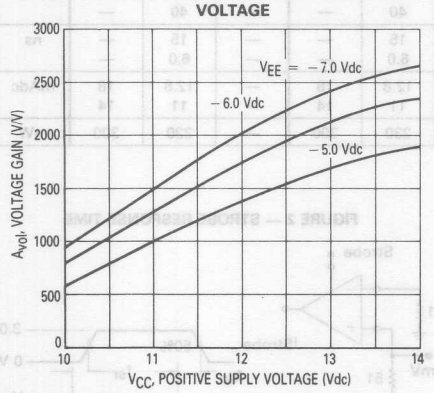


FIGURE 8 — VOLTAGE GAIN versus TEMPERATURE

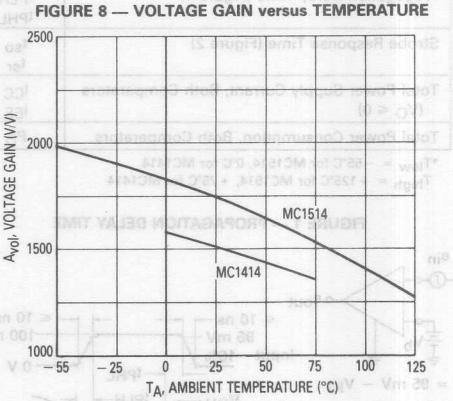


FIGURE 9 — RESPONSE TIME

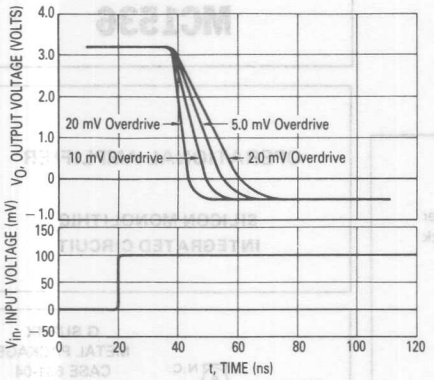


FIGURE 10 — POWER DISSIPATION versus TEMPERATURE

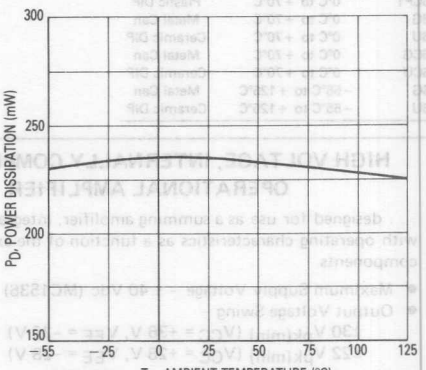


FIGURE 11 — RECOMMENDED SERIES RESISTANCE versus MRTL LOADS

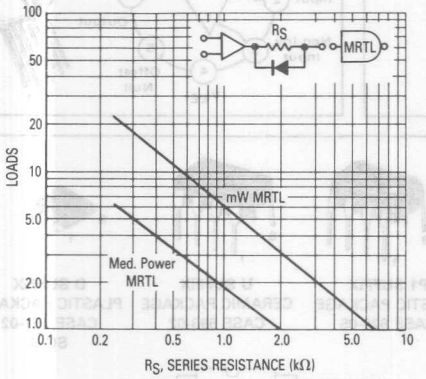


FIGURE 12 — SINK CURRENT versus TEMPERATURE

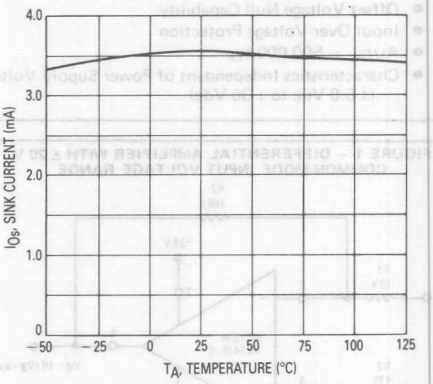
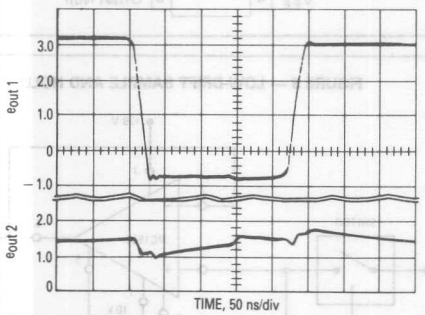
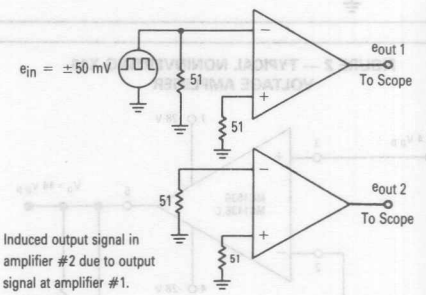


FIGURE 13 — CROSSTALK†



†Worst case condition shown — no load.



MC1436D	0°C to +70°C	SO-8
MC1436P1	0°C to +70°C	Plastic DIP
MC1436CP1	0°C to +70°C	Plastic DIP
MC1436G	0°C to +70°C	Metal Can
MC1436U	0°C to +70°C	Ceramic DIP
MC1436CG	0°C to +70°C	Metal Can
MC1436CU	0°C to +70°C	Ceramic DIP
MC1536G	−55°C to +125°C	Metal Can
MC1536U	−55°C to +125°C	Ceramic DIP

MC1436C
MC1536

OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

HIGH VOLTAGE, INTERNALLY COMPENSATED OPERATIONAL AMPLIFIER

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- Maximum Supply Voltage – ± 40 Vdc (MC1536)
- Output Voltage Swing –
  ±30 $V_{pk(min)}$ (V_{CC} = +36 V, V_{EE} = -36 V) (MC1536)
  ±22 $V_{pk(min)}$ (V_{CC} = +28 V, V_{EE} = -28 V)
- Input Bias Current – 20 nA max (MC1536)
- Input Offset Current – 3.0 nA max (MC1536)
- Fast Slew Rate – 2.0 V/μs typ
- Internally Compensated
- Offset Voltage Null Capability
- Input Over-Voltage Protection
- A_{VOL} – 500,000 typ
- Characteristics Independent of Power Supply Voltages – (±5.0 Vdc to ± 36 Vdc)

G SUFFIX
METAL PACKAGE
CASE 601-04

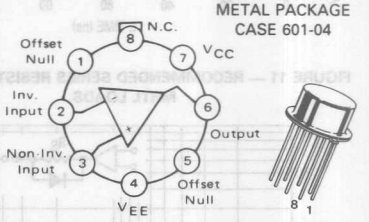
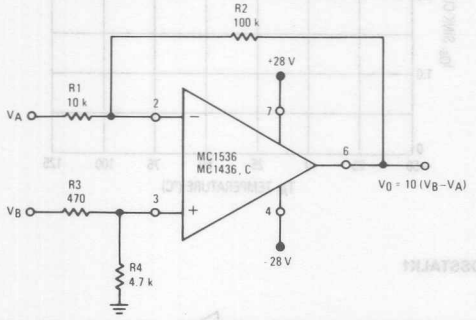
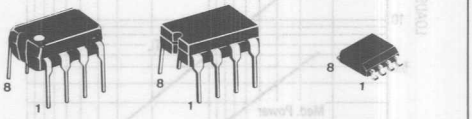


FIGURE 1 – DIFFERENTIAL AMPLIFIER WITH ± 20 V COMMON-MODE INPUT VOLTAGE RANGE





P1 SUFFIX
PLASTIC PACKAGE
CASE 626-05

U SUFFIX
CERAMIC PACKAGE
CASE 693-02

D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SO-8

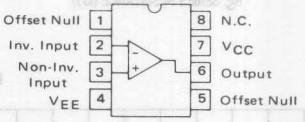


FIGURE 2 — TYPICAL NONINVERTING X10 VOLTAGE AMPLIFIER

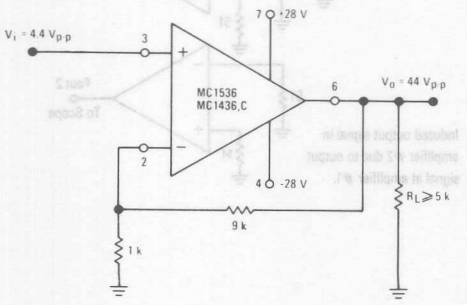
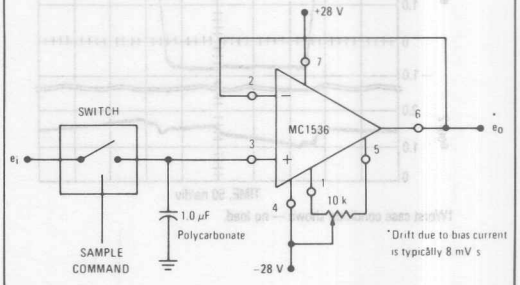


FIGURE 3 — LOW-DRIFT SAMPLE AND HOLD



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	MC1536	MC1436	MC1436C	Unit
Power Supply Voltage	V_{CC} V_{EE}	+40 -40	+34 -34	+30 -30	Vdc
Input Differential Voltage Range	V_{IDR}	Note 3			Volts
Input Common-Mode Voltage Range	V_{ICR}	Note 3			Volts
Output Short Circuit Duration (V_{CC} = V_{EE} = 28 Vdc, V_o = 0)	t_S	5.0			s
Power Dissipation (Package Limitation) Derate above T_A = +25°C	P_D	680 4.6			mW mW/°C
Operating Ambient Temperature Range	T_A	-55 to +125	0 to +70		°C
Storage Temperature Range	T_{stg}	-65 to +150			°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +28 Vdc, V_{EE} = -28 Vdc, T_A = +25°C unless otherwise noted)

Characteristics	Symbol	MC1536 Min	MC1536 Typ	MC1536 Max	MC1436 Min	MC1436 Typ	MC1436 Max	MC1436C Min	MC1436C Typ	MC1436C Max	Unit
Input Bias Current	I_{IB}										nAdc
T_A = +25°C		–	8.0	20	–	15	40	–	25	90	
T_A = T_{low} to T_{high} (See Note 1)		–	–	35	–	–	55	–	–	–	
Input Offset Current	I_{IO}										nAdc
T_A = +25°C		–	1.0	3.0	–	5.0	10	–	10	25	
T_A = +25°C to T_{high}		–	–	4.5	–	–	14	–	–	–	
T_A = T_{low} to +25°C		–	–	7.0	–	–	14	–	–	–	
Input Offset Voltage	V_{IO}										mVdc
T_A = +25°C		–	2.0	5.0	–	5.0	10	–	5.0	12	
T_A = T_{low} to T_{high}		–	–	7.0	–	–	14	–	–	–	
Differential Input Impedance (Open-Loop, f ≤ 5.0 Hz)											
Parallel Input Resistance	r_P	–	10	–	–	10	–	–	10	–	Meg ohms
Parallel Input Capacitance	C_P	–	2.0	–	–	2.0	–	–	2.0	–	pF
Common-Mode Input Impedance (f ≤ 5.0 Hz)	z_{ic}	–	250	–	–	250	–	–	250	–	Meg ohms
Input Common-Mode Voltage Range	V_{ICR}	±24	±25		±22	±25	–	±18	±20	–	V_{pk}
Equivalent Input Noise Voltage	e_n										nV/(Hz)½
(A_V = 100, R_s = 10 k ohms, f = 1.0 kHz, BW = 1.0 Hz)		–	50	–	–	50	–		50	–	
Common-Mode Rejection Ratio (dc)	CMRR	80	110	–	70	110	–	50	90	–	dB
Large Signal dc Open Loop Voltage Gain	A_{VOL}										V/V
(V_o = ± 10 V, R_L = 100 k ohms) T_A = +25°C		100,000	500,000	–	70,000	500,000	–	50,000	500,000	–	
(V_o = ± 10 V, R_L = 100 k ohms) T_A = T_{low} to T_{high}		50,000	–	–	50,000	–	–		–		
(V_o = ±10 V, R_L = 10 k ohms, T_A = +25°C)			200,000			200,000			200,000		
Power Bandwidth (Voltage Follower)	BW_P										kHz
(A_V = 1, R_L = 5.0 k ohms, THD ≤ 5%, V_o = 40 Vp-p)		–	23	–	–	23	–		23		
Unity Gain Crossover Frequency (open-loop)	f_c	–	1.0	–	–	1.0	–		1.0		MHz
Phase Margin (open-loop, unity gain)	ϕ_m	–	50	–	–	50	–	–	50		degrees
Gain Margin	A_M		18			18			18		dB
Slew Rate (Unity Gain)	SR		2.0	–	–	2.0			2.0		V/μs
Output Impedance (f ≤ 5.0 Hz)	z_o		1.0			1.0	–		1.0		k ohms
Short-Circuit Output Current	I_{OS}	–	±17			±17			±19		mAdc
Output Voltage Range (R_L = 5.0 k ohms)	V_{OR}										V_{pk}
V_{CC} = +28 Vdc, V_{EE} = -28 Vdc		+22	±23	–	±20	±22	–	±20	±22		
V_{CC} = +36 Vdc, V_{EE} = -36 Vdc		±30	±32	–	–	–	–		–		
Power Supply Sensitivity (dc)											μV/V
V_{EE} = constant, R_s ≤ 10 k ohms	PSS+	–	15	100	–	35	200		50		
V_{CC} = constant, R_s ≤ 10 k ohms	PSS-		15	100	–	35	200		50		
Power Supply Current (See Note 2)	I_{CC}		2.2	4.0	–	2.6	5.0		2.6	5.0	mAdc
	I_{EE}	–	2.2	4.0	–	2.6	5.0	–	2.6	5.0	
DC Quiescent Power Consumption	P_C										mW
(V_o = 0)		–	124	224	–	146	280		146	280	

Note 1: T_{low} 0°C for MC1436,C
-55°C for MC1536
T_{high} +70°C for MC1436,C
+125°C for MC1536

Note 2: V_{CC} - V_{EE} = 5.0 Vdc to 36 Vdc for MC1536
V_{CC} - V_{EE} = 5.0 Vdc to 30 Vdc for MC1436
V_{CC} - V_{EE} = 5.0 Vdc to 28 Vdc for MC1436C

Note 3: Either or both input voltages must not exceed the magnitude of V_{CC} or V_{EE} +3.0 volts.

2

FIGURE 4 – POWER BANDWIDTH

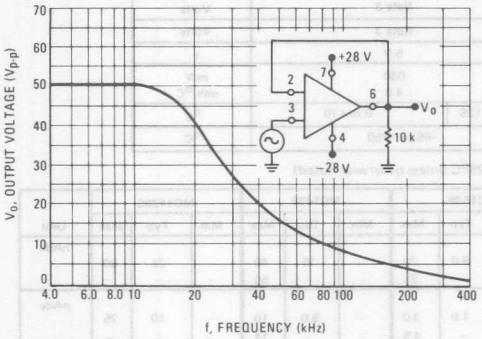


FIGURE 5 – PEAK OUTPUT VOLTAGE SWING, versus POWER SUPPLY VOLTAGE

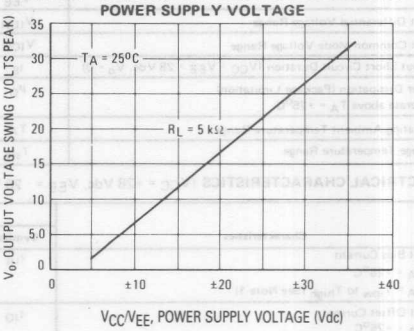


FIGURE 6 – OPEN-LOOP FREQUENCY RESPONSE

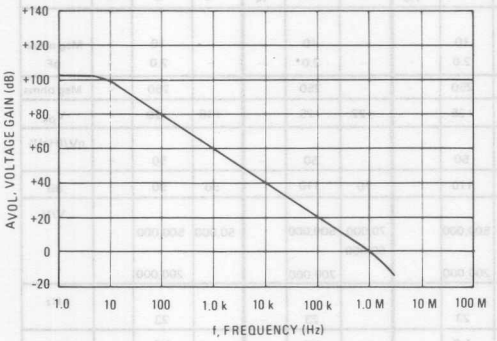


FIGURE 7 – OUTPUT SHORT-CIRCUIT CURRENT versus TEMPERATURE

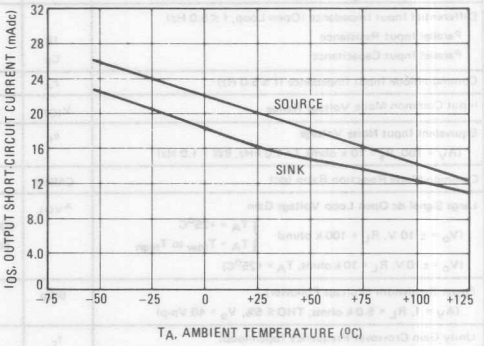


FIGURE 8 – INPUT BIAS CURRENT versus TEMPERATURE

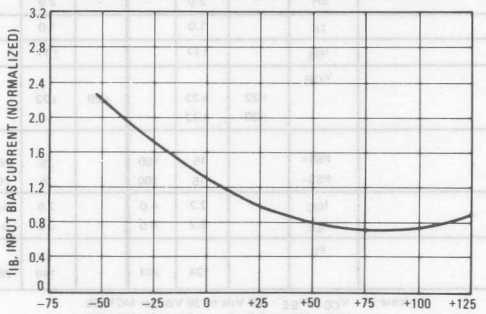


FIGURE 9 – INVERTING FEEDBACK MODEL

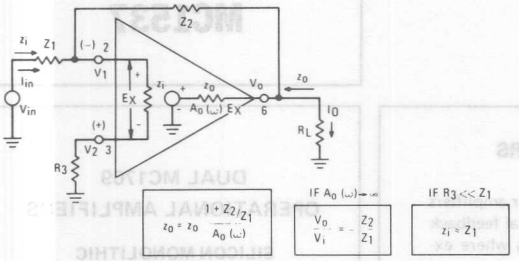


FIGURE 10 – NON-INVERTING FEEDBACK MODEL

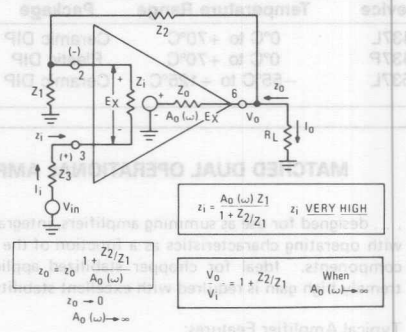


FIGURE 11 – AUDIO AMPLIFIER

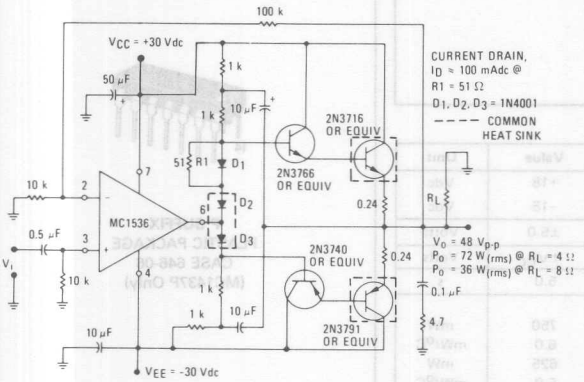


FIGURE 12 – VOLTAGE CONTROLLED CURRENT SOURCE or TRANSCONDUCTANCE AMPLIFIER WITH 0 TO 40 V COMPLIANCE

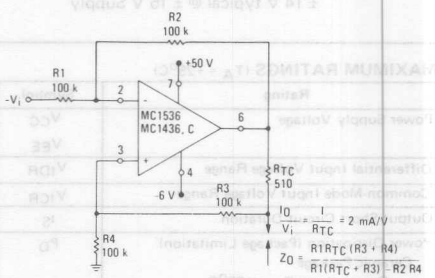


FIGURE 13 – REPRESENTATIVE CIRCUIT SCHEMATIC

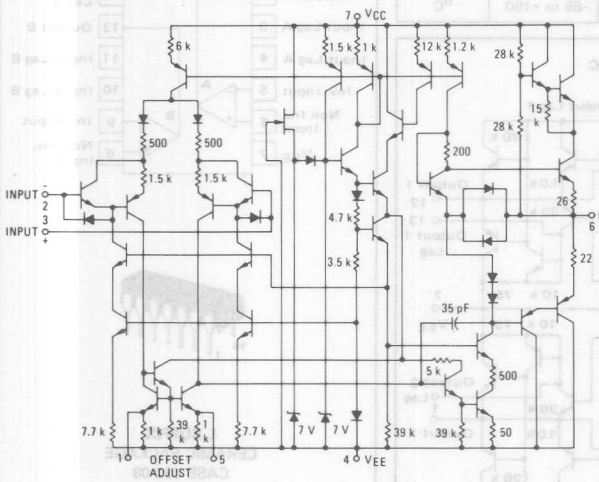
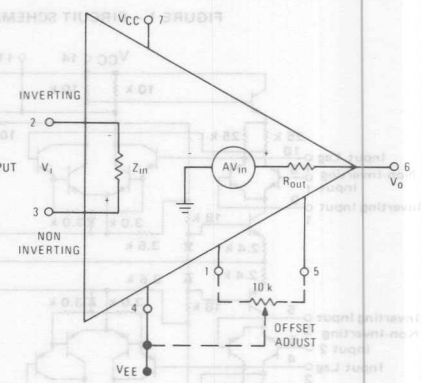


FIGURE 14 – EQUIVALENT CIRCUIT



MC1437L	0°C to +70°C	Ceramic DIP
MC1437P	0°C to +70°C	Plastic DIP
MC1537L	−55°C to +125°C	Ceramic DIP

MATCHED DUAL OPERATIONAL AMPLIFIERS

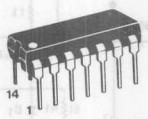
. . . designed for use as summing amplifiers, integrators, or amplifiers with operating characteristics as a function of the external feedback components. Ideal for chopper stabilized applications where extremely high gain is required with excellent stability.

Typical Amplifier Features:

- High-Performance Open Loop Gain Characteristics – A_{VOL} = 45,000 typical
- Low Temperature Drift – ± 3 μV/°C
- Large Output Voltage Swing – ± 14 V typical @ ± 15 V Supply

DUAL MC1709 OPERATIONAL AMPLIFIERS

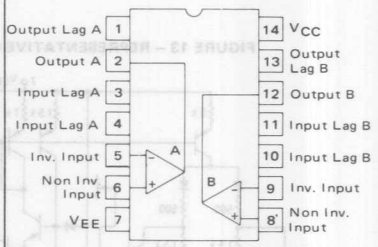
SILICON MONOLITHIC INTEGRATED CIRCUIT

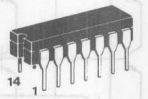


P SUFFIX
PLASTIC PACKAGE
CASE 646-06
(MC1437P Only)

MAXIMUM RATINGS (T_A = +25°C)

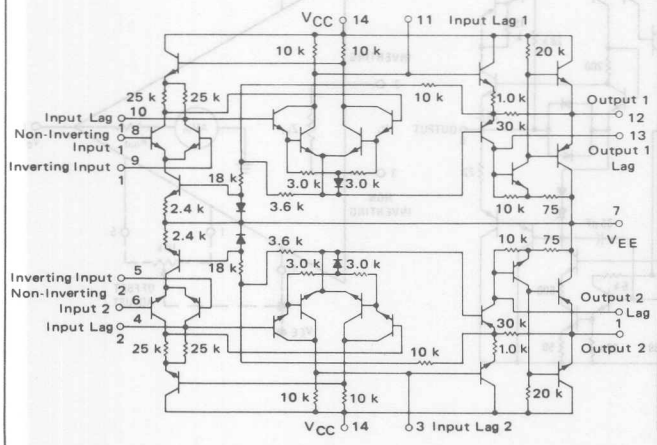
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+18	Vdc
	V_{EE}	-18	Vdc
Differential Input Voltage Range	V_{IDR}	±5.0	Volts
Common-Mode Input Voltage Range	V_{ICR}	±V_{CC}	Volts
Output Short Circuit Duration	t_S	5.0	s
Power Dissipation (Package Limitation)	P_D		
Ceramic Package		750	mW
Derate above T_A = +25°C		6.0	mW/°C
Plastic Package MC1437P		625	mW
Derate above T_A = +25°C		5.0	mW/°C
Operating Ambient Temperature Range	T_A		°C
MC1537		-55 to +125	
MC1437		0 to +70	
Storage Temperature Range	T_{stg}	-65 to +150	°C





L SUFFIX
CERAMIC PACKAGE
CASE 632-08

FIGURE 1 – CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS – Each Amplifier (V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC1537 Min	MC1537 Typ	MC1537 Max	MC1437 Min	MC1437 Typ	MC1437 Max	Unit
Open Loop Voltage Gain (R_L = 5.0 kΩ, V_o = ± 10 V, T_A = T_{low} ① to T_{high} ②)	A_{VOL}	25,000	45,000	70,000	15,000	45,000	–	–
Output Impedance (f = 20 Hz)	z_o	–	30	–	–	30	–	Ω
Input Impedance (f = 20 Hz)	z_i	150	400	–	50	150	–	kΩ
Output Voltage Range (R_L = 10 kΩ)	V_{OR}	+12	+14	–	±12	±14	–	V_{peak}
(R_L = 2.0 kΩ)		+10	±13	–	–	–	–	
Input Common-Mode Voltage Range	V_{ICR}	+8.0	±10	–	+8.0	±10	–	V_{peak}
Common-Mode Rejection Ratio	CMRR	70	100	–	65	100	–	dB
Input Bias Current ($I_{IB} = \frac{I_1 + I_2}{2}$) ($T_A$ = +25°C)	I_{IB}	–	0.2	0.5	–	0.4	1.5	µA
(T_A = T_{low} ①)		–	0.5	1.5	–	–	2.0	
Input Offset Current ($I_{IO} = I_1 - I_2$)	I_{IO}	–	0.05	0.2	–	0.05	0.5	µA
($I_{IO} = I_1 - I_2$, T_A = T_{low} ①)		–	–	0.5	–	–	0.75	
($I_{IO} = I_1 - I_2$, T_A = T_{high} ②)		–	–	0.2	–	–	0.75	
Input Offset Voltage (T_A = +25°C)	V_{IO}	–	1.0	5.0	–	1.0	7.5	mV
(T_A = T_{low} ① to T_{high} ②)		–	–	6.0	–	–	10	
Step Response								
Gain = 100, 5% overshoot, R_1 = 1 kΩ, R_2 = 100 kΩ, R_3 = 1.5 kΩ, C_1 = 100 pF, C_2 = 3.0 pF	t_{TLH}	–	0.8	–	–	0.8	–	µs
	t_{PLH}-t_{PHL}	–	0.38	–	–	0.38	–	µs
	SR	–	12	–	–	12	–	V/µs
Gain = 10, 10% overshoot, R_1 = 1 kΩ, R_2 = 10 kΩ, R_3 = 1.5 kΩ, C_1 = 500 pF, C_2 = 20 pF	t_{TLH}	–	0.6	–	–	0.6	–	µs
	t_{PLH}-t_{PHL}	–	0.34	–	–	0.34	–	µs
	SR	–	1.7	–	–	1.7	–	V/µs
Gain = 1, 5% overshoot, R_1 = 10 kΩ, R_2 = 10 kΩ, R_3 = 1.5 kΩ, C_1 = 5000 pF, C_2 = 200 pF	t_{TLH}	–	2.2	–	–	2.2	–	µs
	t_{PLH}-t_{PHL}	–	1.3	–	–	1.3	–	µs
	SR	–	0.25	–	–	0.25	–	V/µs
Average Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω, T_A = T_{low} ① to T_{high} ②)	$\Delta V_{IO}/\Delta T$	–	1.5	–	–	1.5	–	µV/°C
($R_S \leq$ 10 kΩ, T_A = T_{low} ① to T_{high} ②)		–	3.0	–	–	3.0	–	
Average Temperature Coefficient of Input Offset Voltage (T_A = T_{low} ① to +25°C)	$\Delta I_{IO}/\Delta T$	–	0.7	–	–	0.7	–	nA/°C
(T_A = +25°C to T_{high} ②)		–	0.7	–	–	0.7	–	
DC Power Consumption (Total) (Power Supply = ± 15 V, V_o = 0)	P_C	–	160	225	–	160	225	mW
Positive Supply Sensitivity (V_{EE} constant)	PSS+	–	10	150	–	10	200	µV/V
Negative Supply Sensitivity (V_{CC} constant)	PSS-	–	10	150	–	10	200	µV/V

① T_{low} = 0°C for MC1437, = -55°C for MC1537

② T_{high} = +70°C for MC1437, = +125°C for MC1537

MATCHING CHARACTERISTICS

Open Loop Voltage Gain	A_{VOL1}-A_{VOL2}	–	±1.0	–	–	±1.0	–	dB
Input Bias Current	I_{IB1}-I_{IB2}	–	±0.15	–	–	±0.15	–	µA
Input Offset Current	I_{IO1}-I_{IO2}	–	±0.02	–	–	±0.02	–	µA
Average Temperature Coefficient	$\left\lvert\frac{\Delta I_{IO1}}{\Delta T}\right\rvert$ - $\left\lvert\frac{\Delta I_{IO2}}{\Delta T}\right\rvert$	–	±0.2	–	–	±0.2	–	nA/°C
Input Offset Voltage	V_{IO1}-V_{IO2}	–	±0.2	–	–	±0.2	–	mV
Average Temperature Coefficient	$\left\lvert\frac{\Delta V_{IO1}}{\Delta T}\right\rvert$ - $\left\lvert\frac{\Delta V_{IO2}}{\Delta T}\right\rvert$	–	±0.5	–	–	±0.5	–	µV/°C
Channel Separation (f = 10 kHz)	$\frac{e_{o1}}{e_{o2}}$	–	90	–	–	90	–	dB

2

TYPICAL OUTPUT CHARACTERISTICS

FIGURE 3 – TEST CIRCUIT

V_{CC} = +15 Vdc, V_{EE} = 15 Vdc, T_A = 25°C

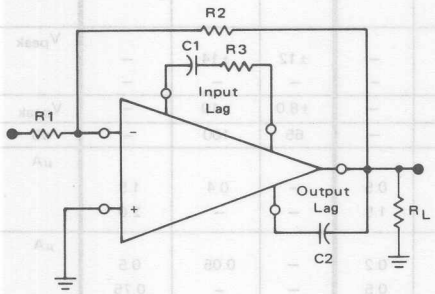


FIGURE NO.	CURVE NO.	VOLTAGE GAIN	TEST CONDITIONS $R_1(\Omega)$	$R_2(\Omega)$	$R_3(\Omega)$	C_1(pF)	C_2(pF)	OUTPUT NOISE (mV(rms))
4	1	1	10 k	10 k	1.5 k	5.0 k	200	0.10
	2	10	10 k	100 k	1.5 k	500	20	0.14
	3	100	10 k	1.0 M	1.5 k	100	3.0	0.7
	4	1000	1.0 k	1.0 M	0	10	3.0	5.2
5	1	1	10 k	10 k	1.5 k	5.0 k	200	0.10
	2	10	10 k	100 k	1.5 k	500	20	0.14
	3	100	10 k	1.0 M	1.5 k	100	3.0	0.7
	4	1000	1.0 k	1.0 M	0	10	3.0	5.2
6	1	A_{VOL}	0	∞	1.5 k	5.0 k	200	5.5
	2	A_{VOL}	0	∞	1.5 k	500	20	10.5
	3	A_{VOL}	0	∞	1.5 k	100	3.0	21.0
	4	A_{VOL}	0	∞	0	10	3.0	39.0
	5	A_{VOL}	0	∞	∞	0	3.0	—

FIGURE 4 – LARGE SIGNAL SWING versus FREQUENCY

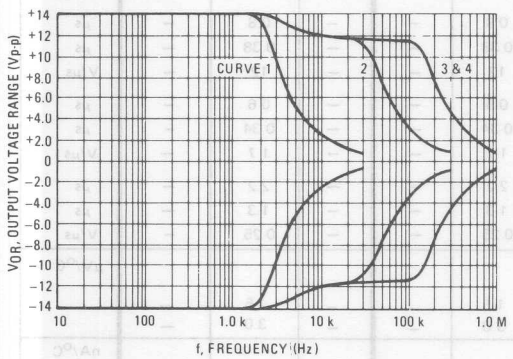


FIGURE 5 – VOLTAGE GAIN versus FREQUENCY

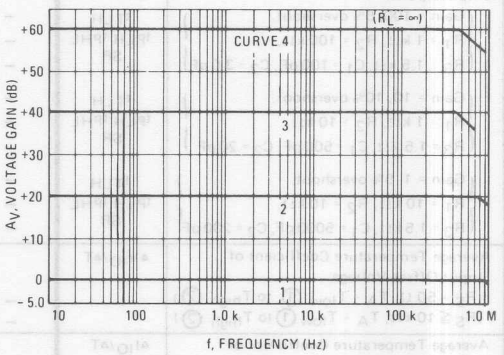


FIGURE 6 – OPEN LOOP VOLTAGE GAIN versus FREQUENCY

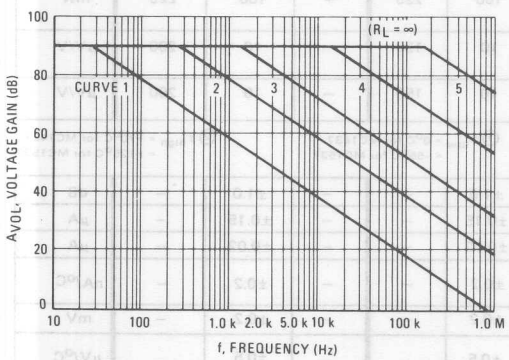
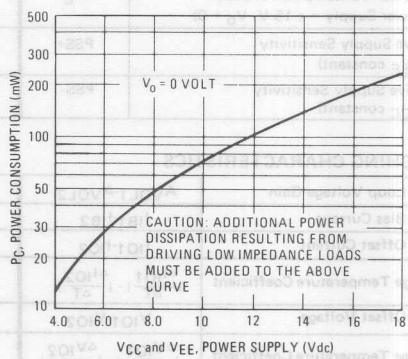


FIGURE 7 – TOTAL POWER CONSUMPTION versus POWER SUPPLY VOLTAGE



TYPICAL CHARACTERISTICS (continued)

FIGURE 8 – VOLTAGE GAIN versus POWER SUPPLY VOLTAGE

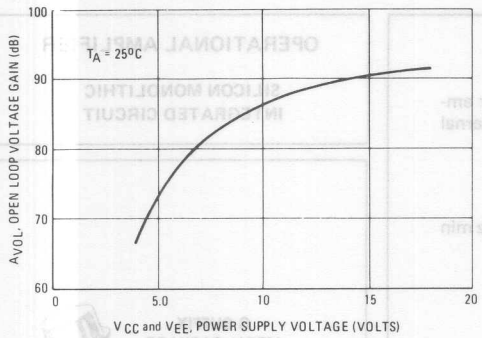


FIGURE 9 – COMMON INPUT SWING versus POWER SUPPLY VOLTAGE

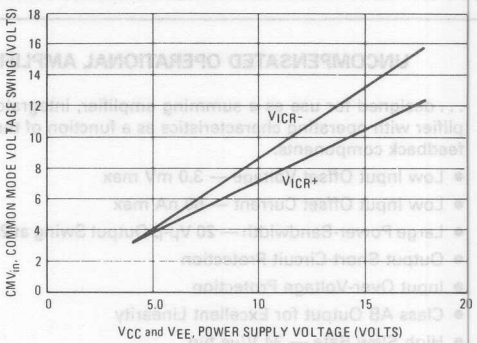


FIGURE 10 – INPUT OFFSET VOLTAGE versus TEMPERATURE

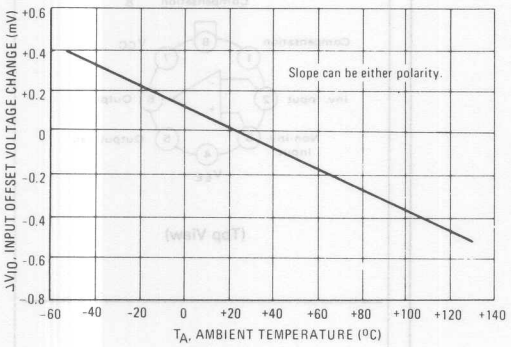


FIGURE 11 – OUTPUT NOISE VOLTAGE versus SOURCE RESISTANCE

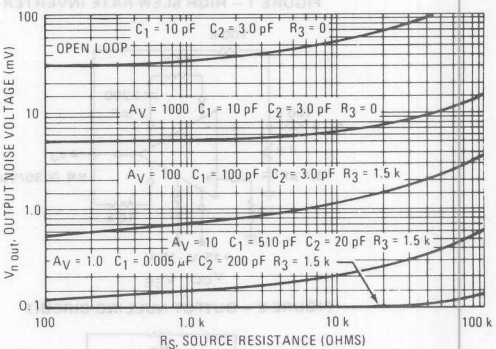
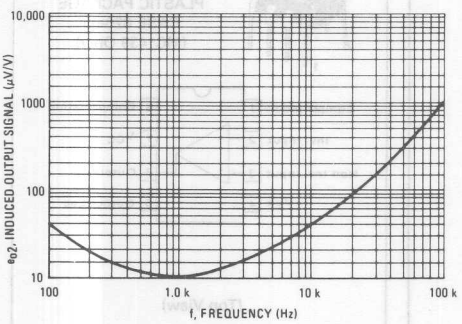
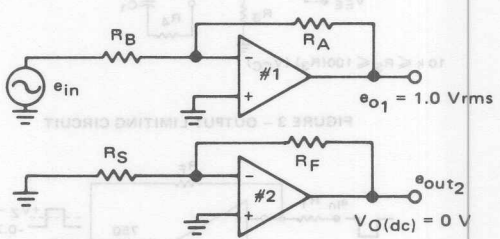


FIGURE 12 – INDUCED OUTPUT SIGNAL (CHANNEL SEPARATION) versus FREQUENCY





Induced output signal (μV of induced output signal in amplifier #2 per volt of output signal at amplifier #1).

Device	Temperature Range	Package
MC1439G	0°C to +70°C	Metal Can
MC1439P1	0°C to +70°C	Plastic DIP
MC1539G	−55°C to +125°C	Metal Can

MC1539

UNCOMPENSATED OPERATIONAL AMPLIFIER

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- Low Input Offset Voltage — 3.0 mV max
- Low Input Offset Current — 60 nA max
- Large Power-Bandwidth — 20 Vp-p Output Swing at 20 kHz min
- Output Short-Circuit Protection
- Input Over-Voltage Protection
- Class AB Output for Excellent Linearity
- High Slew Rate — 34 V/μs typ

OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

FIGURE 1 – HIGH SLEW-RATE INVERTER

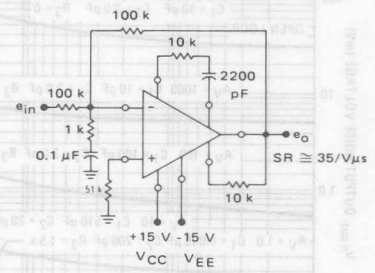
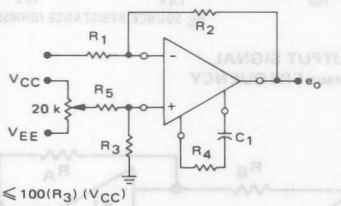
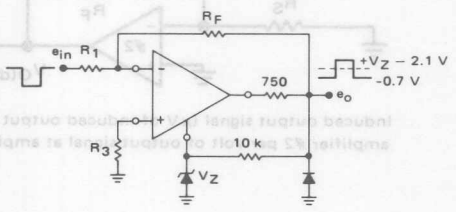


FIGURE 2 – OUTPUT NULLING CIRCUIT



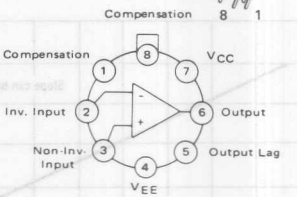
$10\ k \leqslant R_S \leqslant 100(R_3)\ (V_{CC})$

FIGURE 3 – OUTPUT LIMITING CIRCUIT



G SUFFIX
METAL PACKAGE
CASE 601-04

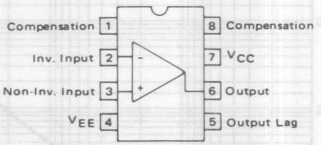




(Top View)

P1 SUFFIX
PLASTIC PACKAGE
CASE 626-05
(MC1439 Only)





(Top View)

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC1539 Min	MC1539 Typ	MC1539 Max	MC1439 Min	MC1439 Typ	MC1439 Max	Unit
Input Bias Current	I_{IB}							μA
(T_A = +25°C)		–	0.20	0.50	–	0.20	1.0	
(T_A = T_{low} ①)		–	0.23	0.70	–	0.23	1.5	
Input Offset Current	$\|I_{IO}\|$							nA
(T_A = T_{low})		–	–	75	–	–	150	
(T_A = +25°C)		–	20	60	–	20	100	
(T_A = T_{high} ①)		–	–	75	–	–	150	
Input Offset Voltage	$\|V_{IO}\|$							mV
(T_A = +25°C)		–	1.0	3.0	–	2.0	7.5	
(T_A = T_{low}, T_{high})		–	–	4.0	–	–	–	
Average Temperature Coefficient of Input Offset Voltage (T_A = T_{low} to T_{high})	$\|TCV_{IO}\|$							μV/°C
(R_S = 50 Ω)		–	3.0	–	–	3.0	–	
($R_S \leq$ 10 kΩ)		–	5.0	–	–	5.0	–	
Input Impedance (f = 20 Hz)	z_{in}	150	300	–	100	300	–	kΩ
Input Common-Mode Voltage Range	V_{ICR}	±11	±12	–	±11	±12	–	V_{pk}
Equivalent Input Noise Voltage (R_S = 10 kΩ, Noise Bandwidth = 1.0 Hz, f = 1.0 kHz)	e_n	–	30	–	–	30	–	nV/(Hz)½
Common-Mode Rejection Ratio (f = 1.0 kHz)	CMRR	80	110	–	80	110		dB
Open-Loop Voltage Gain (V_O = ±10 V, R_L = 10 kΩ, R_S = ∞) (T_A = +25°C to T_{high})	A_{VOL}	50,000	120,000	–	15,000	100,000	–	–
(T_A = T_{low})		25,000	100,000	–	15,000	100,000	–	
Power Bandwidth (A_v = 1, THD ≤ 5%, V_O = 20 Vp-p)	PBW							kHz
(R_L = 2.0 kΩ)		–	–	–	10	50	–	
(R_L = 1.0 kΩ, R_S = 10 k)		20	50	–	–	–	–	
Step Response								
Gain = 1000, no overshoot, R1 = 1.0 kΩ, R2 = 1.0 MΩ, R3 = 1.0 kΩ, R4 = 30 kΩ, R5 = 10 kΩ, C1 = 1000 pF	t_{THL}	–	130	–	–	130	–	ns
	t_{pd}	–	190	–	–	190	–	ns
	SR	–	6.0	–	–	6.0	–	V/μs
Gain = 1000, 15% overshoot, R1 = 1.0 kΩ, R2 = 1.0 MΩ, R3 = 1.0 kΩ, R4 = 0, R5 = 10 kΩ, C1 = 10 pF	t_{THL}	–	80	–	–	80	–	ns
	t_{pd}	–	100	–	–	100	–	ns
	SR	–	14	–	–	14	–	V/μs
Gain = 100, no overshoot, R1 = 1.0 kΩ, R2 = 100 kΩ, R3 = 1.0 kΩ, R4 = 10 kΩ, R5 = 10 kΩ, C1 = 2200 pF	t_{THL}	–	60	–	–	60	–	ns
	t_{pd}	–	100	–	–	100	–	ns
	SR	–	34	–	–	34	–	V/μs
Gain = 10, 15% overshoot, R1 = 1.0 kΩ, R2 = 10 kΩ, R3 = 1.0 kΩ, R4 = 1.0 kΩ, R5 = 10 kΩ, C1 = 2200 pF	t_{THL}	–	120	–	–	120	–	ns
	t_{pd}	–	80	–	–	80	–	ns
	SR	–	6.25	–	–	6.25	–	V/μs
Gain = 1, 15% overshoot, R1 = 10 kΩ, R2 = 10 kΩ, R3 = 5.0 kΩ, R4 = 390 Ω, R5 = 10 kΩ, C1 = 2200 pF	t_{THL}	–	160	–	–	160	–	ns
	t_{pd}	–	80	–	–	80	–	ns
	SR	–	4.2	–	–	4.2	–	V/μs
Output Impedance (f = 20 Hz)	z_o	–	4.0	–	–	4.0	–	kΩ
Output Voltage Swing (R_L = 2.0 kΩ, f = 1.0 kHz)	V_O	–	–	–	±10	±13	–	V_{pk}
(R_L = 1.0 kΩ, f = 1.0 kHz)		±10	±13	–	–	–	–	
Positive Supply Rejection Ratio (V_{EE} constant, R_S = ∞)	PSRR+	–	50	150	–	50	200	μV/V
Negative Supply Rejection Ratio (V_{CC} constant, R_S = ∞)	PSRR-	–	50	150	–	50	200	μV/V
Power Supply Current (V_O = 0)	I_{CC}	–	3.0	5.0	–	3.0	6.7	mAdc
	I_{EE}	–	3.0	5.0	–	3.0	6.7	

① T_{low} = 0°C for MC1439, −55°C for MC1539 T_{high} = +70°C for MC1439, +125°C for MC1539

2

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 +18	Vdc
Differential Input Voltage Range	V_{IDR}	±(V_{CC} + |V_{EE}|)	Vdc
Common-Mode Input Voltage Range	V_{ICR}	+V_{CC},-|V_{EE}|	Vdc
Load Current	I_L	15	mA
Output Short-Circuit Duration	t_S	Continuous	
Power Dissipation (Package Limitation) Metal Package Derate above T_A = +25°C Plastic Dual In-Line Packages MC1439 Derate above T_A = +25°C	P_D	 680 4.6 625 5.0	 mW mW/°C mW mW/°C
Operating Temperature Range MC1539 MC1439	T_A	-55 to +125 0 to +70	°C
Storage Temperature Range Metal Packages Plastic Packages	T_{stg}	 -65 to +150 -55 to +125	°C

FIGURE 4 – EQUIVALENT CIRCUIT SCHEMATIC

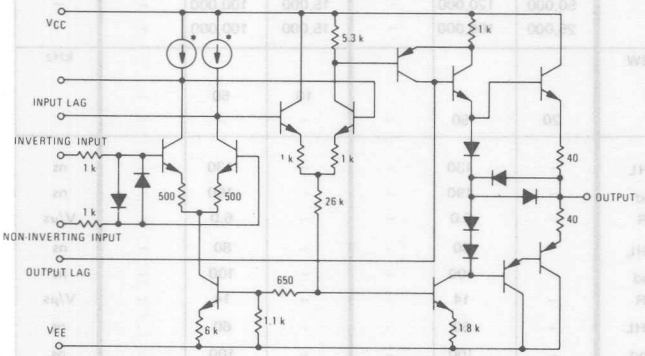


FIGURE 5 – EQUIVALENT CIRCUIT

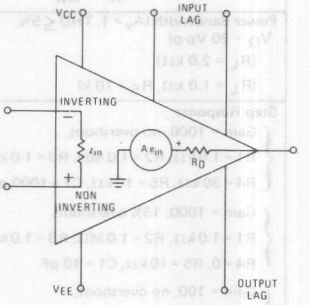
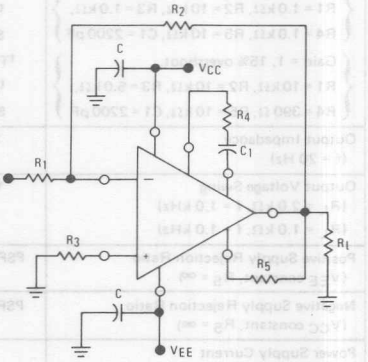


FIGURE 6 – TEST CIRCUIT



TYPICAL OUTPUT CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C

FIGURE NO.	CURVE NO.	VOLTAGE GAIN	TEST CONDITIONS (FIGURE 6) R_1 (Ω)	R_2 (Ω)	R_3 (Ω)	R_4 (Ω)	R_5 (Ω)	C_1 (pF)
7,10,12	1	A_{vol}	0	∞	0	∞	∞	0
	2	1	10 k	10 k	5.0 k	390	10 k	2200
	3	10	1.0 k	10 k	1.0 k	1.0 k	10 k	2200
	4	100	1.0 k	100 k	1.0 k	10 k	10 k	2200
	5	1000	1.0 k	1.0 M	1.0 k	30 k	10 k	1000
	6	1000	1.0 k	1.0 M	1.0 k	0	10 k	10
8	1	A_{vol}	0	∞	0	∞	∞	0
	2	↓	↓	↓	↓	390	↓	2200
	3					1.0 k		2200
	4					10 k		2200
	5					30 k		1000
	6					0		10
13	ALL	1	10 k	10 k	5.0 k	390	10 k	2200
14	ALL	10	1.0 k	10 k	1.0 k	1.0 k	10 k	2200
15	ALL	100	1.0 k	100 k	1.0 k	10 k	10 k	2200
16	ALL	1000	1.0 k	1.0 M	1.0 k	30 k	10 k	2200

TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C, unless otherwise noted.)

FIGURE 7 – LARGE-SIGNAL SWING versus FREQUENCY

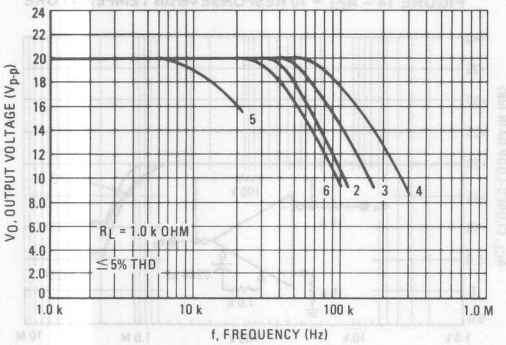


FIGURE 8 – OPEN-LOOP VOLTAGE GAIN versus FREQUENCY

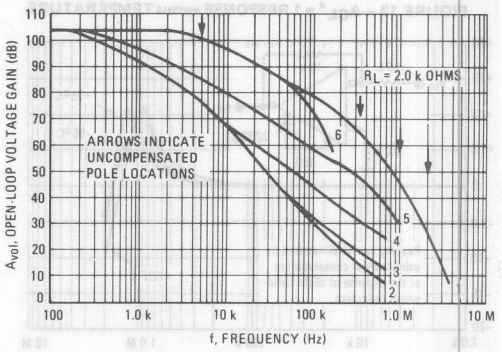


FIGURE 9 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

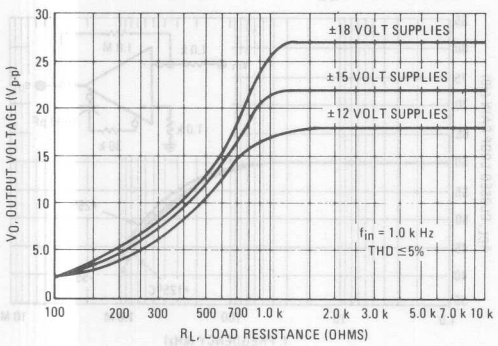


FIGURE 10 – OPEN-LOOP PHASE-SHIFT versus FREQUENCY

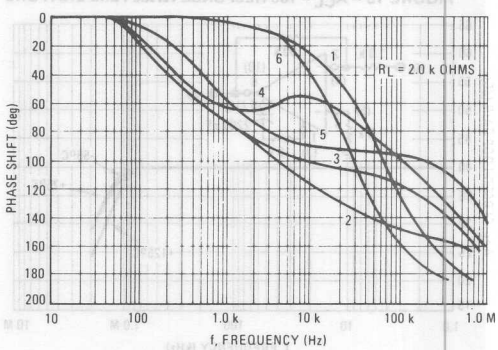


FIGURE 11 – OUTPUT VOLTAGE SWING (to clipping) versus SUPPLY

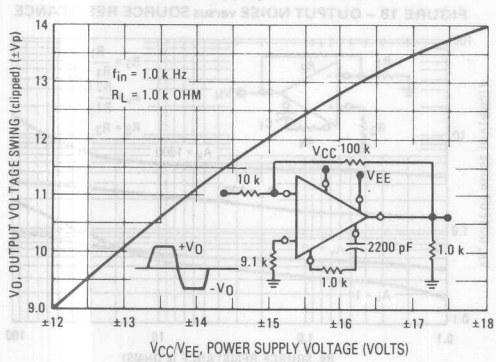
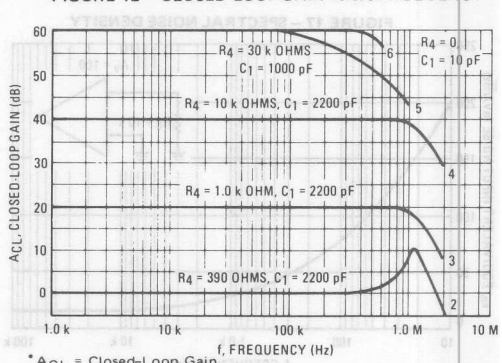


FIGURE 12 – CLOSED-LOOP GAIN versus FREQUENCY



*A_{CL} = Closed-Loop Gain

TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +15 Vdc, V_{EE} = −15 Vdc, T_A = +25°C, unless otherwise noted.)

FIGURE 13 – A_{CL}* = 1 RESPONSE versus TEMPERATURE

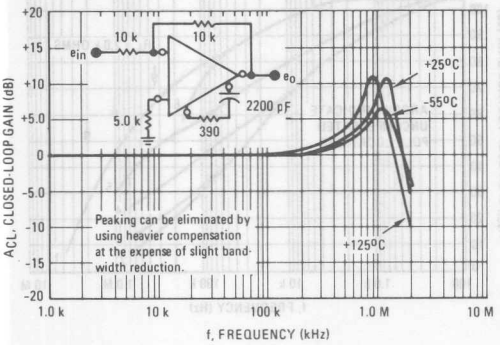


FIGURE 14 – A_{CL} = 10 RESPONSE versus TEMPERATURE

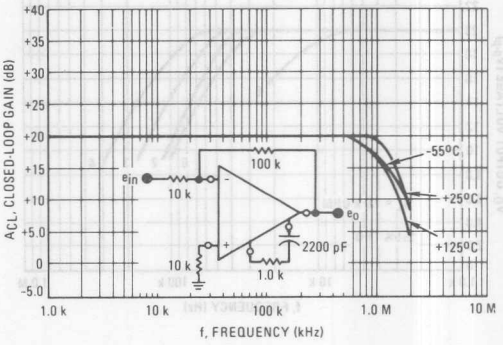


FIGURE 15 – A_{CL} = 100 RESPONSE versus TEMPERATURE

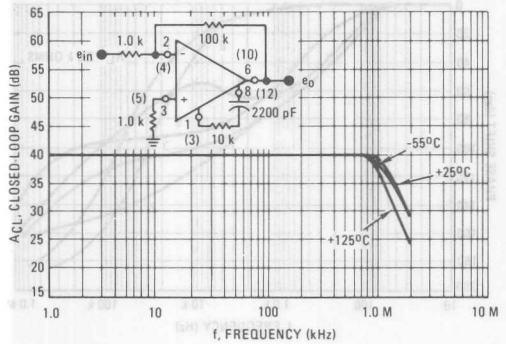


FIGURE 16 – A_{CL} = 1000 RESPONSE versus TEMPERATURE

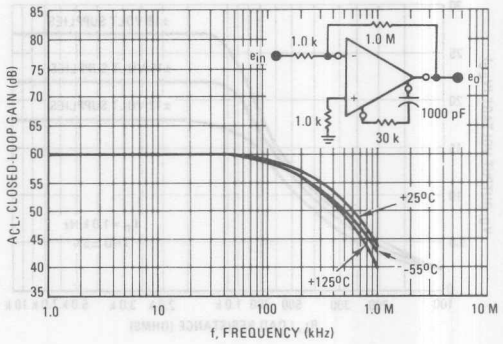
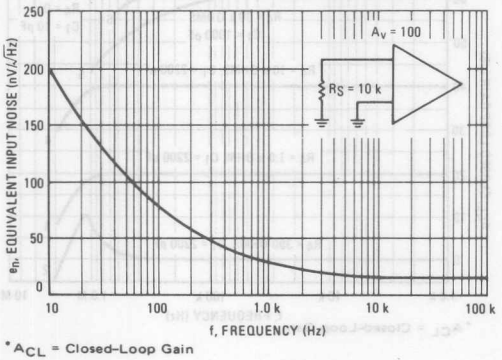
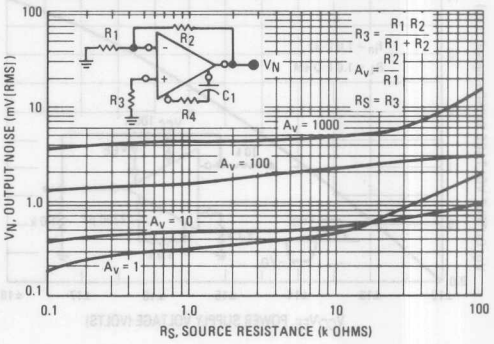


FIGURE 17 – SPECTRAL NOISE DENSITY



*A_{CL} = Closed-Loop Gain

FIGURE 18 – OUTPUT NOISE versus SOURCE RESISTANCE



TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C, unless otherwise noted.)

FIGURE 19 – POWER DISSIPATION versus TEMPERATURE

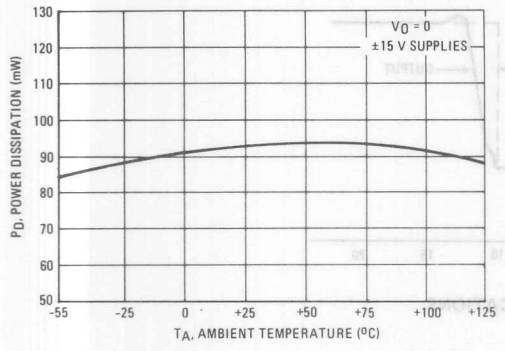


FIGURE 20 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE

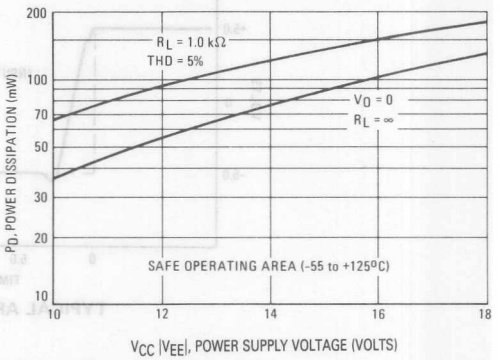


FIGURE 21 – POWER BANDWIDTH (LARGE-SIGNAL SWING versus FREQUENCY)

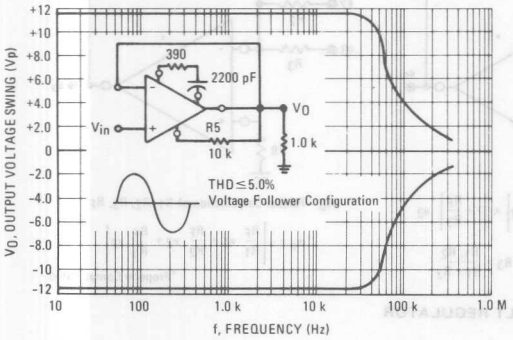


FIGURE 22 – COMMON-MODE INPUT VOLTAGE versus SUPPLY VOLTAGE

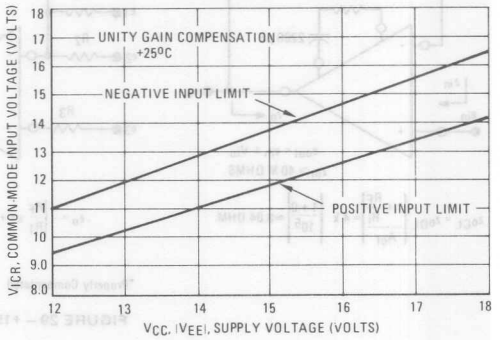


FIGURE 23 – COMMON-MODE REJECTION RATIO versus FREQUENCY

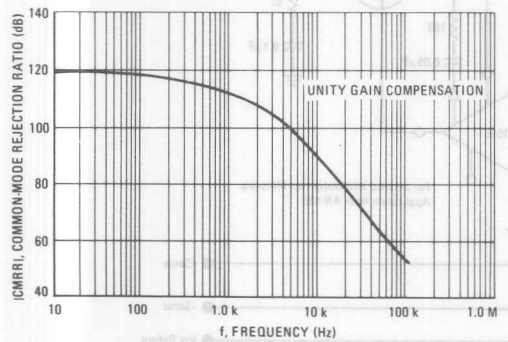
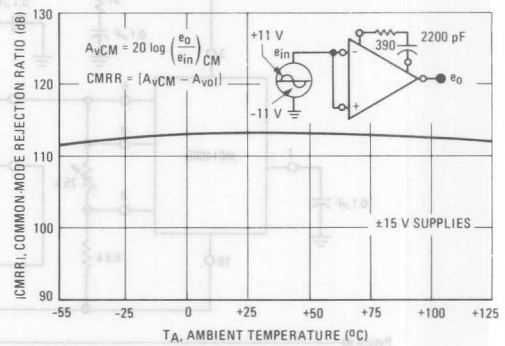
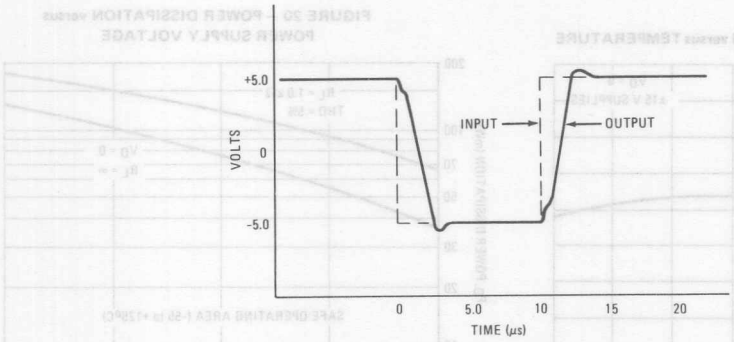


FIGURE 24 – COMMON-MODE REJECTION RATIO versus TEMPERATURE



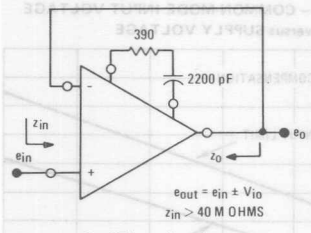
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FIGURE 25 – VOLTAGE-FOLLOWER PULSE RESPONSE



TYPICAL APPLICATIONS

FIGURE 26 – VOLTAGE FOLLOWER

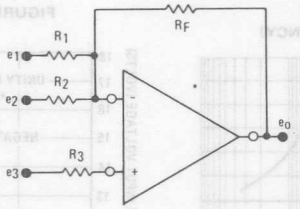


$e_{out} = e_{in} \pm V_{io}$

$z_{in} > 40$ M OHMS

$z_{OCL} = z_{OL}\left|\frac{1+\frac{R_F}{R_i}}{A_{ol}}\right| = 4\text{ k}\left|\frac{1+0}{10^5}\right| \approx 0.04$ OHM

FIGURE 27 – DIFFERENTIAL AMPLIFIER

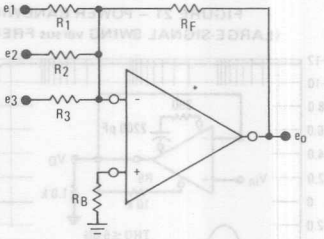


$e_o = -\left|\frac{R_F}{R_1}e_1 + \frac{R_F}{R_2}e_2\right| + \left|1+\frac{R_F}{R_3}\right| e_3$

For $R_3 = \frac{R_1 \cdot R_2}{R_1 + R_2}$

*Properly Compensated

FIGURE 28 – SUMMING AMPLIFIER

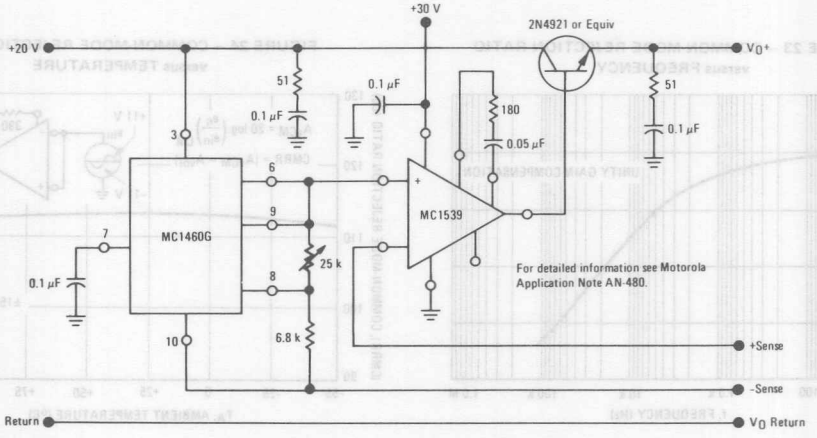


R_B = Parallel Combination of R_1, R_2, R_3, R_F.

$e_o = -\left|\frac{R_F}{R_1}e_1 + \frac{R_F}{R_2}e_2 + \frac{R_F}{R_3}e_3\right|$

*Properly Compensated

FIGURE 29 – +15 VOLT REGULATOR



TYPICAL APPLICATIONS (continued)

FIGURE 30 – LOAD REGULATION FOR CIRCUIT OF FIGURE 29

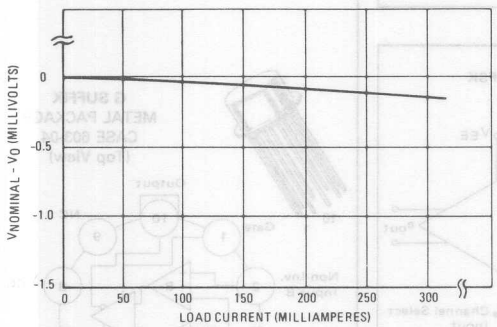
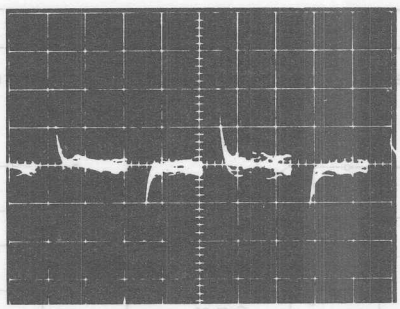


FIGURE 31 – REGULATOR OUTPUT VOLTAGE (under pulsed load condition)



MC1445G	0°C to +75°C	Metal Can
MC1445L	0°C to +75°C	Ceramic DIP
MC1545G	−55°C to +125°C	Metal Can
MC1545L	−55°C to +125°C	Ceramic DIP

MC1445
MC1545

GATE CONTROLLED TWO CHANNEL INPUT WIDEBAND AMPLIFIER

. . . designed for use as a general purpose gated wideband amplifier, video switch, sense amplifier, multiplexer, modulator, FSK circuit, limiter, AGC circuit, or pulse amplifier. See Application Notes AN491 for design details.

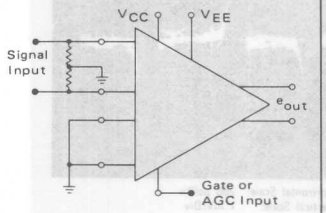
- Large Bandwidth; 50 MHz typical
- Channel-Select Time of 20 ns typical
- Differential Inputs and Differential Output

GATE CONTROLLED TWO CHANNEL INPUT WIDEBAND AMPLIFIER

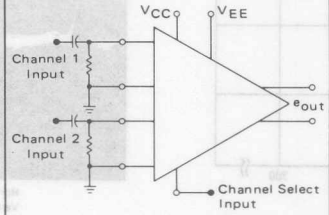
SILICON MONOLITHIC INTEGRATED CIRCUIT

TYPICAL APPLICATIONS

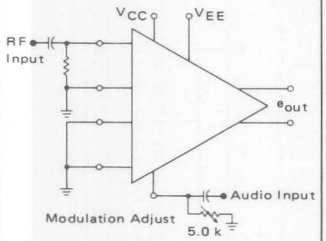
VIDEO SWITCH OR DIFFERENTIAL AMPLIFIER WITH AGC



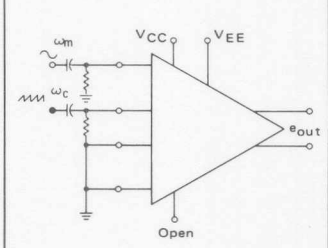
MULTIPLEX OR FSK



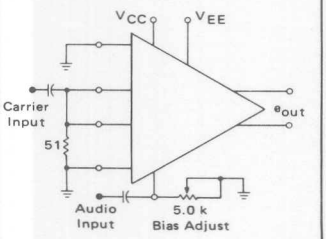
AMPLITUDE MODULATOR



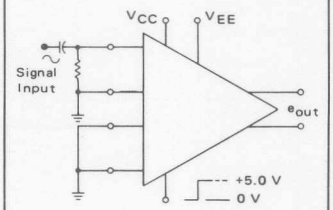
PULSE-WIDTH MODULATOR

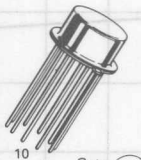


BALANCED MODULATOR

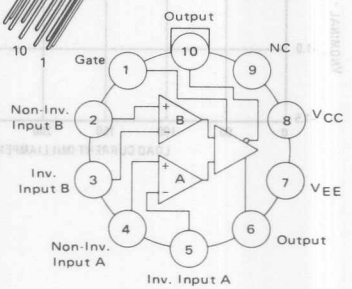


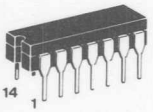
ANALOG SWITCH



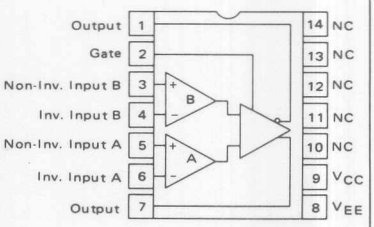


G SUFFIX
METAL PACKAGE
CASE 603-04
(Top View)





L SUFFIX
CERAMIC PACKAGE
CASE 632-08



(Top View)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+12 -12	Vdc Vdc
Input Differential Voltage Range	V_{IDR}	±5.0	Volts
Load Current	I_L	25	mA
Power Dissipation (Package Limitation)	P_D		
Ceramic Dual In-Line Package		625	mW
Derate above T_A = +25°C		5.0	mW/°C
Metal Can		680	mW
Derate above T_A = +25°C		4.6	mW/°C
Operating Ambient Temperature Range MC1445 MC1545	T_A	0 to +75 -55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = −5.0 Vdc, at T_A = +25°C, specifications apply to both input channels unless otherwise noted.)

Characteristic	Fig. No.	Symbol	MC1545 Min	MC1545 Typ	MC1545 Max	MC1445 Min	MC1445 Typ	MC1445 Max	Unit
Single-Ended Voltage Gain	1,12	A_{vs}	16	19	21	16	19.5	23	dB
Bandwidth	1,12	BW	40	50	–	–	50	–	MHz
Input Impedance (f = 50 kHz)	5,14	z_i	4.0	10	–	3.0	10	–	k ohms
Output Impedance (f = 50 kHz)	6,15	z_o	–	25	–	–	25	–	Ohms
Output Differential Voltage Range (R_L = 1.0 k ohm, f = 50 kHz)	4,13	V_{ODR}	1.5	2.5	–	1.5	2.5	–	Vp-p
Input Bias Current	16	I_{IB}	–	15	25	–	15	30	μAdc
Input Offset Current	16	I_{IO}	–	2.0	–	–	2.0	–	μAdc
Input Offset Voltage	17	V_{IO}	–	1.0	5.0	–	–	7.5	mVdc
Quiescent Output dc Level	17	V_O	–	0.1	–	–	0.1	–	Vdc
Output dc Level Change (Gate Input Voltage Change: +5.0 V to 0 V)	17	ΔV_O	–	±15	–	–	±15	–	mV
Common-Mode Rejection Ratio (f = 50 kHz)	9,18	CMRR	–	85	–	–	85	–	dB
Input Common-Mode Voltage Range	18	V_{ICR}	–	±2.5	–	–	±2.5	–	Vp
Gate Characteristics Gate Input Voltage – Low Logic State (Note 1)	8	$V_{IL(G)}$	0.40	0.70	–	0.2	0.4	–	Vdc
Gate Input Voltage – High Logic State (Note 2)		$V_{IH(G)}$	–	1.5	2.2	–	1.3	3.0	
Gate Input Current – Low Logic State ($V_{IL(G)}$ = 0 V)	18	$I_{IL(G)}$	–	–	2.5	–	–	4.0	mA
Gate Input Current – High Logic State ($V_{IH(G)}$ = +5.0 V)	18	$I_{IH(G)}$	–	–	2.0	–	–	4.0	μA
Step Response (e_{in} = 20 mV)	19	t_{PLH}	–	6.5	10	–	6.5	–	ns
		t_{PHL}	–	6.3	10	–	6.3	–	
		t_{TLH}	–	6.5	15	–	6.5	–	
		t_{THL}	–	7.0	15	–	7.0	–	
Wideband Input Noise (5.0 Hz – 10 MHz, R_S = 50 ohms)	10,20	e_n	–	25	–	–	25	–	μV(rms)
DC Power Consumption	11,20	P_C	–	70	110	–	70	150	mW

Note 1. $V_{IL(G)}$ is the gate voltage which results in channel A gain of unity or less and channel B gain of 16 dB or greater.
Note 2. $V_{IH(G)}$ is the gate voltage which results in channel B gain of unity or less and channel A gain of 16 dB or greater.

2

FIGURE 1 – SINGLE-ENDED VOLTAGE GAIN versus FREQUENCY

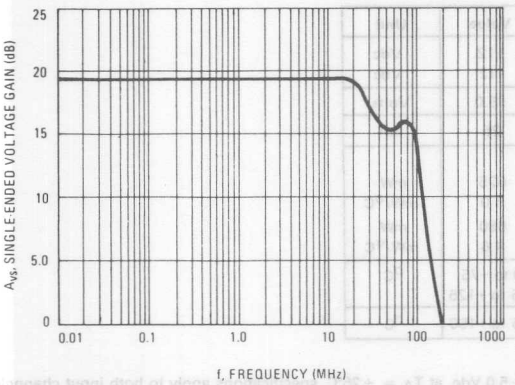


FIGURE 2 – SINGLE-ENDED VOLTAGE GAIN versus TEMPERATURE

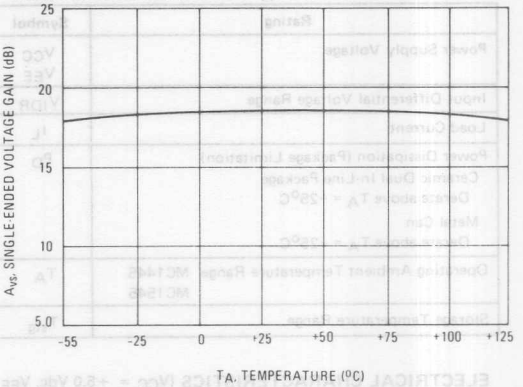


FIGURE 3 – VOLTAGE GAIN versus POWER SUPPLY VOLTAGES

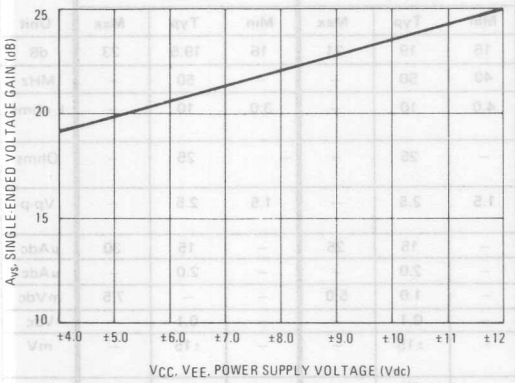


FIGURE 4 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE



FIGURE 5 – INPUT C_P AND R_P versus FREQUENCY (BOTH CHANNELS)

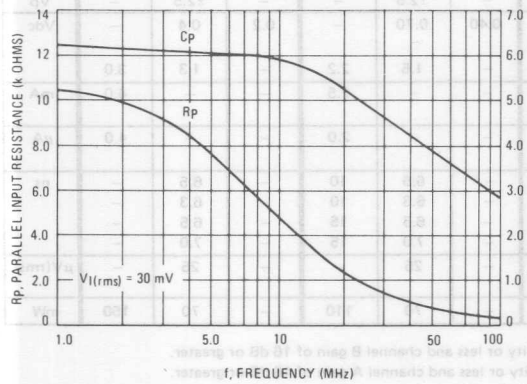


FIGURE 6 – OUTPUT IMPEDANCE versus FREQUENCY

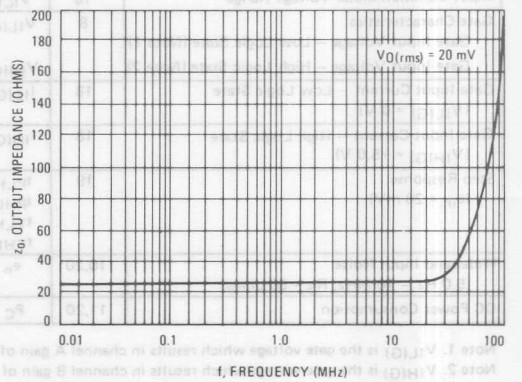


FIGURE 7 – CHANNEL SEPARATION versus FREQUENCY

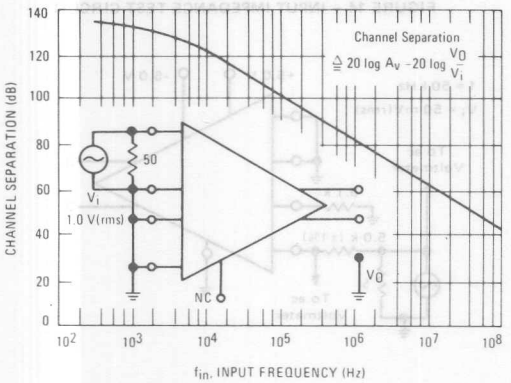


FIGURE 8 – GATE CHARACTERISTICS

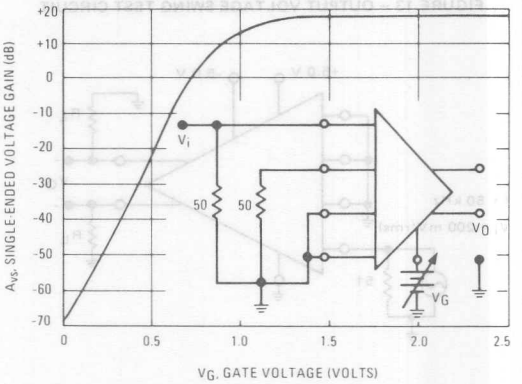


FIGURE 9 – COMMON MODE REJECTION RATIO versus FREQUENCY

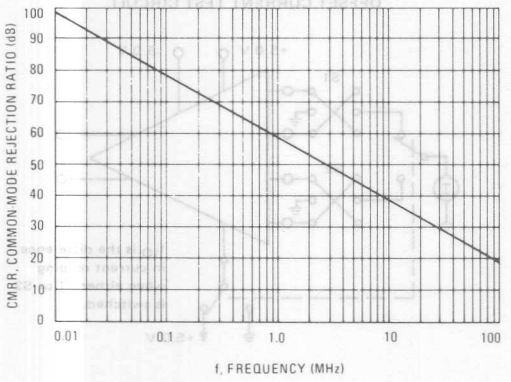


FIGURE 10 – INPUT WIDEBAND NOISE versus SOURCE RESISTANCE

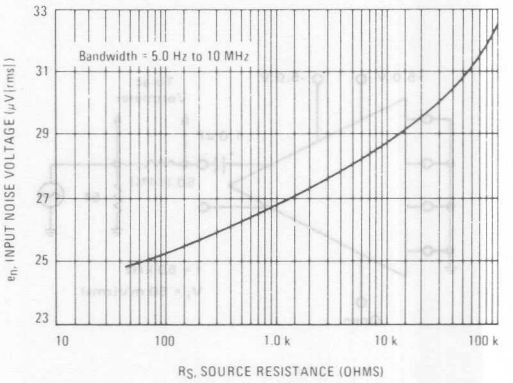


FIGURE 11 – CIRCUIT SCHEMATIC

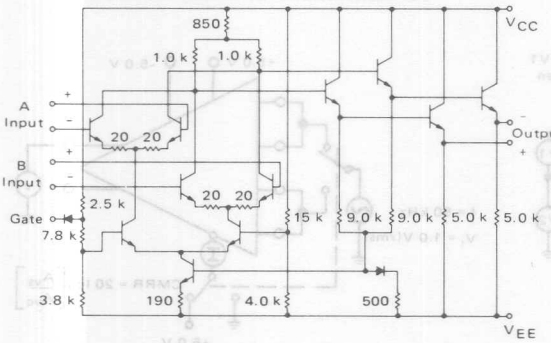


FIGURE 12 – SINGLE-ENDED VOLTAGE GAIN AND BANDWIDTH TEST CIRCUIT

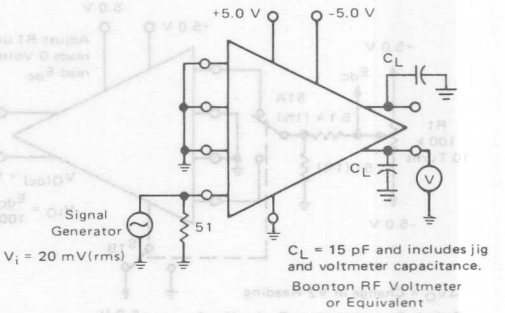


FIGURE 13 – OUTPUT VOLTAGE SWING TEST CIRCUIT

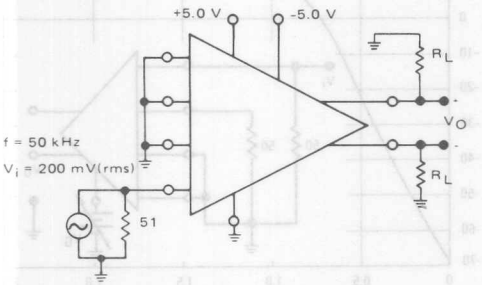


FIGURE 14 – INPUT IMPEDANCE TEST CIRCUIT

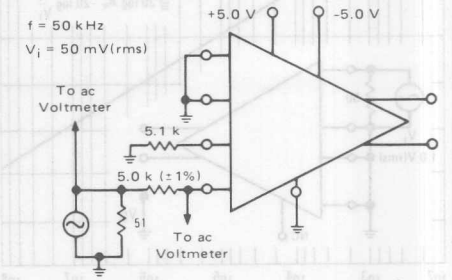


FIGURE 15 – OUTPUT IMPEDANCE TEST CIRCUIT

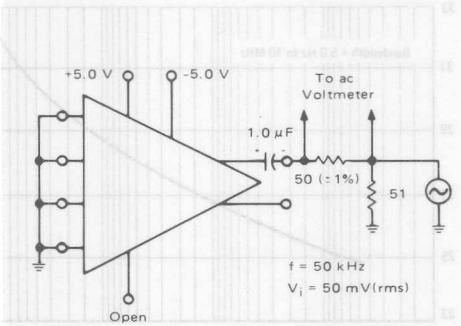


FIGURE 16 – INPUT BIAS CURRENT AND INPUT OFFSET CURRENT TEST CIRCUIT

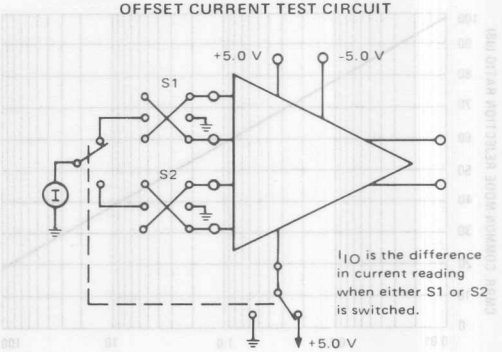


FIGURE 17 – INPUT OFFSET VOLTAGE AND QUIESCENT OUTPUT LEVEL TEST CIRCUIT

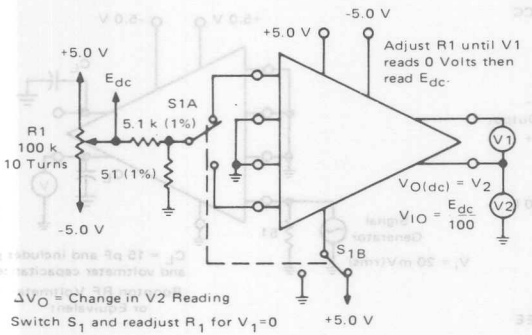
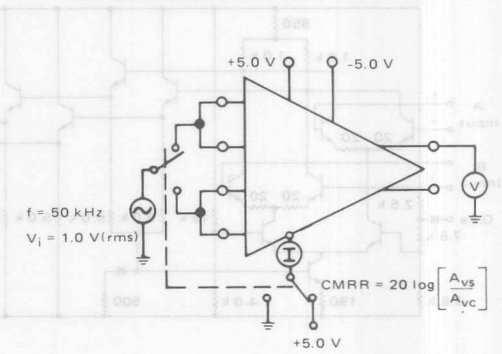
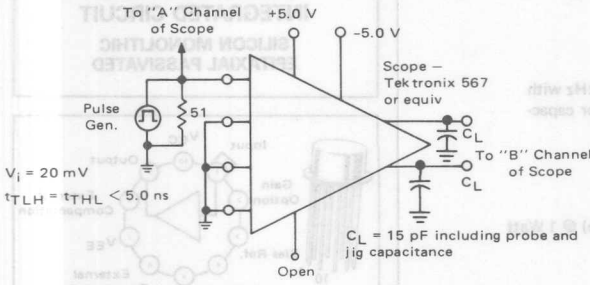


FIGURE 18 – GATE CURRENT (HIGH AND LOW), COMMON-MODE REJECTION AND COMMON-MODE INPUT RANGE TEST CIRCUIT



2

FIGURE 19 – PROPAGATION DELAY AND RISE AND FALL TIMES TEST CIRCUIT



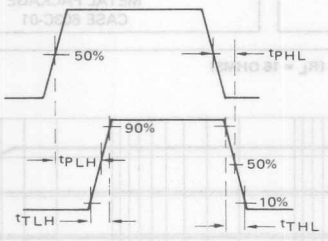


FIGURE 20 – POWER DISSIPATION AND WIDEBAND INPUT NOISE TEST CIRCUIT

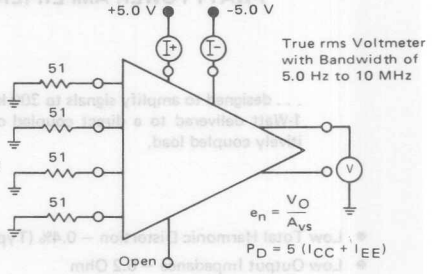
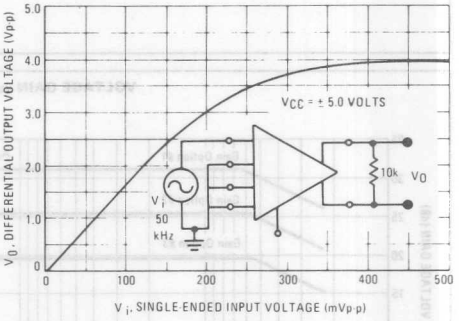


FIGURE 21 – LIMITING CHARACTERISTIC



ORDERING INFORMATION

Device	Temperature Range	Package
MC1454G	0°C to +70°C	Metal Can
MC1554G	−55°C to +125°C	Metal Can

MC1454G
MC1554G

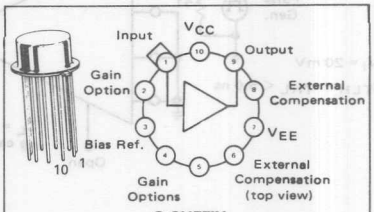
1-WATT POWER AMPLIFIERS

. . . designed to amplify signals to 300-kHz with 1-Watt delivered to a direct coupled or capacitively coupled load.

- Low Total Harmonic Distortion — 0.4% (Typ) @ 1 Watt
- Low Output Impedance — 0.2 Ohm
- Excellent Gain — Temperature Stability

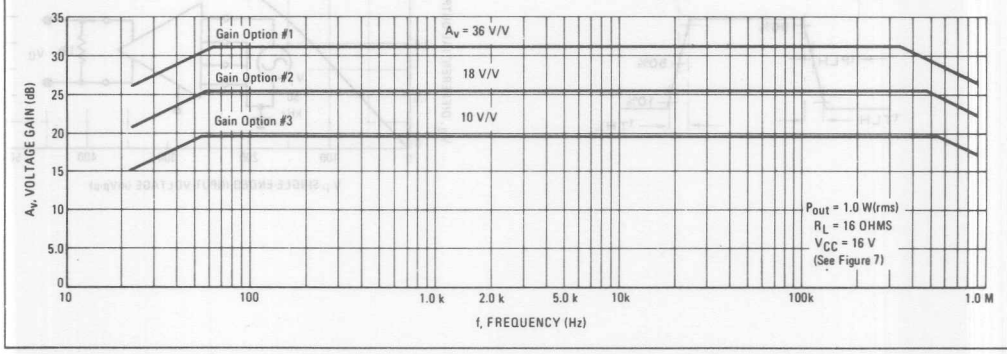
1-WATT POWER AMPLIFIER INTEGRATED CIRCUIT

SILICON MONOLITHIC EPITAXIAL PASSIVATED

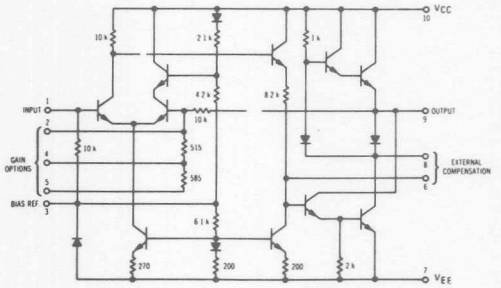


G SUFFIX
METAL PACKAGE
CASE 603C-01

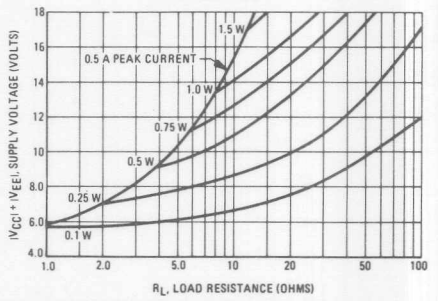
VOLTAGE GAIN versus FREQUENCY (R_L = 16 OHMS)



CIRCUIT SCHEMATIC



MAXIMUM AVAILABLE OUTPUT POWER (SINE WAVE)



ELECTRICAL CHARACTERISTICS (T_C = +25°C unless otherwise noted)
Frequency compensation shown in Figures 6 and 7.

Characteristic	Figure	R_L (Ohms)	Gain Option*	Symbol	MC1554 (-55 to +125°C) Min	MC1554 (-55 to +125°C) Typ	MC1554 (-55 to +125°C) Max	MC1454 (0 to +70°C) Min	MC1454 (0 to +70°C) Typ	MC1454 (0 to +70°C) Max	Unit
Output Power (for e_{out}<5.0% THD)	1	16	–	P_{out}	1.0	1.1	–	–	1.0	–	Watt
Power Dissipation (@ P_{out} = 1.0 W)	1	16	–	P_D	–	0.9	1.2	–	0.9	–	Watt
Voltage Gain	1	16	10	A_v	8.0	10	12	–	10	–	V/V
		16	18		–	18	–	–	18	–	
		16	36		–	36	–	–	36	–	
Input Impedance	1	–	10	z_{in}	7.0	10	–	3.0	10	–	kΩ
Output Impedance	1	–	10	z_o	–	0.2	–	–	0.4	–	Ω
Power Bandwidth (for e_{out}<5.0% THD)	2	16	10	BW	–	270	–	–	270	–	kHz
		16	18		–	250	–	–	250	–	
		16	36		–	210	–	–	210	–	
Total Harmonic Distortion (for e_{in}<0.05% THD, f = 20 Hz to 20 kHz)	2			THD							%
P_{out} = 1.0 Watt (sinewave)		16	10		–	0.4	–	–	0.4	–	
P_{out} = 0.1 Watt (sinewave)		16	10		–	0.5	–	–	0.5	–	
Zero Signal Current Drain	3	∞	–	I_D	–	11	15	–	11	20	mAdc
Output Noise Voltage	3	16	10	V_n	–	0.3	–	–	0.3	–	mV(rms)
Output Quiescent Voltage (Split Supply Operation)	4	16	–	V_o (dc)	–	±10	±30	–	±10	–	mVdc
Positive Supply Sensitivity (V_{EE} constant)	5	∞	–	S^+	–	-40	–	–	-40	–	mV/V
Negative Supply Sensitivity (V_{CC} constant)	5	∞	–	S^-	–	-40	–	–	-40	–	mV/V

*To obtain the voltage gain characteristic desired, use the following pin connections:

Voltage Gain	Pin Connection
10	Pins 2 and 4 open, Pin 5 to ac ground
18	Pins 2 and 5 open, Pin 4 to ac ground
36	Pin 2 connected to Pin 5, Pin 4 to ac ground

Characteristic Definitions
(Linear Operation)

FIGURE 1

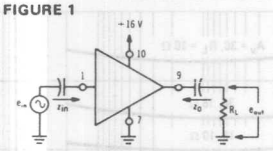


FIGURE 3

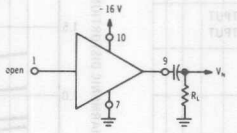


FIGURE 4

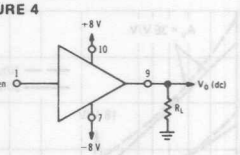
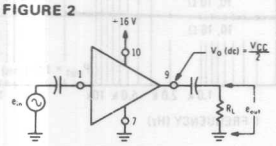


FIGURE 2



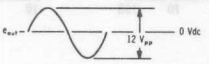
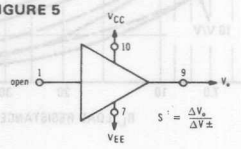


FIGURE 5



Rating		Symbol	Value	Unit
Total Power Supply Voltage		$\|V_{CC}\| + \|V_{EE}\|$	18	Vdc
Peak Load Current		I_{out}	0.5	Ampere
Audio Output Power		P_{out}	1.8	Watts
Power Dissipation (package limitation)				
$T_A = +25^oC$		P_D	600	mW
Derate above 25^oC		$1/\theta J_A$	4.8	$mW/^oC$
$T_C = +25^oC$		P_D	1.8	Watts
Derate above 25^oC		$1/\theta J_C$	14.4	$mW/^oC$
Operating Temperature Range	MC1454	T_A	0 to +70	^oC
	MC1554		-55 to +125	
Storage Temperature Range		T_{stg}	-55 to +150	^oC

TYPICAL CONNECTIONS

FIGURE 6 – SPLIT SUPPLY OPERATION VOLTAGE GAIN (A_V) = 10, $f_{LOW} \approx 25$ Hz

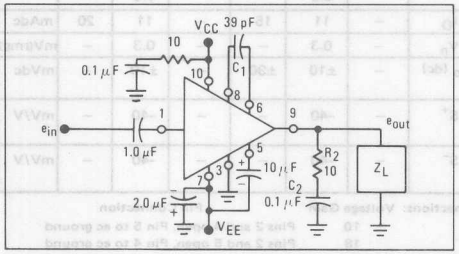
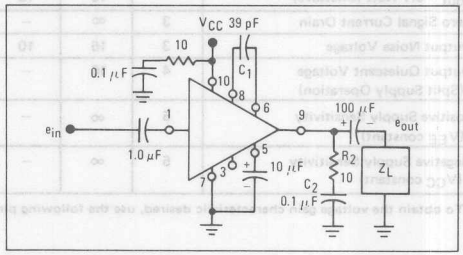


FIGURE 7 – SINGLE SUPPLY OPERATION VOLTAGE GAIN (A_V) = 10, $f_{LOW} \approx 100$ Hz



RECOMMENDED OPERATING CONDITIONS

In order to avoid local VHF instability, the following set of rules must be adhered to:

1. An R-C stabilizing network (0.1 μF in series with 10 ohms) should be placed directly from pin 9 to ground, as shown in Figures 6 and 7, using short leads, to eliminate local VHF instability caused by lead inductance to the load.
2. Excessive lead inductance from the V_{CC} supply to pin 10 can cause high frequency instability. To prevent this, the V_{CC} by-pass capacitor should be connected with short leads from the V_{CC} pin to ground. If this capacitor is remotely located a series R-C network (0.1 μF and 10 ohms) should be used directly from pin 10 to ground as shown in Figures 6 and 7.
3. Lead lengths from the external components to pins 7, 9, and 10 of the package should be as short as possible to insure good VHF grounding for these points.

Due to the large bandwidth of the amplifier, coupling must be avoided between the output and input leads. This can be assured by either (a) use of short leads which are well isolated, (b) narrow-banding the overall amplifier by placing a capacitor from pin 1 to ground to form a low-pass filter in combination with the source impedance, or (c) use of a shielded input cable. In applications which require upper band-edge control the input low-pass filter is recommended.

TYPICAL CHARACTERISTICS

FIGURE 8 – TOTAL HARMONIC DISTORTION versus LOAD RESISTANCE

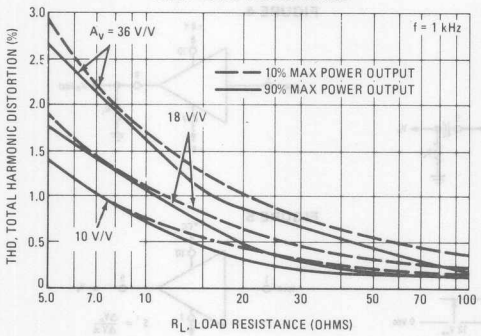
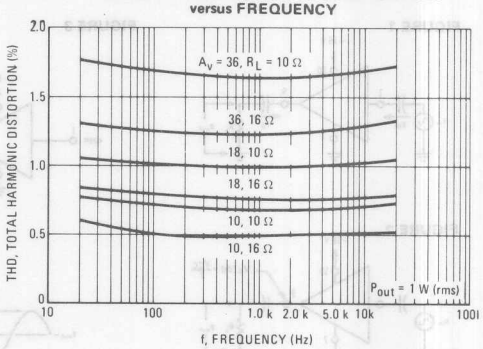


FIGURE 9 – TOTAL HARMONIC DISTORTION versus FREQUENCY



TYPICAL CHARACTERISTICS (continued)

FIGURE 10 – VOLTAGE GAIN versus TEMPERATURE

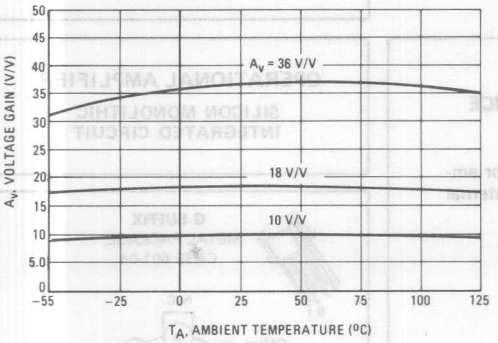


FIGURE 11 – OUTPUT VOLTAGE CHANGE

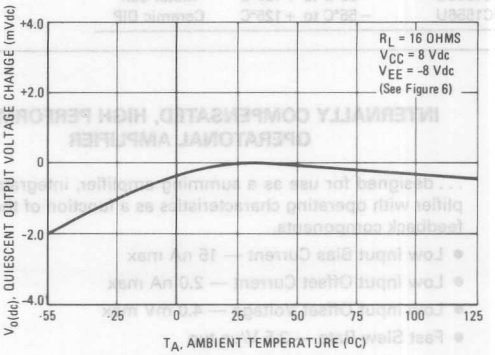


FIGURE 12 – VOLTAGE GAIN versus FREQUENCY ($R_L = \infty$)

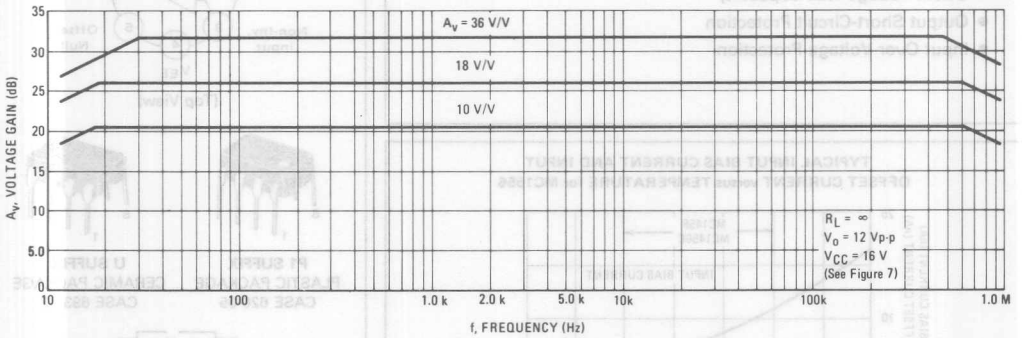
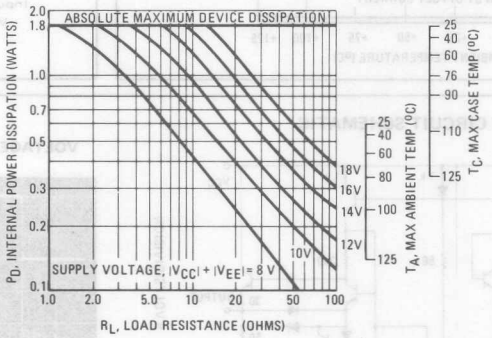


FIGURE 13 – MAXIMUM DEVICE DISSIPATION (SINE WAVE)



MC1456
MC1456C
MC1556

ORDERING INFORMATION

Device	Temperature Range	Package
MC1456G,CG	0°C to +70°C	Metal Can
MC1456CP1,P1	0°C to +70°C	Plastic DIP
MC1556G	−55°C to +125°C	Metal Can
MC1556U	−55°C to +125°C	Ceramic DIP

INTERNALLY COMPENSATED, HIGH PERFORMANCE OPERATONAL AMPLIFIER

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

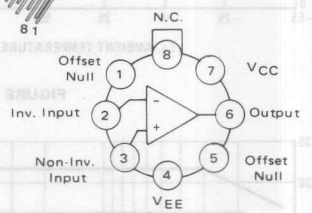
- Low Input Bias Current — 15 nA max
- Low Input Offset Current — 2.0 nA max
- Low Input Offset Voltage — 4.0 mV max
- Fast Slew Rate — 2.5 V/μs typ
- Large Power Bandwidth — 40 kHz typ
- Low Power Consumption — 45 mW max
- Offset Voltage Null Capability
- Output Short-Circuit Protection
- Input Over-Voltage Protection

OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT



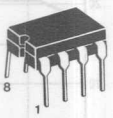
G SUFFIX
METAL PACKAGE
CASE 601-04



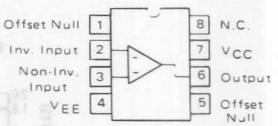
(Top View)



P1 SUFFIX
PLASTIC PACKAGE
CASE 626-05

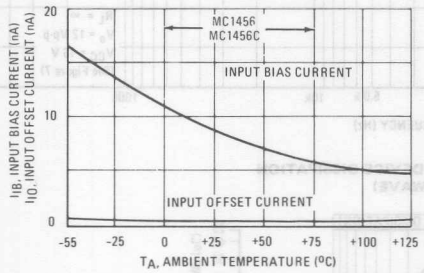


U SUFFIX
CERAMIC PACKAGE
CASE 693-02

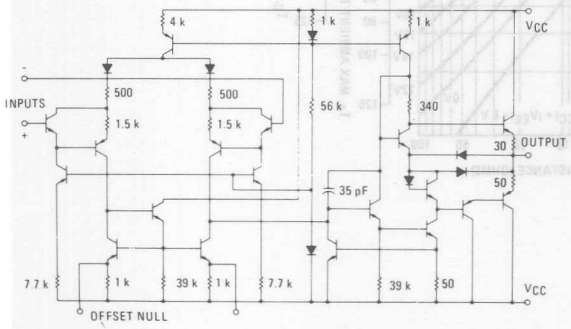


(Top View)

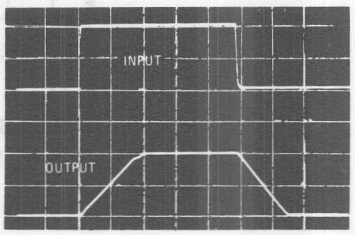
TYPICAL INPUT BIAS CURRENT AND INPUT OFFSET CURRENT versus TEMPERATURE for MC1556



REPRESENTATIVE CIRCUIT SCHEMATIC



VOLTAGE-FOLLOWER PULSE RESPONSE



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	MC1556	MC1456 MC1456C	Unit
Power Supply Voltage	V_{CC} V_{EE}	+22 -22	+18 -18	Vdc
Differential Input Voltage Range	V_{IDR}	±V_{CC}		Volts
Common-Mode Voltage Range	V_{ICR}	±V_{CC}		Volts
Load Current	I_L	20		mA
Output Short Circuit Duration	t_S	Continuous		
Power Dissipation (Package Limitation) Derate above T_A = +25°C	P_D	680 4.6		mW mW/°C
Operating Temperature Range	T_A	-55 to +125	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_{EE} = - 15 Vdc, T_A = +25°C unless otherwise noted).

Characteristic	Fig.	Symbol	MC1556 Min	MC1556 Typ	MC1556 Max	MC1456 Min	MC1456 Typ	MC1456 Max	MC1456C Min	MC1456C Typ	MC1456C Max	Unit
Input Bias Current		I_{IB}										nAdc
T_A = +25°C			–	8.0	15	–	15	30	–	15	90	
T_A = T_{low} to T_{high} (See Note 1)			–	–	30	–	–	40	–	–	–	
Input Offset Current		I_{IO}										nAdc
T_A = +25°C			–	1.0	2.0	–	5.0	10	–	5.0	30	
T_A = +25°C to T_{high}			–	–	3.0	–	–	14	–	–	–	
T_A = T_{low} to +25°C			–	–	5.0	–	–	14	–	–	–	
Input Offset Voltage		V_{IO}										mVdc
T_A = +25°C			–	2.0	4.0	–	5.0	10	–	5.0	12	
T_A = T_{low} to T_{high}			–	–	6.0	–	–	14	–	–	–	
Differential Input Impedance (Open-Loop, f = 20 Hz)												
Parallel Input Resistance		r_p	–	5.0	–	–	3.0	–	–	3.0	–	Megohms
Parallel Input Capacitance		c_p	–	6.0	–	–	6.0	–	–	6.0	–	pF
Common-Mode Input Impedance (f = 20 Hz)		z_i	–	250	–	–	250	–	–	250	–	Megohms
Common-Mode Input Voltage Range	1	V_{ICR}	±12	±13	–	+11	±12	–	±10.5	±12	–	V_{pk}
Equivalent Input Noise Voltage (A_V = 100, R_s = 10 k ohms, f = 1.0 kHz, BW = 1.0 Hz)	2	e_n	–	45			45	–	–	45	–	nV/(Hz)½
Common-Mode Rejection Ratio (f = 100 Hz)	3	CMRR	80	110	–	70	110	–	–	110	–	dB
Open-Loop Voltage Gain, (V_O = ± 10 V, R_L = 2.0 k ohms)	4,5,6	A_{VOL}										V/V
T_A = +25°C			100,000	200,000	–	70,000	100,000	–	25,000	100,000	–	
T_A = T_{low} to T_{high}			40,000	–	–	40,000	–	–	–	–	–	
Power Bandwidth (A_V = 1, R_L = 2.0 k ohms, THD≤5%, V_O = 20 Vp-p)	9	BW_P	–	40	–	–	40	–		40	–	kHz
Unity Gain Crossover Frequency (open-loop)	5	BW	–	1.0	–	–	1.0	–	–	1.0	–	MHz
Phase Margin (open-loop, unity gain)	5,7		–	70	–	–	70	–	–	70	–	degrees
Gain Margin	5,7		–	18	–	–	18	–	–	18	–	dB
Slew Rate (Unity Gain)		SR	–	2.5	–	–	2.5	–	–	2.5	–	V/μs
Output Impedance (f = 20 Hz)		z_o	–	1.0	2.0	–	1.0	2.5	–	1.0	–	kohms
Short-Circuit Output Current	8	I_{OS}	–	-17, +9.0	–	–	-17, +9.0	–	–	-17, +9.0	–	mAdc
Output Voltage Swing (R_L = 2.0 k ohms)	10	V_{OR}	±12	±13	–	+11	±12	–	±10	±12	–	V_{pk}
Power Supply Rejection Ratio												μV/V
V_{CC} = constant, R_S ≤ 10 k ohms		PSRR+		50	100	–	75	200	–	75	–	
V_{EE} = constant, R_S ≤ 10 k ohms		PSRR-		50	100	–	75	200	–	75	–	
Power Supply Current		I_{CC}	–	1.0	1.5	–	1.3	3.0	–	1.3	4.0	mAdc
		I_{EE}	–	1.0	1.5	–	1.3	3.0	–	1.3	4.0	
DC Quiescent Power Dissipation (V_O = 0)	11	P_D	–	30	45	–	40	90	–	40	120	mW

Note 1: T_{low}: 0° for MC1456 and MC1456C
-55°C for MC1556
T_{high}: +70°C for MC1456 and MC1456C
+125°C for MC1556

(V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted).

FIGURE 1 – INPUT COMMON-MODE SWING versus POWER SUPPLY VOLTAGE

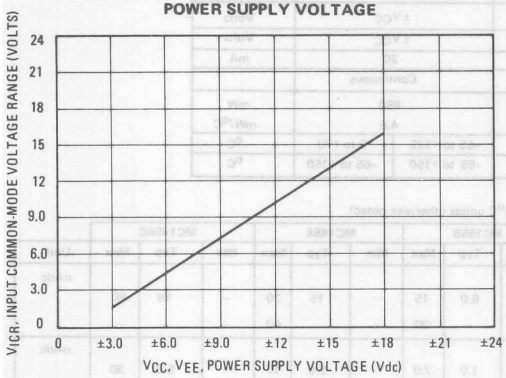


FIGURE 2 – SPECTRAL NOISE DENSITY

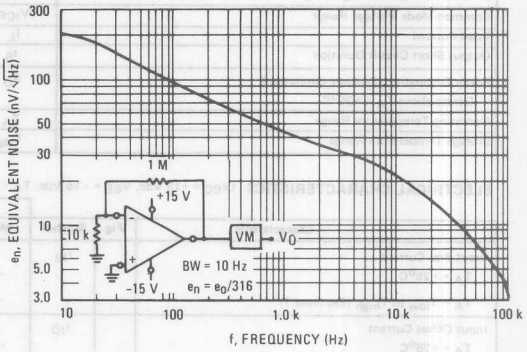


FIGURE 3 – COMMON-MODE REJECTION RATIO versus FREQUENCY

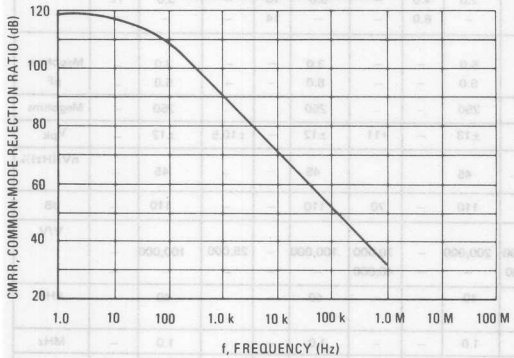


FIGURE 4 – OPEN-LOOP VOLTAGE GAIN versus TEMPERATURE

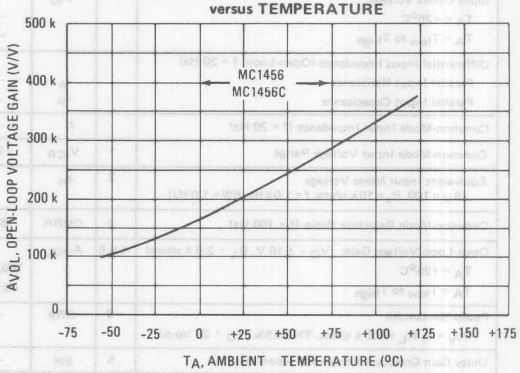


FIGURE 5 – OPEN-LOOP FREQUENCY RESPONSE

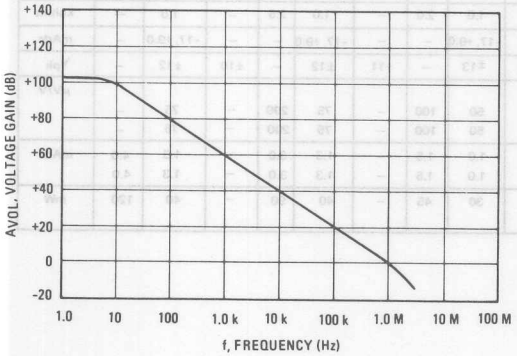
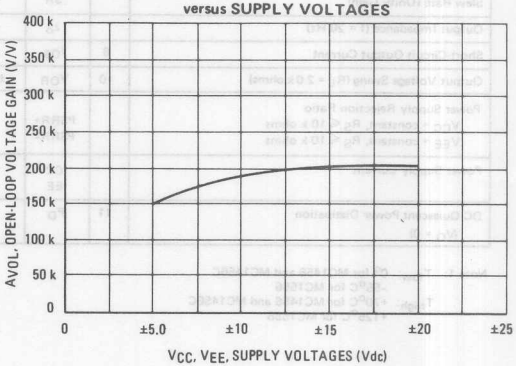


FIGURE 6 – OPEN-LOOP VOLTAGE GAIN versus SUPPLY VOLTAGES



TYPICAL CHARACTERISTICS (continued)

FIGURE 7 – OPEN-LOOP PHASE SHIFT

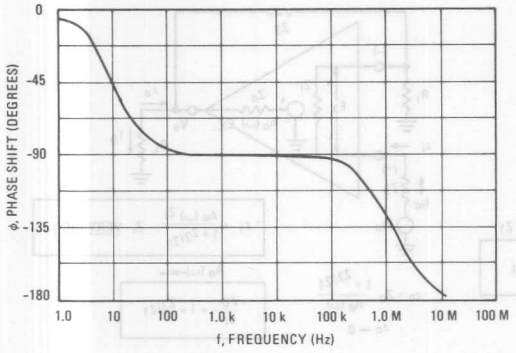


FIGURE 8 – OUTPUT SHORT-CIRCUIT CURRENT versus TEMPERATURE

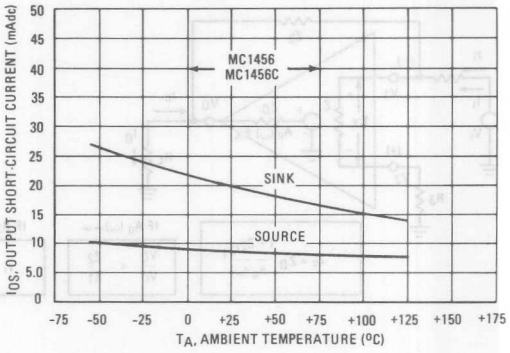


FIGURE 9 – POWER BANDWIDTH

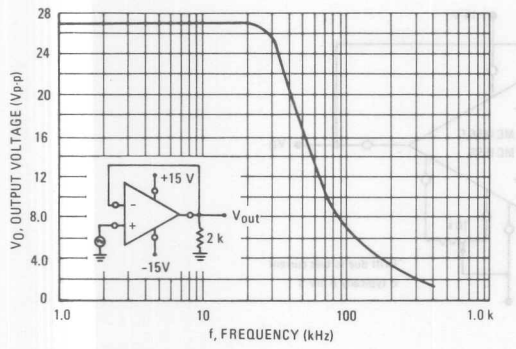


FIGURE 10 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

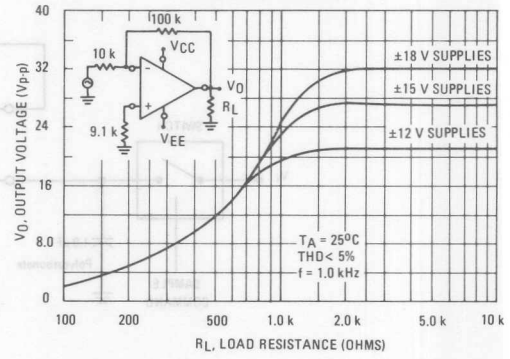
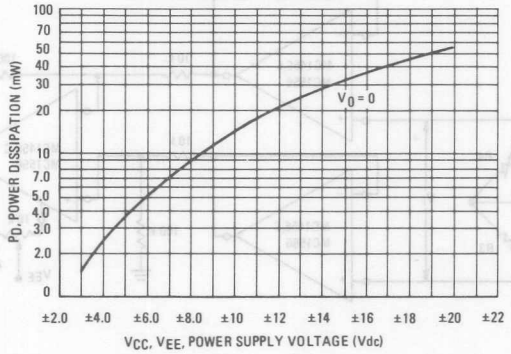


FIGURE 11 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE



2

TYPICAL APPLICATIONS

Where values are not given for external components they must be selected by the designer to fit the requirements of the system.

FIGURE 12 — INVERTING FEEDBACK MODEL

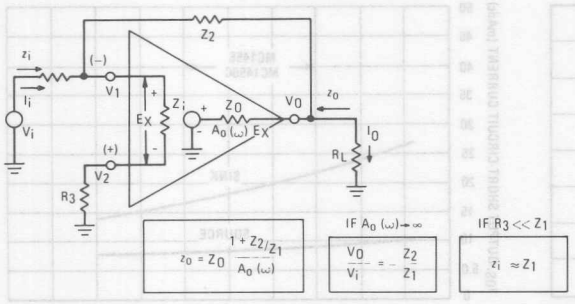


FIGURE 13 — NONINVERTING FEEDBACK MODEL

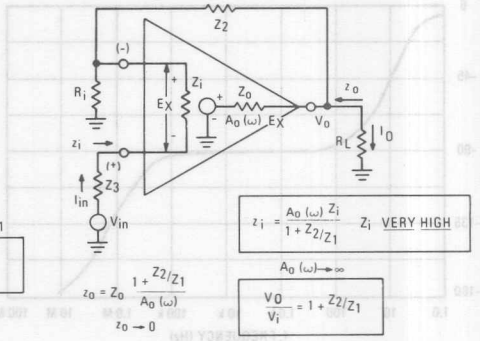


FIGURE 14 — LOW-DRIFT SAMPLE AND HOLD

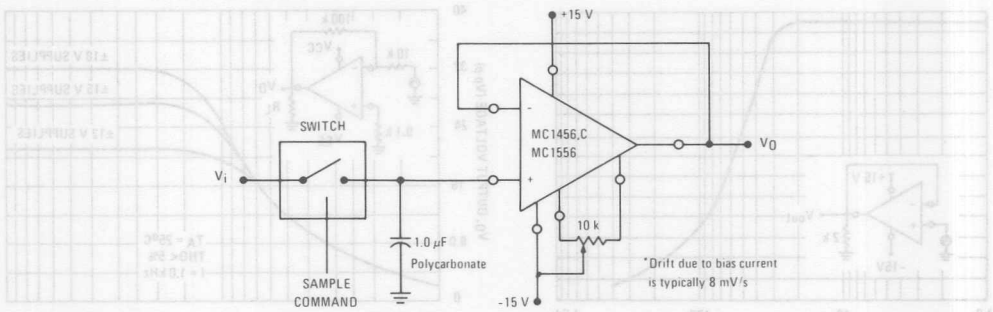
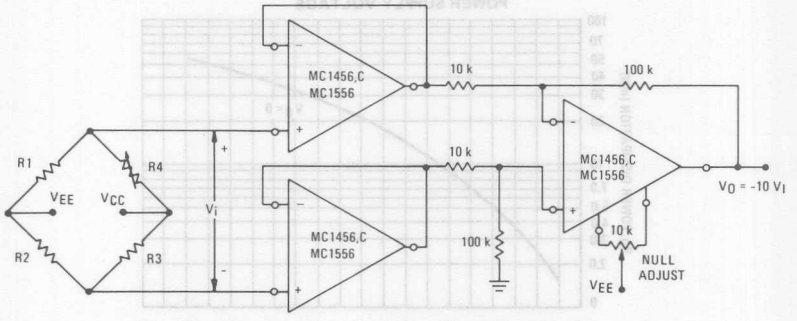


FIGURE 15 — HIGH IMPEDANCE BRIDGE AMPLIFIER



TYPICAL APPLICATIONS (continued)

FIGURE 16 – LOGARITHMIC AMPLIFIER

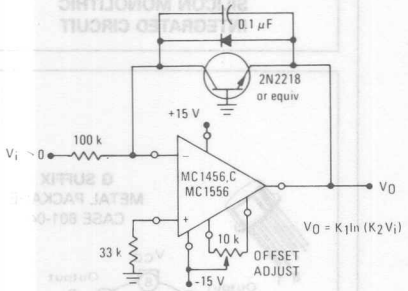
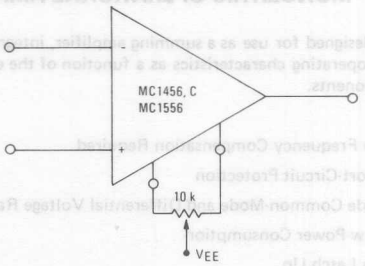


FIGURE 17 – VOLTAGE OFFSET NULL CIRCUIT



MC1558G	−55°C to +125°C	Metal Can
MC1458CU,U	0°C to +70°C	Ceramic DIP
MC1558U	−55°C to +125°C	Ceramic DIP
MC1458CP1,P1	0°C to +70°C	Plastic DIP

MC1558

(DUAL MC1741)
INTERNALLY COMPENSATED, HIGH PERFORMANCE MONOLITHIC OPERATIONAL AMPLIFIERS

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

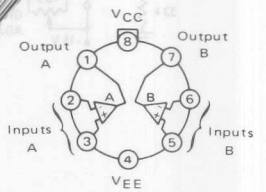
- No Frequency Compensation Required
- Short-Circuit Protection
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up

(DUAL MC1741)
DUAL OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT



G SUFFIX
METAL PACKAGE
CASE 601-04



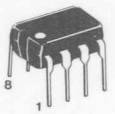
(Top View)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	MC1458	MC1558	Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 -18	+22 -22	Vdc Vdc
Input Differential Voltage	V_{ID}	±30		Volts
Input Common Mode Voltage (Note 1)	V_{ICM}	+15		Volts
Output Short Circuit Duration (Note 2)	t_S	Continuous		
Operating Ambient Temperature Range	T_A	0 to +70	-55 to +125	°C
Storage Temperature Range Metal and Ceramic Packages Plastic Package	T_{stg}	 -65 to +150 -55 to +125		°C
Junction Temperature Metal and Ceramic Packages Plastic Package	T_J	 175 150		°C

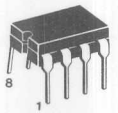
Note 1. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.

Note 2. Supply voltage equal to or less than 15 V.



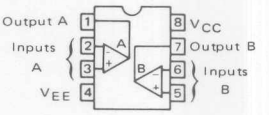
P1 SUFFIX
PLASTIC PACKAGE
CASE 626-05
(MC1458, MC1458C)

U SUFFIX
CERAMIC PACKAGE
CASE 693-02



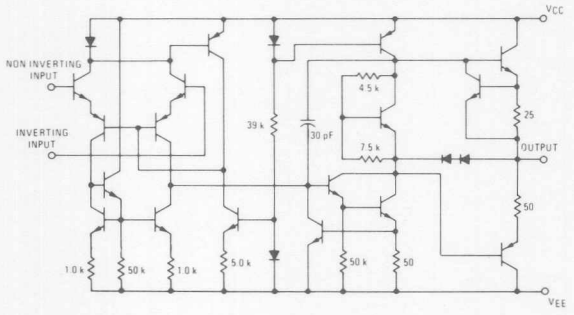


D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SO-8



(Top View)

EQUIVALENT CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS — Note 1. (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C unless otherwise noted).

Characteristic	Symbol	MC1558			MC1458			MC1458C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10$ k)	V_{IO}	–	1.0	5.0	–	2.0	6.0	–	2.0	10	mV
Input Offset Current	I_{IO}	–	20	200	–	20	200	–	20	300	nA
Input Bias Current	I_{IB}	–	80	500	–	80	500	–	80	700	nA
Input Resistance	r_i	0.3	2.0	–	0.3	2.0	–	–	2.0	–	MΩ
Input Capacitance	C_i	–	1.4	–	–	1.4	–	–	1.4	–	pF
Offset Voltage Adjustment Range	V_{IOR}	–	±15	–	–	±15	–	–	±15	–	mV
Common Mode Input Voltage Range	V_{ICR}	±12	±13	–	±12	±13	–	±11	±13	–	V
Large Signal Voltage Gain	A_v										V/mV
(V_O = ±10 V, R_L = 2.0 k)		50	200	–	20	200	–	–	–	–	
(V_O = ±10 V, R_L = 10 k)		–	–	–	–	–	–	20	200	–	
Output Resistance	r_o	–	75	–	–	75	–	–	75	–	Ω
Common Mode Rejection Ratio ($R_S \leq 10$ k)	CMRR	70	90	–	70	90	–	60	90	–	dB
Supply Voltage Rejection Ratio ($R_S \leq 10$ k)	PSRR	–	30	150	–	30	150	–	30	–	μV/V
Output Voltage Swing	V_O										V
($R_L \geq 10$ k)		±12	±14	–	±12	±14	–	±11	±14	–	
($R_L \geq 2$ k)		±10	±13	–	±10	±13	–	±9.0	±13	–	
Output Short-Circuit Current	I_{os}	–	20	–	–	20	–	–	20	–	mA
Supply Currents (Both Amplifiers)	I_D	–	2.3	5.0	–	2.3	5.6	–	2.3	8.0	mA
Power Consumption	P_C	–	70	150	–	70	170	–	70	240	mW
Transient Response (Unity Gain)											
(V_I = 20 mV, $R_L \geq 2$ kΩ, $C_L \leq 100$ pF) Rise Time	t_{TLH}	–	0.3	–	–	0.3	–	–	0.3	–	μs
(V_I = 20 mV, $R_L \geq 2$ kΩ, $C_L \leq 100$ pF) Overshoot	os	–	15	–	–	15	–	–	15	–	%
(V_I = 10 V, $R_L \geq 2$ kΩ, $C_L \leq 100$ pF) Slew Rate	SR	–	0.5	–	–	0.5	–	–	0.5	–	V/μs

ELECTRICAL CHARACTERISTICS Note 1 (V_{CC} = +15 V, V_{EE} = −15 V, T_A = *T_{high} to T_{low} unless otherwise noted).

Characteristic	Symbol	MC1558			MC1458			MC1458C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10$ kΩ)	V_{IO}	–	1.0	6.0	–	–	7.5	–	–	12	mV
Input Offset Current	I_{IO}										nA
(T_A = 125°C)			7.0	200	–	–	–	–	–	–	
(T_A = −55°C)		–	85	500	–	–	–	–	–	–	
(T_A = 0°C to +70°C)		–	–	–	–	–	300	–	–	400	
Input Bias Current	I_{IB}										nA
(T_A = 125°C)		–	30	500	–	–	–	–	–	–	
(T_A = −55°C)		–	300	1500	–	–	–	–	–	–	
(T_A = 0°C to +70°C)		–	–	–	–	–	800	–	–	1000	
Common Mode Input Voltage Range	V_{ICR}	±12	±13	–	–	–	–	–	–	–	V
Common Mode Rejection Ratio ($R_S \leq 10$ k)	CMRR	70	90	–	–	–	–	–	–	–	dB
Supply Voltage Rejection Ratio ($R_S \leq 10$ k)	PSRR	–	30	150	–	–	–	–	–	–	μV/V
Output Voltage Swing	V_O										V
($R_L \geq 10$ k)		±12	±14	–	±12	±14	–	–	–	–	
($R_L \geq 2$ k)		±10	±13	–	±10	±13	–	±9.0	±13	–	
Large Signal Voltage Gain	A_v										V/mV
(V_O = ±10 V, R_L = 2 k)		25	–	–	15	–	–	–	–	–	
(V_O = ±10 V, R_L = 10 k)		–	–	–	–	–	–	15	–	–	
Supply Currents (Both Amplifiers)	I_D										mA
(T_A = 125°C)		–	–	4.5	–	–	–	–	–	–	
(T_A = −55°C)		–	–	6.0	–	–	–	–	–	–	
Power Consumption (T_A = 125°C)	P_C	–	–	135	–	–	–	–	–	–	mW
(T_A = −55°C)		–	–	180	–	–	–	–	–	–	

*T_{high} = 125°C for MC1558 and 70°C for MC1458, MC1458C
T_{low} = −55°C for MC1558 and 0°C for MC1458, MC1458C

Note 1. Input pins of an unused amplifier must be grounded for split supply operation or biased at least 3.0 V above V_{EE} for single supply operation.

2

FIGURE 1 – BURST NOISE versus SOURCE RESISTANCE

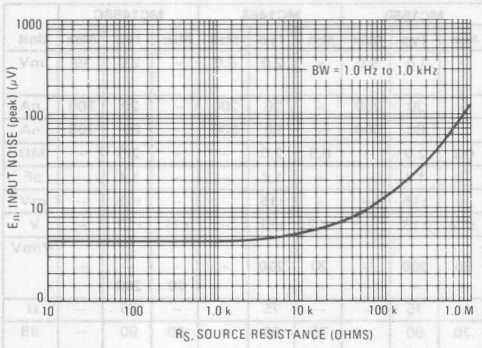


FIGURE 2 – RMS NOISE versus SOURCE RESISTANCE

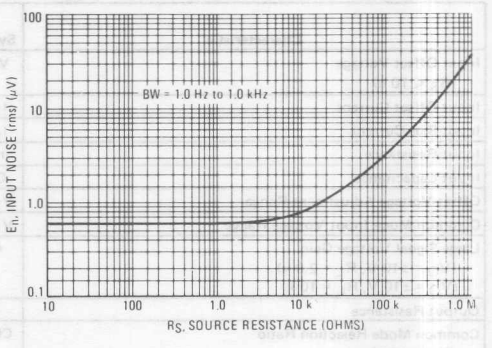


FIGURE 3 – OUTPUT NOISE versus SOURCE RESISTANCE

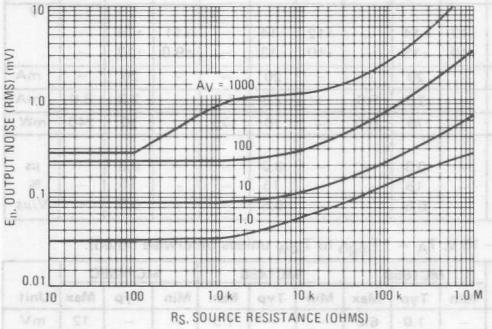


FIGURE 4 – SPECTRAL NOISE DENSITY

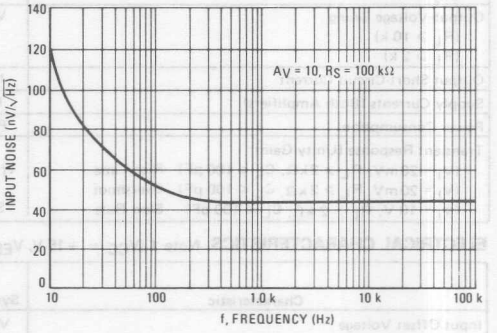
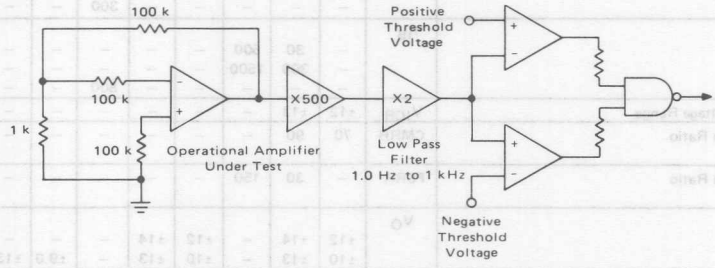


FIGURE 5 – BURST NOISE TEST CIRCUIT



Unlike conventional peak reading or RMS meters, this system was especially designed to provide the quick response time essential to burst (popcorn) noise testing.

The test time employed is 10 seconds and the 20 μV peak limit refers to the operational amplifier input thus eliminating errors in the closed-loop gain factor of the operational amplifier under test.

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted).

FIGURE 6 – POWER BANDWIDTH
(LARGE SIGNAL SWING versus FREQUENCY)

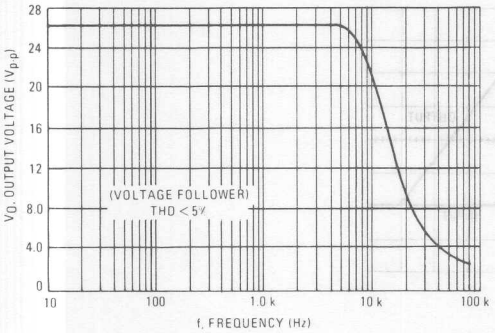


FIGURE 7 – OPEN LOOP FREQUENCY RESPONSE

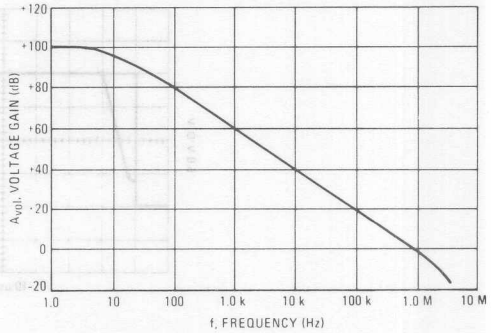


FIGURE 8 – POSITIVE OUTPUT VOLTAGE SWING
versus LOAD RESISTANCE

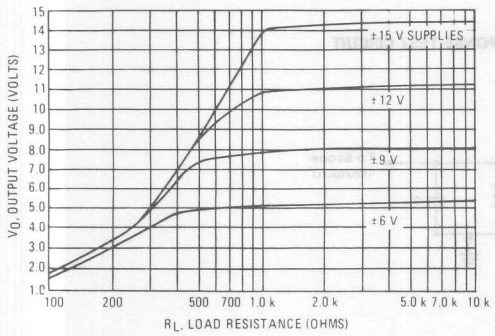


FIGURE 9 – NEGATIVE OUTPUT VOLTAGE SWING
versus LOAD RESISTANCE

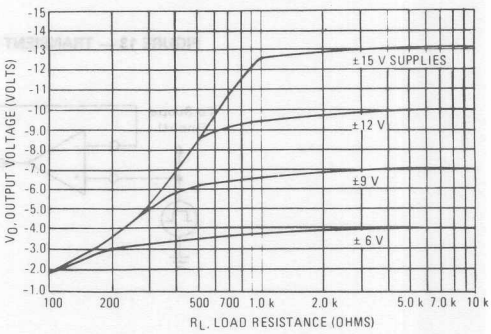


FIGURE 10 – OUTPUT VOLTAGE SWING versus
LOAD RESISTANCE (Single Supply Operation)

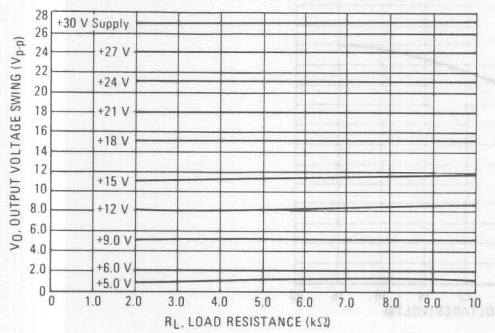


FIGURE 11 – SINGLE SUPPLY INVERTING AMPLIFIER

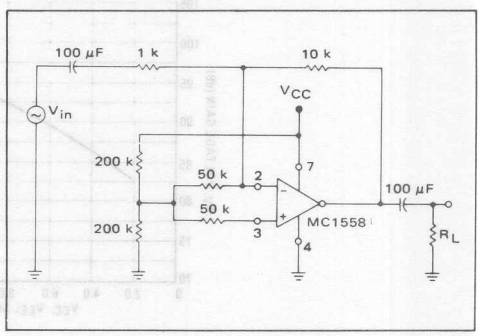


FIGURE 12 — NONINVERTING PULSE RESPONSE

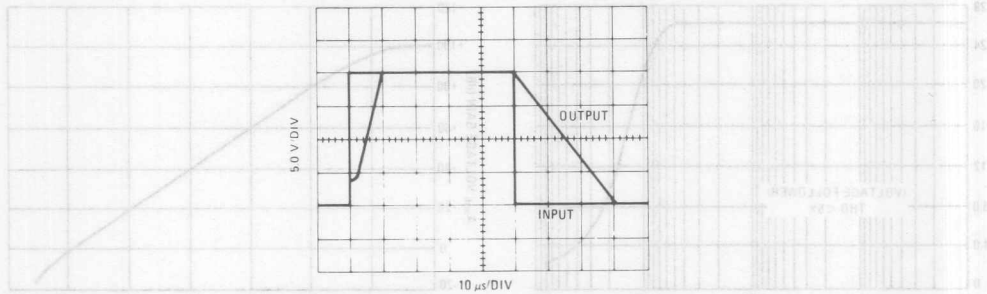


FIGURE 13 — TRANSIENT RESPONSE TEST CIRCUIT

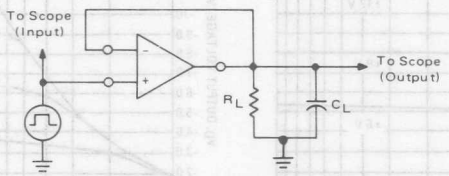
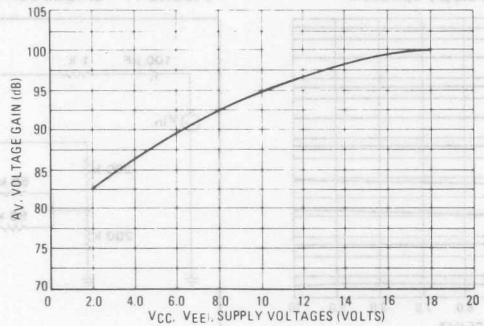


FIGURE 14 — OPEN LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE



MC1458S
MC1558S

ORDERING INFORMATION

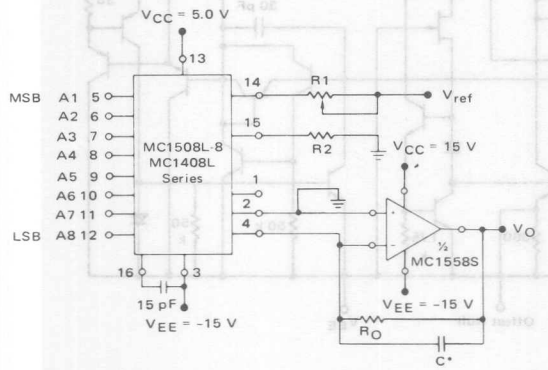
Device	Temperature Range	Package
MC1458SD	0°C to +70°C	SO-8
MC1458SG	0°C to +70°C	Metal Can
MC1458SP1	0°C to +70°C	Plastic DIP
MC1458SU	0°C to +70°C	Ceramic DIP
MC1558SG	−55°C to +125°C	Metal Can
MC1558SU	−55°C to +125°C	Ceramic DIP

DUAL HIGH SLEW RATE INTERNALLY-COMPENSATED OPERATIONAL AMPLIFIERS

The MC1558S is functionally equivalent, pin compatible, and possesses the same ease of use as the popular MC1558 circuit, yet offers 20 times higher slew rate and power bandwidth. This device is ideally suited for D/A converters due to its fast settling time and high slew rate.

- High Slew Rate — 10 V/μs Guaranteed Minimum (for inverting unity gain only)
- No Frequency Compensation Required
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low Power Consumption
- No Latch-Up

TYPICAL APPLICATION OUTPUT CURRENT TO VOLTAGE TRANSFORMATION FOR A D-TO-A CONVERTER



Settling time to within 1/2 LSB (±19.5 mV) is approximately 4.0 μs from the time that all bits are switched.

*The value of C may be selected to minimize overshoot and ringing (C ≈ 68 pF).

Theoretical V_O

$$V_O = \frac{V_{ref}}{R1}(R_O)\left[\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right]$$

Adjust V_{ref}, R1 or R_O so that V_O with all digital inputs at high level is equal to 9.961 volts.

V_{ref} = 2.0 Vdc
R1 = R2 ≅ 1.0 kΩ
R_O = 5.0 kΩ

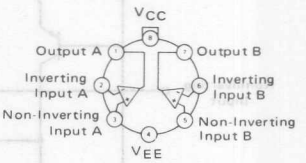
$$V_O = \frac{2\ V}{1\ k}(5\ k)\left[\frac{1}{2}+\frac{1}{4}+\frac{1}{8}+\frac{1}{16}+\frac{1}{32}+\frac{1}{64}+\frac{1}{128}+\frac{1}{256}\right] = 10\ V\left[\frac{255}{256}\right] = 9.961\ V$$

DUAL OPERATIONAL AMPLIFIERS

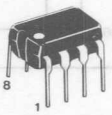
SILICON MONOLITHIC INTEGRATED CIRCUIT



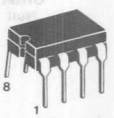
G SUFFIX
METAL PACKAGE
CASE 601-04



(Top View)



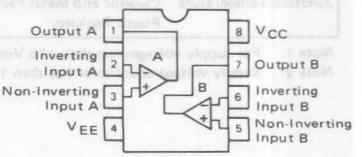
P1 SUFFIX
PLASTIC PACKAGE
CASE 626-05
(MC1458S Only)



U SUFFIX
CERAMIC PACKAGE
CASE 693-02



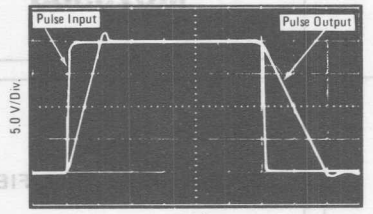
D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SO-8
(MC1458S Only)



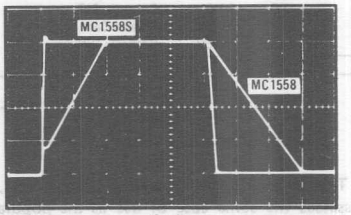
(Top View)

2

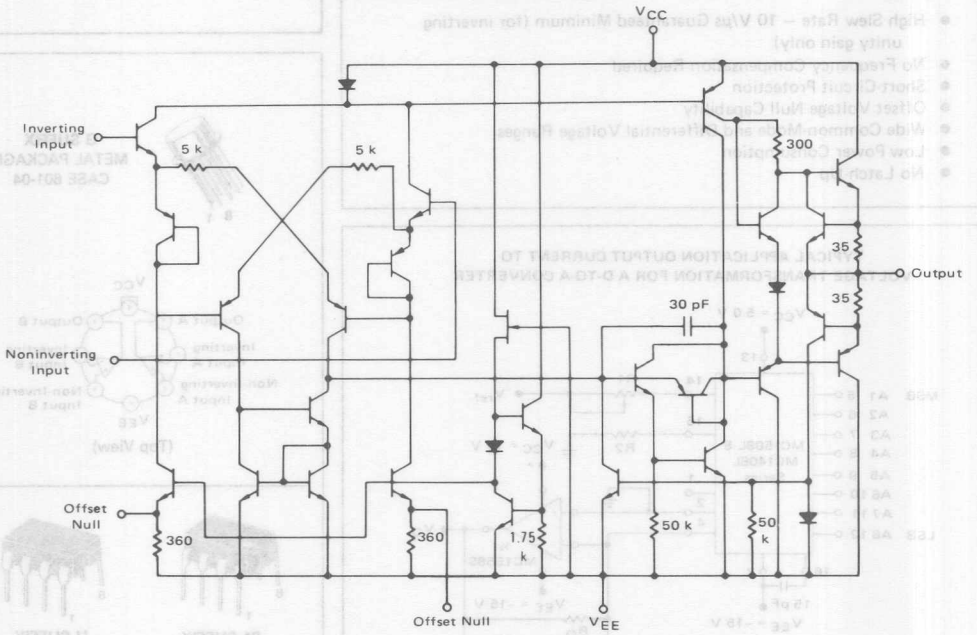
MC1558S LARGE-SIGNAL TRANSIENT RESPONSE
(Inverting Mode)



STANDARD MC1558 versus MC1558S RESPONSE COMPARISON
(Inverting Mode)



½ REPRESENTATIVE CIRCUIT SCHEMATIC



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	MC1558S	MC1458S	Unit
Power Supply Voltage	V_{CC} V_{EE}	+22 -22	+18 -18	Vdc
Input Differential Voltage Range (1)	V_{IDR}	±30		Volts
Input Common-Mode Voltage Range (2)	V_{ICR}	±15		Volts
Output Short Circuit Duration	t_S	Continuous		
Operating Ambient Temperature Range	T_A	-55 to +125	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	°C
Junction Temperature Ceramic and Metal Package Plastic Package	T_J	175 150	175 150	°C °C

Note 1. For supply voltages less than ±15 Vdc, the absolute maximum input voltage is equal to the supply voltage.
Note 2. Supply voltage equal to or less than 15 Vdc.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC1558S Min	MC1558S Typ	MC1558S Max	MC1458S Min	MC1458S Typ	MC1458S Max	Unit
Power Bandwidth (See Figure 3) A_v = 1, R_L = 2.0 kΩ, THD = 5%, V_O = 20 V(p-p)	BW_P	150	200	–	150	200	–	kHz
Large-Signal Transient Response Slew Rate (Figures 10 and 11) V(–) to V(+) V(+) to V(–) Settling Time (Figures 10 and 11) (to within 0.1%)	SR t_{setlg}	 10 10 –	 20 12 3.0	 – – –	 10 10 –	 20 12 3.0	 – – –	 V/μs μs
Small-Signal Transient Response (Gain = 1, E_{in} = 20 mV, see Figures 7 and 8) Rise Time Fall Time Propagation Delay Time Overshoot	 t_{TLH} t_{THL} t_{PLH},t_{PHL} OS	 – – – –	 0.25 0.25 0.25 20	 – – – –	 – – – –	 0.25 0.25 0.25 20	 – – – –	 μs μs μs %
Short-Circuit Output Currents	I_{OS}	±10	–	±45	±10	–	±45	mA
Open-Loop Voltage Gain (R_L = 2.0 kΩ) (See Figure 4) V_O = ±10 V	A_{VOL}	50,000	200,000	–	20,000	100,000	–	–
Output Impedance (f = 20 Hz)	z_o	–	75	–	–	75	–	Ω
Input Impedance (f = 20 Hz)	z_i	0.3	1.0	–	0.3	1.0	–	MΩ
Output Voltage Swing R_L = 10 kΩ R_L = 2.0 kΩ	V_O	 ±12 ±10	 ±14 ±13	 – –	 ±12 ±10	 ±14 ±13	 – –	V_{pk}
Input Common-Mode Voltage Swing	V_{ICR}	±12	±13	–	±12	±13	–	V_{pk}
Common-Mode Rejection Ratio (f = 20 Hz)	CMRR	70	90	–	70	90	–	dB
Input Bias Current (See Figure 2)	I_{IB}	–	200	500	–	200	500	nA
Input Offset Current	$\|I_{IO}\|$	–	30	200	–	30	200	nA
Input Offset Voltage (R_S ≤ 10 kΩ)	$\|V_{IO}\|$	–	1.0	5.0	–	2.0	6.0	mV
DC Power Consumption (See Figure 9) (Power Supply = ±15 V, V_O = 0)	P_C	–	70	150	–	70	170	mW
Positive Voltage Supply Sensitivity (V_{EE} constant)	PSS+	–	2.0	150	–	2.0	150	μV/V
Negative Voltage Supply Sensitivity (V_{CC} constant)	PSS-	–	10	150	–	10	150	μV/V

**Plastic package offered in limited temperature range device only.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_{EE} = −15 Vdc, T_A = −55 to +125°C for MC1558S and T_A = 0 to 70°C for MC1458S, unless otherwise noted.)

Characteristic	Symbol	MC1558S Min	MC1558S Typ	MC1558S Max	MC1458S Min	MC1458S Typ	MC1458S Max	Unit
Open Loop Voltage Gain V_O = ±10 V	A_{VOL}	25,000	–	–	15,000	–	–	V/V
Output Voltage Swing R_L = 10 kΩ R_L = 2 kΩ	V_O	 ±12 ±10	 – –	 – –	 ±12 ±10	 – –	 – –	V_{pk}
Input Common-Mode Voltage Range	V_{ICR}	±12	–	–	–	–	–	V_{pk}
Common-Mode Rejection Ratio (f = 20 Hz)	CMRR	70	–	–	–	–	–	dB
Input Bias Current T_A = 125°C T_A = -55°C T_A = 0 to 70°C	I_{IB}	 – – –	 200 500 –	 500 1500 –	 – – –	 – – –	 – – 800	nA
Input Offset Current T_A = 125°C T_A = -55°C T_A = 0 to 70°C	I_{IO}	 – – –	 30 – –	 200 500 –	 – – –	 – – –	 – – 300	nA
Input Offset Voltage R_S ≤ 10 kΩ	V_{IO}	–	–	6.0	–	–	7.5	mV
DC Power Consumption V_O = 0 V	P_C	–	–	200	–	–	–	mW
Positive Power Supply Sensitivity V_{EE} = -15 V	P_{SS+}	–	–	150	–	–	–	μV/V
Negative Power Supply Sensitivity V_{CC} = 15 V	P_{SS-}	–	–	150	–	–	–	μV/V

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 1 – OFFSET ADJUST CIRCUIT

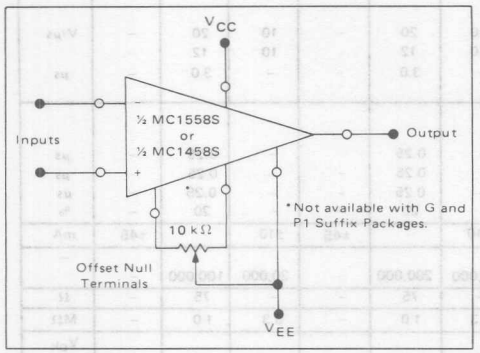


FIGURE 2 – INPUT BIAS CURRENT versus TEMPERATURE

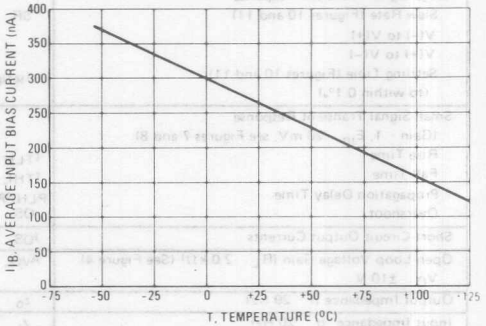


FIGURE 3 – POWER BANDWIDTH – NONDISTORTED OUTPUT VOLTAGE versus FREQUENCY

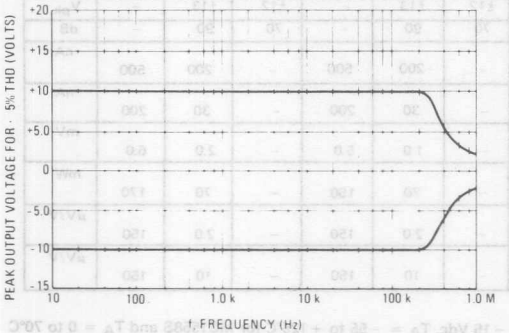


FIGURE 4 – OPEN-LOOP FREQUENCY RESPONSE

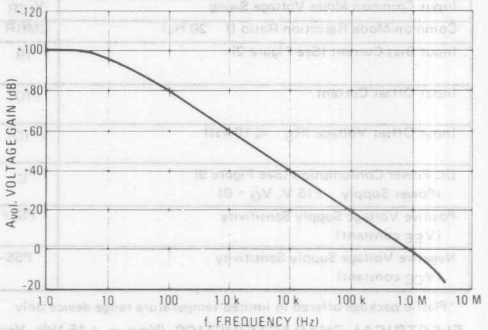
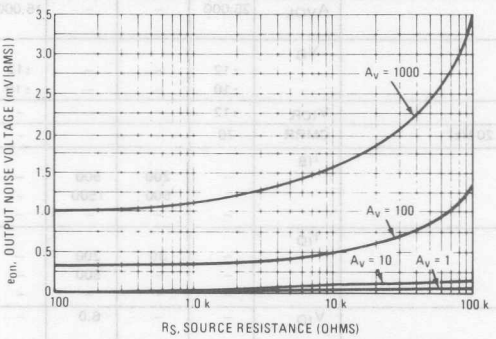


FIGURE 5 – OUTPUT NOISE versus SOURCE RESISTANCE



TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 6 – SMALL-SIGNAL TRANSIENT RESPONSE DEFINITIONS

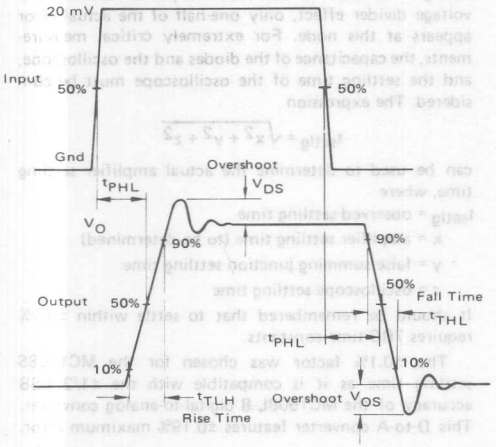


FIGURE 7 – SMALL-SIGNAL TRANSIENT RESPONSE

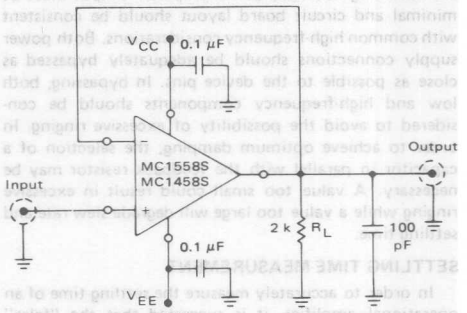


FIGURE 8 – POWER CONSUMPTION versus POWER SUPPLY VOLTAGES

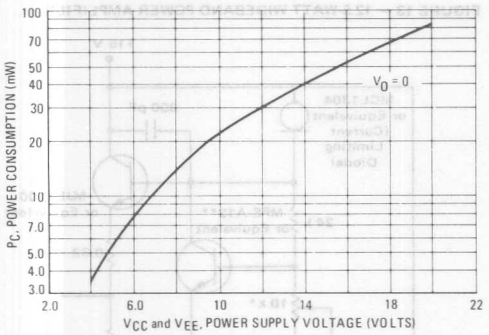


FIGURE 9 – LARGE-SIGNAL TRANSIENT WAVEFORMS

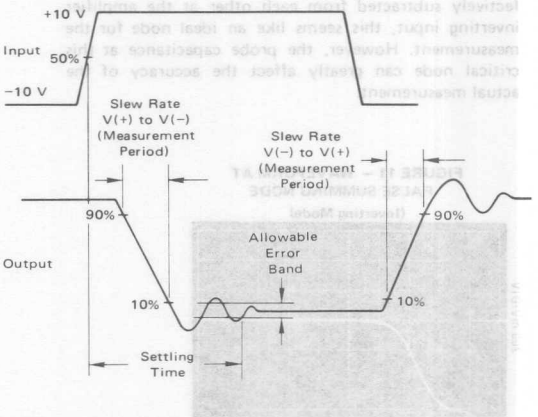
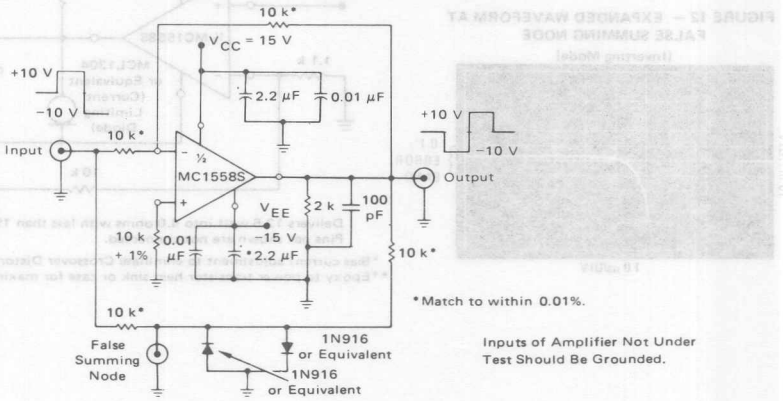


FIGURE 10 – SLEW RATE AND SETTLING TIME TEST CIRCUIT*



*Match to within 0.01%.

Inputs of Amplifier Not Under Test Should Be Grounded.

2

SETTLING TIME

In order to properly utilize the high slew rate and fast settling time of an operational amplifier, a number of system considerations must be observed. Capacitance at the summing node and at the amplifier output must be minimal and circuit board layout should be consistent with common high-frequency considerations. Both power supply connections should be adequately bypassed as close as possible to the device pins. In bypassing, both low and high-frequency components should be considered to avoid the possibility of excessive ringing. In order to achieve optimum damping, the selection of a capacitor in parallel with the feedback resistor may be necessary. A value too small could result in excessive ringing while a value too large will degrade slew rate and settling time.

SETTLING TIME MEASUREMENT

In order to accurately measure the settling time of an operational amplifier, it is suggested that the "false" summing junction approach be taken as shown in Figure 11. This is necessary since it is difficult to determine when the waveform at the output of the operational amplifier settles to within 0.1% of it's final value. Because the output and input voltages are effectively subtracted from each other at the amplifier inverting input, this seems like an ideal node for the measurement. However, the probe capacitance at this critical node can greatly affect the accuracy of the actual measurement.

The solution to these problems is the creation of a second or "false" summing node. The addition of two diodes at this node clamps the error voltage to limit the voltage excursion to the oscilloscope. Because of the voltage divider effect, only one-half of the actual error appears at this node. For extremely critical measurements, the capacitance of the diodes and the oscilloscope, and the settling time of the oscilloscope must be considered. The expression

$$t_{setlg} = \sqrt{x^2 + y^2 + z^2}$$

can be used to determine the actual amplifier settling time, where

t_{setlg} = observed settling time

x = amplifier settling time (to be determined)

y = false summing junction settling time

z = oscilloscope settling time

It should be remembered that to settle within ±0.1% requires 7RC time constants.

The ±0.1% factor was chosen for the MC1558S settling time as it is compatible with the ±1/2 LSB accuracy of the MC1508L-8 digital-to-analog converter. This D-to-A converter features ±0.19% maximum error.

FIGURE 11 – WAVEFORM AT FALSE SUMMING NODE

(Inverting Mode)

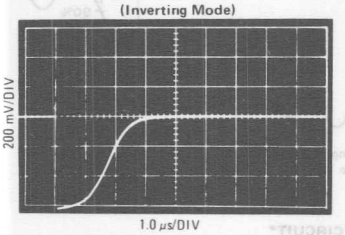
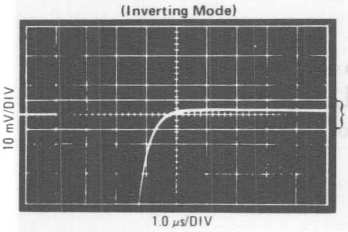


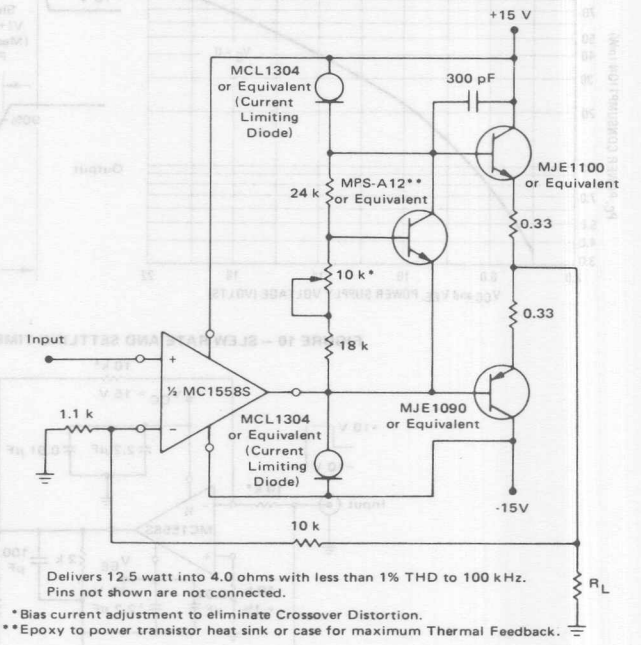
FIGURE 12 – EXPANDED WAVEFORM AT FALSE SUMMING NODE

(Inverting Mode)



TYPICAL APPLICATION

FIGURE 13 – 12.5-WATT WIDEBAND POWER AMPLIFIER



Delivers 12.5 watt into 4.0 ohms with less than 1% THD to 100 kHz.
Pins not shown are not connected.

*Bias current adjustment to eliminate Crossover Distortion.

**Epoxy to power transistor heat sink or case for maximum Thermal Feedback.

MOTOROLA

MC1490P

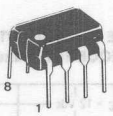
WIDEBAND AMPLIFIER WITH AGC

SILICON MONOLITHIC INTEGRATED CIRCUIT

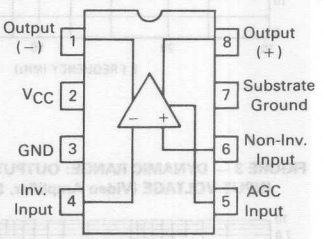
RF/IF/AUDIO AMPLIFIER

. . . an integrated circuit featuring wide-range AGC for use in RF/IF amplifiers and audio amplifiers over the temperature range, −40 to +85°C. See Motorola Application Note AN513 for design details.

- High Power Gain — 50 dB Typ at 10 MHz
  45 dB Typ at 60 MHz
  35 dB Typ at 100 MHz
- Wide-Range AGC — 60 dB Min, dc to 60 MHz
- 6.0 to 15 V Operation, Single-Polarity Power Supply



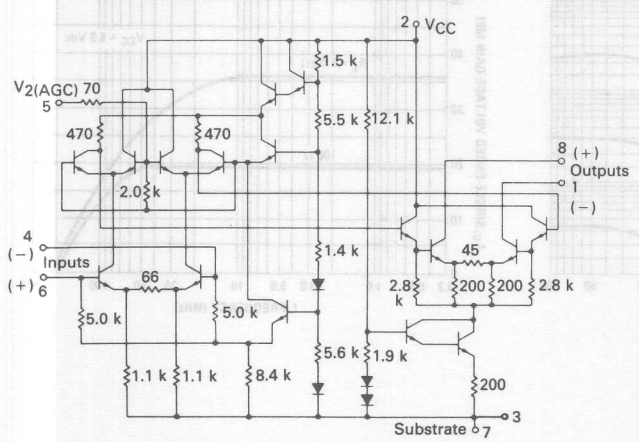
P SUFFIX
PLASTIC PACKAGE
CASE 626-05



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+18	Vdc
Output Supply	V_O	+18	Vdc
AGC Supply	$V_{2(AGC)}$	V_{CC}	Vdc
Differential Input Voltage	V_I	5.0	Vdc
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Junction Temperature	T_J	+150	°C

REPRESENTATIVE CIRCUIT SCHEMATIC



Pins 3 and 7 should both be connected to circuit ground.

SCATTERING PARAMETERS (V_{CC} = +12 Vdc, T_A = +25°C, Z_o = 50 Ω)

Parameter	Symbol	f = MHz Typ 30	f = MHz Typ 60	Unit
Input Reflection Coefficient	$\|S_{11}\|$ θ_{11}	0.95 −7.3	0.93 −16	— degrees
Output Reflection Coefficient	$\|S_{22}\|$ θ_{22}	0.99 −3.0	0.98 −5.5	— degrees
Forward Transmission Coefficient	$\|S_{21}\|$ θ_{21}	16.8 128	14.7 64.3	— degrees
Reverse Transmission Coefficient	S_{12} θ_{12}	0.00048 84.9	0.00092 79.2	— degrees

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 Vdc, f = 60 MHz, BW = 1.0 MHz, T_A = 25°C)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Power Supply Current Drain	—	I_{CC}	—	—	17	mA
AGC Range (AGC) 5.0 V Min to 7.0 V Max	19	M_{AGC}	−60	—	—	dB
Output Stage Current (Sum of Pins 1 and 8)	—	I_O	4.0	—	7.5	mA
Single Ended Power Gain R_S = R_L = 50 Ohms	19	G_P	40	—	—	dB
Noise Figure R_S = 50 Ohms	19	NF	—	6.0	—	dB
Power Dissipation	—	P_D	—	168	204	mW

TYPICAL CHARACTERISTICS

($V_{2\ (AGC)}$ = 0, V_{CC} = 12 Vdc, T_A = +25°C unless otherwise noted)

FIGURE 1 — UNNEUTRALIZED POWER GAIN versus FREQUENCY (Tuned Amplifier, See Figure 19)

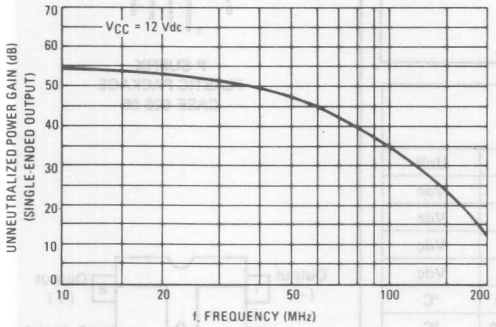


FIGURE 2 — VOLTAGE GAIN versus FREQUENCY (Video Amplifier, See Figure 21)

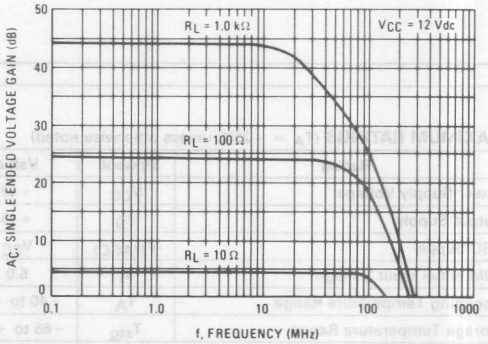


FIGURE 3 — DYNAMIC RANGE: OUTPUT VOLTAGE versus INPUT VOLTAGE (Video Amplifier, See Figure 21)

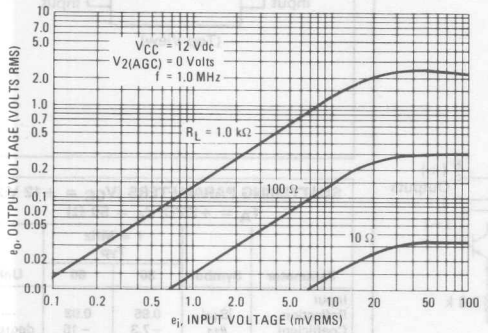


FIGURE 4 — VOLTAGE GAIN versus FREQUENCY (Video Amplifier, See Figure 21)

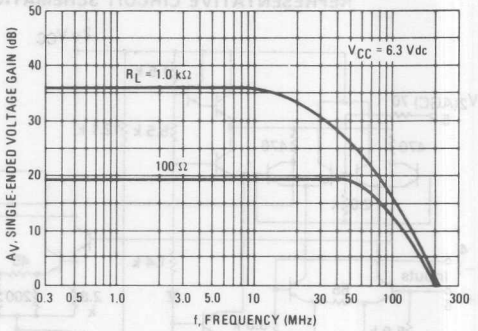


FIGURE 5 — VOLTAGE GAIN AND SUPPLY CURRENT versus SUPPLY VOLTAGE (Video Amplifier, See Figure 21)

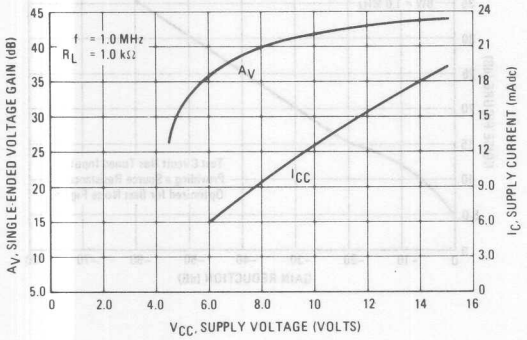


FIGURE 6 — TYPICAL GAIN REDUCTION versus AGC VOLTAGE

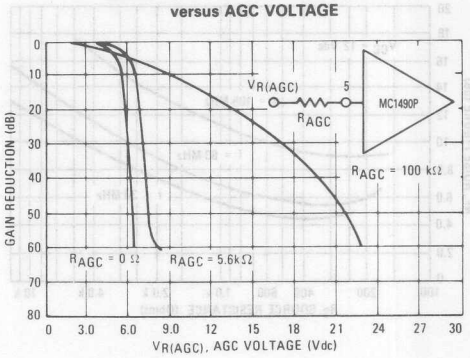


FIGURE 7 — TYPICAL GAIN REDUCTION versus AGC CURRENT

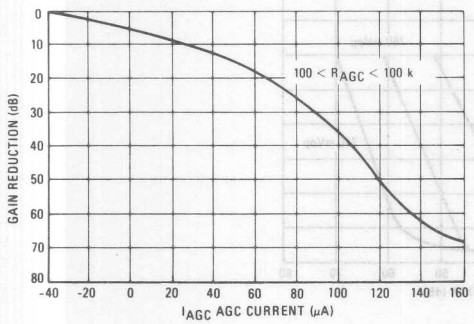


FIGURE 8 — FIXED TUNED POWER GAIN REDUCTION versus TEMPERATURE (See Test Circuit, Figure 19)

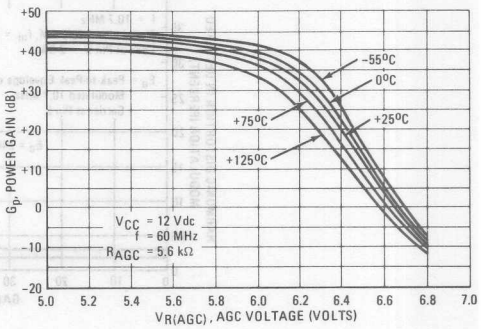


FIGURE 9 — POWER GAIN versus SUPPLY VOLTAGE (See Test Circuit, Figure 19)

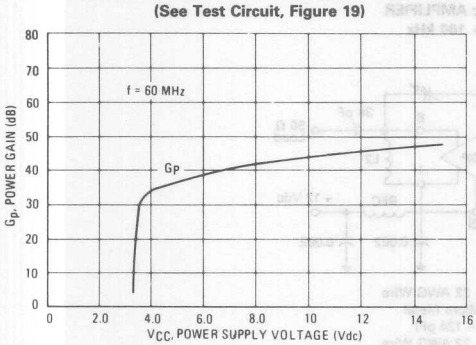
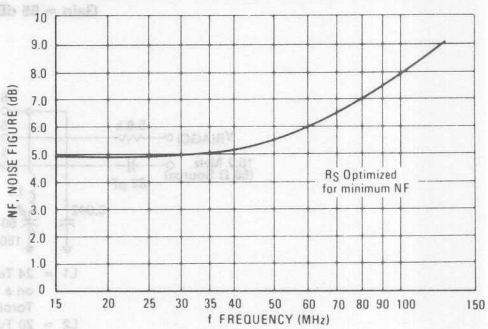


FIGURE 10 — NOISE FIGURE versus FREQUENCY



2

FIGURE 11 — NOISE FIGURE versus SOURCE RESISTANCE

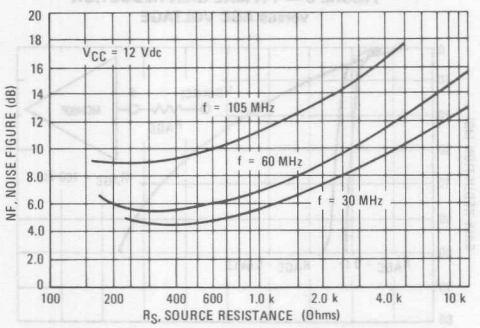


FIGURE 12 — NOISE FIGURE versus AGC GAIN REDUCTION

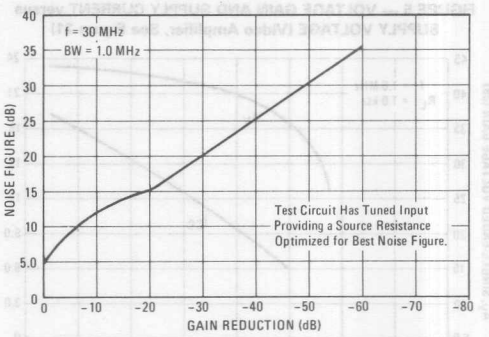


FIGURE 13 — HARMONIC DISTORTION versus AGC GAIN REDUCTION FOR AM CARRIER (For Test Circuit, See Figure 14)

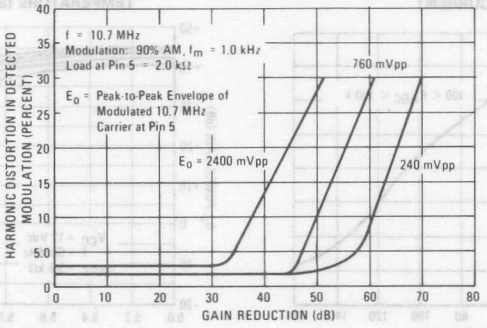
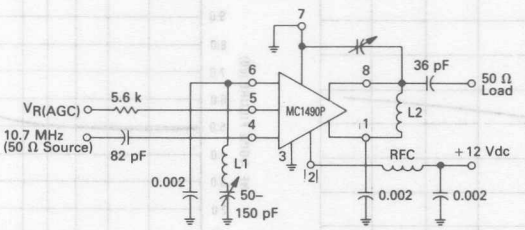


FIGURE 14 — 10.7 MHz AMPLIFIER
Gain ≃ 55 dB, BW ≃ 100 kHz



L1 = 24 Turns, No. 22 AWG Wire on a T12-44 Micro Metal Toroid Core (– 124 pF)

L2 = 20 Turns, No. 22 AWG Wire on a T12-44 Micro Metal Toroid Core (– 100 pF)

TYPICAL CHARACTERISTICS (continued)

FIGURE 15 — S_{11} AND S_{22}, INPUT AND OUTPUT REFLECTION COEFFICIENT

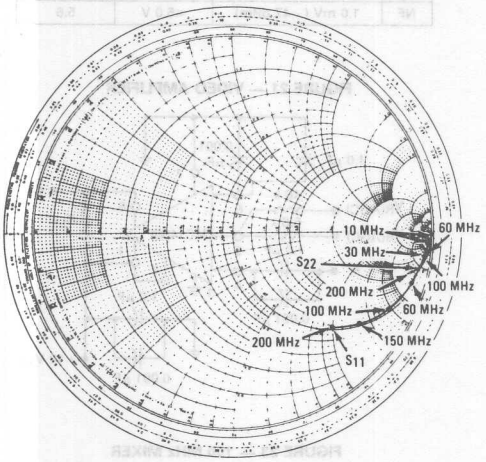


FIGURE 16 — S_{11} AND S_{22}, INPUT AND OUTPUT REFLECTION COEFFICIENT

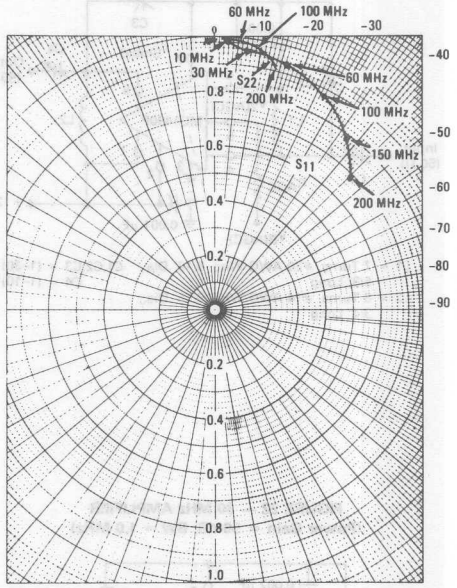


FIGURE 17 — S_{21}, FORWARD TRANSMISSION COEFFICIENT (GAIN)

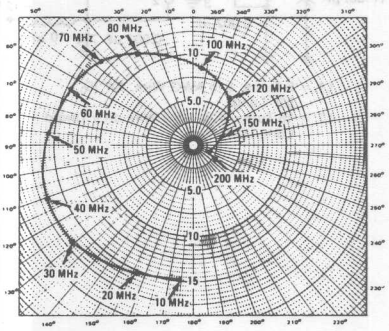
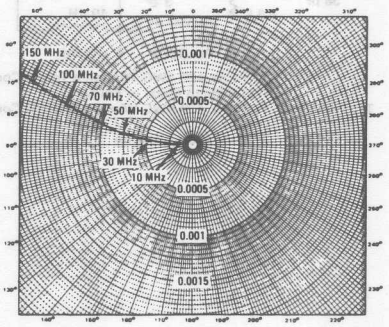
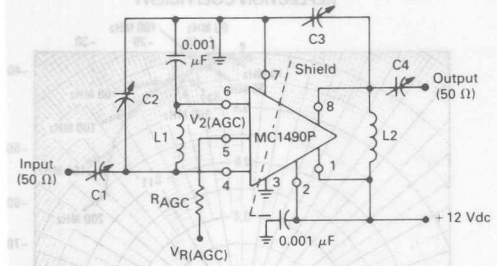


FIGURE 18 — S_{12}, REVERSE TRANSMISSION COEFFICIENT (FEEDBACK)



2

FIGURE 19 — 60 MHz POWER GAIN TEST CIRCUIT



L1 = 7 Turns, #20 AWG Wire, 5/16" Dia., 5/8" Long
L2 = 6 Turns, #14 AWG Wire, 9/16" Dia., 3/4" Long
C1,C2,C3 = (1–30) pF
C4 = (1–10) pF

FIGURE 20 — PROCEDURE FOR SETUP USING FIGURE 19

Test	e_{in}	$V_{2(AGC)}$	$R_{AGC}(k\Omega)$
M_{AGC}	2.23 mV (−40 dBm)	5–7 V	0
G_p	1.0 mV (−47 dBm)	≤5.0 V	5.6
NF	1.0 mV (−47 dBm)	≤5.0 V	5.6

FIGURE 21 — VIDEO AMPLIFIER

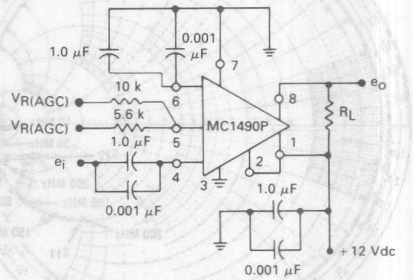
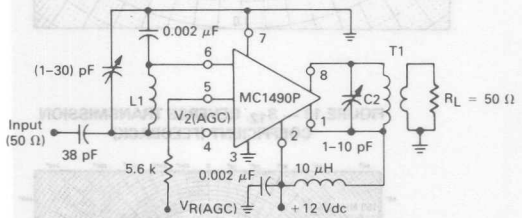
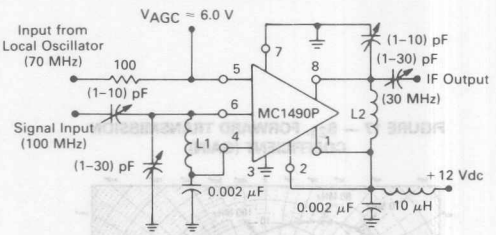


FIGURE 22 — 30 MHz AMPLIFIER (Power Gain = 50 dB, BW ≈ 1.0 MHz)



L1 = 12 Turns #22 AWG Wire on a Toroid Core, (T37-6 Micro Metal or Equiv)
T1: Primary = 17 Turns #20 AWG Wire on a Toroid Core, (T44-6)
Secondary = 2 Turns #20 AWG Wire

FIGURE 23 — 100 MHz MIXER



L1 = 5 Turns, #16 AWG Wire, 1/4" ID, 5/8" Long
L2 = 16 Turns, #20 AWG Wire on a Toroid Core, (T44-6)

MOTOROLA

MC1590G

RF/IF/AUDIO AMPLIFIER

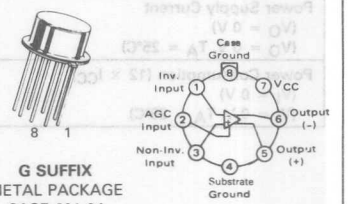
. . . an integrated circuit featuring wide-range AGC for use in RF/IF amplifiers and audio amplifiers over the temperature range, −55 to +125°C. See Motorola Application Note AN513 for design details.

- High Power Gain — 50 dB Typ at 10 MHz
  45 dB Typ at 60 MHz
  35 dB Typ at 100 MHz
- Wide-Range AGC — 60 dB min, dc to 60 MHz
- Low Reverse Transfer Admittance — <10 μmhos Typ at 60 MHz
- 6.0 to 15-Volt Operation, Single-Polarity Power Supply

WIDEBAND AMPLIFIER WITH AGC

SILICON MONOLITHIC INTEGRATED CIRCUIT

PIN CONNECTIONS

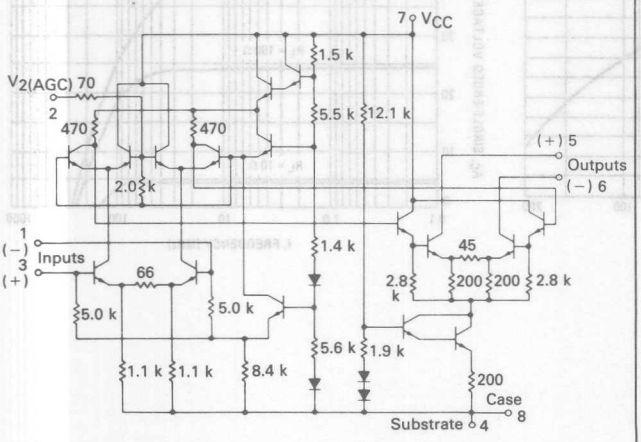


G SUFFIX
METAL PACKAGE
CASE 601-04

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol*	Value	Unit
Power Supply Voltage	V_{CC}	+18	Vdc
Output Supply	V_O	+18	Vdc
AGC Supply	$V_{2(AGC)}$	V_{CC}	Vdc
Differential Input Voltage	V_I	5.0	Vdc
Operating Temperature Range	T_A	−55 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Junction Temperature	T_J	+175	°C

REPRESENTATIVE CIRCUIT SCHEMATIC



Pins 4 and 8 should both be connected to circuit ground.

ADMITTANCE PARAMETERS (V_{CC} = +12 Vdc, T_A = +25°C)

Parameter	Symbol	f = MHz Typ 30	f = MHz Typ 60	Unit
Single-Ended Input Admittance	g_{11} b_{11}	0.4 1.2	0.6 −3.0	mmhos
Single-Ended Output Admittance	g_{22} b_{22}	0.05 0.50	0.1 1.0	mmho
Forward Transfer Admittance (Pin 1 to Pin 5)	Y_{21} θ_{21} (Polar)	175 −30	150 −105	mmhos degrees
Reverse Transfer Admittance*	g_{12} b_{12}	−0 −5.0	−0 −10	μmhos

*The value of Reverse Transfer Admittance includes the feedback admittance of the test circuit used in the measurement. The total feedback capacitance (including test circuit) is 0.025 pF and is a more practical value for design calculations than the internal feedback of the device alone. (See Figure 10.)

SCATTERING PARAMETERS (V_{CC} = +12 Vdc, T_A = +25°C, Z_o = 50 Ω)

Parameter	Symbol	f = MHz Typ 30	f = MHz Typ 60	Unit
Input Reflection Coefficient	S_{11} θ_{11}	0.95 −7.3	0.93 −16	– degrees
Output Reflection Coefficient	S_{22} θ_{22}	0.99 −3.0	0.98 −5.5	– degrees
Forward Transmission Coefficient	S_{21} θ_{21}	16.8 128	14.7 64.3	– degrees
Reverse Transmission Coefficient	S_{12} θ_{12}	0.00048 84.9	0.00092 79.2	– degrees

2

ELECTRICAL CHARACTERISTICS (V_{CC} = +12 Vdc, f = 60 MHz, BW = 1.0 MHz, T_A = −55°C to +125°C unless otherwise noted)

Characteristic	Fig.	Symbol	Min	Typ	Max	Unit
AGC Range	24	M_{AGC}				dB
($V_{2(AGC)}$ = 5.0 V to 7.0 V)			58	—	—	
($V_{2(AGC)}$ = 5.0 V to 7.0 V, T_A = 25°C)			60	68	—	
Single-Ended Power Gain	24	G_p	37	—	—	dB
(T_A = 25°C)			40	45	—	
Noise Figure	24	NF	—	6.0	7.0	dB
(R_S optimized for best NF) (T_A = 25°C)						
Output Stage Current	32	I_O				mA
(Sum of Pins 5 and 6)			3.5	—	8.0	
(T_A = 25°C)			4.0	5.6	7.5	
Output Current Matching	32	ΔI_O	—	0.7	—	mA
(Magnitude of Difference of Output Currents)						
($I_5 - I_6$) (T_A = 25°C)						
Power Supply Current	32	I_{CC}				mA
(V_O = 0 V)			—	—	20	
(V_O = 0 V, T_A = 25°C)			—	14	17	
Power Consumption (12 × I_{CC})	—	P_C				mW
(V_I = 0 V)			—	—	240	
(V_I = 0 V, T_A = 25°C)			—	168	204	

FIGURE 1 – UNNEUTRALIZED POWER GAIN versus FREQUENCY
(Tuned Amplifier, See Figure 24)

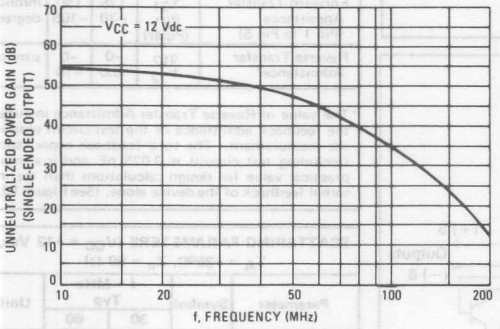
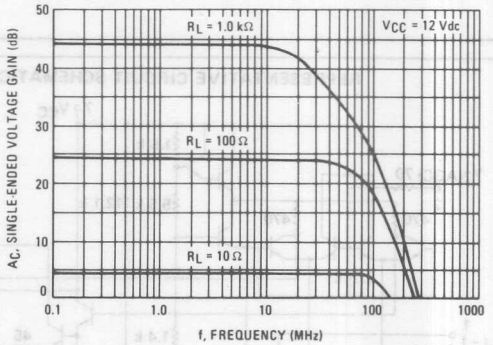


FIGURE 2 – VOLTAGE GAIN versus FREQUENCY
(Video Amplifier, See Figure 26)



TYPICAL CHARACTERISTICS

($V_{2\,(AGC)}$ = 0, V_{CC} = 12 Vdc, T_A = +25°C unless otherwise noted)

FIGURE 3 – DYNAMIC RANGE: OUTPUT VOLTAGE versus INPUT VOLTAGE (Video Amplifier, See Figure 26)

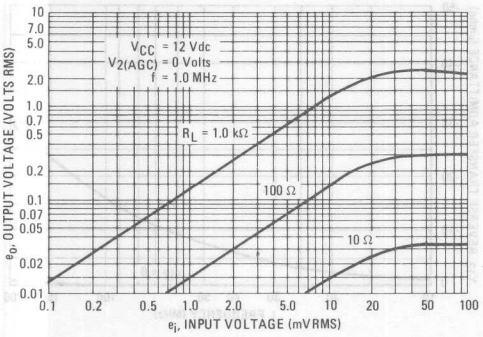


FIGURE 4 – VOLTAGE GAIN versus FREQUENCY (Video Amplifier, See Figure 26)

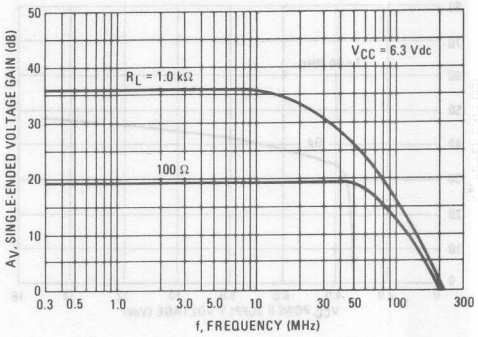


FIGURE 5 – VOLTAGE GAIN AND SUPPLY CURRENT versus SUPPLY VOLTAGE (Video Amplifier, See Figure 26)

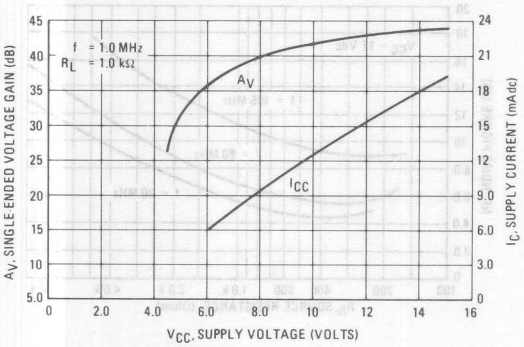


FIGURE 6 – TYPICAL GAIN REDUCTION versus AGC VOLTAGE

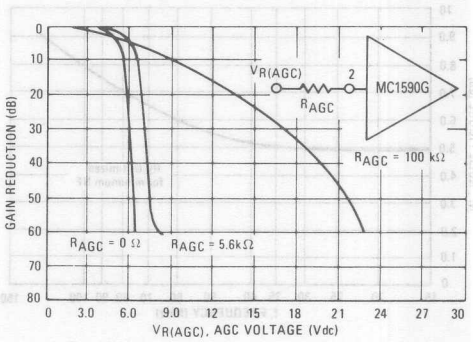


FIGURE 7 – TYPICAL GAIN REDUCTION versus AGC CURRENT

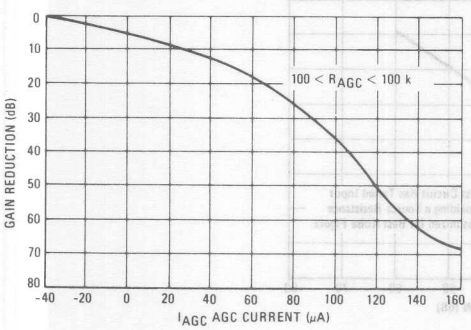


FIGURE 8 – FIXED TUNED POWER GAIN REDUCTION versus TEMPERATURE (See Test Circuit, Figure 24)

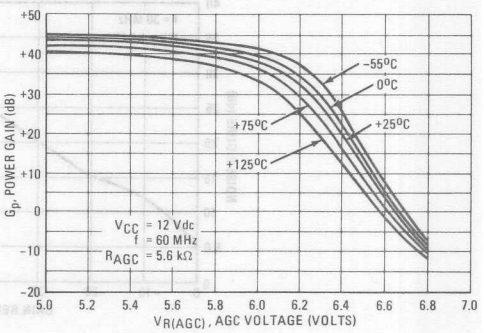


FIGURE 9 – POWER GAIN versus SUPPLY VOLTAGE (See Test Circuit, Figure 24)

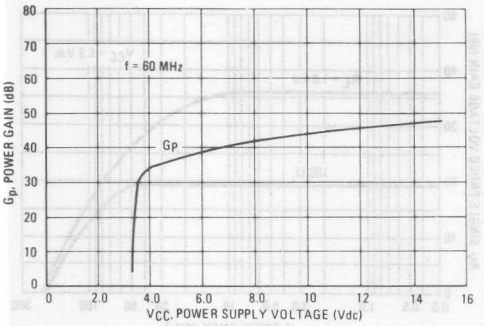


FIGURE 10 – REVERSE TRANSFER ADMITTANCE versus FREQUENCY (See Parameter Table, Page 1)

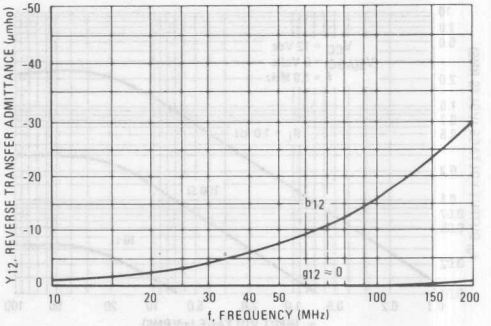


FIGURE 11 – NOISE FIGURE versus FREQUENCY

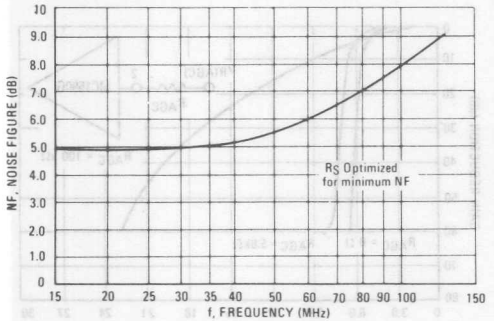


FIGURE 12 – NOISE FIGURE versus SOURCE RESISTANCE

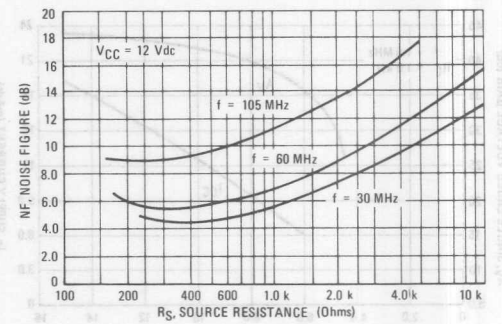
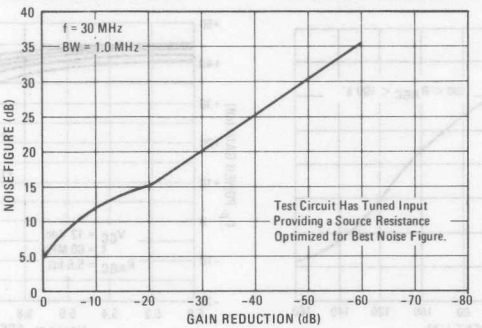


FIGURE 13 – NOISE FIGURE versus AGC GAIN REDUCTION



TYPICAL CHARACTERISTICS (continued)

FIGURE 14 – SINGLE-ENDED OUTPUT ADMITTANCE

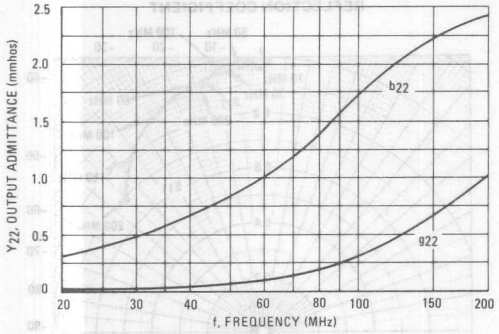


FIGURE 15 – SINGLE-ENDED INPUT ADMITTANCE

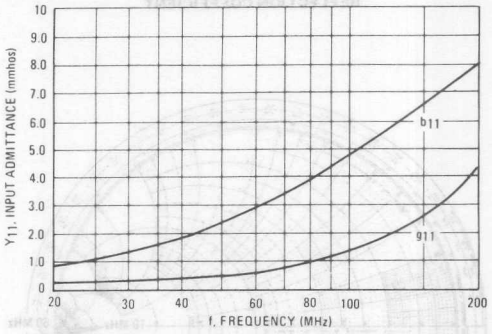


FIGURE 16 – HARMONIC DISTORTION versus AGC GAIN REDUCTION FOR AM CARRIER (For Test Circuit, See Figure 17)

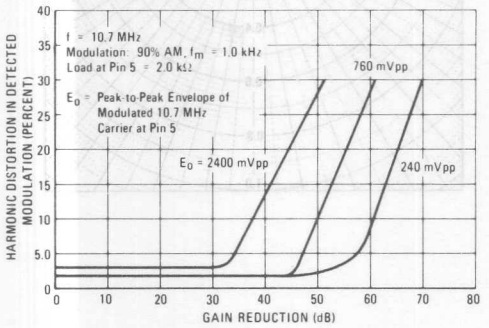
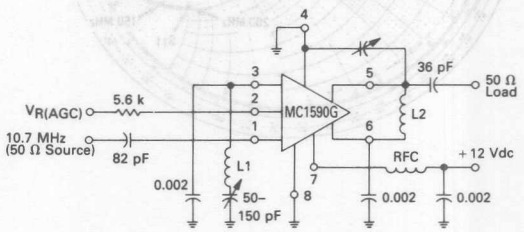


FIGURE 17 — 10.7 MHz AMPLIFIER
Gain ≈ 55 dB, BW ≈ 100 kHz



L1 = 24 Turns, No. 22 AWG Wire on a T12-44 Micro Metal Toroid Core (– 124 pF)
L2 = 20 Turns, No. 22 AWG Wire on a T12-44 Micro Metal Toroid Core (– 100 pF)

FIGURE 18 – Y_{21}, FORWARD TRANSFER ADMITTANCE RECTANGULAR FORM

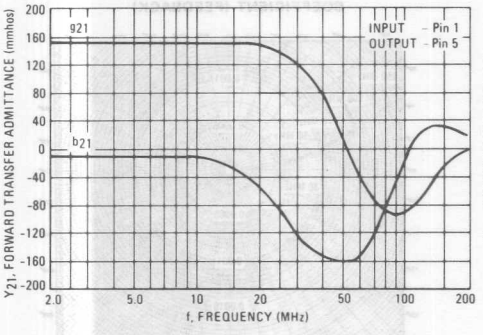
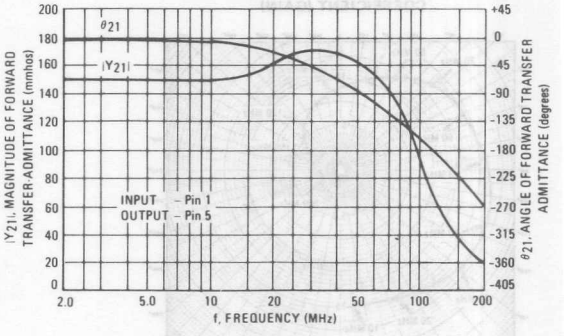


FIGURE 19 — Y_{21}, FORWARD TRANSFER ADMITTANCE POLAR FORM



2

TYPICAL CHARACTERISTICS (continued)

FIGURE 20 – S_{11} AND S_{22}, INPUT AND OUTPUT REFLECTION COEFFICIENT

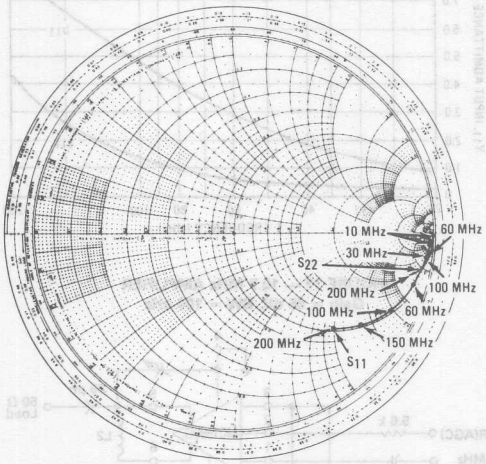


FIGURE 21 – S_{11} AND S_{22}, INPUT AND OUTPUT REFLECTION COEFFICIENT

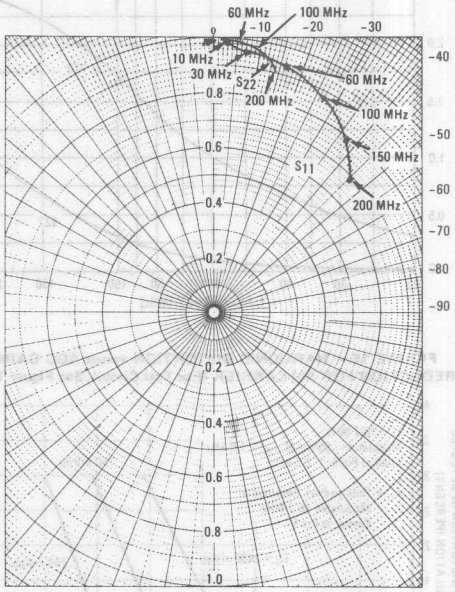


FIGURE 22 – S_{21}, FORWARD TRANSMISSION COEFFICIENT (GAIN)

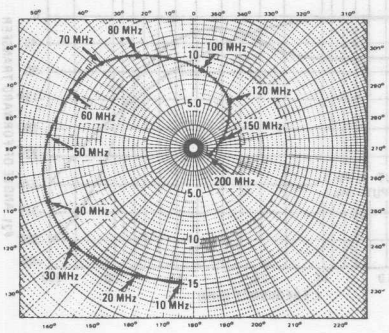
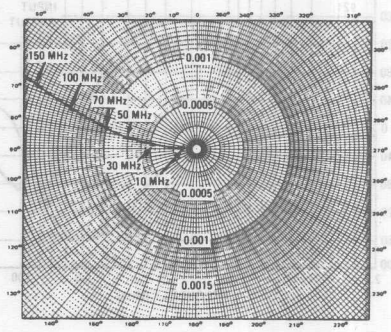
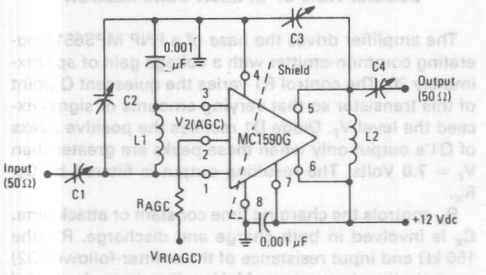


FIGURE 23 – S_{12}, REVERSE TRANSMISSION COEFFICIENT (FEEDBACK)



TYPICAL APPLICATIONS

FIGURE 24 — 60 MHz POWER GAIN TEST CIRCUIT



L1 = 7 Turns, #20 AWG Wire, 5/16" Dia., 5/8" Long
L2 = 6 Turns, #14 AWG Wire, 9/16" Dia., 3/4" Long
C1,C2,C3 = (1-30) pF
C4 = (1-10) pF

FIGURE 25 — PROCEDURE FOR SETUP USING FIGURE 24

Test	e_{in}	$V_{2(AGC)}$	R_{AGC}(kΩ)
M_{AGC}	2.23 mV (−40dBm)	5.7 V	0
Gp	1.0 mV (−47dBm)	≤ 5.0 V	5.6
NF	1.0 mV (−47dBm)	≤ 5.0 V	5.6

FIGURE 26 – VIDEO AMPLIFIER

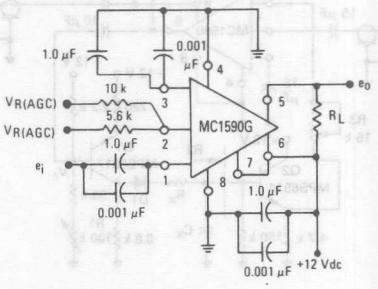
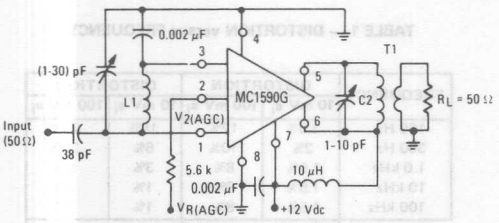
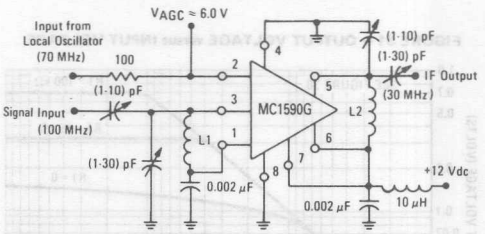


FIGURE 27 — 30 MHz AMPLIFIER (Power Gain = 50 dB, BW ≈ 1.0 MHz)



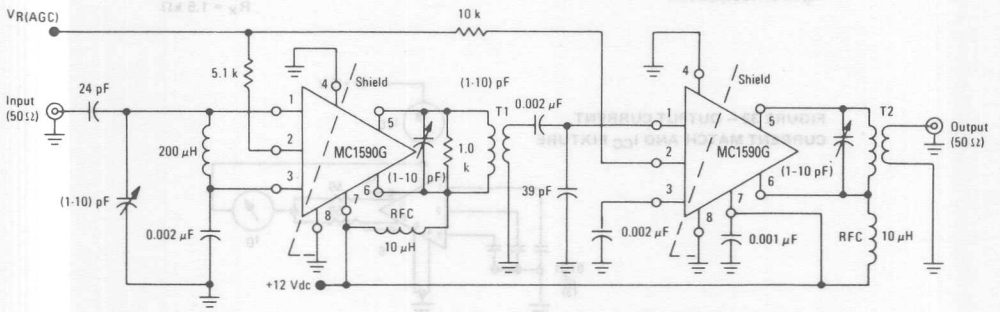
L1 = 12 Turns #22 AWG Wire on a Toroid Core, (T37-6 Micro Metal or Equiv)
T1: Primary = 17 Turns #20 AWG Wire on a Toroid Core, (T44-6 Micro Metal or Equiv)
Secondary = 2 Turns #20 AWG Wire

FIGURE 28 – 100 MHz MIXER



L1 = 5 Turns, #16 AWG Wire, 1/4" ID, 5/8" Long
L2 = 16 Turns, #20 AWG Wire on a Toroid Core, (T44-6 Micro Metal or Equiv)

FIGURE 29 – TWO-STAGE 60 MHz IF AMPLIFIER (Power Gain ≈ 80 dB, BW ≈ 1.5 MHz)

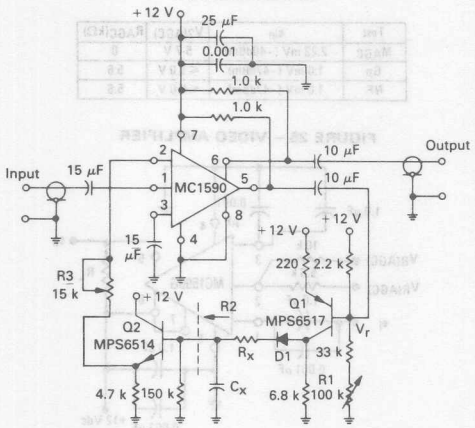


T1: Primary Winding = 15 Turns, #22 AWG Wire, 1/4" ID Air Core
Secondary Winding = 4 Turns, #22 AWG Wire,
Coefficient of Coupling ≈ 1.0

T2: Primary Winding = 10 Turns, #22 AWG Wire, 1/4" ID Air Core
Secondary Winding = 2 Turns, #22 AWG Wire,
Coefficient of Coupling ≈ 1.0

2

FIGURE 30 – SPEECH COMPRESSOR



DESCRIPTION OF SPEECH COMPRESSOR

The amplifier drives the base of a PNP MPS6517 operating common-emitter with a voltage gain of approximately 20. The control R1 varies the quiescent Q point of this transistor so that varying amounts of signal exceed the level V_r. Diode D1 rectifies the positive peaks of Q1's output only when these peaks are greater than V_r = 7.0 Volts. The resulting output is filtered by C_X, R_X.

R_X controls the charging time constant or attack time. C_X is involved in both charge and discharge. R2 (the 150 kΩ and input resistance of the emitter-follower Q2) controls the decay time. Making the decay long and attack short is accomplished by making R_X small and R2 large. (A Darlington emitter-follower may be needed if extremely slow decay times are required.)

The emitter-follower Q2 drives the AGC Pin 2 of the MC1590G and reduces the gain. R3 controls the slope of signal compression. The following graph (Figure 31) details performance with R3 set to 15 kΩ.

FIGURE 31 – OUTPUT VOLTAGE versus INPUT VOLTAGE

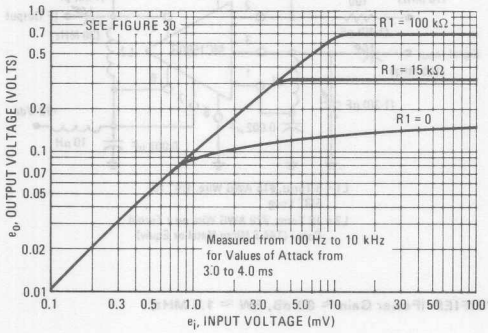
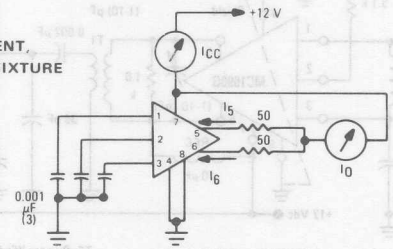


TABLE 1 — DISTORTION versus FREQUENCY

FREQUENCY	DISTORTION		DISTORTION	
	10 mV e_i	100 mV e_i	10 mV e_i	100 mV e_i
100 Hz	3.5%	12%	15%	27%
300 Hz	2%	10%	6%	20%
1.0 kHz	1.5%	8%	3%	9%
10 kHz	1.5%	8%	1%	3%
100 kHz	1.5%	8%	1%	3%
	Notes 1 and 2		Notes 3 and 4	

Note: (1) Decay = 300 ms
Attack = 20 ms
(2) C_X = 7.5 μF
R_X = 0 (Short)
(3) Decay = 20 ms
Attack = 3 ms
(4) C_X = 0.68 μF
R_X = 1.5 kΩ

FIGURE 32 – OUTPUT CURRENT, CURRENT MATCH AND I_{CC} FIXTURE



MC1709
MC1709A
MC1709C

OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

ORDERING INFORMATION

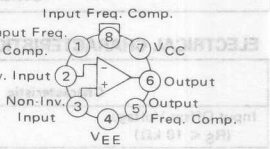
Device	Temperature Range	Package
MC1709CG	0°C to +70°C	Metal Can
MC1709CU	0°C to +70°C	Ceramic DIP
MC1709CP1	0°C to +70°C	Plastic DIP
MC1709G,AG	−55°C to +125°C	Metal Can
MC1709AU	−55°C to +125°C	Ceramic DIP

MONOLITHIC OPERATIONAL AMPLIFIER

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- High-Performance Open Loop Gain Characteristics
  A_{vol} = 45,000 typical
- Low Temperature Drift — ±3.0 μV/°C typical (MC1709)
- Large Output Voltage Swing — ±14 V typical @ ±15 V Supply
- Low Output Impedance — z_o = 150 ohms typical

PIN CONNECTIONS



(Top View)

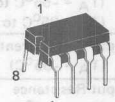
G SUFFIX
METAL PACKAGE
CASE 601-04



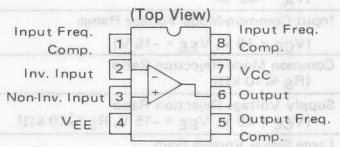
P1 SUFFIX
PLASTIC PACKAGE
CASE 626-05
(MC1709C Only)



U SUFFIX
CERAMIC PACKAGE
CASE 693-02



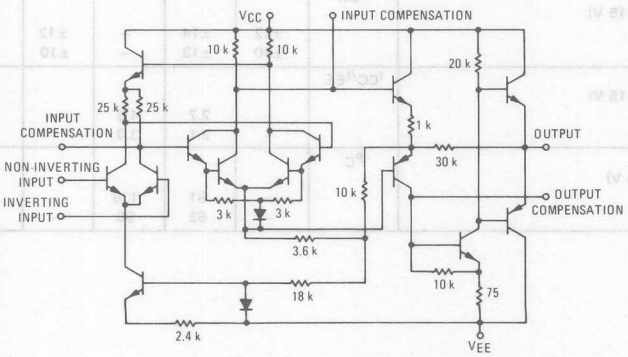
(Top View)



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 −18	Vdc
Input Differential Voltage Range	V_{IDR}	±5.0	Volts
Input Common-Mode Range	V_{ICR}	±10	Volts
Output Load Current	I_L	10	mA
Output Short-Circuit Duration	t_S	5.0	s
Power Dissipation (Package Limitation) Metal Can Derate above T_A = +25°C	P_D	 680 4.6	 mW mW/°C
Plastic Dual In-Line Packages (MC1709C only) Derate above T_A = +25°C		625 5.0	mW mW/°C
Ceramic Dual In-Line Package Derate above T_A = +25°C		750 6.0	mW mW/°C
Operating Ambient Temperature Range MC1709A, MC1709 MC1709C	T_A	−55 to +125 0 to +70	°C
Storage Temperature Range Metal and Ceramic Packages Plastic Packages	T_{stg}	 −65 to +150 −55 to +125	°C

FIGURE 1 — EQUIVALENT CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS (unless otherwise noted, $+9.0\ V \leq V_{CC} \leq 15\ V$, $-9.0\ V \geq V_{EE} \geq -15\ V$, $T_A = 25°C$)

Characteristic	Symbol	MC1709A			MC1709			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10\ k\Omega$)	V_{IO}	–	0.6	2.0	–	1.0	5.0	mV
Input Offset Current	I_{IO}	–	10	50	–	50	200	nA
Input Bias Current	I_{IB}	–	100	200	–	200	500	nA
Input Resistance	r_i	350	700	–	150	400	–	kΩ
Output Resistance	r_o	–	150	–	–	150	–	Ω
Power Supply Currents ($V_{CC} = 15\ V$, $V_{EE} = -15\ V$)	I_{CC}, I_{EE}	–	2.5	3.6	–	–	–	mA
Power Consumption ($V_{CC} = 15\ V$, $V_{EE} = -15\ V$)	P_C	–	75	108	–	80	165	mW
Transient Response ($V_{CC} = 15\ V$, $V_{EE} = -15\ V$) See Figure 8								
Risetime	t_{TLH}	–	–	1.5	–	0.3	1.0	μs
Overshoot	OS	–	–	30	–	10	30	%

ELECTRICAL CHARACTERISTICS (unless otherwise noted, $+9.0\ V \leq V_{CC} \leq 15\ V$, $-9.0\ V \geq V_{EE} \geq -15\ V$, $T_A = -55°C$ to $+125°C$)

Characteristic	Symbol	MC1709A			MC1709			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10\ k\Omega$)	V_{IO}	–	–	3.0	–	–	6.0	mV
Average Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$							μV/°C
($R_S = 50\ \Omega$, $T_A = 25°C$ to $125°C$)		–	1.8	10	–	–	–	
($R_S = 50\ \Omega$, $T_A = -55°C$ to $25°C$)		–	1.8	10	–	–	–	
($R_S = 50\ \Omega$, $T_A = -55°C$ to $125°C$)		–	–	–	–	3.0	–	
($R_S = 10\ k\Omega$, $T_A = 25°C$ to $125°C$)		–	2.0	15	–	–	–	
($R_S = 10\ k\Omega$, $T_A = -55°C$ to $25°C$)		–	4.8	25	–	–	–	
($R_S = 10\ k\Omega$, $T_A = -55°C$ to $125°C$)		–	–	–	–	6.0	–	
Input Offset Current	I_{IO}							nA
($T_A = -55°C$)		–	40	250	–	100	500	
($T_A = 125°C$)		–	3.5	50	–	20	200	
Average Temperature Coefficient of Input Offset Current	$\Delta I_{IO}/\Delta T$							nA/°C
($T_A = -55°C$ to $25°C$)		–	0.45	2.8	–	–	–	
($T_A = 25°C$ to $125°C$)		–	0.08	0.5	–	–	–	
Input Bias Current ($T_A = -55°C$)	I_{IB}	–	300	600	–	500	1500	nA
Input Resistance ($T_A = -55°C$)	r_i	85	170	–	40	100	–	kΩ
Input Common-Mode Voltage Range ($V_{CC} = 15\ V$, $V_{EE} = -15\ V$)	V_{ICR}	±8.0	±10	–	±8.0	±10	–	V
Common Mode Rejection Ratio ($R_S \leq 10\ k\Omega$)	CMRR	80	110	–	70	90	–	dB
Supply Voltage Rejection Ratio ($V_{CC} = 15\ V$, $V_{EE} = -15\ V$, $R_S \leq 10\ k\Omega$)	PSRR	–	40	100	–	25	150	μV/V
Large Signal Voltage Gain ($V_{CC} = 15\ V$, $V_{EE} = -15\ V$, $R_L \geq 2.0\ k\Omega$, $V_O = \pm 15\ V$)	A_V	25	45	70	25	45	70	V/mV
Output Voltage Range ($V_{CC} = 15\ V$, $V_{EE} = -15\ V$)	V_{OR}							V
($R_L \geq 10\ k\Omega$)		±12	±14	–	±12	±14	–	
($R_L \geq 2.0\ k\Omega$)		±10	±13	–	±10	±13	–	
Power Supply Currents ($V_{CC} = 15\ V$, $V_{EE} = -15\ V$)	I_{CC}/I_{EE}							mA
($T_A = -55°C$)		–	2.7	4.5	–	–	–	
($T_A = 125°C$)		–	2.1	3.0	–	–	–	
Power Consumption ($V_{CC} = 15$, $V_{EE} = -15\ V$)	P_C							mW
($T_A = -55°C$)		–	81	135	–	–	–	
($T_A = 125°C$)		–	63	90	–	–	–	

ELECTRICAL CHARACTERISTICS (unless otherwise noted, V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C)

Characteristic	Symbol	MC1709C Min	MC1709C Typ	MC1709C Max	Unit
Input Offset Voltage ($R_S \leq 10$ kΩ, 9.0 V ≤ 15 V, -9.0 V ≥ $V_{EE} \geq$ -15 V)	V_{IO}	–	2.0	7.5	mV
Input Offset Current	I_{IO}	–	100	500	nA
Input Bias Current	I_{IB}	–	300	1500	nA
Input Resistance	r_i	50	250	–	kΩ
Output Resistance	r_o	–	150	–	Ω
Power Consumption	P_C	–	80	200	mW
Large Signal Voltage Gain ($R_L \geq$ 2.0 kΩ, V_O = ±10 V)	A_V	15	45	–	V/mV
Output Voltage Range ($R_L \geq$ 10 kΩ) ($R_L \geq$ 2.0 kΩ)	V_{OR}	±12 ±10	±14 ±13	– –	V
Input Common-Mode Voltage Range	V_{ICR}	±8.0	±10	–	V
Common Mode Rejection Ratio ($R_S \leq$ 10 kΩ)	CMRR	65	90	–	dB
Supply Voltage Rejection Ratio ($R_S \leq$ 10 kΩ)	PSRR	–	25	200	μV/V
Transient Response See Figure 8 Rise Time Overshoot	t_{TLH} OS	– –	0.3 10	– –	μs %

ELECTRICAL CHARACTERISTICS (unless otherwise specified, V_{CC} = +15 V, V_{EE} = −15 V, T_A = 0°C to 70°C)

Parameter	Symbol	MC1709C Min	MC1709C Typ	MC1709C Max	Unit
Input Offset Voltage ($R_S \leq$ 10 kΩ, 9.0 V ≤ $V_{CC} \leq$ 15 V, -9.0 V ≥ $V_{EE} \geq$ 15 V)	V_{IO}	–	–	10	mV
Input Offset Current	I_{IO}	–	–	750	nA
Input Bias Current	I_{IB}	–	–	2.0	μA
Large Signal Voltage Gain ($R_L \geq$ 2.0 kΩ, V_O = ±10 V)	A_V	12	–	–	V/mV
Input Resistance	r_i	35	–	–	kΩ

TYPICAL CHARACTERISTICS

FIGURE 2 – TEST CIRCUIT
(V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C)

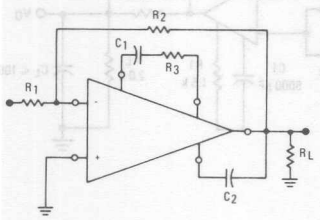


Fig. No.	Curve No.	Test Conditions R_1 (Ω)	R_2 (Ω)	R_3 (Ω)	C_1 (pF)	C_2 (pF)
3	1	10 k	10 k	1.5 k	5.0 k	200
	2	10 k	100 k	1.5 k	500	20
	3	10 k	1.0 M	1.5 k	100	3.0
	4	1.0 k	1.0 M	0	10	3.0
4	1	1.0 k	1.0 M	0	10	3.0
	2	10 k	1.0 M	1.5 k	100	3.0
	3	10 k	100 k	1.5 k	500	20
	4	10 k	10 k	1.5 k	5.0 k	200
5	1	0	∞	1.5 k	5.0 k	200
	2	0	∞	1.5 k	500	20
	3	0	∞	1.5 k	100	3.0
	4	0	∞	0	10	3.0

FIGURE 3 – LARGE SIGNAL SWING versus FREQUENCY

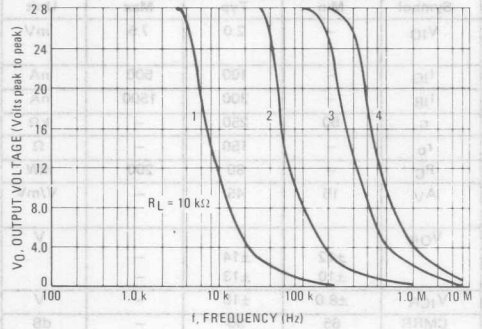


FIGURE 4 – CLOSED LOOP VOLTAGE GAIN versus FREQUENCY

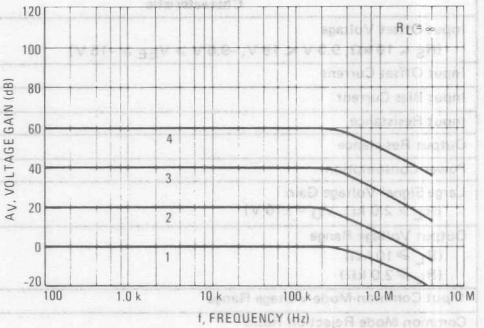


FIGURE 5 – OPEN LOOP VOLTAGE GAIN versus FREQUENCY

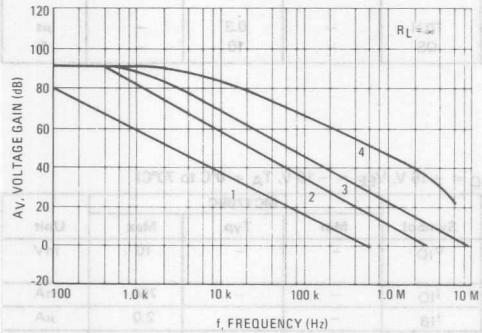


FIGURE 6 – VOLTAGE GAIN versus POWER SUPPLY VOLTAGE

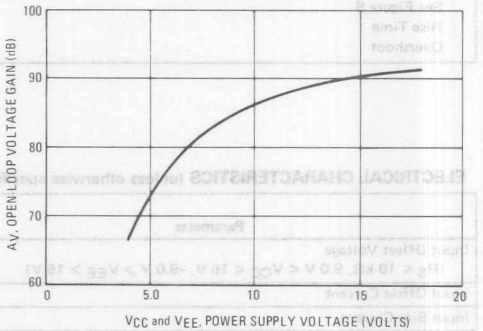


FIGURE 7 – SLEW RATE versus CLOSED LOOP GAIN USING RECOMMENDED COMPENSATION NETWORKS

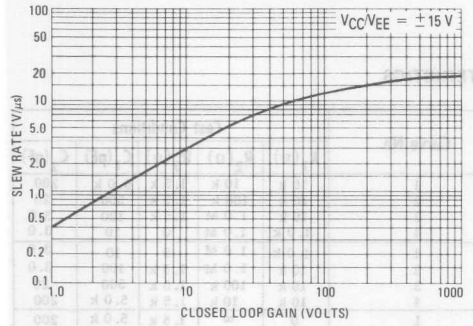
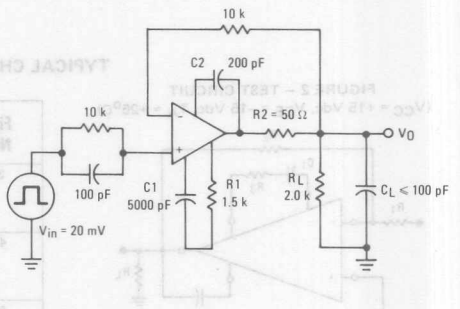


FIGURE 8 – TRANSIENT RESPONSE TEST CIRCUIT



ORDERING INFORMATION

Device	Temperature Range	Package
MC1733G	−55°C to +125°C	Metal Can
MC1733L	−55°C to +125°C	Ceramic DIP
MC1733CG	0°C to +70°C	Metal Can
MC1733CL	0°C to +70°C	Ceramic DIP
MC1733CP	0°C to +70°C	Plastic DIP

MC1733
MC1733C

DIFFERENTIAL VIDEO AMPLIFIER

. . . a wideband amplifier with differential input and differential output. Gain is fixed at 10, 100, or 400 without external components or, with the addition of one external resistor, gain becomes adjustable from 10 to 400.

- Bandwidth – 120 MHz typical @ A_{vd} = 10
- Rise Time – 2.5 ns typical @ A_{vd} = 10
- Propagation Delay Time – 3.6 ns typical @ A_{vd} = 10

DIFFERENTIAL VIDEO WIDEBAND AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

FIGURE 1 – BASIC CIRCUIT

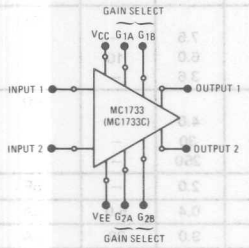


FIGURE 2 – VOLTAGE GAIN ADJUST CIRCUIT

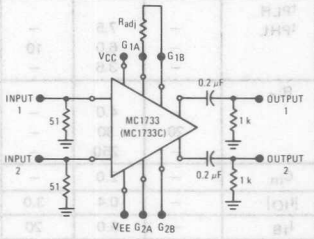
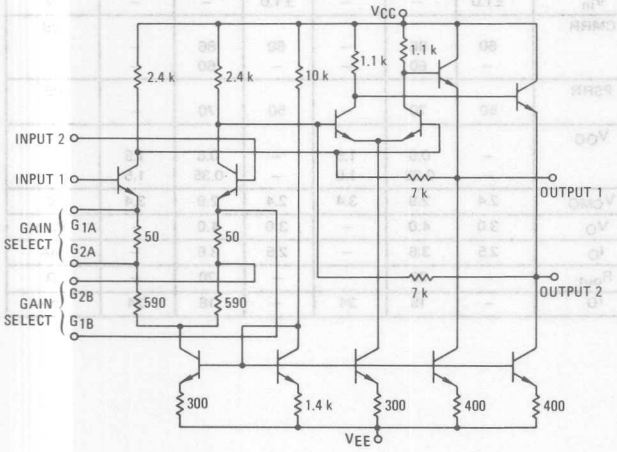
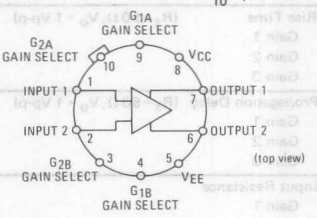


FIGURE 3 – EQUIVALENT CIRCUIT SCHEMATIC

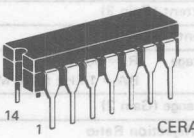


G SUFFIX
METAL PACKAGE
CASE 603-04



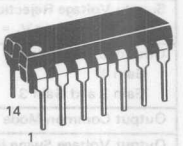


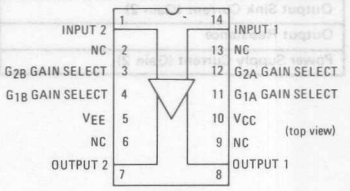
(Top View)



L SUFFIX
CERAMIC PACKAGE
CASE 632-08

P SUFFIX
PLASTIC PACKAGE
CASE 646-06





(Top View)

2

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+8.0 -8.0	Volts
Differential Input Voltage	V_{in}	±5.0	Volts
Common-Mode Input Voltage	V_{ICM}	±6.0	Volts
Output Current	I_O	10	mA
Internal Power Dissipation (Note 1) Metal Can Package Ceramic Dual In-Line Package	P_D	 500 500	mW
Operating Temperature Range MC1733C MC1733	T_A	0 to +70 -55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +6.0 Vdc, V_{EE} = -6.0 Vdc, at T_A = +25°C unless otherwise noted.)

		MC1733			MC1733C			
Characteristic	Symbol	Min	Typ	Max	Min	Typ	Max	Units
Differential Voltage Gain								V/V
Gain 1 (Note 2)	A_{vd}	300	400	500	250	400	600	
Gain 2 (Note 3)		90	100	110	80	100	120	
Gain 3 (Note 4)		9.0	10	11	8.0	10	12	
Bandwidth (R_s = 50 Ω)	BW							MHz
Gain 1		–	40	–	–	40	–	
Gain 2		–	90	–	–	90	–	
Gain 3		–	120	–	–	120	–	
Rise Time (R_s = 50 Ω, V_o = 1 Vp-p)	t_{TLH}							ns
Gain 1	t_{THL}	–	10.5	–	–	10.5	–	
Gain 2		–	4.5	10	–	4.5	12	
Gain 3		–	2.5	–	–	2.5	–	
Propagation Delay (R_s = 50 Ω, V_o = 1 Vp-p)	t_{PLH}							ns
Gain 1	t_{PHL}	–	7.5	–	–	7.5	–	
Gain 2		–	6.0	10	–	6.0	10	
Gain 3		–	3.6	–	–	3.6	–	
Input Resistance	R_{in}							kΩ
Gain 1		–	4.0	–	–	4.0	–	
Gain 2		20	30	–	10	30	–	
Gain 3		–	250	–	–	250	–	
Input Capacitance (Gain 2)	C_{in}	–	2.0	–	–	2.0	–	pF
Input Offset Current (Gain 3)	$\|I_{IO}\|$	–	0.4	3.0	–	0.4	5.0	μA
Input Bias Current (Gain 3)	I_{IB}	–	9.0	20	–	9.0	30	μA
Input Noise Voltage (R_s = 50 Ω, BW = 1 kHz to 10 MHz)	V_n	–	12	–	–	12	–	μV(rms)
Input Voltage Range (Gain 2)	V_{in}	±1.0	–	–	±1.0	–	–	V
Common-Mode Rejection Ratio	CMRR							dB
Gain 2 (V_{CM} = ±1 V, f ≤ 100 kHz)		60	86	–	60	86	–	
Gain 2 (V_{CM} = ±1 V, f = 5 MHz)		–	60	–	–	60	–	
Supply Voltage Rejection Ratio	PSRR							dB
Gain 2 (ΔV_s = ±0.5 V)		50	70	–	50	70	–	
Output Offset Voltage	V_{OO}							V
Gain 1		–	0.6	1.5	–	0.6	1.5	
Gain 2 and Gain 3		–	0.35	1.0	–	0.35	1.5	
Output Common-Mode Voltage (Gain3)	V_{CMO}	2.4	2.9	3.4	2.4	2.9	3.4	V
Output Voltage Swing (Gain 2)	V_O	3.0	4.0	–	3.0	4.0	–	Vp-p
Output Sink Current (Gain 2)	I_O	2.5	3.6	–	2.5	3.6	–	mA
Output Resistance	R_{out}	–	20	–	–	20	–	Ω
Power Supply Current (Gain 2)	I_D	–	18	24	–	18	24	mA

ELECTRICAL CHARACTERISTICS (V_{CC} = +6.0 Vdc, V_{EE} = -6.0 Vdc, at $T_A = T_{high}$ to T_{low} unless otherwise noted.)*

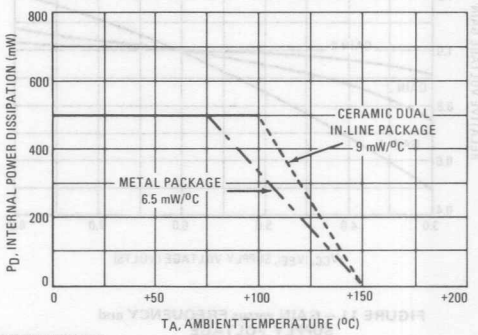
Characteristic	Symbol	MC1733 Min	MC1733 Typ	MC1733 Max	MC1733C Min	MC1733C Typ	MC1733C Max	Units
Differential Voltage Gain	A_{vd}							V/V
Gain 1 (Note 2)		200	–	600	250	–	600	
Gain 2 (Note 3)		80	–	120	80	–	120	
Gain 3 (Note 4)		8.0	–	12	8.0	–	12	
Input Resistance Gain 2	R_{in}	8.0	–	–	8.0	–	–	kΩ
Input Offset Current (Gain 3)	$\|I_{IO}\|$	–	–	5.0	–	–	6.0	μA
Input Bias Current (Gain 3)	I_{IB}	–	–	40	–	–	40	μA
Input Voltage Range (Gain 2)	V_{in}	±1.0	–	–	±1.0	–	–	V
Common-Mode Rejection Ratio Gain 2 (V_{CM} = ±1 V, f ≤ 100 kHz)	CMRR	50	–	–	50	–	–	dB
Supply Voltage Rejection Ratio Gain 2 (ΔV_s = ±0.5 V)	PSRR	50	–	–	50	–	–	dB
Output Offset Voltage	V_{OO}							V
Gain 1		–	–	1.5	–	–	1.5	
Gain 2 and Gain 3		–	–	1.2	–	–	1.5	
Output Voltage Swing (Gain 2)	V_O	2.5	–	–	2.5	–	–	Vp-p
Output Sink Current (Gain 2)	I_O	2.2	–	–	2.5	–	–	mA
Power Supply Current (Gain 2)	I_D	–	–	27	–	–	27	mA

*T_{low} = 0°C for MC1733C, -55°C for MC1733
T_{high} = +70°C for MC1733C, +125°C for MC1733.

NOTES

Note 1: Derate metal package at 6.5 mW/°C for operation at ambient temperatures above 75°C and dual in-line package at 9 mW/°C for operation at ambient temperatures above 100°C (see Figure 4). If operation at high ambient temperatures is required (MC1733) a heatsink may be necessary to limit maximum junction temperature to 150°C. Thermal resistance, junction-to-case, for the metal package is 69.4°C per Watt.
Note 2: Gain Select pins G_{1A} and G_{1B} connected together.
Note 3: Gain Select pins G_{2A} and G_{2B} connected together.
Note 4: All Gain Select pins open.

FIGURE 4 – MAXIMUM ALLOWABLE POWER DISSIPATION



TYPICAL CHARACTERISTICS

(V_{CC} = +6.0 Vdc, V_{EE} = -6.0 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 5 – SUPPLY CURRENT versus TEMPERATURE

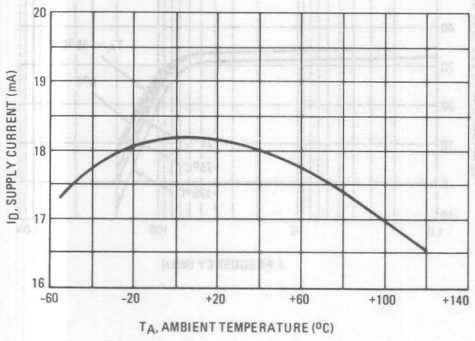


FIGURE 6 – SUPPLY CURRENT versus SUPPLY VOLTAGE

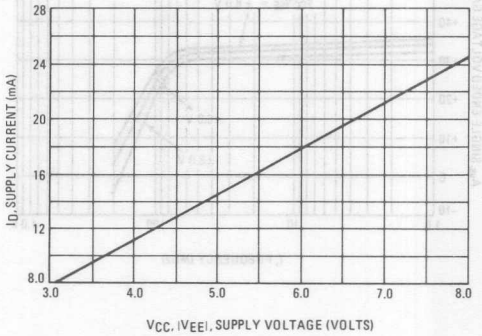


FIGURE 7 – GAIN versus TEMPERATURE

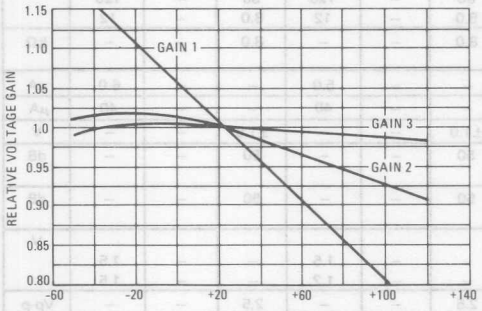


FIGURE 8 – GAIN versus FREQUENCY

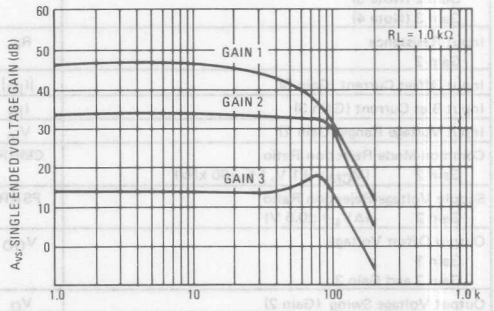


FIGURE 9 – GAIN versus SUPPLY VOLTAGE

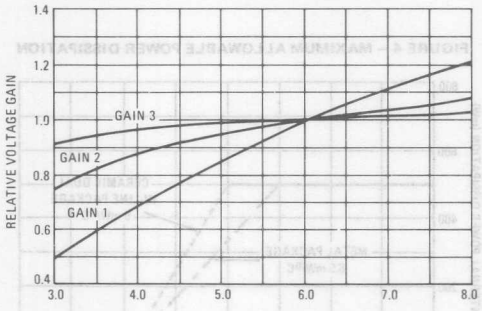


FIGURE 10 – GAIN versus R_{ADJUST}

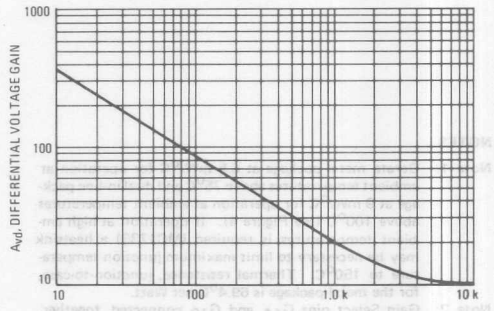


FIGURE 11 – GAIN versus FREQUENCY and SUPPLY VOLTAGE

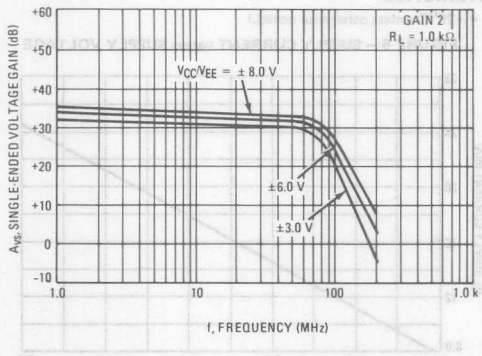
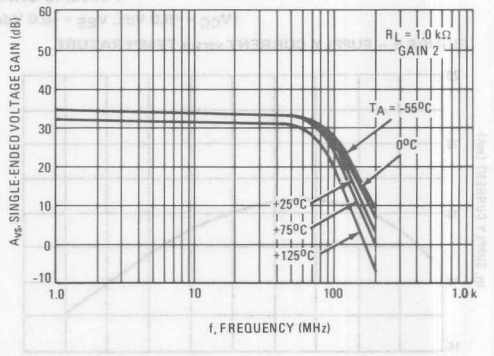


FIGURE 12 – GAIN versus FREQUENCY and TEMPERATURE



TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +6.0 Vdc, V_{EE} = -6.0 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 13 – PULSE RESPONSE versus GAIN

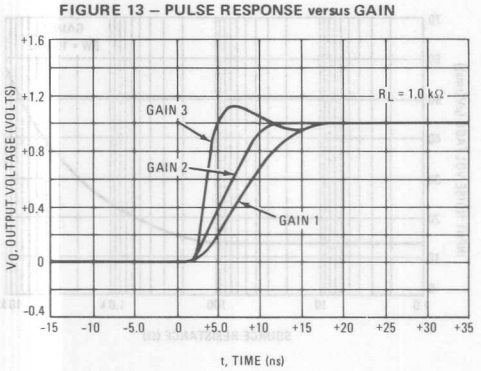


FIGURE 14 – PULSE RESPONSE versus SUPPLY VOLTAGE

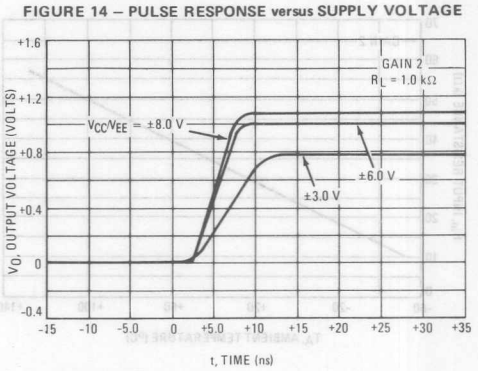


FIGURE 15 – PULSE RESPONSE versus TEMPERATURE

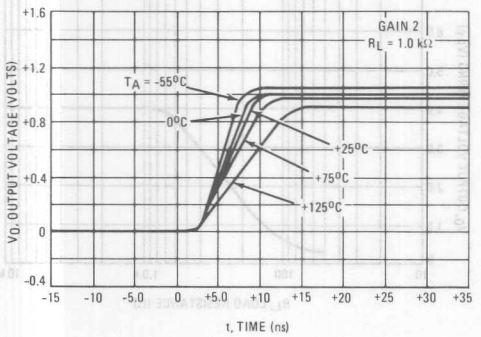


FIGURE 16 – DIFFERENTIAL OVERDRIVE RECOVERY TIME

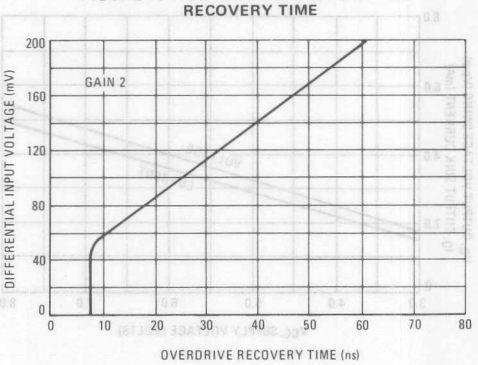


FIGURE 17 – PHASE SHIFT versus FREQUENCY

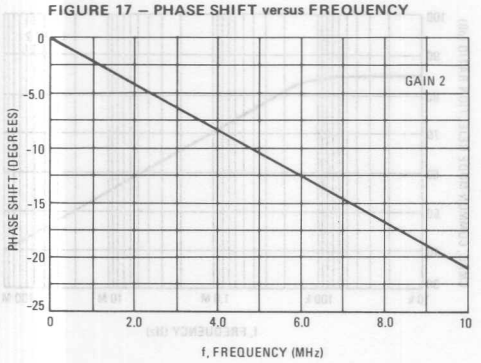
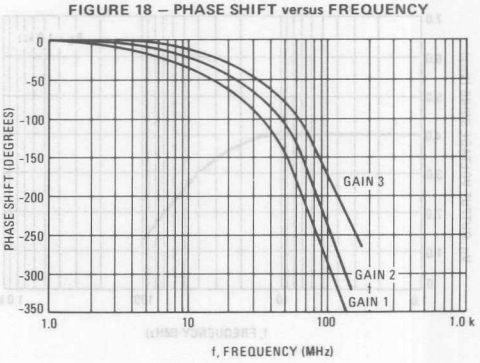


FIGURE 18 – PHASE SHIFT versus FREQUENCY



2

TYPICAL CHARACTERISTICS (Continued)

(V_{CC} = +6.0 Vdc, V_{EE} = -6.0 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 19 – INPUT RESISTANCE versus TEMPERATURE

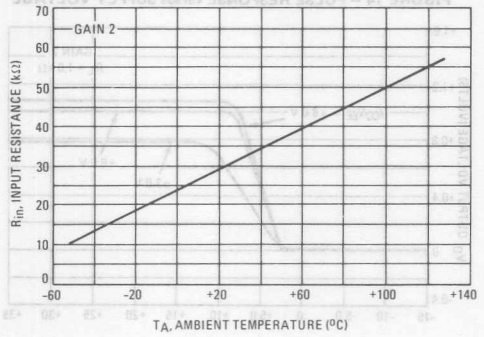


FIGURE 20 – INPUT NOISE VOLTAGE

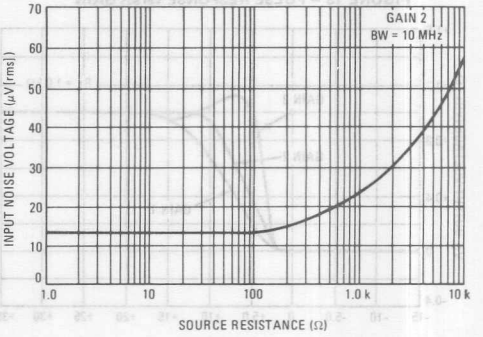


FIGURE 21 – OUTPUT VOLTAGE SWING and SINK CURRENT versus SUPPLY VOLTAGE

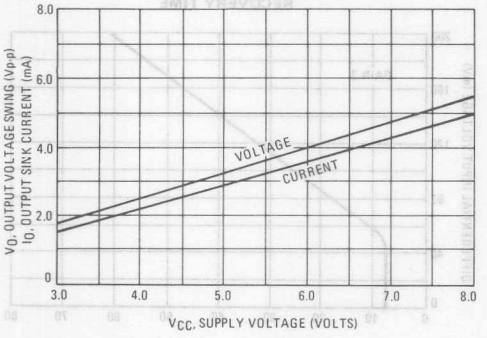


FIGURE 22 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

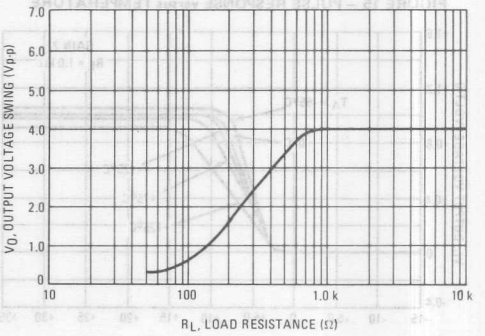


FIGURE 23 – OUTPUT VOLTAGE SWING versus FREQUENCY

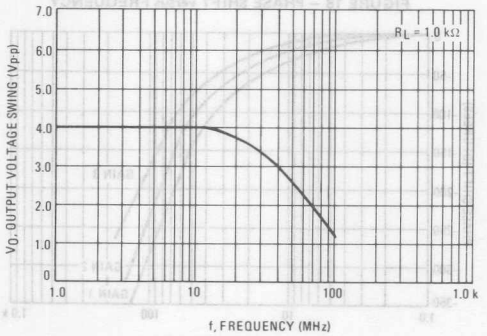
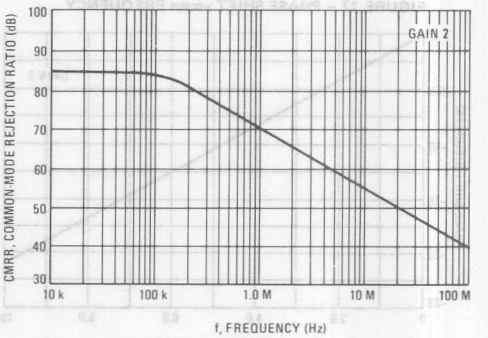
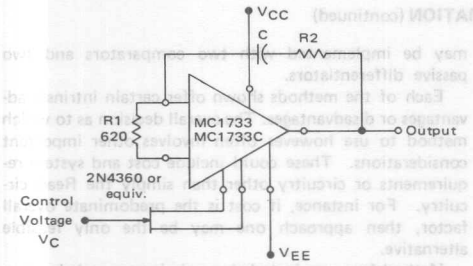


FIGURE 24 – COMMON-MODE REJECTION RATIO



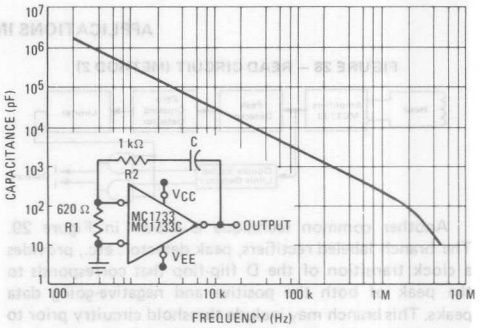
APPLICATIONS INFORMATION

FIGURE 25 – VOLTAGE CONTROLLED OSCILLATOR



By changing the voltage V_C the gain will vary over a range of 10 to 400. This will give a frequency variation about the value set by the capacitor and shown in Figure 26.

FIGURE 26 – OSCILLATOR FREQUENCY FOR VARIOUS CAPACITOR VALUES



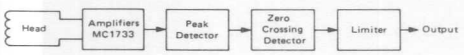
TAPE, DRUM OR DISC MEMORY READ AMPLIFIERS

The first of several methods to be discussed is shown in Figure 27. This block diagram describes a simple Read circuit with no threshold circuitry. Each block represents a basic function that must be performed by the Read circuit. The first block, referred to as "amplfiication", increases the level of the signal available from the Read head to a level adequate to drive the peak detector. Obviously, these signal levels will vary depending on factors such as tape speed, whether the system used is disc or tape, and the type of head and the circuitry used. For a representative tape system, levels of 7 to 25 mV for the signal from the Read head and 2 V for the signal to the peak detector are typical. These signal levels are "peak-to-peak" unless otherwise specified. On the basis of the signal levels mentioned above, the overall amplification required is 38 to 49 dB.

How the overall gain requirement is implemented will depend somewhat on the system used. For instance, a tape cassette system with variable tape speed may utilize a first stage for gain and a second stage primarily for gain control. Thus, a typical circuit would utilize 35 dB in the first stage and 10 to 15 dB in the second stage.

Devices suitable for use as amplifiers fall into one of two categories, operational amplifiers or wideband video amplifiers. Lower speed equipment with low transfer rates commonly uses low cost operational amplifiers. Examples of these are the MC1741, MC1458, MC1709, and MLM301. Equipment requiring higher transfer rates, such as disc systems normally use wideband amplifiers such as the MC1733. The actual cross-over point where wideband amplifiers are used exclusively varies with equipment design. For purposes of comparison, the MLM301 has slightly less than a 40 dB open-loop gain at 100 kHz; the MC1741, a compensated op-amp, has approximately 20 dB open loop gain at 100 kHz; the MC1733 has approximately 33 dB of gain out to 100 MHz (depending on gain option and loading).

FIGURE 27 – TYPICAL READ CIRCUIT (METHOD 1)



There are a number of ways to implement the peak detector function. However, the simplest and most widely used method is a passive differentiator that generates "zero-crossings" for each of the data peaks in the Read signal.

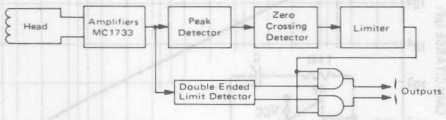
The actual circuitry used to differentiate the Read signal varies from a differential LC type in disc systems to a simple RC type in reel and cassette systems. Either type, of course, attenuates the signal by an amount depending on the circuit used and system specifications. A good approximation of attenuation using the RC type is 20 dB. Thus, the 2 V signal going into the differentiator is reduced to 200 mV.

The next block in Figure 27 to be discussed is the zero-crossing detector. In most cases detection of the zero-crossings is combined with the limiter. These functions serve to generate a TTL compatible pulse waveform with "edges" corresponding to zero-crossings. For low transfer rates, the circuit often used consists of an operational amplifier with series or shunt limiting. For higher transfer rates (greater than 100K B/S) comparators are used.

The method described above is often modified to include threshold sensing. In Figure 28, the function called "double-ended, limit-detector" enables the output NAND gate when either the negative or positive data peaks of the Read signal exceed a predetermined threshold. This function can be implemented in either of two ways. One method first rectifies the signal before it is applied to a comparator with a set threshold. The other method utilizes two comparators, one comparator for positive-going peaks and the other for negative-going peaks. These comparator outputs are then combined in the output logic gates.

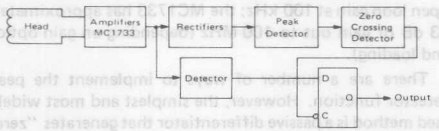
APPLICATIONS INFORMATION (continued)

FIGURE 28 – READ CIRCUIT (METHOD 2)



Another common technique is shown in Figure 29. The branch labeled rectifiers, peak detector, etc., provides a clock transition of the D flip-flop that corresponds to the peak of both the positive and negative-going data peaks. This branch may include threshold circuitry prior to the peak detector. The detector in the lower path detects whether the signal peaks are positive or negative and feeds this data to the flip-flop. This detector can be implemented using a comparator with pre-set threshold.

FIGURE 29 – READ CIRCUIT (METHOD 3)

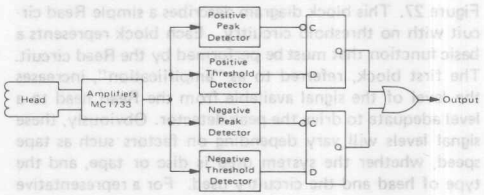


The technique shown in Figure 30 uses separate circuits with threshold provisions for both negative and positive peaks. The peak detectors and threshold detectors may be implemented with two comparators and two passive differentiators.

Each of the methods shown offer certain intrinsic advantages or disadvantages. The overall decision as to which method to use however often involves other important considerations. These could include cost and system requirements or circuitry other than simply the Read circuitry. For instance, if cost is the predominate overall factor, then approach one may be the only feasible alternative.

Method four was included as a design example because it illustrates several unique advantages. First, it uses threshold sensing to reduce noise peak errors. Second, it may be implemented using only integrated circuits. Third, it offers separate, direct threshold sensing for both positive and negative peaks.

FIGURE 30 – READ CIRCUIT (Method 4)



MC1741CG	LM741CH, μA741HC	0°C to +70°C	Metal Can
MC1741CP1	LM741CN, μA741TC	0°C to +70°C	Plastic DIP
MC1741CU	—	0°C to +70°C	Ceramic DIP
MC1741G	—	−55°C to +125°C	Metal Can
MC1741U	—	−55°C to +125°C	Ceramic DIP

MC1741C

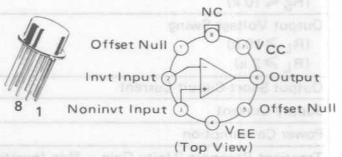
INTERNALLY COMPENSATED, HIGH PERFORMANCE OPERATIONAL AMPLIFIERS

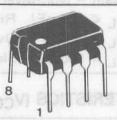
. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- No Frequency Compensation Required
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up

OPERATIONAL AMPLIFIER
SILICON MONOLITHIC
INTEGRATED CIRCUIT

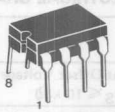
G SUFFIX
METAL PACKAGE
CASE 601-04





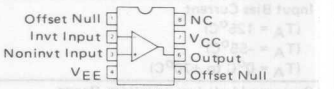
P1 SUFFIX
PLASTIC PACKAGE
CASE 626-05

U SUFFIX
CERAMIC PACKAGE
CASE 693-02





D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SO-8

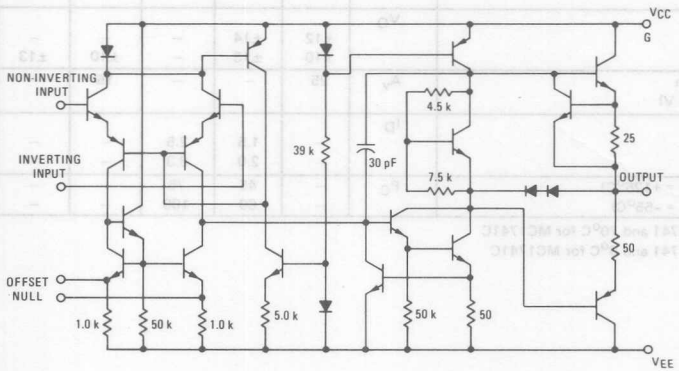


MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	MC1741C	MC1741	Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 −18	+22 −22	Vdc Vdc
Input Differential Voltage	V_{ID}	±30		Volts
Input Common Mode Voltage (Note 1)	V_{ICM}	±15		Volts
Output Short Circuit Duration (Note 2)	t_S	Continuous		
Operating Ambient Temperature Range	T_A	0 to +70	−55 to +125	°C
Storage Temperature Range Metal and Ceramic Packages Plastic Packages	T_{stg}	 −65 to +150 −55 to +125		°C

Note 1. For supply voltages less than +15 V, the absolute maximum input voltage is equal to the supply voltage.
Note 2. Supply voltage equal to or less than 15 V.

EQUIVALENT CIRCUIT SCHEMATIC



2

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C unless otherwise noted).

Characteristic	Symbol	MC1741			MC1741C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10$ k)	V_{IO}	–	1.0	5.0	–	2.0	6.0	mV
Input Offset Current	I_{IO}	–	20	200	–	20	200	nA
Input Bias Current	I_{IB}	–	80	500	–	80	500	nA
Input Resistance	r_i	0.3	2.0	–	0.3	2.0	–	MΩ
Input Capacitance	C_i	–	1.4	–	–	1.4	–	pF
Offset Voltage Adjustment Range	V_{IOR}	–	±15	–	–	±15	–	mV
Common Mode Input Voltage Range	V_{ICR}	±12	±13	–	±12	±13	–	V
Large Signal Voltage Gain (V_O = ±10 V, $R_L \geq 2.0$ k)	A_V	50	200	–	20	200	–	V/mV
Output Resistance	r_o	–	75	–	–	75	–	Ω
Common Mode Rejection Ratio ($R_S \leq 10$ k)	CMRR	70	90	–	70	90	–	dB
Supply Voltage Rejection Ratio ($R_S \leq 10$ k)	PSRR	–	30	150	–	30	150	μV/V
Output Voltage Swing	V_O							V
($R_L \geq 10$ k)		±12	±14	–	±12	±14	–	
($R_L \geq 2$ k)		±10	±13	–	±10	±13	–	
Output Short-Circuit Current	I_{os}	–	20	–	–	20	–	mA
Supply Current	I_D	–	1.7	2.8	–	1.7	2.8	mA
Power Consumption	P_C	–	50	85	–	50	85	mW
Transient Response (Unity Gain – Non-Inverting)								
(V_I = 20 mV, $R_L \geq 2$ k, $C_L \leq 100$ pF) Rise Time	t_{TLH}	–	0.3	–	–	0.3	–	μs
(V_I = 20 mV, $R_L \geq 2$ k, $C_L \leq 100$ pF) Overshoot	os	–	15	–	–	15	–	%
(V_I = 10 V, $R_L \geq 2$ k, $C_L \leq 100$ pF) Slew Rate	SR	–	0.5	–	–	0.5	–	V/μs

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = T_{low} to T_{high} unless otherwise noted).

Characteristic	Symbol	MC1741			MC1741C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10$ kΩ)	V_{IO}	–	1.0	6.0	–	–	7.5	mV
Input Offset Current	I_{IO}							nA
(T_A = 125°C)		–	7.0	200	–	–	–	
(T_A = -55°C)		–	85	500	–	–	–	
(T_A = 0°C to +70°C)		–	–	–	–	–	300	
Input Bias Current	I_{IB}							nA
(T_A = 125°C)		–	30	500	–	–	–	
(T_A = -55°C)		–	300	1500	–	–	–	
(T_A = 0°C to +70°C)		–	–	–	–	–	800	
Common Mode Input Voltage Range	V_{ICR}	±12	±13	–	–	–	–	V
Common Mode Rejection Ratio ($R_S \leq 10$ k)	CMRR	70	90	–	–	–	–	dB
Supply Voltage Rejection Ratio ($R_S \leq 10$ k)	PSRR	–	30	150	–	–	–	μV/V
Output Voltage Swing	V_O							V
($R_L \geq 10$ k)		±12	±14	–	–	–	–	
($R_L \geq 2$ k)		±10	±13	–	±10	±13	–	
Large Signal Voltage Gain ($R_L \geq 2$ k, V_{out} = ±10 V)	A_V	25	–	–	15	–	–	V/mV
Supply Currents	I_D							mA
(T_A = 125°C)		–	1.5	2.5	–	–	–	
(T_A = -55°C)		–	2.0	3.3	–	–	–	
Power Consumption (T_A = +125°C)	P_C	–	45	75	–	–	–	mW
(T_A = -55°C)		–	60	100	–	–	–	

*T_{high} = 125°C for MC1741 and 70°C for MC1741C
T_{low} = -55°C for MC1741 and 0°C for MC1741C

FIGURE 1 – BURST NOISE versus SOURCE RESISTANCE

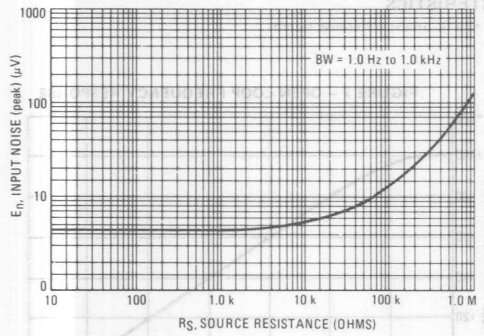


FIGURE 2 – RMS NOISE versus SOURCE RESISTANCE

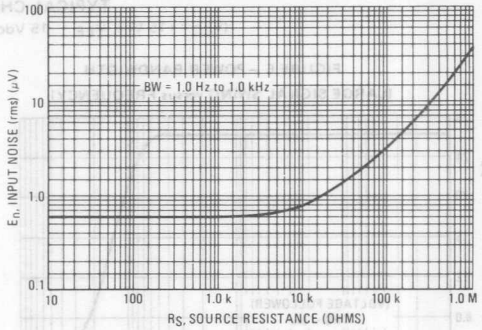


FIGURE 3 – OUTPUT NOISE versus SOURCE RESISTANCE

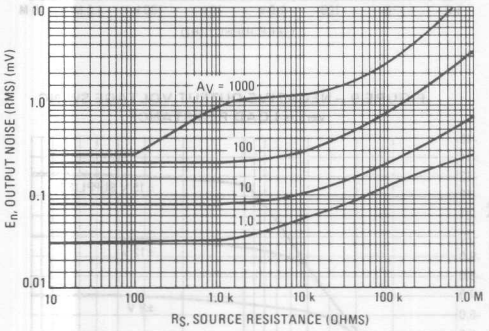


FIGURE 4 – SPECTRAL NOISE DENSITY

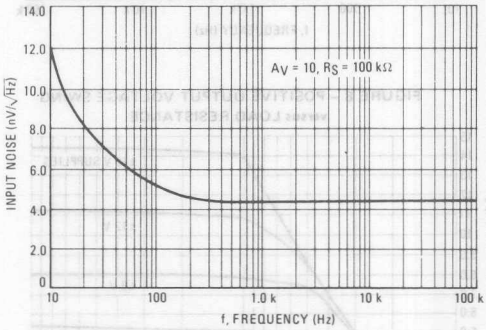
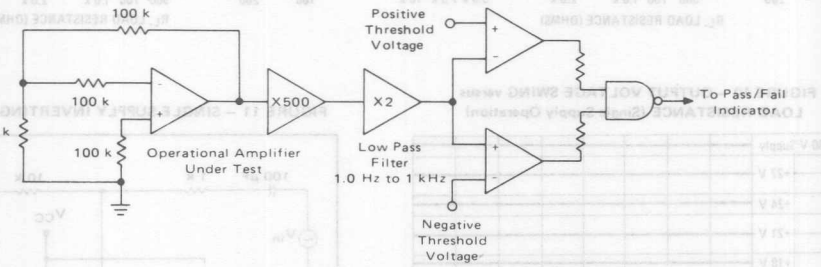


FIGURE 5 – BURST NOISE TEST CIRCUIT



Unlike conventional peak reading or RMS meters, this system was especially designed to provide the quick response time essential to burst (popcorn) noise testing.

The test time employed is 10 seconds and the 20 μV peak limit refers to the operational amplifier input thus eliminating errors in the closed-loop gain factor of the operational amplifier under test.

FIGURE 6 – POWER BANDWIDTH
(LARGE SIGNAL SWING versus FREQUENCY)

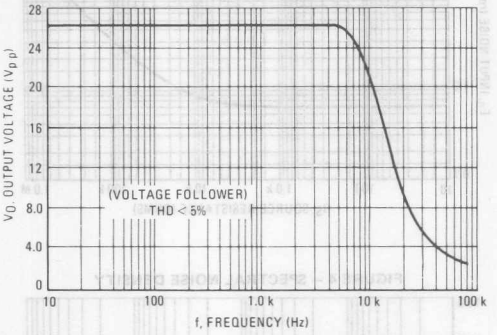


FIGURE 7 – OPEN LOOP FREQUENCY RESPONSE

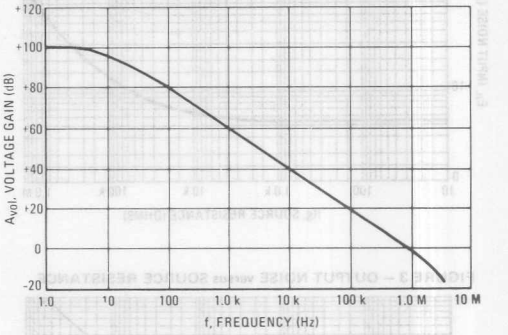


FIGURE 8 – POSITIVE OUTPUT VOLTAGE SWING
versus LOAD RESISTANCE

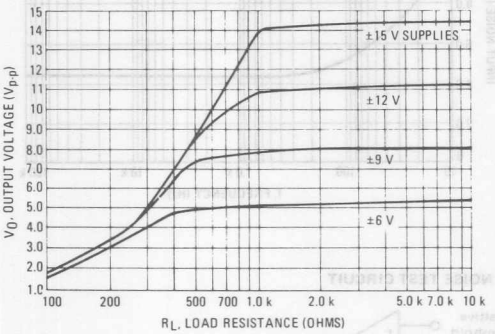


FIGURE 9 – NEGATIVE OUTPUT VOLTAGE SWING
versus LOAD RESISTANCE

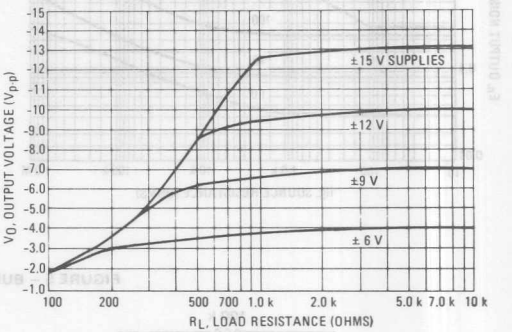


FIGURE 10 – OUTPUT VOLTAGE SWING versus
LOAD RESISTANCE (Single Supply Operation)

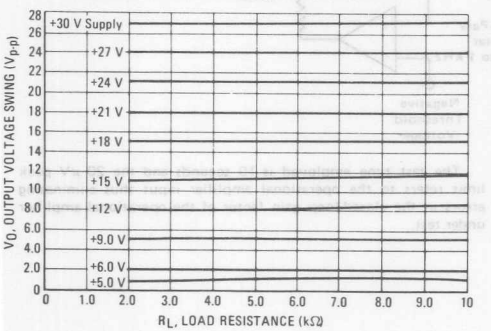


FIGURE 11 – SINGLE SUPPLY INVERTING AMPLIFIER

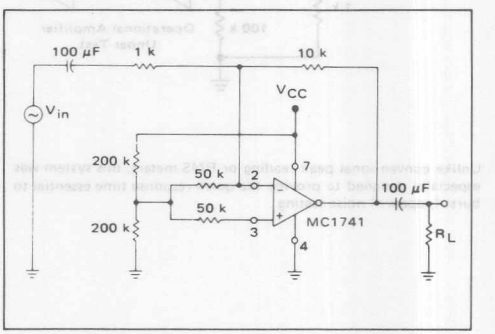


FIGURE 12 — NONINVERTING PULSE RESPONSE

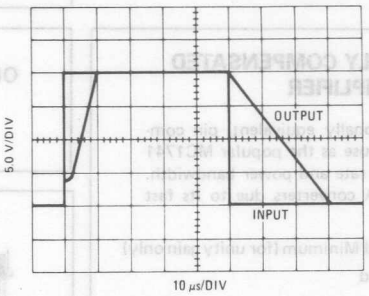


FIGURE 13 — TRANSIENT REPONSE TEST CIRCUIT

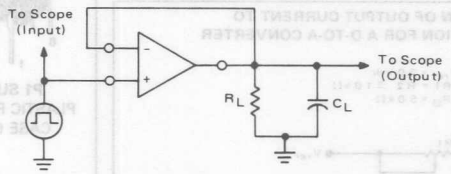
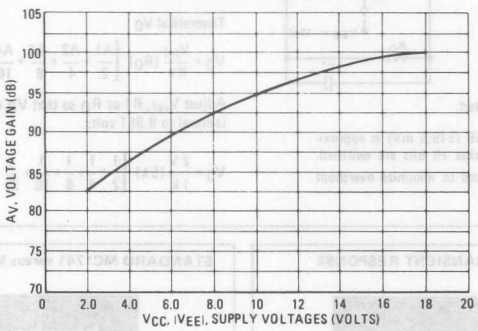


FIGURE 14 — OPEN LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE



MC1741S
MC1741SC

ORDERING INFORMATION

Device	Temperature Range	Package
MC1741SG	−55°C to +125°C	Metal Can
MC1741SCD	0°C to +70°C	SO-8
MC1741SCG	0°C to +70°C	Metal Can
MC1741SCP1	0°C to +70°C	Plastic DIP

HIGH SLEW RATE, INTERNALLY COMPENSATED OPERATIONAL AMPLIFIER

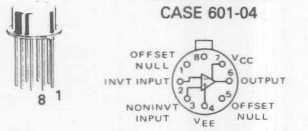
The MC1741S/MC1741SC is functionally equivalent, pin compatible, and possesses the same ease of use as the popular MC1741 circuit, yet offers 20 times higher slew rate and power bandwidth. This device is ideally suited for D-to-A converters due to its fast settling time and high slew rate.

- High Slew Rate — 10 V/μs Guaranteed Minimum (for unity gain only)
- No Frequency Compensation Required
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low Power Consumption
- No Latch-Up

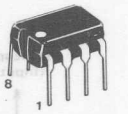
OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

G SUFFIX
METAL PACKAGE
CASE 601-04



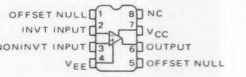
(Top View)



P1 SUFFIX
PLASTIC PACKAGE
CASE 626-05

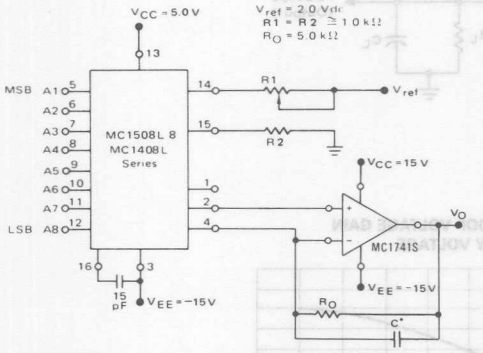


D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SO-8



(Top View)

TYPICAL APPLICATION OF OUTPUT CURRENT TO VOLTAGE TRANSFORMATION FOR A D-TO-A CONVERTER



Pins not shown are not connected.

Settling time to within 1/2 LSB (±19.5 mV) is approximately 4.0 μs from the time that all bits are switched.

*The value of C may be selected to minimize overshoot and ringing (C ≈ 150 pF).

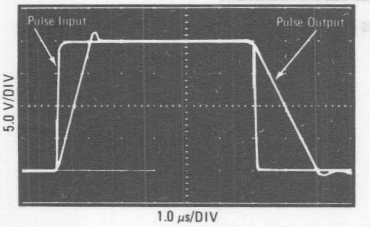
Theoretical V_O

$$V_O = \frac{V_{ref}}{R1}(R_O)\left[\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right]$$

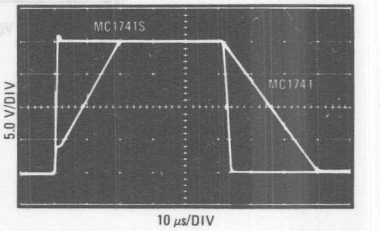
Adjust V_{ref}, R1 or R_O so that V_O with all digital inputs at high level is equal to 9.961 volts.

$$V_O = \frac{2\ V}{1\ k}(5\ k)\left[\frac{1}{2}+\frac{1}{4}+\frac{1}{8}+\frac{1}{16}+\frac{1}{32}+\frac{1}{64}+\frac{1}{128}+\frac{1}{256}\right] = 10\ V\left[\frac{255}{256}\right] = 9.961\ V$$

MC1741S LARGE-SIGNAL TRANSIENT RESPONSE

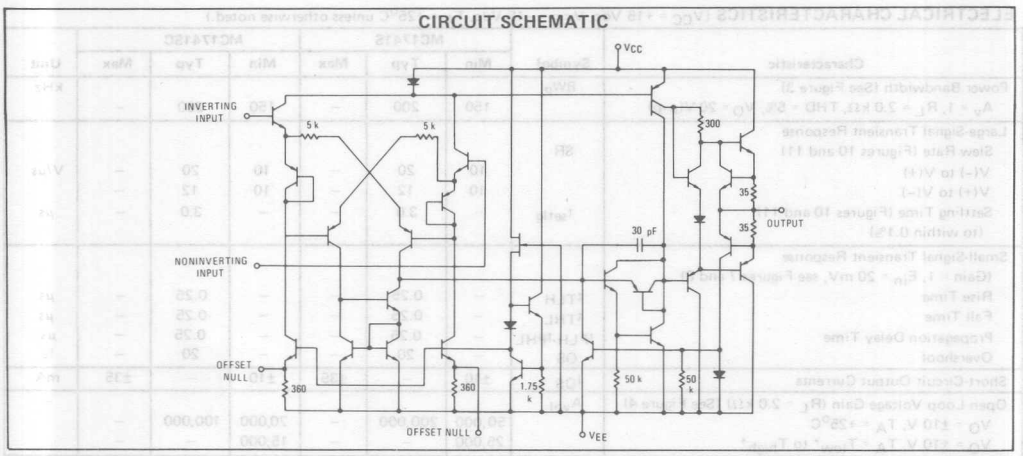


STANDARD MC1741 versus MC1741S RESPONSE COMPARISON



2

CIRCUIT SCHEMATIC



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value MC1741SC	Value MC1741S	Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 -18	+22 -22	Vdc
Differential Input Signal Voltage	V_{ID}	±30		Volts
Common-Mode Input Voltage Swing (See Note 1)	V_{ICR}	±15		Volts
Output Short-Circuit Duration (See Note 2)	t_s	Continuous		
Power Dissipation (Package Limitation)	P_D			
Metal Package		680		mW
Derate above T_A = +25°C		4.6		mW/°C
Plastic Dual In-Line Package		625		mW
Derate above T_A = +25°C		5.0		mW/°C
Operating Ambient Temperature Range	T_A	0 to +75	-55 to +125	°C
Storage Temperature Range	T_{stg}			°C
Metal Package		-65 to +150		
Plastic Package		-55 to +125		

Note 1. For supply voltages less than ±15 Vdc, the absolute maximum input voltage is equal to the supply voltage.
Note 2. Supply voltage equal to or less than 15 Vdc.

FIGURE 1 – OFFSET ADJUST CIRCUIT

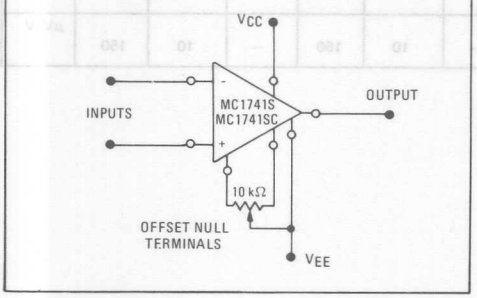
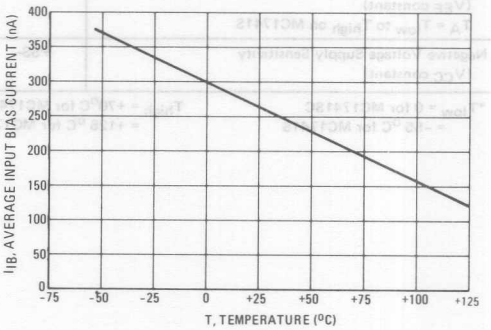


FIGURE 2 – INPUT BIAS CURRENT versus TEMPERATURE



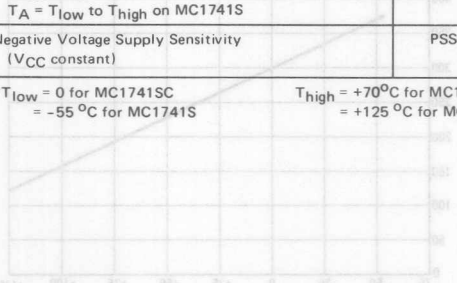
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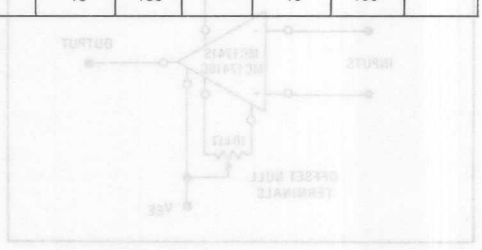
ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC1741S Min	MC1741S Typ	MC1741S Max	MC1741SC Min	MC1741SC Typ	MC1741SC Max	Unit
Power Bandwidth (See Figure 3) A_V = 1, R_L = 2.0 kΩ, THD = 5%, V_O = 20 V(p-p)	BW_P	150	200	–	150	200	–	kHz
Large-Signal Transient Response Slew Rate (Figures 10 and 11) V(-) to V(+) V(+) to V(-) Settling Time (Figures 10 and 11) (to within 0.1%)	SR t_{setlg}	 10 10 –	 20 12 3.0	 – – –	 10 10 –	 20 12 3.0	 – – –	 V/μs μs
Small-Signal Transient Response (Gain = 1, E_{in} = 20 mV, see Figures 7 and 8) Rise Time Fall Time Propagation Delay Time Overshoot	 t_{TLH} t_{THL} t_{PLH},t_{PHL} OS	 – – – –	 0.25 0.25 0.25 20	 – – – –	 – – – –	 0.25 0.25 0.25 20	 – – – –	 μs μs μs %
Short-Circuit Output Currents	I_{OS}	±10	–	±35	±10	–	±35	mA
Open-Loop Voltage Gain (R_L = 2.0 kΩ) (See Figure 4) V_O = ±10 V, T_A = +25°C V_O = ±10 V, T_A = T_{low}* to T_{high}*	A_{vol}	 50,000 25,000	 200,000 –	 – –	 20,000 15,000	 100,000 –	 – –	–
Output Impedance (f = 20 Hz)	z_o	–	75	–	–	75	–	Ω
Input Impedance (f = 20 Hz)	z_i	0.3	1.0	–	0.3	1.0	–	MΩ
Output Voltage Swing R_L = 10 kΩ, T_A = T_{low} to T_{high} (MC1741S only) R_L = 2.0 kΩ, T_A = +25°C R_L = 2.0 kΩ, T_A = T_{low} to T_{high}	V_O	 ±12 ±10 ±10	 ±14 ±13 –	 – – –	 ±12 ±10 ±10	 ±14 ±13 –	 – – –	V_{pk}
Input Common-Mode Voltage Range T_A = T_{low} to T_{high} (MC1741S)	V_{ICR}	±12	±13	–	±12	±13	–	V_{pk}
Common-Mode Rejection Ratio (f = 20 Hz) T_A = T_{low} to T_{high} (MC1741S)	CMRR	70	90	–	70	90	–	dB
Input Bias Current (See Figure 2) T_A = +25°C and T_{high} T_A = T_{low}	I_{IB}	 – –	 200 500	 500 1500	 – –	 200 –	 500 800	nA
Input Offset Current T_A = +25°C and T_{high} T_A = T_{low}	$\|I_{IO}\|$	 – –	 30 –	 200 500	 – –	 30 –	 200 300	nA
Input Offset Voltage (R_S = ⩽10 kΩ) T_A = +25°C T_A = T_{low} to T_{high}	$\|V_{IO}\|$	 – –	 1.0 –	 5.0 6.0	 – –	 2.0 –	 6.0 7.5	mV
DC Power Consumption (See Figure 9) (Power Supply = ±15 V, V_O = 0) T_A = T_{low} to T_{high}	P_C	–	50	85	–	50	85	mW
Positive Voltage Supply Sensitivity (V_{EE} constant) T_A = T_{low} to T_{high} on MC1741S	PSS+	–	2.0	100	–	2.0	150	μV/V
Negative Voltage Supply Sensitivity (V_{CC} constant)	PSS-	–	10	150	–	10	150	μV/V

*T_{low} = 0 for MC1741SC
= -55 °C for MC1741S

T_{high} = +70°C for MC1741SC
= +125 °C for MC1741S





TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 3 – POWER BANDWIDTH – NONDISTORTED OUTPUT VOLTAGE versus FREQUENCY

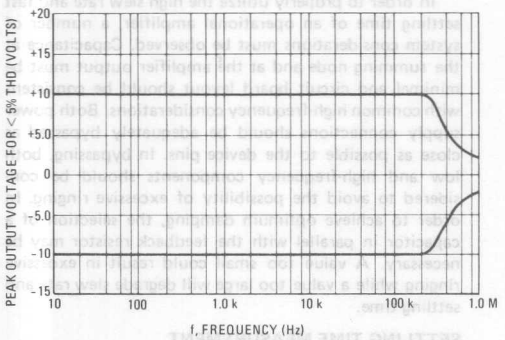


FIGURE 4 – OPEN-LOOP FREQUENCY RESPONSE

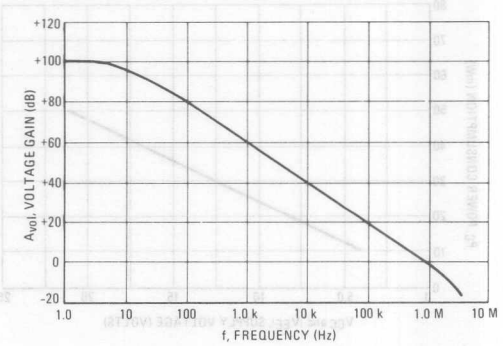


FIGURE 5 – NOISE versus FREQUENCY

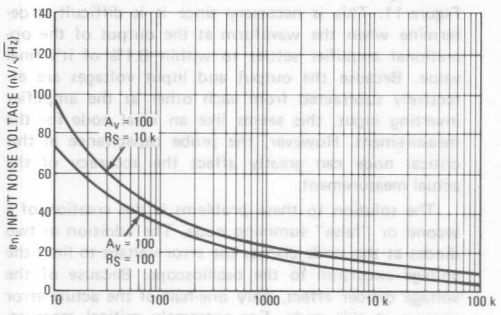


FIGURE 6 – OUTPUT NOISE versus SOURCE RESISTANCE

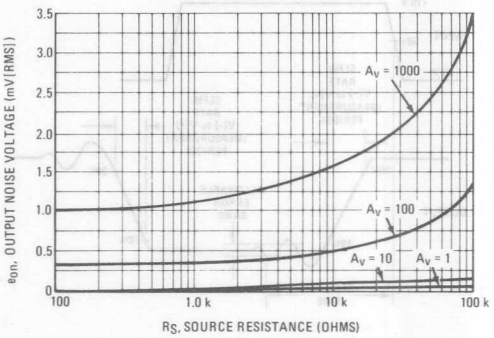


FIGURE 7 – SMALL-SIGNAL TRANSIENT RESPONSE DEFINITIONS

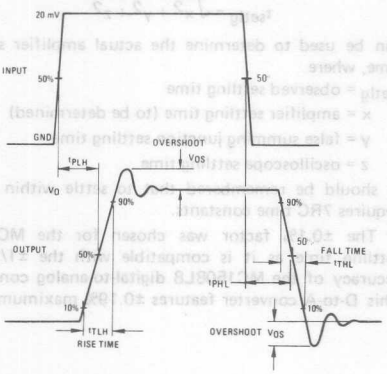
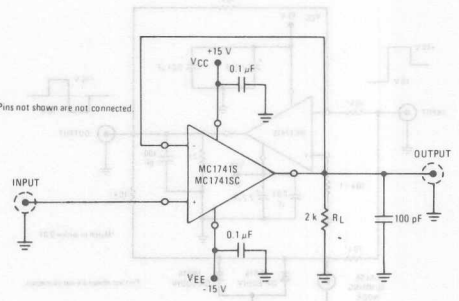


FIGURE 8 – SMALL-SIGNAL TRANSIENT RESPONSE TEST CIRCUIT



TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = −15 Vdc, T_A = +25°C unless otherwise noted.)

2

FIGURE 9 – POWER CONSUMPTION versus POWER SUPPLY VOLTAGES

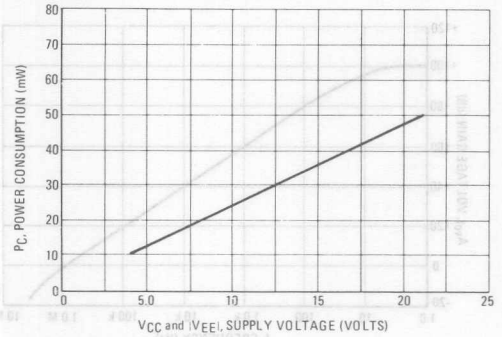


FIGURE 10 – LARGE-SIGNAL TRANSIENT WAVEFORMS

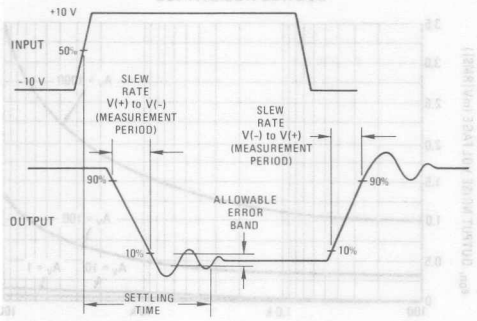
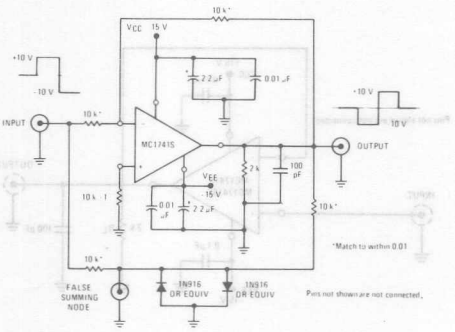


FIGURE 11 – SETTLING TIME AND SLEW RATE TEST CIRCUIT



SETTLING TIME

In order to properly utilize the high slew rate and fast settling time of an operational amplifier, a number of system considerations must be observed. Capacitance at the summing node and at the amplifier output must be minimal and circuit board layout should be consistent with common high-frequency considerations. Both power supply connections should be adequately bypassed as close as possible to the device pins. In bypassing, both low and high-frequency components should be considered to avoid the possibility of excessive ringing. In order to achieve optimum damping, the selection of a capacitor in parallel with the feedback resistor may be necessary. A value too small could result in excessive ringing while a value too large will degrade slew rate and settling time.

SETTLING TIME MEASUREMENT

In order to accurately measure the settling time of an operational amplifier, it is suggested that the "false" summing junction approach be taken as shown in Figure 11. This is necessary since it is difficult to determine when the waveform at the output of the operational amplifier settles to within 0.1% of it's final value. Because the output and input voltages are effectively subtracted from each other at the amplifier inverting input, this seems like an ideal node for the measurement. However, the probe capacitance at this critical node can greatly affect the accuracy of the actual measurement.

The solution to these problems is the creation of a second or "false" summing node. The addition of two diodes at this node clamps the error voltage to limit the voltage excursion to the oscilloscope. Because of the voltage divider effect, only one-half of the actual error appears at this node. For extremely critical measurements, the capacitance of the diodes and the oscilloscope, and the settling time of the oscilloscope must be considered. The expression

$$t_{setlg} = \sqrt{x^2 + y^2 + z^2}$$

can be used to determine the actual amplifier settling time, where

t_{setlg} = observed settling time

x = amplifier settling time (to be determined)

y = false summing junction settling time

z = oscilloscope settling time

It should be remembered that to settle within ±0.1% requires 7RC time constants.

The ±0.1% factor was chosen for the MC1741S settling time as it is compatible with the ±1/2 LSB accuracy of the MC1508L8 digital-to-analog converter. This D-to-A converter features ±0.19% maximum error.

FIGURE 12 – WAVEFORM AT FALSE SUMMING NODE

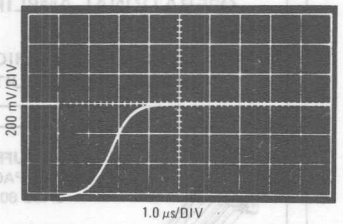
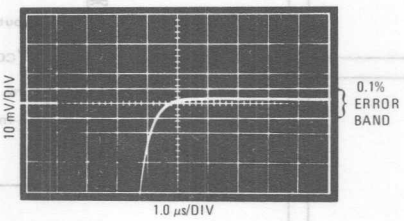
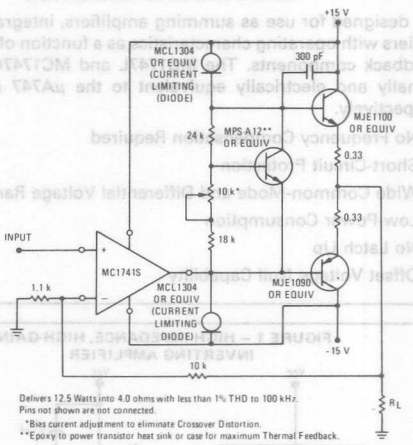


FIGURE 13 – EXPANDED WAVEFORM AT FALSE SUMMING NODE



TYPICAL APPLICATION

FIGURE 14 – 12.5-WATT WIDEBAND POWER AMPLIFIER



Delivers 12.5 Watts into 4.0 ohms with less than 1% THD to 100 kHz.
Pins not shown are not connected.
*Bias current adjustment to eliminate Crossover Distortion.
**Epoxy to power transistor heat sink or case for maximum Thermal Feedback.

MC1747G	−55°C to +125°C	Metal Can
MC1747L	−55°C to +125°C	Ceramic DIP
MC1747CD	0°C to +70°C	SO-14
MC1747CG	0°C to +70°C	Metal Can
MC1747CL	0°C to +70°C	Ceramic DIP
MC1747CP2	0°C to +70°C	Plastic DIP

MC1747
MC1747C

(DUAL MC1741)

INTERNALLY COMPENSATED, HIGH PERFORMANCE OPERATIONAL AMPLIFIER

. . . designed for use as summing amplifiers, integrators, or amplifiers with operating characteristics as a function of the external feedback components. The MC1747L and MC1747CL are functionally and electrically equivalent to the μA747 and μA747C respectively.

- No Frequency Compensation Required
- Short-Circuit Protection
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up
- Offset Voltage Null Capability

FIGURE 1 – HIGH-IMPEDANCE, HIGH-GAIN INVERTING AMPLIFIER

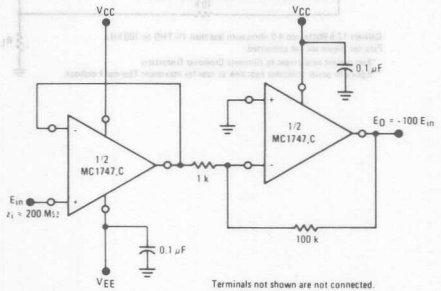
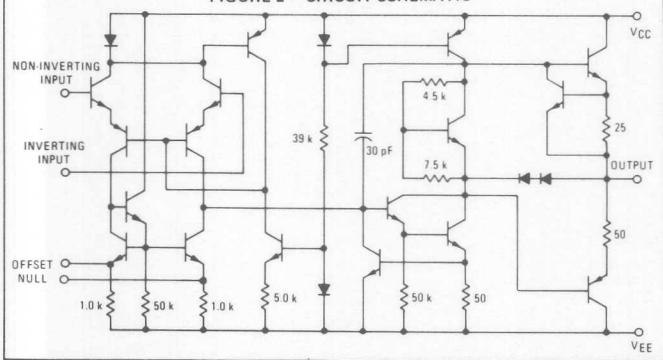


FIGURE 2 – CIRCUIT SCHEMATIC

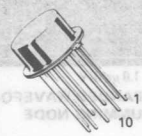


Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent right of Motorola Inc. or others.

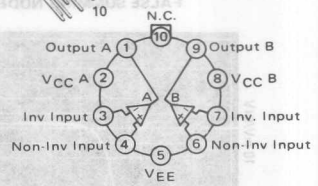
(DUAL MC1741)

DUAL OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

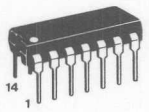


G SUFFIX
METAL PACKAGE
CASE 603-04

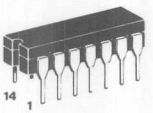


D SUFFIX
PLASTIC PACKAGE
CASE 751A-02
SO-14

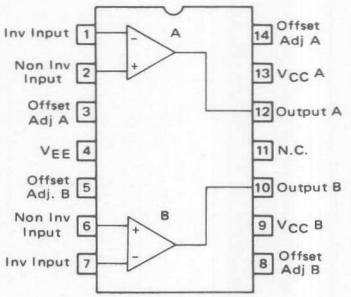




P2 SUFFIX
PLASTIC PACKAGE
CASE 646-06



L SUFFIX
CERAMIC PACKAGE
CASE 632-08



VCCA and VCCB are not connected internally.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	MC1747	MC1747C	Unit
Power Supply Voltages	V_{CC}	+22	+18	Vdc
	V_{EE}	-22	-18	
Differential Input Signal Voltage ①	V_{ID}	± 30		Volts
Common-Mode Input Swing Voltage ②	V_{ICR}	± 15		Volts
Output Short-Circuit Duration	t_{OS}	Continuous		
Voltage (Measurement between Offset Null and V_{EE})		± 0.5		Volts
Operating Ambient Temperature Range	T_A	-55 to +125	0 to + 70	°C
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	°C
Junction Temperature Ceramic and Metal Package Plastic Package	T_J	175 150		°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted.)

Characteristics	Symbol	MC1747 Min	MC1747 Typ	MC1747 Max	MC1747C Min	MC1747C Typ	MC1747C Max	Unit
Input Bias Current	I_{IB}							nAdc
T_A = +25°C		–	80	500	–	80	500	
T_A = T_{high} ③		–	30	500	–	30	800	
T_A = T_{low} ③		–	300	1500	–	30	800	
Input Offset Current	I_{IO}							nAdc
T_A = +25°C		–	20	200	–	20	200	
T_A = T_{high}		–	7.0	200	–	7.0	300	
T_A = T_{low}		–	85	500	–	7.0	300	
Input Offset Voltage ($R_S \leq 10\ k\Omega$)	V_{IO}							mVdc
T_A = +25°C		–	1.0	5.0	–	1.0	6.0	
T_A = T_{low} to T_{high}		–	1.0	6.0	–	1.0	7.5	
Offset Voltage Adjustment Range		–	± 15	–	–	± 15	–	mV
Differential Input Impedance (Open-loop, f = 20 Hz)								
Parallel Input Resistance	r_i	0.3	2.0	–	0.3	2.0	–	MΩ
Parallel Input Capacitance	C_i	–	1.4	–	–	1.4	–	pF
Common-Mode Input Voltage Swing	V_{ICR}							Volts
$T_{low} \leq T_A \leq T_{high}$		± 12	± 13	–	± 12	± 13	–	
Common-Mode Rejection Ratio (R_S = 10 kΩ)	CMRR							dB
$T_{low} \leq T_A \leq T_{high}$		70	90	–	70	90	–	
Open-Loop Voltage Gain	A_{vol}							Volts
T_A = +25°C (V_O = ±10 V, R_L = 2.0 kΩ)		50,000	200,000	–	25,000	200,000	–	
T_A = T_{low} to T_{high} (V_O = ±10 V, R_L = 2.0 kΩ)		25,000	–	–	15,000	–	–	
Transient Response (Unity Gain) (V_{in} = 20 mV, R_L = 2.0 kΩ, $C_L \leq$ 100 pF)								
Rise Time	t_{PLH}	–	0.3	–	–	0.3	–	μs
Overshoot Percentage		–	5.0	–	–	5.0	–	%
Slew Rate (Unity Gain)	SR	–	0.5	–	–	0.5	–	V/μs
Output Impedance	z_o	–	75	–	–	75	–	ohms
Short-Circuit Output Current	I_{OS}	–	25	–	–	25	–	mAdc
Channel Separation		–	120	–	–	120	–	dB
Output Voltage Swing ($T_{low} \leq T_A \leq T_{high}$)	V_{OR}							V_{pk}
R_L = 10 kΩ		± 12	± 14	–	± 12	± 14	–	
R_L = 2.0 kΩ		± 10	± 13	–	± 10	± 13	–	
Power Supply Sensitivity (T_{low} to T_{high})								μV/V
V_{EE} = Constant, $R_S \leq$ 10 kΩ	PSS+	–	30	150	–	30	150	
V_{CC} = Constant, $R_S \leq$ 10 kΩ	PSS-	–	30	150	–	30	150	
Power Supply Current (each amplifier)	I_{CC},I_{EE}							mAdc
T_A = +25°C		–	1.7	2.8	–	1.7	2.8	
T_A = T_{low}		–	2.0	3.3	–	2.0	3.3	
T_A = T_{high}		–	1.5	2.5	–	2.0	3.3	
DC Power Consumption (each amplifier)	P_C							mW
T_A = +25°C		–	50	85	–	50	85	
T_A = T_{low}		–	60	100	–	60	100	
T_A = T_{high}		–	45	75	–	60	100	

① For supply voltages of less than ±15 V, the maximum differential input voltage is equal to ± (V_{CC} + $|V_{EE}|$).
② For supply voltages of less than ±15 V, the maximum input voltage is equal to the supply voltage (+V_{CC}, -$|V_{EE}|$).
③ T_{low} : 0°C for MC1747CL
-55°C for MC1747L
T_{high}: +70°C for MC1747CL
+125°C for MC1747L

2

FIGURE 3 – TYPICAL FREQUENCY-SHIFT KEYER TONE GENERATOR TEST CIRCUIT

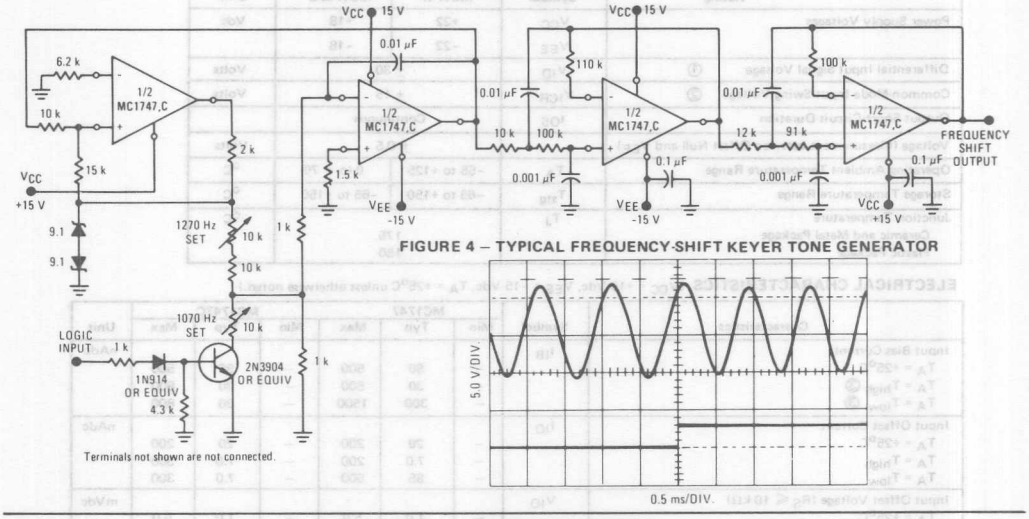


FIGURE 4 – TYPICAL FREQUENCY-SHIFT KEYER TONE GENERATOR

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = −15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 5 – OPEN-LOOP VOLTAGE GAIN versus POWER-SUPPLY VOLTAGE

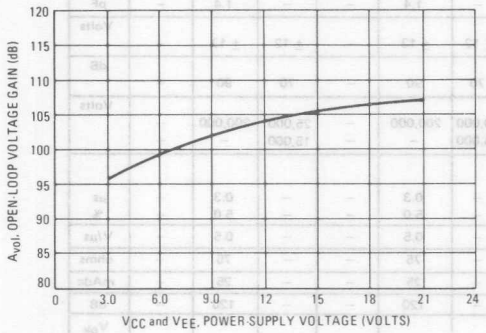


FIGURE 6 – OPEN-LOOP FREQUENCY RESPONSE

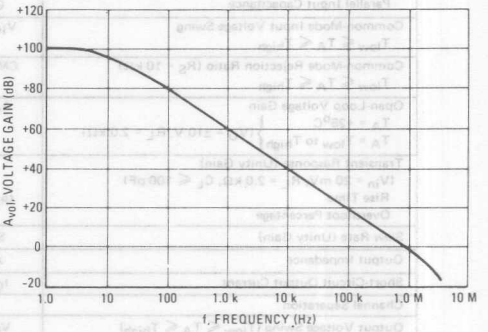


FIGURE 7 – POWER BANDWIDTH (LARGE SIGNAL SWING versus FREQUENCY)

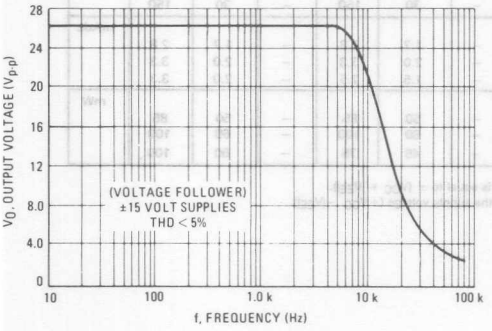
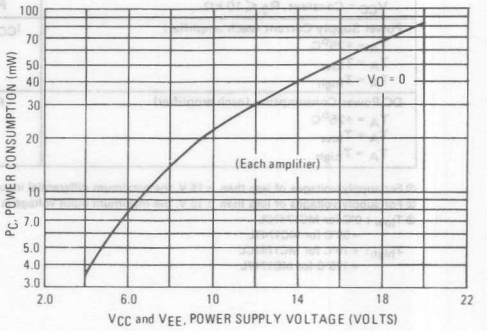


FIGURE 8 – POWER CONSUMPTION versus POWER SUPPLY VOLTAGE



TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +15 Vdc, V_{EE} = −15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 9 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

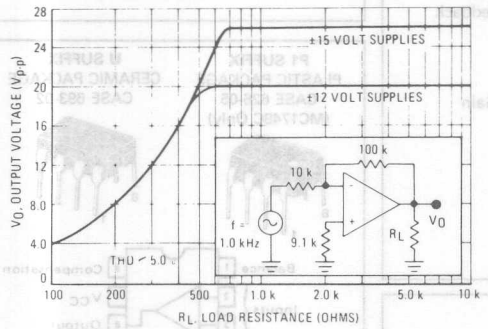
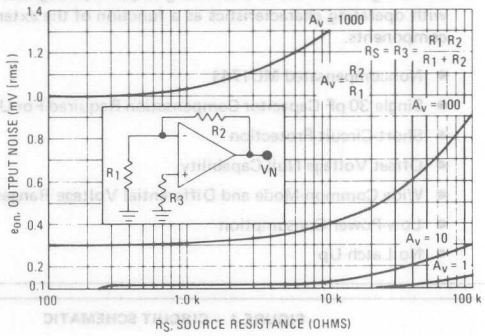


FIGURE 10 – OUTPUT NOISE versus SOURCE RESISTANCE



MC1748CG	0°C to +70°C	Metal Can
MC1748CP1	0°C to +70°C	Plastic DIP
MC1748CU	0°C to +70°C	Ceramic DIP

MC1748C

HIGH PERFORMANCE OPERATIONAL AMPLIFIER

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- Noncompensated MC1741
- Single 30 pF Capacitor Compensation Required For Unity Gain
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up

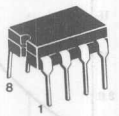
OPERATIONAL AMPLIFIER

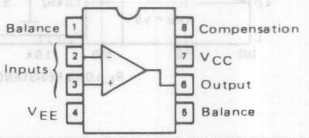
SILICON MONOLITHIC INTEGRATED CIRCUIT

P1 SUFFIX
PLASTIC PACKAGE
CASE 626-05
(MC1748C Only)



U SUFFIX
CERAMIC PACKAGE
CASE 693-02





G SUFFIX
METAL PACKAGE
CASE 601-04



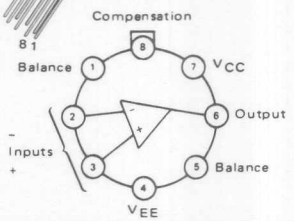
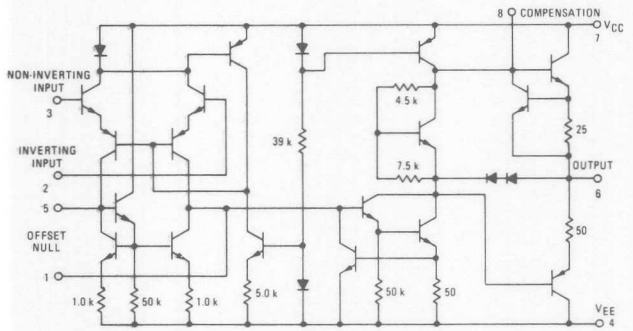


FIGURE 1 – CIRCUIT SCHEMATIC



TYPICAL COMPENSATION CIRCUITS

FIGURE 2 – OFFSET ADJUST AND FREQUENCY COMPENSATION

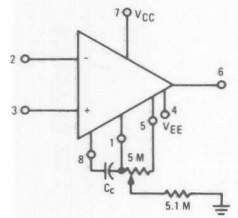
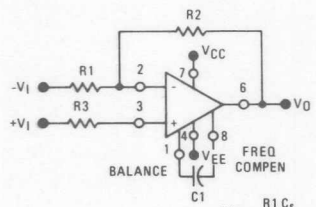


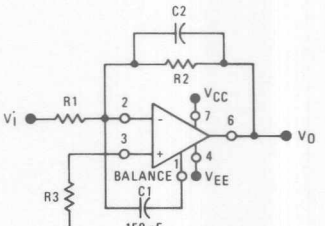
FIGURE 3 – SINGLE-POLE COMPENSATION



$$C1 \geq \frac{R1\,C_s}{R1 + R2}$$

C_s = 30 pF

FIGURE 4 – FEEDFORWARD COMPENSATION



$$C2 = \frac{1}{2\pi f_0 R2}$$

f_0 = 3.0 MHz

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	MC1748	MC1748C	Unit
Power Supply Voltage	V_{CC} V_{EE}	+22 -22	+18 -18	Vdc
Differential Input Signal	V_{in}	±30		Volts
Common-Mode Input Swing ①	V_{ICR}	±15		Volts
Output Short Circuit Duration	t_s	Continuous		
Power Dissipation (Package Limitation) Derate above T_A = +25°C	P_D	680 4.6		mW mW/°C
Operating Temperature Range	T_A	-55 to +125	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted.)

Characteristics	Symbol	MC1748			MC1748C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Bias Current	I_{IB}							µAdc
T_A = +25°C		–	0.08	0.5	–	0.08	0.5	
T_A = T_{low} to T_{high} ②		–	0.3	1.5	–	–	0.8	
Input Offset Current	$\|I_{IO}\|$							µAdc
T_A = +25°C		–	0.02	0.2	–	0.02	0.2	
T_A = T_{low} to T_{high}		–	0.08	0.5	–	–	0.3	
Input Offset Voltage ($R_S \leq 10$ k Ω)	$\|V_{IO}\|$							mVdc
T_A = +25°C		–	1.0	5.0	–	1.0	6.0	
T_A = T_{low} to T_{high}		–	–	6.0	–	–	7.5	
Differential Input Impedance (Open-Loop, f = 20 Hz)								
Parallel Input Resistance	R_p	0.3	2.0	–	0.3	2.0	–	Megohm
Parallel Input Capacitance	C_p	–	1.4	–	–	1.4	–	pF
Common-Mode Input Impedance (f 20 Hz)	z_{in}	–	200	–	–	200		Megohms
Common-Mode Input Voltage Swing	V_{ICR}	±12	±13	–	±12	±13	–	V_{pk}
Common-Mode Rejection Ratio (f = 100 Hz)	CMRR	70	90	–	70	90	–	dB
Open-Loop Voltage Gain, (V_o = ±10 V, R_L = 2.0 k ohms)	A_{vol}							V/V
T_A = +25°C		50,000	200,000	–	20,000	200,000	–	
T_A = T_{low} to T_{high}		25,000	–	–	15,000	–	–	
Step Response (V_{in} = 20 mV, C_c = 30 pF, R_L = 2 kΩ, C_L = 100 pF)								
Rise Time	t_r	–	0.3	–	–	0.3	–	µs
Overshoot Percentage		–	5.0	–	–	5.0	–	%
Slew Rate	dV_{out}/dt	–	0.8	–	–	0.8	–	V/µs
Output Impedance (f = 20 Hz)	z_o	–	75	–	–	75	–	ohms
Short-Circuit Output Current	I_{sc}	–	25	–	–	25	–	mAdc
Output Voltage Swing (R_L = 10 k ohms)	V_O	±12	±14	–	±12	±14	–	Vpk
R_L = 2 k ohms (T_A = T_{low} to t_{high})		±10	±13	–	±10	±13	–	
Power Supply Sensitivity								µV/V
V_{EE} = constant, $R_s \leq$ 10 k ohms	S+	–	30	150	–	30	150	
V_{CC} = constant, $R_s \leq$ 10 k ohms	S-	–	30	150	–	30	150	
Power Supply Current	I_D^+	–	1.67	2.83	–	1.67	2.83	mAdc
	I_D^-	–	1.67	2.83	–	1.67	2.83	
DC Quiescent Power Dissipation	P_D							mW
(V_o = 0)		–	50	85	–	50	85	

① For supply voltages less than ±15 V, the Maximum Input Voltage is equal to the Supply Voltage.

② T_{low}: 0°C for MC1748C
-55°C for MC1748
T_{high}: +70° for MC1748C
+125°C for MC1748

2

TYPICAL CHARACTERISTICS

(V_{CC} = +15 V, V_{EE} = -15 V, T_A = +25°C unless otherwise noted.)

FIGURE 5 – MINIMUM INPUT VOLTAGE RANGE

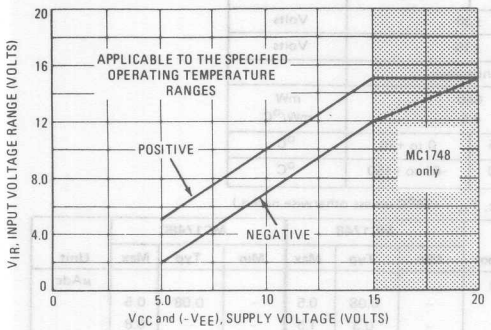


FIGURE 6 – MINIMUM OUTPUT VOLTAGE SWING

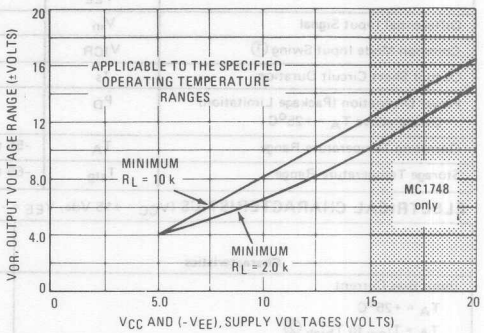


FIGURE 7 – MINIMUM VOLTAGE GAIN

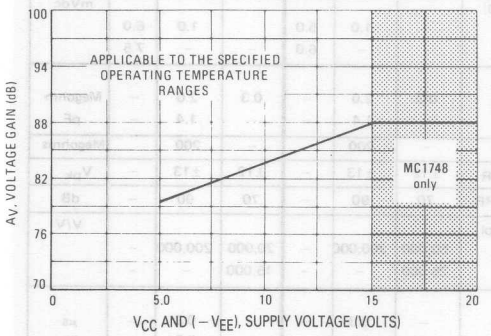


FIGURE 8 – TYPICAL SUPPLY CURRENTS

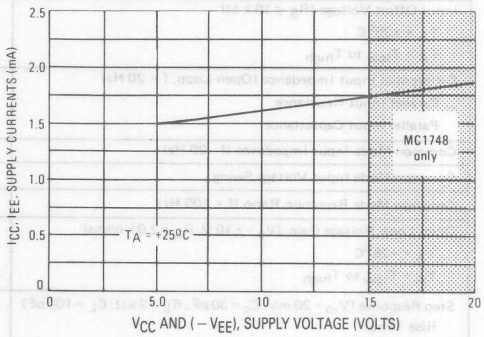


FIGURE 9 – OPEN-LOOP FREQUENCY RESPONSE

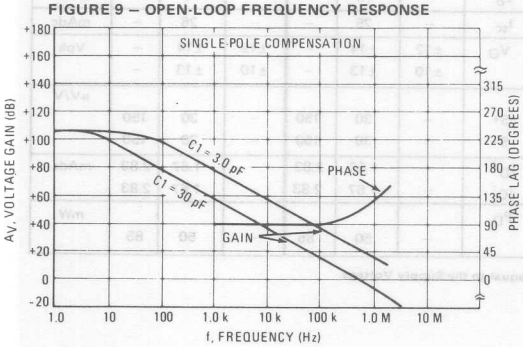
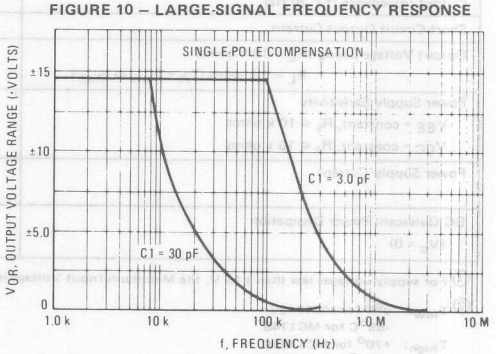


FIGURE 10 – LARGE-SIGNAL FREQUENCY RESPONSE



TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25°C unless otherwise noted.)

FIGURE 11 – VOLTAGE FOLLOWER PULSE RESPONSE

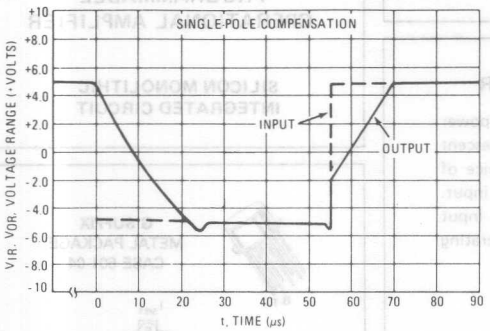


FIGURE 12 – OPEN-LOOP FREQUENCY RESPONSE

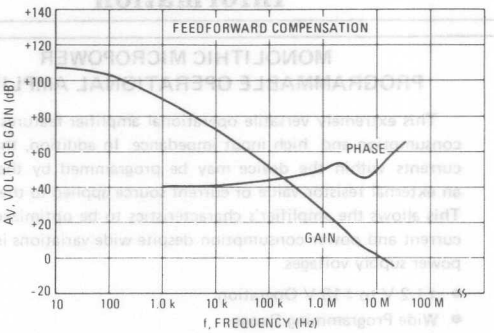


FIGURE 13 – LARGE-SIGNAL FREQUENCY RESPONSE

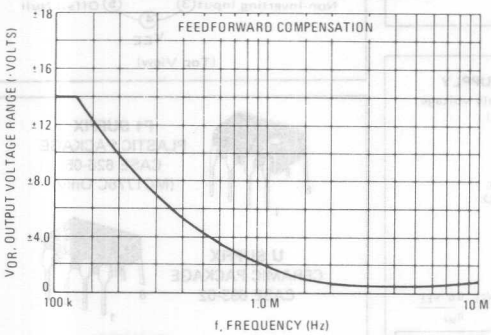
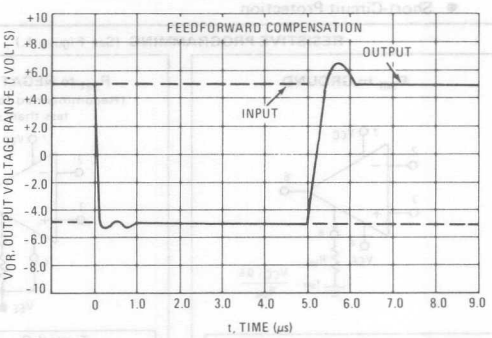


FIGURE 14 – INVERTER PULSE RESPONSE



2

Specifications and Applications Information

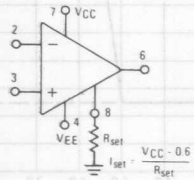
MONOLITHIC MICROPOWER PROGRAMMABLE OPERATIONAL AMPLIFIER

This extremely versatile operational amplifier features low power consumption and high input impedance. In addition, the quiescent currents within the device may be programmed by the choice of an external resistor value or current source applied to the I_{set} input. This allows the amplifier's characteristics to be optimized for input current and power consumption despite wide variations in operating power supply voltages.

- ±1.2 V to ±18 V Operation
- Wide Programming Range
- Offset Null Capability
- No Frequency Compensation Required
- Low Input Bias Currents
- Short-Circuit Protection

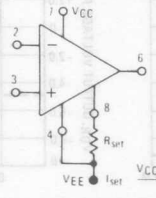
RESISTIVE PROGRAMMING (See Figure 1.)

R_{set} to GROUND



Typical R_{set} Values		
V_{CC}, V_{EE}	I_{set} = 1.5 µA	I_{set} = 15 µA
±6.0V	3.6 MΩ	360 kΩ
±10V	6.2 MΩ	620 kΩ
±12V	7.5 MΩ	750 kΩ
±15V	10 MΩ	1.0 MΩ

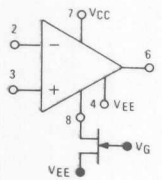
R_{set} to NEGATIVE SUPPLY
(Recommended for supply voltage less than ±6.0 V)



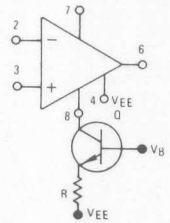
Typical R_{set} Values		
V_{CC}, V_{EE}	I_{set} = 1.5 µA	I_{set} = 15 µA
±1.5V	1.6 MΩ	160 kΩ
±3.0V	3.6 MΩ	360 kΩ
±6.0V	7.5 MΩ	750 kΩ
±15 V	20 MΩ	2.0 MΩ

ACTIVE PROGRAMMING

FET CURRENT SOURCE



BIPOLAR CURRENT SOURCE



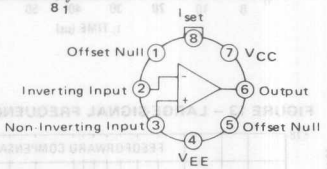
Pins not shown are not connected.

PROGRAMMABLE OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT



G SUFFIX
METAL PACKAGE
CASE 601-04

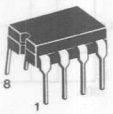


(Top View)



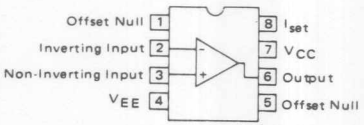
P1 SUFFIX
PLASTIC PACKAGE
CASE 626-05
(MC1776C Only)

U SUFFIX
CERAMIC PACKAGE
CASE 693-02





D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SO-8



(Top View)

ORDERING INFORMATION

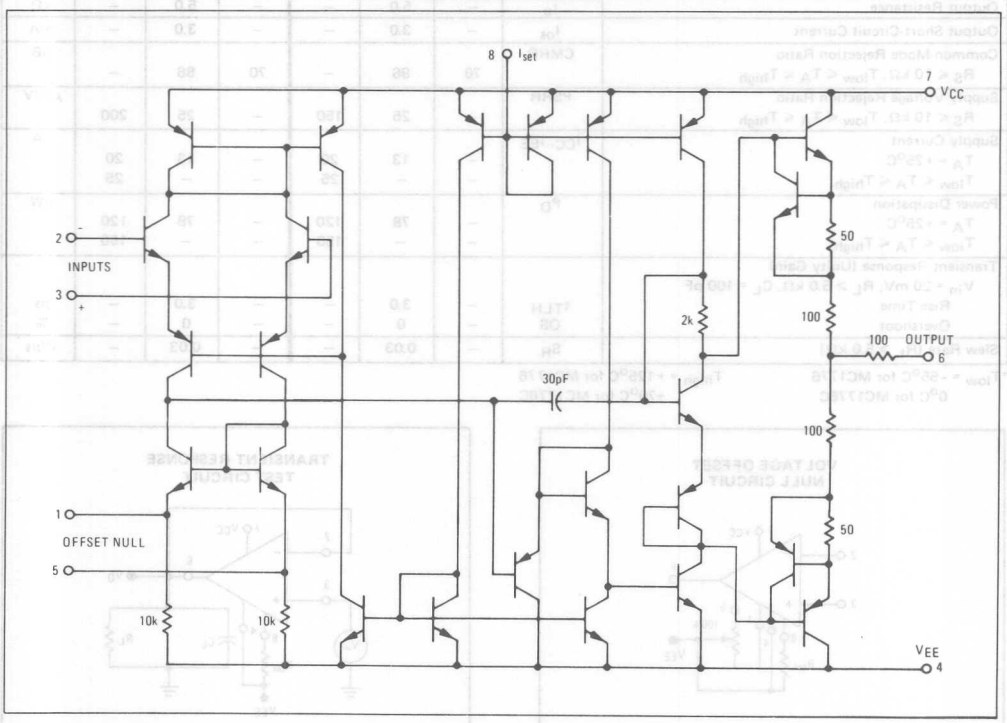
Device	Temperature Range	Package
MC1776G	−55 to +125°C	Metal Can
MC1776U		Ceramic DIP
MC1776CD	0 to +70°C	SO-8
MC1776CG		Metal Can
MC1776CP1		Plastic DIP
MC1776CU		Ceramic DIP

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC}, V_{EE}	±18	Vdc
Differential Input Voltage	V_{ID}	±30	Vdc
Common-Mode Input Voltage V_{CC} and $\|V_{EE}\| < 15$ V V_{CC} and $\|V_{EE}\| \geq 15$ V	V_{ICM}	 V_{CC}, V_{EE} ±15	Vdc
Offset Null to V_{EE} Voltage	V_{off}-V_{EE}	±0.5	Vdc
Programming Current	I_{set}	500	μA
Programming Voltage (Voltage from I_{set} terminal to ground)	V_{set}	(V_{CC}-2.0 V) to V_{CC}	Vdc
Output Short-Circuit Duration*	t_s	Indefinite	s
Operating Temperature Range MC1776 MC1776C	T_A	 -55 to +125 0 to +70	°C
Storage Temperature Range Metal and Ceramic Packages Plastic Package	T_{stg}	 -65 to +150 -55 to +125	°C
Junction Temperature Metal and Ceramic Packages Plastic Package	T_J	 175 150	°C

*May be to ground or either Supply Voltage. Rating applies up to a case temperature of +125°C or ambient temperature of +70°C and $I_{set} \leq 30$ μA.

SCHEMATIC DIAGRAM



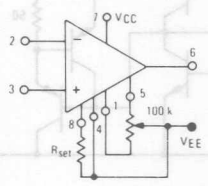
2

ELECTRICAL CHARACTERISTICS (V_{CC} = +3.0 V, V_{EE} = -3.0 V, I_{set} = 1.5 μA, T_A = +25°C unless otherwise noted.)

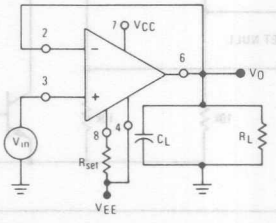
Characteristic	Symbol	MC1776 Min	MC1776 Typ	MC1776 Max	MC1776C Min	MC1776C Typ	MC1776C Max	Unit
Input Offset Voltage ($R_S \leq 10$ kΩ)	V_{IO}							mV
T_A = +25°C		–	2.0	5.0	–	2.0	6.0	
T_{low}* ≤ T_A ≤ T_{high}*		–	–	6.0	–	–	7.5	
Offset Voltage Adjustment Range	V_{IOR}	–	9.0	–	–	9.0	–	mV
Input Offset Current	I_{IO}							nA
T_A = +25°C		–	0.7	3.0	–	0.7	6.0	
T_A = T_{high}		–	–	5.0	–	–	6.0	
T_A = T_{low}		–	–	10	–	–	10	
Input Bias Current	I_{IB}							nA
T_A = +25°C		–	2.0	7.5	–	2.0	10	
T_A = T_{high}		–	–	7.5	–	–	10	
T_A = T_{low}		–	–	20	–	–	20	
Input Resistance	r_i	–	50	–	–	50	–	MΩ
Input Capacitance	c_i	–	2.0	–	–	2.0	–	pF
Input Voltage Range	V_{ID}							V
T_{low} ≤ T_A ≤ T_{high}		±1.0	–	–	±1.0	–	–	
Large Signal Voltage Gain	A_{VOL}							V/V
$R_L \geq 75$ kΩ, V_O = ±1.0 V, T_A = +25°C		50 k	200 k	–	25 k	200 k	–	
$R_L \geq 75$ kΩ, V_O = ±1.0 V, $T_{low} \leq T_A \leq T_{high}$		25 k	–	–	25 k	–	–	
Output Voltage Swing	V_O							V
$R_L \geq 75$ kΩ, $T_{low} \leq T_A \leq T_{high}$		±2.0	±2.4	–	±2.0	±2.4	–	
Output Resistance	r_o	–	5.0	–	–	5.0	–	kΩ
Output Short-Circuit Current	I_{os}	–	3.0	–	–	3.0	–	mA
Common-Mode Rejection Ratio	CMRR							dB
$R_S \leq 10$ kΩ, $T_{low} \leq T_A \leq T_{high}$		70	86	–	70	86	–	
Supply Voltage Rejection Ratio	PSRR							μV/V
$R_S \leq 10$ kΩ, $T_{low} \leq T_A \leq T_{high}$		–	25	150	–	25	200	
Supply Current	I_{CC}, I_{EE}							μA
T_A = +25°C		–	13	20	–	13	20	
$T_{low} \leq T_A \leq T_{high}$		–	–	25	–	–	25	
Power Dissipation	P_D							μW
T_A = +25°C		–	78	120	–	78	120	
$T_{low} \leq T_A \leq T_{high}$		–	–	150	–	–	150	
Transient Response (Unity Gain)								
V_{in} = 20 mV, $R_L \geq 5.0$ kΩ, C_L = 100 pF								
Rise Time	t_{TLH}	–	3.0	–	–	3.0	–	μs
Overshoot	OS	–	0	–	–	0	–	%
Slew Rate ($R_L \geq 5.0$ kΩ)	S_R	–	0.03	–	–	0.03	–	V/μs

*T_{low} = -55°C for MC1776, 0°C for MC1776C T_{high} = +125°C for MC1776, +70°C for MC1776C

VOLTAGE OFFSET NULL CIRCUIT



TRANSIENT-RESPONSE TEST CIRCUIT



Pins not shown are not connected.

2

ELECTRICAL CHARACTERISTICS (V_{CC} = +3.0 V, V_{EE} = -3.0 V, I_{set} = 15 μA, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC1776 Min	MC1776 Typ	MC1776 Max	MC1776C Min	MC1776C Typ	MC1776C Max	Unit
Input Offset Voltage ($R_S \leq 10$ kΩ)	V_{IO}							mV
T_A = +25°C		–	2.0	5.0	–	2.0	6.0	
T_{low}* ≤ T_A ≤ T_{high}*		–	–	6.0	–	–	7.5	
Offset Voltage Adjustment Range	V_{IOR}	–	18	–	–	18	–	mV
Input Offset Current	I_{IO}							nA
T_A = +25°C		–	2.0	15	–	2.0	25	
T_A = T_{high}		–	–	15	–	–	25	
T_A = T_{low}		–	–	40	–	–	40	
Input Bias Current	I_{IB}							nA
T_A = +25°C		–	15	50	–	15	50	
T_A = T_{high}		–	–	50	–	–	50	
T_A = T_{low}		–	–	120	–	–	100	
Input Resistance	r_i	–	5.0	–	–	5.0	–	MΩ
Input Capacitance	c_i	–	2.0	–	–	2.0	–	pF
Input Voltage Range	V_{ID}							V
T_{low} ≤ T_A ≤ T_{high}		±1.0	–	–	±1.0	–	–	
Large Signal Voltage Gain	A_{VOL}							V/V
$R_L \geq 5.0$ kΩ, V_O = ±1.0 V, T_A = +25°C		50 k	200 k	–	25 k	200 k	–	
$R_L \geq 5.0$ kΩ, V_O = ±1.0 V, $T_{low} \leq T_A \leq T_{high}$		25 k	–	–	25k	–	–	
Output Voltage Swing	V_O							V
$R_L \geq 5.0$ kΩ, $T_{low} \leq T_A \leq T_{high}$		±1.9	±2.1	–	±2.0	±2.1	–	
Output Resistance	r_o	–	1.0	–	–	1.0	–	kΩ
Output Short-Circuit Current	I_{os}	–	5.0	–	–	5.0	–	mA
Common-Mode Rejection Ratio	CMRR							dB
$R_S \leq 10$ kΩ, $T_{low} \leq T_A \leq T_{high}$		70	86	–	70	86	–	
Supply Voltage Rejection Ratio	PSRR							μV/V
$R_S \leq 10$ kΩ, $T_{low} \leq T_A \leq T_{high}$		–	25	150	–	25	200	
Supply Current	I_{CC}, I_{EE}							μA
T_A = +25°C		–	130	160	–	130	170	
$T_{low} \leq T_A \leq T_{high}$		–	–	180	–	–	180	
Power Dissipation	P_D							μW
T_A = +25°C		–	780	960	–	780	1020	
$T_{low} \leq T_A \leq T_{high}$		–	–	1080	–	–	1080	
Transient Response (Unity Gain)								
V_{in} = 20 mV, $R_L \geq 5.0$ kΩ, C_L = 100 pF								
Rise Time	t_{TLH}	–	0.6	–	–	0.6	–	μs
Overshoot	OS	–	5.0	–	–	5.0	–	%
Slew Rate ($R_L \geq 5.0$ kΩ)	S_R	–	0.35	–	–	0.35	–	V/μs

*T_{low} = -55°C for MC1776, 0°C for MC1776C T_{high} = +125°C for MC1776, +70°C for MC1776C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = -15 V, I_{set} = 1.5 μA, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC1776 Min	MC1776 Typ	MC1776 Max	MC1776C Min	MC1776C Typ	MC1776C Max	Unit
Input Offset Voltage ($R_S \leq 10$ kΩ)	V_{IO}							mV
T_A = +25°C		–	2.0	5.0	–	2.0	6.0	
T_{low}* ≤ $T_A \leq T_{high}$*		–	–	6.0	–	–	7.5	
Offset Voltage Adjustment Range	V_{IOR}	–	9.0	–	–	9.0	–	mV
Input Offset Current	I_{IO}							nA
T_A = +25°C		–	0.7	3.0	–	0.7	6.0	
$T_A = T_{high}$		–	–	5.0	–	–	6.0	
$T_A = T_{low}$		–	–	10	–	–	10	
Input Bias Current	I_{IB}							nA
T_A = +25°C		–	2.0	7.5	–	2.0	10	
$T_A = T_{high}$		–	–	7.5	–	–	10	
$T_A = T_{low}$		–	–	20	–	–	20	
Input Resistance	r_i	–	50	–	–	50	–	MΩ
Input Capacitance	c_i	–	2.0	–	–	2.0	–	pF
Input Voltage Range	V_{ID}							V
$T_{low} \leq T_A \leq T_{high}$		±10	–	–	±10	–	–	
Large Signal Voltage Gain	A_{VOL}							V/V
$R_L \geq 75$ kΩ, V_O = ±10 V, T_A = +25°C		200 k	400 k	–	50 k	400 k	–	
$R_L \geq 75$ kΩ, V_O = ±10 V, $T_{low} \leq T_A \leq T_{high}$		100 k	–	–	50 k	–	–	
Output Voltage Swing	V_O							V
$R_L \geq 75$ kΩ, T_A = +25°C		±12	±14	–	±12	±14	–	
$R_L \geq 75$ kΩ, $T_{low} \leq T_A \leq T_{high}$		±10	–	–	±10	–	–	
Output Resistance	r_o	–	5.0	–	–	5.0	–	kΩ
Output Short-Circuit Current	I_{os}	–	3.0	–	–	3.0	–	mA
Common-Mode Rejection Ratio	CMRR							dB
$R_S \leq 10$ kΩ, $T_{low} \leq T_A \leq T_{high}$		70	90	–	70	90	–	
Supply Voltage Rejection Ratio	PSRR							μV/V
$R_S \leq 10$ kΩ, $T_{low} \leq T_A \leq T_{high}$		–	25	150	–	25	200	
Supply Current	I_{CC}, I_{EE}							μA
T_A = +25°C		–	20	25	–	20	30	
$T_{low} \leq T_A \leq T_{high}$		–	–	30	–	–	35	
Power Dissipation	P_D							mW
T_A = +25°C		–	–	0.75	–	–	0.9	
$T_{low} \leq T_A \leq T_{high}$		–	–	0.9	–	–	1.05	
Transient Response (Unity Gain)								
V_{in} = 20 mV, $R_L \geq 5.0$ kΩ, C_L = 100 pF								
Rise Time	t_{TLH}	–	1.6	–	–	1.6	–	μs
Overshoot	OS	–	0	–	–	0	–	%
Slew Rate ($R_L \geq 5.0$ kΩ)	S_R	–	0.1	–	–	0.1	–	V/μs

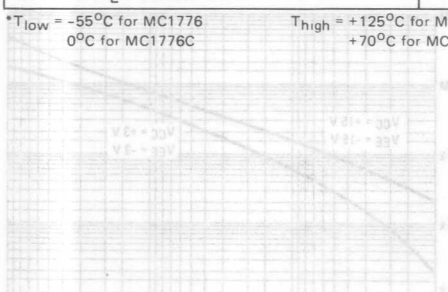
*T_{low} = -55°C for MC1776, 0°C for MC1776C T_{high} = +125°C for MC1776, +70°C for MC1776C

2

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, I_{set} = 15 μA, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC1776 Min	MC1776 Typ	MC1776 Max	MC1776C Min	MC1776C Typ	MC1776C Max	Unit
Input Offset Voltage ($R_S \leq 10$ kΩ)	V_{IO}							mV
T_A = +25°C		–	2.0	5.0	–	2.0	6.0	
T_{low}* ≤ T_A ≤ T_{high}*		–	–	6.0	–	–	7.5	
Offset Voltage Adjustment Range	V_{IOR}	–	18	–	–	18	–	mV
Input Offset Current	I_{IO}							nA
T_A = +25°C		–	2.0	15	–	2.0	25	
T_A = T_{high}		–	–	15	–	–	25	
T_A = T_{low}		–	–	40	–	–	40	
Input Bias Current	I_{IB}							nA
T_A = +25°C		–	15	50	–	15	50	
T_A = T_{high}		–	–	50	–	–	50	
T_A = T_{low}		–	–	120	–	–	100	
Input Resistance	r_i	–	5.0	–	–	5.0	–	MΩ
Input Capacitance	c_i	–	2.0	–	–	2.0	–	pF
Input Voltage Range	V_{ID}							V
T_{low} ≤ T_A ≤ T_{high}		±10	–	–	±10	–	–	
Large Signal Voltage Gain	A_{VOL}							V/V
$R_L \geq 5.0$ kΩ, V_O = ±10 V, T_A = +25°C		100 k	400 k	–	50 k	400 k	–	
$R_L \geq 75$ kΩ, V_O = ±10 V, $T_{low} \leq T_A \leq T_{high}$		75 k	–	–	50 k	–	–	
Output Voltage Swing	V_O							V
$R_L \geq 5.0$ kΩ, T_A = +25°C		±10	±13	–	±10	±13	–	
$R_L \geq 75$ kΩ, $T_{low} \leq T_A \leq T_{high}$		±10	–	–	±10	–	–	
Output Resistance	r_o	–	1.0	–	–	1.0	–	kΩ
Output Short-Circuit Current	I_{os}	–	12	–	–	12	–	mA
Common-Mode Rejection Ratio	CMRR							dB
$R_S \leq 10$ kΩ, $T_{low} \leq T_A \leq T_{high}$		70	90	–	70	90	–	
Supply Voltage Rejection Ratio	PSRR							μV/V
$R_S \leq 10$ kΩ, $T_{low} \leq T_A \leq T_{high}$		–	25	150	–	25	200	
Supply Current	I_{CC}, I_{EE}							μA
T_A = +25°C		–	160	180	–	160	190	
$T_{low} \leq T_A \leq T_{high}$		–	–	200	–	–	200	
Power Dissipation	P_D							mW
T_A = +25°C		–	–	5.4	–	–	5.7	
$T_{low} \leq T_A \leq T_{high}$		–	–	6.0	–	–	6.0	
Transient Response (Unity Gain)								
V_{in} = 20 mV, $R_L \geq 5.0$ kΩ, C_L = 100 pF								
Rise Time	t_{TLH}	–	0.35	–	–	0.35	–	μs
Overshoot	OS	–	10	–	–	10	–	%
Slew Rate ($R_L \geq 5.0$ kΩ)	S_R	–	0.8	–	–	0.8	–	V/μs

*T_{low} = −55°C for MC1776, 0°C for MC1776C T_{high} = +125°C for MC1776, +70°C for MC1776C



2

TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted.)

FIGURE 1 – SET CURRENT versus SET RESISTOR

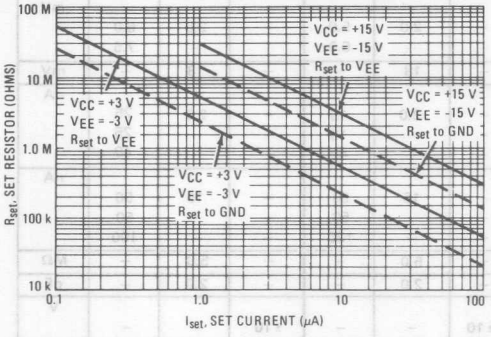


FIGURE 2 – POSITIVE STANDBY SUPPLY CURRENT versus SET CURRENT

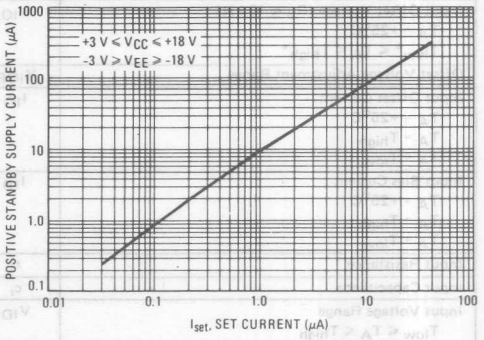


FIGURE 3 – OPEN-LOOP GAIN versus SET CURRENT

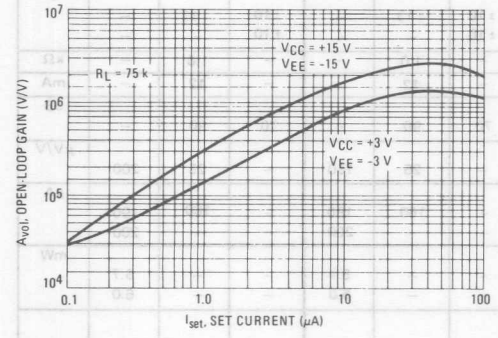


FIGURE 4 – INPUT BIAS CURRENT versus SET CURRENT

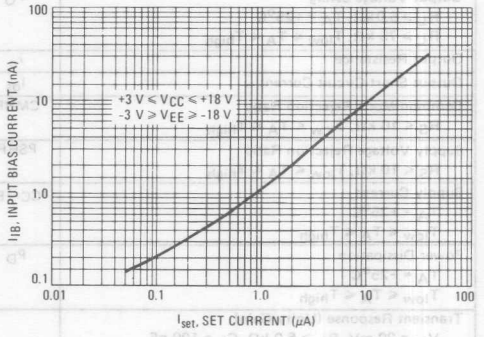


FIGURE 5 – INPUT BIAS CURRENT versus AMBIENT TEMPERATURE

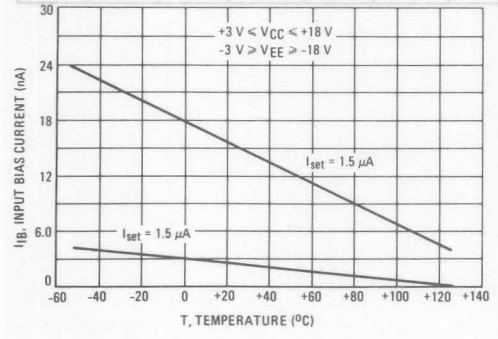
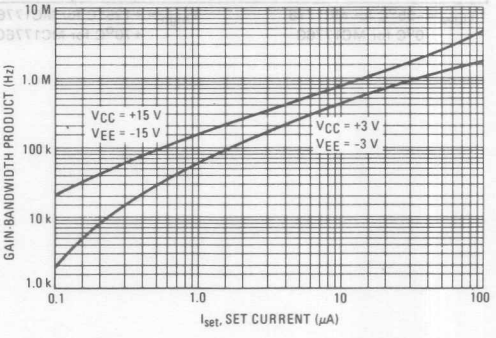


FIGURE 6 – GAIN-BANDWIDTH PRODUCT (GBW) versus SET CURRENT



TYPICAL CHARACTERISTICS (continued)

(T_A = +25°C unless otherwise noted.)

FIGURE 7 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

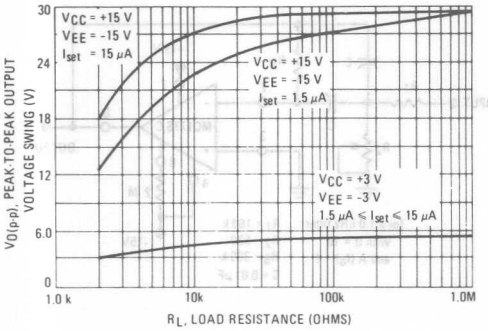


FIGURE 8 – SUPPLY CURRENT versus AMBIENT TEMPERATURE

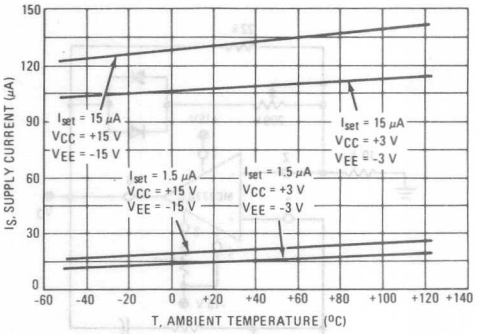


FIGURE 9 – OUTPUT SWING versus SUPPLY VOLTAGE

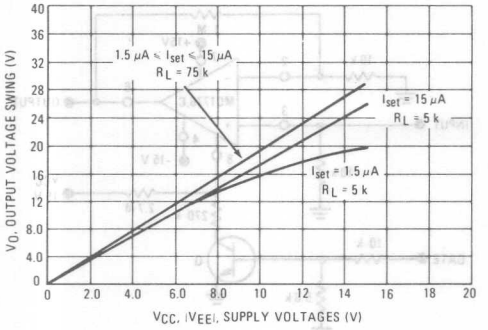


FIGURE 10 – SLEW RATE versus SET CURRENT

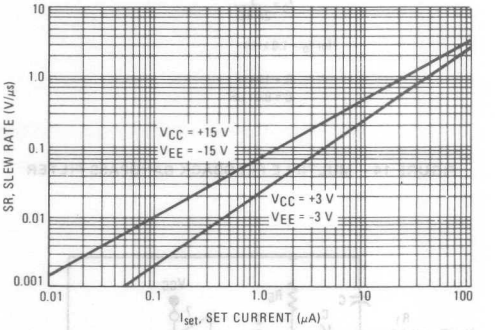


FIGURE 11 – INPUT NOISE VOLTAGE versus SET CURRENT

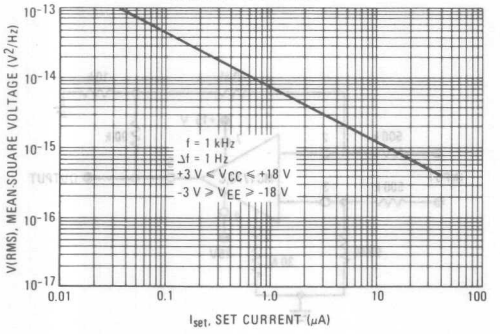
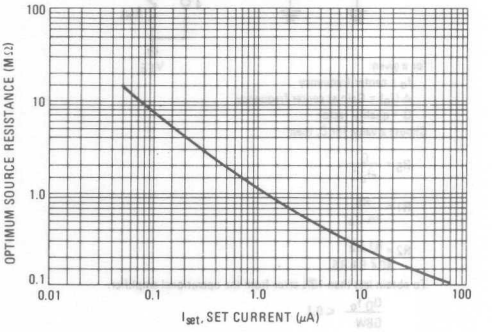
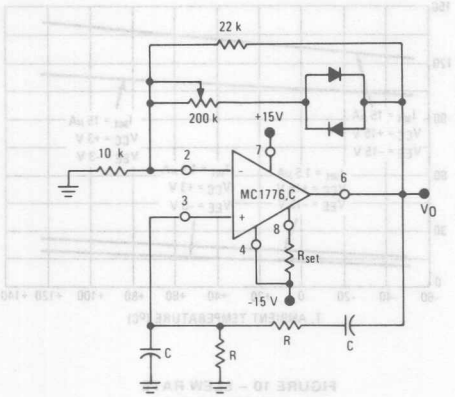


FIGURE 12 – OPTIMUM SOURCE RESISTANCE FOR MINIMUM NOISE versus SET CURRENT



2

FIGURE 13 – WIEN BRIDGE OSCILLATOR

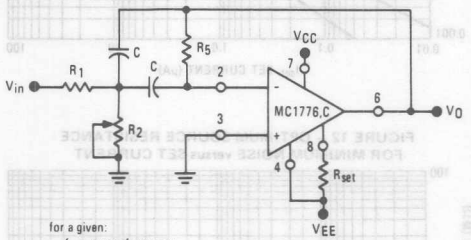


$$f_O = \frac{1}{2\pi RC}$$

(for f_O = 1.0 kHz)

R = 16 kΩ
C = 0.01 μF

FIGURE 14 – MULTIPLE FEEDBACK BANDPASS FILTER



for a given:
f_O = center frequency
A (f_O) = Gain at center frequency
Q = quality factor
Choose a value for C, then

$$R_5 = \frac{Q}{\pi f_O C}$$

$$R1 = \frac{R5}{2A\,(f_O)}$$

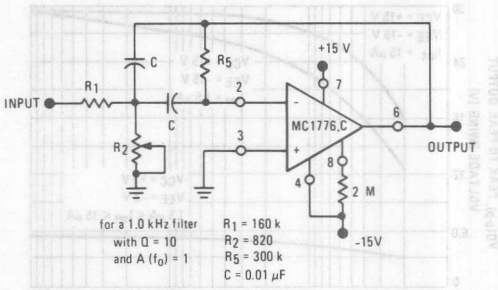
$$R2 = \frac{R1 \cdot R5}{4Q^2\,R1 - R5}$$

To obtain less than 10% error from the operational amplifier:

$$\frac{Q_O\, f_O}{GBW} \leq 0.1$$

where f_O and GBW are expressed in Hz. GBW is available from Figure 6 as a function of Set Current, I_{set}.

FIGURE 15 – MULTIPLE FEEDBACK BANDPASS FILTER (1.0 kHz)



for a 1.0 kHz filter with Q = 10 and A (f_O) = 1

R_1 = 160 k
R_2 = 820
R_5 = 300 k
C = 0.01 μF

FIGURE 16 – GATED AMPLIFIER

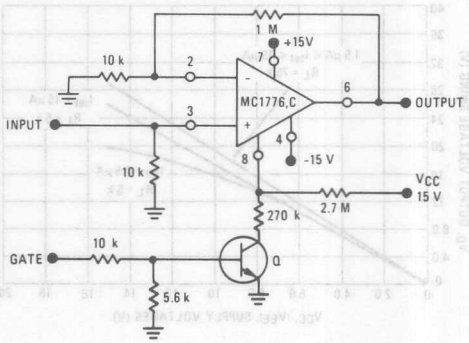
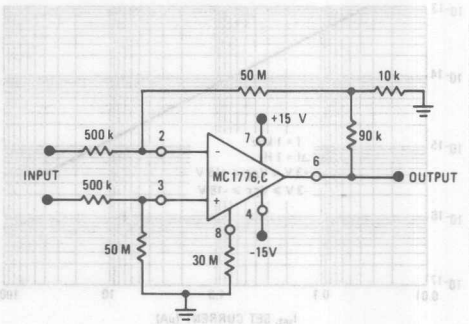


FIGURE 17 – HIGH INPUT IMPEDANCE AMPLIFIER



MOTOROLA

MC3301 LM2900 MC3401 LM3900

Specifications and Applications Information

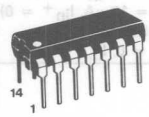
QUAD SINGLE SUPPLY OPERATIONAL AMPLIFIER

These internally compensated Norton operational amplifiers are designed specifically for single positive power supply applications found in industrial control systems and automotive electronics. Each device contains four independent amplifiers — making it ideal for applications such as active filters, multi-channel amplifiers, tachometers, oscillators and other similar usages.

- Single-Supply Operation
- Internally Compensated
- Wide Unity Gain Bandwidth: 4.0 MHz Typical
- Low Input Bias Current: 50 nA Typical
- High Open-Loop Gain: 1000 V/V Minimum
- Large Output Voltage Swing: (V_{CC} − 1) V_{p-p}

QUAD OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT



N, P SUFFIX
PLASTIC PACKAGE
CASE 646-06

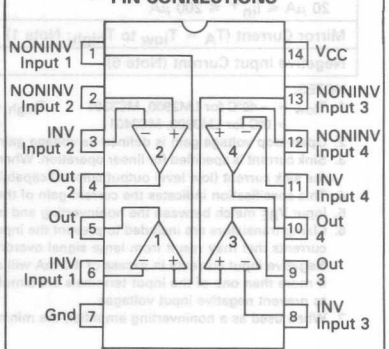
D SUFFIX
PLASTIC PACKAGE
CASE 751A-02
SO-14



MAXIMUM RATINGS

Rating	Symbol	LM2900/ LM3900	MC3301	MC3401	Unit
Supply Voltage	V_{CC}	+32	+28	+18	V
Input Currents (I_{in}^+ or I_{in}^-)	I_{in}	5.0	5.0	5.0	mA
Output Current	I_O	50	50	50	mA
Power Dissipation (T_A = +25°C) Derate above T_A = +25°C	P_D $1/R_{\theta JA}$	625 5.0	625 5.0	625 5.0	mW mW/°C
Operating Ambient Temperature Range LM2900 LM3900	T_A	— −40 to +85 0 to +70	−40 to +85 — —	0 to +70 — —	°C
Storage Temperature Range	T_{stg}	−65 to +150	−65 to +150	−65 to +150	°C

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
LM3900D MC3401D	0°C to +70°C	SO-14
LM3900N MC3401P	0°C to +70°C	Plastic DIP
LM2900N MC3301P	−40°C to +85°C	Plastic DIP

2

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, T_A = +25°C unless otherwise noted)

Characteristic	Symbol	LM2900			LM3900			MC3301			MC3401			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Open-Loop Voltage Gain	A_{VOL}													V/mV
f = 100 Hz, R_L = 5.0 k		1.2	2.0	—	1.2	2.0	—	1.2	2.0	—	1.2	2.0	—	
T_A = T_{low} to T_{high} (Notes 1, 2)		—	—	—	—	—	—	—	—	—	0.8	—	—	
Input Resistance (Inverting Input)	r_i	—	1.0	—	—	1.0	—	—	1.0	—	0.1	1.0	—	MΩ
Output Resistance	r_O	—	8.0	—	—	8.0	—	—	8.0	—	—	8.0	—	kΩ
Input Bias Current (Inverting Input)	I_{IB}	—	50	200	—	50	200	—	50	300	—	50	300	nA
T_A = T_{low} to T_{high} (Note 1)		—	—	—	—	—	—	—	—	—	—	—	500	
Slew Rate (C_L = 100 pF, R_L = 2.0 k)	SR													V/μs
Positive Output Swing		—	0.5	—	—	0.5	—	—	0.5	—	—	0.5	—	
Negative Output Swing		—	20	—	—	20	—	—	20	—	—	20	—	
Unity Gain Bandwidth	BW	—	4.0	—	—	4.0	—	—	4.0	—	—	4.0	—	MHz
Output Voltage Swing (Note 7)														V
V_{CC} = +15 V, R_L = 2.0 k														
V_{out} High (I_{in}^- = 0, I_{in}^+ = 0)	V_{OH}	13.5	14.2	—	13.5	14.2	—	13.5	14.2	—	13.5	14.2	—	
V_{out} Low (I_{in}^- = 10 μA, I_{in}^+ = 0)	V_{OL}	—	0.03	0.2	—	0.03	0.2	—	0.03	0.2	—	0.03	0.2	
V_{CC} = Maximum Rating, R_L = ∞														
V_{out} High (I_{in}^- = 0, I_{in}^+ = 0)	V_{OH}	—	29.5	—	—	29.5	—	—	25.5	—	—	15.5	—	
Output Current														mA
Source	I_{source}	6.0	10	—	6.0	10	—	5.0	10	—	5.0	10	—	
Sink (Note 3)	I_{sink}	0.5	0.87	—	0.5	0.87	—	0.5	0.87	—	0.5	0.87	—	
Low Level Output Current	I_{OL}	—	5.0	—	—	5.0	—	—	5.0	—	—	5.0	—	
I_{in}^- = 5.0 μA, V_{OL} = 1.0 V														
Supply Current (All Four Amplifiers)														mA
Noninverting Inputs Open	I_{DO}	—	6.9	10	—	6.9	10	—	6.9	10	—	6.9	10	
Noninverting Inputs Grounded	I_{DG}	—	7.8	14	—	7.8	14	—	7.8	14	—	7.8	14	
Power Supply Rejection (f = 100 Hz)	PSRR	—	55	—	—	55	—	—	55	—	—	55	—	dB
Mirror Gain (T_A = T_{low} to T_{high}; Notes 1, 4)	A_i													μA
I_{in}^+ = 20 μA		0.90	1.0	1.1	0.90	1.0	1.1	0.90	1.0	1.1	0.90	1.0	1.1	
I_{in}^+ = 200 μA		0.90	1.0	1.1	0.90	1.0	1.1	0.90	1.0	1.1	0.90	1.0	1.0	
Δ Mirror Gain (T_A = T_{low} to T_{high}; Notes 1, 4)	ΔA_i	—	2.0	5.0	—	2.0	5.0	—	2.0	5.0	—	2.0	5.0	%
20 μA ≤ I_{in}^+ ≤ 200 μA														
Mirror Current (T_A = T_{low} to T_{high}; Note 1)		—	10	500	—	10	500	—	10	500	—	10	500	μA
Negative Input Current (Note 6)		—	1.0	—	—	1.0	—	—	1.0	—	—	1.0	—	mA

NOTES:

1. T_{low} = −40°C for LM2900, MC3301; T_{high} = +85°C for LM2900, MC3301
   = 0°C for LM3900, MC3401 = +70°C ffor LM3900, MC3401
2. Open-loop voltage gain is defined as voltage gain from the inverting input to the output.
3. Sink current is specified for linear operation. When the device is used as a comparator (non-linear operation) where the inverting input is overdriven, the sink current (low level output current) capability is typically 5.0 mA.
4. This specification indicates the current gain of the current mirror which is used as the noninverting input.
5. Input V_{BE} match between the noninverting and inverting inputs occurs for a mirror current (noninverting input current) of approximately 10 μA.
6. Clamp transistors are included to prevent the input voltages from swinging below ground more than approximately −0.3 volts. The negative input currents that may result from large signal overdrive with capacitive input coupling must be limited externally to values of approximately 1.0 mA. Negative input currents in excess of 4.0 mA will cause the output to drop to a low voltage. These values apply for any one of the input terminals. If more than one of the input terminals are simultaneously driven negative, maximum currents are reduced. Common-mode biasing can be used to prevent negative input voltages.
7. When used as a noninverting amplifier, the minimum output voltage is the V_{BE} of the inverting input transistor.

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, R_L = 5.0 kΩ, T_A = +25°C
[each amplifier] unless otherwise noted.)

FIGURE 1 — OPEN-LOOP VOLTAGE GAIN versus FREQUENCY

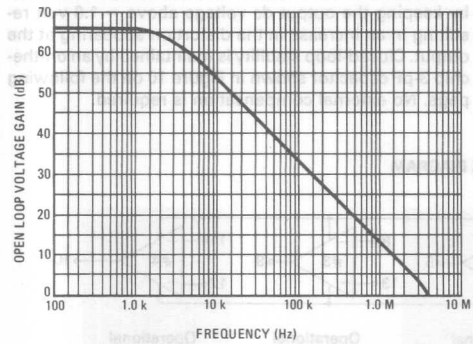


FIGURE 2 — OPEN-LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE

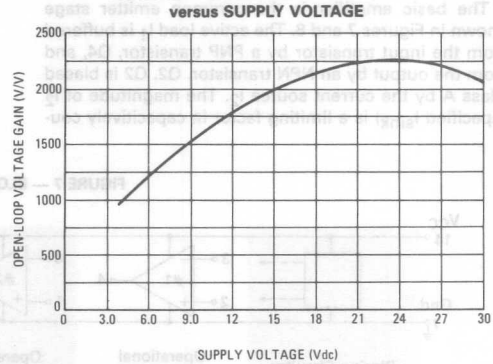


FIGURE 3 — OUTPUT RESISTANCE versus FREQUENCY

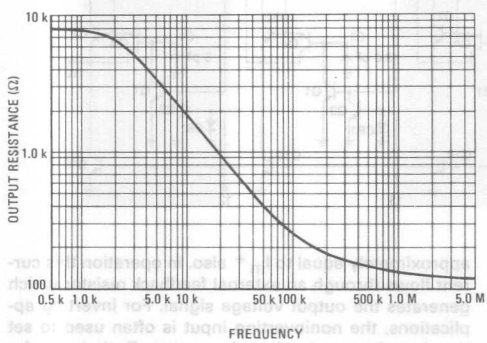


FIGURE 4 — SUPPLY CURRENT versus SUPPLY VOLTAGE

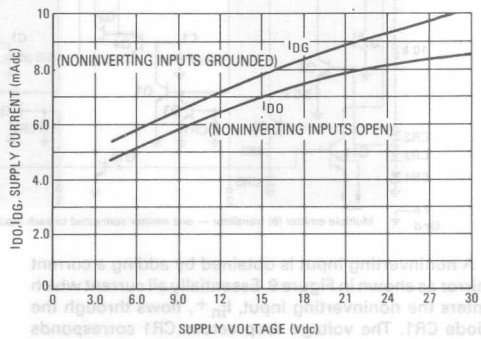


FIGURE 5 — LINEAR SOURCE CURRENT versus SUPPLY VOLTAGE

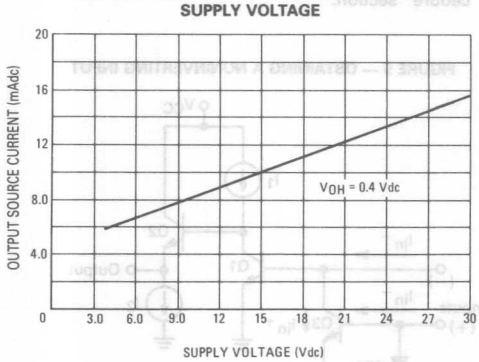
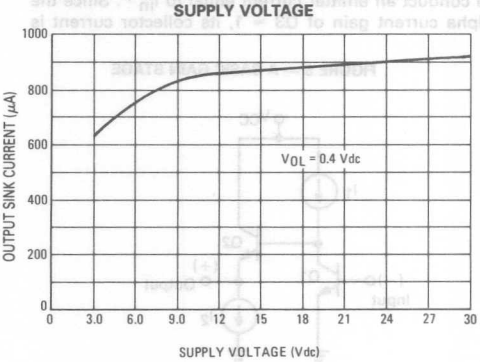


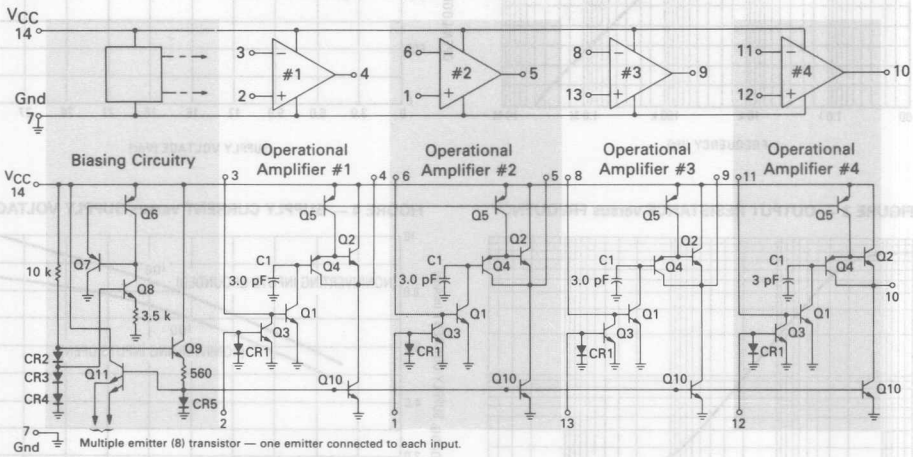
FIGURE 6 — LINEAR SINK CURRENT versus SUPPLY VOLTAGE



BASIC AMPLIFIER

The basic amplifier is the common emitter stage shown in Figures 7 and 8. The active load I_1 is buffered from the input transistor by a PNP transistor, Q4, and from the output by an NPN transistor, Q2. Q2 is biased Class A by the current source I_2. The magnitude of I_2 (specified I_{sink}) is a limiting factor in capacitively coupled linear operation at the output. The sink current of the device can be forced to exceed the specified level by keeping the output dc voltage above ≈ 1.0 volt resulting in an increase in the distortion appearing at the output. Closed-loop stability is maintained by an on-the-chip 3-pF capacitor shown in Figure 10 on the following page. No external compensation is required.

FIGURE 7 — BLOCK DIAGRAM



A noninverting input is obtained by adding a current mirror as shown in Figure 9. Essentially all current which enters the noninverting input, I_{in}^+, flows through the diode CR1. The voltage drop across CR1 corresponds to this input current magnitude and this same voltage is applied to a matched device, Q3. Thus Q3 is biased to conduct an emitter current equal to I_{in}^+. Since the alpha current gain of Q3 ≈ 1, its collector current is approximately equal to I_{in}^+ also. In operation this current flows through an external feedback resistor which generates the output voltage signal. For inverting applications, the noninverting input is often used to set the dc quiescent level at the output. Techniques for doing this are discussed in the "Normal Design Procedure" section.

FIGURE 8 — A BASIC GAIN STAGE

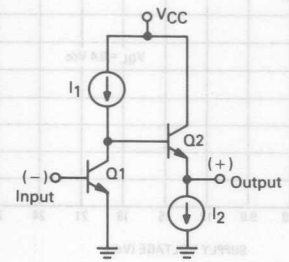
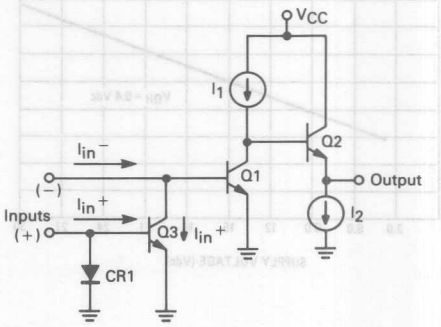


FIGURE 9 — OBTAINING A NONINVERTING INPUT



OPERATION AND APPLICATIONS (continued)

BIASING CIRCUITRY

The circuitry common to all four amplifiers is shown in Figure 11. The purpose of this circuitry is to provide biasing voltage for the PNP and NPN current sources used in the amplifiers.

The voltage drops across diodes CR2, CR3 and CR4 are used as references. The voltage across resistor R1 is the sum of the drops across CR4 and CR3 minus the V_{BE} of Q8. The PNP current sources (Q5, etc.) are set to the magnitude $V_{BE}/R1$ by transistor Q6. Transistor Q7 reduces base current loading. The voltage across resistor R2 is the sum of the voltage drops across CR2, CR3 and CR4, minus the V_{BE} drops of transistor Q9 and diode CR5 thus the current set is established by CR5 in all the NPN current sources (Q10, etc.). This technique results in current source magnitudes which are relatively independent of the supply voltage. Q11 (Figure 7) provides circuit protection from signals that are negative with respect to ground.

FIGURE 10 — A BASIC OPERATIONAL AMPLIFIER

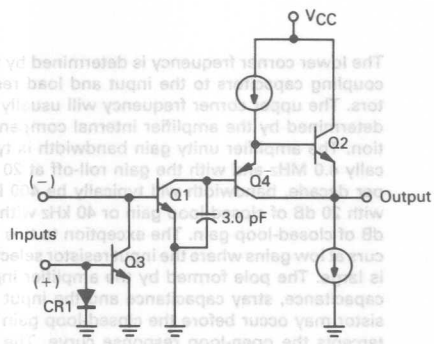
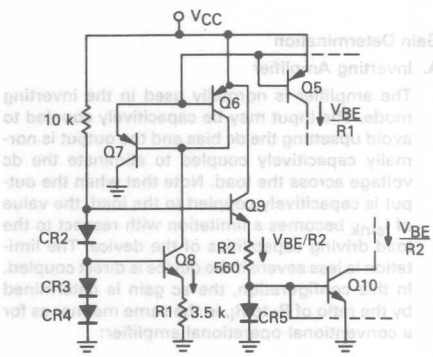


FIGURE 11 — BIASING CIRCUITRY



NORMAL DESIGN PROCEDURE

1. Output Q-Point Biasing

   A. A number of techniques may be devised to bias the quiescent output voltage to an acceptable level. However, in terms of loop gain considerations it is usually desirable to use the noninverting input to effect the biasing; as shown in Figures 12 and 13 (see the first page of this specification). The high impedance of the collector of the noninverting "current mirror" transistor helps to achieve the maximum loop gain for any particular configuration. It is desirable that the noninverting input current be in the 10 μA to 200 μA range.

   B. V_{CC} Reference Voltage (see Figures 12 and 13)
   The noninverting input is normally returned to the V_{CC} voltage (which should be well filtered) through a resistor, R_r, allowing the input current, I_{in}^+, to be within the range of 10 μA to 200 μA. Choosing the feedback resistor, R_f, to be equal to ½ R_r will now bias the amplifier output dc level to approximately $\frac{V_{CC}}{2}$. This allows the maximum dynamic range of the output voltage.

   C. Reference Voltage other than V_{CC} (see Figure 14)
   The biasing resistor R_r may be returned to a voltage (V_r) other than V_{CC}. By setting $R_f = R_r$, (still keeping I_{in}^+ between 10 μA and 200 μA) the output dc level will be equal to V_r. The expression for determining V_{Odc} is:

$$V_{Odc} = \frac{(A_i)(V_r)(R_f)}{R_r} + \left(1 - \frac{R_f}{R_r} A_i\right) \phi$$

   where ϕ is the V_{BE} drop of the input transistors (approximately 0.6 Vdc @ +25°C and assumed equal). A_i is the current mirror gain.

2

FIGURE 12 — INVERTING AMPLIFIER

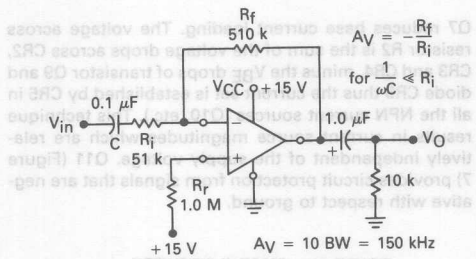
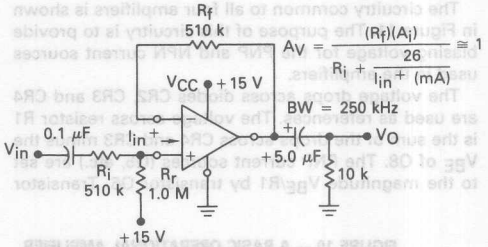


FIGURE 13 — NONINVERTING AMPLIFIER



2. Gain Determination

A. Inverting Amplifier

The amplifier is normally used in the inverting mode. The input may be capacitively coupled to avoid upsetting the dc bias and the output is normally capacitively coupled to eliminate the dc voltage across the load. Note that when the output is capacitively coupled to the load, the value of I_{sink} becomes a limitation with respect to the load driving capabilities of the device. The limitation is less severe if the device is direct coupled. In this configuration, the ac gain is determined by the ratio of R_f to R_i, in the same manner as for a conventional operational amplifier:

$$A_v = \frac{R_f}{R_i}$$

The lower corner frequency is determined by the coupling capacitors to the input and load resistors. The upper corner frequency will usually be determined by the amplifier internal compensation. The amplifier unity gain bandwidth is typically 4.0 MHz and with the gain roll-off at 20 dB per decade, bandwidth will typically be 400 kHz with 20 dB of closed-loop gain or 40 kHz with 40 dB of closed-loop gain. The exception to this occurs at low gains where the input resistor selected is large. The pole formed by the amplifier input capacitance, stray capacitance and the input resistor may occur before the closed-loop gain intercepts the open-loop response curve. The inverting input capacity is typically 3.0 pF.

FIGURE 14 — INVERTING AMPLIFIER WITH ARBITRARY REFERENCE

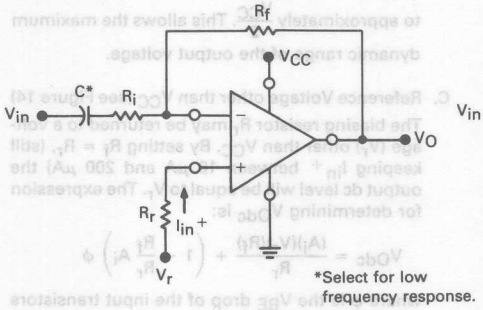
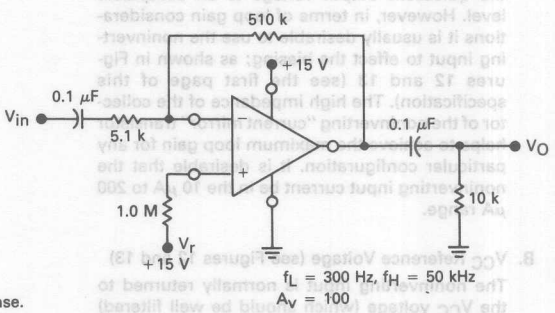


FIGURE 15 — INVERTING AMPLIFIER WITH A_v = 100 AND V_r = V_{CC}



B. Noninverting Amplifier

These devices may be used in the noninverting mode (see Figure 13). The amplifier gain in this configuration is subject to the current mirror gain. In addition, the resistance of the input diode must be included in the value of the input resistor. This resistance is approximately $\frac{26}{I_{in}^+}$ ohms, where I_{in}^+ is input current in milliamperes. The noninverting ac gain expression is given by:

$$A_V = \frac{(R_f)(A_i)}{R_i + \frac{26}{I_{in}^+ \text{ (mA)}}}$$

The bandwidth of the noninverting configuration for a given R_f value is essentially independent of the gain chosen. For R_f = 510 kΩ the bandwidth will be in excess of 200 kHz for noninverting gains of 1, 10, or 100. This is a result of the loop gain remaining constant for these gains since the input resistor is effectively isolated from the feedback loop.

TYPICAL APPLICATIONS

FIGURE 16 — TACHOMETER CIRCUIT

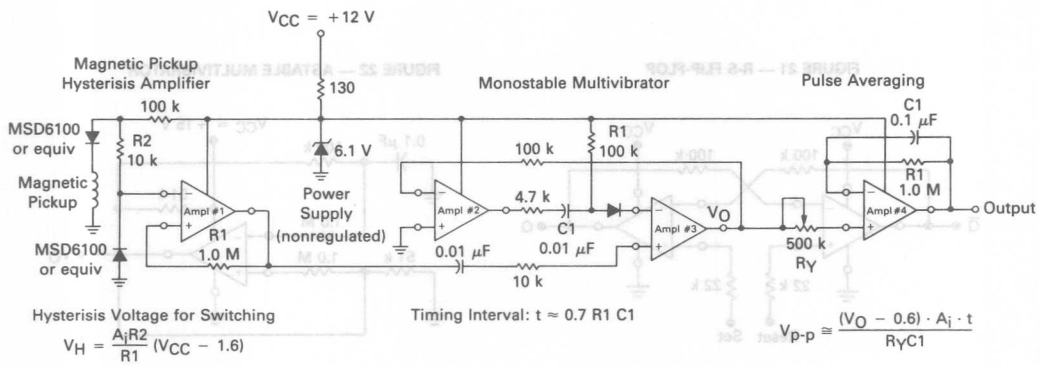
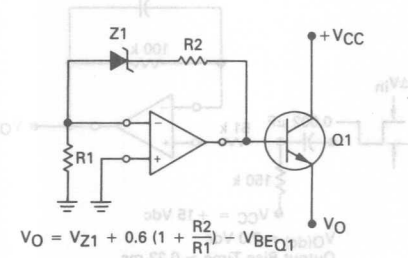
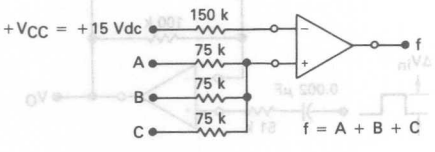


FIGURE 17 — VOLTAGE REGULATOR



NOTE:
For positive T_C zeners R2 and R1 can be selected to give T_C output.

FIGURE 18 — LOGIC "OR" GATE



TYPICAL APPLICATIONS (continued)

FIGURE 19 — LOGIC "NAND" GATE (Large Fan-In)

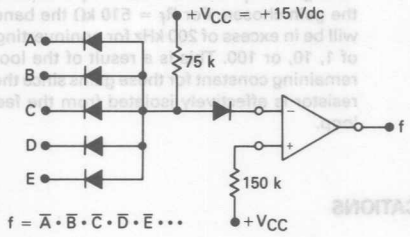


FIGURE 20 — LOGIC "NOR" GATE

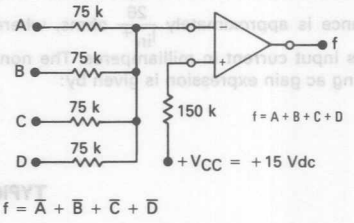


FIGURE 21 — R-S FLIP-FLOP

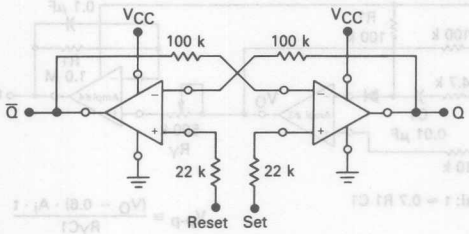


FIGURE 22 — ASTABLE MULTIVIBRATOR

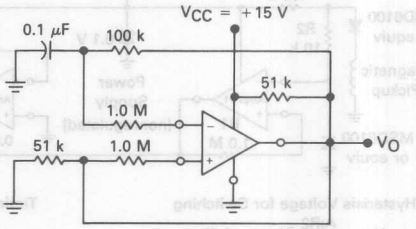


FIGURE 23 — POSITIVE-EDGE DIFFERENTIATOR

Output Rise Time ≈ 0.22 ms
Input Change Time Constant ≈ 1.0 ms

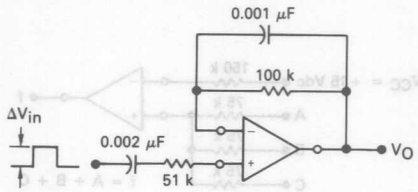
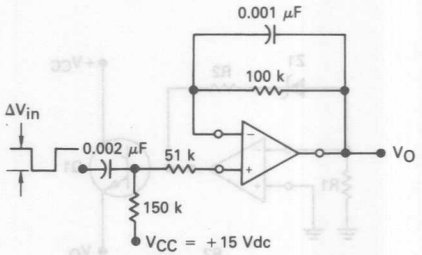


FIGURE 24 — NEGATIVE-EDGE DIFFERENTIATOR



VO(dc) ≈ 7.0 Vdc
Output Rise Time ≈ 0.22 ms
Input Change Time Constant ≈ 1.0 ms

FIGURE 25 — AMPLIFIER AND DRIVER FOR A 50-OHM LINE

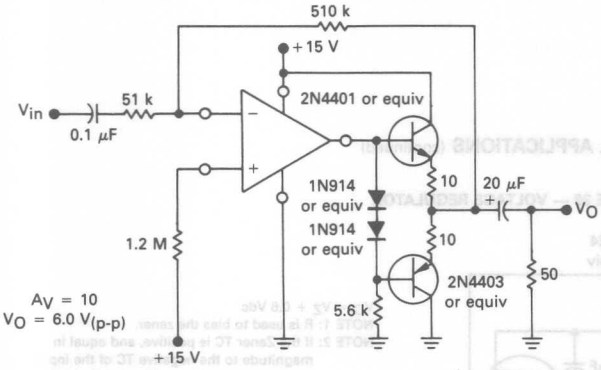


FIGURE 26 — BASIC BANDPASS AND NOTCH FILTER

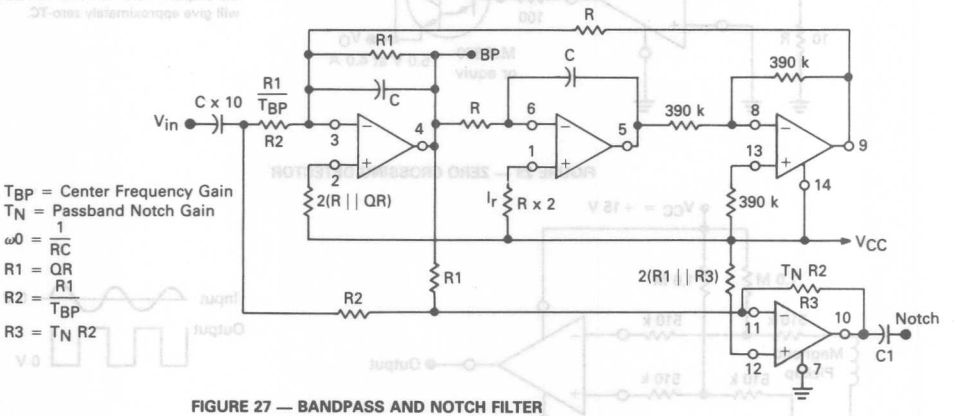
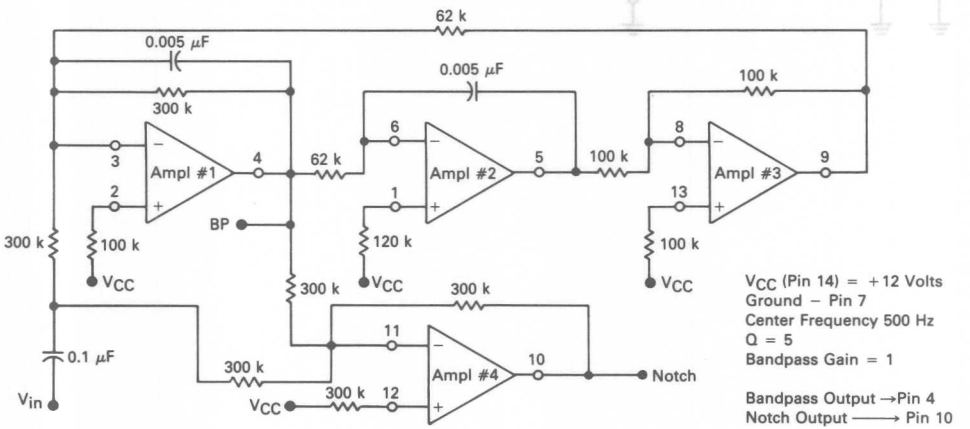


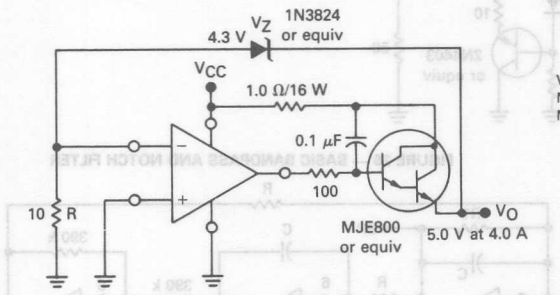
FIGURE 27 — BANDPASS AND NOTCH FILTER



2

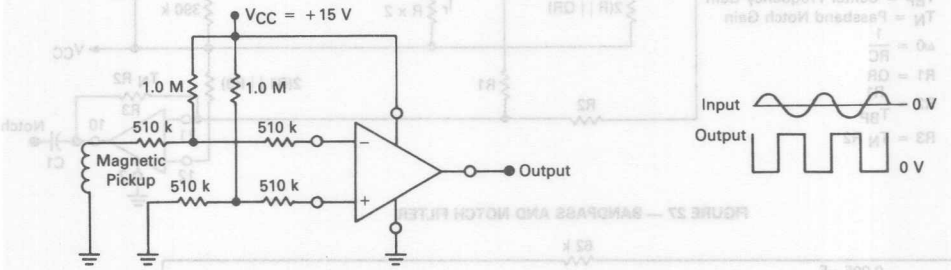
TYPICAL APPLICATIONS (continued)

FIGURE 28 — VOLTAGE REGULATOR



$V_O = V_Z + 0.6$ Vdc
NOTE 1: R is used to bias the zener.
NOTE 2: If the Zener TC is positive, and equal in magnitude to the negative TC of the input to the operational amplifier (≈2.0 mV/°C), the output is zero-TC. A 7.0 Volt Zener will give approximately zero-TC.

FIGURE 29 — ZERO CROSSING DETECTOR



MC3302 For Specifications, See LM139 Data.

MOTOROLA

MC3403
MC3503
MC3303

2

Specifications and Applications Information

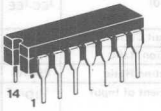
QUAD LOW POWER OPERATIONAL AMPLIFIERS

The MC3503 is a low-cost, quad operational amplifier with true differential inputs. The device has electrical characteristics similar to the popular MC1741. However, the MC3503 has several distinct advantages over standard operational amplifier types in single supply applications. The quad amplifier can operate at supply voltages as low as 3.0 Volts or as high as 36 Volts with quiescent currents about one third of those associated with the MC1741 (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

- Short Circuit Protected Outputs
- Class AB Output Stage for Minimal Crossover Distortion
- True Differential Input Stage
- Single Supply Operation: 3.0 to 36 Volts
- Split Supply Operation: ±1.5 to ±18 Volts
- Low Input Bias Currents: 500 nA Max
- Four Amplifiers Per Package
- Internally Compensated
- SImilar Performance to Popular MC1741
- Industry Standard Pinouts

QUAD DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

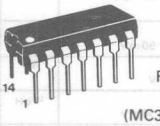
SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 632-08

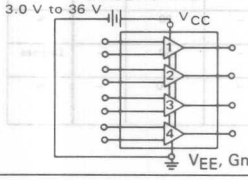


D SUFFIX
PLASTIC PACKAGE
CASE 751A-02
SO-14

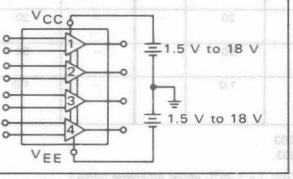


P SUFFIX
PLASTIC PACKAGE
CASE 646-06
(MC3403 and MC3303 Only)

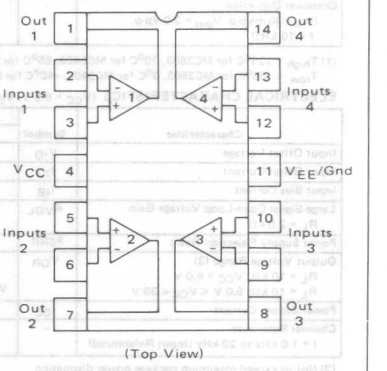
SINGLE SUPPLY



SPLIT SUPPLIES



PIN CONNECTIONS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltages			Vdc
Single Supply	V_{CC}	36	
Split Supplies	V_{CC}	+18	
	V_{EE}	-18	
Input Differential Voltage Range (1)	V_{IDR}	±36	Vdc
Input Common Mode Voltage Range (1) (2)	V_{ICR}	±18	Vdc
Storage Temperature Range	T_{stg}		°C
Ceramic Package		-65 to +150	
Plastic Package		-55 to +125	
Operating Ambient Temperature Range	T_A		°C
MC3503		-55 to +125	
MC3403		0 to +70	
MC3303		-40 to +85	
Junction Temperature	T_J		°C
Ceramic Package		175	
Plastic Package		150	

(1) Split Power Supplies.
(2) For Supply Voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

ORDERING INFORMATION

Type	Temperature Range	Package
MC3303L	−40°C to +85°C	Ceramic DIP
MC3303P	−40°C to +85°C	Plastic DIP
MC3403D	0°C to +70°C	SO-14
MC3403L	0°C to +70°C	Ceramic DIP
MC3403P	0°C to +70°C	Plastic DIP
MC3503L	−55°C to +125°C	Ceramic DIP

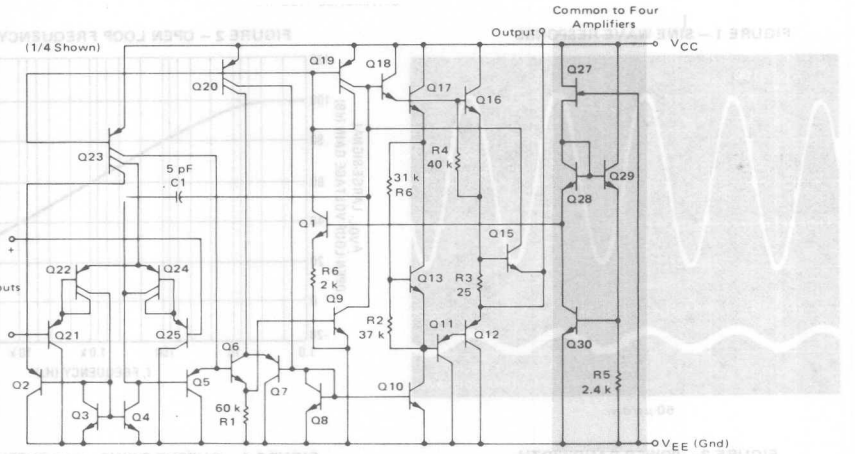
Characteristic	Symbol	MC3503			MC3403			MC3303			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	–	2.0	5.0	–	2.0	10	–	2.0	8.0	mV
$T_A = T_{high}$ to T_{low} (1)		–	–	6.0	–	–	12	–	–	10	
Input Offset Current	I_{IO}	–	30	50	–	30	50	–	30	75	nA
$T_A = T_{high}$ to T_{low}		–	–	200	–	–	200	–	–	250	
Large Signal Open-Loop Voltage Gain	A_{VOL}										V/mV
$V_O = \pm 10$ V, $R_L = 2.0$ kΩ,		50	200	–	20	200	–	20	200	–	
$T_A = T_{high}$ to T_{low}		25	–	–	15	–	–	15	–	–	
Input Bias Current	I_{IB}	–	-200	-500	–	-200	-500	–	-200	-500	nA
$T_A = T_{high}$ to T_{low}		–	-300	-1500	–	–	-800	–	–	-1000	
Output Impedance	z_o	–	75	–	–	75	–	–	75	–	Ω
f = 20 Hz											
Input Impedance	z_i	0.3	1.0	–	0.3	1.0	–	0.3	1.0	–	MΩ
f = 20 Hz											
Output Voltage Range	V_{OR}										V
$R_L = 10$ kΩ		±12	±13.5	–	±12	±13.5	–	+12	+12.5	–	
$R_L = 2.0$ kΩ		±10	±13	–	±10	±13	–	+10	+12	–	
$R_L = 2.0$ kΩ, $T_A = T_{high}$ to T_{low}		±10	–	–	±10	–	–	+10	–	–	
Input Common-Mode Voltage Range	V_{ICR}	+13 V -V_{EE}	+13.5 V -V_{EE}	–	+13 V -V_{EE}	+13.5V -V_{EE}	–	+12 V -V_{EE}	+12.5V -V_{EE}	–	V
Common-Mode Rejection Ratio	CMRR	70	90	–	70	90	–	70	90	–	dB
$R_S \leq 10$ kΩ											
Power Supply Current ($V_O = 0$)	I_{CC},I_{EE}	–	2.8	4.0	–	2.8	7.0	–	2.8	7.0	mA
$R_L = \infty$											
Individual Output Short-Circuit Current (2)	$I_{OS\pm}$	±10	±30	±45	±10	±20	±45	±10	±30	±45	mA
Positive Power Supply Rejection Ratio	PSRR+	–	30	150	–	30	150	–	30	150	μV/V
Negative Power Supply Rejection Ratio	PSRR-	–	30	150	–	30	150	–	–	–	μV/V
Average Temperature Coefficient of Input Offset Current	$\Delta I_{IO}/\Delta T$	–	50	–	–	50	–	–	50	–	pA/°C
$T_A = T_{high}$ to T_{low}											
Average Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	–	10	–	–	10	–	–	10	–	μV/°C
$T_A = T_{high}$ to T_{low}											
Power Bandwidth	BWp	–	9.0	–	–	9.0	–	–	9.0	–	kHz
$A_V = 1$, $R_L = 2.0$ kΩ, $V_O = 20$ V(p-p), THD = 5%											
Small-Signal Bandwidth	BW	–	1.0	–	–	1.0	–	–	1.0	–	MHz
$A_V = 1$, $R_L = 10$ kΩ, $V_O = 50$ mV											
Slew Rate	SR	–	0.6	–	–	0.6	–	–	0.6	–	V/μs
$A_V = 1$, $V_i = -10$ V to +10 V											
Rise Time	t_{TLH}	–	0.35	–	–	0.35	–	–	0.35	–	μs
$A_V = 1$, $R_L = 10$ kΩ, $V_O = 50$ mV											
Fall Time	t_{THL}	–	0.35	–	–	0.35	–	–	0.35	–	μs
$A_V = 1$, $R_L = 10$ kΩ, $V_O = 50$ mV											
Overshoot	OS	–	20	–	–	20	–	–	20	–	%
$A_V = 1$, $R_L = 10$ kΩ, $V_O = 50$ mV											
Phase Margin	φm	–	60	–	–	60	–	–	60	–	Degrees
$A_V = 1$, $R_L = 2.0$ kΩ, $C_L = 200$ pF											
Crossover Distortion	–	–	1.0	–	–	1.0	–	–	1.0	–	%
($V_{in} = 30$ mVp-p, $V_{out} = 2.0$ Vp-p, f = 10 kHz)											

(1) T_{high} = 125°C for MC3503, 70°C for MC3403, 85°C for MC3303
T_{low} = -55°C for MC3503, 0°C for MC3403, -40°C for MC3303

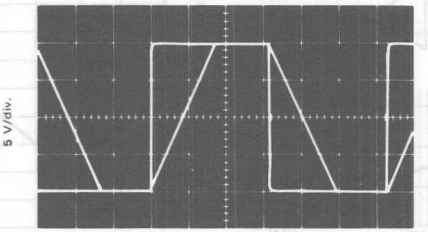
ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	MC3503			MC3403			MC3303			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	–	2.0	5.0	–	2.0	10	–	–	10	mV
Input Offset Current	I_{IO}	–	30	50	–	30	50	–	–	75	nA
Input Bias Current	I_{IB}	–	-200	-500	–	-200	-500	–	–	-500	nA
Large-Signal Open-Loop Voltage Gain	A_{VOL}	10	200	–	10	200	–	10	200	–	V/mV
$R_L = 2.0$ kΩ											
Power Supply Rejection Ratio	PSRR	–	–	150	–	–	150	–	–	150	μV/V
Output Voltage Range (3)	V_{OR}										Vp-p
$R_L = 10$ kΩ, $V_{CC} = 5.0$ V		3.3	3.5	–	3.3	3.5	–	3.3	3.5	–	
$R_L = 10$ kΩ, 5.0 V ≤ V_{CC} ≤ 30 V		$V_{CC}-2.0$	$V_{CC}-1.7$	–	$V_{CC}-2.0$	$V_{CC}-1.7$	–	$V_{CC}-2.0$	$V_{CC}-1.7$	–	
Power Supply Current	I_{CC}	–	2.5	4.0	–	2.5	7.0	–	2.5	7.0	mA
Channel Separation	–	–	-120	–	–	-120	–	–	-120	–	dB
f = 1.0 kHz to 20 kHz (Input Referenced)											

(2) Not to exceed maximum package power dissipation.
(3) Output will swing to ground



INVERTER PULSE RESPONSE



20 μs/div.

CIRCUIT DESCRIPTION

The MC3503/3403/3303 is made using four internally compensated, two-stage operational amplifiers. The first stage of each consists of differential input devices Q24 and Q22 with input buffer transistors Q25 and Q21 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance a smaller compensation capacitor (only 5 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q24 and Q22. Another feature of this input stage is that the input common-mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single-ended converter. The second stage consists of a standard current source load amplifier stage.

The output stage is unique because it allows the output to swing to ground in single supply operation and yet does not exhibit any crossover distortion in split supply operation. This is possible because class AB operation is utilized.

Each amplifier is biased from an internal-voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

2

TYPICAL PERFORMANCE CURVES

FIGURE 1 – SINE WAVE RESPONSE

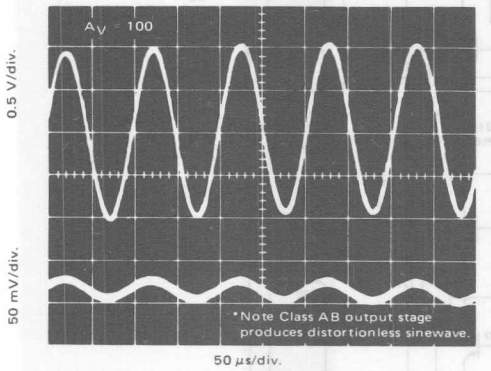


FIGURE 2 – OPEN LOOP FREQUENCY RESPONSE

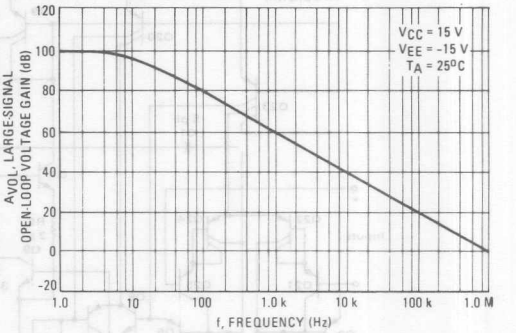


FIGURE 3 – POWER BANDWIDTH

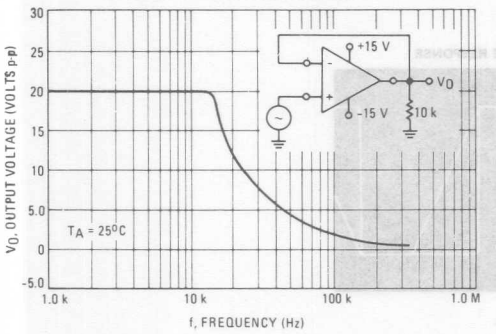


FIGURE 4 – OUTPUT SWING versus SUPPLY VOLTAGE

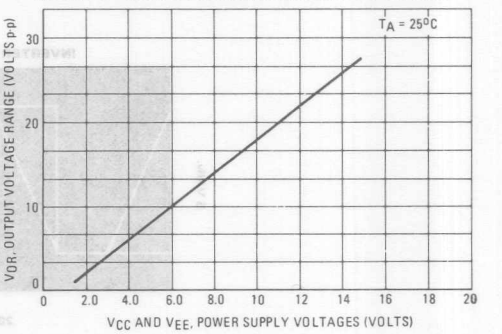


FIGURE 5 – INPUT BIAS CURRENT versus TEMPERATURE

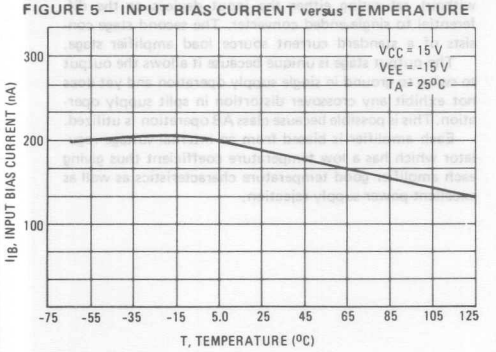
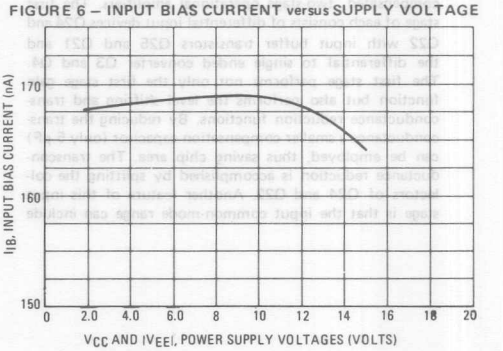
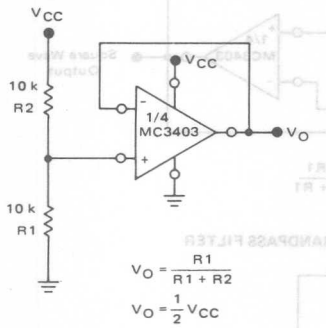


FIGURE 6 – INPUT BIAS CURRENT versus SUPPLY VOLTAGE



APPLICATIONS INFORMATION

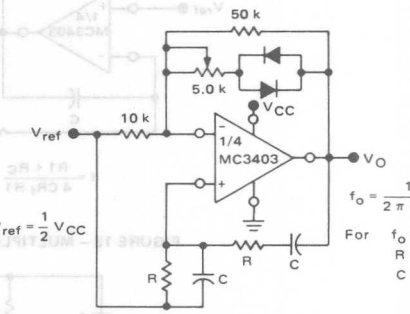
FIGURE 7 – VOLTAGE REFERENCE



$$V_O = \frac{R1}{R1 + R2}$$

$$V_O = \frac{1}{2} V_{CC}$$

FIGURE 8 — WIEN BRIDGE OSCILLATOR

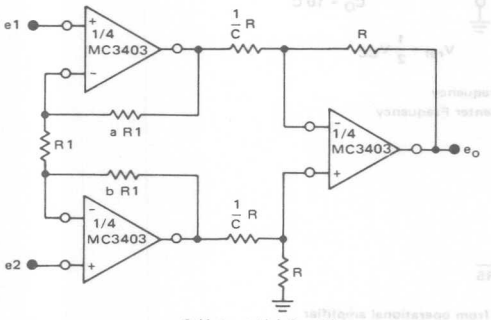


$$V_{ref} = \frac{1}{2} V_{CC}$$

$$f_o = \frac{1}{2 \pi RC}$$

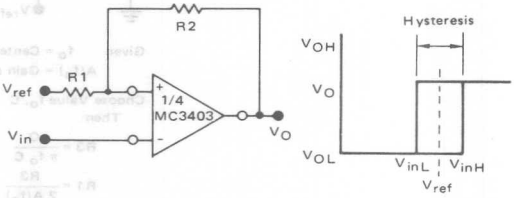
For f_o = 1 kHz
R = 16 kΩ
C = 0.01 μF

FIGURE 9 – HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER



$$e_o = C (1 + a + b) (e2 - e1)$$

FIGURE 10 – COMPARATOR WITH HYSTERESIS

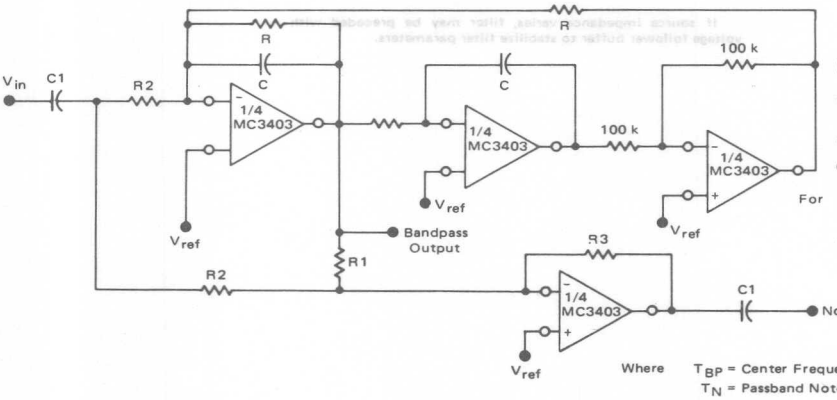


$$V_{inL} = \frac{R1}{R1 + R2} (V_{OL} - V_{ref}) + V_{ref}$$

$$V_{inH} = \frac{R1}{R1 + R2} (V_{OH} - V_{ref}) + V_{ref}$$

$$H = \frac{R1}{R1 + R2} (V_{OH} - V_{OL})$$

FIGURE 11 – BI-QUAD FILTER



$$f_o = \frac{1}{2 \pi RC}$$

R1 = QR

$$R2 = \frac{R1}{T_{BP}}$$

$$R3 = T_N R2$$

C1 = 10 C

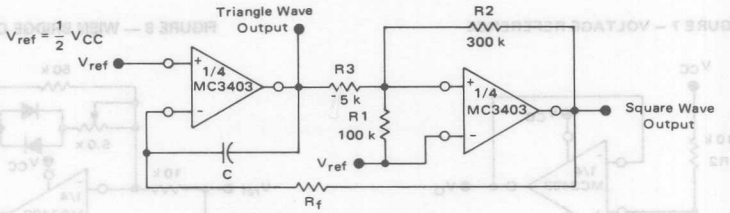
$$V_{ref} = \frac{1}{2} V_{CC}$$

For f_o = 1 kHz
Q = 10
T_{BP} = 1
T_N = 1

R = 160 kΩ
C = 0.001 μF
R1 = 1.6 MΩ
R2 = 1.6 MΩ
R3 = 1.6 MΩ

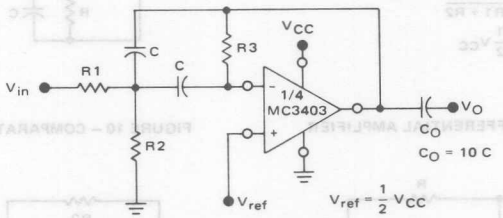
Where T_{BP} = Center Frequency Gain
T_N = Passband Notch Gain

FIGURE 12 – FUNCTION GENERATOR



$$f = \frac{R1 + RC}{4\,CR_f\,R1} \quad \text{if} \quad R3 = \frac{R2\,R1}{R2 + R1}$$

FIGURE 13 – MULTIPLE FEEDBACK BANDPASS FILTER



Given f_o = Center Frequency
$A(f_o)$ = Gain at Center Frequency

Choose Value f_o, C
Then:

$$R3 = \frac{Q}{\pi\, f_o\, C}$$

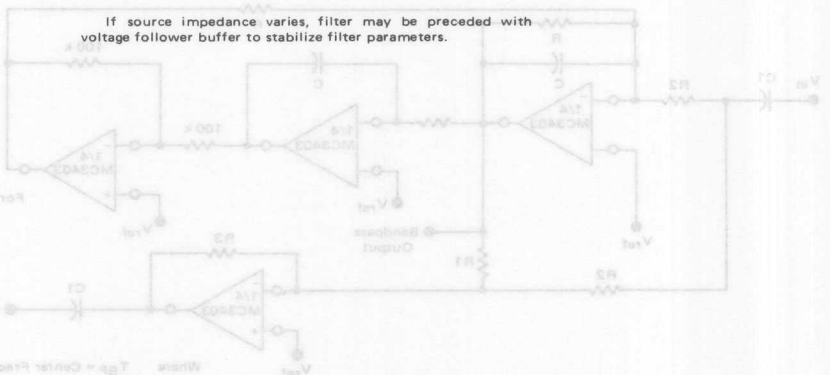
$$R1 = \frac{R3}{2\,A(f_o)}$$

$$R2 = \frac{R1\,R5}{4Q^2\,R1 - R5}$$

For less than 10% error from operational amplifier

$$\frac{Q_o\, f_o}{BW} < 0.1$$ Where f_o and BW are expressed in Hz.

If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.



DUAL OPERATIONAL AMPLIFIER AND DUAL COMPARATOR

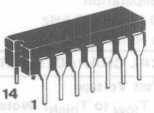
The MC3405/3505 contains two differential-input operational amplifiers and two comparators, each set capable of single supply operation. This operational amplifier-comparator circuit fulfills its applications as a general purpose product for automotive and consumer circuits as well as an industrial building block.

The MC3405 is specified over the commercial operating temperature range of 0 to +70°C, while the MC3505 is specified over the military operating range of −55 to +125°C.

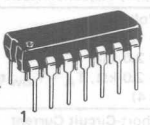
- Operational Amplifiers Equivalent in Performance to MC3403/3503
- Comparators Similar in Performance to LM339/139
- Single Supply Operation: 3.0 to 36 Volts
- Split Supply Operation: ±1.5 to ±18 Volts
- Low Supply Current Drain
- Operational Amplifiers Are Internally Frequency Compensated
- Comparators TTL and CMOS Compatible

DUAL OPERATIONAL AMPLIFIER AND DUAL VOLTAGE COMPARATOR

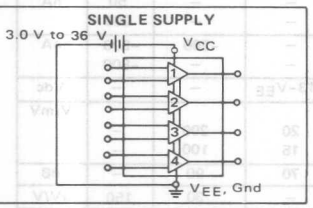
SILICON MONOLITHIC INTEGRATED CIRCUIT

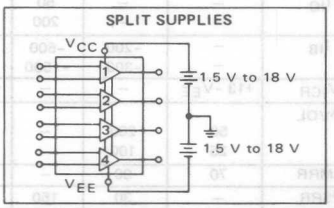


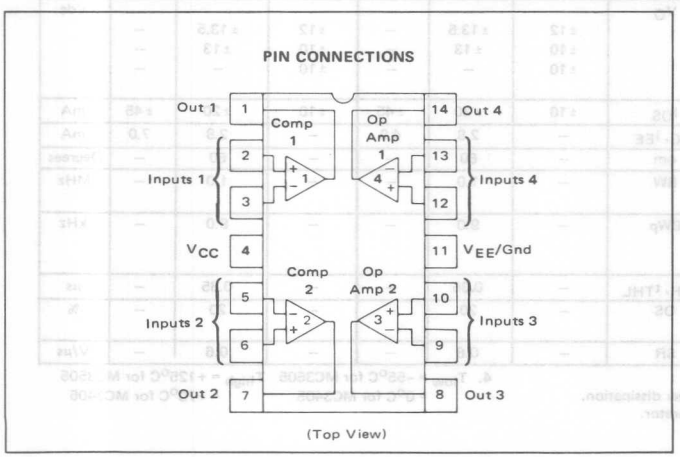
L SUFFIX
CERAMIC PACKAGE
CASE 632-08



P SUFFIX
PLASTIC PACKAGE
CASE 646-06







ORDERING INFORMATION

Device	Temperature Range	Package
MC3405L	0 to +70°C	Ceramic DIP
MC3405P	0 to +70°C	Plastic DIP
MC3505L	−55 to +125°C	Ceramic DIP

2

OPERATIONAL AMPLIFIER SECTION

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage—Single Supply Split Supplies	V_{CC} V_{CC}, V_{EE}	36 ±18	Vdc
Input Differential Voltage Range	V_{IDR}	±36	Vdc
Input Common Mode Voltage Range	V_{ICR}	±18	Vdc
Operating Ambient Temperature Range—MC3505 MC3405	T_A	-55 to +125 0 to +70	°C
Storage Temperature Range—Ceramic Package Plastic Package	T_{stg}	-65 to +150 -55 to +125	°C
Operating Junction Temperature Range—Ceramic Package Plastic Package	T_J	175 150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	MC3505 Min	MC3505 Typ	MC3505 Max	MC3405 Min	MC3405 Typ	MC3405 Max	Unit
Input Offset Voltage	V_{IO}	–	2.0	5.0	–	2.0	10	mV
Input Offset Current	I_{IO}	–	30	50	–	30	50	nA
Input Bias Current	I_{IB}	–	-200	-500	–	-200	-500	nA
Large-Signal Open-Loop Voltage Gain (R_L = 2.0 kΩ)	A_{VOL}	20	200	–	20	200	–	V/mV
Power Supply Rejection Ratio	PSRR	–	–	150	–	–	150	μV/V
Output Voltage Range (Note 1) (R_L = 10 kΩ, V_{CC} = 5.0 V) (R_L = 10 kΩ, 5.0 V ≤ V_{CC} ≤ 30 V)	V_{OR}	 3.3 V_{CC}-2.0	 3.5 V_{CC}-1.7	 – –	 3.3 V_{CC}-2.0	 3.5 V_{CC}-1.7	 – –	Vp-p
Power Supply Current (Notes 2 and 3)	I_{CC}	–	2.5	4.0	–	2.5	7.0	mA
Channel Separation f = 1.0 kHz to 20 kHz (Input Referenced)	–	–	-120	–	–	-120	–	dB

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = -15 V, T_A = 25°C unless otherwise noted)

Input Offset Voltage (T_A = T_{low} to T_{high}) (Note 4)	V_{IO}	– –	2.0 –	5.0 6.0	– –	2.0 –	10 12	mV
Average Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	–	15	–	–	15	–	μV/°C
Input Offset Current (T_A = T_{low} to T_{high}) (Note 4)	I_{IO}	– –	– –	50 200	– –	– –	50 200	nA
Input Bias Current (T_A = T_{low} to T_{high} (Note 4)	I_{IB}	– –	-200 -300	-500 -1500	– –	-200 –	-500 -800	nA
Input Common Mode Voltage Range	V_{ICR}	+13 -V_{EE}	–	–	+13-V_{EE}	–	–	Vdc
Large Signal Open Loop Voltage Gain (V_O = ±10 V, R_L = 2.0 kΩ) (T_A = T_{low} to T_{high}) (Note 4)	A_{VOL}	 50 25	 200 100	 – –	 20 15	 200 100	 – –	V/mV
Common Mode Rejection Ratio	CMRR	70	90	–	70	90	–	dB
Power Supply Rejection Ratio	PSRR	–	30	150	–	30	150	μV/V
Output Voltage (R_L = 10 kΩ) (R_L = 2.0 kΩ) (R_L = 2.0 kΩ, T_A = T_{low} to T_{high}) (Note 4)	V_O	 ±12 ±10 ±10	 ±13.5 ±13 –	 – – –	 ±12 ±10 ±10	 ±13.5 ±13 –	 – – –	Vdc
Output Short-Circuit Current	I_{OS}	±10	±30	±45	±10	±20	±45	mA
Power Supply Current (Notes 2 and 3)	I_{CC}, I_{EE}	–	2.8	4.0	–	2.8	7.0	mA
Phase Margin	ϕm	–	60	–	–	60	–	Degrees
Small-Signal Bandwidth (A_V = 1, R_L = 10 kΩ, V_O = 50 mV)	BW	–	1.0	–	–	1.0	–	MHz
Power Bandwidth (A_V = 1, R_L = 2.0 kΩ, V_O = 20 V (p-p), THD = 5%)	BWp	–	9.0	–	–	9.0	–	kHz
Rise Time/Fall Time	t_{TLH}, t_{THL}	–	0.35	–	–	0.35	–	μs
Overshoot (A_V = 1, R_L = 10 kΩ, V_O = 50 mV)	OS	–	20	–	–	20	–	%
Slew Rate	SR	–	0.6	–	–	0.6	–	V/μs

NOTES: 1. Output will swing to ground
2. Not to exceed maximum package power dissipation.
3. For Operational Amplifier and Comparator.
4. T_{low} = -55°C for MC3505, T_{high} = +125°C for MC3505
= 0°C for MC3405 = +70°C for MC3405

COMPARATOR SECTION

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage—Single Supply Split Supplies	V_{CC} V_{CC}, V_{EE}	36 ±18	Vdc
Input Differential Voltage Range	V_{IDR}	±36	Vdc
Input Common Mode Voltage Range	V_{ICR}	-0.3 to +36	Vdc
Sink Current	I_{sink}	20	mA
Operating Ambient Temperature Range—MC3505 MC3405	T_A	-55 to +125 0 to +70	°C
Storage Temperature Range—Ceramic Package Plastic Package	T_{stg}	-65 to +150 -55 to +125	°C
Operating Junction Temperature Range—Ceramic Package Plastic Package	T_J	175 150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	MC3505			MC3405			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	–	2.0	5.0	–	2.0	10	mV
(T_A = T_{low} to T_{high}) (Notes 1 and 2)		–	–	9.0	–	–	12	
Average Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	–	15	–	–	15	–	μV/°C
Input Offset Current	I_{IO}	–	50	75	–	50	100	nA
(T_A = T_{low} to T_{high}) (Note 1)		–	–	150	–	–	200	
Input Bias Current	I_{IB}	–	-125	-500	–	-125	-500	nA
(T_A = T_{low} to T_{high}) (Note 1)		–	–	-1500	–	–	-800	
Input Common Mode Voltage Range	V_{ICR}	0	V_{CC} -1.5	V_{CC} -1.7	0	V_{CC} -1.5	V_{CC} -1.7	Vp-p
(T_A = T_{low} to T_{high}) (Note 1)		0	V_{CC} -1.7	V_{CC} -2.0	0	V_{CC} -1.7	V_{CC} -2.0	
Input Differential Voltage	V_{ID}	–	–	36	–	–	36	V
(All V_{in} ≥ 0 Vdc)								
Large-Signal Open-Loop Voltage Gain	A_{VOL}	–	200	–	–	200	–	V/mV
(R_L = 15 kΩ)								
Output Sink Current	I_{sink}	6.0	16	–	6.0	16	–	mA
(V_{in} (-) ≥ 1.0 Vdc, V_{in} (+) = 0, V_O ≤ 1.5 V)								
Low Level Output Voltage	V_{OL}							mV
(V_{in} (+) = 0 V, V_{in} (-) = 1.0 V, I_{sink} = 4.0 mA)		–	350	500	–	350	500	
(T_A = T_{low} to T_{high}) (Note 1)		–	–	700	–	–	700	
Output Leakage Current	I_{OL}							μA
(V_{in} (+) ≥ 1.0 Vdc, V_{in} (-) = 0, V_O = 5.0 Vdc)		–	0.1	1.0	–	0.1	1.0	
(T_A = T_{low} to T_{high}) (Note 1)		–	0.1	1.0	–	0.1	1.0	
Large-Signal Response	–	–	300	–	–	300	–	ns
Response Time (Note 3)	–	–	1.3	–	–	1.3	–	μs
(V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ)								

NOTES: 1. T_{low} = -55°C for MC3505 T_{high} = +125°C for MC3505
= 0°C for MC3405 = +70°C for MC3405

2. V_O ≅ 1.4 V, R_S = 0 Ω with V_{CC} from 5.0 Vdc to 30 Vdc, and over the input common mode range 0 to V_{CC} -1.7 V.

3. The response time specified is for a 100 mV input step with 5.0 mV overdrive. For larger signals 300 ns is typical.

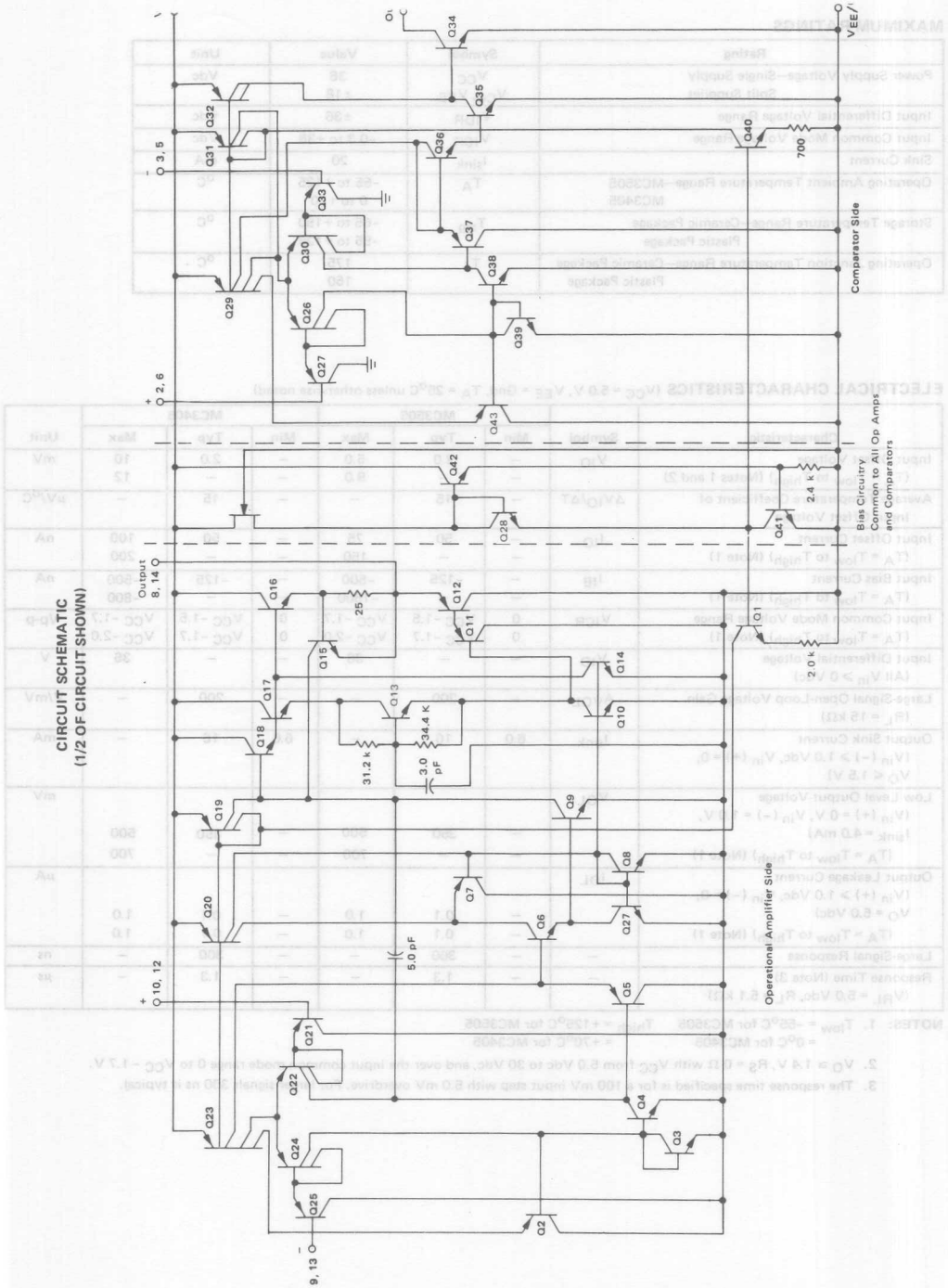

CIRCUIT SCHEMATIC
(1/2 OF CIRCUIT SHOWN)
Output
8, 14
3, 5
2, 6
10, 12
9, 13
Comparator Side
Bias Circuitry
Common to All Op Amps
and Comparators
Operational Amplifier Side
700
2.4 k
2.0 k
25
31.2 k
34.4 k
3.0 pF
5.0 pF

FIGURE 1 – SINE WAVE RESPONSE

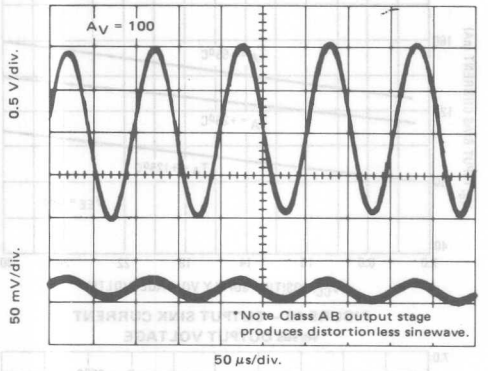


FIGURE 2 – OPEN LOOP FREQUENCY RESPONSE

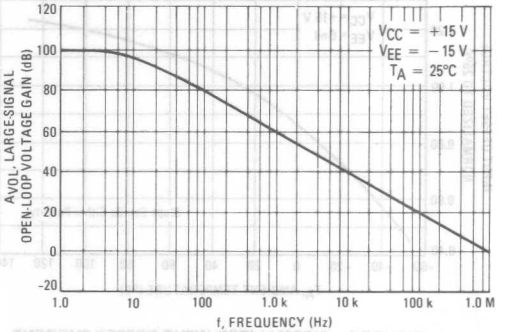


FIGURE 3 – POWER BANDWIDTH

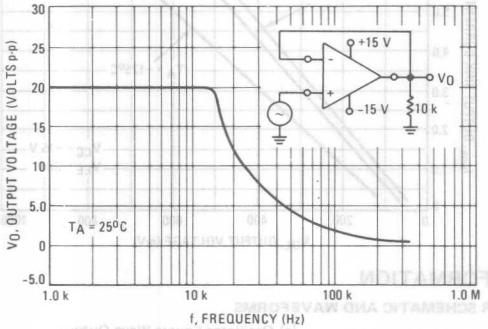


FIGURE 4 – OUTPUT SWING versus SUPPLY VOLTAGE

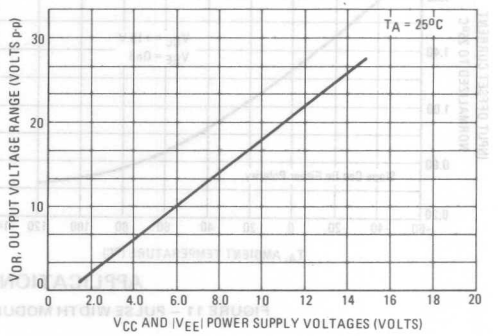


FIGURE 5 – INPUT BIAS CURRENT versus TEMPERATURE

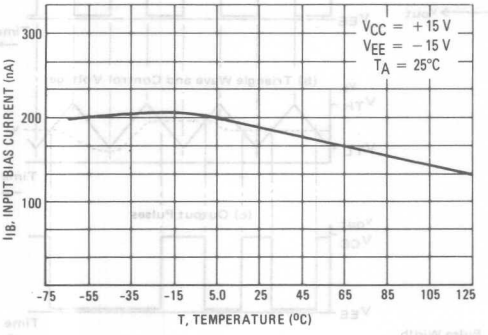
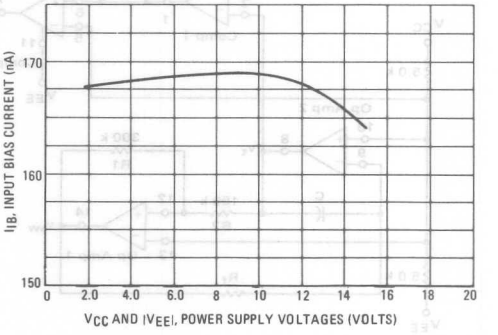


FIGURE 6 – INPUT BIAS CURRENT versus SUPPLY VOLTAGE



2

COMPARATOR SECTION

TYPICAL PERFORMANCE CURVES

FIGURE 7 – NORMALIZED INPUT OFFSET VOLTAGE

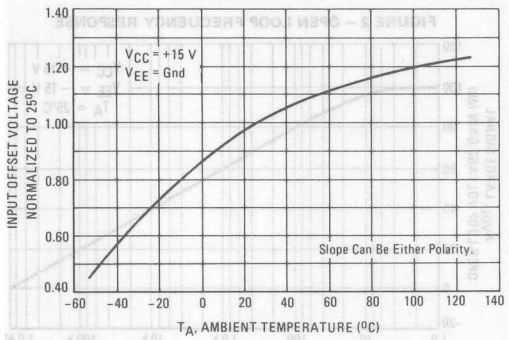


FIGURE 8 – INPUT BIAS CURRENT

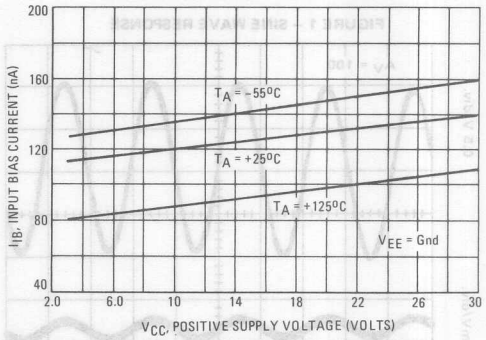


FIGURE 9 – NORMALIZED INPUT OFFSET CURRENT

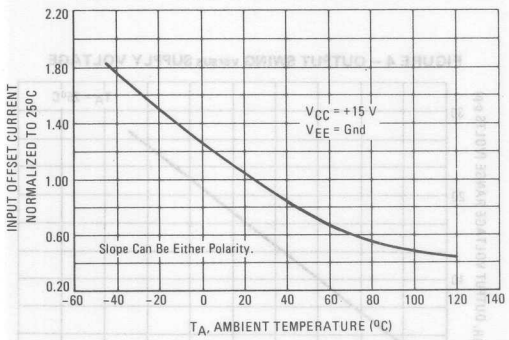
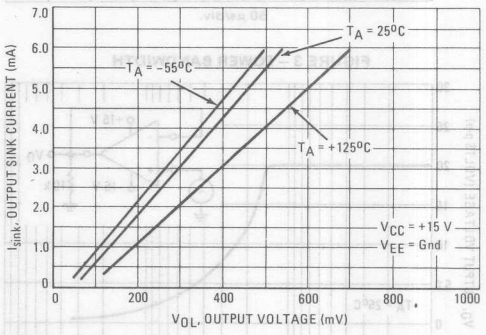
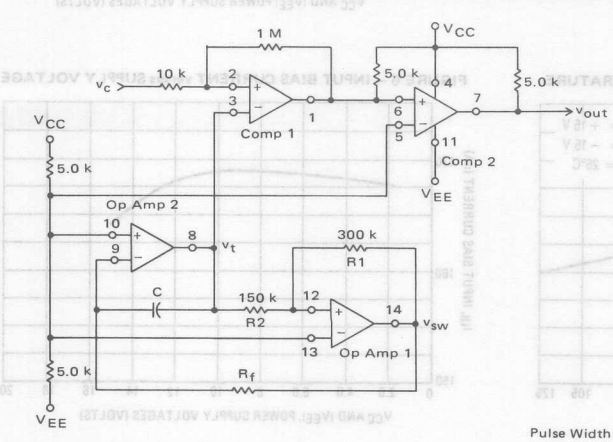


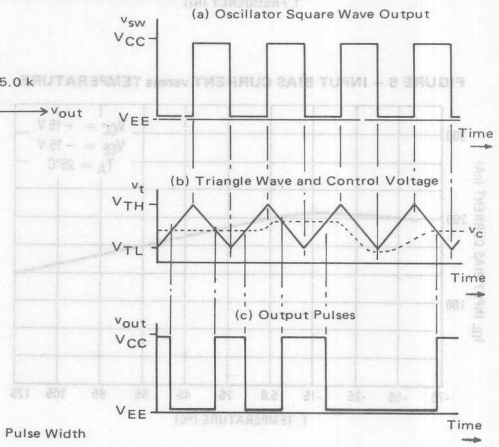
FIGURE 10 – OUTPUT SINK CURRENT versus OUTPUT VOLTAGE



APPLICATIONS INFORMATION

FIGURE 11 – PULSE WIDTH MODULATOR SCHEMATIC AND WAVEFORMS





Pulse Width

$$V_{TH} = \frac{1}{2}V_S(1 + R2/R1) + V_{EE} \qquad V_S = V_{CC} - V_{EE}$$

$$V_{TL} = \frac{1}{2}V_S(1 - R2/R1) + V_{EE}$$

Oscillator Frequency

$$f = \frac{R1}{4R_fCR2}$$

$$P.W. = \left(\frac{1}{f}\right)\left(\frac{v_c - V_{TL}}{V_{TH} - V_{TL}}\right) \quad \text{When: } V_{TL} < V_C < V_{TH}$$

Duty Cycle in %

$$D.C. = \left(\frac{v_c - V_{TL}}{V_{TH} - V_{TL}}\right)(100)$$

FIGURE 12 – WINDOW COMPARATOR

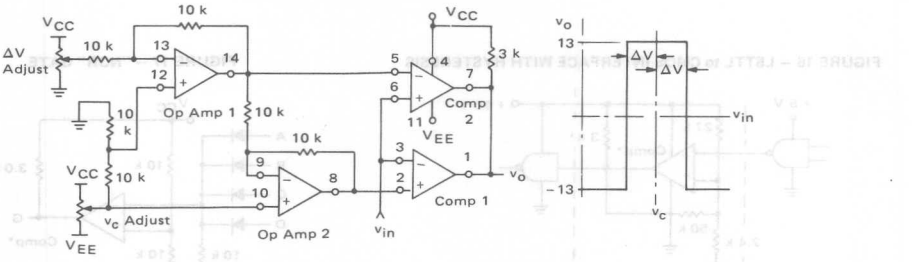
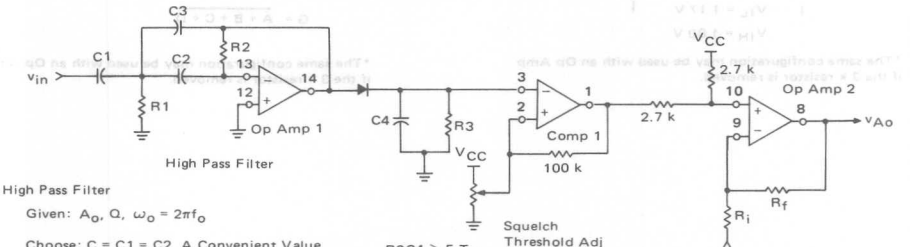


FIGURE 13 – SQUELCH CIRCUIT FOR AM OR FM



High Pass Filter

High Pass Filter

Given: A_o, Q, $\omega_o = 2\pi f_o$

Choose: C = C1 = C2, A Convenient Value

Calculate: $R2 = \frac{Q}{\omega_o C}(2A_o + 1)$

$C3 = \frac{C}{A_o}$

$R1 = \frac{A_o}{Q\omega_o C(2A_o + 1)}$

$R3C4 > 5\,T_{in}$

Where: T_{in} is the period of v_{in}

Q = Quality Factor

A_o = High Frequency Gain

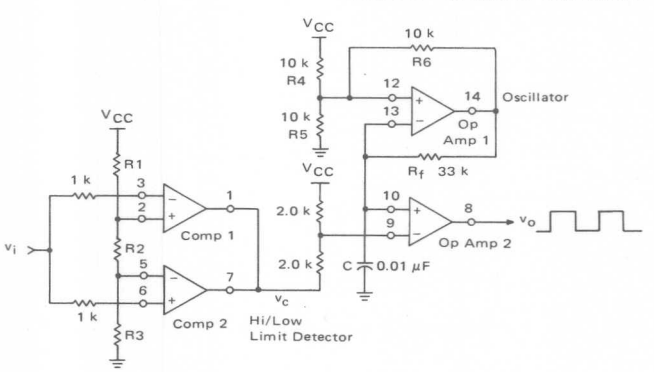
ω_o = Break Frequency

Switched Audio Stage

Gain of Audio Stage

$A_{cl} = -\frac{R_f}{R_i}$

FIGURE 14 – HIGH/LOW LIMIT ALARM





$V_{IL} = V_{CC}\frac{R3}{R1 + R2 + R3}$

$V_{IH} = V_{CC}\frac{R2 + R3}{R1 + R2 + R3}$

Oscillator

If R4 = R5 = R6

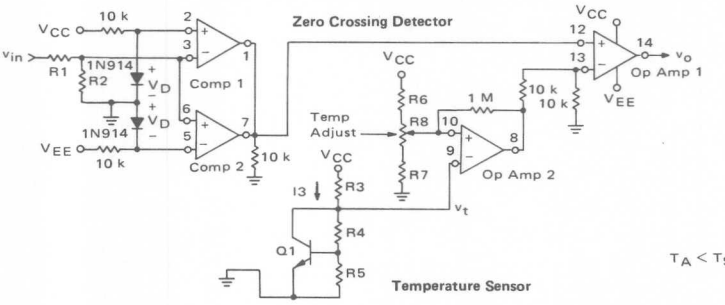
$f = 0.72/R_fC$

As Shown, f = 2.2 kHz

v_o Will Oscillate If $V_{IH} < v_i$, or $V_{IL} > v_i$

v_o Will Be Low If $V_{IL} < v_i < V_{IH}$

FIGURE 15 – ZERO CROSSING DETECTOR WITH TEMPERATURE SENSOR



$v_t = (V_{BE}\text{ of Q1})\left(\frac{R4 + R5}{R5}\right)$

$I3 > \frac{2V_{BE}}{R5}$

R1 and R2 control the switching voltage of the zero crossing detector

$\pm V_s = \pm V_D\frac{R1 + R2}{R2}$

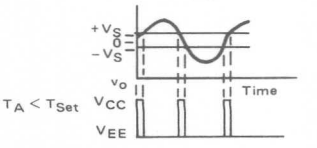
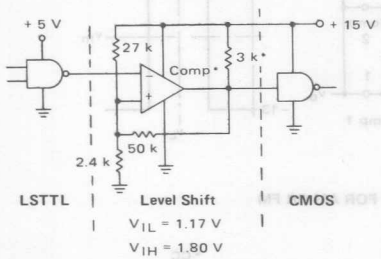
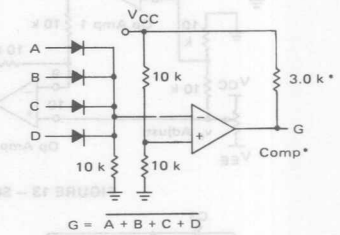


FIGURE 16 – LSTTL to CMOS INTERFACE WITH HYSTERESIS



*The same configuration may be used with an Op Amp if the 3 k resistor is removed.

FIGURE 17 – "NOR" GATE



$G = \overline{A + B + C + D}$

*The same configuration may be used with an Op Amp if the 3 k resistor is removed.

MOTOROLA

MC3430 thru MC3433

2

QUAD DIFFERENTIAL VOLTAGE COMPARATOR/SENSE AMPLIFIERS

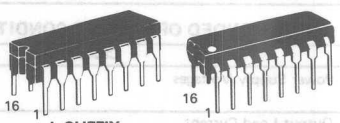
The MC3430 thru MC3433 high-speed comparators are ideal for application as sense amplifiers in MOS memory systems. They are specified in a unique way which combines the effects of input offset voltage, input offset current, voltage gain, temperature variations and input common-mode range into a single functional parameter. This parameter, called Input Sensitivity, specifies a minimum differential input voltage which will guarantee a given logic state. Four variations are offered in the comparator series.

The MC3430 and MC3431 versions feature a three-state strobe input common to all four channels which can be used to place the four outputs in a high-impedance state. These two devices use active-pull-up MTTL compatible outputs. The MC3432 and MC3433 are open-collector types which permit the implied AND connection. The MC3430 and MC3432 versionsare specified for a ±7.0 mV input sensitivity over the 0 to 70°C temperature range, while the MC3431 and MC3433 are specified for ±12 mV.

- Propagation Delay Time – 40 ns
- Outputs Specified for a Fanout of 10 (MC7400 type loads)
- Specified for all conditions of ±5% Power Supply Variations, Operating Temperature Range, Input Common-Mode Voltage Swing from -3.0 V to 3.0 V, and $R_S \leq 200$ ohms.

QUAD HIGH SPEED VOLTAGE COMPARATORS

SILICON MONOLITHIC INTEGRATED CIRCUITS



L SUFFIX
CERAMIC PACKAGE
CASE 620-10

P SUFFIX
PLASTIC PACKAGE
CASE 648-06

CONNECTION DIAGRAM

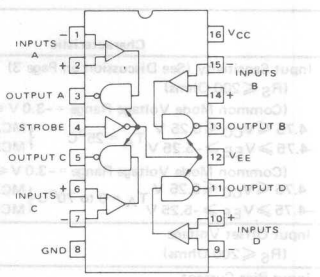
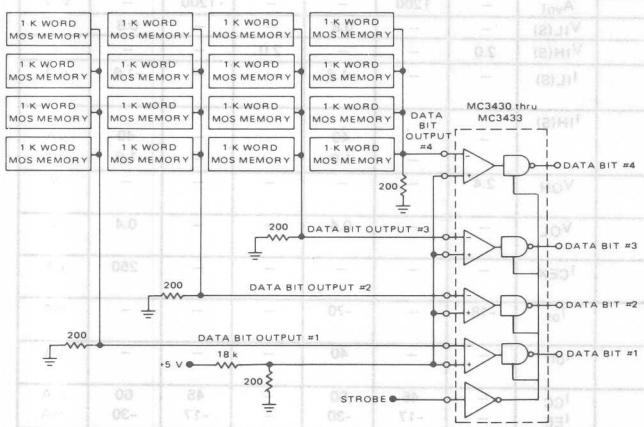


FIGURE 1 – A TYPICAL MOS MEMORY SENSING APPLICATION FOR A 4-K WORD BY 4-BIT MEMORY ARRANGEMENT EMPLOYING 1103 TYPE MEMORY DEVICES



Only four devices are required for a 4-k word by 16-bit memory system.

TRUTH TABLE
MC3430 and MC3432

Input	Strobe	Output	Device
$V_{ID} \geq 7.0$ mV	L	H	MC3430
	H	Z	
T_A = 0 to 70°C	L	Off	MC3432
	H	Off	
-7.0 mV $\leq V_{ID}$	L	I	MC3430
$\leq$ 7.0 mV	H	Z	
T_A = 0 to 70°C	L	I	MC3432
	H	Off	
$V_{ID} \leq$ -7.0 mV	L	L	MC3430
T_A = 0 to 70°C	H	Z	
	L	On	MC3432
	H	Off	

TRUTH TABLE
MC3431 and MC3433

Input	Strobe	Output	Device
$V_{ID} \geq 12$ mV	L	H	MC3431
T_A = 0 to 70°C	H	Z	
	L	Off	MC3433
	H	Off	
-12 mV $\leq V_{ID}$	L	I	MC3431
$\leq$ +12 mV	H	Z	
T_A = 0 to 70°C	L	I	MC3433
	H	Off	
$V_{ID} \leq$ -12 mV	L	L	MC3431
T_A = 0 to 70°C	H	Z	
	L	On	MC3433
	H	Off	

L = Low Logic State Z = Third (High Impedance)
H = High Logic State I = Indeterminate State
RS ≤ 200 Ω

2

MAXIMUM RATINGS (T_A = 0 to +70°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}, V_{EE}	±7.0	Vdc
Differential Mode Input Signal Voltage Range	V_{IDR}	±6.0	Vdc
Common-Mode Input Voltage Range	V_{ICR}	±5.0	Vdc
Strobe Input Voltage	$V_{I(S)}$	5.5	Vdc
Output Voltage (MC3432 – 33 versions)	V_O	+7.0	Vdc
Junction Temperature Ceramic Package Plastic Package	T_J	 175 150	°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltages	V_{CC} V_{EE}	+4.75 -4.75	+5.0 -5.0	+5.25 -5.25	Vdc
Output Load Current	I_{OL}	–	–	16	mA
Differential-Mode Input Voltage Range	V_{IDR}	-5.0	–	+5.0	Vdc
Common-Mode Input Voltage Range	V_{ICR}	-3.0	–	+3.0	Vdc
Input Voltage Range (any input to Ground)	V_{IR}	-5.0	–	+3.0	Vdc

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = −5.0 Vdc, T_A = 0°C to +70°C unless otherwise noted.)
Typical Values are Measured at T_A = 25°C

Characteristic	Symbol	MC3430, MC3431 Min	MC3430, MC3431 Typ	MC3430, MC3431 Max	MC3432, MC3433 Min	MC3432, MC3433 Typ	MC3432, MC3433 Max	Unit
Input Sensitivity (See Discussion on Page 3) ($R_S \leq 200$ Ohms)	V_{IS}							mV
(Common Mode Voltage Range = -3.0 V ≤ V_{in} ≤ 3.0 V) 4.75 ≤ V_{CC} ≤ 5.25 V, -4.75 ≥ V_{EE} ≥ -5.25 V, T_A = 25°C								
MC3430, MC3432		–	–	±6.0	–	–	±6.0	
MC3431, MC3433		–	–	±10	–	–	±10	
(Common Mode Voltage Range = -3.0 V ≤ V_{in} ≤ 3.0 V) 4.75 ≤ V_{CC} ≤ 5.25 V, -4.75 ≥ V_{EE} ≥ -5.25 V, T_A = 0 to 70°C								
MC3430, MC3432		–	–	±7.0	–	–	±7.0	
MC3431, MC3433		–	–	±12	–	–	±12	
Input Offset Voltage ($R_S \leq 200$ Ohms)	V_{IO}	–	2.0	–	–	2.0	–	mV
Input Bias Current (V_{CC} = 5.25 V, V_{EE} = -5.25 V)	I_{IB}							μA
MC3430, MC3432		–	20	40	–	20	40	
MC3431, MC3433		–	20	40	–	20	40	
Input Offset Current	I_{IO}	–	1.0	–	–	1.0	–	μA
Voltage Gain	A_{vol}	–	1200	–	–	1200	–	V/V
Strobe Input Voltage (Low State)	$V_{IL(S)}$	–	–	0.8	–	–	0.8	V
Strobe Input Voltage (High State)	$V_{IH(S)}$	2.0	–	–	2.0	–	–	V
Strobe Current (Low State) (V_{CC} = 5.25 V, V_{EE} = -5.25 V, V_{in} = 0.4 V)	$I_{IL(S)}$	–	–	-1.6	–	–	-1.6	mA
Strobe Current (High State)	$I_{IH(S)}$							
(V_{CC} = 5.25 V, V_{EE} = -5.25 V, V_{in} = 2.4 V)		–	–	40	–	–	40	μA
(V_{CC} = 5.25 V, V_{EE} = -5.25 V, V_{in} = 5.25 V)		–	–	1.0	–	–	1.0	mA
Output Voltage (High State) (I_O = -400 μA, V_{CC} = 4.75 V, V_{EE} = -4.75 V)	V_{OH}	2.4	–	–	–	–	–	V
Output Voltage (Low State) (I_O = 16 mA, V_{CC} = 4.75 V, V_{EE} = 4.75 V)	V_{OL}	–	–	0.4	–	–	0.4	V
Output Leakage Current (V_{CC} = 4.75 V, V_{EE} = -4.75 V, V_O = 5.25 V)	I_{CEX}	–	–	–	–	–	250	μA
Output Current Short Circuit (V_{CC} = 5.25 V, V_{EE} = -5.25 V)	I_{os}	-18	–	-70	–	–	–	mA
Output Disable Leakage Current (V_{CC} = 5.25 V, V_{EE} = -5.25 V)	I_{off}	–	–	40	–	–	–	μA
High Logic Level Supply Currents (V_{CC} = 5.25 V, V_{EE} = -5.25 V)	I_{CC}	–	45	60	–	45	60	mA
	I_{EE}	–	-17	-30	–	-17	-30	mA

A UNIQUE FUNCTIONAL PARAMETER FOR COMPARATORS

A unique approach is used in specifying the MC3430-33 quad comparators. Previously, comparators have been specified as linear devices with common operational amplifier type parameters such as voltage gain (A_{vol}), input offset voltage (V_{IO}), input offset current (I_{IO}) and common-mode rejection ratio (CMRR). This is true despite the fact that most comparators are seldom operated in their linear region because it is difficult to hold a high gain comparator in this narrow region. Comparators are normally used to "detect" when an unknown voltage level exceeds a given reference voltage.

The most desirable comparator parameter is what minimum differential input voltage is required at the comparator's input terminals to guarantee a given output logic state. This new and important parameter has been called input sensitivity (V_{IS}) and is analagous to the input threshold voltage specification on a core memory sense amplifier. The input sensitivity specification includes the effects of voltage gain, input offset voltage and input offset current and eliminates the need for specifying these three parameters.

In order to make this parameter as inclusive as possible on the MC3430-33 series quad comparators, the input sensitivity is specified within the following conditions:

Commercial Temperature Range – 0 to 70°C
Power Supply Variations – ±5% (all conditions)
Input Source Resistance – ≤200 Ohms
Common-Mode Voltage Range – -3.0 V to +3.0 V

Note: Typical values have been included on the omitted parameters for applications where the offset voltages are externally nulled.

Voltage gain is defined as the ratio of the resulting ΔV_O to a change in the V_{IDR} using conditions at which the V_{IO} and I_{IO} are nulled. Thus, for worst case MTTL logic levels, the required output voltage change is 2.0 V (V_{OH}min – V_{OL}max = 2.4 V – 0.4 V). If 2.0 mV are required at the input terminals to induce this change in logic state, the voltage gain would be 1000 V/V.

Gain however is not the only factor affecting the logic transition. Normally input offset voltages, that are not externally nulled, can add an appreciable error that drastically overshadows the comparator gain. Therefore, the 2.0 mV for example, required to cause the logic transition is often masked. An input offset voltage of up to 7.5 mV might be required to reach the linear region. A further consideration is the input offset current of up to ±10 μA flowing through the matched 200-Ohm source resistors at the input terminals which can create an additional error of ±2.0 mV. In order to determine a worst case input sensitivity, it must be assumed that minimum specified gain and maximum specified offset voltage and current conditions exist. Also it must be assumed that these three factors are cumulative, requiring a worst case input of:

Logic Transition = 2.0 mV
V_{IO} = 7.5 mV
I_{IO} of ±10 μA thru 200-Ohm resistor = 2.0 mV

Therefore, 2 + 7.5 + 2 = 11.5 mV.

The effects of power supply voltage variations, temperature changes and common-mode input voltage conditions have not been considered, as they are not present in the gain and offset specifications on most comparators.

Thus, the input sensitivity specification greatly reduces the effort required in determining the worst case differential voltage required by a given comparator type.

Table I compares the worst case input sensitivity of three popular comparator types at both room temperature and over the specified commercial temperature range (0 to 70°C). This sensitivity was computed from the specified voltage gain, offset voltage and offset current limits.

TABLE I – WORST CASE COMPARISONS

	T_A = 25°C						T_A = 0 to 70°C					
Type Number	V_{IO} mV Max	A_{vol}* V/V Typ	Differential Input Voltage Required for 3.0 V Output Change	I_{IO} R_S = 200 Ω μA Max	Error Voltage Generated Into 200 Ω Source Resistors	Total Sensitivity mV	V_{IO} mV Max	A_{vol}* V/V Typ	Differential Input Voltage Required for 3.0 V Output Change	I_{IO} R_S = 200 Ω μA Max	Error Voltage Generated Into 200 Ω Source Resistors	Total Sensitivity mV
MC3430, MC3432	–	–	–	–	–	6.0	–	–	–	–	–	7.0
MC3431, MC3433	–	–	–	–	–	10	–	–	–	–	–	12
MC1711C	5.0	1500	2.0 mV	15	3.0 mV	10	5.0	1000	3.0 mV	25	5.0 mV	13
LM311	7.5	200 k	0.015 mV	6.0**	0.0012 mV	7.516	10	100 k	0.030 mV	70**	0.014 mV	10.04

*Typical values given, as minimum gain not always specified.
**I_{IO} measured in nA

FIGURE 2 – GUARANTEED OUTPUT STATE versus DIFFERENTIAL INPUT VOLTAGE

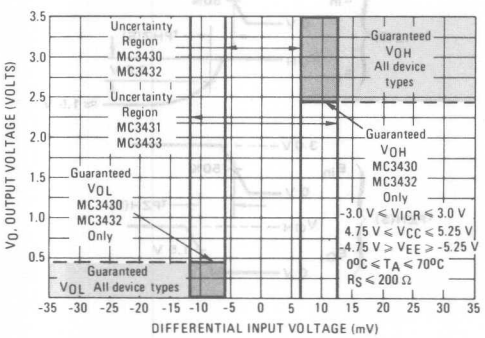
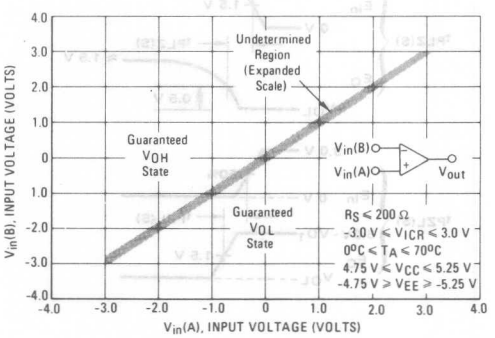


FIGURE 3 – GUARANTEED OUTPUT STATE versus INPUT VOLTAGE

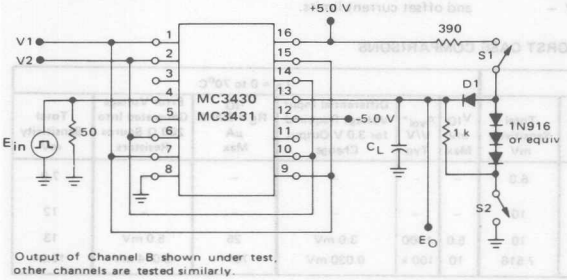


SWITCHING CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = -5.0 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	Fig.	MC3430, MC3431 Min	MC3430, MC3431 Typ	MC3430, MC3431 Max	MC3432, MC3433 Min	MC3432, MC3433 Typ	MC3432, MC3433 Max	Unit
High to Low Logic Level Propagation Delay Time (Differential Inputs) 5.0 mV + V_{IS}	$t_{PHL(D)}$	6,8-11	–	20	45	–	27	50	ns
Low to High Logic Level Propagation Delay Time (Differential Inputs) 5.0 mV + V_{IS}	$t_{PLH(D)}$	6,8-11	–	33	55	–	40	65	ns
Open State to High Logic Level Propagation Delay Time (Strobe)	$t_{PZH(S)}$	4	–	–	35	–	–	–	ns
High Logic Level to Open State Propagation Delay Time (Strobe)	$t_{PHZ(S)}$	4	–	–	35	–	–	–	ns
Open State to Low Logic Level Propagation Delay Time (Strobe)	$t_{PZL(S)}$	4	–	–	40	–	–	–	ns
Low Logic Level to Open State Propagation Delay Time (Strobe)	$t_{PLZ(S)}$	4	–	–	35	–	–	–	ns
High Logic to Low Logic Level Propagation Delay Time (Strobe)	$t_{PHL(S)}$	5	–	–	–	–	–	40	ns
Low Logic to High Logic Level Propagation Delay Time (Strobe)	$t_{PLH(S)}$	5	–	–	–	–	–	35	ns

TEST CIRCUITS

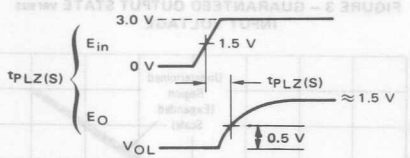
FIGURE 4 – STROBE PROPAGATION DELAY TIMES $t_{PLZ(S)}$, $t_{PZL(S)}$, $t_{PHZ(S)}$, and $t_{PZH(S)}$

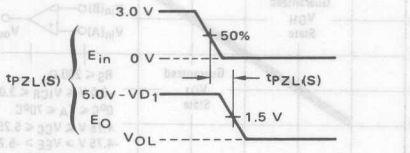


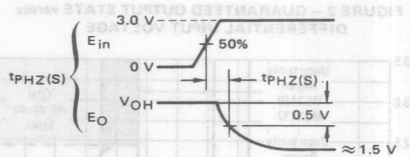
Output of Channel B shown under test, other channels are tested similarly.

	V1	V2	S1	S2	C_L
$t_{PLZ(S)}$	100 mV	GND	Closed	Closed	15 pF
$t_{PZL(S)}$	100 mV	GND	Closed	Open	50 pF
$t_{PHZ(S)}$	GND	100 mV	Closed	Closed	15 pF
$t_{PZH(S)}$	GND	100 mV	Open	Closed	50 pF

C_L includes jig and probe capacitance.
E_{in} waveform characteristics:
t_{TLH} and t_{THL} ≤ 10 ns measured 10% to 90%.
PRR = 1.0 MHz
Duty Cycle = 50%







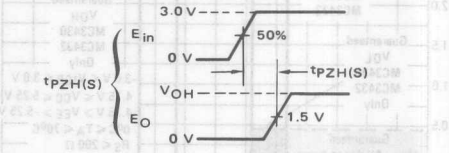
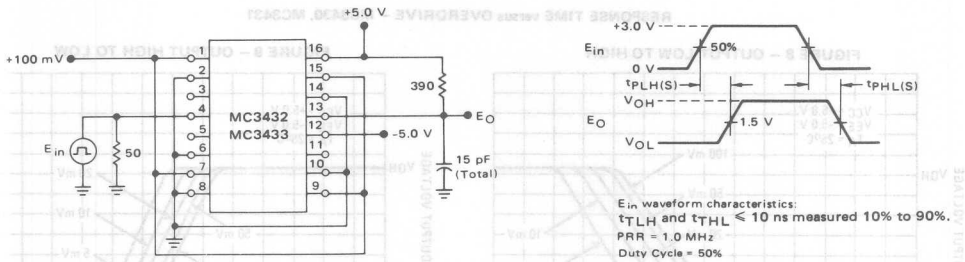


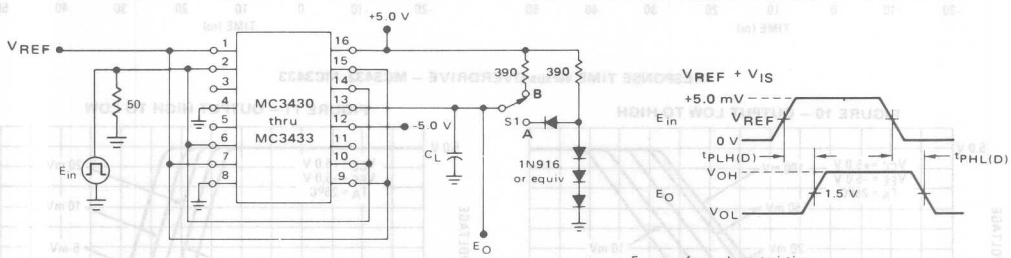
FIGURE 5 – STROBE PROPAGATION DELAY $t_{PLH(S)}$ AND $t_{PHL(S)}$



Output of Channel B shown under test, other channels are tested similarly.

E_{in} waveform characteristics:
t_{TLH} and $t_{THL} \leq 10$ ns measured 10% to 90%.
PRR = 1.0 MHz
Duty Cycle = 50%

FIGURE 6 – DIFFERENTIAL INPUT PROPAGATION DELAY $t_{PLH(D)}$ AND $t_{PHL(D)}$



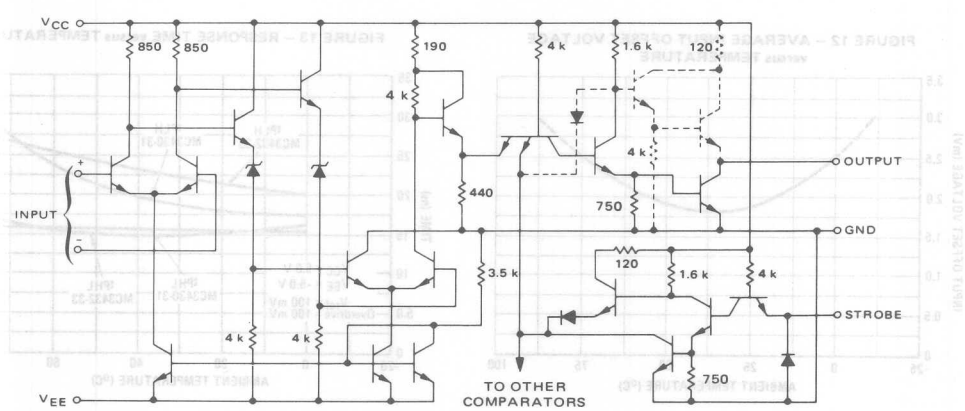
Output of Channel B shown under test, other channels are tested similarly.

S1 at "A" for MC3430, MC3431
S1 at "B" for MC3432, MC3433
C_L = 50 pF total for MC3430, MC3431
C_L = 15 pF total for MC3432, MC3433

Device	V_{REF} mV
MC3430	11
MC3431	15
MC3432	11
MC3433	15

E_{in} waveform characteristics:
t_{TLH} and $t_{THL} \leq 10$ ns measured 10% to 90%.
PRR = 1.0 MHz
Duty Cycle = 50%

FIGURE 7 – CIRCUIT SCHEMATIC
(1/4 Circuit Shown)



Dashed components apply to the MC3430 and MC3431 circuits only.

2

TYPICAL PERFORMANCE CURVES

RESPONSE TIME versus OVERDRIVE – MC3430, MC3431

FIGURE 8 – OUTPUT LOW TO HIGH

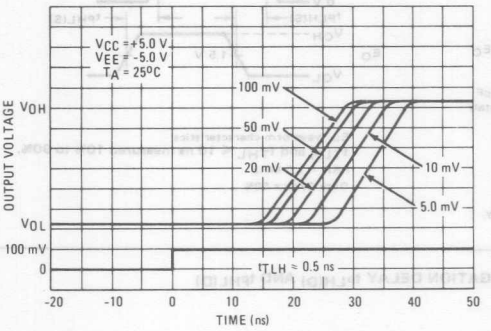
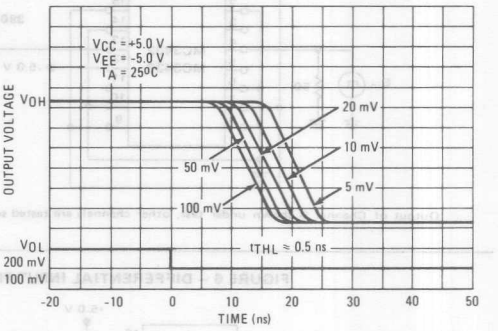


FIGURE 9 – OUTPUT HIGH TO LOW



RESPONSE TIME versus OVERDRIVE – MC3432, MC3433

FIGURE 10 – OUTPUT LOW TO HIGH

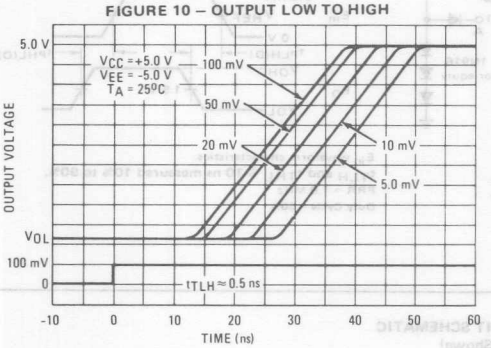


FIGURE 11 – OUTPUT HIGH TO LOW

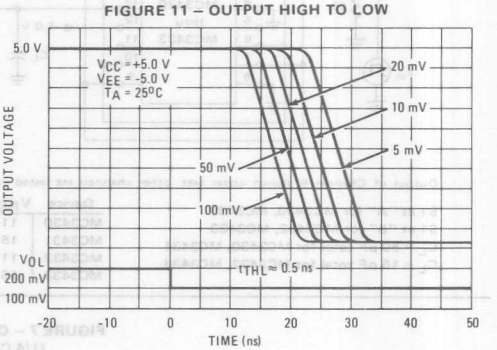


FIGURE 12 – AVERAGE INPUT OFFSET VOLTAGE versus TEMPERATURE

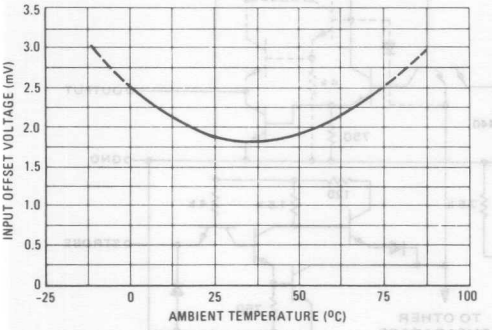
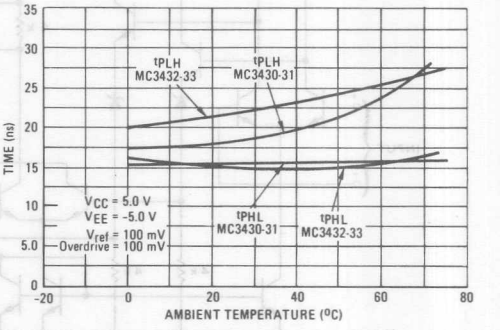


FIGURE 13 – RESPONSE TIME versus TEMPERATURE



APPLICATIONS INFORMATION

FIGURE 14 – 4-BIT PARALLEL A/D CONVERTER

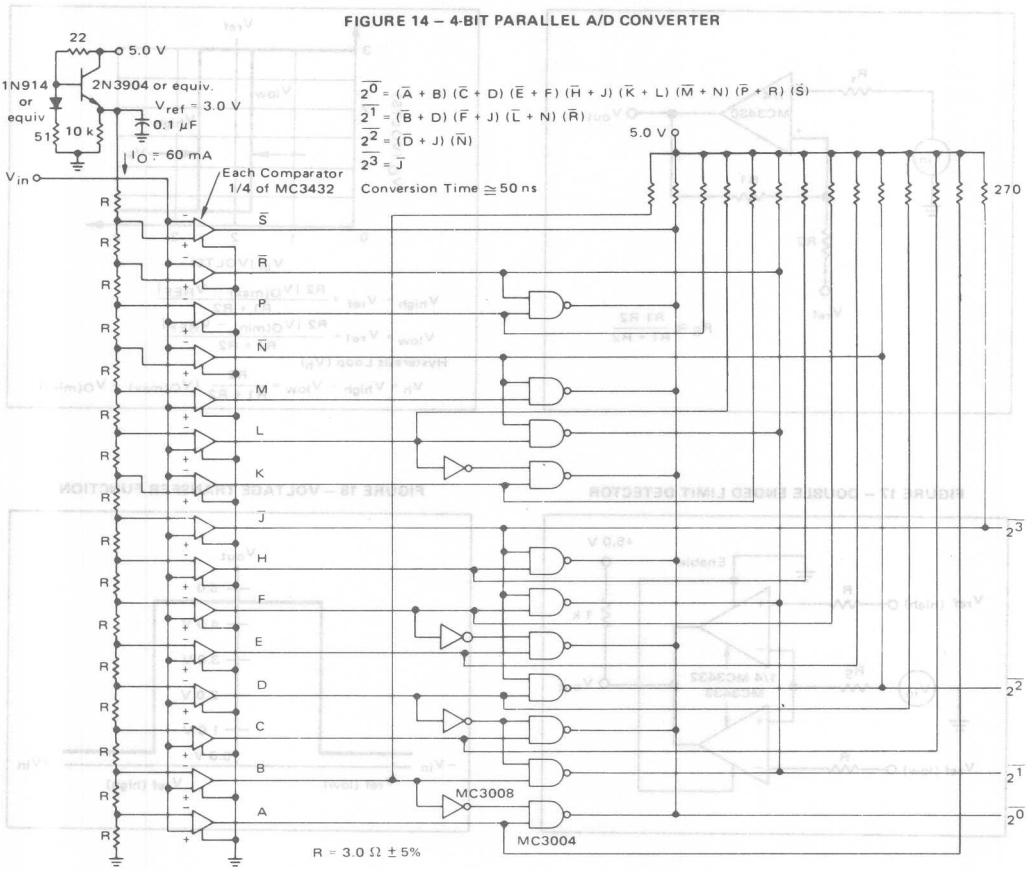


FIGURE 15 – LEVEL DETECTOR WITH HYSTERESIS

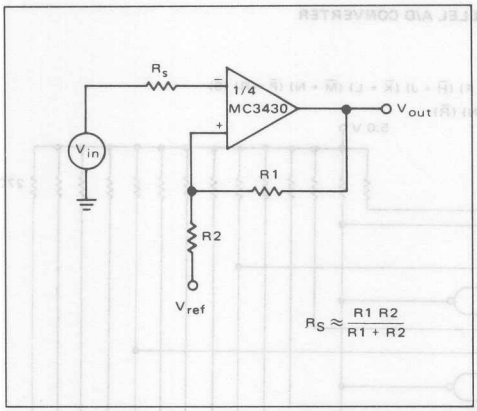


FIGURE 16 – TRANSFER CHARACTERISTICS AND EQUATIONS FOR FIGURE 15

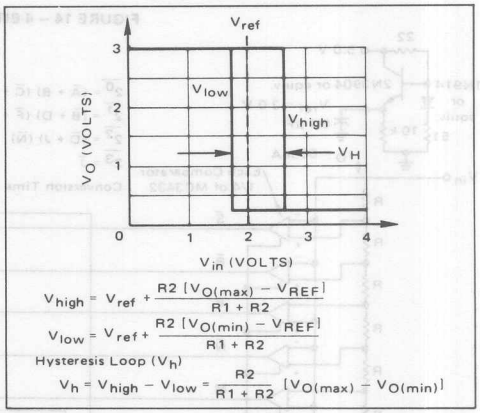


FIGURE 17 – DOUBLE ENDED LIMIT DETECTOR

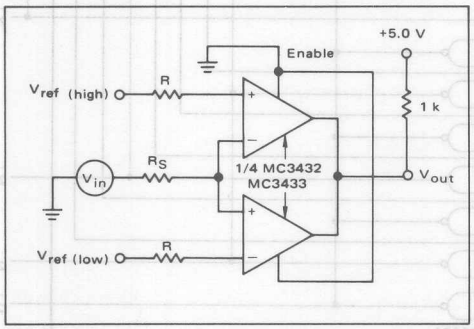
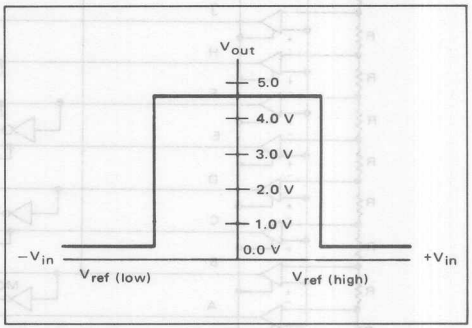


FIGURE 18 – VOLTAGE TRANSFER FUNCTION



ORDERING INFORMATION

Device	Temperature Range	Package
MC3358P1	−40°C to +85°C	Plastic DIP
MC3458D	0°C to +70°C	SO-8
MC3458G	0°C to +70°C	Metal Can
MC3458P1	0°C to +70°C	Plastic DIP
MC3458U	0°C to +70°C	Ceramic DIP
MC3558G	−55°C to +125°C	Metal Can
MC3558U	−55°C to +125°C	Ceramic DIP

MC3458
MC3558
MC3358

Specifications and Applications Information

DUAL DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUIT

DUAL LOW POWER OPERATIONAL AMPLIFIERS

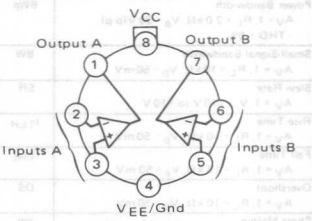
Utilizing the circuit designs perfected for recently introduced Quad Operational Amplifiers, these dual operational amplifiers feature 1) low power drain, 2) a common mode input voltage range extending to ground/V_{EE}, 3) Single Supply or Split Supply operation and 4) pin outs compatible with the popular MC1558 dual operational amplifier. The MC3558 Series is equivalent to one-half of a MC3503.

These amplifiers have several distinct advantages over standard operational amplifier types in single supply applications. They can operate at supply voltages as low as 3.0 Volts or as high as 36 Volts with quiescent currents about one-fifth of those associated with the MC1741 (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

- Short Circuit Protected Outputs
- True Differential Input Stage
- Single Supply Operation: 3.0 to 36 Volts
- Low Input Bias Currents
- Internally Compensated
- Common Mode Range Extends to Negative Supply
- Class AB Output Stage for Minimum Crossover Distortion
- Single and Split Supply Operations Available
- Similar Performance to the Popular MC1558

G SUFFIX
METAL PACKAGE
CASE 601-04



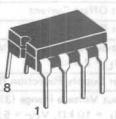


(Top View)

P1 SUFFIX
PLASTIC PACKAGE
CASE 626-05
(MC3458, MC3358 Only)

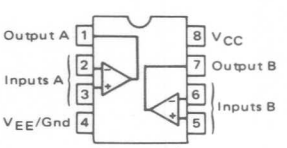


U SUFFIX
CERAMIC PACKAGE
CASE 693-02



D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SO-8





(Top View)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltages			Vdc
Single Supply	V_{CC}	36	
Split Supplies	V_{CC}	+18	
	V_{EE}	−18	
Input Differential Voltage Range (1)	V_{IDR}	±30	Vdc
Input Common Mode Voltage Range (2)	V_{ICR}	±15	Vdc
Input Forward Current (V_I < −0.3 V)	I_{IF}	50	mA
Junction Temperature	T_J		°C
Ceramic and Metal Packages		175	
Plastic Package		150	
Storage Temperature Range	T_{stg}		°C
Ceramic and Metal Packages		-65 to +150	
Plastic Package		-55 to +125	
Operating Ambient Temperature Range	T_A		°C
MC3558		−55 to +125	
MC3458		0 to +70	
MC3358		−40 to +85	

(1) Split Power Supplies.
(2) For Supply Voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

2

ELECTRICAL CHARACTERISTICS (For MC3558, MC3458, V_{CC} = +15 V, V_{EE} = -15 V, T_A = 25°C unless otherwise noted.) (For MC3358, V_{CC} = +14 V, V_{EE} = Gnd, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	MC3558			MC3458			MC3358			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage $T_A = T_{high}$ to T_{low} (1)	V_{IO}	– –	2.0 –	5.0 6.0	– –	2.0 –	10 12	– –	2.0 –	8.0 10	mV
Input Offset Current $T_A = T_{high}$ to T_{low}	I_{IO}	– –	30 –	50 200	– –	30 –	50 200	– –	30 –	75 250	nA
Large Signal Open-Loop Voltage Gain V_O = ±10 V, R_L = 2.0 kΩ, $T_A = T_{high}$ to T_{low}	A_{VOL}	50 25	200 300	–	20 15	200 –	–	20 15	200 –	–	V/mV
Input Bias Current $T_A = T_{high}$ to T_{low}	I_{IB}	– –	-200 -300	-500 -1500	– –	-200 –	-500 -800	– –	-200 –	-500 -1000	nA
Output Impedance f = 20 Hz	z_o	–	75	–	–	75	–	–	75	–	Ω
Input Impedance f = 20 Hz	z_i	0.3	1.0		0.3	1.0		0.3	1.0		MΩ
Output Voltage Range R_L = 10 kΩ R_L = 2.0 kΩ R_L = 2.0 kΩ, $T_A = T_{high}$ to T_{low}	V_{OR}	±12 ±10 ±10	±13.5 ±13		±12 ±10 ±10	±13.5 ±13 –		12 10 10	12.5 12 –		V
Input Common-Mode Voltage Range	V_{ICR}	+13 V -V_{EE}	+13.5 V-V_{EE}		+13 V -V_{EE}	+13.5V-V_{EE}		+12 V -V_{EE}	+12.5V-V_{EE}		V
Common-Mode Rejection Ratio $R_S \leq 10$ kΩ	CMRR	70	90		70	90		70	90		dB
Power Supply Current (V_O = 0) R_L = ∞	I_{CC},I_{EE}	–	1.6	2.2		1.6	3.7		1.6	3.7	mA
Individual Output Short-Circuit Current (2)	I_{OS}	±10	±30	±45	±10	±20	±45	±10	±30	±45	mA
Positive Power Supply Rejection Ratio	PSRR+	–	30	150	–	30	150	–	30	150	μV/V
Negative Power Supply Rejection Ratio	PSRR-	–	30	150	–	30	150	–	–	–	μV/V
Average Temperature Coefficient of Input Offset Current $T_A = T_{high}$ to T_{low}	$\Delta I_{IO}/\Delta T$	–	50		–	50	–	–	50	–	pA/°C
Average Temperature Coefficient of Input Offset Voltage $T_A = T_{high}$ to T_{low}	$\Delta V_{IO}/\Delta T$	–	10		–	10	–	–	10	–	μV/°C
Power Bandwidth A_V = 1, R_L = 2.0 kΩ, V_O = 20 Vp-p, THD = 5%	BWp	–	9.0		–	9.0	–	–	9.0	–	kHz
Small-Signal Bandwidth A_V = 1, R_L = 10 kΩ, V_O = 50 mV	BW	–	1.0		–	1.0	–	–	1.0	–	MHz
Slew Rate A_V = 1, V_i = -10 V to +10 V	SR	–	0.6		–	0.6	–	–	0.6	–	V/μs
Rise Time A_V = 1, R_L = 10 kΩ, V_O = 50 mV	t_{TLH}	–	0.35		–	0.35	–	–	0.35	–	μs
Fall Time A_V = 1, R_L = 10 kΩ, V_O = 50 mV	t_{THL}	–	0.35		–	0.35	–	–	0.35	–	μs
Overshoot A_V = 1, R_L = 10 kΩ, V_O = 50 mV	OS	–	20	–	–	20	–	–	20	–	%
Phase Margin A_V = 1, R_L = 2.0 kΩ, C_L = 200 pF	ϕ_m	–	60	–	–	60	–	–	60	–	Degrees
Crossover Distortion (V_{in} = 30 mVp-p, V_{out} = 2.0 Vp-p, f = 10 kHz)	–	–	1.0	–	–	1.0	–	–	1.0	–	%

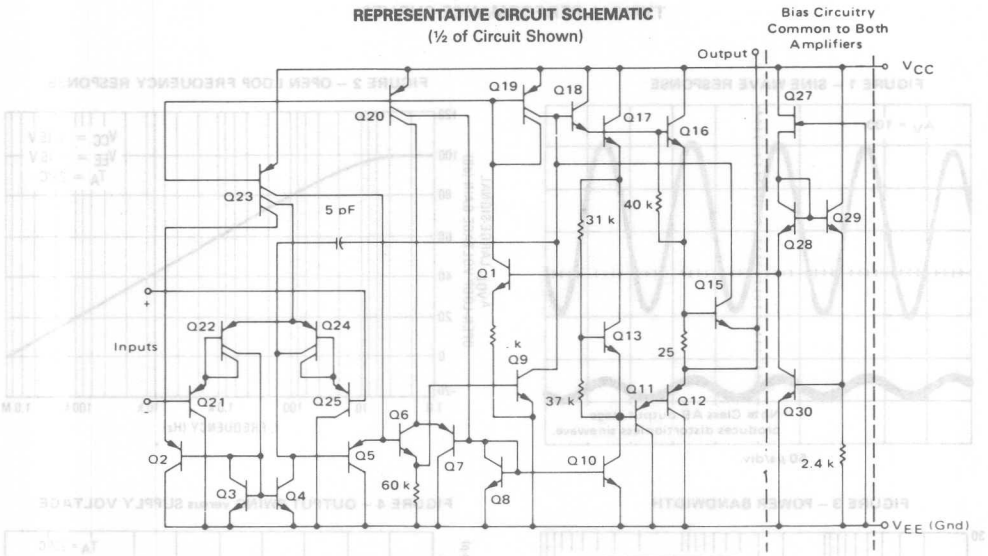
(1) T_{high} = 125°C for MC3558, 70°C for MC3458, 85°C for MC3358.
T_{low} = -55°C for MC3558, 0°C for MC3458, -40°C for MC3358.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C unless otherwise noted.)

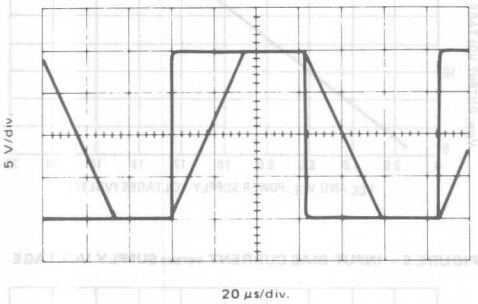
Characteristic	Symbol	MC3558			MC3458			MC3358			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	–	2.0	5.0	–	2.0	10	–	2.0	10	mV
Input Offset Current	I_{IO}	–	30	50	–	30	50	–	–	75	nA
Input Bias Current	I_{IB}	–	-200	-500	–	-200	-500	–	–	-500	nA
Large-Signal Open-Loop Voltage Gain R_L = 2.0 kΩ	A_{VOL}	20	200	–	20	200	–	20	200	–	V/mV
Power Supply Rejection Ratio	PSRR	–	–	150	–	–	150	–	–	150	μV/V
Output Voltage Range (3) R_L = 10 kΩ, V_{CC} = 5.0 V R_L = 10 kΩ, 5.0 V ≤ V_{CC} ≤ 30 V	V_{OR}	3.3 –	3.5 V_{CC}-1.7 V	– –	3.3 –	3.5 V_{CC} -1.7 V	– –	3.3 –	3.5 V_{CC} -1.7 V	– –	Vp-p
Power Supply Current	I_{CC}	–	2.5	4.0	–	2.5	7.0	–	2.5	4.0	mA
Channel Separation f = 1.0 kHz to 20 kHz (Input Referenced)	–	–	-120	–	–	-120	–	–	-120	–	dB

(2) Not to exceed maximum package power dissipation.
(3) Output will swing to ground

REPRESENTATIVE CIRCUIT SCHEMATIC
(½ of Circuit Shown)



INVERTER PULSE RESPONSE



CIRCUIT DESCRIPTION

The MC3558 Series is made using two internally compensated, two-stage operational amplifiers. The first stage of each consists of differential input devices Q24 and Q22 with input buffer transistors Q25 and Q21 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance a smaller compensation capacitor (only 5 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q24 and Q22. Another feature of this input stage is that the input common-mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single-ended converter. The second stage consists of a standard current source load amplifier stage.

The output stage is unique because it allows the output to swing to ground in single supply operation and yet does not exhibit any crossover distortion in split supply operation. This is possible because class AB operation is utilized.

Each amplifier is biased from an internal-voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

FIGURE 1 – SINE WAVE RESPONSE

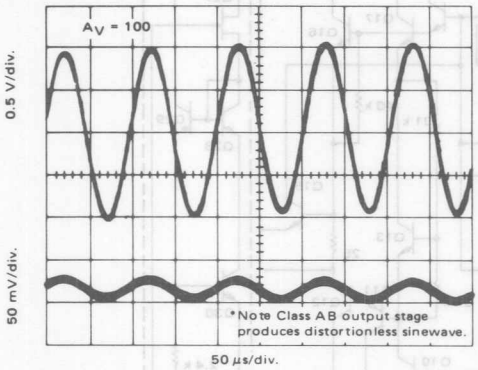


FIGURE 2 – OPEN LOOP FREQUENCY RESPONSE

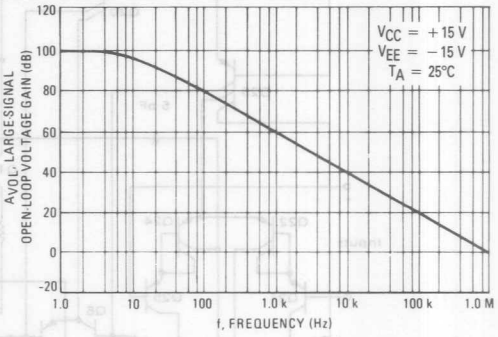


FIGURE 3 – POWER BANDWIDTH

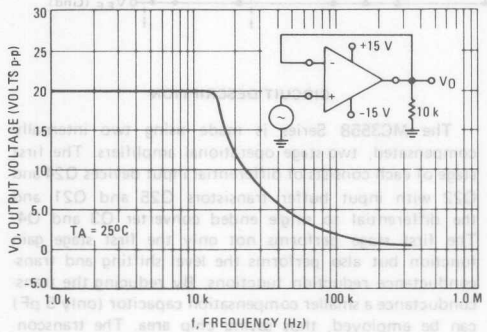


FIGURE 4 – OUTPUT SWING versus SUPPLY VOLTAGE

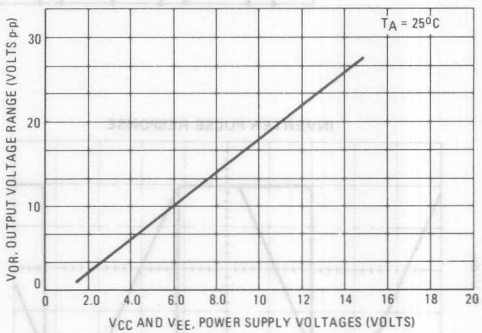


FIGURE 5 – INPUT BIAS CURRENT versus TEMPERATURE

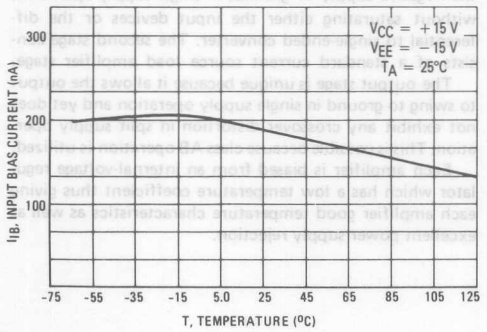
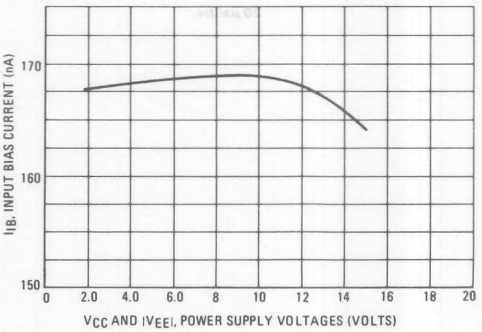


FIGURE 6 – INPUT BIAS CURRENT versus SUPPLY VOLTAGE



APPLICATIONS INFORMATION

FIGURE 7 – VOLTAGE REFERENCE

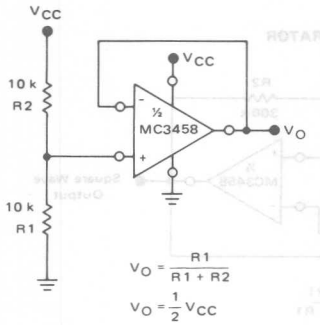


FIGURE 8 – WIEN BRIDGE OSCILLATOR

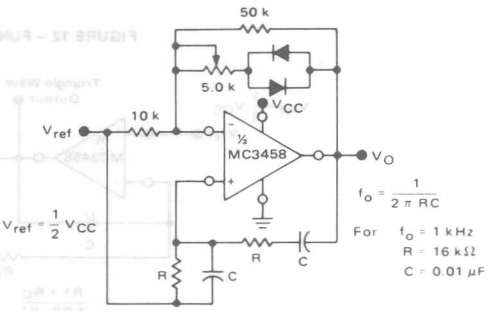


FIGURE 9 – HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER

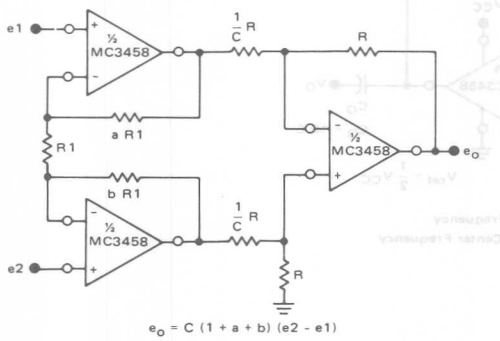


FIGURE 10 – COMPARATOR WITH HYSTERESIS

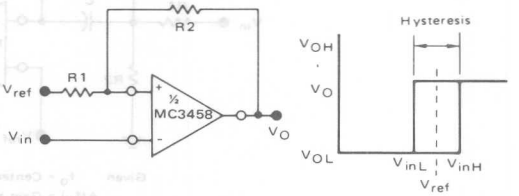
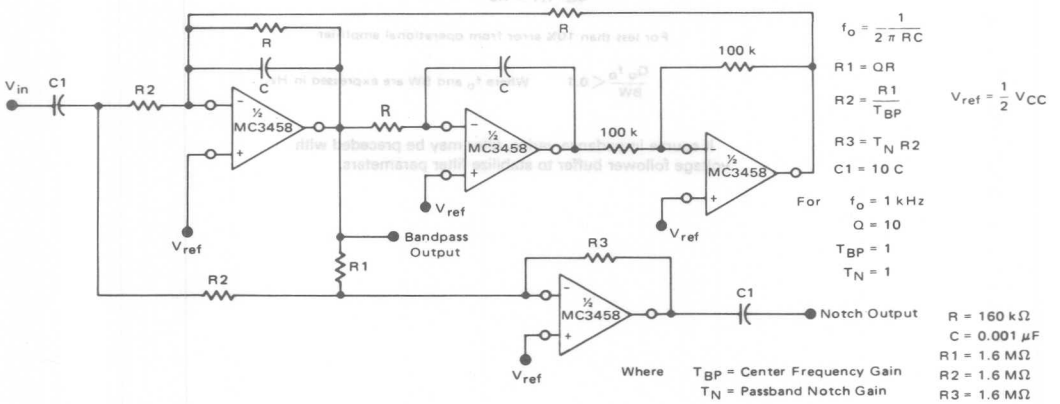


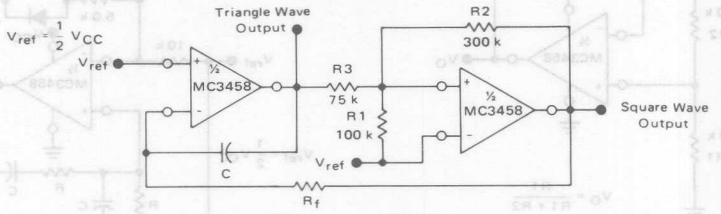
FIGURE 11 – BI-QUAD FILTER



2

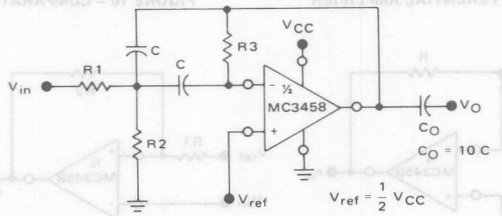
APPLICATIONS INFORMATION (continued)

FIGURE 12 – FUNCTION GENERATOR



$$f = \frac{R1 + R_C}{4 C R_f R1} \quad \text{if} \quad R3 = \frac{R2\ R1}{R2 + R1}$$

FIGURE 13 – MULTIPLE FEEDBACK BANDPASS FILTER



Given f_o = Center Frequency
$A(f_o)$ = Gain at Center Frequency

Choose Value f_o, C
Then:

$$R3 = \frac{Q}{\pi f_o C}$$

$$R1 = \frac{R3}{2 A(f_o)}$$

$$R2 = \frac{R1\ R3}{4Q^2 R1 - R3}$$

For less than 10% error from operational amplifier

$$\frac{Q_o f_o}{BW} < 0.1$$ Where f_o and BW are expressed in Hz.

If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

MC3476

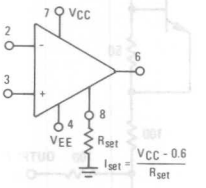
LOW COST PROGRAMMABLE OPERATIONAL AMPLIFIER

The MC3476 is a low cost selection of the popular, industry-standard MC1776 programmable operational amplifier. This extremely versatile operational amplifier features low power consumption and high input impedance. In addition, the quiescent currents within the device may be programmed by the choice of an external resistor value or current source applied to the I_{set} input. This allows the amplifier's characteristics to be optimized for input current and power consumption despite wide variations in operating power supply voltages.

- ±6.0 V to ±18 V Operation
- Wide Programming Range
- Offset Null Capability
- No Frequency Compensation Required
- Low Input Bias Currents
- Short-Circuit Protection

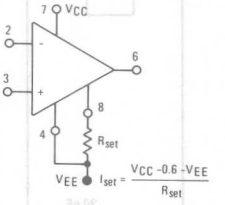
RESISTIVE PROGRAMMING (See Figure 1.)

R_{set} to GROUND



Typical R_{set} Values		
V_{CC}, V_{EE}	I_{set} = 10 μA	I_{set} = 15 μA
±6.0 V	560 kΩ	360 kΩ
±9.0 V	820 kΩ	560 kΩ
±12 V	1.0 MΩ	750 kΩ
±15 V	1.5 MΩ	1.0 MΩ

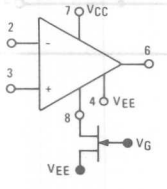
R_{set} to NEGATIVE SUPPLY



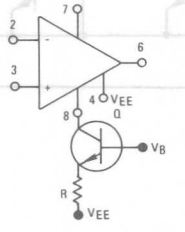
Typical R_{set} Values		
V_{CC}, V_{EE}	I_{set} = 10 μA	I_{set} = 15 μA
±6.0 V	1.0 MΩ	820 kΩ
±9.0 V	1.8 MΩ	1.2 MΩ
±12 V	2.2 MΩ	1.5 MΩ
±15 V	2.7 MΩ	2.0 MΩ

ACTIVE PROGRAMMING

FET CURRENT SOURCE



BIPOLAR CURRENT SOURCE



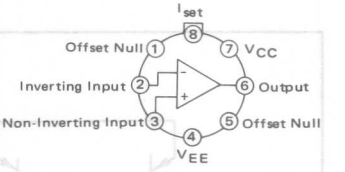
Pins not shown are not connected.

LOW COST PROGRAMMABLE OPERATIONAL AMPLIFIER

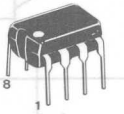
SILICON MONOLITHIC INTEGRATED CIRCUIT



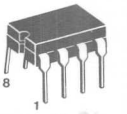
G SUFFIX
METAL PACKAGE
CASE 601-04



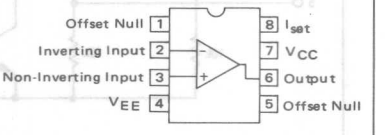
(Top View)



P1 SUFFIX
PLASTIC PACKAGE
CASE 626-05



U SUFFIX
CERAMIC PACKAGE
CASE 693-02



(Top View)

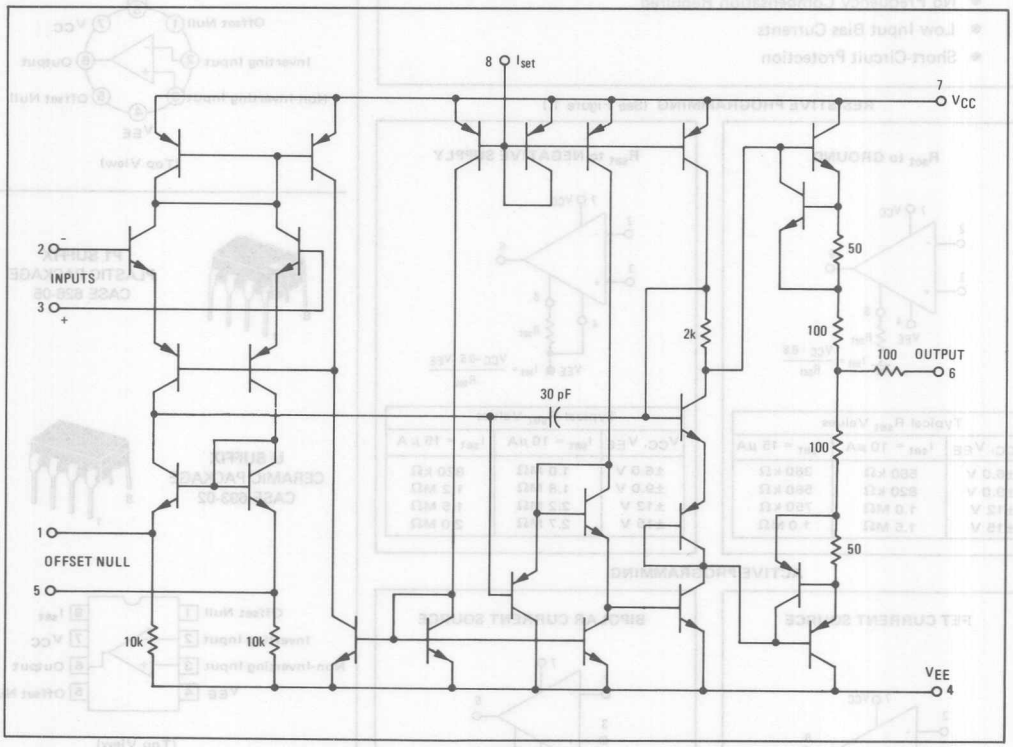
ORDERING INFORMATION

Device	Temperature Range	Package
MC3476G	0 to +70°C	Metal Can
MC3476P1	0 to +70°C	Plastic DIP
MC3476U	0 to +70°C	Ceramic DIP

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC}, V_{EE}	±18	Vdc
Input Differential Voltage Range	V_{IDR}	±30	Vdc
Input Common-Mode Voltage Range	V_{ICR}	V_{CC}, V_{EE}	Vdc
Offset Null to V_{EE} Voltage	$V_{off}-V_{EE}$	±0.5	Vdc
Programming Current	I_{set}	200	μA
Programming Voltage (Voltage from I_{set} terminal to ground)	V_{set}	(V_{CC}−0.6 V) to V_{CC}	Vdc
Output Short-Circuit Duration*	t_S	Indefinite	s
Operating Ambient Temperature Range	T_A	0 to 70	°C
Storage Temperature Range Metal and Ceramic Packages Plastic Package	T_{stg}	 −65 to +150 −55 to +125	°C
Junction Temperature Metal and Ceramic Packages Plastic Package	T_J	 175 150	°C

*Short-Circuit to ground with $I_{set} \leq 15$ μA. Rating applies up to ambient temperature of +70°C.

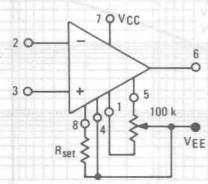
EQUIVALENT SCHEMATIC DIAGRAM



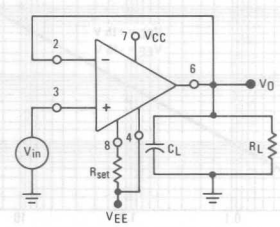
ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, I_{set} = 15 μA, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S \leq 10$ kΩ)	V_{IO}				mV
T_A = +25°C		–	2.0	6.0	
0°C ≤ T_A ≤ 70°C		–	–	7.5	
Offset Voltage Adjustment Range	V_{IOR}	–	18	–	mV
Input Offset Current	I_{IO}				nA
T_A = +25°C		–	2.0	25	
T_A = 70°C		–	–	25	
T_A = 0°C		–	–	40	
Input Bias Current	I_{IB}				nA
T_A = +25°C		–	15	50	
T_A = 70°C		–	–	50	
T_A = 0°C		–	–	100	
Input Resistance	r_i	–	5.0	–	MΩ
Input Capacitance	C_i	–	2.0	–	pF
Input Common-Mode Voltage Range 0°C ≤ T_A ≤ 70°C	V_{ICR}	±10	–	–	V
Large Signal Voltage Gain	A_{VOL}				V/V
$R_L \geq 10$ kΩ, V_O = ±10 V, T_A = +25°C		50 k	400 k	–	
$R_L \geq 10$ kΩ, V_O = ±10 V, 0°C ≤ T_A ≤ 70°C		25 k	–	–	
Output Voltage Range	V_{OR}				V
$R_L \geq 10$ kΩ, T_A = +25°C		±12	±13	–	
$R_L \geq 10$ kΩ, 0°C ≤ T_A ≤ 70°C		±12	–	–	
Output Resistance	r_o	–	1.0	–	kΩ
Output Short-Circuit Current	I_{os}	–	12	–	mA
Common-Mode Rejection Ratio $R_S \leq 10$ kΩ, 0°C ≤ T_A ≤ 70°C	CMRR	70	90	–	dB
Supply Voltage Rejection Ratio $R_S \leq 10$ kΩ, 0°C ≤ T_A ≤ 70°C	PSRR	–	25	200	μV/V
Supply Current	I_{CC}, I_{EE}				μA
T_A = +25°C		–	160	200	
0°C ≤ T_A ≤ 70°C		–	–	225	
Power Dissipation	P_D				mW
T_A = +25°C		–	4.8	6.0	
0°C ≤ T_A ≤ 70°C		–	–	6.75	
Transient Response (Unity Gain) V_{in} = 20 mV, $R_L \geq 10$ kΩ, C_L = 100 pF					
Rise Time	t_{TLH}	–	0.35	–	μs
Overshoot	OS	–	10	–	%
Slew Rate ($R_L \geq 10$ kΩ)	SR	–	0.8	–	V/μs

VOLTAGE OFFSET NULL CIRCUIT



TRANSIENT-RESPONSE TEST CIRCUIT



Pins not shown are not connected.

2

TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted.)

FIGURE 1 – SET CURRENT versus SET RESISTOR

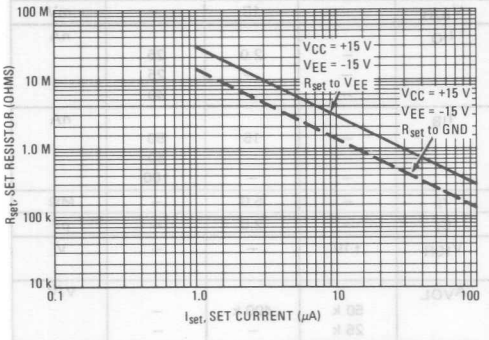


FIGURE 2 – POSITIVE STANDBY SUPPLY CURRENT versus SET CURRENT

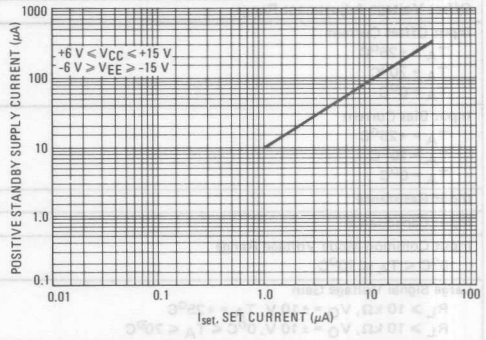


FIGURE 3 – OPEN-LOOP GAIN versus SET CURRENT

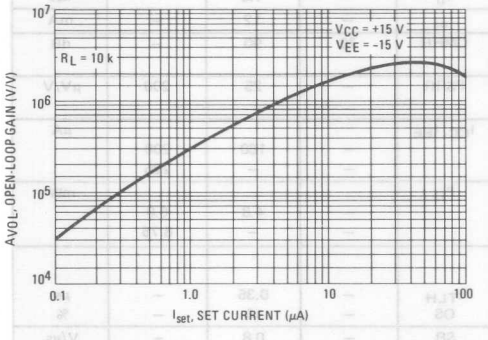


FIGURE 4 – INPUT BIAS CURRENT versus SET CURRENT

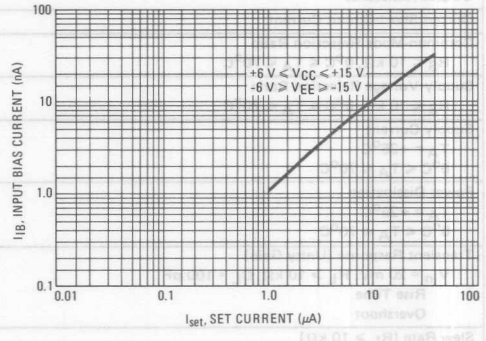


FIGURE 5 – SLEW RATE versus SET CURRENT

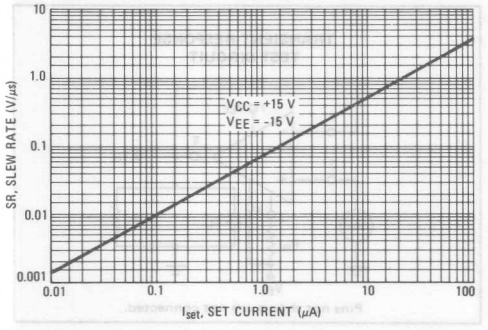
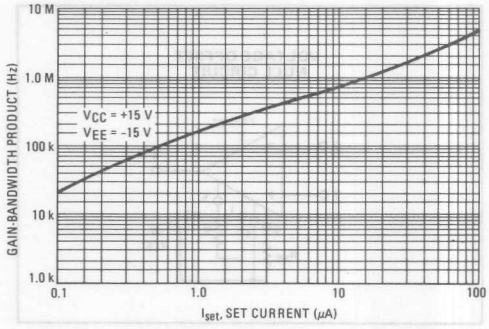


FIGURE 6 – GAIN-BANDWIDTH PRODUCT (GBW) versus SET CURRENT



2

TYPICAL CHARACTERISTICS (continued)

(T_A = +25°C unless otherwise noted.)

FIGURE 7 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

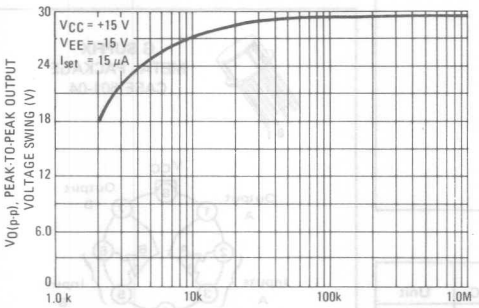
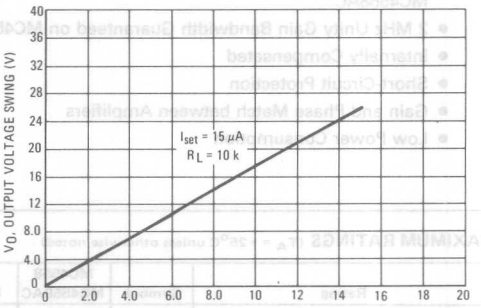


FIGURE 8 – OUTPUT SWING versus SUPPLY VOLTAGE



DUAL WIDEBAND OPERATIONAL AMPLIFIER

The MC4558, MC4558AC, and MC4558C combine all the outstanding features of the MC1458 and, in addition, possess three times the unity gain bandwidth of the industry standard.

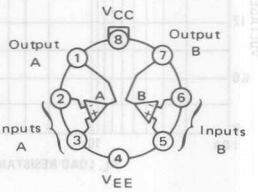
- 2.5 MHz Unity Gain Bandwidth Guaranteed on MC4558 and MC4558AC
- 2 MHz Unity Gain Bandwidth Guaranteed on MC4558C
- Internally Compensated
- Short-Circuit Protection
- Gain and Phase Match between Amplifiers
- Low Power Consumption

DUAL WIDE BANDWIDTH OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT



G SUFFIX
METAL PACKAGE
CASE 601-04



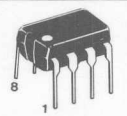
(Top View)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

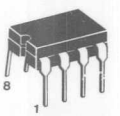
Rating	Symbol	MC4558 MC4558AC	MC4558C	Unit
Power Supply Voltage	V_{CC}	+22	+18	Vdc
	V_{EE}	-22	-18	Vdc
Input Differential Voltage	V_{ID}	±30		Volts
Input Common Mode Voltage (Note 1)	V_{ICM}	±15		Volts
Output Short-Circuit Duration (Note 2)	t_S	Continuous		
Operating Ambient Temperature Range	T_A	See Ordering Information Below		
Storage Temperature Range Metal and Ceramic Packages Plastic Package	T_{stg}	 -65 to +150 -55 to +125		°C
Junction Temperature Metal and Ceramic Packages Plastic Package	T_J	 175 150		°C

Note 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

Note 2. Short circuit may be to ground or either supply.



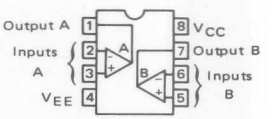
P1 SUFFIX
PLASTIC PACKAGE
CASE 626-05



U SUFFIX
CERAMIC PACKAGE
CASE 693-02

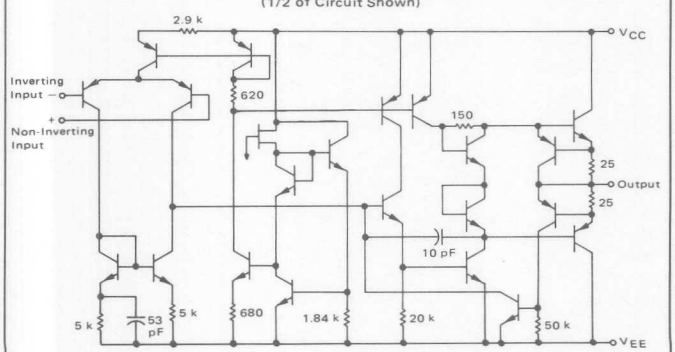


D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SO-8



(Top View)

EQUIVALENT CIRCUIT SCHEMATIC
(1/2 of Circuit Shown)



ORDERING INFORMATION

Device	Temperature Range	Package
MC4558G	-55 to +125°C	Metal Can
MC4558U		Ceramic DIP
MC4558CD	0 to +70°C	SO-8
MC4558CG		Metal Can
MC4558ACP1, CP1		Plastic DIP
MC4558CU		Ceramic DIP

FREQUENCY CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C)

Characteristic	Symbol	MC4558, MC4558AC			MC4558C			Unit
		Min	Typ	Max	Min	Typ	Max	
Unity Gain Bandwidth	BW	2.5	2.8	–	2.0	2.8	–	MHz

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, V_{EE} = −15 V, T_A = 25°C unless otherwise noted.)

Input Offset Voltage ($R_S \leq 10$ kΩ)	V_{IO}	–	1.0	5.0	–	2.0	6.0	mV
Input Offset Current	I_{IO}	–	20	200	–	20	200	nA
Input Bias Current†	I_{IB}	–	80	500	–	80	500	nA
Input Resistance	r_i	0.3	2.0	–	0.3	2.0	–	MΩ
Input Capacitance	C_i	–	1.4	–	–	1.4	–	pF
Common Mode Input Voltage Range	V_{ICR}	±12	±13	–	±12	±13	–	V
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 kΩ)	A_v	50	200	–	20	200	–	V/mV
Output Resistance	r_o	–	75	–	–	75	–	Ω
Common Mode Rejection Ratio ($R_S \leq 10$ kΩ)	CMRR	70	90	–	70	90	–	dB
Supply Voltage Rejection Ratio ($R_S \leq 10$ kΩ)	PSRR	–	30	150	–	30	150	μV/V
Output Voltage Swing ($R_L \geq 10$ kΩ)	V_O	±12	±14	–	±12	±14	–	V
($R_L \geq 2$ kΩ)		±10	±13	–	±10	±13	–	
Output Short-Circuit Current	I_{os}	10	20	40	10	20	40	mA
Supply Currents (Both Amplifiers)	I_D	–	2.3	5.0	–	2.3	5.6	mA
Power Consumption (Both Amplifiers)	P_C	–	70	150	–	70	170	mW
Transient Response (Unity Gain)								
(V_I = 20 mV, $R_L \geq 2$ kΩ, $C_L \leq 100$ pF) Rise Time	t_{TLH}	–	0.3	–	–	0.3	–	μs
(V_I = 20 mV, $R_L \geq 2$ kΩ, $C_L \leq 100$ pF) Overshoot	os	–	15	–	–	15	–	%
(V_I = 10 V, $R_L \geq 2$ kΩ, $C_L \leq 100$ pF) Slew Rate	SR	1.5	1.6	–	1.0	1.6	–	V/μs

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = *T_{high} to T_{low} unless otherwise noted).

Input Offset Voltage ($R_S \leq 10$ kΩ)	V_{IO}	–	1.0	6.0	–	–	7.5	mV
Input Offset Current	I_{IO}							nA
($T_A = T_{high}$)		–	7.0	200	–	–	–	
($T_A = T_{low}$)		–	85	500	–	–	–	
(T_A = 0°C to +70°C)		–	–	–	–	–	300	
Input Bias Current	I_{IB}							nA
($T_A = T_{high}$)		–	30	500	–	–	–	
($T_A = T_{low}$)		–	300	1500	–	–	–	
(T_A = 0°C to +70°C)		–	–	–	–	–	800	
Common Mode Input Voltage Range	V_{ICR}	±12	±13	–	–	–	–	V
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2 kΩ)	A_v	25	–	–	15	–	–	V/mV
Common Mode Rejection Ratio ($R_S \leq 10$ kΩ)	CMRR	70	90	–	–	–	–	dB
Supply Voltage Rejection Ratio ($R_S \leq 10$ kΩ)	PSRR	–	30	150	–	–	–	μV/V
Output Voltage Swing ($R_L \geq 10$ kΩ)	V_O	±12	±14	–	±12	±14	–	V
($R_L \geq 2$ kΩ)		±10	±13	–	±10	±13	–	
Supply Currents (Both Amplifiers)	I_D							mA
($T_A = T_{high}$)		–	–	4.5	–	–	5.0	
($T_A = T_{low}$)		–	–	6.0	–	–	6.7	
Power Consumption (Both Amplifiers)	P_C	–	–	135	–	–	150	mW
($T_A = T_{high}$)		–	–	180	–	–	200	
($T_A = T_{low}$)								

*T_{high} = 125°C for MC4558 and 70°C for MC4558C and MC4558AC.
T_{low} = −55°C for MC4558 and 0°C for MC4558C and MC4558AC.
†I_{IB} is out of the amplifier due to PNP input transistors.

2

FIGURE 1 – BURST NOISE versus SOURCE RESISTANCE

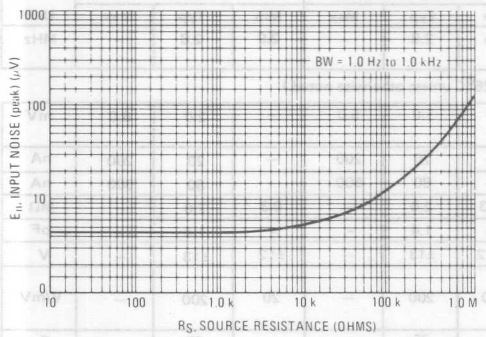


FIGURE 2 – RMS NOISE versus SOURCE RESISTANCE

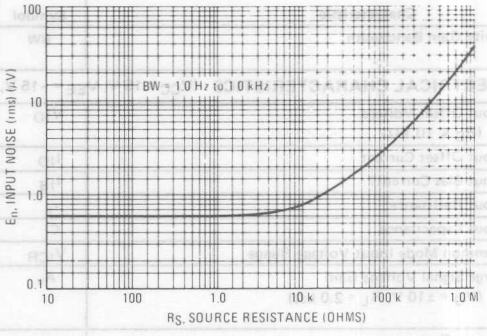


FIGURE 3 – OUTPUT NOISE versus SOURCE RESISTANCE

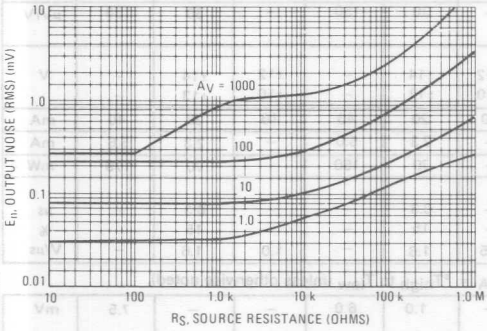


FIGURE 4 – SPECTRAL NOISE DENSITY

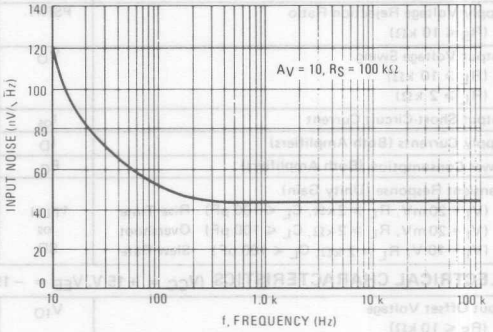
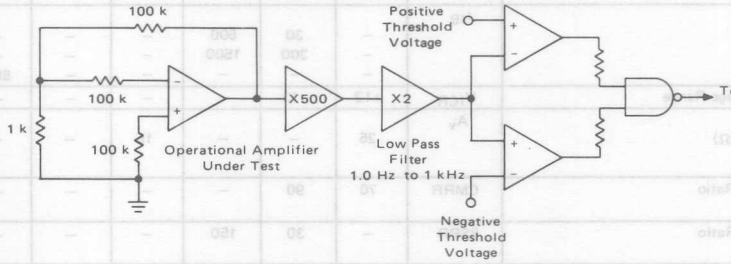


FIGURE 5 – BURST NOISE TEST CIRCUIT



Unlike conventional peak reading or RMS meters, this system was especially designed to provide the quick response time essential to burst (popcorn) noise testing.

The test time employed is 10 seconds and the 20 μV peak limit refers to the operational amplifier input thus eliminating errors in the closed-loop gain factor of the operational amplifier under test.

FIGURE 6 – OPEN LOOP FREQUENCY RESPONSE

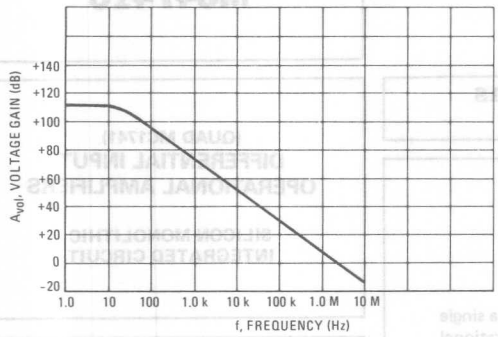


FIGURE 7 – PHASE MARGIN versus FREQUENCY

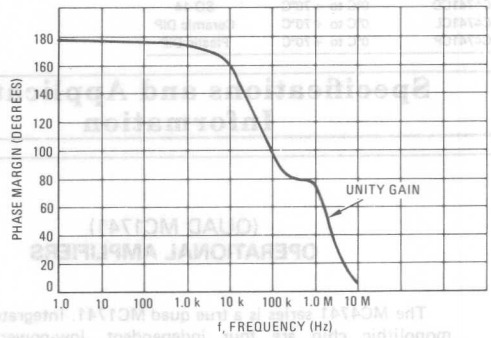


FIGURE 8 – POSITIVE OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

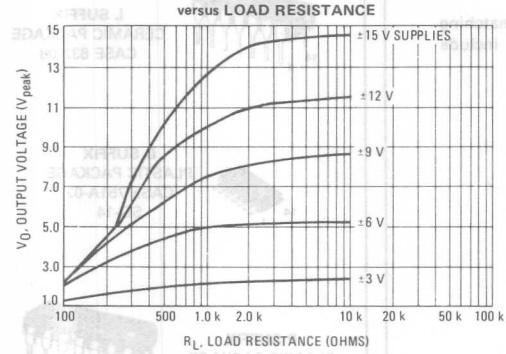


FIGURE 9 – NEGATIVE OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

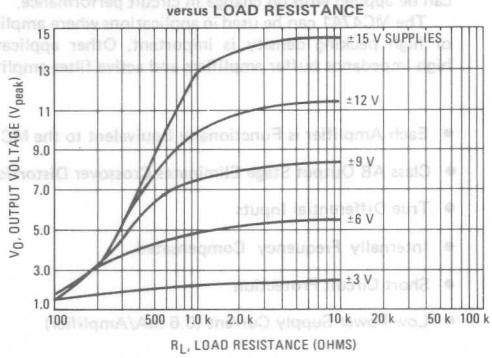


FIGURE 10 – POWER BANDWIDTH
(LARGE SIGNAL SWING versus FREQUENCY)

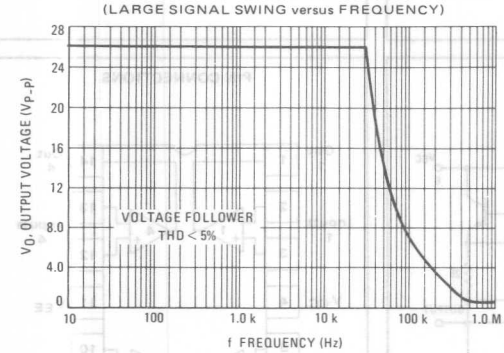
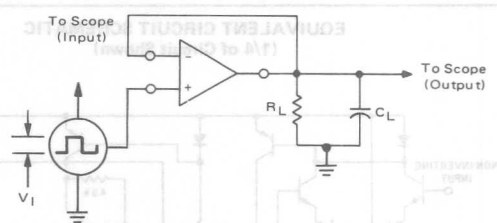


FIGURE 11 – TRANSIENT RESPONSE TEST CIRCUIT



Device	Temperature Range	Package
MC4741L	−55°C to +125°C	Ceramic DIP
MC4741CD	0°C to +70°C	SO-14
MC4741CL	0°C to +70°C	Ceramic DIP
MC4741CP	0°C to +70°C	Plastic DIP

MC4741C

Specifications and Applications Information

(QUAD MC1741)
DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

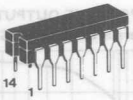
SILICON MONOLITHIC INTEGRATED CIRCUIT

(QUAD MC1741)
OPERATIONAL AMPLIFIERS

The MC4741 series is a true quad MC1741. Integrated on a single monolithic chip are four independent, low-power operational amplifiers which have been designed to provide operating characteristics identical to those of the industry standard MC1741, and can be applied with no change in circuit performance.

The MC4741 can be used in applications where amplifier matching or high packing density is important. Other applications include high impedance buffer amplifiers and active filter amplifiers.

- Each Amplifier is Functionally Equivalent to the MC1741
- Class AB Output Stage Eliminates Crossover Distortion
- True Differential Inputs
- Internally Frequency Compensated
- Short Circuit Protection
- Low Power Supply Current (0.6 mA/Amplifier)

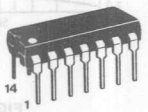


L SUFFIX
CERAMIC PACKAGE
CASE 632-08

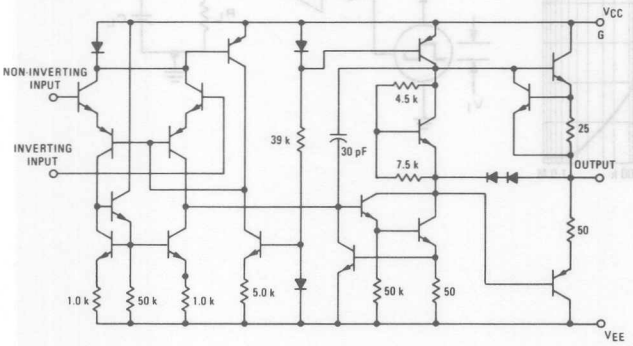


D SUFFIX
PLASTIC PACKAGE
CASE 751A-02
SO-14

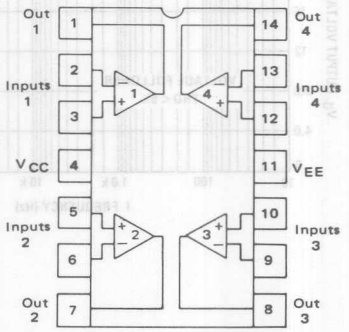
P SUFFIX
PLASTIC PACKAGE
CASE 646-06



EQUIVALENT CIRCUIT SCHEMATIC
(1/4 of Circuit Shown)



PIN CONNECTIONS



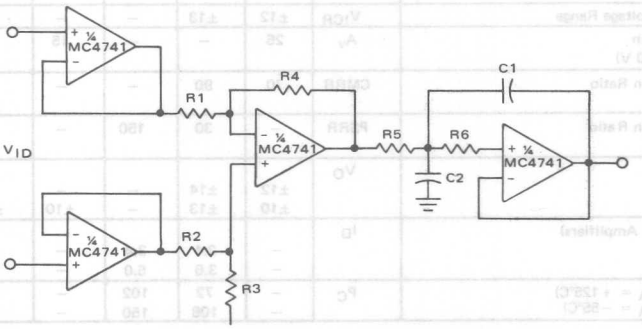
(Top View)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted).

Rating	Symbol	MC4741	MC4741C	Unit
Power Supply Voltage	V_{CC}	+22	+18	Vdc
	V_{EE}	-22	-18	Vdc
Input Differential Voltage	V_{ID}	±44	±36	Volts
Input Common Mode Voltage	V_{ICM}	±22	±18	Volts
Output Short Circuit Duration	t_S	Continuous		
Operating Ambient Temperature Range	T_A	-55 to +125	0 to +70	°C
Storage Temperature Range	T_{stg}			°C
Ceramic Package		-65 to +150		
Plastic Package		-55 to +125		
Junction Temperature	T_J			°C
Ceramic Package		175		
Plastic Package		150		

TYPICAL APPLICATION

HIGH IMPEDANCE INSTRUMENTATION BUFFER/FILTER



2

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = -15 V, T_A = 25°C unless otherwise noted).

Characteristic	Symbol	MC4741			MC4741C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10$ k)	V_{IO}	–	1.0	5.0	–	2.0	6.0	mV
Input Offset Current	I_{IO}	–	20	200	–	20	200	nA
Input Bias Current	I_{IB}	–	80	500	–	80	500	nA
Input Resistance	r_i	0.3	2.0	–	0.3	2.0	–	MΩ
Input Capacitance	C_i	–	1.4	–	–	1.4	–	pF
Offset Voltage Adjustment Range	V_{IOR}	–	±15	–	–	±15	–	mV
Common Mode Input Voltage Range	V_{ICR}	±12	±13	–	±12	±13	–	V
Large Signal Voltage Gain (V_O = ±10 V, $R_L \geq 2.0$ k)	A_v	50	200	–	20	200	–	V/mV
Output Resistance	r_o	–	75	–	–	75	–	Ω
Common Mode Rejection Ratio ($R_S \leq 10$ k)	CMRR	70	90	–	70	90	–	dB
Supply Voltage Rejection Ratio ($R_S \leq 10$ k)	PSRR	–	30	150	–	30	150	μV/V
Output Voltage Swing	V_O							V
($R_L \geq 10$ k)		±12	±14	–	±12	±14	–	
($R_L \geq 2$ k)		±10	±13	–	±10	±13	–	
Output Short-Circuit Current	I_{os}	–	20	–	–	20	–	mA
Supply Current – (All Amplifiers)	I_D	–	2.4	4.0	–	3.5	7.0	mA
Power Consumption (All Amplifiers)	P_C	–	72	120	–	105	210	mW
Transient Response (Unity Gain – Non-Inverting)								
(V_I = 20 mV, $R_L \geq 2$ k, $C_L \leq 100$ pF) Rise Time	t_{TLH}	–	0.3	–	–	0.3	–	μs
(V_I = 20 mV, $R_L \geq 2$ k, $C_L \leq 100$ pF) Overshoot	os	–	15	–	–	15	–	%
(V_I = 10 V, $R_L \geq 2$ k, $C_L \leq 100$ pF) Slew Rate	SR	–	0.5	–	–	0.5	–	V/μs

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = -15 V, T_A = *T_{high} to T_{low} unless otherwise noted.)

Characteristic	Symbol	MC4741			MC4741C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10$ kΩ)	V_{IO}	–	1.0	6.0	–	–	7.5	mV
Input Offset Current	I_{IO}							nA
(T_A = 125°C)		–	7.0	200	–	–	–	
(T_A = -55°C)		–	85	500	–	–	–	
(T_A = 0°C to +70°C)		–	–	–	–	–	300	
Input Bias Current	I_{IB}							nA
(T_A = 125°C)		–	30	500	–	–	–	
(T_A = -55°C)		–	300	1500	–	–	–	
(T_A = 0°C to +70°C)		–	–	–	–	–	800	
Common Mode Input Voltage Range	V_{ICR}	±12	±13	–	–	–	–	V
Large Signal Voltage Gain ($R_L \geq 2$ k, V_{out} = ±10 V)	A_v	25	–	–	15	–	–	V/mV
Common Mode Rejection Ratio ($R_S \leq 10$ k)	CMRR	70	90	–	–	–	–	dB
Supply Voltage Rejection Ratio ($R_S \leq 10$ k)	PSRR	–	30	150	–	–	–	μV/V
Output Voltage Swing	V_O							V
($R_L \geq 10$ k)		±12	±14	–	–	–	–	
($R_L \geq 2$ k)		±10	±13	–	±10	±13	–	
Supply Currents – (All Amplifiers)	I_D							mA
(T_A = 125°C)		–	2.4	3.4	–	–	–	
(T_A = -55°C)		–	3.6	5.0	–	–	–	
Power Consumption (T_A = +125°C)	P_C	–	72	102	–	–	–	mW
(All Amplifiers) (T_A = -55°C)		–	108	150	–	–	–	

*T_{high} = 125°C for MC4741 and 70°C for MC4741C
T_{low} = -55°C for MC4741 and 0°C for MC4741C

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted).

FIGURE 1 – POWER BANDWIDTH (LARGE SIGNAL SWING versus FREQUENCY)

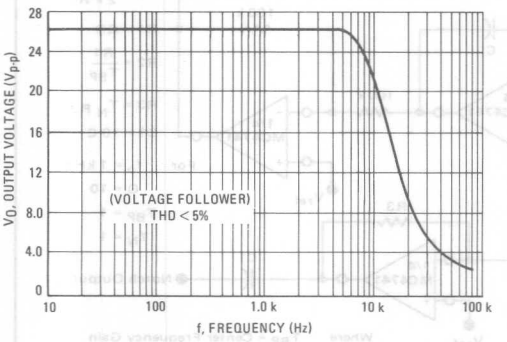


FIGURE 2 – OPEN LOOP FREQUENCY RESPONSE

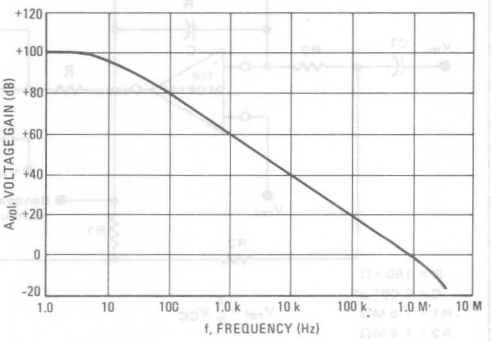


FIGURE 3 – POSITIVE OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

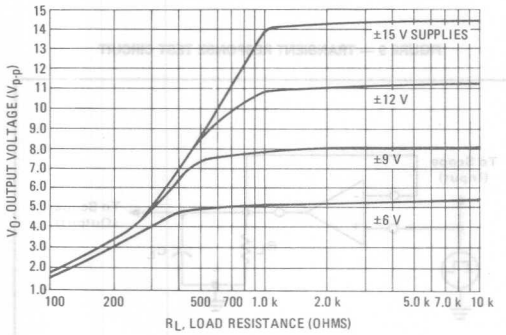


FIGURE 4 – NEGATIVE OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

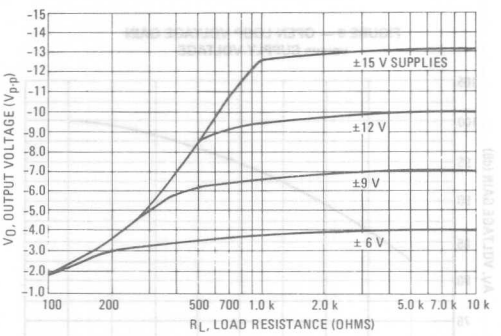


FIGURE 5 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE (Single Supply Operation)

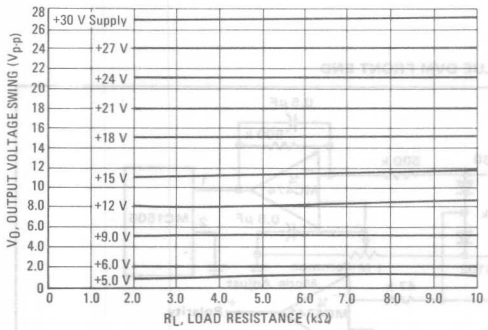
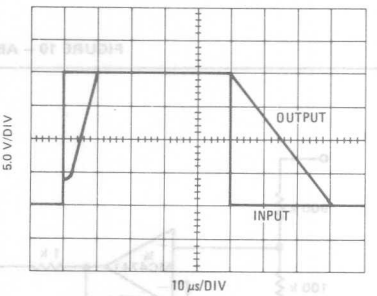


FIGURE 6 — NONINVERTING PULSE RESPONSE



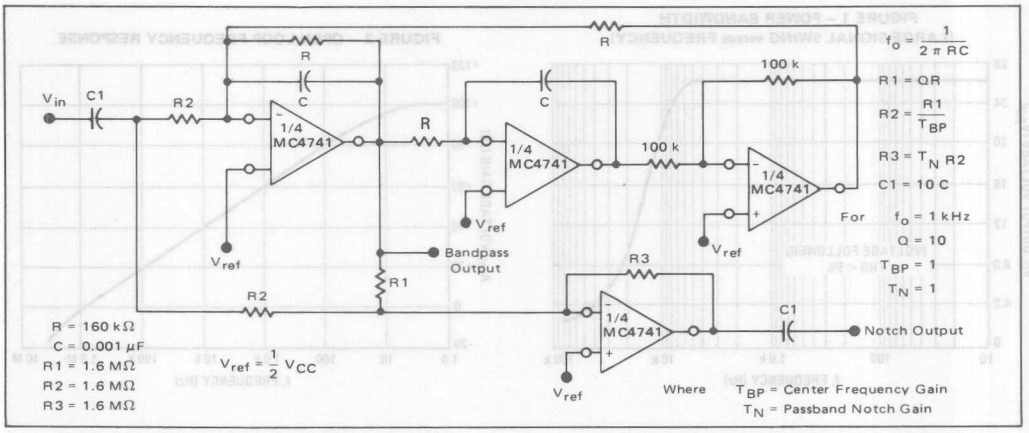


FIGURE 8 — OPEN LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE

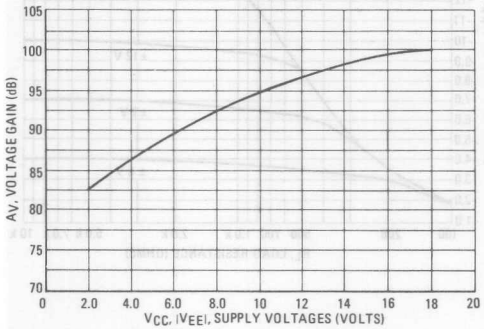


FIGURE 9 — TRANSIENT RESPONSE TEST CIRCUIT

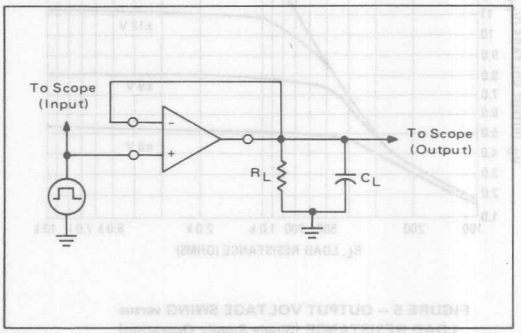
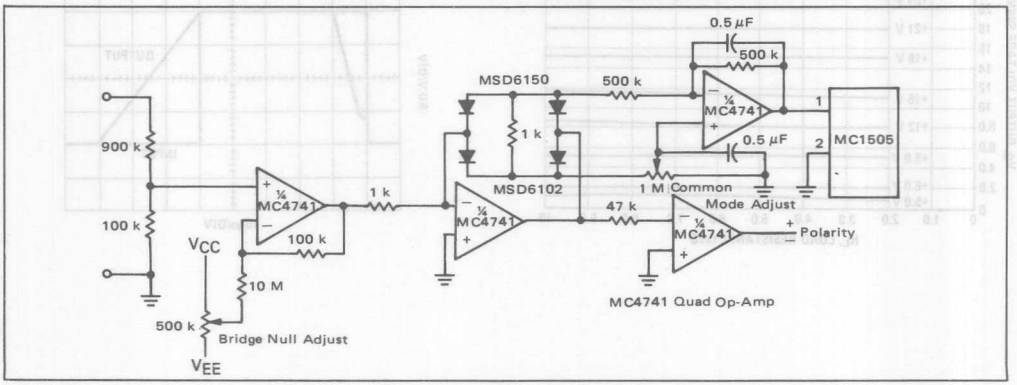


FIGURE 10 — ABSOLUTE VALUE DVM FRONT END



MOTOROLA

MC33077

Advance Information

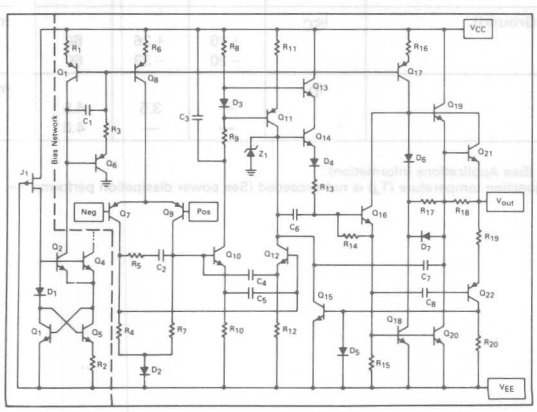
DUAL, LOW NOISE OPERATIONAL AMPLIFIER

The MC33077 is a precision high quality, high frequency, low noise monolithic dual operational amplifier employing innovative bipolar design techniques. Precision matching coupled with a unique analog resistor trim technique is used to obtain low input offset voltages. Dual-doublet frequency compensation techniques are used to enhance the gain bandwidth product of the amplifier. In addition, the MC33077 offers low input noise voltage, low temperature coefficient of input offset voltage, high slew rate, high ac and dc open-loop voltage gain and low supply current drain. The all NPN transistor output stage exhibits no deadband crossover distortion, large output voltage swing, excellent phase and gain margins, low open-loop output impedance and symmetrical source and sink ac frequency performance.

The MC33077 is tested over the vehicular temperature range and is available in plastic DIP and SO-8 package (P and D suffixes).

- Low Voltage Noise: 4.4 nV/$\sqrt{Hz}$ @ 1.0 kHz
- Low Input Offset Voltage: 0.2 mV
- Low TC of Input Offset Voltage: 2.0 μV/°C
- High Gain Bandwidth Product: 37 MHz @ 100 kHz
- High AC Voltage Gain: 370 @ 100 kHz
  1850 @ 20 kHz
- Unity Gain Stable: with Capacitance Loads to 500 pF
- High Slew Rate: 11 V/μs
- Low Total Harmonic Distortion: 0.0007%
- Large Output Voltage Swing: +14 V to −14.7 V
- High DC Open-Loop Voltage Gain: 400 k (112 dB)
- High Common Mode Rejection: 107 dB
- Low Power Supply Drain Current: 3.5 mA
- Dual Supply Operation: ±2.5 V to ±18 V

EQUIVALENT CIRCUIT SCHEMATIC (EACH AMPLIFIER)



DUAL OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

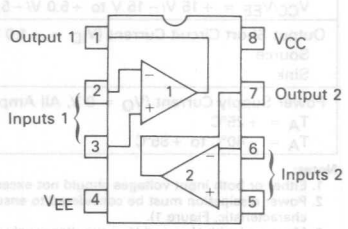


P SUFFIX
PLASTIC PACKAGE
CASE 626-05



D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SO-8

PIN ASSIGNMENTS



Dual, Top View

ORDERING INFORMATION

Op Amp Function	Device	Ambient Test Temperature Range	Package
Dual	MC33077D MC33077P	−40°C to +85°C	SO-8 Plastic DIP

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	+36	Volts
Input Differential Voltage Range	V_{IDR}	(Note 1)	Volts
Input Voltage Range	V_{IR}	(Note 1)	Volts
Output Short Circuit Duration (Note 2)	t_S	Indefinite	Seconds
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	−60 to +150	°C
Maximum Power Dissipation	P_D	(Note 2)	mW

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V) T_A = +25°C T_A = −40°C to +85°C	$\|V_{IO}\|$	 — —	 0.13 —	 1.0 1.5	mV
Average Temperature Coefficient of Input Offset Voltage R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V, T_A = −40°C to +85°C	$\Delta V_{IO}/\Delta T$	—	2.0	—	μV/°C
Input Bias Current (V_{CM} = 0 V, V_O = 0 V) T_A = +25°C T_A = −40°C to +85°C	I_{IB}	 — —	 280 —	 1000 1200	nA
Input Offset Current (V_{CM} = 0 V, V_O = 0 V) T_A = +25°C T_A = −40°C to +85°C	I_{IO}	 — —	 15 —	 180 240	nA
Common Mode Input Voltage Range (ΔV_{IO} = 5.0 mV, V_O = 0 V)	V_{ICR}	±13.5	±14	—	V
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 kΩ) T_A = +25°C T_A = −40°C to +85°C	A_{VOL}	 150 k 125 k	 400 k —	 — —	V/V
Output Voltage Swing (V_{ID} = ±1.0 V) R_L = 2.0 kΩ R_L = 2.0 kΩ R_L = 10 kΩ R_L = 10 kΩ	 V_O+ V_O- V_O+ V_O-	 13 — 13.4 —	 13.6 −14.1 14 −14.7	 — −13.5 — −14.3	V
Common Mode Rejection (V_{in} = ±13 V)	CMR	85	107	—	dB
Power Supply Rejection (Note 3) V_{CC}/V_{EE} = +15 V/−15 V to +5.0 V/−5.0 V	PSR	80	90	—	dB
Output Short Circuit Current (V_{ID} = ±1.0 V, Output to Ground) Source Sink	I_{SC}	 +10 −20	 +26 −33	 60 60	mA
Power Supply Current (V_O = 0 V, All Amplifiers) T_A = +25°C T_A = −40°C to +85°C	I_D	 — —	 3.5 —	 4.5 4.8	mA

Notes:
1. Either or both input voltages should not exceed V_{CC} or V_{EE} (See Applications Information).
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (See power dissipation performance characteristic, Figure 1).
3. Measured with V_{CC} and V_{EE} simultaneously varied.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = −10 V to +10 V, R_L = 2.0 kΩ, C_L = 100 pF, A_V = +1.0)	SR	8.0	11	—	V/μs
Gain Bandwidth Product (f = 100 kHz)	GBW	25	37	—	MHz
AC Voltage Gain (R_L = 2.0 kΩ, V_O = 0 V) f = 100 kHz f = 20 kHz	A_{VO}	 — —	 370 1850	 — —	V/V
Unity Gain Frequency (Open-Loop)	f_U	—	7.5	—	MHz
Gain Margin (R_L = 2.0 kΩ, C_L = 0 pF)	A_m	—	10	—	dB
Phase Margin (R_L = 2.0 kΩ, C_L = 0 pF)	$Ø_m$	—	55	—	Deg
Channel Separation (f = 20 Hz to 20 kHz, R_L = 2.0 kΩ, V_O = 10 V_{p-p})	CS	—	−120	—	dB
Power Bandwidth (V_O = 27 V_{p-p}, R_L = 2.0 kΩ, THD ≤ 1%)	BW_P	—	200	—	kHz
Distortion (R_L = 2.0 kΩ) A_V = +1.0, f = 20 Hz to 20 kHz V_O = 3.0 V_{rms} A_V = 2000, f = 20 kHz V_O = 2.0 V_{p-p} V_O = 10 V_{p-p} A_V = 4000, f = 100 kHz V_O = 2.0 V_{p-p} V_O = 10 V_{p-p}	THD	 — — — — —	 0.0007 0.215 0.242 0.319 0.316	 — — — — —	%
Open-Loop Output Impedance (V_O = 0 V, f = f_U)	$\|Z_O\|$	—	36	—	Ω
Differential Input Resistance (V_{CM} = 0 V)	R_{IN}	—	270	—	kΩ
Differential Input Capacitance (V_{CM} = 0 V)	C_{IN}	—	15	—	pF
Equivalent Input Noise Voltage (R_S = 100 Ω) f = 10 Hz f = 1.0 kHz	e_n	 — —	 6.7 4.4	 — —	nV/√Hz
Equivalent Input Noise Current (f = 1.0 kHz) f = 10 Hz f = 1.0 kHz	i_n	 — —	 1.3 0.6	 — —	pA/√Hz

FIGURE 1 — MAXIMUM POWER DISSIPATION versus TEMPERATURE

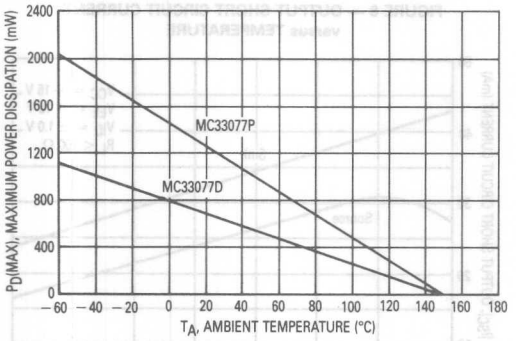


FIGURE 2 — INPUT BIAS CURRENT versus SUPPLY VOLTAGE

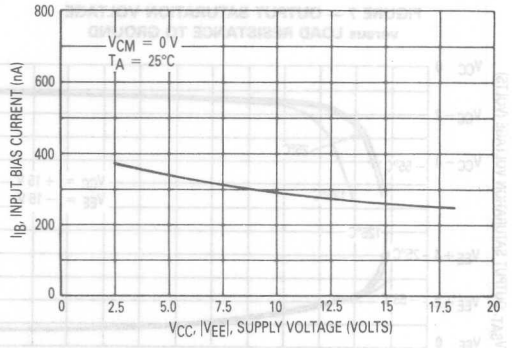


FIGURE 3 — INPUT BIAS CURRENT versus TEMPERATURE

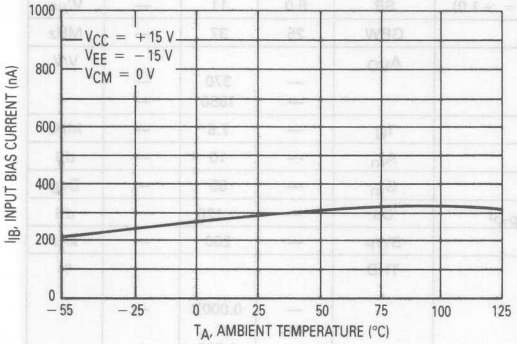


FIGURE 4 — INPUT OFFSET VOLTAGE versus TEMPERATURE

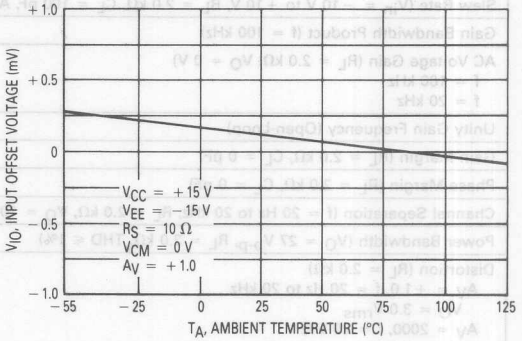


FIGURE 5 — INPUT BIAS CURRENT versus COMMON MODE VOLTAGE

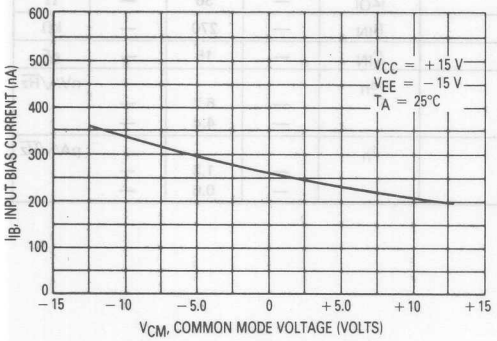


FIGURE 6 — INPUT COMMON MODE VOLTAGE RANGE versus TEMPERATURE

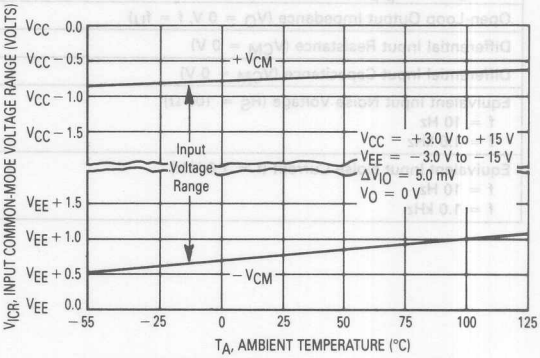


FIGURE 7 — OUTPUT SATURATION VOLTAGE versus LOAD RESISTANCE TO GROUND

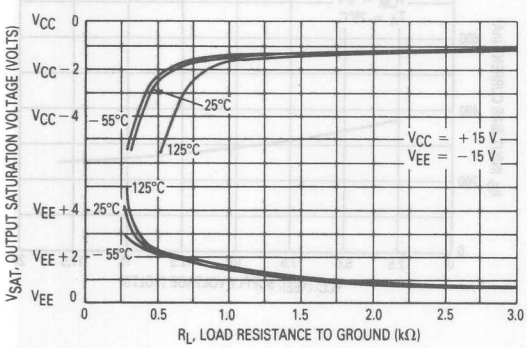


FIGURE 8 — OUTPUT SHORT CIRCUIT CURRENT versus TEMPERATURE

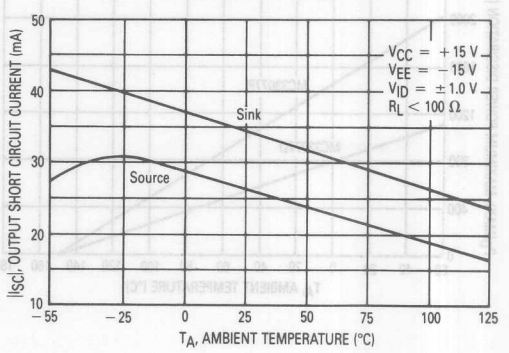


FIGURE 9 — SUPPLY CURRENT versus TEMPERATURE

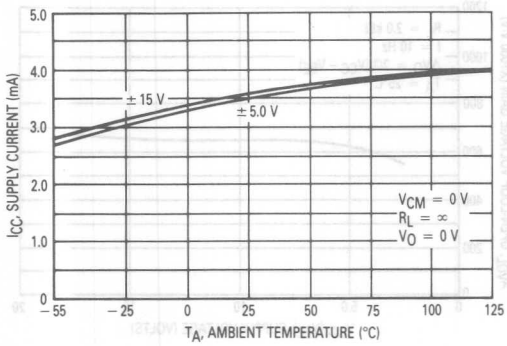


FIGURE 10 — COMMON MODE REJECTION versus FREQUENCY

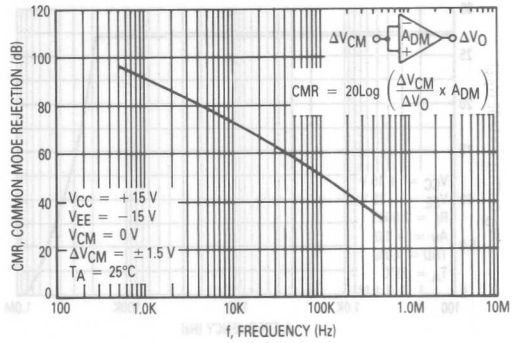


FIGURE 11 — POWER SUPPLY REJECTION versus FREQUENCY

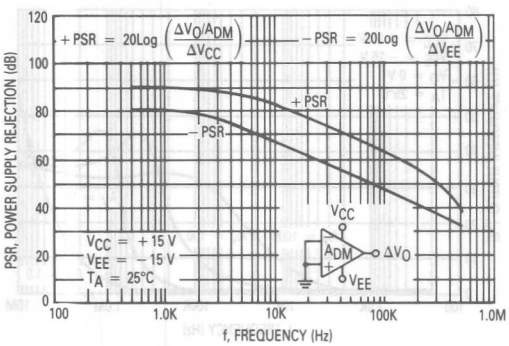


FIGURE 12 — GAIN BANDWIDTH PRODUCT versus SUPPLY VOLTAGE

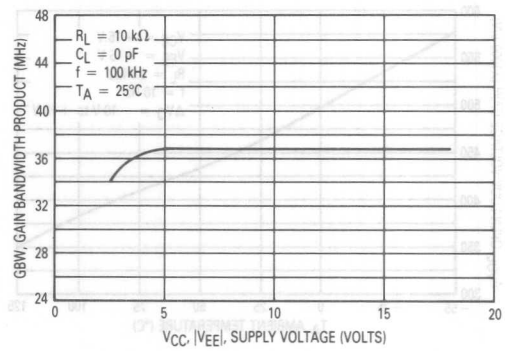


FIGURE 13 — GAIN BANDWIDTH PRODUCT versus TEMPERATURE

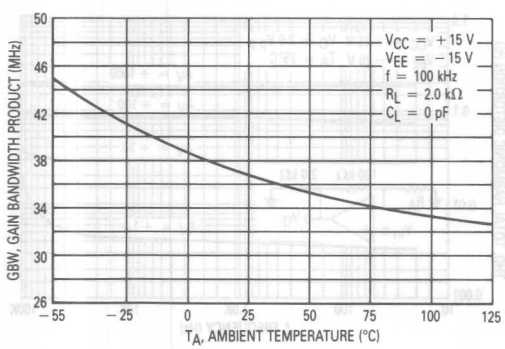
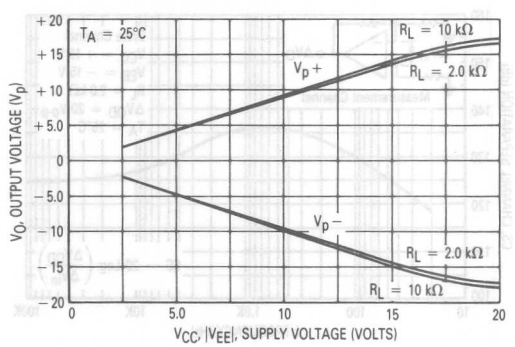


FIGURE 14 — MAXIMUM OUTPUT VOLTAGE versus SUPPLY VOLTAGE



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FIGURE 15 — OUTPUT VOLTAGE versus FREQUENCY

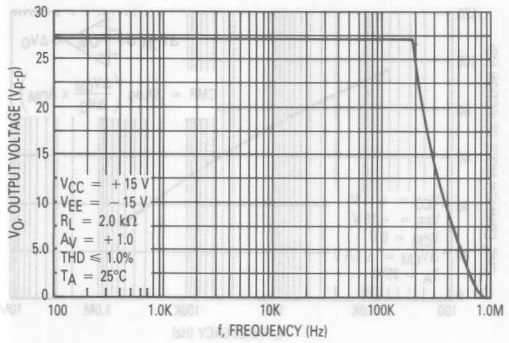


FIGURE 16 — OPEN-LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE

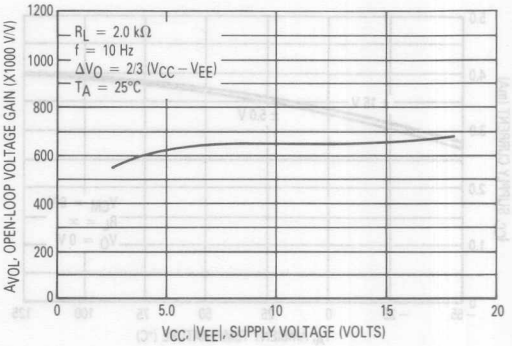


FIGURE 17 — OPEN-LOOP VOLTAGE GAIN versus TEMPERATURE

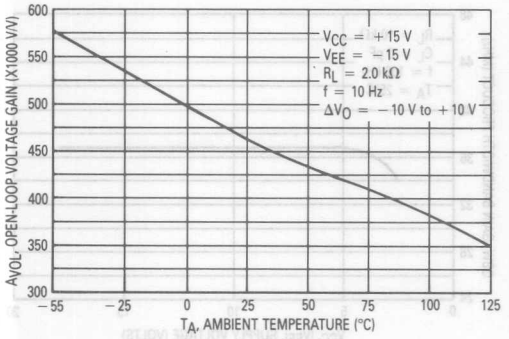


FIGURE 18 — OUTPUT IMPEDANCE versus FREQUENCY

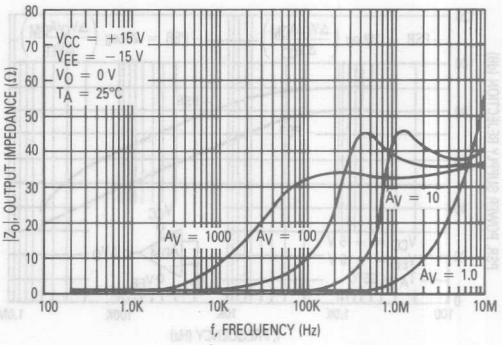


FIGURE 19 — CHANNEL SEPARATION versus FREQUENCY

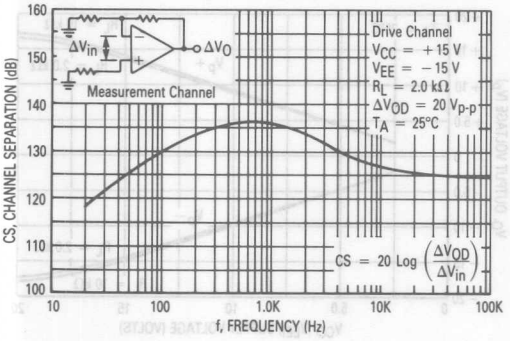


FIGURE 20 — TOTAL HARMONIC DISTORTION versus FREQUENCY

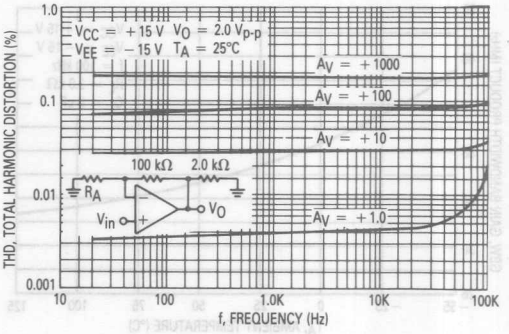


FIGURE 21 — TOTAL HARMONIC DISTORTION versus FREQUENCY

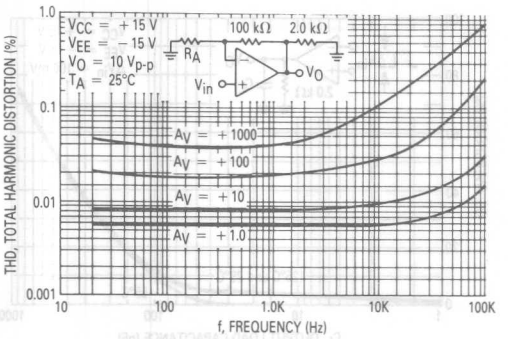


FIGURE 22 — TOTAL HARMONIC DISTORTION versus OUTPUT VOLTAGE

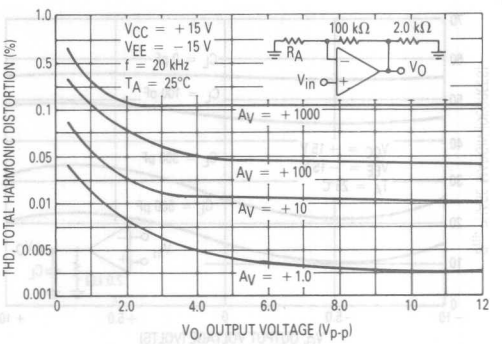


FIGURE 23 — SLEW RATE versus SUPPLY VOLTAGE

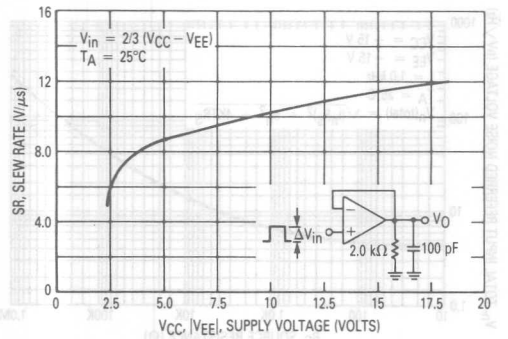


FIGURE 24 — SLEW RATE versus TEMPERATURE

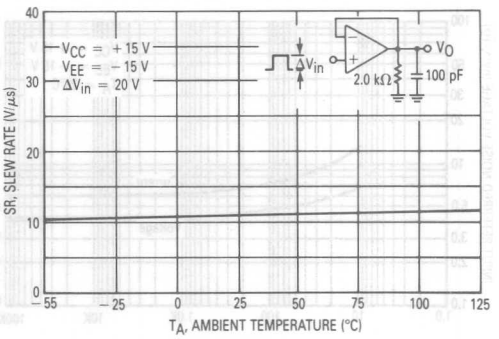


FIGURE 25 — VOLTAGE GAIN and PHASE versus FREQUENCY

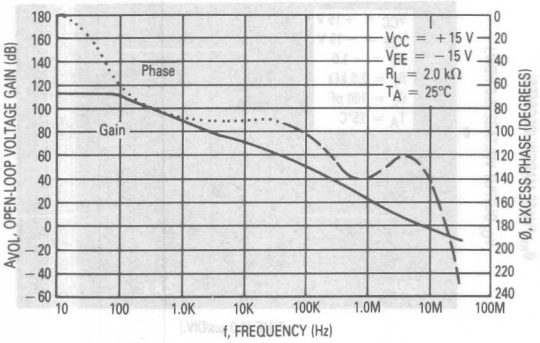


FIGURE 26 — OPEN-LOOP GAIN MARGIN and PHASE MARGIN versus OUTPUT LOAD CAPACITANCE

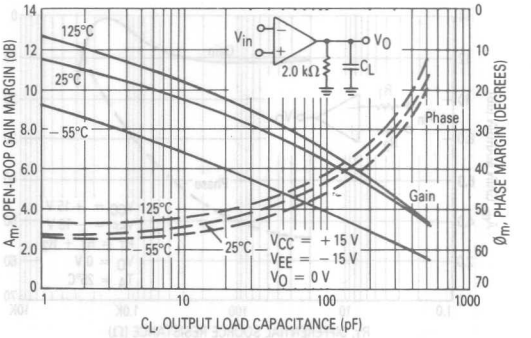


FIGURE 27 — PHASE MARGIN versus OUTPUT VOLTAGE

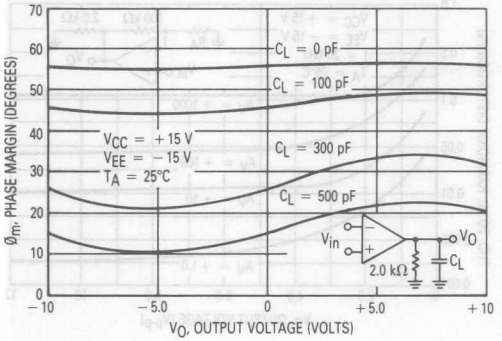


FIGURE 28 — OVERSHOOT versus OUTPUT LOAD CAPACITANCE

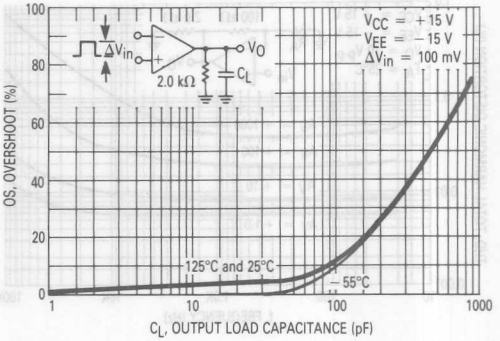


FIGURE 29 — INPUT REFERRED NOISE VOLTAGE and CURRENT versus FREQUENCY

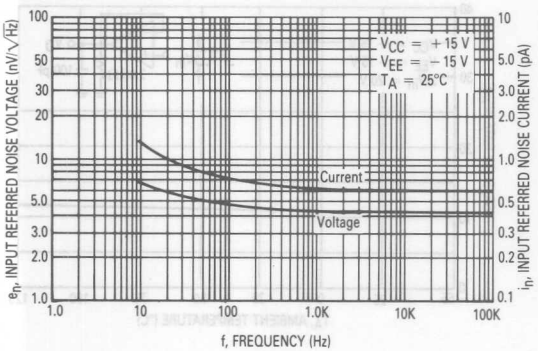


FIGURE 30 — TOTAL INPUT REFERRED NOISE VOLTAGE versus SOURCE RESISTANCE

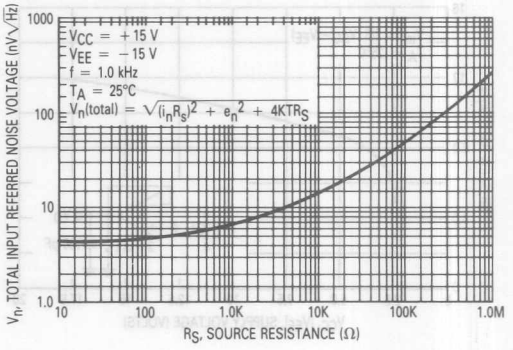


FIGURE 31 — PHASE MARGIN AND GAIN MARGIN versus DIFFERENTIAL SOURCE RESISTANCE

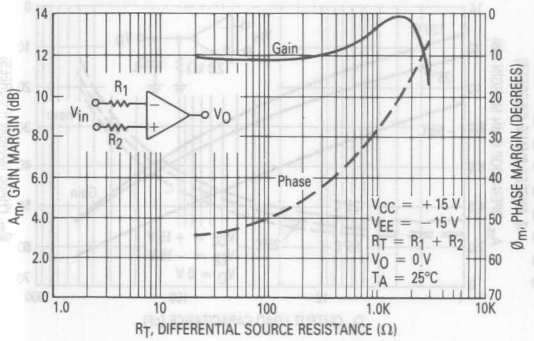


FIGURE 32 — INVERTING AMPLIFIER SLEW RATE

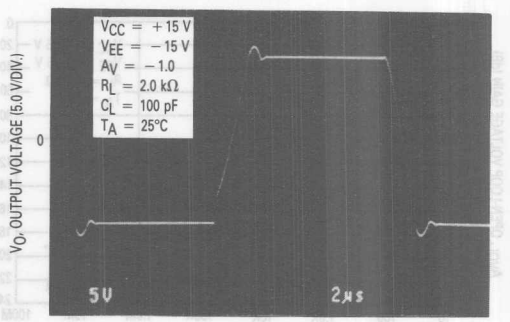


FIGURE 33 — NON-INVERTING AMPLIFIER SLEW RATE

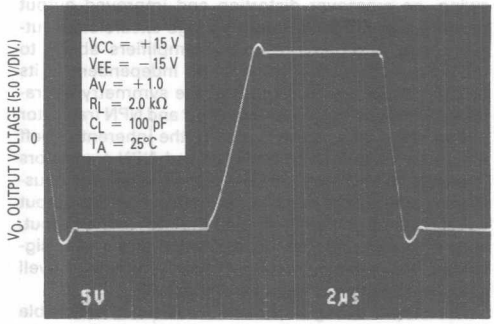


FIGURE 34 — NON-INVERTING AMPLIFIER OVERSHOOT

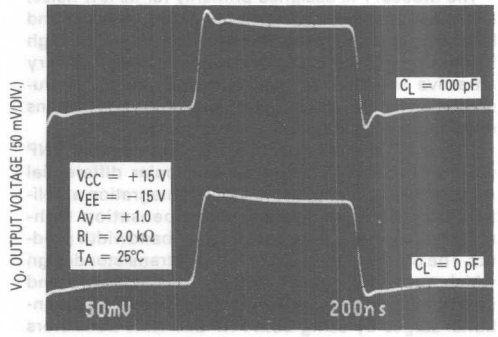
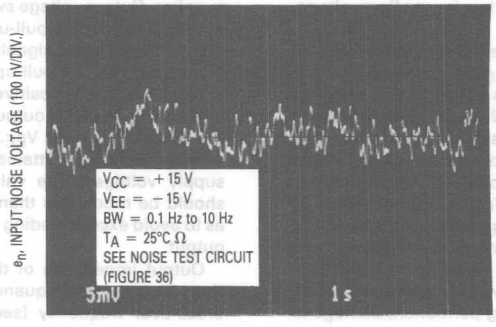


FIGURE 35 — LOW FREQUENCY NOISE VOLTAGE versus TIME



2

APPLICATIONS INFORMATION

The MC33077 is designed primarily for its low noise, low offset voltage, high gain bandwidth product and large output swing characteristics. Its outstanding high frequency gain/phase performance make it a very attractive amplifier for high quality pre-amps, instrumentation amps, active filters and other applications requiring precision quality characteristics.

The MC33077 utilizes high frequency lateral PNP input transistors in a low noise bipolar differential stage driving a compensated Miller integration amplifier. Dual-doublet frequency compensation techniques are used to enhance the gain bandwidth product. The output stage uses an all NPN transistor design which provides greater output voltage swing and improved frequency performance over more conventional stages by using both PNP and NPN transistors (Class AB). This combination produces an amplifier with superior characteristics.

Through precision component matching and innovative current mirror design, a lower than normal temperature coefficient of input offset voltage (2.0 μV/°C as opposed to 10 μV/°C), as well as low input offset voltage, is accomplished.

The minimum common mode input range is from 1.5 volts below the positive rail (V_{CC}) to 1.5 volts above the negative rail (V_{EE}). The inputs will typically common mode to within 1.0 volt of both negative and positive rails though degradation in offset voltage and gain will be experienced as the common mode voltage nears either supply rail. In practice, though not recommended, the input voltage may exceed V_{CC} by approximately 30 volts and decrease below the V_{EE} rail by approximately 0.6 volts without causing permanent damage to the device. If the input voltage on either or both inputs is less than approximately 0.6 volts, excessive current may flow, if not limited, causing permanent damage to the device.

The amplifier will not latch with input source currents up to 20 mA, though in practice, source currents should be limited to 5.0 mA so as to avoid any parametric damage to the device. If both inputs exceed V_{CC}, the output will be in the high state and phase reversal may occur. No phase reversal will occur if the voltage on one input is within the common mode range and the voltage on the other input exceeds V_{CC}. Phase reversal may occur if the input voltage on either or both inputs is less than 1.0 volt above the negative rail. Phase reversal will be experienced if the voltage on either or both inputs is less than V_{EE}.

Through the use of dual-doublet frequency compensation techniques, the gain bandwidth product has been greatly enhanced over other amplifiers using the conventional single pole compensation. The phase and gain error of the amplifier remains low to higher frequencies for fixed amplifier gain configurations.

With the all NPN output stage, there is minimal swing loss to the supply rails, producing superior output swing, no crossover distortion and improved output phase symmetry with output voltage excursions. Output phase symmetry being the amplifiers ability to maintain a constant phase relation independent of its output voltage swing. Output phase symmetry degradation in the more conventional PNP and NPN transistor output stage was primarily due to the inherent cut-off frequency mismatch of the PNP and NPN transistors (typically 10 MHz and 300 MHz respectively) used causing considerable phase change to occur as the output voltage changes. By eliminating the PNP in the output, such phase change has been avoided and a very significant improvement in output phase symmetry as well as output swing has been accomplished.

The output swing improvement is most noticeable when operation is with lower supply voltages (typically 30% with ±5.0 V supplies). With a 10 k load, the output of the amplifier can typically swing to within 1.0 V of the positive rail (V_{CC}), and to within 0.3 V of the negative rail (V_{EE}), producing a 28.7 V_{p-p} signal from ±15 V supplies. Output voltage swing can be further improved by using an output pull-up resistor referenced to the V_{CC}. Where output signals are referenced to the positive supply rail, the pull-up resistor will pull the output to V_{CC} during the positive swing and during the negative swing, the NPN output transistor collector will pull the output very near V_{EE}. This configuration will produce the maximum attainable output signal from given supply voltages. The value of load resistance used should be much less than any feedback resistance so as to avoid excess loading and allow easy pull-up of the output.

Output impedance of the amplifier is typically less than 50 ohms at frequencies less than the unity gain cross-over frequency (see Output Impedance versus Frequency curve). The amplifier is unity gain stable with output capacitance loads up to 500 pF at full output swing over the −55°C to +125°C temperature range. Output phase symmetry is excellent with typically 4° total phase change over a 20 volt output excursion at 25°C with a 2.0 kΩ and 100 pF load. With a 2.0 kΩ resistive load and no capacitance loading the total phase change is approximately one degree for the same 20 volt output excursion. With a 2.0 kΩ and 500 pF load at 125°C the total phase change is typically only 10° for a 20 volt output excursion (see Phase Margin versus Output Voltage curve).

As with all amplifiers, care should be exercised so as to insure that one does not create a pole at the input of the amplifier which is near the closed loop corner frequency. This becomes a greater concern when using high frequency amplifiers since it is very easy to create such a pole with relatively small values of resistance on the inputs. If this does occur, the amplifiers phase will

degrade severely causing the amplifier to become unstable. Effective source resistances, acting in conjunction with the input capacitance of the amplifier, should be kept to a minimum so as to avoid creating such a pole at the input (see Phase Margin and Gain Margin versus Differential Source Resistance curve). There is minimal effect on stability where the created input pole is much greater than the closed loop corner frequency. Where amplifier stability is affected as a result of a negative feedback resistor in conjunction with the amplifier's input capacitance, creating a pole near the closed loop corner frequency, lead capacitor compensation techniques (lead capacitor in parallel with the feedback resistor) can be employed to improve stability. The feedback resistor and lead capacitor RC time constant should be larger than that of the uncompensated input pole frequency. Having a high resistance connected to the non-inverting input of the amplifier can create a like instability problem. Compensation for this condition can be accomplished by adding a lead capacitor in parallel with the non-inverting input resistor of such a value as to make the RC time constant larger than the RC time constant of the uncompensated input resistor acting in conjunction with the amplifiers input capacitance.

For optimum frequency performance and stability careful component placement and printed circuit board layout should be exercised. For example, long unshielded input or output leads may result in unwanted input-output coupling. In order to reduce the input capacitance, the body of resistors connected to the input pins should be physically close to the input pins. This not only minimizes the input pole creation for optimum frequency response, but also minimizes extraneous signal "pickup" at this node. Power supplies should be decoupled with adequate capacitance as close as possible to the device supply pin.

In addition to amplifier stability considerations, input source resistance values should be low so as to take full advantage of the low noise characteristics of the amplifier. Thermal noise (Johnson noise) of a resistor is generated by thermally-charged carriers randomly moving within the resistor creating a voltage. The rms thermal noise voltage in a resistor can be calculated from:

$$E_{nr} = \sqrt{4kTR \times BW}$$

where:

k = Boltzmann's constant (1.38×10^{-23} joules/K)
T = Kelvin temperature
R = Resistance in ohms
BW = Upper and lower frequency limit in hertz.

By way of reference, a 1.0 kΩ resistor, at 25°C, will produce 4.0 nV/$\sqrt{Hz}$ of rms noise voltage. If this resistor is connected to the input of the amplifier, the noise voltage will be gained up in accordance to the amplifiers gain configuration. For this reason the selection of input source resistance for low noise circuit applications warrants serious consideration. The total noise of the amplifier, as referred to its inputs, is typically only 4.4 nV/$\sqrt{Hz}$ at 1.0 kHz.

The output of any one amplifier is current limited and thus protected from a direct short to ground. However, under such conditions, it is important to not allow the amplifier to exceed the maximum junction temperature rating. Typically for ±15 volt supplies, any one output can be shorted continuously to ground without exceeding the temperature rating.

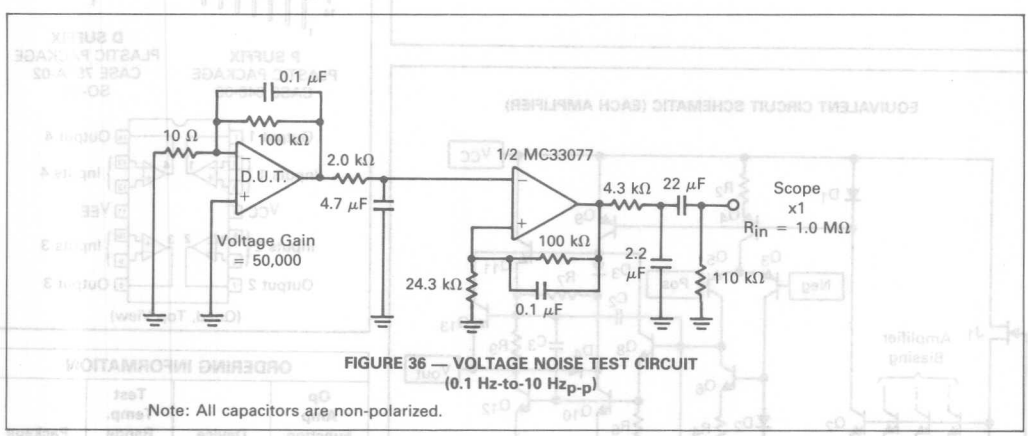


FIGURE 36 — VOLTAGE NOISE TEST CIRCUIT (0.1 Hz-to-10 Hz_{p-p})

Note: All capacitors are non-polarized.

MOTOROLA

MC33079

Advance Information

LOW NOISE OPERATIONAL AMPLIFIER

The MC33078/9 series is a family of high quality monolithic amplifiers employing Bipolar technology with innovative high-performance concepts for quality audio and data signal processing applications. This family incorporates the use of high frequency PNP input transistors to produce amplifiers exhibiting low input voltage noise with high gain bandwidth product and slew rate. The all NPN output stage exhibits no deadband crossover distortion, large output voltage swing, excellent phase and gain margins, low open-loop high frequency output impedance and symmetrical source and sink ac frequency performance.

The MC33078/9 family offers both dual and quad amplifier versions, tested over the vehicular temperature range and available in the plastic DIP and SOIC packages (P and D suffixes).

- Dual Supply Operation: ±18 V (Max)
- Low Voltage Noise: 4.5 nV/√Hz
- Low Input Offset Voltage: 0.15 mV
- Low T.C. of Input Offset Voltage: 2.0 μV/°C
- Low Total Harmonic Distortion: 0.002%
- High Gain Bandwidth Product: 16 MHz
- High Slew Rate: 7.0 V/μs
- High Open-Loop ac Gain: 800 @ 20 kHz
- Excellent Frequency Stability
- Large Output Voltage Swing: +14.1 V/−14.6 V

DUAL/QUAD OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUIT

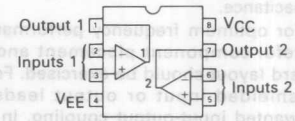
MC33078



P SUFFIX
PLASTIC PACKAGE
CASE 626-05

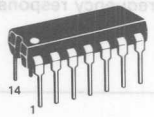


D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SO-8



(Dual, Top View)

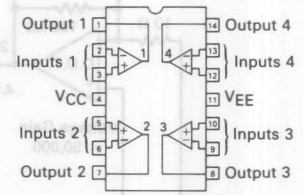
MC33079



P SUFFIX
PLASTIC PACKAGE
CASE 646-06

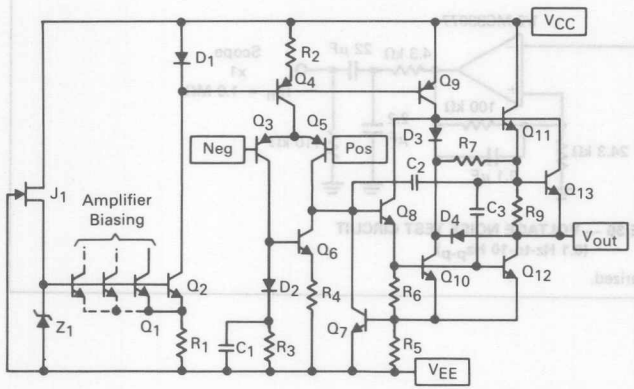


D SUFFIX
PLASTIC PACKAGE
CASE 751A-02
SO-14



(Quad, Top View)

EQUIVALENT CIRCUIT SCHEMATIC (EACH AMPLIFIER)



ORDERING INFORMATION			
Op Amp Function	Device	Test Temp. Range	Package
Dual	MC33078D MC33078P	−40°C to +85°C	SO-8 Plastic DIP
Quad	MC33079D MC33079P	−40°C to +85°C	SO-14 Plastic DIP

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	+36	Volts
Input Differential Voltage Range	V_{IDR}	(Note 1)	Volts
Input Voltage Range	V_{IR}	(Note 1)	Volts
Output Short-Circuit Duration (Note 2)	t_S	Indefinite	Seconds
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	−60 to +150	°C
Maximum Power Dissipation	P_D	(Note 2)	mW

Notes:
1. Either or both input voltages must not exceed the magnitude of V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (See power dissipation performance characteristic, Figure 1).
3. Measured with V_{CC} and V_{EE} differentially varied simultaneously.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V)	$\|V_{IO}\|$				mV
MC33078 T_A = +25°C		—	0.15	2.0	
T_A = −40°C to +85°C		—	—	3.0	
MC33079 T_A = +25°C		—	0.15	2.5	
T_A = −40°C to +85°C		—	—	3.5	
Average Temperature Coefficient of Input Offset Voltage R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V, T_A = T_{low} to T_{high}	$\Delta V_{IO}/\Delta T$	—	2.0	—	μV/°C
Input Bias Current (V_{CM} = 0 V, V_O = 0 V)	I_{IB}				nA
T_A = +25°C		—	300	750	
T_A = −40°C to +85°C		—	—	800	
Input Offset Current (V_{CM} = 0 V, V_O = 0 V)	I_{IO}				nA
T_A = +25°C		—	25	150	
T_A = −40°C to +85°C		—	—	175	
Common Mode Input Voltage Range (ΔV_{IO} = 5.0 mV, V_O = 0 V)	V_{ICR}	±13	±14	—	V
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 kΩ)	A_{VOL}				dB
T_A = +25°C		90	110	—	
T_A = −40°C to +85°C		85	—	—	
Output Voltage Swing (V_{ID} = ±1.0 V)					V
R_L = 600 Ω	V_O+	—	10.7	—	
R_L = 600 Ω	V_O-	—	−11.9	—	
R_L = 2.0 kΩ	V_O+	13.2	13.8	—	
R_L = 2.0 kΩ	V_O-	—	−13.7	−13.2	
R_L = 10 kΩ	V_O+	13.5	14.1	—	
R_L = 10 kΩ	V_O-	—	−14.6	−14	
Common Mode Rejection (V_{in} = ±13 V)	CMR	80	100	—	dB
Power Supply Rejection (Note 3) V_{CC}/V_{EE} = +15 V/−15 V to +5.0 V/−5.0 V	PSR	80	105	—	dB
Output Short Circuit Current (V_{ID} = 1.0 V, Output to Ground)	I_{SC}				mA
Source		+15	+29	—	
Sink		−20	−37	—	
Power Supply Current (V_O = 0 V, All Amplifiers)	I_D				mA
MC33078 T_A = +25°C		—	4.1	5.0	
T_A = −40°C to +85°C		—	—	5.5	
MC33079 T_A = +25°C		—	8.4	10	
T_A = −40°C to +85°C		—	—	11	

2

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C unless otherwise noted)

Characteristics		Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = −10 V to +10 V, R_L = 2.0 kΩ, C_L = 100 pF, A_V = +1.0)		SR	5.0	7.0	—	V/μs
Gain BAndwidth Product (f = 100 kHz)		GBW	10	16	—	MHz
Unity Gain Frequency (Open-Loop)		f_U	—	9.0	—	MHz
Gain Margin (R_L = 2.0 kΩ)	C_L = 0 pF	A_m	—	−11	—	dB
	C_L = 100 pF		—	−6.0	—	
Phase Margin (R_L = 2.0 kΩ)	C_L = 0 pF	ϕ_m	—	55	—	Deg
	C_L = 100 pF		—	40	—	
Channel Separation (f = 20 Hz to 20 kHz)		CS	—	−120	—	dB
Power Bandwidth (V_O = 27 V_{p-p}, R_L = 2.0 kΩ, THD ≤ 1.0%)		BW_P	—	120	—	kHz
Distortion (R_L = 2.0 kΩ, f = 20 Hz to 20 kHz, V_O = 3.0 V_{rms}, A_V = +1.0)		THD	—	0.002	—	%
Open-Loop Output Impedance (V_O = 0 V, f = 9.0 MHz)		$\|Z_O\|$	—	37	—	Ω
Differential Input Resistance (V_{CM} = 0 V)		R_{IN}	—	175	—	kΩ
Differential Input Capacitance (V_{CM} = 0 V)		C_{IN}	—	12	—	pF
Equivalent Input Noise Voltage (R_S = 100 Ω, f = 1.0 kHz)		e_n	—	4.5	—	$nV/\sqrt{Hz}$
Equivalent Input Noise Current (f = 1.0 kHz)		i_n	—	0.5	—	$pA/\sqrt{Hz}$

TYPICAL CHARACTERISTICS

FIGURE 1 — MAXIMUM POWER DISSIPATION versus TEMPERATURE

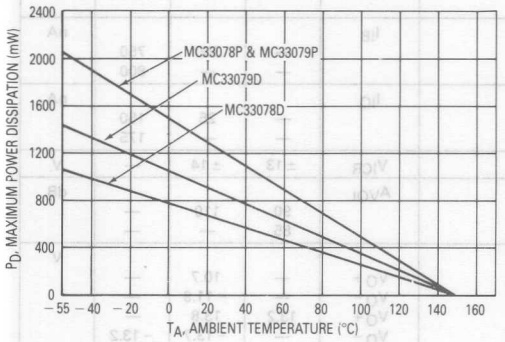


FIGURE 2 — INPUT BIAS CURRENT versus SUPPLY VOLTAGE

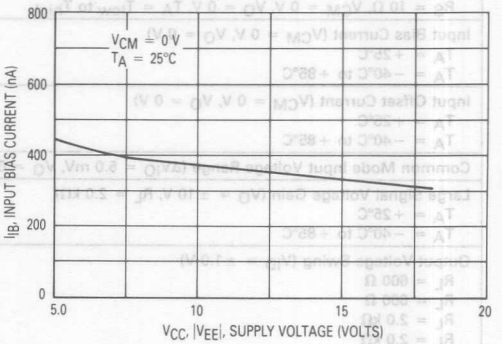


FIGURE 3 — INPUT BIAS CURRENT versus TEMPERATURE

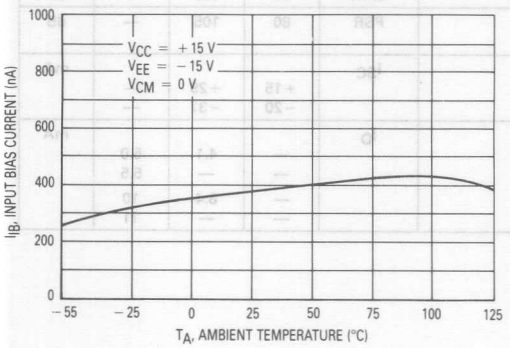
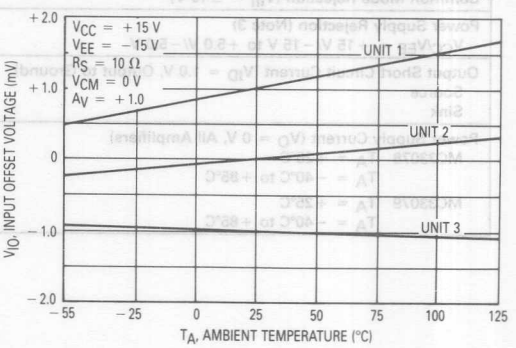


FIGURE 4 — INPUT OFFSET VOLTAGE versus TEMPERATURE



TYPICAL CHARACTERISTICS — continued

FIGURE 5 — INPUT BIAS CURRENT versus COMMON MODE VOLTAGE

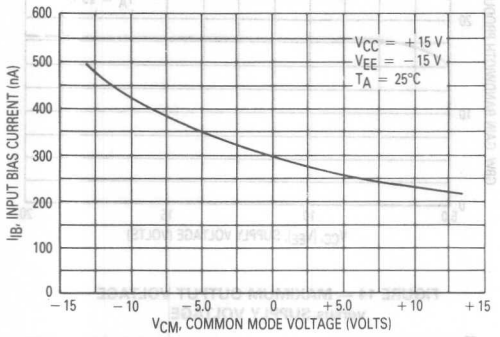


FIGURE 6 — INPUT COMMON-MODE VOLTAGE RANGE versus TEMPERATURE

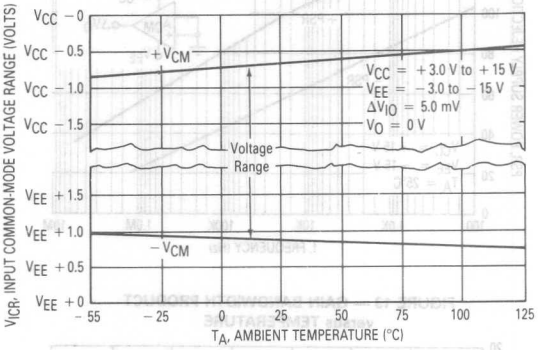


FIGURE 7 — OUTPUT SATURATION VOLTAGE versus LOAD RESISTANCE TO GROUND

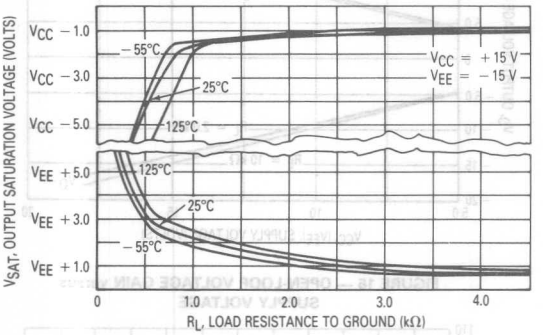


FIGURE 8 — OUTPUT SHORT CIRCUIT CURRENT versus TEMPERATURE

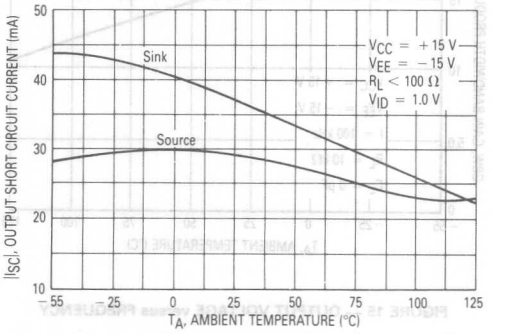


FIGURE 9 — SUPPLY CURRENT versus TEMPERATURE

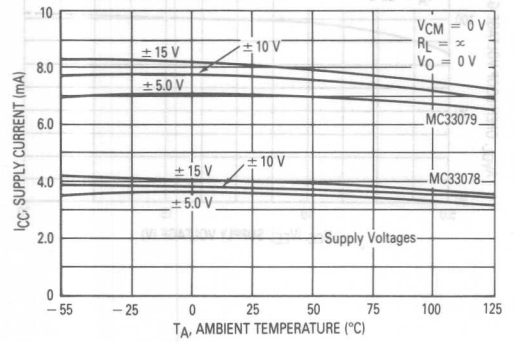
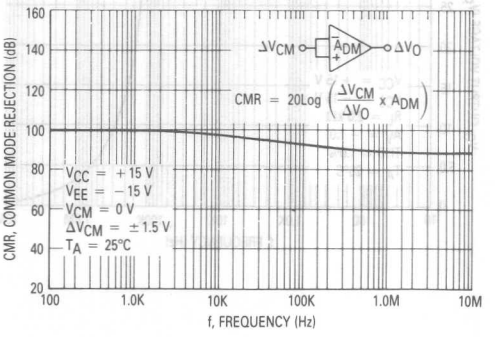


FIGURE 10 — COMMON MODE REJECTION versus FREQUENCY



versus FREQUENCY

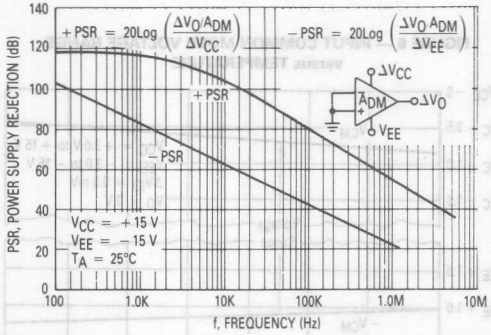


FIGURE 13 — GAIN BANDWIDTH PRODUCT versus TEMPERATURE

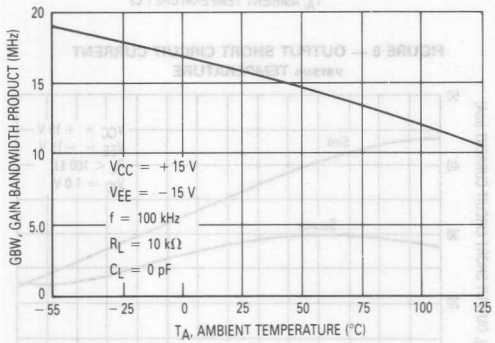
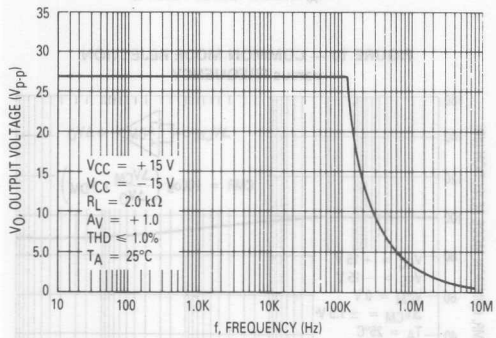


FIGURE 15 — OUTPUT VOLTAGE versus FREQUENCY



SUPPLY VOLTAGE

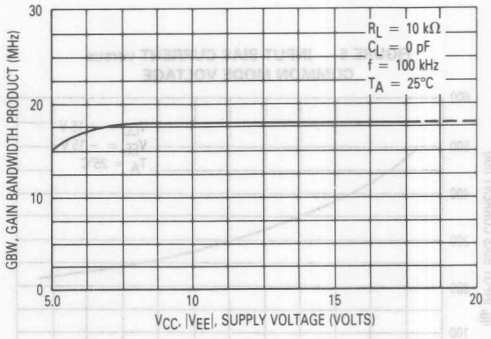


FIGURE 14 — MAXIMUM OUTPUT VOLTAGE versus SUPPLY VOLTAGE

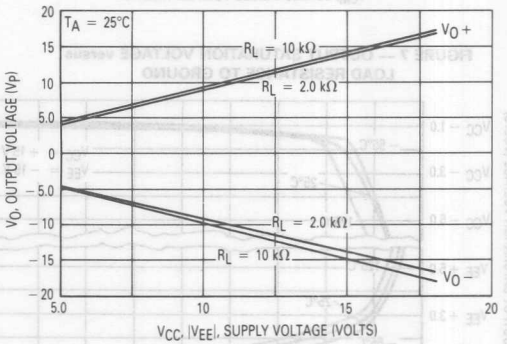
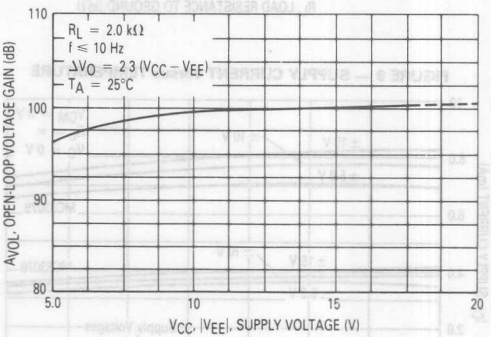


FIGURE 16 — OPEN-LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE



TYPICAL CHARACTERISTICS — continued

FIGURE 17 — OPEN-LOOP VOLTAGE GAIN versus TEMPERATURE

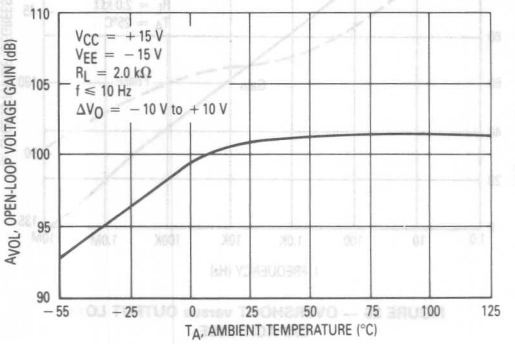


FIGURE 18 — OUTPUT IMPEDANCE versus FREQUENCY

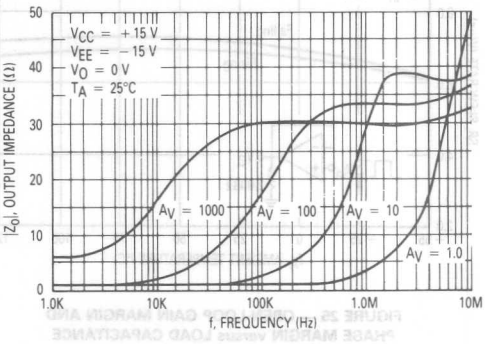


FIGURE 19 — CHANNEL SEPARATION versus FREQUENCY

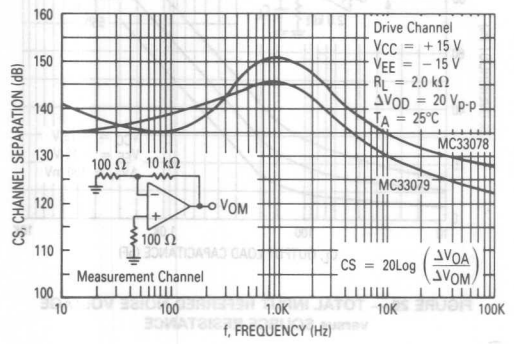


FIGURE 20 — TOTAL HARMONIC DISTORTION versus FREQUENCY

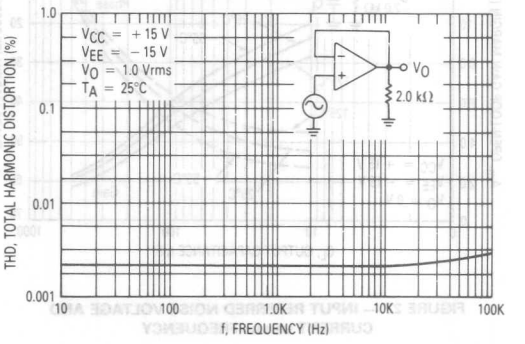


FIGURE 21 — TOTAL HARMONIC DISTORTION versus OUTPUT VOLTAGE

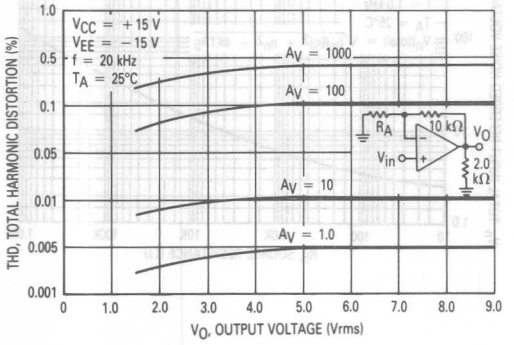
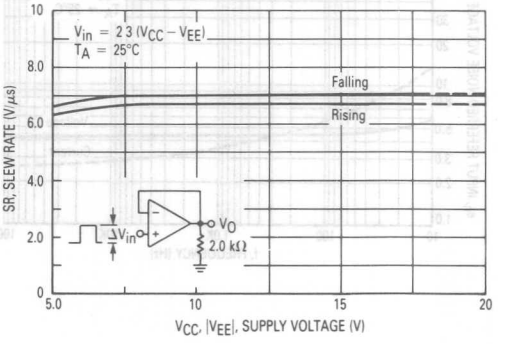


FIGURE 22 — SLEW RATE versus SUPPLY VOLTAGE



2

FIGURE 23 — SLEW RATE versus TEMPERATURE

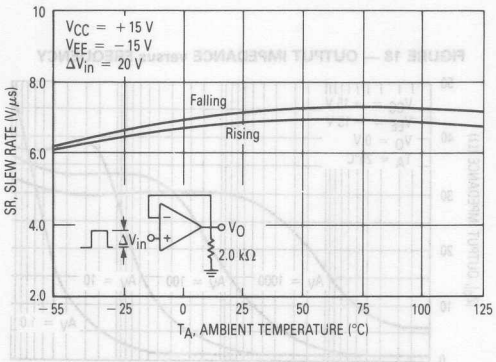


FIGURE 24 — VOLTAGE GAIN AND PHASE versus FREQUENCY

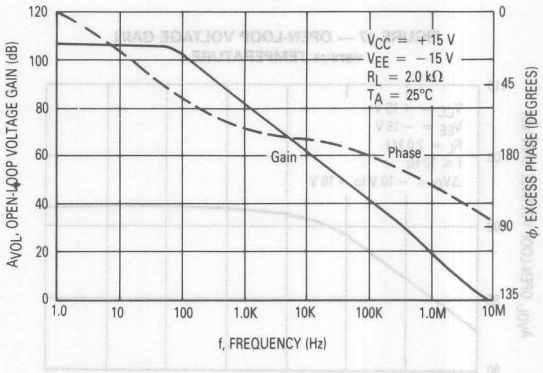


FIGURE 25 — OPEN-LOOP GAIN MARGIN AND PHASE MARGIN versus LOAD CAPACITANCE

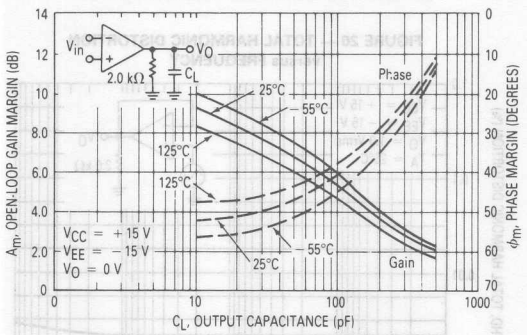


FIGURE 26 — OVERSHOOT versus OUTPUT LOAD CAPACITANCE

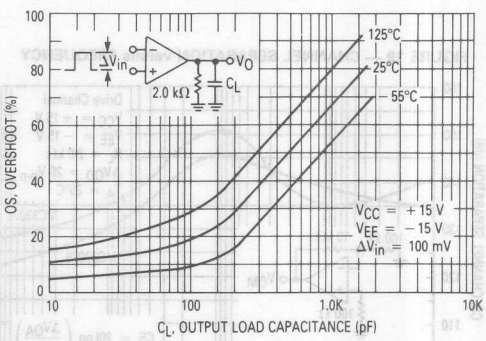


FIGURE 27 — INPUT REFERRED NOISE VOLTAGE AND CURRENT versus FREQUENCY

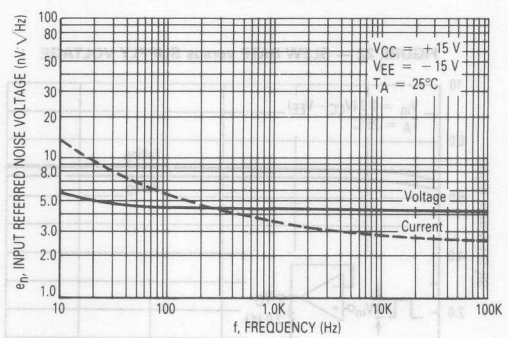
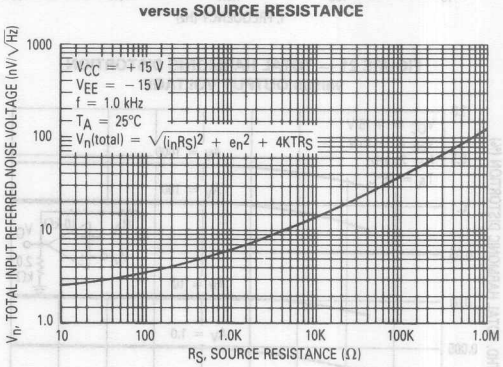


FIGURE 28 — TOTAL INPUT REFERRED NOISE VOLTAGE versus SOURCE RESISTANCE



TYPICAL CHARACTERISTICS — continued

FIGURE 29 — PHASE MARGIN AND GAIN MARGIN versus DIFFERENTIAL SOURCE RESISTANCE

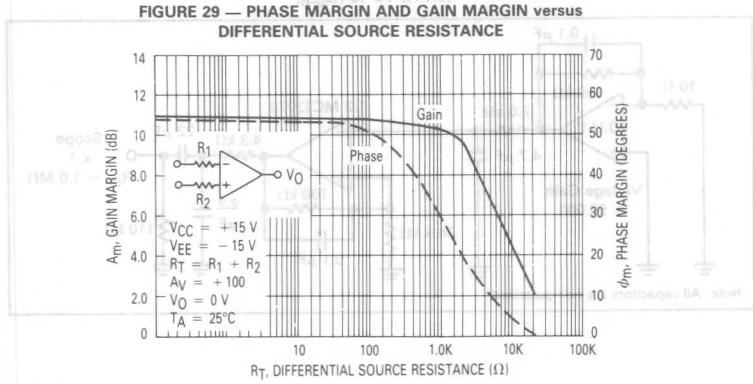


FIGURE 30 — INVERTING AMPLIFIER SLEW RATE

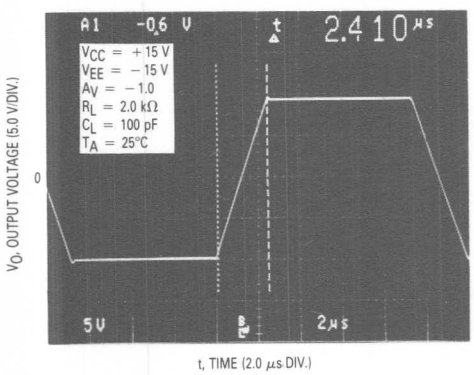


FIGURE 31 — NON-INVERTING AMPLIFIER SLEW RATE

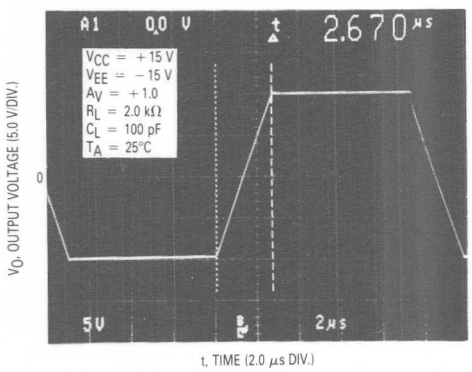


FIGURE 32 — NON-INVERTING AMPLIFIER OVERSHOOT

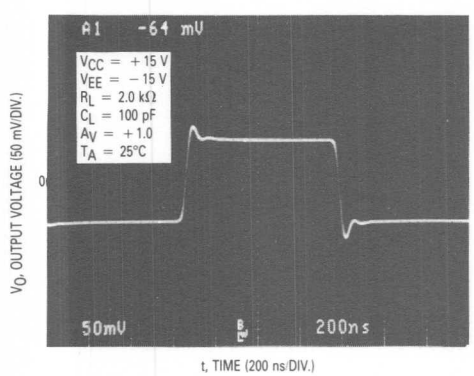


FIGURE 33 — LOW FREQUENCY NOISE VOLTAGE versus TIME

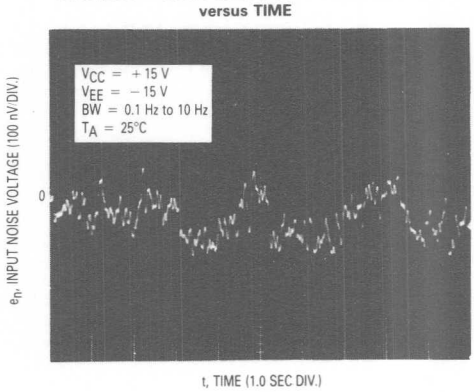
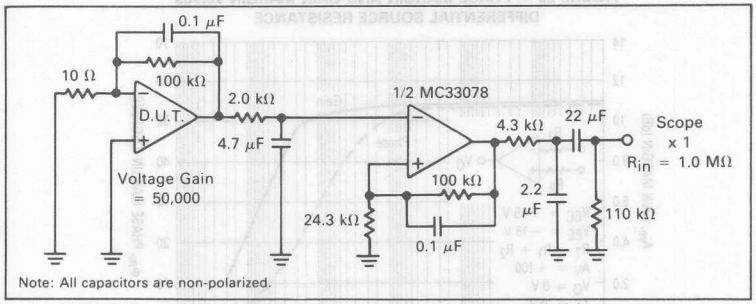


FIGURE 34 — VOLTAGE NOISE TEST CIRCUIT
(0.1 Hz-TO-10 Hz_{p-p})



MOTOROLA

MC33171, MC35171
MC33172, MC35172
MC33174, MC35174

2

LOW POWER, SINGLE SUPPLY OPERATIONAL AMPLIFIERS

Quality bipolar fabrication with innovative design concepts are employed for the MC33171/2/4, MC35171/2/4 series of monolithic operational amplifiers. This series of operational amplifiers operates at 180 μA per amplifier and offers 1.8 MHz of gain bandwidth product and 2.1 V/μs slew rate without the use of JFET device technology. Although this series can be operated from split supplies, it is particularly suited for single supply operation, since the common mode input voltage range includes ground potential (V_{EE}). With a Darlington input stage, this series exhibits high input resistance, low input offset voltage and high gain. The all NPN output stage, characterized by no deadband crossover distortion and large output voltage swing, provides high capacitance drive capability, excellent phase and gain margins, low open-loop high frequency output impedance and symmetrical source/sink AC frequency response.

The MC33171/2/4, MC35171/2/4 series of devices are specified over the industrial/vehicular or military temperature ranges. The complete series of single, dual and quad operational amplifiers are available in the plastic and ceramic DIP as well as the SOIC surface mount packages.

- Low Supply Current: 180 μA (Per Amplifier)
- Wide Supply Operating Range: +3.0 V to +44 V or ±1.5 V to ±22 V
- Wide Input Common Mode Range Including Ground (V_{EE})
- Wide Bandwidth: 1.8 MHz
- High Slew Rate: 2.1 V/μs
- Low Input Offset Voltage: 2.0 mV
- Large Output Voltage Swing: −14.2 V to +14.2 V (with +/−15 V Supplies)
- Large Capacitance Drive Capability: 0 to 500 pF
- Low Total Harmonic Distortion: 0.03%
- Excellent Phase Margin: 60°
- Excellent Gain Margin: 15 dB
- Output Short Circuit Protection

ORDERING INFORMATION

Op Amp Function	Device	Temperature Range	Package
Single	MC33171D	−40 to +85°C	SO-8 Plastic DIP
	MC35171U	−55 to +125°C	Ceramic DIP
	MC33171P	−40 to +85°C	Plastic DIP
Dual	MC33172D	−40 to +85°C	SO-8 Plastic DIP
	MC35172U	−55 to +125°C	Ceramic DIP
	MC33172P	−40 to +85°C	Plastic DIP
Quad	MC33174D	−40 to +85°C	SO-14 Plastic DIP
	MC35174L	−55 to +125°C	Ceramic DIP
	MC33174P	−40 to +85°C	Plastic DIP

LOW POWER, SINGLE SUPPLY OPERATIONAL AMPLIFIERS



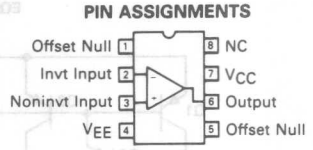
P SUFFIX
PLASTIC PACKAGE
CASE 626-05

U SUFFIX
CERAMIC PACKAGE
CASE 693-02

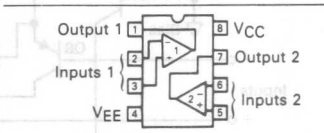


D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SO-8

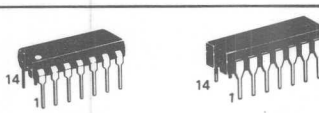
PIN ASSIGNMENTS



Single, Top View



Dual, Top View



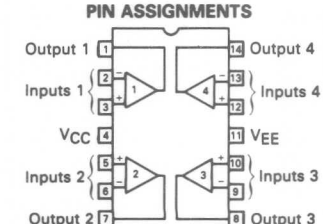
P SUFFIX
PLASTIC PACKAGE
CASE 646-06

L SUFFIX
CERAMIC PACKAGE
CASE 632-08



D SUFFIX
PLASTIC PACKAGE
CASE 751A-02
SO-14

PIN ASSIGNMENTS



Quad, Top View

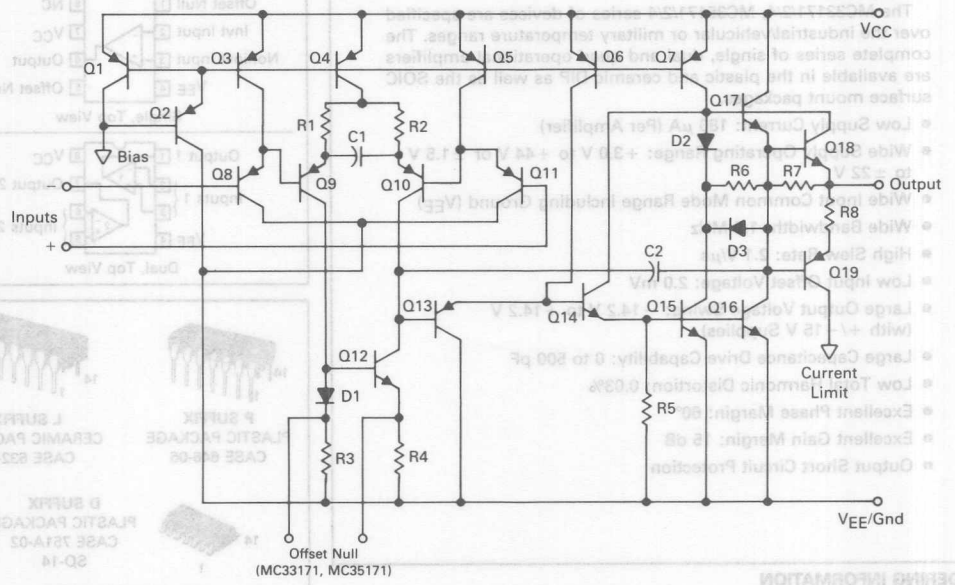
2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}/V_{EE}	±22	Volts
Input Differential Voltage Range	V_{IDR}	(Note 1)	Volts
Input Voltage Range	V_{IR}	(Note 1)	Volts
Output Short Circuit Duration (Note 2)	t_S	Indefinite	Seconds
Operating Ambient Temperature Range MC35171/MC35172/MC35174 MC33171/MC33172/MC33174	T_A	 −55 to +125 −40 to +85	°C
Operating Junction Temperature	T_J	+150	°C
Storage Temperature Range Ceramic Package Plastic Package	T_{stg}	 −65 to +150 −55 to +125	°C

Notes: 1. Either or both input voltages must not exceed the magnitude of V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded.

EQUIVALENT CIRCUIT SCHEMATIC (EACH AMPLIFIER)

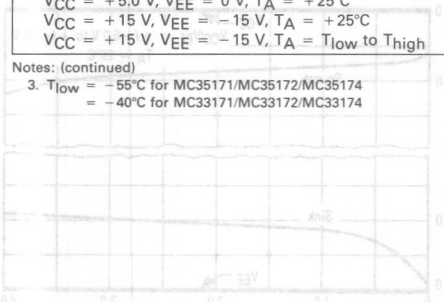


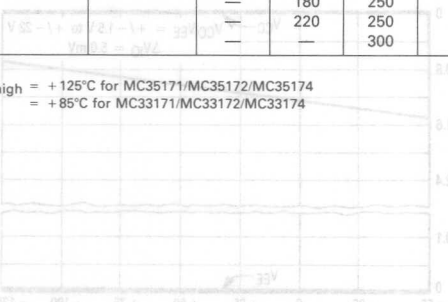
DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, R_L connected to ground, T_A = T_{low} to T_{high} [Note 3] unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (V_{CM} = 0 V)	V_{IO}				mV
V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25°C		—	2.0	4.5	
V_{CC} = +5 V, V_{EE} = 0 V, T_A = +25°C		—	2.5	5.0	
V_{CC} = +15 V, V_{EE} = −15 V, T_A = T_{low} to T_{high}		—	—	6.5	
Average Temperature Coefficient of Offset Voltage	$\Delta V_{IO}/\Delta T$	—	10	—	μV/°C
Input Bias Current (V_{CM} = 0 V)	I_{IB}				nA
T_A = +25°C		—	20	100	
T_A = T_{low} to T_{high}		—	—	200	
Input Offset Current (V_{CM} = 0 V)	I_{IO}				nA
T_A = +25°C		—	5.0	20	
T_A = T_{low} to T_{high}		—	—	40	
Large Signal Voltage Gain (V_O = ±10 V, R_L = 10 k)	A_{VOL}				V/mV
T_A = +25°C		50	500	—	
T_A = T_{low} to T_{high}		25	—	—	
Output Voltage Swing	V_{OH}				V
V_{CC} = +5.0 V, V_{EE} = 0 V, R_L = 10 k, T_A = +25°C		3.5	4.3	—	
V_{CC} = +15 V, V_{EE} = −15 V, R_L = 10 k, T_A = +25°C		13.6	14.2	—	
V_{CC} = +15 V, V_{EE} = −15 V, R_L = 10 k, T_A = T_{low} to T_{high}		13.3	—	—	
V_{CC} = +5.0 V, V_{EE} = 0 V, R_L = 10 k, T_A = +25°C	V_{OL}	—	0.05	0.15	
V_{CC} = +15 V, V_{EE} = −15 V, R_L = 10 k, T_A = +25°C		—	−14.2	−13.6	
V_{CC} = +15 V, V_{EE} = −15 V, R_L = 10 k, T_A = T_{low} to T_{high}		—	—	−13.3	
Output Short Circuit Current (T_A = +25°C)	I_{SC}				mA
Input Overdrive = 1.0 V, Output to Ground					
Source		3.0	5.0	—	
Sink		15	27	—	
Input Common Mode Voltage Range	V_{ICR}				V
T_A = +25°C		V_{EE} to (V_{CC} − 1.8)			
T_A = T_{low} to T_{high}		V_{EE} to (V_{CC} − 2.2)			
Common Mode Rejection Ratio (R_S ≤ 10 k)	CMRR	80	90	—	dB
Power Supply Rejection Ratio (R_S = 100 Ω)	PSRR	80	100	—	dB
Power Supply Current (Per Amplifier)	I_D				μA
V_{CC} = +5.0 V, V_{EE} = 0 V, T_A = +25°C		—	180	250	
V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25°C		—	220	250	
V_{CC} = +15 V, V_{EE} = −15 V, T_A = T_{low} to T_{high}		—	—	300	

Notes: (continued)

3. T_{low} = −55°C for MC35171/MC35172/MC35174
   = −40°C for MC33171/MC33172/MC33174
   T_{high} = +125°C for MC35171/MC35172/MC35174
   = +85°C for MC33171/MC33172/MC33174





AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, R_L connected to ground, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = −10 V to +10 V, R_L = 10 k, C_L = 100 pF) A_V + 1 A_V − 1	SR	 1.6 —	 2.1 2.1	 — —	V/μs
Gain Bandwidth Product (f = 100 kHz)	GBW	1.4	1.8	—	MHz
Power Bandwidth A_V = +1.0, R_L = 10 k, V_O = 20 V_{p-p}, THD = 5%	BWp	—	35	—	kHz
Phase Margin R_L = 10 k R_L = 10 k, C_L = 100 pF	ϕm	 — —	 60 45	 — 	Degrees
Gain Margin R_L = 10 k R_L = 10 k, C_L = 100 pF	A_m	 — —	 15 5.0	 — —	dB
Equivalent Input Noise Voltage R_S = 100 Ω, f = 1.0 kHz	e_n	—	32	—	nV/√Hz
Equivalent Input Noise Current (f = 1.0 kHz)	I_n	—	0.2	—	pA/√Hz
Differential Input Resistance V_{CM} = 0 V	R_{IN}	—	300	—	MΩ
Input Capacitance	C_i	—	0.8	—	pF
Total Harmonic Distortion A_V = +10, R_L = 10 k, 2.0 $V_{p-p} \leq V_O \leq$ 20 V_{p-p}, f = 10 kHz	THD	—	0.03	—	%
Channel Separation (f = 10 kHz)	—	—	120	—	dB
Open-Loop Output Impedance (f = 1.0 MHz)	z_o	—	100	—	Ω

TYPICAL PERFORMANCE CURVES

FIGURE 1 — INPUT COMMON-MODE VOLTAGE RANGE versus TEMPERATURE

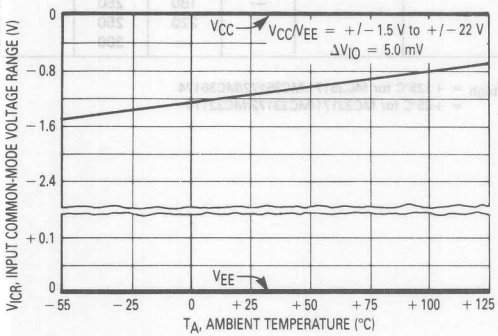


FIGURE 2 — SPLIT SUPPLY OUTPUT SATURATION versus LOAD CURRENT

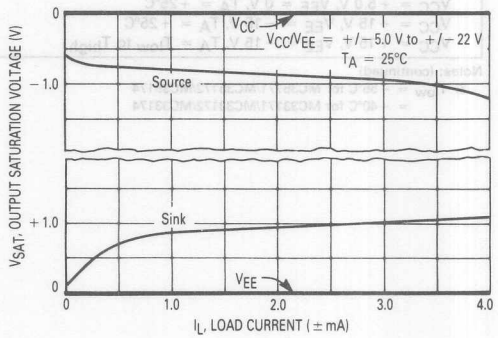


FIGURE 3 — OPEN-LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY

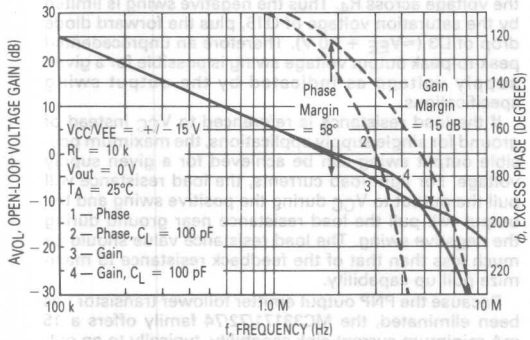


FIGURE 4 — PHASE MARGIN AND PERCENT OVERSHOOT versus LOAD CAPACITANCE

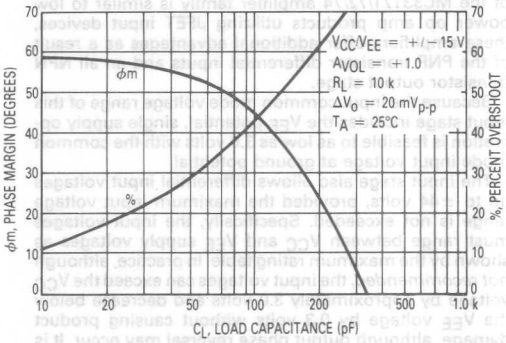


FIGURE 5 — NORMALIZED GAIN BANDWIDTH PRODUCT AND SLEW RATE versus TEMPERATURE

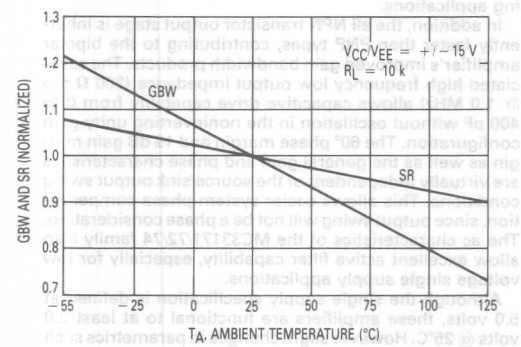


FIGURE 6 — SMALL AND LARGE SIGNAL TRANSIENT RESPONSE

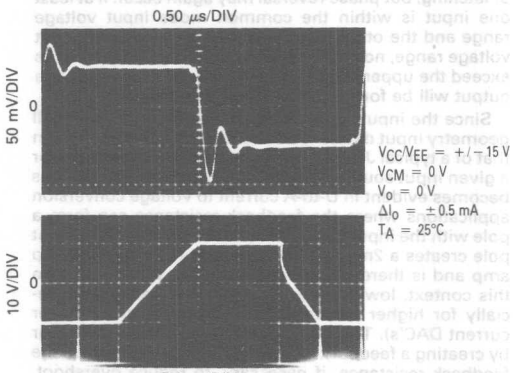


FIGURE 7 — OUTPUT IMPEDANCE versus FREQUENCY

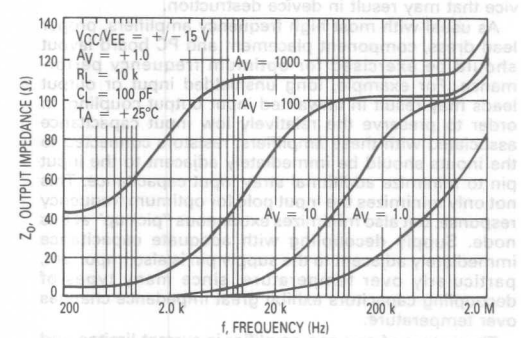
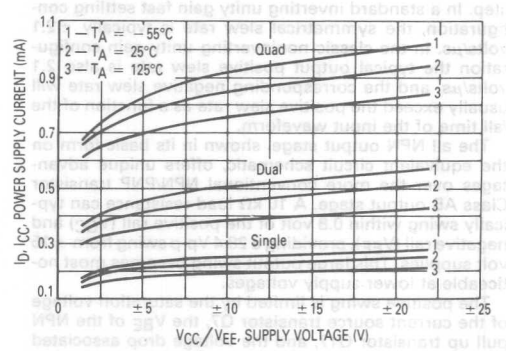


FIGURE 8 — SUPPLY CURRENT versus SUPPLY VOLTAGE



APPLICATIONS INFORMATION

CIRCUIT DESCRIPTION/PERFORMANCE FEATURES

Although the bandwidth, slew rate, and settling time of the MC33171/72/74 amplifier family is similar to low power op amp products utilizing JFET input devices, these amplifiers offer additional advantages as a result of the PNP transistor differential inputs and an all NPN transistor output stage.

Because the input common mode voltage range of this input stage includes the V_{EE} potential, single supply operation is feasible to as low as 3.0 volts with the common mode input voltage at ground potential.

The input stage also allows differential input voltages up to ±44 volts, provided the maximum input voltage range is not exceeded. Specifically, the input voltages must range between V_{CC} and V_{EE} supply voltages as shown by the maximum rating table. In practice, although *not recommended,* the input voltages can exceed the V_{CC} voltage by approximately 3.0 volts and decrease below the V_{EE} voltage by 0.3 volts without causing product damage, although output phase reversal may occur. It is also possible to source up to 5.0 mA of current from V_{EE} through either input's clamping diode without damage or latching, but phase reversal may again occur. If at least one input is within the common mode input voltage range and the other input is within the maximum input voltage range, no phase reversal will occur. If both inputs exceed the upper common mode input voltage limit, the output will be forced to its lowest voltage state.

Since the input capacitance associated with the small geometry input device is substantially lower (0.8 pF) than that of a typical JFET (3.0 pF), the frequency response for a given input source resistance is greatly enhanced. This becomes evident in D-to-A current to voltage conversion applications where the feedback resistance can form a pole with the input capacitance of the op amp. This input pole creates a 2nd order system with the single pole op amp and is therefore detrimental to its settling time. In this context, lower input capacitance is desirable especially for higher values of feedback resistances (lower current DAC's). This input pole can be compensated for by creating a feedback zero with a capacitance across the feedback resistance, if necessary, to reduce overshoot. For 10 kΩ of feedback resistance, the MC33171/72/74 family can typically settle to within 1/2 LSB of 8 bits in 4.2 μs, and within 1/2 LSB of 12 bits in 4.8 μs for a 10 volt step. In a standard inverting unity gain fast settling configuration, the symmetrical slew rate is typically ±2.1 volts/μs. In the classic noninverting unity gain configuration the typical output positive slew rate is also 2.1 volts/μs, and the corresponding negative slew rate will usually exceed the positive slew rate as a function of the fall time of the input waveform.

The all NPN output stage, shown in its basic form on the equivalent circuit schematic, offers unique advantages over the more conventional NPN/PNP transistor Class AB output stage. A 10 kΩ load resistance can typically swing within 0.8 volt of the positive rail (V_{CC}) and negative rail (V_{EE}), providing a 28.4 Vp-p swing from ±15 volt supplies. This large output swing becomes most noticeable at lower supply voltages.

The positive swing is limited by the saturation voltage of the current source transistor Q7, the V_{BE} of the NPN pull up transistor Q17, and the voltage drop associated with the short circuit resistance, R_5. For sink currents less than 0.4 mA, the negative swing is limited by the saturation voltage of the pull-down transistor Q15, and the voltage drop across R_4 and R_5. For small valued sink currents, the above voltage drops are negligible, allowing the negative swing voltage to approach within millivolts of V_{EE}. For sink currents (> 0.4 mA), diode D3 clamps the voltage across R_4. Thus the negative swing is limited by the saturation voltage of Q15, plus the forward diode drop of D3 ($\approx V_{EE}$ + 1.0 V). Therefore an unprecedented peak-to-peak output voltage swing is possible for a given supply voltage as indicated by the output swing specifications.

If the load resistance is referenced to V_{CC} instead of ground for single supply applications, the maximum possible output swing can be achieved for a given supply voltage. For light load currents, the load resistance will pull the output to V_{CC} during the positive swing and the output will pull the load resistance near ground during the negative swing. The load resistance value should be much less than that of the feedback resistance to maximize pull up capability.

Because the PNP output emitter follower transistor has been eliminated, the MC33171/72/74 family offers a 15 mA minimum current sink capability, typically to an output voltge of (V_{EE} + 1.8 V). In single supply applications the output can directly source or sink base current from a common emitter NPN transistor for high current switching applications.

In addition, the all NPN transistor output stage is inherently faster than PNP types, contributing to the bipolar amplifier's improved gain bandwidth products. The associated high frequency low output impedance (200 Ω typ @ 1.0 MHz) allows capacitive drive capability from 0 to 400 pF without oscillation in the noninverting unity gain configuration. The 60° phase margin and 15 dB gain margin as well as the general gain and phase characteristics are virtually independent of the source/sink output swing conditions. This allows easier system phase compensation, since output swing will not be a phase consideration. The ac characteristics of the MC33171/72/74 family also allow excellent active filter capability, especially for low voltage single supply applications.

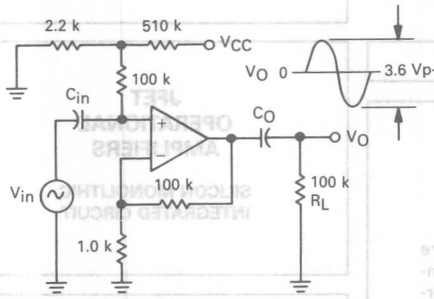
Although the single supply specification is defined at 5.0 volts, these amplifiers are functional to at least 3.0 volts @ 25°C. However slight changes in parametrics such as bandwidth, slew rate, and dc gain may occur.

If power to this integrated circuit is applied in reverse polarity or if the IC is installed backwards in a socket, large unlimited current surges will occur through the device that may result in device destruction.

As usual with most high frequency amplifiers, proper lead dress, component placement and PC board layout should be exercised for optimum frequency performance. For example, long unshielded input or output leads may result in unwanted input output coupling. In order to preserve the relatively low input capacitance associated with these amplifiers, resistors connected to the inputs should be immediately adjacent to the input pin to minimize additional stray input capacitance. This not only minimizes the input pole for optimum frequency response, but also minimizes extraneous "pick up" at this node. Supply decoupling with adequate capacitance immediately adjacent to the supply pin is also important, particularly over temperature, since many types of decoupling capacitors exhibit great impedance changes over temperature.

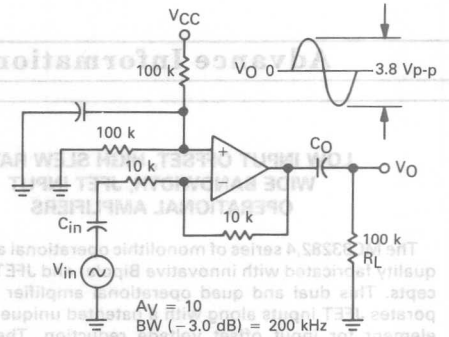
The output of any one amplifier is current limited and thus protected from a direct short to ground. However, under such conditions, it is important not to allow the device to exceed the maximum junction temperature rating. Typically for ±15 volt supplies, any one output can be shorted continuously to ground without exceeding the maximum temperature rating.

FIGURE 9 — AC COUPLED NONINVERTING AMPLIFIER WITH SINGLE +5.0 V SUPPLY



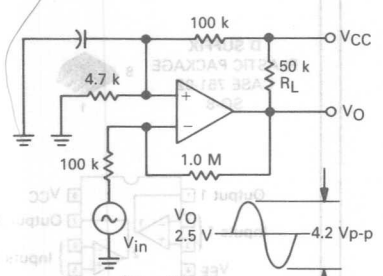
AV = 101
BW (−3.0 dB) = 20 kHz

FIGURE 10 — AC COUPLED INVERTING AMPLIFIER WITH SINGLE +5.0 V SUPPLY



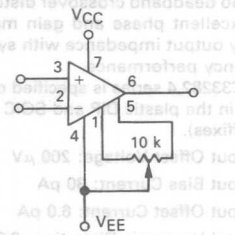
AV = 10
BW (−3.0 dB) = 200 kHz

FIGURE 11 — DC COUPLED INVERTING AMPLIFIER MAXIMUM OUTPUT SWING WITH SINGLE +5.0 V SUPPLY



AV = 10
BW (−3.0 dB) = 200 kHz

FIGURE 12 — OFFSET NULLING CIRCUIT



Offset Nulling range is approximately ±80 mV with a 10 k potentiometer, MC33171/MC35171 only.

FIGURE 13 — ACTIVE HIGH-Q NOTCH FILTER

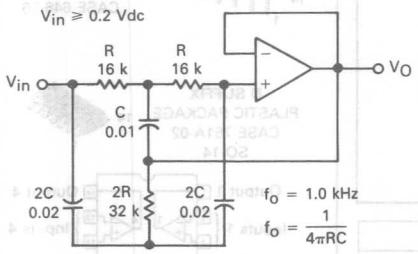
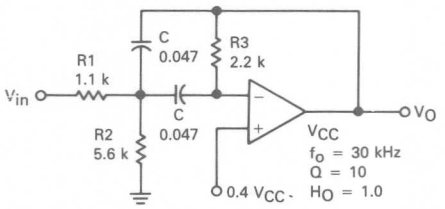


FIGURE 14 — ACTIVE BANDPASS FILTER



Given f_O = Center Frequency
A_O = Gain at Center Frequency
Choose Value f_o, Q, A_o, C
Then

$R1 = \frac{R3}{2\,H_o}$ $R2 = \frac{R1\,R3}{4Q^2\,R1 - R3}$

$R3 = \frac{Q}{\pi f_o C}$ $\frac{Q_o\,f_o}{GBW} < 0.1$

For less than 10% error from operational amplifier
Where f_o and GBW are expressed in Hz.

Advance Information

LOW INPUT OFFSET, HIGH SLEW RATE, WIDE BANDWIDTH, JFET INPUT OPERATIONAL AMPLIFIERS

The MC33282,4 series of monolithic operational amplifiers are quality fabricated with innovative Bipolar and JFET design concepts. This dual and quad operational amplifier series incorporates JFET inputs along with a patented unique resistor trim element for input offset voltage reduction. The MC33282,4 series of operational amplifiers exhibits low input offset voltage, low input bias current, high gain bandwidth and high slew rate. Dual-doublet frequency compensation is incorporated to produce high quality phase/gain performance. In addition, the MC33282,4 series exhibits moderately low input noise characteristics for JFET input amplifiers. It's all NPN output stage exhibits no deadband crossover distortion, large output voltage swing, excellent phase and gain margin, low open-loop high frequency output impedance with symmetrical source and sink ac frequency performance.

The MC33282,4 series is specified over −40°C to +85°C and is available in the plastic DIP and SOIC surface mount packages (P and D suffixes).

- Low Input Offset Voltage: 200 μV
- Low Input Bias Current: 30 pA
- Low Input Offset Current: 6.0 pA
- Low Total Harmonic Distortion: 0.003%
- Low Noise: 18 nV/$\sqrt{\text{Hz}}$ @ 1.0 kHz
- High Gain Bandwidth Product: 30 MHz @ 100 kHz
- High Slew Rate: 12 V/μs
- Excellent Frequency Stability
- Large Output Voltage Swing: +14.1 V/−14.6 V
- Dual Supply Operation: ±18 V (Max)

JFET OPERATIONAL AMPLIFIERS

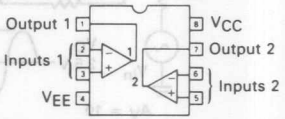
SILICON MONOLITHIC INTEGRATED CIRCUIT



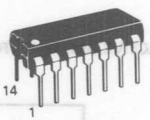
P SUFFIX
PLASTIC PACKAGE
CASE 626-05

D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SO-8





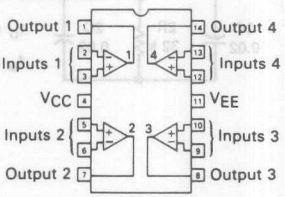
(Dual, Top View)



P SUFFIX
PLASTIC PACKAGE
CASE 646-06

D SUFFIX
PLASTIC PACKAGE
CASE 751A-02
SO-14





(Quad, Top View)

ORDERING INFORMATION

Op Amp Function	Device	Ambient Test Temperature Range	Package
Dual	MC33282D MC33282P	−40°C to +85°C	SO-8 Plastic DIP
Quad	MC33284D MC33284P	−40°C to +85°C	SO-14 Plastic DIP

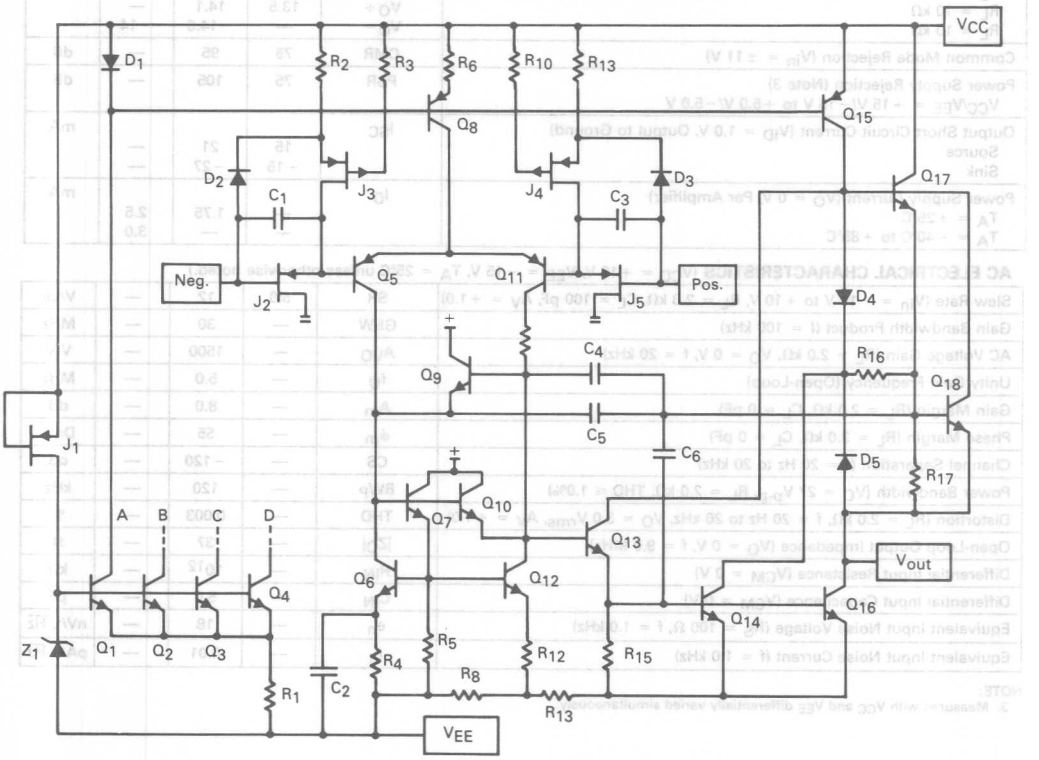
This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	+36	Volts
Input Differential Voltage Range	V_{IDR}	(Note 1)	Volts
Input Voltage Range	V_{IR}	(Note 1)	Volts
Output Short Circuit Duration (Note 2)	t_S	Indefinite	Seconds
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	−60 to +150	°C
Maximum Power Dissipation	P_D	(Note 2)	mW

NOTES:
1. Either or both input voltages should not exceed V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded.

EQUIVALENT CIRCUIT SCHEMATIC (EACH AMPLIFIER)



2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V)	$\|V_{IO}\|$				mV
T_A = +25°C		—	0.2	2.0	
T_A = −40°C to +85°C		—	—	4.0	
Average Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	—	5.0	—	μV/°C
R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V, T_A = T_{low} to T_{high}					
Input Bias Current (V_{CM} = 0 V, V_O = 0 V)	I_{IB}				
T_A = +25°C		—	30	100	pA
T_A = −40°C to +85°C		—	—	4.0	nA
Input Offset Current (V_{CM} = 0 V, V_O = 0 V)	I_{IO}				
T_A = +25°C		—	6.0	50	pA
T_A = −40°C to +85°C		—	—	2.0	nA
Common Mode Input Voltage Range (ΔV_{IO} = 5.0 mV, V_O = 0 V)	V_{ICR}	−11	−12	—	V
		—	14	11	
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 kΩ)	A_{VOL}				V/mV
T_A = +25°C		50	200	—	
T_A = −40°C to +85°C		25	—	—	
Output Voltage Swing (V_{ID} = ±1.0 V)					V
R_L = 2.0 kΩ	V_O+	13.2	13.7	—	
R_L = 2.0 kΩ	V_O-	—	−13.9	−13.2	
R_L = 10 kΩ	V_O+	13.5	14.1	—	
R_L = 10 kΩ	V_O-	—	−14.6	−14	
Common Mode Rejection (V_{in} = ±11 V)	CMR	75	95	—	dB
Power Supply Rejection (Note 3)	PSR	75	105	—	dB
V_{CC}/V_{EE} = +15 V/−15 V to +5.0 V/−5.0 V					
Output Short Circuit Current (V_{ID} = 1.0 V, Output to Ground)	I_{SC}				mA
Source		15	21	—	
Sink		−15	−27	—	
Power Supply Current (V_O = 0 V, Per Amplifier)	I_D				mA
T_A = +25°C		—	1.75	2.5	
T_A = −40°C to +85°C		—	—	3.0	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C unless otherwise noted.)

Slew Rate (V_{in} = −10 V to +10 V, R_L = 2.0 kΩ, C_L = 100 pF, A_V = +1.0)	SR	8.0	12	—	V/μs
Gain Bandwidth Product (f = 100 kHz)	GBW	—	30	—	MHz
AC Voltage Gain (R_L = 2.0 kΩ, V_O = 0 V, f = 20 kHz)	A_{VO}	—	1500	—	V/V
Unity Gain Frequency (Open-Loop)	f_U	—	5.0	—	MHz
Gain Margin (R_L = 2.0 kΩ, C_L = 0 pF)	A_m	—	8.0	—	dB
Phase Margin (R_L = 2.0 kΩ, C_L = 0 pF)	ϕ_m	—	55	—	Deg.
Channel Separation (f = 20 Hz to 20 kHz)	CS	—	−120	—	dB
Power Bandwidth (V_O = 27 V_{p-p}, R_L = 2.0 kΩ, THD ≤ 1.0%)	BW_P	—	120	—	kHz
Distortion (R_L = 2.0 kΩ, f = 20 Hz to 20 kHz, V_O = 3.0 V_{rms}, A_V = +1.0)	THD	—	0.003	—	%
Open-Loop Output Impedance (V_O = 0 V, f = 9.0 MHz)	$\|Z_O\|$	—	37	—	Ω
Differential Input Resistance (V_{CM} = 0 V)	R_{IN}	—	10^{12}	—	kΩ
Differential Input Capacitance (V_{CM} = 0 V)	C_{IN}	—	5.0	—	pF
Equivalent Input Noise Voltage (R_S = 100 Ω, f = 1.0 kHz)	e_n	—	18	—	$nV/\sqrt{Hz}$
Equivalent Input Noise Current (f = 1.0 kHz)	i_n	—	0.01	—	$pA/\sqrt{Hz}$

NOTE:
3. Measured with V_{CC} and V_{EE} differentially varied simultaneously.

MOTOROLA

MC34001, MC35001
MC34002, MC35002
MC34004, MC35004

2

JFET INPUT OPERATIONAL AMPLIFIERS

These low cost JFET Input operational amplifiers combine two state-of-the-art linear technologies on a single monolithic integrated circuit. Each internally compensated operational amplifier has well matched high voltage JFET input devices for low input offset voltage. The BIFET technology provides wide bandwidths and fast slew rates with low input bias currents, input offset currents, and supply currents.

The Motorola BIFET family offers single, dual and quad operational amplifiers which are pin-compatible with the industry standard MC1741, MC1458, and the MC3403/LM324 bipolar devices. The MC35001/35002/35004 series are specified over the military operating temperature range of −55°C to +125°C and the MC34001/34002/34004 series are specified from 0°C to +70°C.

- Input Offset Voltage Options of 2.0, 5.0, and 10 mV Maximum
- Low Input Bias Current — 40 pA
- Low Input Offset Current — 10 pA
- Wide Gain Bandwidth — 4.0 MHz
- High Slew Rate — 13 V/μs
- Low Supply Current — 1.8 mA per Amplifier
- High Input Impedance — 10^{12} Ω
- High Common-Mode and Supply Voltage Rejection Ratios — 100 dB
- Industry Standard Pinouts

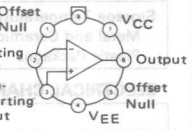
JFET INPUT OPERATIONAL AMPLIFIERS

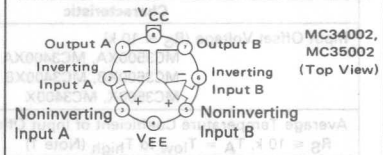
SILICON MONOLITHIC INTEGRATED CIRCUITS

G SUFFIX
METAL PACKAGE
CASE 601-04

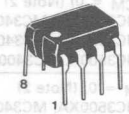


MC34001, MC35001
(Top View)

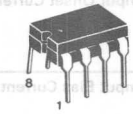




MC34002, MC35002
(Top View)



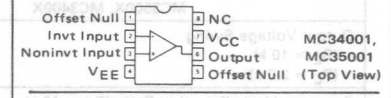
P SUFFIX
PLASTIC PACKAGE
CASE 626-05



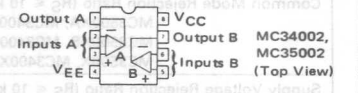
U SUFFIX
CERAMIC PACKAGE
CASE 693-02



D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SO-8



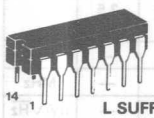
MC34001, MC35001
(Top View)



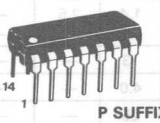
MC34002, MC35002
(Top View)

ORDERING INFORMATION

Op Amp Function	Device	Temperature Range	Package
Single	MC34001AD, BD, D	0 to +70	SO-8
	MC34001AG, BG, G		Metal Can
	MC34001AP, BP, P		Plastic DIP
	MC34001AU, BU, U		Ceramic DIP
	MC35001AG, BG, G	−55 to +125°C	Metal Can
	MC35001AU, BU, U		Ceramic DIP
Dual	MC34002AD, BD, D	0 to +70°C	SO-8
	MC34002AG, BG, G		Metal Can
	MC34002AP, BP, P		Plastic DIP
	MC34002AU, BU, U		Ceramic DIP
	MC35002AG, BG, G	−55 to +125°C	Metal Can
	MC35002AU, BU, U		Ceramic DIP
Quad	MC34004BD, D	0 to +70°C	SO-14
	MC34004BL, L		Ceramic DIP
	MC34004BP, P		Plastic DIP
	MC35004BL, L	−55 to +125°C	Ceramic DIP



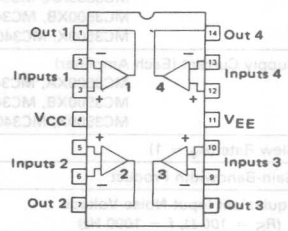
L SUFFIX
CERAMIC PACKAGE
CASE 632-08



P SUFFIX
PLASTIC PACKAGE
CASE 646-06



D SUFFIX
PLASTIC PACKAGE
CASE 751A-02
SO-14



MC34004, MC35004 (Top View)

Rating	Symbol	MC35001 MC35002 MC35004	MC34001 MC34002 MC34004	Unit
Supply Voltage	V_{CC} V_{EE}	+22 −22	+18 −18	V
Differential Input Voltage	V_{ID}	±40	±30	V
Input Voltage Range	V_{IDR}	±20	±16	V
Output Short-Circuit Duration	t_S	Continuous		
Operating Ambient Temperature Range	T_A	−55 to +125	0 to +70	°C
Operating Junction Temperature Metal and Ceramic Packages Plastic Packages	T_J	 150 —	 115 115	°C
Storage Temperature Range Metal and Ceramic Packages Plastic Packages	T_{stg}	 −65 to +150 —	 −65 to +150 −55 to +125	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25° unless otherwise noted).

Characteristic	Symbol	MC35001/35002/35004			MC34001/34002/34004			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10$ k) MC3500XA, MC3400XA MC3500XB, MC3400XB MC3500X, MC3400X	V_{IO}	 — — —	 1.0 3.0 5.0	 2.0 5.0 10	 — — —	 1.0 3.0 5.0	 2.0 5.0 10	mV
Average Temperature Coefficient of Input Offset Voltage $R_S \leq 10$ k, $T_A = T_{low}$ to T_{high} (Note 1)	$\Delta V_{IO}/\Delta T$	—	10	—	—	10	—	μV/°C
Input Offset Current (V_{CM} = 0) (Note 2) MC3500XA, MC3400XA MC3500XB, MC3400XB MC3500X, MC3400X	I_{IO}	 — — —	 10 10 25	 25 50 100	 — — —	 25 25 25	 50 100 100	pA
Input Bias Current (V_{CM} = 0) (Note 2) MC3500XA, MC3400XA MC3500XB, MC3400XB MC3500X, MC3400X	I_{IB}	 — — —	 40 40 50	 75 100 200	 — — —	 50 50 50	 100 200 200	pA
Input Resistance	r_i	—	10^{12}	—	—	10^{12}	—	Ω
Common Mode Input Voltage Range	V_{ICR}	±11	+15 −12	—	±11	+15 −12	—	V
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 k) MC3500XA, MC3400XA MC3500XB, MC3400XB MC3500X, MC3400X	A_{VOL}	 50 50 25	 150 150 100	 — — —	 50 50 25	 150 150 100	 — — —	V/mV
Output Voltage Swing ($R_L \geq 10$ k) ($R_L \geq 2.0$ k)	V_O	 ±12 ±10	 ±14 ±13	 — —	 ±12 ±10	 ±14 ±13	 — —	V
Common Mode Rejection Ratio ($R_S \leq 10$ k) MC3500XA, MC3400XA MC3500XB, MC3400XB MC3500X, MC3400X	CMRR	 80 80 —	 100 100 —	 — — —	 80 80 70	 100 100 100	 — — —	dB
Supply Voltage Rejection Ratio ($R_S \leq 10$ k) (Note 3) MC3500XA, MC3400XA MC3500XB, MC3400XB MC3500X, MC3400X	PSRR	 80 80 70	 100 100 100	 — — —	 80 80 70	 100 100 100	 — — —	dB
Supply Current (Each Amplifier) MC3500XA, MC3400XA MC3500XB, MC3400XB MC3500X, MC3400X	I_D	 — — —	 1.4 1.4 1.4	 2.5 2.5 2.7	 — — —	 1.4 1.4 1.4	 2.5 2.5 2.7	mA
Slew Rate (A_V = 1)	SR	—	13	—	—	13	—	V/μs
Gain-Bandwidth Product	GBW	—	4.0	—	—	4.0	—	MHz
Equivalent Input Noise Voltage (R_S = 100 Ω, f = 1000 Hz)	e_n	—	25	—	—	25	—	nV/√Hz
Equivalent Input Noise Current (f = 1000 Hz)	i_n	—	0.01	—	—	0.01	—	pA/√Hz

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = T_{low} to T_{high} [Note 1]).

Characteristic	Symbol	MC35001/35002/35004 Min	Typ	Max	MC34001/34002/34004 Min	Typ	Max	Unit
Input Offset Voltage ($R_S \leq 10$ k)	V_{IO}							mV
MC3500XA, MC3400XA		—	—	4.0	—	—	4.0	
MC3500XB, MC3400XB		—	—	7.0	—	—	7.0	
MC3500X, MC3400X		—	—	14	—	—	13	
Input Offset Current (V_{CM} = 0) (Note 2)	I_{IO}							nA
MC3500XA, MC3400XA		—	—	20	—	—	2.0	
MC3500XB, MC3400XB		—	—	40	—	—	4.0	
MC3500X, MC3400X		—	—	40	—	—	4.0	
Input Bias Current (V_{CM} = 0) (Note 2)	I_{IB}							nA
MC3500XA, MC3400XA		—	—	50	—	—	4.0	
MC3500XB, MC3400XB		—	—	50	—	—	8.0	
MC3500X, MC3400X		—	—	50	—	—	8.0	
Common Mode Input Voltage Range	V_{ICR}	±11	—	—	±11	—	—	V
Large Signal (V_O = ±10 V, R_L = 2.0 k)	A_{VOL}							V/mV
MC3500XA, MC3400XA		25	—	—	25	—	—	
MC3500XB, MC3400XB		25	—	—	25	—	—	
MC3500X, MC3400X		15	—	—	15	—	—	
Output Voltage Swing	V_O							V
($R_L \geq 10$ k)		±12	—	—	±12	—	—	
($R_L \geq 2.0$ k)		±10	—	—	±10	—	—	
Common Mode Rejection Ratio ($R_S \leq 10$ k)	CMRR							dB
MC3500XA, MC3400XA		80	—	—	80	—	—	
MC3500XB, MC3400XB		80	—	—	80	—	—	
MC3500X, MC3400X		70	—	—	70	—	—	
Supply Voltage Rejection Ratio ($R_S \leq 10$ k) (Note 3)	PSRR							dB
MC3500XA, MC3400XA		80	—	—	80	—	—	
MC3500XB, MC3400XB		80	—	—	80	—	—	
MC3500X, MC3400X		70	—	—	70	—	—	
Supply Current (Each Amplifier)	I_D							mA
MC3500XA, MC3400XA		—	—	2.8	—	—	2.8	
MC3500XB, MC3400XB		—	—	2.8	—	—	2.8	
MC3500X, MC3400X		—	—	3.0	—	—	3.0	

NOTES: (1) T_{low} = −55°C for MC35001/MC35001A/35001B
MC35002/MC35002A/35002B
MC35004/35004B
= 0°C for MC34001/34001A/34001B
MC34002/34002A/34002B
MC34004/34004B
T_{high} = +125°C for MC35001/MC35001A/35001B
MC35002/MC35002A/35002B
MC35004/35004B
= +70°C for MC34001/34001A/34001B
MC34002/34002A/34002B
MC34004/34004B

(2) The input bias currents approximately double for every 10°C rise in junction temperature, T_J. Due to limited test time, the input bias currents are correlated to junction temperature. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

(3) Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

(4) Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply.

2

TYPICAL PERFORMANCE CHARACTERISTICS

FIGURE 1 — INPUT BIAS CURRENT versus TEMPERATURE

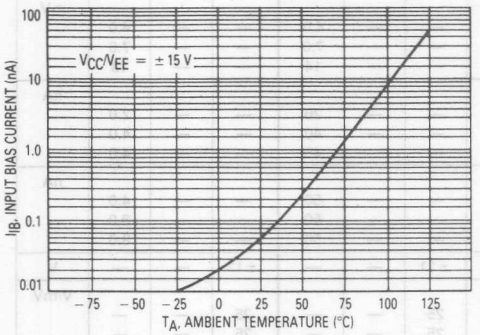


FIGURE 2 — OUTPUT VOLTAGE SWING versus FREQUENCY

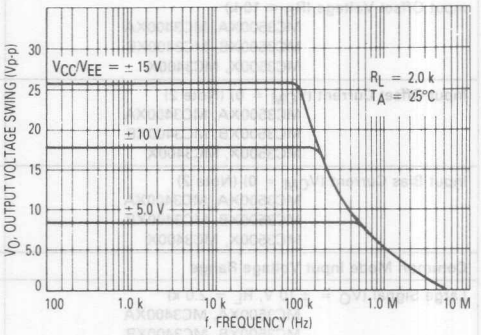


FIGURE 3 — OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

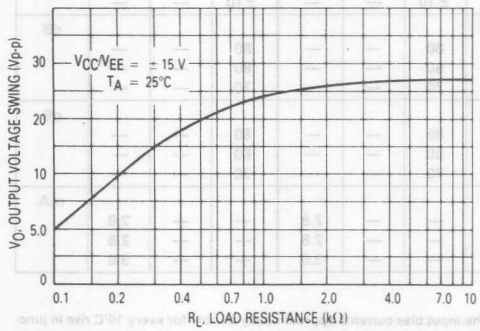


FIGURE 4 — OUTPUT VOLTAGE SWING versus SUPPLY VOLTAGE

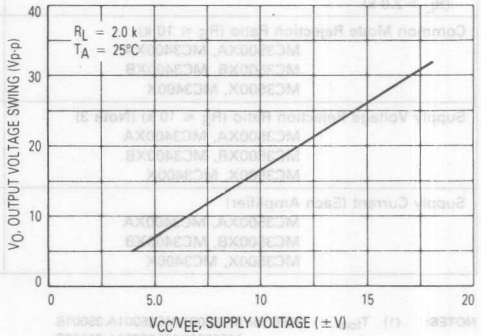


FIGURE 5 — OUTPUT VOLTAGE SWING versus TEMPERATURE

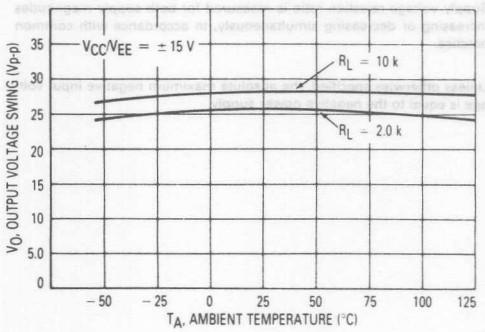


FIGURE 6 — SUPPLY CURRENT PER AMPLIFIER versus TEMPERATURE

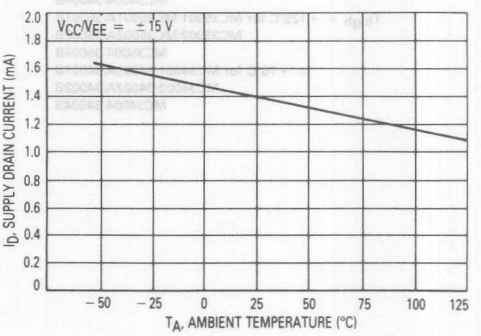


FIGURE 7 — LARGE-SIGNAL VOLTAGE GAIN AND PHASE SHIFT versus FREQUENCY

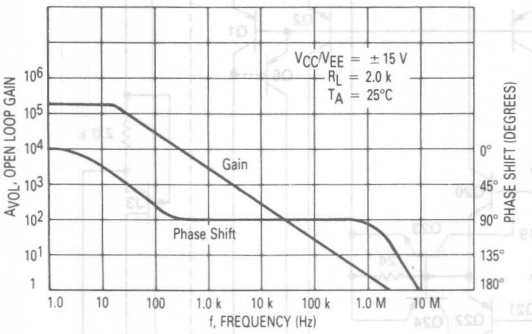


FIGURE 8 — LARGE-SIGNAL VOLTAGE GAIN versus TEMPERATURE

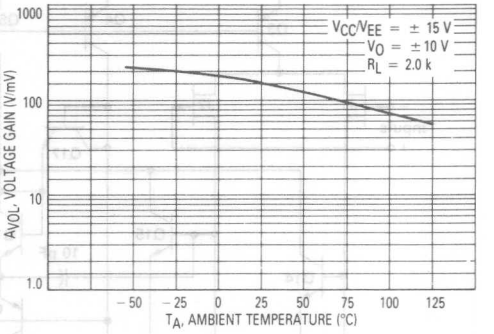


FIGURE 9 — NORMALIZED SLEW RATE versus TEMPERATURE

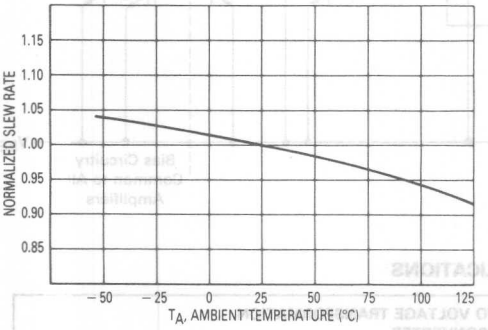


FIGURE 10 — EQUIVALENT INPUT NOISE VOLTAGE versus FREQUENCY

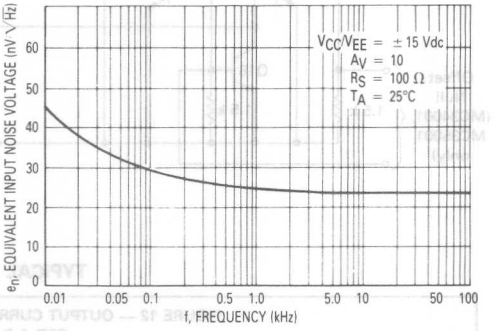
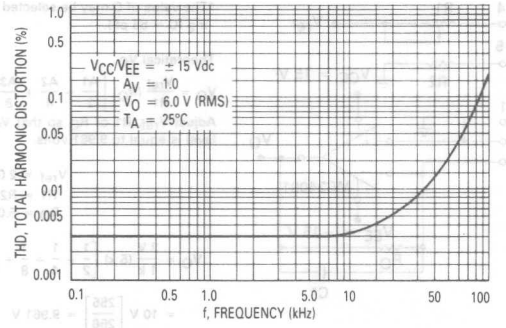
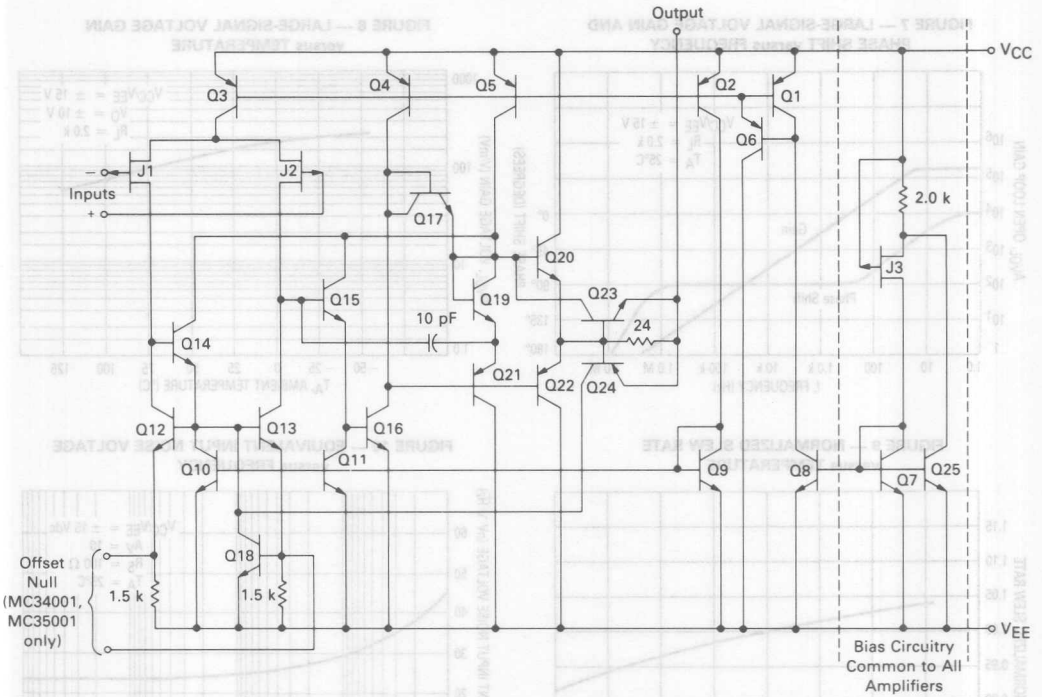


FIGURE 11 — TOTAL HARMONIC DISTORTION versus FREQUENCY

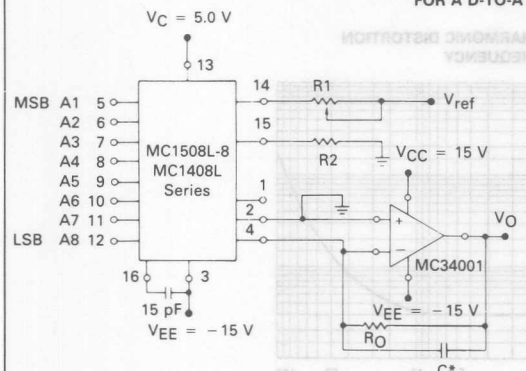


REPRESENTATIVE CIRCUIT SCHEMATIC
(Each Amplifier)



TYPICAL APPLICATIONS

FIGURE 12 — OUTPUT CURRENT TO VOLTAGE TRANSFORMATION FOR A D-TO-A CONVERTER



Settling time to within 1/2 LSB (±19.5 mV) is approximately 4.0 μs from the time all bits are switched.

*The value of C may be selected to minimize overshoot and ringing (C ≈ 68 pF).

Theoretical V_O

$$V_O = \frac{V_{ref}}{R1}(R_O)\left[\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right]$$

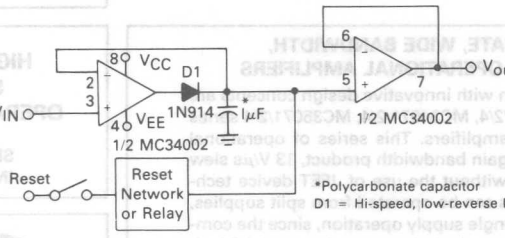
Adjust V_{ref}, R1 or R_O so that V_O with all digital inputs at high level is equal to 9.961 volts.

V_{ref} = 2.0 Vdc
R1 = R2 ≈ 1.0 kΩ
R_O = 5.0 kΩ

$$V_O = \frac{2\ V}{1\ k}(5\ k)\left[\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} + \frac{1}{256}\right]$$

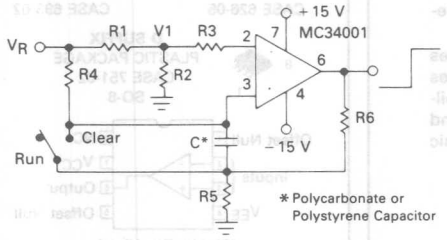
$$= 10\ V\left[\frac{255}{256}\right] = 9.961\ V$$

FIGURE 13 — POSITIVE PEAK DETECTOR



*Polycarbonate capacitor
D1 = Hi-speed, low-reverse leakage diode

FIGURE 14 — LONG INTERVAL RC TIMER

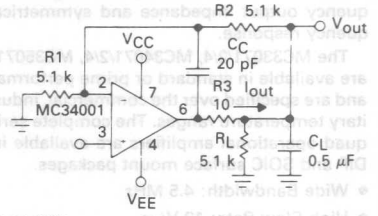


* Polycarbonate or Polystyrene Capacitor

Time (t) = R4 C ℓn (VR/VR−VI), R3 = R4, R5 = 0.1 R6
If R1 = R2: t = 0.693 R4C

Design Example: 100 Second Timer
VR = 10 v C = 1.0 μF R3 = R4 = 144 M
R6 = 20 k R5 = 2.0 k R1 = R2 = 1.0 k

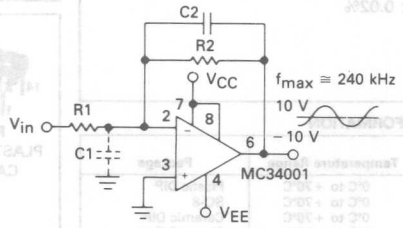
FIGURE 15 — ISOLATING LARGE CAPACITIVE LOADS



- Overshoot <10%
- t_s = 10 μs
- When driving large C_L, the V_{out} slew rate is determined by C_L and $I_{out(max)}$:

$$\frac{\Delta V_{out}}{\Delta t} = \frac{I_{out}}{C_L} = \frac{0.02}{0.5}\ V/\mu s = 0.04\ V/\mu s \text{ (with } C_L \text{ shown)}$$

FIGURE 16 — WIDE BW, LOW NOISE, LOW DRIFT AMPLIFIER



- Power BW: $f_{max} = \frac{S_r}{2\pi V_p} \cong 240\ kHz$
- Parasitic input capacitance (C1 ≅ 3 pF plus any additional layout capacitance) interacts with feedback elements and creates undesirable high-frequency pole. To compensate add C2 such that: R2C2 ≅ R1C1.

MOTOROLA

MC34071,2,4
MC35071,2,4
MC33071,2,4

HIGH SLEW RATE, WIDE BANDWIDTH, SINGLE SUPPLY OPERATIONAL AMPLIFIERS

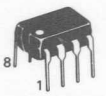
Quality bipolar fabrication with innovative design concepts are employed for the MC33071/2/4, MC34071/2/4, MC35071/2/4 series of monolithic operational amplifiers. This series of operational amplifiers offer 4.5 MHz of gain bandwidth product, 13 V/μs slew rate and fast settling time without the use of JFET device technology. Although this series can be operated from split supplies, it is particularly suited for single supply operation, since the common mode input voltage range includes ground potential (V_{EE}). With a Darlington input stage, this series exhibits high input resistance, low input offset voltage and high gain. The all NPN output stage, characterized by no deadband crossover distortion and large output voltage swing, provides high capacitance drive capability, excellent phase and gain margins, low open-loop high frequency output impedance and symmetrical source/sink ac frequency response.

The MC33071/2/4, MC34071/2/4, MC35071/2/4 series of devices are available in standard or prime performance (A Suffix) grades and are specified over the commercial, industrial/vehicular or military temperature ranges. The complete series of single, dual and quad operational amplifiers are available in the plastic, ceramic DIP and SOIC surface mount packages.

- Wide Bandwidth: 4.5 MHz
- High Slew Rate: 13 V/μs
- Fast Settling Time: 1.1 μs to 0.1%
- Wide Single Supply Operation: 3.0 V to 44 V
- Wide Input Common Mode Voltage Range: Includes Ground (V_{EE})
- Low Input Offset Voltage: 3.0 mV Maximum (A Suffix)
- Large Output Voltage Swing: −14.7 V to +14 V (with ±15 V Supplies)
- Large Capacitance Drive Capability: 0 to 10,000 pF
- Low Total Harmonic Distortion: 0.02%
- Excellent Phase Margin: 60°
- Excellent Gain Margin: 12 dB
- Output Short Circuit Protection

HIGH PERFORMANCE SINGLE SUPPLY OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUIT



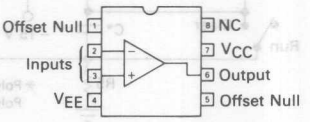
P SUFFIX
PLASTIC PACKAGE
CASE 626-05



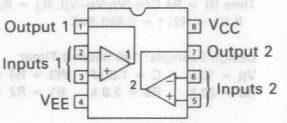
U SUFFIX
CERAMIC PACKAGE
CASE 693-02



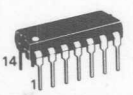
D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SO-8



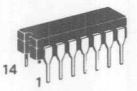
(Single, Top View)



(Dual, Top View)



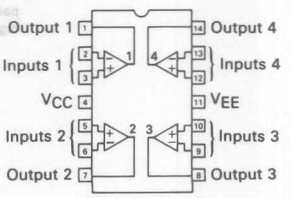
P SUFFIX
PLASTIC PACKAGE
CASE 646-06



L SUFFIX
CERAMIC PACKAGE
CASE 632-08



D SUFFIX
PLASTIC PACKAGE
CASE 751A-02
SO-14



(Quad, Top View)

ORDERING INFORMATION

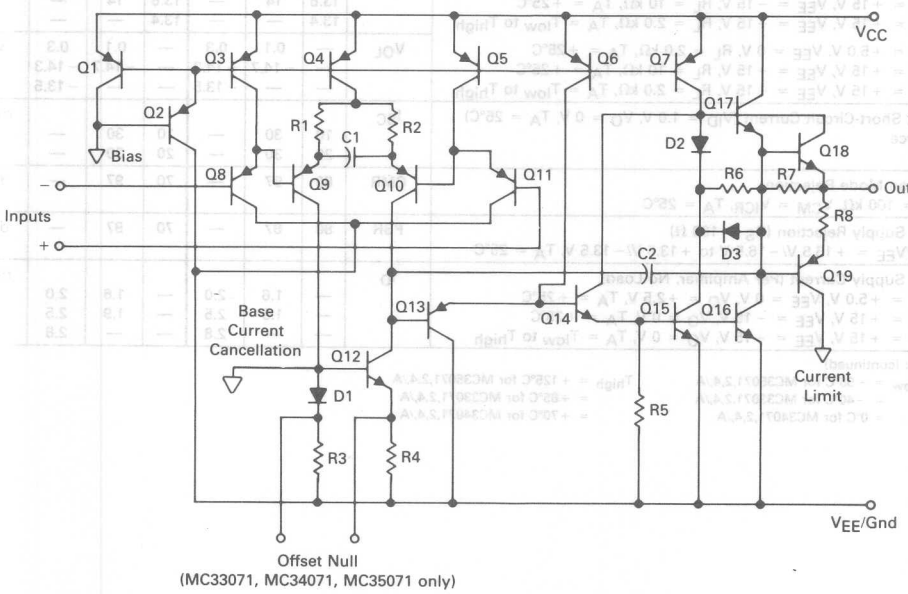
Op Amp Function	Device	Temperature Range	Package
Single	MC34071P, AP	0°C to +70°C	Plastic DIP
	MC34071D, AD	0°C to +70°C	SO-8
	MC34071U, AU	0°C to +70°C	Ceramic DIP
	MC33071P, AP	−40°C to +85°C	Plastic DIP
	MC33071D, AD	−40°C to +85°C	SO-8
	MC33071U, AU	−40°C to +85°C	Ceramic DIP
	MC35071U, AU	−55°C to +125°C	Ceramic DIP
Dual	MC34072P, AP	0°C to +70°C	Plastic DIP
	MC34072D AD	0°C to +70°C	SO-8
	MC34072U, AU	0°C to +70°C	Ceramic DIP
	MC33072P, AP	−40°C to +85°C	Plastic DIP
	MC33072D AD	−40°C to +85°C	SO-8
	MC33072U, AU	−40°C to +85°C	Ceramic DIP
	MC35072U, AU	−55°C to +125°C	Ceramic DIP
Quad	MC34074P, AP	0°C to +70°C	Plastic DIP
	MC34074D, AD	0°C to +70°C	SO-14
	MC34074U, AU	0°C to +70°C	Ceramic DIP
	MC33074P, AP	−40°C to +85°C	Plastic DIP
	MC33074D, AD	−40°C to +85°C	SO-14
	MC33074U, AU	−40°C to +85°C	Ceramic DIP
	MC35074U, AU	−55°C to +125°C	Ceramic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (from V_{EE} to V_{CC})	V_S	+44	Volts
Input Differential Voltage Range	V_{IDR}	Note 1	Volts
Input Voltage Range	V_{IR}	Note 1	Volts
Output Short-Circuit Duration (Note 2)	t_S	Indefinite	Seconds
Operating Junction Temperature Ceramic Package Plastic Package	T_J	 +160 +150	°C
Storage Temperature Range Ceramic Package Plastic Package	T_{stg}	 −65 to +160 −60 to +150	°C

NOTES:
1. Either or both input voltages should not exceed the magnitude of V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (see Figure 1).

EQUIVALENT CIRCUIT SCHEMATIC (EACH AMPLIFIER)



DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, R_L = connected to ground unless otherwise noted. See [Note 3] for T_A = T_{low} to T_{high})

		A Suffix			Non-Suffix			
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Input Offset Voltage (R_S = 100 Ω, V_{CM} = 0 V, V_O = 0 V)	V_{IO}							mV
V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25°C		—	0.5	3.0	—	1.0	5.0	
V_{CC} = +5.0 V, V_{EE} = 0 V, T_A = +25°C		—	0.5	3.0	—	1.5	5.0	
V_{CC} = +15 V, V_{EE} = −15 V, T_A = T_{low} to T_{high}		—	—	5.0	—	—	7.0	
Average Temperature Coefficient of Input Offset Voltage R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V, T_A = T_{low} to T_{high}	$\Delta V_{IO}/\Delta T$	—	10	—	—	10	—	μV/°C
Input Bias Current (V_{CM} = 0 V, V_O = 0 V)	I_{IB}							nA
T_A = +25°C		—	100	500	—	100	500	
T_A = T_{low} to T_{high}		—	—	700	—	—	700	
Input Offset Current (V_{CM} = 0 V, V_O = 0 V)	I_{IO}							nA
T_A = +25°C		—	6.0	50	—	6.0	75	
T_A = T_{low} to T_{high}		—	—	300	—	—	300	
Input Common Mode Voltage Range	V_{ICR}							V
T_A = +25°C		V_{EE} to (V_{CC} − 1.8)			V_{EE} to (V_{CC} − 1.8)			
T_A = T_{low} to T_{high}		V_{EE} to (V_{CC} − 2.2)			V_{EE} to (V_{CC} − 2.2)			
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 kΩ)	A_{VOL}							V/mV
T_A = +25°C		50	100	—	25	100	—	
T_A = T_{low} to T_{high}		25	—	—	20	—	—	
Output Voltage Swing (V_{ID} = ±1.0 V)	V_{OH}							V
V_{CC} = +5.0 V, V_{EE} = 0 V, R_L = 2.0 kΩ, T_A = +25°C		3.7	4.0	—	3.7	4.0	—	
V_{CC} = +15 V, V_{EE} = −15 V, R_L = 10 kΩ, T_A = +25°C		13.6	14	—	13.6	14	—	
V_{CC} = +15 V, V_{EE} = −15 V, R_L = 2.0 kΩ, T_A = T_{low} to T_{high}		13.4	—	—	13.4	—	—	
V_{CC} = +5.0 V, V_{EE} = 0 V, R_L = 2.0 kΩ, T_A = +25°C	V_{OL}	—	0.1	0.3	—	0.1	0.3	V
V_{CC} = +15 V, V_{EE} = −15 V, R_L = 10 kΩ, T_A = +25°C		—	−14.7	−14.3	—	−14.7	−14.3	
V_{CC} = +15 V, V_{EE} = −15 V, R_L = 2.0 kΩ, T_A = T_{low} to T_{high}		—	—	−13.5	—	—	−13.5	
Output Short-Circuit Current (V_{ID} = 1.0 V, V_O = 0 V, T_A = 25°C)	I_{SC}							mA
Source		10	30	—	10	30	—	
Sink		20	30	—	20	30	—	
Common Mode Rejection R_S = 100 kΩ, V_{CM} = V_{ICR}, T_A = 25°C	CMR	80	97	—	70	97	—	dB
Power Supply Rejection (R_S = 100 Ω) V_{CC}/V_{EE} = +16.5 V/−16.5 V to +13.5 V/−13.5 V, T_A = 25°C	PSR	80	97	—	70	97	—	dB
Power Supply Current (Per Amplifier, No Load)	I_D							mA
V_{CC} = +5.0 V, V_{EE} = 0 V, V_O = +2.5 V, T_A = +25°C		—	1.6	2.0	—	1.6	2.0	
V_{CC} = +15 V, V_{EE} = −15 V, V_O = 0 V, T_A = +25°C		—	1.9	2.5	—	1.9	2.5	
V_{CC} = +15 V, V_{EE} = −15 V, V_O = 0 V, T_A = T_{low} to T_{high}		—	—	2.8	—	—	2.8	

NOTES: (continued)

3. T_{low} = −55°C for MC35071,2,4,/A
= −40°C for MC33071,2,4,/A
= 0°C for MC34071,2,4,/A

T_{high} = +125°C for MC35071,2,4,/A
= +85°C for MC33071,2,4,/A
= +70°C for MC34071,2,4,/A

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, R_L = connected to ground, T_A = +25°C unless otherwise noted)

Characteristic	Symbol	A Suffix Min	A Suffix Typ	A Suffix Max	Non-Suffix Min	Non-Suffix Typ	Non-Suffix Max	Unit
Slew Rate (V_{in} = −10 V to +10 V, R_L = 2.0 kΩ, C_L = 500 pF)	SR							V/μs
A_V = +1.0		8.0	10	—	8.0	10	—	
A_V = −1.0		—	13	—	—	13	—	
Settling Time (10 V Step, A_V = −1.0)	t_s							μs
To 0.1% (+1/2 LSB of 9-Bits)		—	1.1	—	—	1.1	—	
To 0.01% (+1/2 LSB of 12-Bits)		—	2.2	—	—	2.2	—	
Gain Bandwidth Product (f = 100 kHz)	GBW	3.5	4.5	—	3.5	4.5	—	MHz
Power Bandwidth A_V = +1.0, R_L = 2.0 kΩ, V_O = 20 V_{p-p}, THD = 5.0%	BW	—	200	—	—	200	—	kHz
Phase Margin	ϕ_m							Deg
R_L = 2.0 kΩ		—	60	—	—	60	—	
R_L = 2.0 kΩ, C_L = 300 pF		—	40	—	—	40	—	
Gain Margin	A_m							dB
R_L = 2.0 kΩ		—	12	—	—	12	—	
R_L = 2.0 kΩ, C_L = 300 pF		—	4.0	—	—	4.0	—	
Equivalent Input Noise Voltage R_S = 100 Ω, f = 1.0 kHz	e_n	—	32	—	—	32	—	$\frac{pA}{\sqrt{Hz}}$
Equivalent Input Noise Current f = 1.0 kHz	i_n	—	0.22	—	—	0.22	—	$\frac{pA}{\sqrt{Hz}}$
Differential Input Resistance V_{CM} = 0 V	R_{IN}	—	150	—	—	150	—	MΩ
Differential Input Capacitance V_{CM} = 0 V	C_{IN}	—	2.5	—	—	2.5	—	pF
Total Harmonic Distortion A_V = +10, R_L = 2.0 kΩ, 2.0 $V_{p-p} \leq V_O \leq$ 20 V_{p-p}, f = 10 kHz	THD	—	0.02	—	—	0.02	—	%
Channel Separation (f = 10 kHz)	—	—	120	—	—	120	—	dB
Open-Loop Output Impedance (f = 1.0 MHz)	$\|Z_O\|$	—	30	—	—	30	—	Ω

FIGURE 1 — POWER SUPPLY CONFIGURATIONS

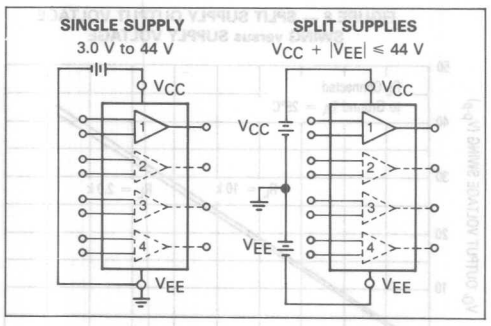
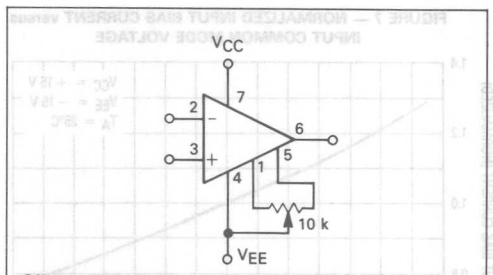


FIGURE 2 — OFFSET NULL CIRCUIT



Offset nulling range is approximately ±80 mV with a 10 k potentiometer (MC33071, MC34071, MC35071 only).

2

TYPICAL PERFORMANCE CURVES

FIGURE 3 — MAXIMUM POWER DISSIPATION versus TEMPERATURE FOR PACKAGE TYPES

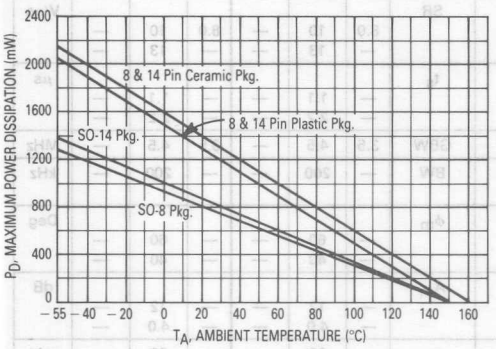


FIGURE 4 — INPUT OFFSET VOLTAGE versus TEMPERATURE FOR REPRESENTATIVE UNITS

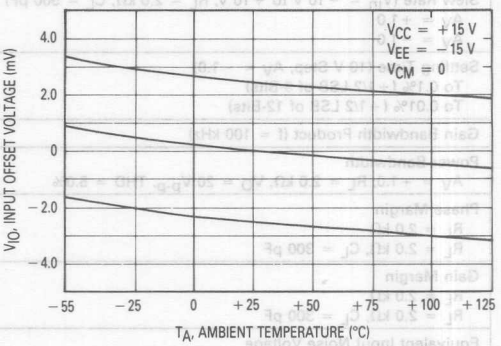


FIGURE 5 — INPUT COMMON MODE VOLTAGE RANGE versus TEMPERATURE

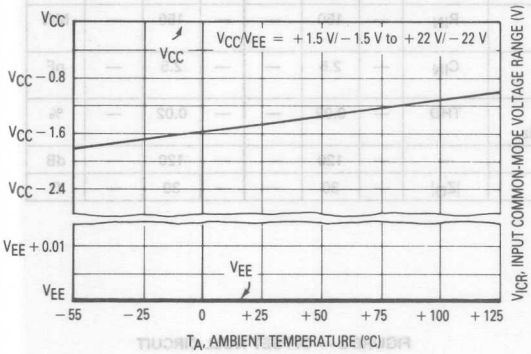


FIGURE 6 — NORMALIZED INPUT BIAS CURRENT versus TEMPERATURE

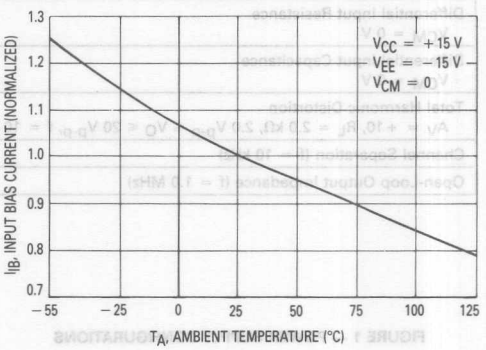


FIGURE 7 — NORMALIZED INPUT BIAS CURRENT versus INPUT COMMON MODE VOLTAGE

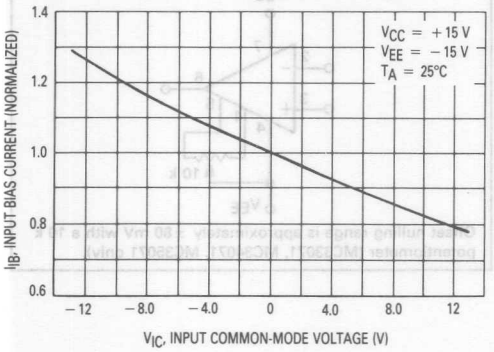


FIGURE 8 — SPLIT SUPPLY OUTPUT VOLTAGE SWING versus SUPPLY VOLTAGE

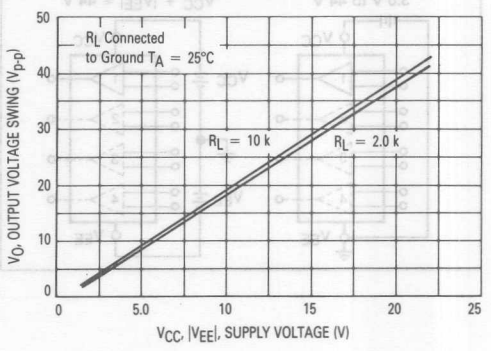


FIGURE 9 — SPLIT SUPPLY OUTPUT SATURATION versus LOAD CURRENT

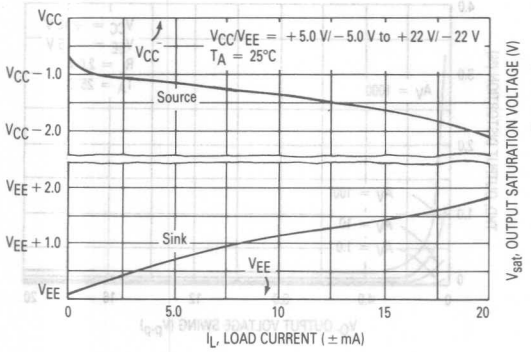


FIGURE 10 — SINGLE SUPPLY OUTPUT SATURATION versus LOAD RESISTANCE TO GROUND

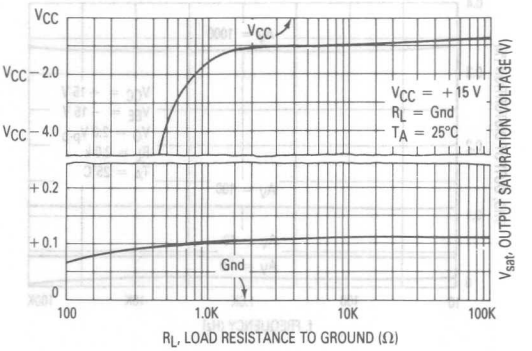


FIGURE 11 — SINGLE SUPPLY OUTPUT SATURATION versus LOAD RESISTANCE TO V_{CC}

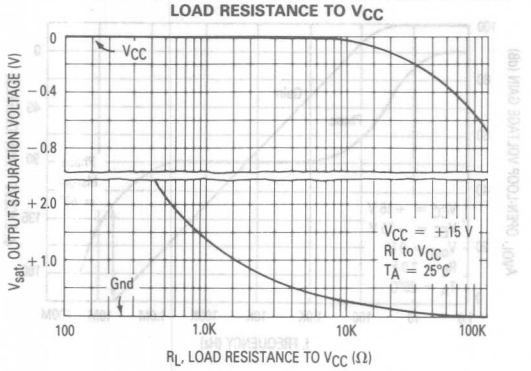


FIGURE 12 — OUTPUT SHORT CIRCUIT CURRENT versus TEMPERATURE

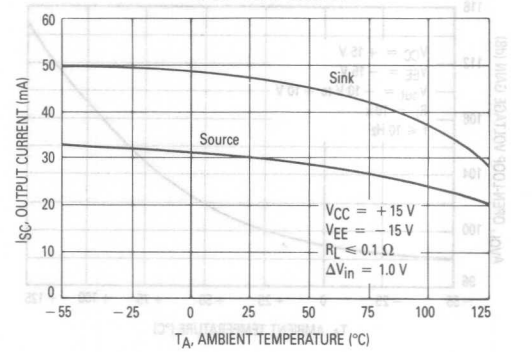


FIGURE 13 — OUTPUT IMPEDANCE versus FREQUENCY

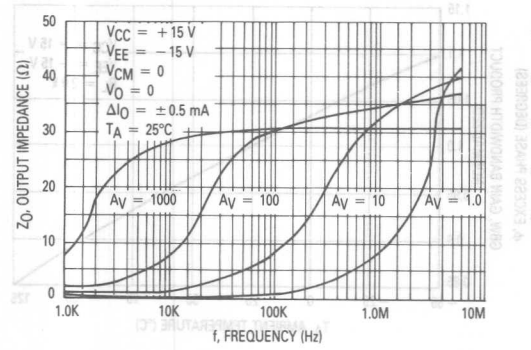


FIGURE 14 — OUTPUT VOLTAGE SWING versus FREQUENCY

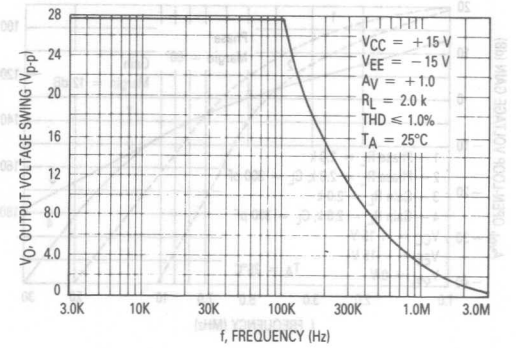


FIGURE 15 — OUTPUT DISTORTION versus FREQUENCY

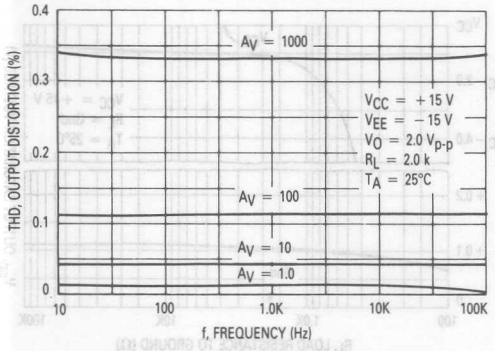


FIGURE 16 — OUTPUT DISTORTION versus OUTPUT VOLTAGE SWING

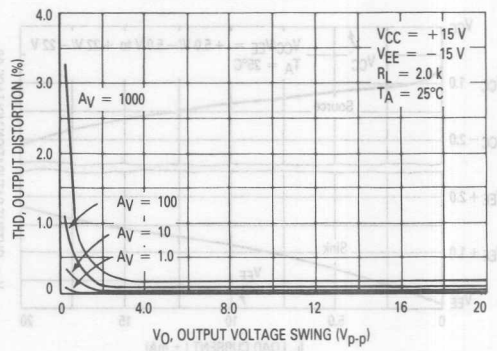


FIGURE 17 — OPEN-LOOP VOLTAGE GAIN versus TEMPERATURE

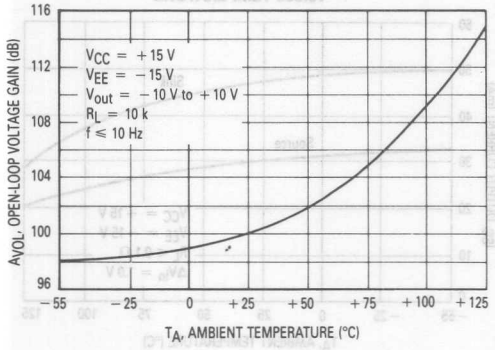


FIGURE 18 — OPEN-LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY

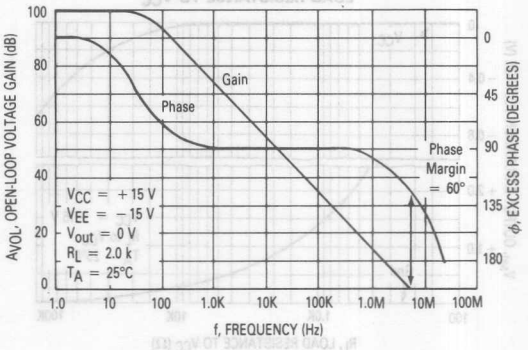


FIGURE 19 — OPEN-LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY

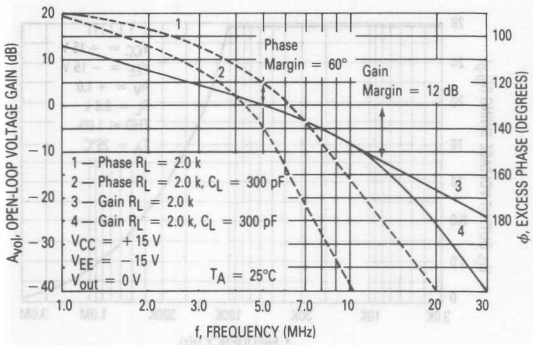


FIGURE 20 — NORMALIZED GAIN BANDWIDTH PRODUCT versus TEMPERATURE

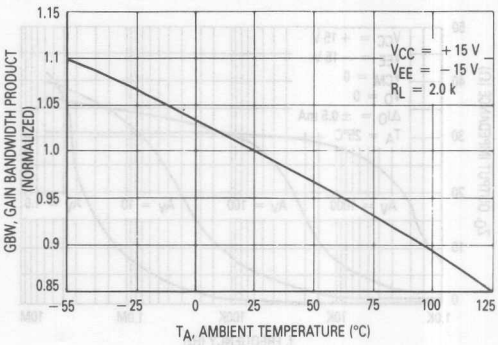


FIGURE 21 — PERCENT OVERSHOOT versus LOAD CAPACITANCE

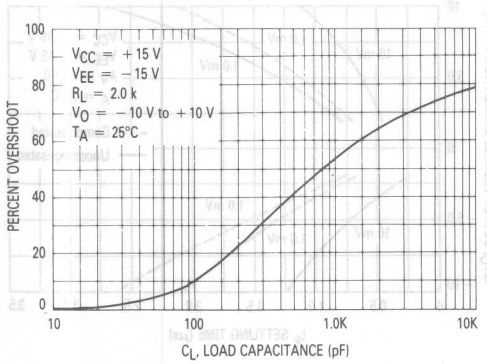


FIGURE 22 — PHASE MARGIN versus LOAD CAPACITANCE

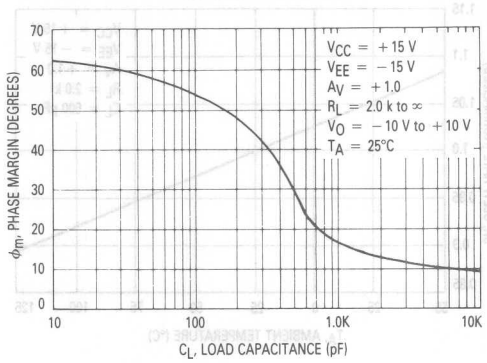


FIGURE 23 — GAIN MARGIN versus LOAD CAPACITANCE

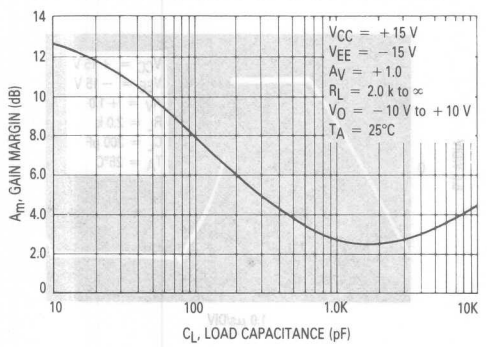


FIGURE 24 — PHASE MARGIN versus TEMPERATURE

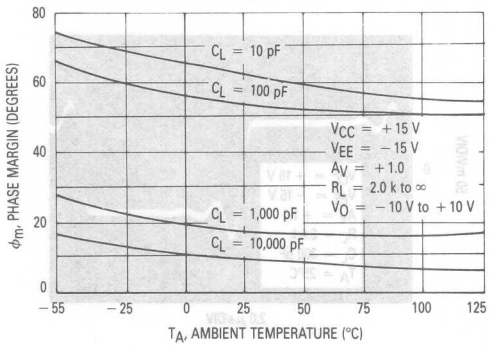


FIGURE 25 — GAIN MARGIN versus TEMPERATURE

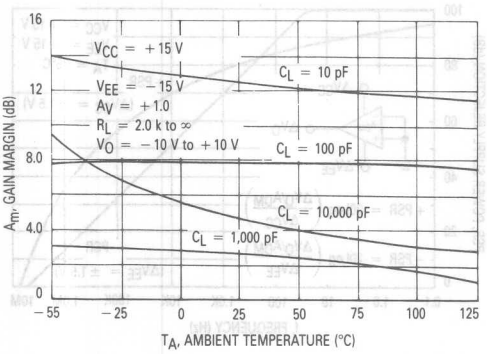
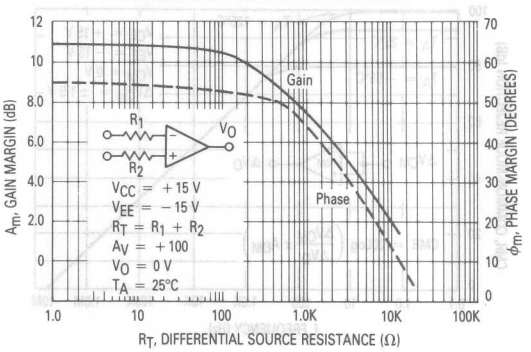


FIGURE 26 — PHASE MARGIN AND GAIN MARGIN versus DIFFERENTIAL SOURCE RESISTANCE



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FIGURE 27 — NORMALIZED SLEW RATE versus TEMPERATURE

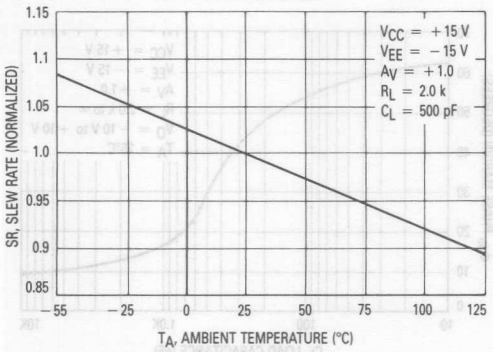


FIGURE 28 — OUTPUT SETTLING TIME

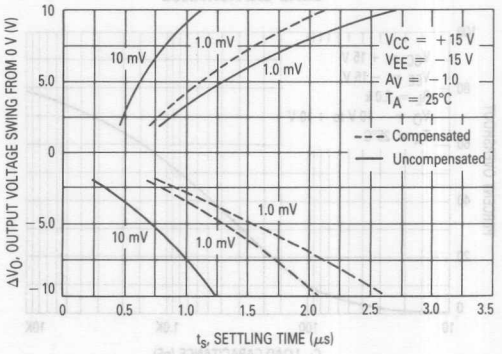


FIGURE 29 — SMALL SIGNAL TRANSIENT RESPONSE

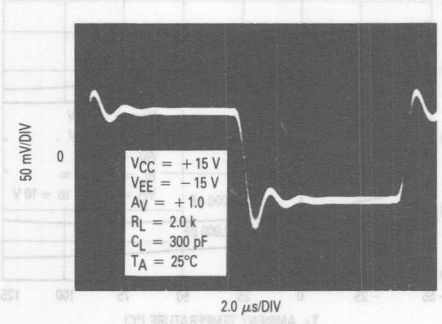


FIGURE 30 — LARGE SIGNAL TRANSIENT RESPONSE

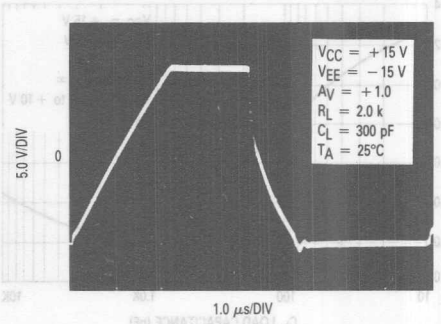


FIGURE 31 — COMMON MODE REJECTION versus FREQUENCY

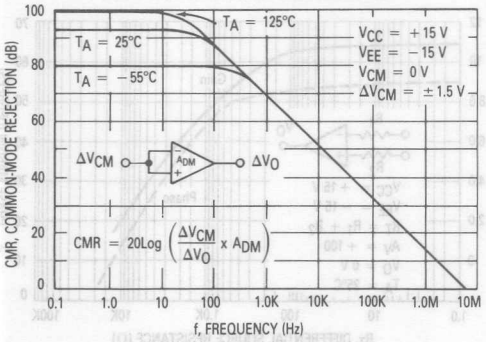


FIGURE 32 — POWER SUPPLY REJECTION versus FREQUENCY

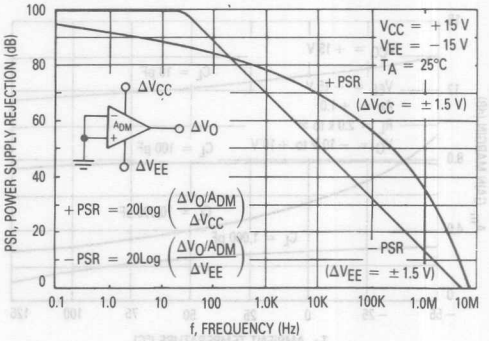


FIGURE 33 — SUPPLY CURRENT versus SUPPLY VOLTAGE

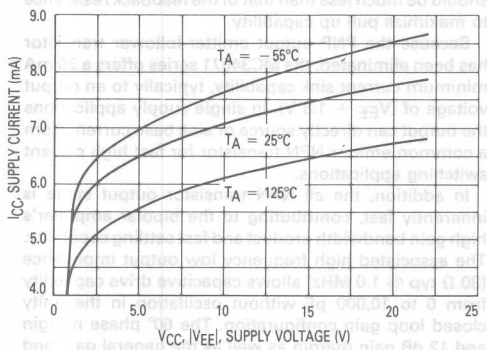


FIGURE 34 — POWER SUPPLY REJECTION versus TEMPERATURE

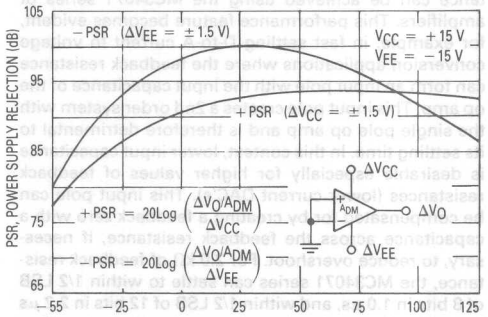


FIGURE 35 — CHANNEL SEPARATION versus FREQUENCY

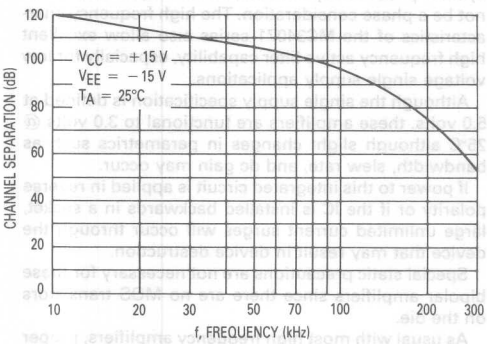
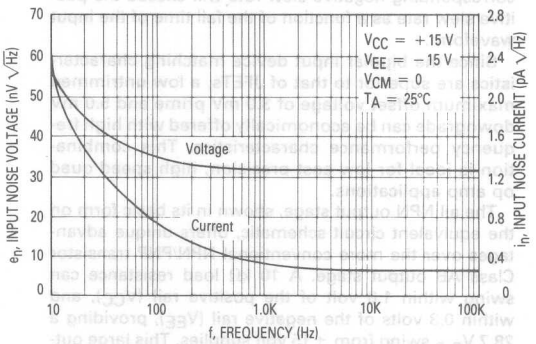


FIGURE 36 — INPUT NOISE versus FREQUENCY



APPLICATIONS INFORMATION

CIRCUIT DESCRIPTION/PERFORMANCE FEATURES OF THE MC34071 SERIES

Although the bandwidth, slew rate, and settling time of the MC34071 amplifier series are similar to op amp products utilizing JFET input devices, these amplifiers offer other additional distinct advantages as a result of the PNP transistor differential input stage and an all NPN transistor output stage.

Since the input common mode voltage range of this input stage includes the V_{EE} potential, single supply operation is feasible to as low as 3.0 volts with the common mode input voltage at ground potential.

The input stage also allows differential input voltages up to ±44 volts, provided the maximum input voltage range is not exceeded. Specifically, the input voltages must range between V_{EE} and V_{CC} supply voltages as shown by the maximum rating table. In practice, although not recommended, the input voltages can exceed the V_{CC} voltage by approximately 3.0 volts and decrease below the V_{EE} voltage by 0.3 volts without causing product damage, although output phase reversal may occur. It is also possible to source up to approximately 5.0 mA of current from V_{EE} through either input's clamping diode without damage or latching, although phase reversal may again occur.

If one or both inputs exceed the upper common mode voltage limit the amplifier output is readily predictable and may be in a low or high state depending on the existing input bias conditions.

than the typical JFET input gate capacitance (5.0 pF), better frequency response for a given input source resistance can be achieved using the MC34071 series of amplifiers. This performance feature becomes evident, for example, in fast settling D-to-A current to voltage conversion applications where the feedback resistance can form an input pole with the input capacitance of the op amp. This input pole creates a 2nd order system with the single pole op amp and is therefore detrimental to its settling time. In this context, lower input capacitance is desirable especially for higher values of feedback resistances (lower current DAC's). This input pole can be compensated for by creating a feedback zero with a capacitance across the feedback resistance, if necessary, to reduce overshoot. For 2.0 kΩ of feedback resistance, the MC34071 series can settle to within 1/2 LSB of 8 bits in 1.0 μs, and within 1/2 LSB of 12 bits in 2.2 μs for a 10 volt step. In a inverting unity gain fast settling configuration, the symmetrical slew rate is ±13 volts/μs. In the classic noninverting unity gain configuration the output positive slew rate is +10 volts/μs, and the corresponding negative slew rate will exceed the positive slew rate as a function of the fall time of the input waveform.

Since the bipolar input device matching characteristics are superior to that of JFETs, a low untrimmed maximum offset voltage of 3.0 mV prime and 5.0 mV downgrade can be economically offered with high frequency performance characteristics. This combination is ideal for low cost precision, high speed quad op amp applications.

The all NPN output stage, shown in its basic form on the equivalent circuit schematic, offers unique advantages over the more conventional NPN/PNP transistor Class AB output stage. A 10 kΩ load resistance can swing within 1.0 volt of the positive rail (V_{CC}), and within 0.3 volts of the negative rail (V_{EE}), providing a 28.7 V_{p-p} swing from ±15 volt supplies. This large output swing becomes most noticable at lower supply voltages.

The positive swing is limited by the saturation voltage of the current source transistor Q_7, and V_{BE} of the NPN pull up transistor Q_{17}, and the voltage drop associated with the short circuit resistance, R_7. The negative swing is limited by the saturation voltage of the pull-down transistor Q_{16}, the voltage drop $I_L R_6$, and the voltage drop associated with resistance R_7, where I_L is the sink load current. For small valued sink currents, the above voltage drops are negligible, allowing the negative swing voltage to approach within millivolts of V_{EE}. For large valued sink currents (>5.0 mA), diode D3 clamps the voltage across R_6, thus limiting the negative swing to the saturation voltage of Q_{16}, plus the forward diode drop of D3 ($\approx V_{EE}$ + 1.0 V). Thus for a given supply voltage, unprecedented peak-to-peak output voltage swing is possible as indicated by the output swing specifications.

If the load resistance is referenced to V_{CC} instead of ground for single supply applications, the maximum possible output swing can be achieved for a given supply and the output will pull the load resistance near ground during the negative swing. The load resistance value should be much less than that of the feedback resistance to maximize pull up capability.

Because the PNP output emitter-follower transistor has been eliminated, the MC34071 series offers a 20 mA minimum current sink capability, typically to an output voltage of (V_{EE} + 1.8 V). In single supply applications the output can directly source or sink base current from a common emitter NPN transistor for fast high current switching applications.

In addition, the all NPN transistor output stage is inherently fast, contributing to the bipolar amplifier's high gain bandwidth product and fast settling capability. The associated high frequency low output impedance (30 Ω typ @ 1.0 MHz) allows capacitive drive capability from 0 to 10,000 pF without oscillation in the unity closed loop gain configuration. The 60° phase margin and 12 dB gain margin as well as the general gain and phase characteristics are virtually independent of the source/sink output swing conditions. This allows easier system phase compensation, since output swing will not be a phase consideration. The high frequency characteristics of the MC34071 series also allow excellent high frequency active filter capability, especially for low voltage single supply applications.

Although the single supply specification is defined at 5.0 volts, these amplifiers are functional to 3.0 volts @ 25°C although slight changes in parametrics such as bandwidth, slew rate, and dc gain may occur.

If power to this integrated circuit is applied in reverse polarity or if the IC is installed backwards in a socket, large unlimited current surges will occur through the device that may result in device destruction.

Special static precautions are not necessary for these bipolar amplifiers since there are no MOS transistors on the die.

As usual with most high frequency amplifiers, proper lead dress, component placement, and PC board layout should be exercised for optimum frequency performance. For example, long unshielded input or output leads may result in unwanted input-output coupling. In order to preserve the relatively low input capacitance associated with these amplifiers, resistors connected to the inputs should be immediately adjacent to the input pin to minimize additional stray input capacitance. This not only minimizes the input pole for optimum frequency response, but also minimizes extraneous "pick up" at this node. Supply decoupling with adequate capacitance immediately adjacent to the supply pin is also important, particularly over temperature, since many types of decoupling capacitors exhibit great impedance changes over temperature.

The output of any one amplifier is current limited and thus protected from a direct short to ground. However, under such conditions, it is important not to allow the device to exceed the maximum junction temperature rating. Typically for ±15 volt supplies, any one output can be shorted continuously to ground without exceeding the maximum temperature rating.

TYPICAL SINGLE SUPPLY APPLICATIONS V_{CC} = 5.0 VOLTS

FIGURE 37 — AC COUPLED NONINVERTING AMPLIFIER

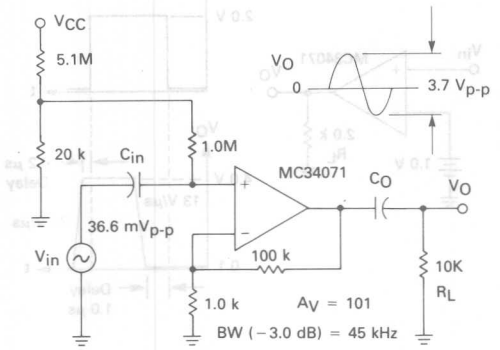


FIGURE 38 — AC COUPLED INVERTING AMPLIFIER

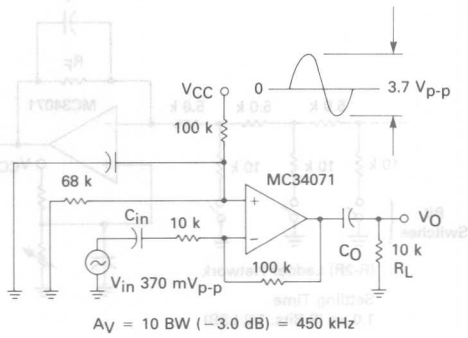


FIGURE 39 — DC COUPLED INVERTING AMPLIFIER MAXIMUM OUTPUT SWING

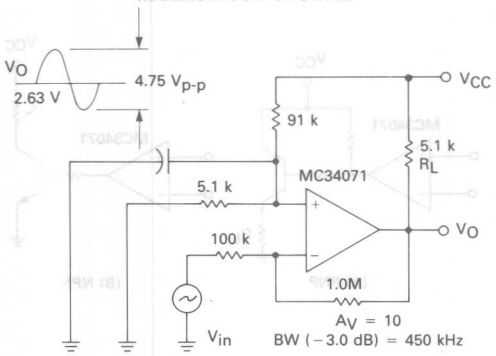


FIGURE 40 — UNITY GAIN BUFFER TTL DRIVER

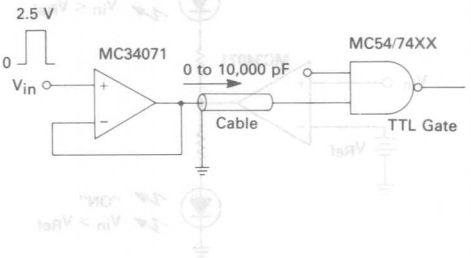


FIGURE 41 — ACTIVE HIGH-Q NOTCH FILTER

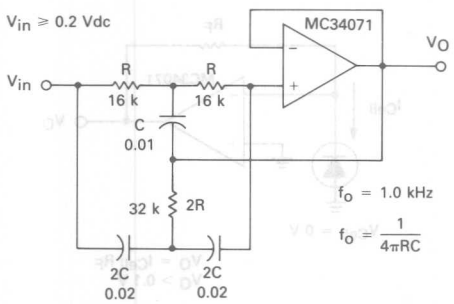
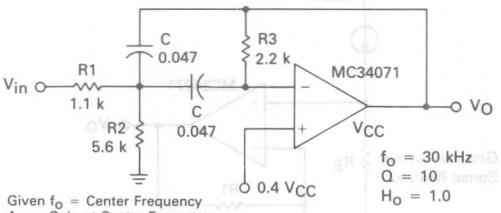


FIGURE 42 — ACTIVE BANDPASS FILTER



Given f_o = Center Frequency
A_o = Gain at Center Frequency
Choose Value f_o, Q, A_o, C
Then

$$R3 = \frac{Q}{\pi f_o C} \qquad R1 = \frac{R3}{2H_o} \qquad R2 = \frac{R1\,R3}{4Q^2R1 - R3}$$

For less than 10% error from operational amplifier

$$\frac{Q_o f_o}{GBW} < 0.1$$

Where f_o and GBW are expressed in Hz.
GBW = 4.5 MHz Typ.

2

FIGURE 43 — LOW VOLTAGE FAST D/A CONVERTER

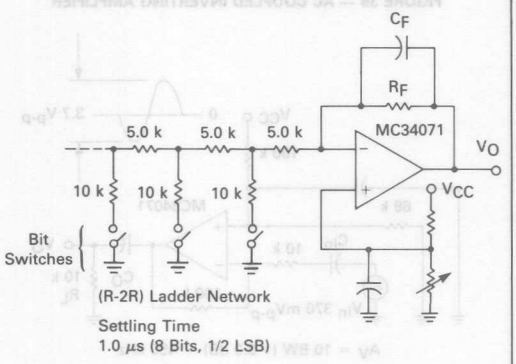


FIGURE 44 — HIGH SPEED LOW VOLTAGE COMPARATOR

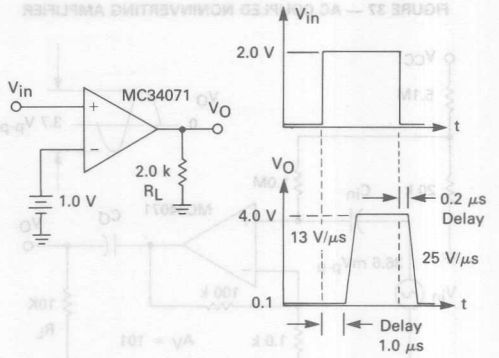


FIGURE 45 — LED DRIVER

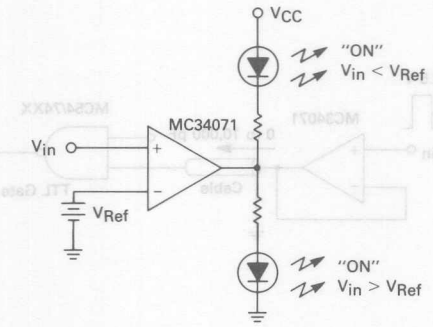


FIGURE 46 — TRANSISTOR DRIVER

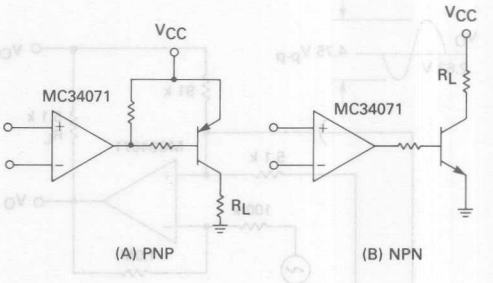


FIGURE 47 — AC/DC GROUND CURRENT MONITOR

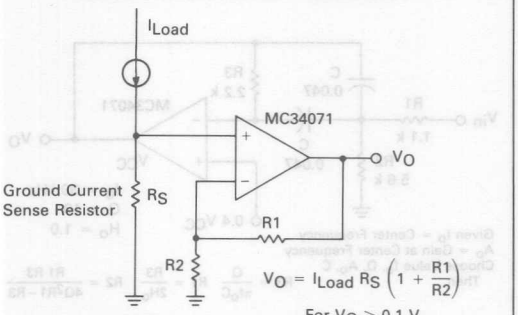


FIGURE 48 — PHOTOVOLTAIC CELL AMPLIFIER

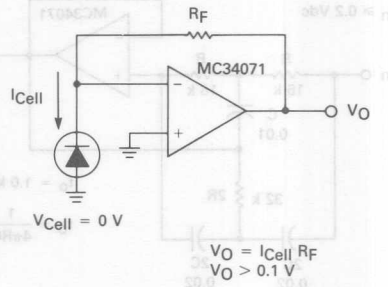
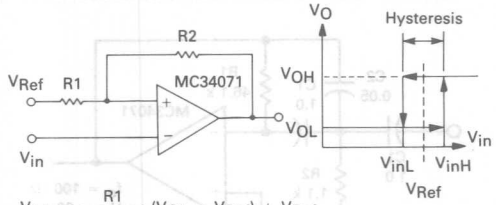


FIGURE 49 — LOW INPUT VOLTAGE COMPARATOR WITH HYSTERESIS

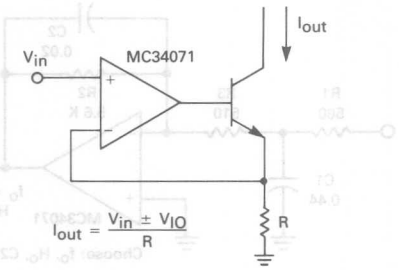


$$V_{inL} = \frac{R1}{R1 + R2}(V_{OL} - V_{Ref}) + V_{Ref}$$

$$V_{inH} = \frac{R1}{R1 + R2}(V_{OH} - V_{Ref}) + V_{Ref}$$

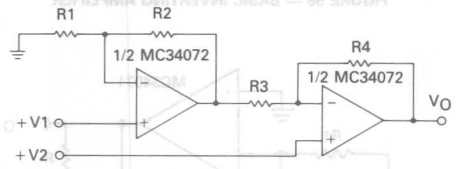
$$V_H = \frac{R1}{R1 + R}(V_{OH} - V_{OL})$$

FIGURE 50 — HIGH COMPLIANCE VOLTAGE TO SINK CURRENT CONVERTER



$$I_{out} = \frac{V_{in} \pm V_{IO}}{R}$$

FIGURE 51 — HIGH INPUT IMPEDANCE DIFFERENTIAL AMPLIFIER

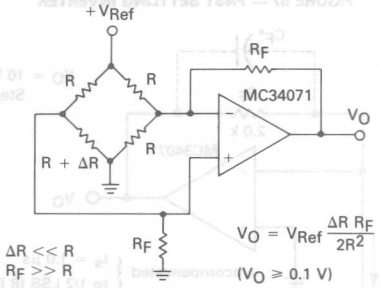


$$\frac{R2}{R1} = \frac{R4}{R3} \text{ (Critical to CMRR)}$$

$$V_O = 1\left(+\frac{R4}{R3}\right)\left(V2 - V1\frac{R4}{R3}\right)$$

For (V2 ≥ V1), V > 0

FIGURE 52 — BRIDGE CURRENT AMPLIFIER



$$V_O = V_{Ref}\frac{\Delta R\, R_F}{2R^2}$$

$\Delta R << R$

$R_F >> R$

$(V_O \geq 0.1\ V)$

FIGURE 53 — LOW VOLTAGE PEAK DETECTOR

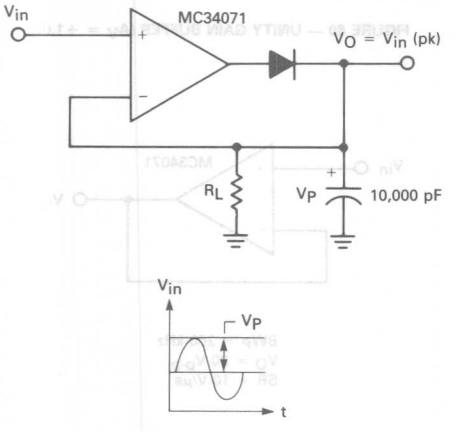


FIGURE 54 — HIGH FREQUENCY PULSE WIDTH MODULATION

$$f_{OSC} \cong \frac{0.85}{RC}$$

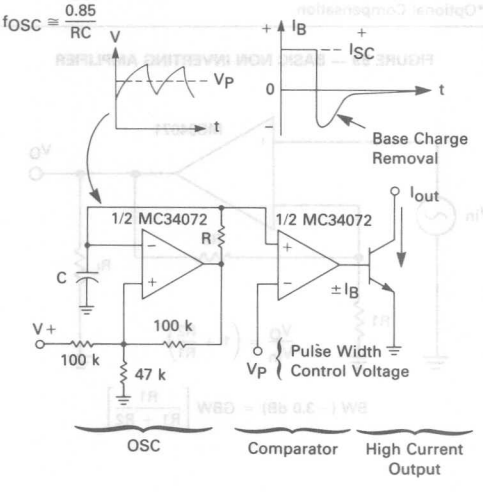
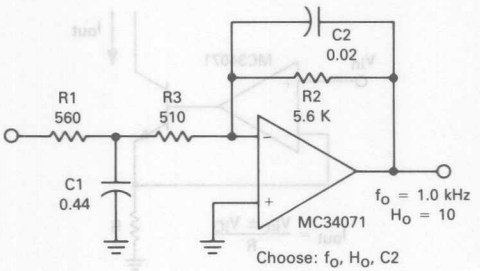


FIGURE 55 — SECOND ORDER LOW-PASS ACTIVE FILTER

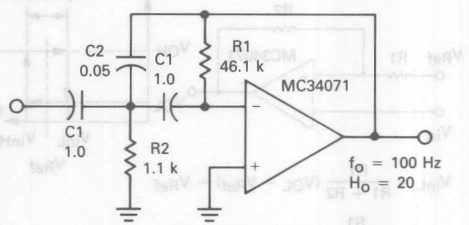


Choose: f_o, H_o, C2

Then: C1 = 2C2 (H_o + 1)

$$R2 = \frac{\sqrt{2}}{4\pi f_o C2} \qquad R3 = \frac{R2}{H_o + 1} \qquad R1 = \frac{R2}{H_o}$$

FIGURE 56 — SECOND ORDER HIGH-PASS ACTIVE FILTER

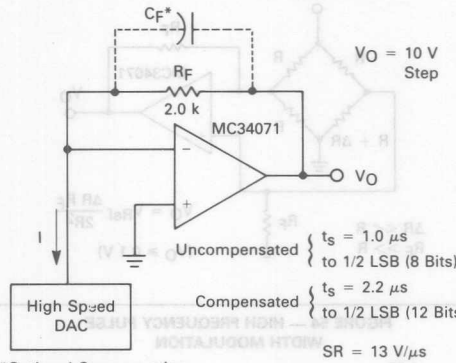


Choose: f_o, H_o, C1 Then: $R1 = \frac{H_o + 0.5}{\pi f_o C1\sqrt{2}}$

$$R2 = \frac{\sqrt{2}}{2\pi f_o C1\,(1/H_o + 2)}$$

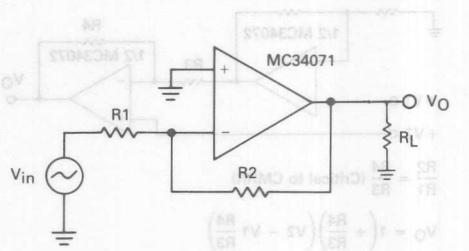
$$C2 = \frac{C}{H_o}$$

FIGURE 57 — FAST SETTLING INVERTER



*Optional Compensation

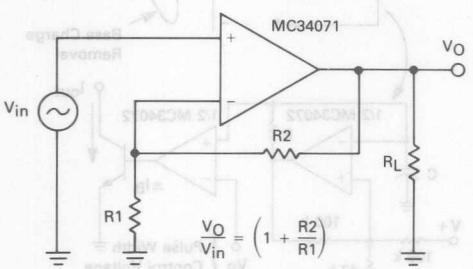
FIGURE 58 — BASIC INVERTING AMPLIFIER



$$\frac{V_O}{V_{in}} = \frac{R2}{R1} \qquad BW\ (-3.0\ dB = GBW\left[\frac{R1}{R1 + R2}\right]$$

SR = 13 V/μs

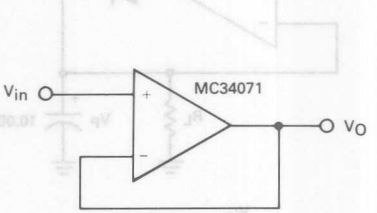
FIGURE 59 — BASIC NON INVERTING AMPLIFIER



$$\frac{V_O}{V_{in}} = \left(1 + \frac{R2}{R1}\right)$$

$$BW\ (-3.0\ dB) = GBW\left[\frac{R1}{R1 + R2}\right]$$

FIGURE 60 — UNITY GAIN BUFFER (A_V = +1.0)



BW_P = 200 kHz
V_O = 20 V_{p-p}
SR = 10 V/μs

FIGURE 61 — HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER

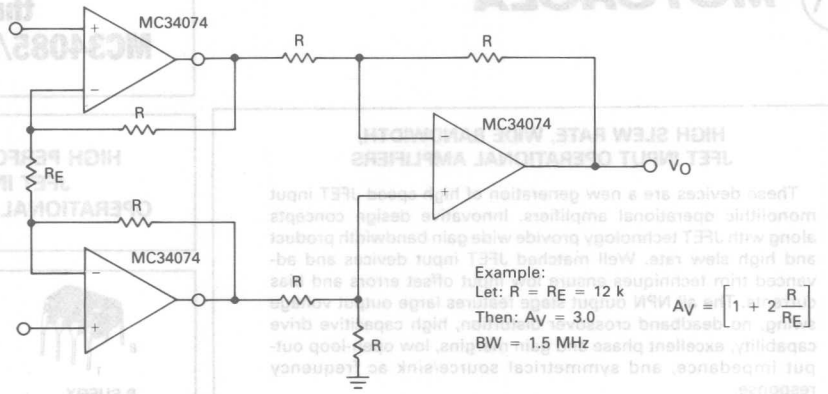
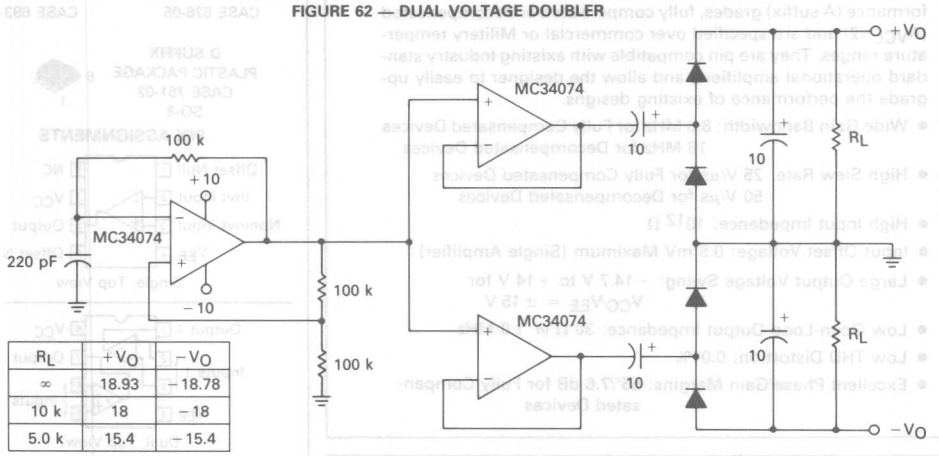


FIGURE 62 — DUAL VOLTAGE DOUBLER



R_L	+V_O	−V_O
∞	18.93	−18.78
10 k	18	−18
5.0 k	15.4	−15.4

MOTOROLA

MC34080/MC35080 thru MC34085/MC35085

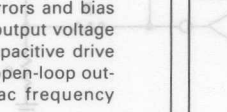
HIGH PERFORMANCE JFET INPUT OPERATIONAL AMPLIFIERS

HIGH SLEW RATE, WIDE BANDWIDTH, JFET INPUT OPERATIONAL AMPLIFIERS

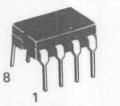
These devices are a new generation of high speed JFET input monolithic operational amplifiers. Innovative design concepts along with JFET technology provide wide gain bandwidth product and high slew rate. Well matched JFET input devices and advanced trim techniques ensure low input offset errors and bias currents. The all NPN output stage features large output voltage swing, no deadband crossover distortion, high capacitive drive capability, excellent phase and gain margins, low open-loop output impedance, and symmetrical source/sink ac frequency response.

This series of devices are available in standard or prime performance (A suffix) grades, fully compensated or decompensated ($A_{VCL} \geq 2$) and are specified over commercial or Military temperature ranges. They are pin compatible with existing Industry standard operational amplifiers, and allow the designer to easily upgrade the performance of existing designs.

- Wide Gain Bandwidth: 8.0 MHz for Fully Compensated Devices
  16 MHz for Decompensated Devices
- High Slew Rate: 25 V/μs for Fully Compensated Devices
  50 V/μs for Decompensated Devices
- High Input Impedance: 10^{12} Ω
- Input Offset Voltage: 0.5 mV Maximum (Single Amplifier)
- Large Output Voltage Swing: −14.7 V to +14 V for $V_{CC}/V_{EE} = \pm 15$ V
- Low Open-Loop Output Impedance: 30 Ω @ 1.0 MHz
- Low THD Distortion: 0.01%
- Excellent Phase/Gain Margins: 55°/7.6 dB for Fully Compensated Devices



P SUFFIX
PLASTIC PACKAGE
CASE 626-05

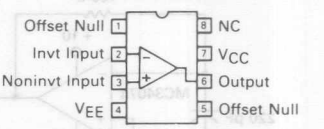


U SUFFIX
CERAMIC PACKAGE
CASE 693-02

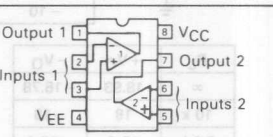
D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SO-8



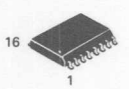
PIN ASSIGNMENTS



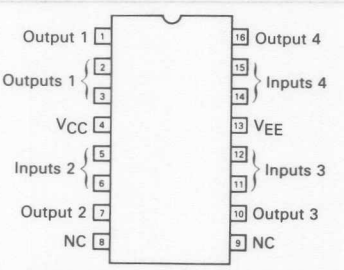
Single, Top View

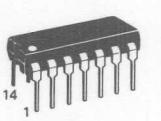


Dual, Top View

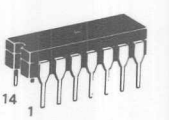


DW SUFFIX
PLASTIC PACKAGE
CASE 751G-01
SO-16L



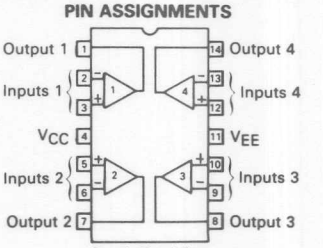


P SUFFIX
PLASTIC PACKAGE
CASE 646-06



L SUFFIX
CERAMIC PACKAGE
CASE 632-08

PIN ASSIGNMENTS



Quad, Top View

ORDERING INFORMATION

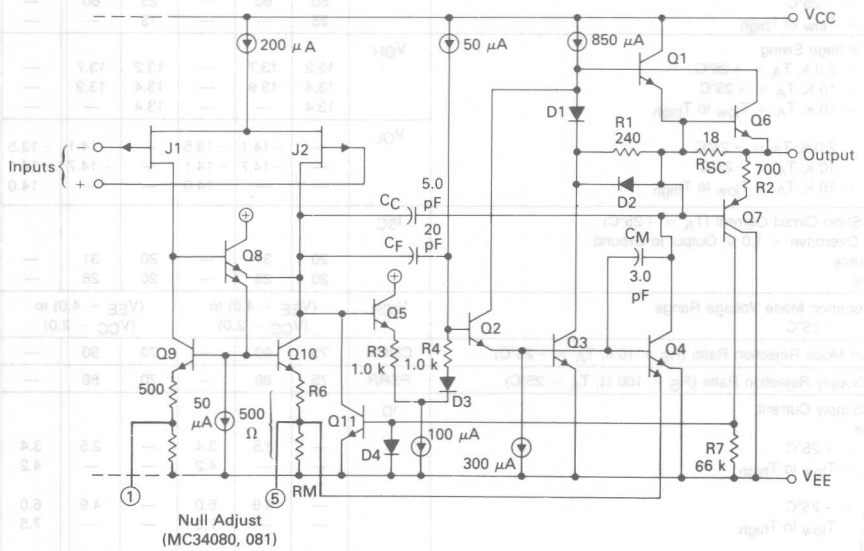
Op Amp Function	Fully Compensated	$A_{VCL} \geq 2$ Decompensated	Temperature Range	Package
Single	MC35081U,AU	MC35080U,AU	−55 to +125°C	Ceramic DIP
	MC34081D,AD	MC34080D,AD	0 to +70°C	SO-8
	MC34081P,AP	MC34080P,AP	0 to +70°C	Plastic DIP
Dual	MC34082P,AP	MC34083P,AP	0 to +70°C	Plastic DIP
Quad	MC35084L,AL	MC35085L,AL	−55 to +125°C	Ceramic DIP
	MC34084DW	MC34085DW	0 to +70°C	SO-16L
	MC34084P,AP	MC34085P,AP	0 to +70°C	Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (from V_{CC} to V_{EE})	V_S	+44	Volts
Input Differential Voltage Range	V_{IDR}	Note 1	Volts
Input Voltage Range	V_{IR}	Note 1	Volts
Output Short-Circuit Duration (Note 2)	t_S	Indefinite	Seconds
Operating Ambient Temperature Range MC35XXX MC34XXX	T_A	 −55 to +125 0 to +70	°C
Operating Junction Temperature Ceramic Package Plastic Package	T_J	 +165 +125	°C
Storage Temperature Range Ceramic Package Plastic Package	T_{stg}	 −65 to +165 −55 to +125	°C

NOTES:
1. Either or both input voltages must not exceed the magnitude of V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded.

EQUIVALENT CIRCUIT SCHEMATIC (EACH AMPLIFIER)



DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = T_{low} to T_{high} [Note 3], unless otherwise noted.)

Characteristic	Symbol	A Suffix			Non-Suffix			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 4)	V_{IO}							mV
Single								
T_A = +25°C		—	0.3	0.5	—	0.5	1.0	
T_A = 0°C to +70°C (MC34080, MC34081)		—	—	2.5	—	—	3.0	
T_A = −55°C to +125°C (MC35080, MC35081)		—	—	3.5	—	—	4.0	
Dual								
T_A = +25°C		—	0.6	1.0	—	1.0	3.0	
T_A = 0°C to +70°C (MC34082, MC34083)		—	—	3.0	—	—	5.0	
T_A = −55°C to +125°C (MC35082, MC35083)		—	—	4.0	—	—	6.0	
Quad								
T_A = +25°C		—	3.0	6.0	—	6.0	12	
T_A = 0°C to +70°C (MC34084, MC34085)		—	—	8.0	—	—	14	
T_A = −55°C to +125°C (MC35084, MC35085)		—	—	9.0	—	—	15	
Average Temperature Coefficient of Offset Voltage	$\Delta V_{IO}/\Delta T$	—	10	—	—	10	—	μV/°C
Input Bias Current (V_{CM} = 0 Note 5)	I_{IB}							nA
T_A = +25°C		—	0.06	0.2	—	0.06	0.2	
T_A = 0°C to +70°C		—	—	4.0	—	—	4.0	
T_A = −55°C to +125°C		—	—	50	—	—	50	
Input Offset Current (V_{CM} = 0 Note 5)	I_{IO}							nA
T_A = +25°C		—	0.02	0.1	—	0.02	0.1	
T_A = 0°C to +70°C		—	—	2.0	—	—	2.0	
T_A = −55°C to +125°C		—	—	25	—	—	25	
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 k)	A_{VOL}							V/mV
T_A = +25°C		50	80	—	25	80	—	
T_A = T_{low} to T_{high}		25	—	—	15	—	—	
Output Voltage Swing	V_{OH}							V
R_L = 2.0 k, T_A = +25°C		13.2	13.7	—	13.2	13.7	—	
R_L = 10 k, T_A = +25°C		13.4	13.9	—	13.4	13.9	—	
R_L = 10 k, T_A = T_{low} to T_{high}		13.4	—	—	13.4	—	—	
	V_{OL}							
R_L = 2.0 k, T_A = +25°C		—	−14.1	−13.5	—	−14.1	−13.5	
R_L = 10 k, T_A = +25°C		—	−14.7	−14.1	—	−14.7	−14.1	
R_L = 10 k, T_A = T_{low} to T_{high}		—	—	−14.0	—	—	−14.0	
Output Short-Circuit Current (T_A = +25°C)	I_{SC}							mA
Input Overdrive = 1.0 V, Output to Ground								
Source		20	31	—	20	31	—	
Sink		20	28	—	20	28	—	
Input Common Mode Voltage Range	V_{ICR}	(V_{EE} + 4.0) to (V_{CC} − 2.0)			(V_{EE} + 4.0) to (V_{CC} − 2.0)			V
T_A = +25°C								
Common Mode Rejection Ratio ($R_S \leq$ 10 k, T_A = +25°C)	CMRR	75	90	—	70	90	—	dB
Power Supply Rejection Ratio (R_S = 100 Ω, T_A = 25°C)	PSRR	75	86	—	70	86	—	dB
Power Supply Current	I_D							mA
Single								
T_A = +25°C		—	2.5	3.4	—	2.5	3.4	
T_A = T_{low} to T_{high}		—	—	4.2	—	—	4.2	
Dual								
T_A = +25°C		—	4.9	6.0	—	4.9	6.0	
T_A = T_{low} to T_{high}		—	—	7.5	—	—	7.5	
Quad								
T_A = +25°C		—	9.7	11	—	9.7	11	
T_A = T_{low} to T_{high}		—	—	13	—	—	13	

NOTES: (CONTINUED)

3. T_{low} = −55°C for MC35080,A, MC35081,A, MC35082,A, MC35083,A, MC35084,A, MC35085,A; 0°C for MC34080,A, MC34081,A, MC34082,A, MC34083,A, MC34084,A, MC34085,A. T_{high} = +125°C for MC35080,A, MC35081,A, MC35082,A, MC35083,A, MC35084,A, MC35085,A; +70°C for MC34080,A, MC34081,A, MC34082,A, MC34083,A, MC34084,A, MC34085,A.
4. See application information for typical changes in input offset voltage due to solderability and temperature cycling.
5. Limits at T_A = +25°C are guaranteed by high temperature (T_{high}) testing.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25°C unless otherwise noted)

Characteristic	Symbol	A Suffix			Non-Suffix			Unit
		Min	Typ	Max	Min	Typ	Max	
Slew Rate (V_{in} = −10 V to +10 V, R_L = 2.0 k, C_L = 100 pF)	SR							V/μs
Compensated A_V = +1.0		20	25	—	20	25	—	
A_V = −1.0		—	30	—	—	30	—	
Decompensated A_V = +2.0		40	50	—	40	50	—	
A_V = −1.0		—	50	—	—	50	—	
Settling Time (10 V Step, A_V = −1.0)	t_s							μs
To 0.10% (± ½ LSB of 9-Bits)		—	0.72	—	—	0.72	—	
To 0.01% (± ½ LSB of 12-Bits)		—	1.6	—	—	1.6	—	
Gain Bandwidth Product (f = 200 kHz)	GBW							MHz
Compensated		6.0	8.0	—	6.0	8.0	—	
Decompensated		12	16	—	12	16	—	
Power Bandwidth (R_L = 2.0 k, V_O = 20 V_{p-p}, THD = 5.0%)	BWp							kHz
Compensated A_V = +1.0		—	400	—	—	400	—	
Decompensated A_V = −1.0		—	800	—	—	800	—	
Phase Margin (Compensated)	ϕm							Degrees
R_L = 2.0 k		—	55	—	—	55	—	
R_L = 2.0 k, C_L = 100 pF		—	39	—	—	39	—	
Gain Margin (Compensated)	A_m							dB
R_L = 2.0 k		—	7.6	—	—	7.6	—	
R_L = 2.0 k, C_L = 100 pF		—	4.5	—	—	4.5	—	
Equivalent Input Noise Voltage R_S = 100 Ω, f = 1.0 kHz	e_n	—	30	—	—	30	—	$\frac{nV}{\sqrt{Hz}}$
Equivalent Input Noise Current (f = 1.0 kHz)	I_n	—	0.01	—	—	0.01	—	$\frac{pA}{\sqrt{Hz}}$
Input Capacitance	C_i	—	5.0	—	—	5.0	—	pF
Input Resistance	r_i	—	10^{12}	—	—	10^{12}	—	Ω
Total Harmonic Distortion A_V = +10, R_L = 2.0 k, 2.0 ≤ V_O ≤ 20 V_{p-p}, f = 10 kHz	THD	—	0.05	—	—	0.05	—	%
Channel Separation (f = 10 kHz)	—	—	120	—	—	120	—	dB
Open-Loop Output Impedance (f = 1.0 MHz)	z_o	—	35	—	—	35	—	Ω

TYPICAL PERFORMANCE CURVES

FIGURE 1 — INPUT COMMON MODE VOLTAGE RANGE versus TEMPERATURE

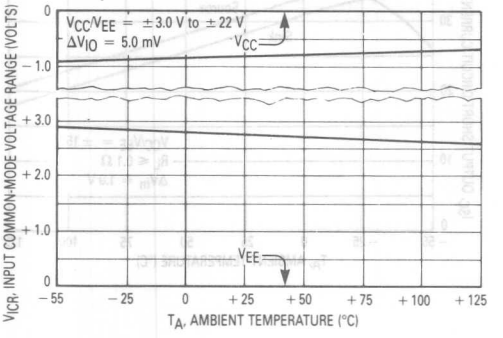
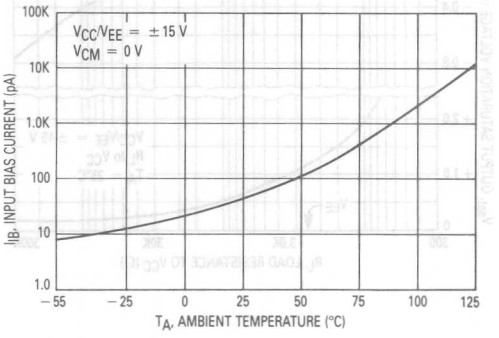


FIGURE 2 — INPUT BIAS CURRENT versus TEMPERATURE



2

FIGURE 3 — INPUT BIAS CURRENT versus INPUT COMMON-MODE VOLTAGE

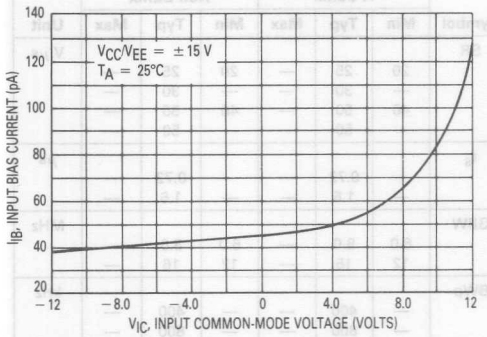


FIGURE 4 — OUTPUT VOLTAGE SWING versus SUPPLY VOLTAGE

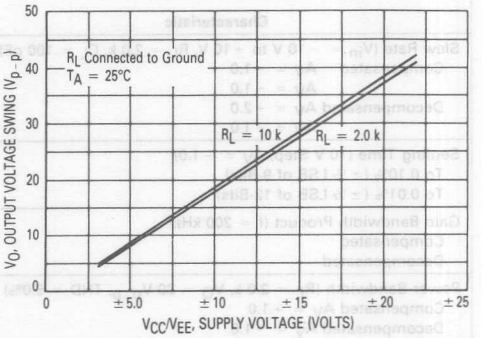


FIGURE 5 — OUTPUT SATURATION versus LOAD CURRENT

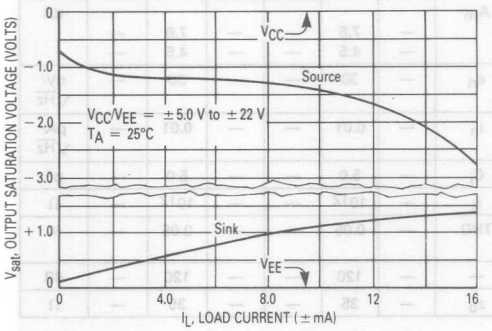


FIGURE 6 — OUTPUT SATURATION versus LOAD RESISTANCE TO GROUND

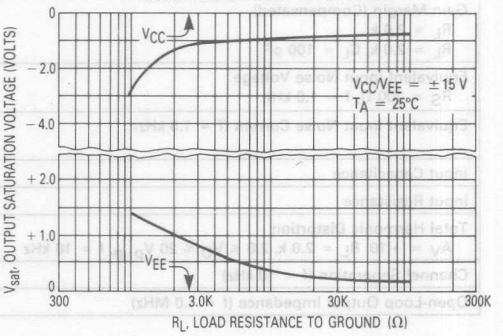


FIGURE 7 — OUTPUT SATURATION versus LOAD RESISTANCE TO V_{CC}

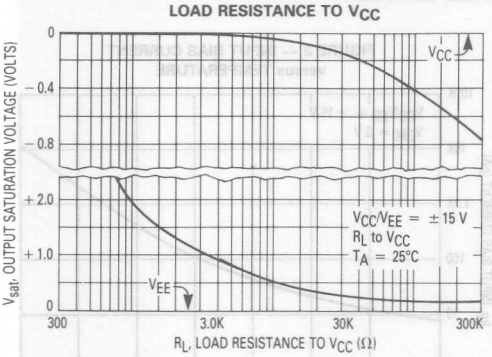


FIGURE 8 — OUTPUT SHORT CIRCUIT CURRENT versus TEMPERATURE

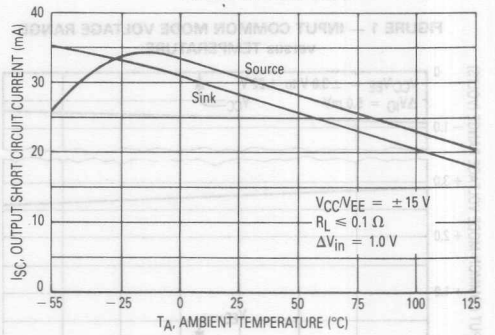


FIGURE 9 — OUTPUT IMPEDANCE versus FREQUENCY

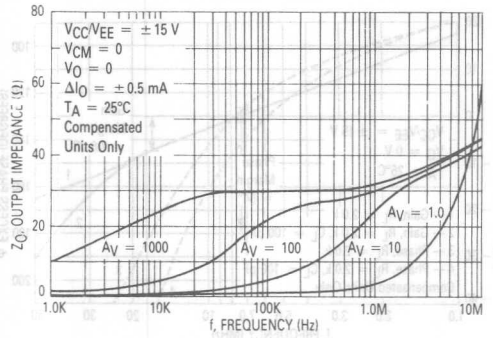


FIGURE 10 — OUTPUT IMPEDANCE versus FREQUENCY

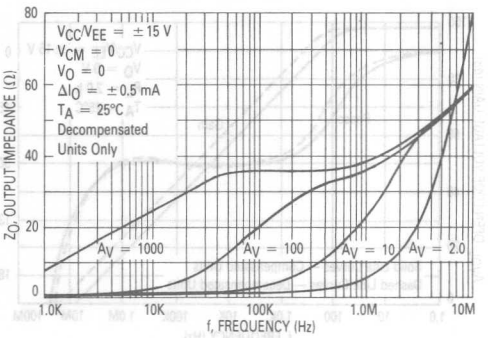


FIGURE 11 — OUTPUT VOLTAGE SWING versus FREQUENCY

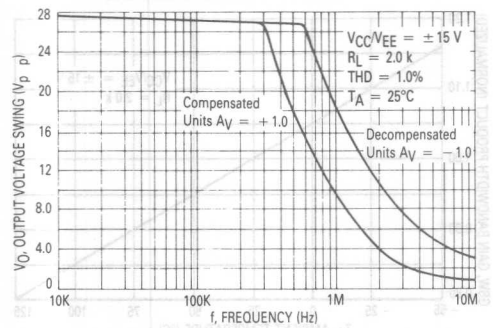


FIGURE 12 — OUTPUT DISTORTION versus FREQUENCY

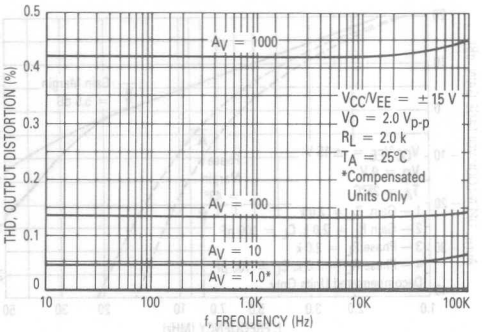


FIGURE 13 — OPEN-LOOP VOLTAGE GAIN versus TEMPERATURE

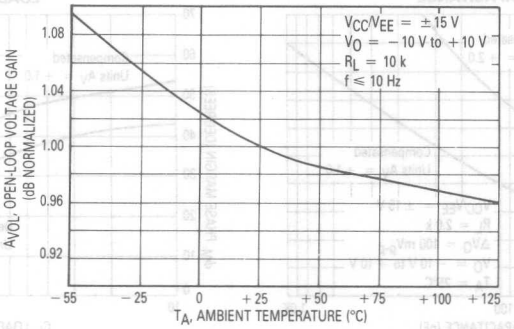


FIGURE 14 — OPEN-LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY

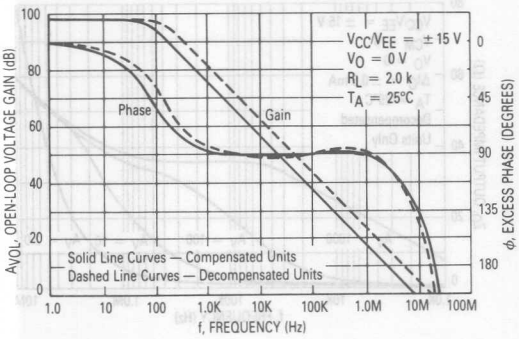


FIGURE 15 — OPEN-LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY

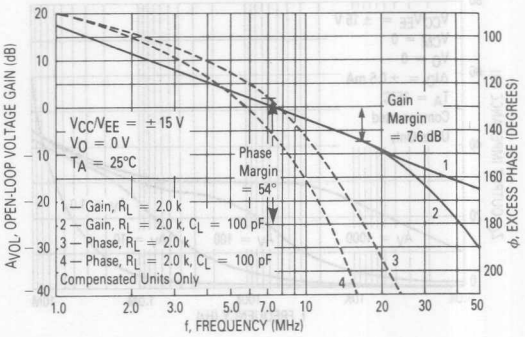


FIGURE 16 — OPEN-LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY

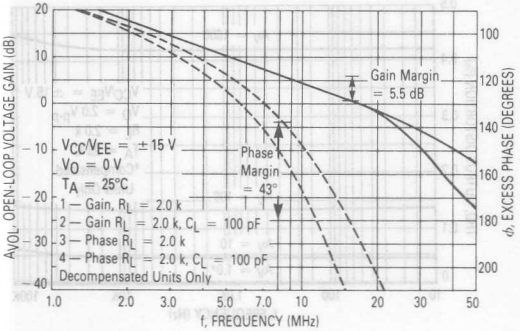


FIGURE 17 — NORMALIZED GAIN BANDWIDTH PRODUCT versus TEMPERATURE

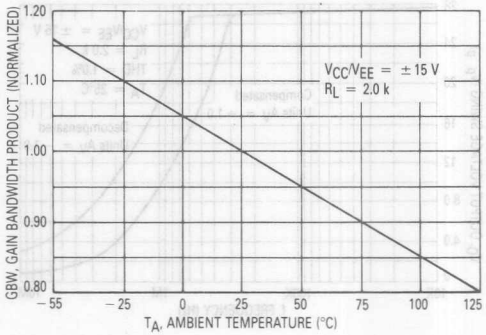


FIGURE 18 — PERCENT OVERSHOOT versus LOAD CAPACITANCE

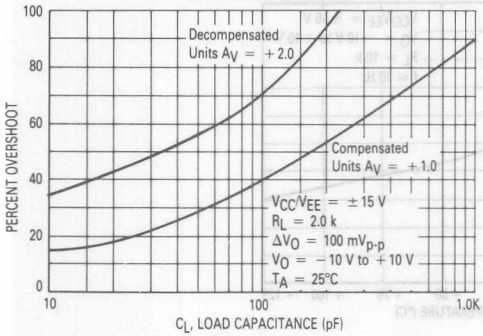


FIGURE 19 — PHASE MARGIN versus LOAD CAPACITANCE

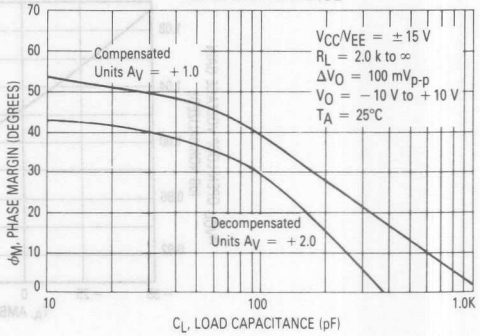


FIGURE 20 — GAIN MARGIN versus LOAD CAPACITANCE

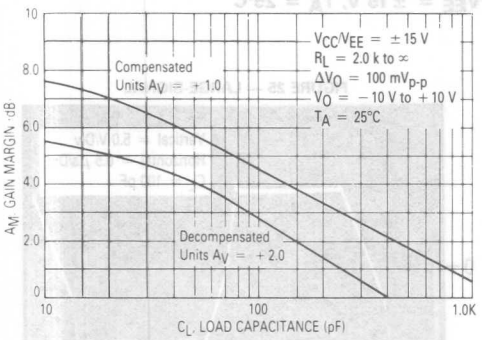


FIGURE 21 — PHASE MARGIN versus TEMPERATURE

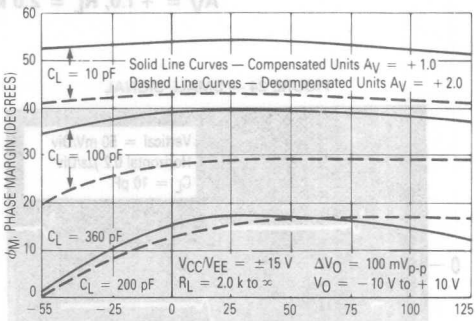


FIGURE 22 — GAIN MARGIN versus TEMPERATURE

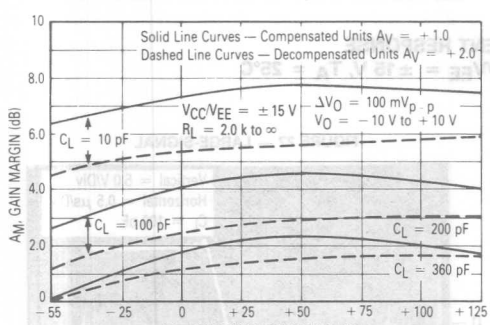
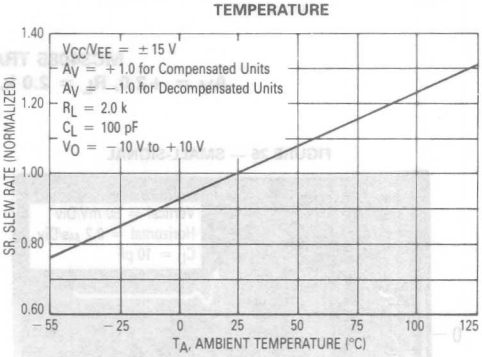


FIGURE 23 — NORMALIZED SLEW RATE versus TEMPERATURE



2

MC34084 TRANSIENT RESPONSE

$A_V = +1.0$, $R_L = 2.0$ k, $V_{CC}/V_{EE} = \pm 15$ V, $T_A = 25°C$

FIGURE 24 — SMALL-SIGNAL

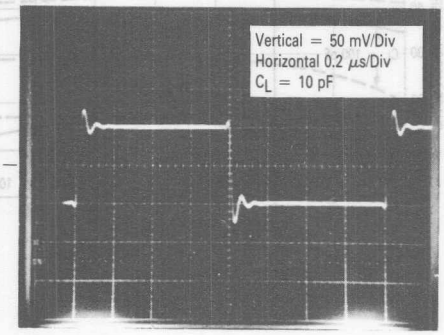
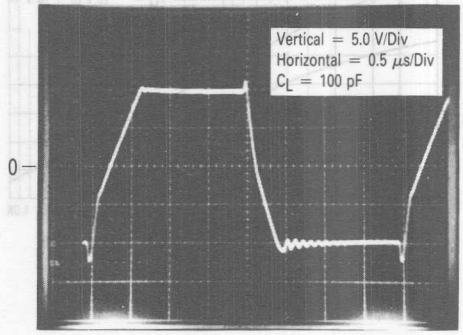


FIGURE 25 — LARGE-SIGNAL



MC34085 TRANSIENT RESPONSE

$A_V = +2.0$, $R_L = 2.0$ k, $V_{CC}/V_{EE} = \pm 15$ V, $T_A = 25°C$

FIGURE 26 — SMALL-SIGNAL

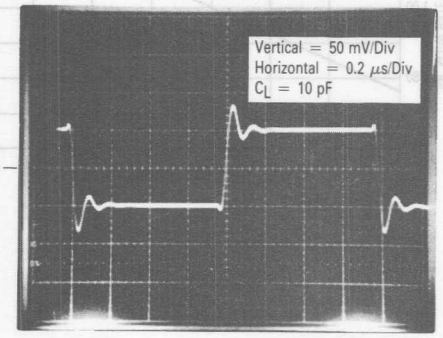


FIGURE 27 — LARGE-SIGNAL

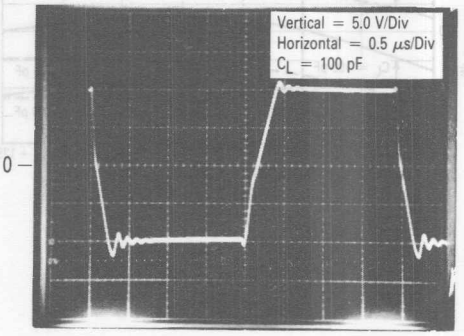


FIGURE 28 — COMMON-MODE REJECTION RATIO versus FREQUENCY

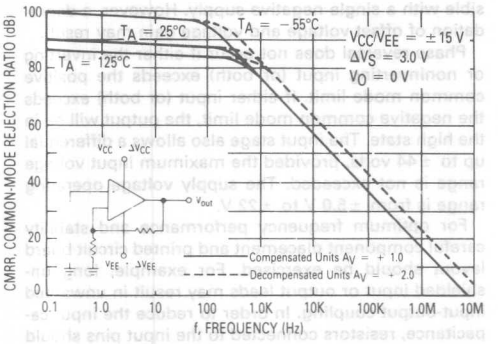


FIGURE 29 — POWER SUPPLY REJECTION RATIO versus FREQUENCY

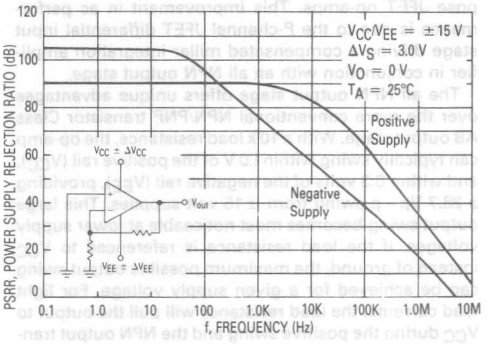


FIGURE 30 — POWER SUPPLY REJECTION RATIO versus TEMPERATURE

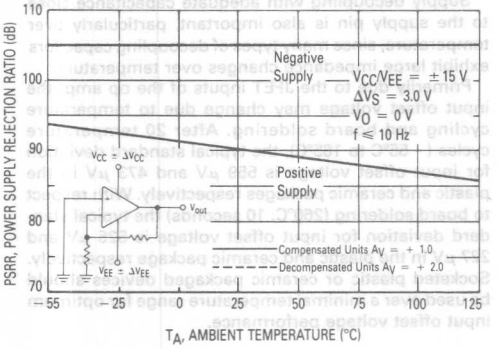


FIGURE 31 — NORMALIZED SUPPLY CURRENT versus SUPPLY VOLTAGE

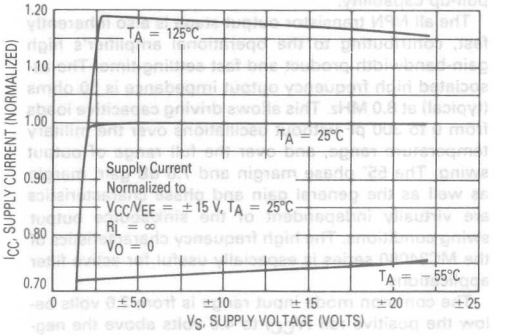


FIGURE 32 — CHANNEL SEPARATION versus FREQUENCY

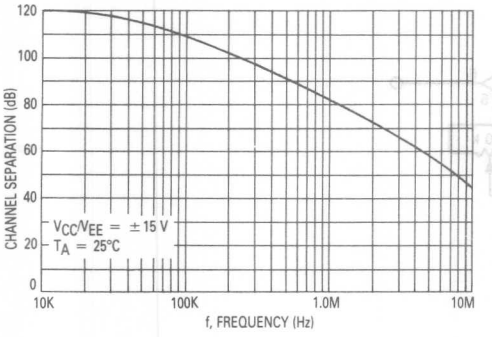
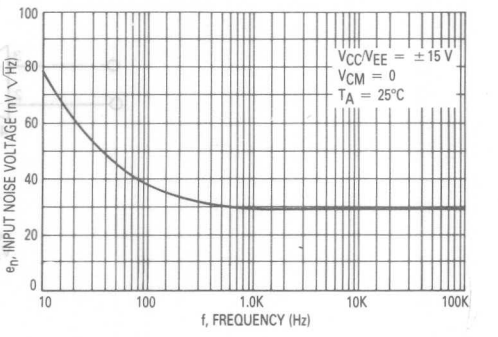


FIGURE 33 — SPECTRAL NOISE DENSITY



APPLICATIONS INFORMATION

The bandwidth and slew rate of the MC34080 series is nearly double that of currently available general purpose JFET op-amps. This improvement in ac performance is due to the P-channel JFET differential input stage driving a compensated miller integration amplifier in conjunction with an all NPN output stage.

The all NPN output stage offers unique advantages over the more conventional NPN/PNP transistor Class AB output stage. With a 10 k load resistance, the op-amp can typically swing within I.0 V of the positive rail (V_{CC}), and within 0.3 volts of the negative rail (V_{EE}), providing a 28.7 Vp−p swing from ±15 volt supplies. This large output swing becomes most noticeable at lower supply voltages. If the load resistance is referenced to V_{CC} instead of ground, the maximum possible output swing can be achieved for a given supply voltage. For light load currents, the load resistance will pull the output to V_{CC} during the positive swing and the NPN output transistor will pull the output very near V_{EE} during the negative swing. The load resistance value should be much less than that of the feedback resistance to maximize pull-up capability.

The all NPN transistor output stage is also inherently fast, contributing to the operational amplifier's high gain-bandwidth product and fast settling time. The associated high frequency output impedance is 50 ohms (typical) at 8.0 MHz. This allows driving capacitive loads from 0 to 300 pF without oscillations over the military temperature range, and over the full range of output swing. The 55° phase margin and 7.6 dB gain margin as well as the general gain and phase characteristics are virtually independent of the sink/source output swing conditions. The high frequency characteristics of the MC34080 series is especially useful for active filter applications.

The common mode input range is from 2.0 volts below the positive rail (V_{CC}) to 4.0 volts above the negative rail (V_{EE}). The amplifier remains active if the inputs are biased at the positive rail. This may be useful for some applications in that single supply operation is possible with a single negative supply. However, a degradation of offset voltage and voltage gain may result.

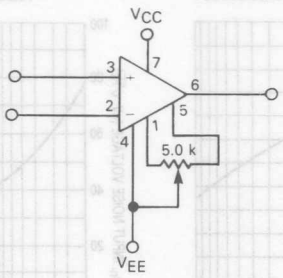
Phase reversal does not occur if either the inverting or noninverting input (or both) exceeds the positive common mode limit. If either input (or both) exceeds the negative common mode limit, the output will be in the high state. The input stage also allows a differential up to ±44 volts, provided the maximum input voltage range is not exceeded. The supply voltage operating range is from ±5.0 V to ±22 V.

For optimum frequency performance and stability careful component placement and printed circuit board layout should be exercised. For example, long unshielded input or output leads may result in unwanted input-output coupling. In order to reduce the input capacitance, resistors connected to the input pins should be physically close to these pins. This not only minimizes the input pole for optimum frequency response, but also minimizes extraneous "pickup" at this node.

Supply decoupling with adequate capacitance close to the supply pin is also important, particularly over temperature, since many types of decoupling capacitors exhibit large impedance changes over temperature.

Primarily due to the JFET inputs of the op amp, the input offset voltage may change due to temperature cycling and board soldering. After 20 temperature cycles (−55°C to 165°C), the typical standard deviation for input offset voltage is 559 μV and 473 μV in the plastic and ceramic packages respectively. With respect to board soldering (260°C, 10 seconds) the typical standard deviation for input offset voltage is 525 μV and 227 μV in the plastic and ceramic package respectively. Socketed plastic or ceramic packaged devices should be used over a minimal temperature range for optimum input offset voltage performance.

FIGURE 34 — OFFSET NULLING CIRCUIT



MOTOROLA

MC34181,2,4
MC35181,2,4
MC33181,2,4

LOW POWER, HIGH SLEW RATE, WIDE BANDWIDTH, JFET INPUT OPERATIONAL AMPLIFIERS

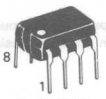
Quality bipolar fabrication with innovative design concepts are employed for the MC33181/2/4, MC34181/2/4, MC35181/2/4 series of monolithic operational amplifiers. This JFET input series of operational amplifiers operate at 210 μA per amplifier and offer 4.0 MHz of gain bandwidth product and 10 V/μs slew rate. Precision matching and an innovative trim technique of the single and dual versions provide low input offset voltages. With a JFET input stage, this series exhibits high input resistance, low input offset voltage and high gain. The all NPN output stage, characterized by no deadband crossover distortion and large output voltage swing, provides high capacitance drive capability, excellent phase and gain margins, low open-loop high frequency output impedance and symmetrical source/sink ac frequency response.

The MC33181/2/4, MC34181/2/4, MC35181/2/4 series of devices are specified over the commercial, industrial/vehicular or military temperature ranges. The complete series of single, dual and quad operational amplifiers are available in the plastic and ceramic DIP as well as the SOIC surface mount packages.

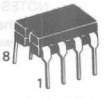
- Low Supply Current: 210 μA (Per Amplifier)
- Wide Supply Operating Range: ±1.5 V to ±18 V
- Wide Bandwidth: 4.0 MHz
- High Slew Rate: 10 V/μs
- Low Input Offset Voltage: 2.0 mV
- Large Output Voltage Swing: −14 V to +14 V (with ±15 V Supplies)
- Large Capacitance Drive Capability: 0 to 500 pF
- Low Total Harmonic Distortion: 0.04%
- Excellent Phase Margin: 67°
- Excellent Gain Margin: 6.7 dB
- Output Short Circuit Protection

LOW POWER JFET INPUT OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUITS



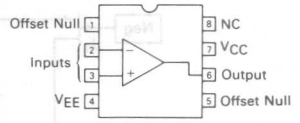
P SUFFIX
PLASTIC PACKAGE
CASE 626-05



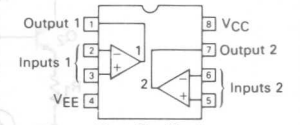
U SUFFIX
CERAMIC PACKAGE
CASE 693-02



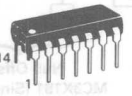
D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SO-8



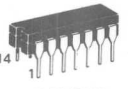
(Single, Top View)



(Dual, Top View)



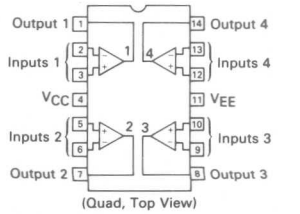
P SUFFIX
PLASTIC PACKAGE
CASE 646-06



L SUFFIX
CERAMIC PACKAGE
CASE 632-08



D SUFFIX
PLASTIC PACKAGE
CASE 751A-02
SO-14



(Quad, Top View)

ORDERING INFORMATION

Op Amp Function	Device	Test Temperature Range	Package
Single	MC34181P	0 to +70°C	Plastic DIP
	MC34181D	0 to +70°C	SO-8
	MC33181P	−40 to +85°C	Plastic DIP
	MC33181D	−40 to +85°C	SO-8
	MC35181U	−55 to +125°C	Ceramic DIP
Dual	MC34182P	0 to +70°C	Plastic DIP
	MC34182D	0 to +70°C	SO-8
	MC33182P	−40 to +85°C	Plastic DIP
	MC33182D	−40 to +85°C	SO-8
	MC35182U	−55 to +125°C	Ceramic DIP
Quad	MC34184P	0 to +70°C	Plastic DIP
	MC34184D	0 to +70°C	SO-14
	MC33184P	−40 to +85°C	Plastic DIP
	MC33184D	−40 to +85°C	SO-14
	MC35184L	−55 to +125°C	Ceramic DIP

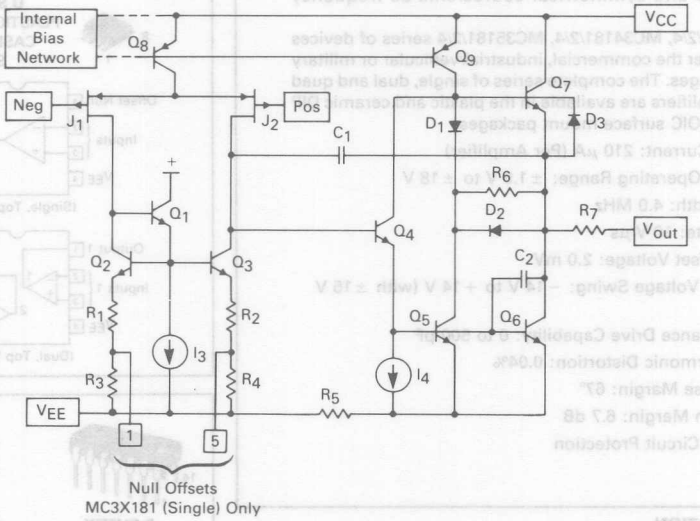
2

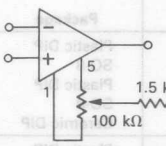
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (from V_{CC} to V_{EE})	V_S	+36	Volts
Input Differential Voltage Range	V_{IDR}	Note 1	Volts
Input Voltage Range	V_{IR}	Note 1	Volts
Output Short-Circuit Duration (Note 2)	t_S	Indefinite	Seconds
Operating Junction Temperature Ceramic Package Plastic Package	T_J	 +160 +150	°C
Storage Temperature Range Ceramic Package Plastic Package	T_{stg}	 −65 to +160 −60 to +150	°C

NOTES:
1. Either or both input voltages must not exceed the magnitude of V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (see Figure 1).

EQUIVALENT CIRCUIT SCHEMATIC (EACH AMPLIFIER)





MC3X181 Input Offset Voltage Null Circuit

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 50 Ω, V_O = 0 V)	V_{IO}				mV
Single					
T_A = +25°C		—	0.5	2.0	
T_A = 0°C to +70°C (MC34181)		—	—	3.0	
T_A = −40°C to +85°C (MC33181)		—	—	3.5	
T_A = −55°C to +125°C (MC35181)		—	—	4.5	
Dual					
T_A = +25°C		—	1.0	3.0	
T_A = 0°C to +70°C (MC34182)		—	—	4.0	
T_A = −40°C to +85°C (MC33182)		—	—	4.5	
T_A = −55°C to +125°C (MC35182)		—	—	5.5	
Quad					
T_A = +25°C		—	4.0	10	
T_A = 0°C to +70°C (MC34184)		—	—	11	
T_A = −40°C to +85°C (MC33184)		—	—	11.5	
T_A = −55°C to +125°C (MC35184)		—	—	12.5	
Average Temperature Coefficient of V_{IO} (R_S = 50 Ω, V_O = 0 V)	$\Delta V_{IO}/\Delta T$	—	10	—	μV/°C
Input Offset Current (V_{CM} = 0 V, V_O = 0 V)	I_{IO}				nA
T_A = +25°C		—	0.001	0.05	
T_A = 0°C to +70°C		—	—	1.0	
T_A = −40°C to +85°C		—	—	2.0	
T_A = −55°C to +125°C		—	—	13	
Input Bias Current (V_{CM} = 0 V, V_O = 0 V)	I_{IB}				nA
T_A = +25°C		—	0.003	0.1	
T_A = 0°C to +70°C		—	—	2.0	
T_A = −40°C to +85°C		—	—	4.0	
T_A = −55°C to +125°C		—	—	25	
Input Common Mode Voltage Range	V_{ICR}	(V_{EE} + 4.0 V) to (V_{CC} − 2.0 V)			V
Large Signal Voltage Gain (R_L = 10 kΩ, V_O = ±10 V)	A_{VOL}				V/mV
T_A = +25°C		25	60	—	
T_A = T_{low} to T_{high}		15	—	—	
Output Voltage Swing (V_{ID} = 1.0 V, R_L = 10 kΩ)	V_O+	+13.5	+14	—	V
T_A = +25°C	V_O-	—	−14	−13.5	
Common Mode Rejection (R_S = 50 Ω, V_{CM} = V_{ICR}, V_O = 0 V)	CMR	70	86	—	dB
Power Supply Rejection (R_S = 50 Ω, V_{CM} = 0 V, V_O = 0 V)	PSR	70	84	—	dB
Output Short Circuit Current (V_{ID} = 1.0 V, Output to Ground)	I_{SC}				mA
Source		3.0	8.0	—	
Sink		8.0	11	—	
Power Supply Current (No Load, V_O = 0 V)	I_D				μA
Single					
T_A = +25°C		—	210	250	
T_A = T_{low} to T_{high}		—	—	250	
Dual					
T_A = +25°C		—	420	500	
T_A = T_{low} to T_{high}		—	—	500	
Quad					
T_A = +25°C		—	840	1000	
T_A = T_{low} to T_{high}		—	—	1000	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = −10 V to +10 V, R_L = 10 kΩ, C_L = 100 pF) A_V = +1.0 A_V = −1.0	SR	 7.0 —	 10 10	 — —	V/μs
Settling Time (A_V = −1.0, R_L = 10 kΩ, V_O = 0 V to +10 V Step) To Within 0.10% To Within 0.01%	t_s	 — —	 1.1 1.5	 — —	μs
Gain Bandwidth Product (f = 100 kHz)	GBW	3.0	4.0	—	MHz
Power Bandwidth (A_V = +1.0, R_L = 10 kΩ, V_O = 20 V_{p-p}, THD = 5%)	BW_p	—	200	—	kHz
Phase Margin (−10 V < V_O < +10 V) R_L = 10 kΩ R_L = 10 kΩ, C_L = 100 pF	$Ø_m$	 — —	 67 34	 — —	Degrees
Gain Margin (−10 V < V_O < +10 V) R_L = 10 kΩ R_L = 10 kΩ, C_L = 100 pF	A_m	 — —	 6.7 3.4	 — —	dB
Equivalent Input Noise Voltage R_S = 100 Ω, f = 1.0 kHz	e_n	—	38	—	nV/√Hz
Equivalent Input Noise Current f = 1.0 kHz	i_n	—	0.01	—	pA/√Hz
Differential Input Capacitance	C_i	—	3.0	—	pF
Differential Input Resistance	R_i	—	10^{12}	—	Ω
Total Harmonic Distortion A_V = 10, R_L = 10 kΩ, 2 V_{p-p} < V_O < 20 V_{p-p}, f = 10 kHz	THD	—	0.04	—	%
Channel Separation (R_L = 10 kΩ, −10 V < V_O < +10 V, 0 Hz < f < 10 kHz)	—	—	120	—	dB
Open-Loop Output Impedance (f = 1.0 MHz)	$\|Z_o\|$	—	200	—	Ω

FIGURE 1 — MAXIMUM POWER DISSIPATION versus TEMPERATURE FOR PACKAGE VARIATIONS

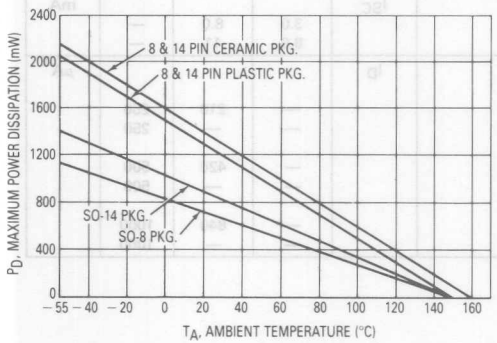


FIGURE 2 — INPUT COMMON-MODE VOLTAGE RANGE versus TEMPERATURE

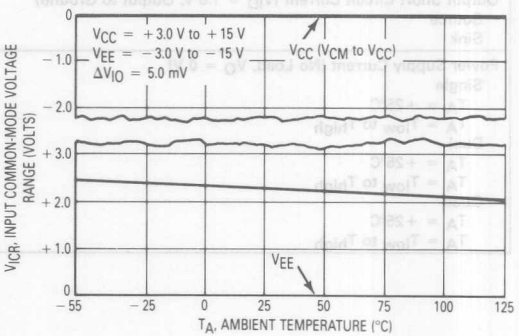


FIGURE 3 — INPUT BIAS CURRENT versus TEMPERATURE

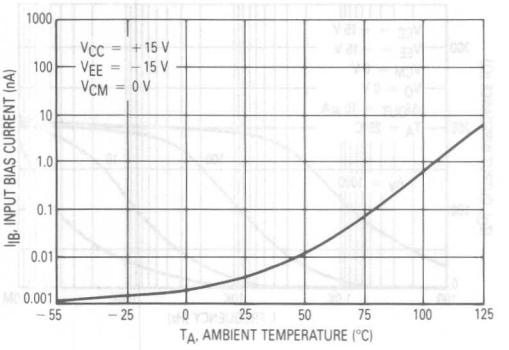


FIGURE 4 — INPUT BIAS CURRENT versus INPUT COMMON-MODE VOLTAGE

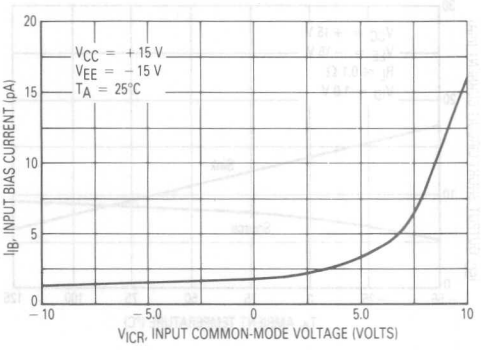


FIGURE 5 — OUTPUT VOLTAGE SWING versus SUPPLY VOLTAGE

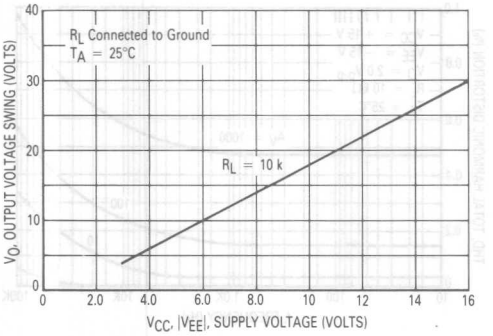


FIGURE 6 — OUTPUT SATURATION VOLTAGE versus LOAD CURRENT

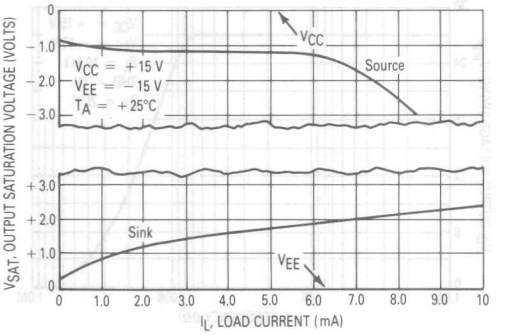


FIGURE 7 — OUTPUT SATURATION VOLTAGE versus LOAD RESISTANCE TO GROUND

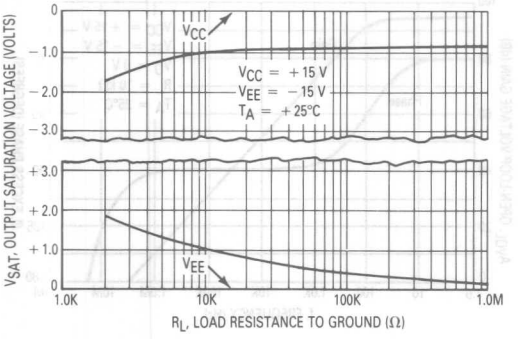
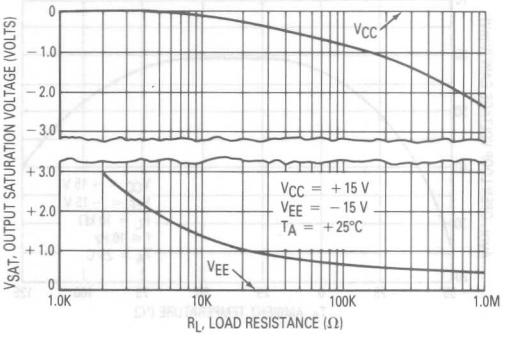


FIGURE 8 — OUTPUT SATURATION VOLTAGE versus LOAD RESISTANCE TO V_{CC}



2

FIGURE 9 — OUTPUT SHORT CIRCUIT CURRENT versus TEMPERATURE

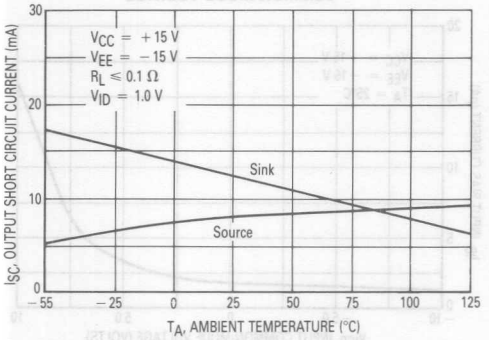


FIGURE 10 — OUTPUT IMPEDANCE versus FREQUENCY

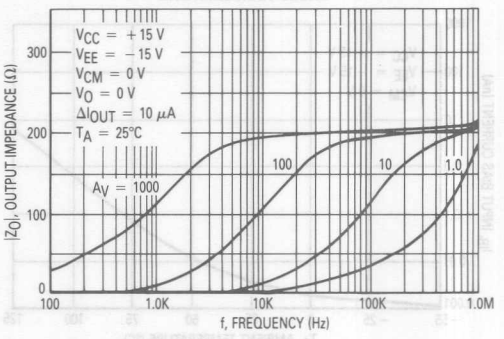


FIGURE 11 — OUTPUT VOLTAGE SWING versus FREQUENCY

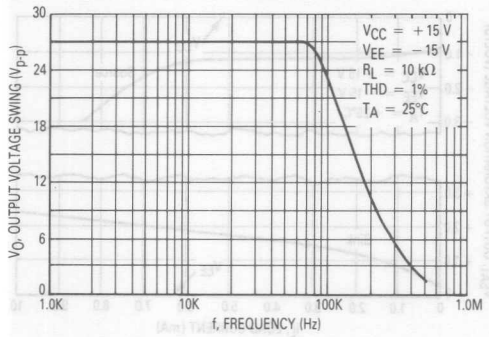


FIGURE 12 — OUTPUT DISTORTION versus FREQUENCY

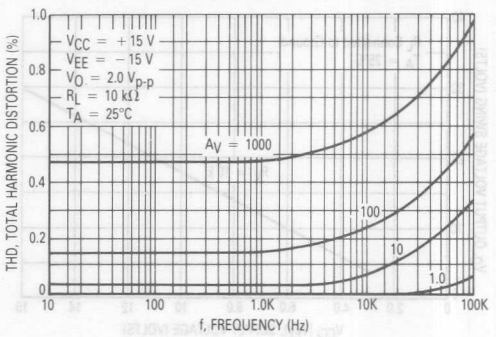


FIGURE 13 — OPEN-LOOP VOLTAGE GAIN versus TEMPERATURE

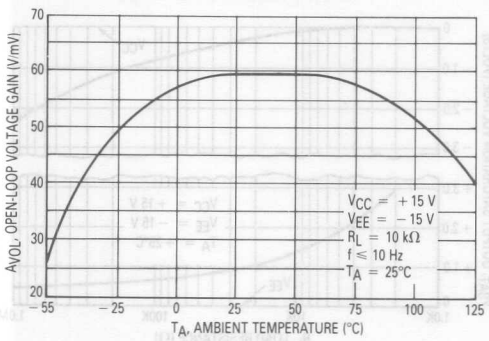


FIGURE 14 — OPEN-LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY

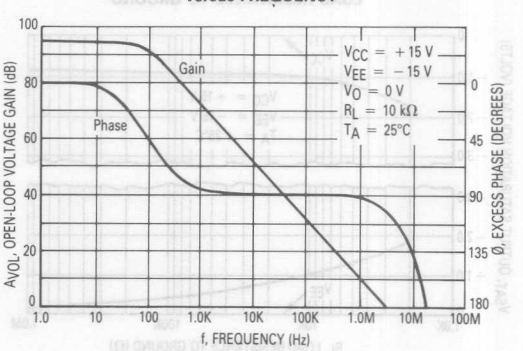


FIGURE 15 — NORMALIZED GAIN BANDWIDTH PRODUCT versus TEMPERATURE

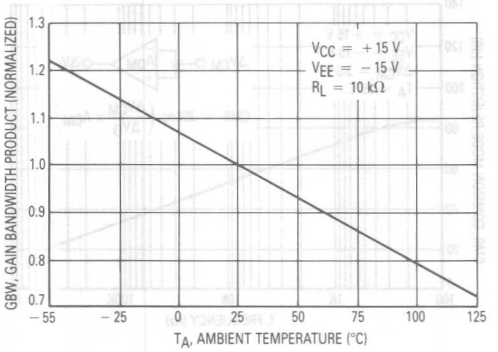


FIGURE 16 — OUTPUT VOLTAGE OVERSHOOT versus LOAD CAPACITANCE

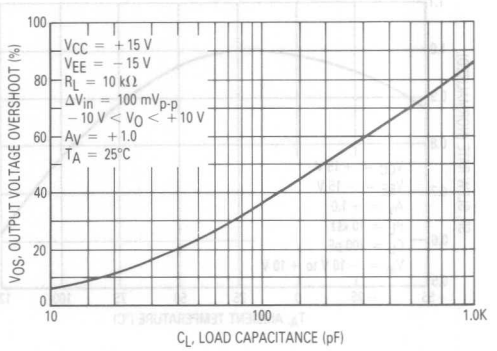


FIGURE 17 — PHASE MARGIN versus LOAD CAPACITANCE

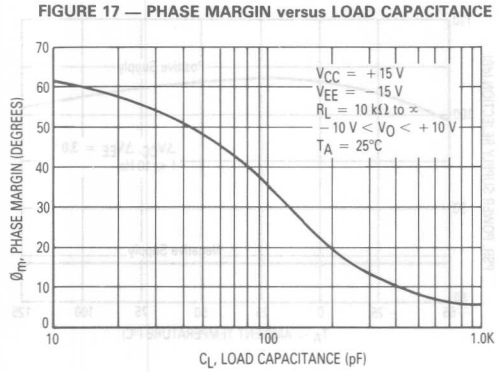


FIGURE 18 — GAIN MARGIN versus LOAD CAPACITANCE

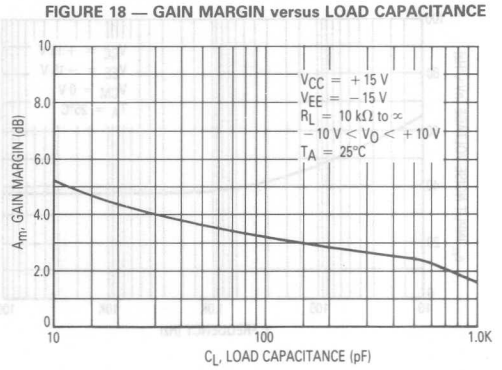


FIGURE 19 — PHASE MARGIN versus TEMPERATURE

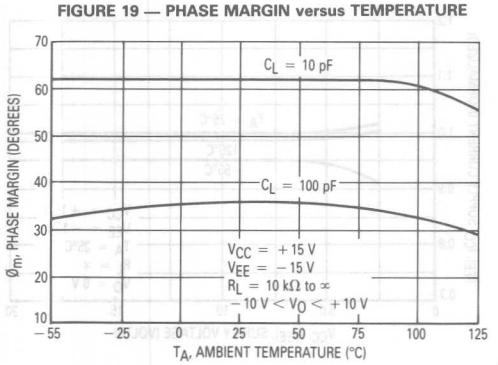
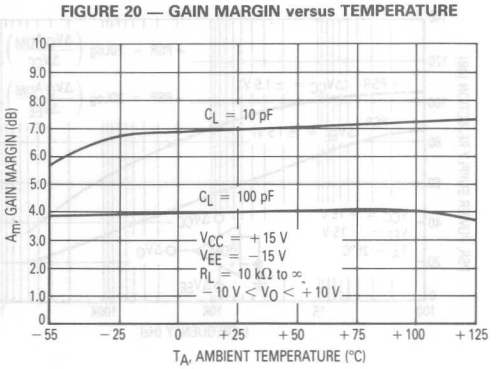


FIGURE 20 — GAIN MARGIN versus TEMPERATURE



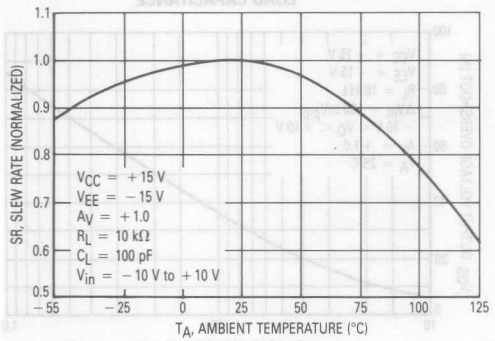


FIGURE 23 — INPUT NOISE VOLTAGE versus FREQUENCY

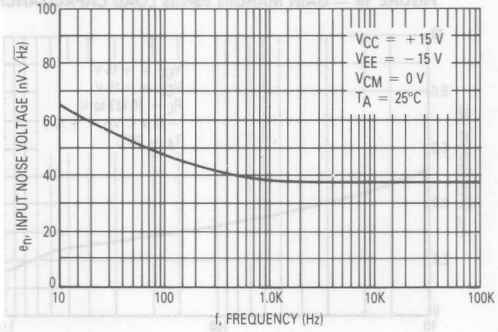
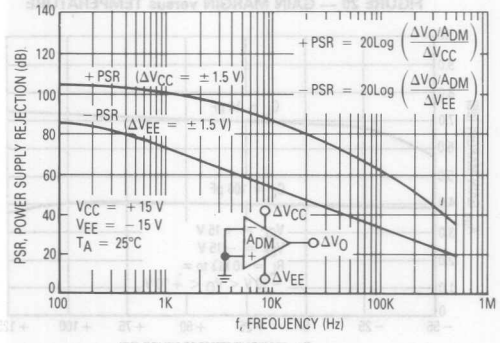


FIGURE 25 — POWER SUPPLY REJECTION versus FREQUENCY



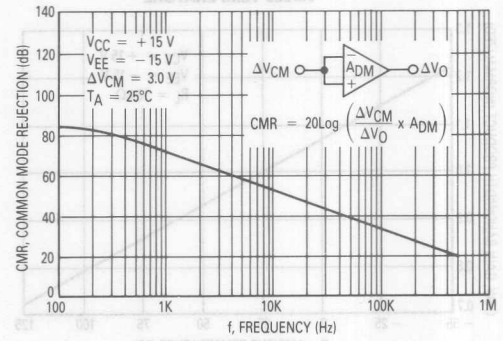


FIGURE 24 — POWER SUPPLY REJECTION versus TEMPERATURE

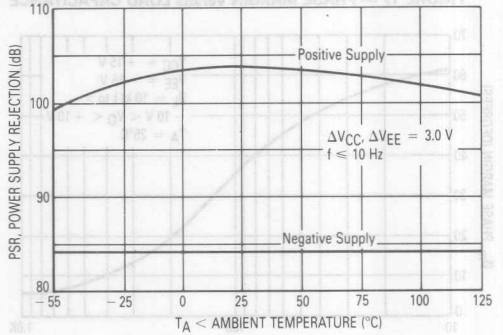


FIGURE 26 — NORMALIZED SUPPLY CURRENT versus SUPPLY VOLTAGE

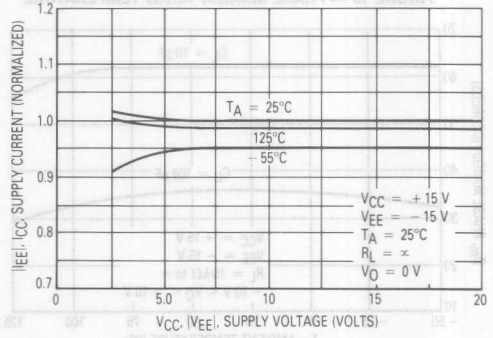


FIGURE 27 — CHANNEL SEPARATION versus FREQUENCY

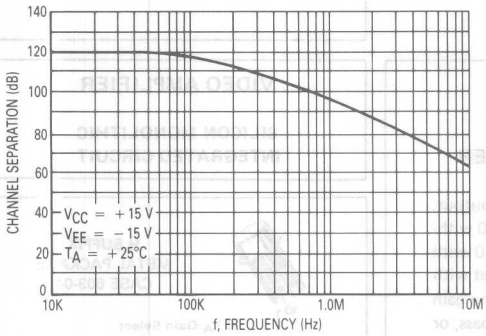


FIGURE 28 — TRANSIENT RESPONSE

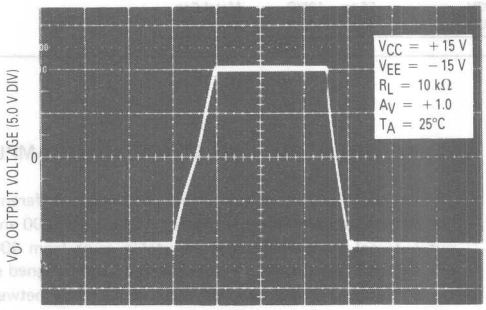
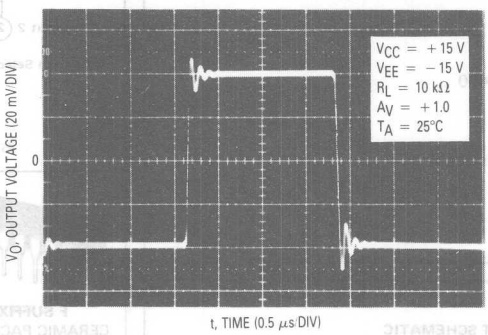


FIGURE 29 — SMALL SIGNAL TRANSIENT RESPONSE



ORDERING INFORMATION

Device	Temperature Range	Package
NE592D	0 to 70°C	SO-14
NE592N	0 to 70°C	Plastic DIP
NE592H	0 to 70°C	Metal Can
NE592F	0 to 70°C	Ceramic DIP
SE592H	−55 to +125°C	Metal Can
SE592F	−55 to +125°C	Ceramic DIP

NE592
SE592

VIDEO AMPLIFIER

SILICON MONOLITHIC
INTEGRATED CIRCUIT

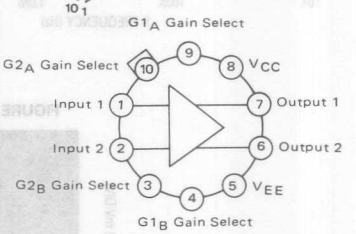
DIFFERENTIAL TWO STAGE VIDEO AMPLIFIER

The SE/NE592 is a monolithic, two stage, differential output, wideband video amplifier. It offers fixed gains of 100 and 400 without external components and adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high pass, low pass, or band pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display and video recorder systems. The 592 is a pin-for-pin replacement for the MC1733.

- 90 MHz Bandwidth
- Adjustable Gains From 0 to 400
- Adjustable Pass Band
- No Frequency Compensation Required

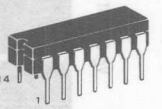


H SUFFIX
METAL PACKAGE
CASE 603-04

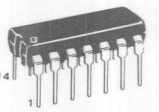


(Top View)

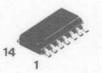
Pin 5 connected to case



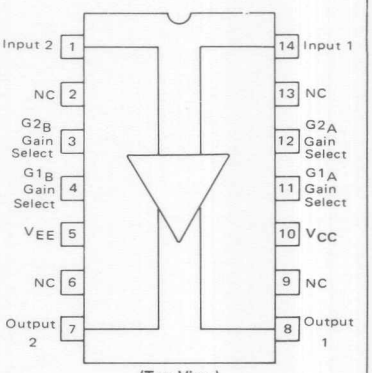
F SUFFIX
CERAMIC PACKAGE
CASE 632-10



N SUFFIX
PLASTIC PACKAGE
CASE 646-06

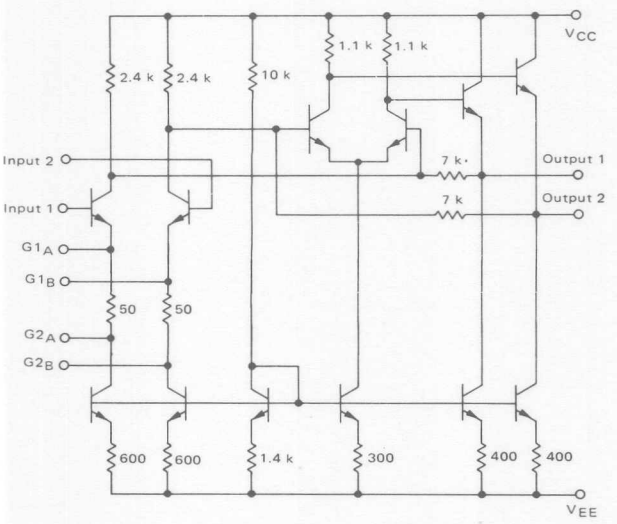


D SUFFIX
PLASTIC PACKAGE
CASE 751A-02
SO-14



(Top View)

CIRCUIT SCHEMATIC



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+8.0 −8.0	Volts
Differential Input Voltages	V_{ID}	±5.0	Volts
Common-Mode Input Voltage	V_{IC}	±6.0	Volts
Output Current	I_o	10	mA
Operating Ambient Temperature Range SE592 NE592	T_A	 −55 to +125 0 to +70	°C
Operating Junction Temperature Range Metal and Ceramic Packages Plastic Package	T_J	 175 150	°C
Storage Temperature Range Metal and Ceramic Packagee Plastic Package	T_{stg}	 −65 to +150 −55 to +125	°C

ELECTRICAL CHARACTERISTICS T_A = 25°C unless otherwise noted. (V_{CC} = +6.0 V, V_{EE} = −6.0 V, V_{CM} = 0)

Characteristic	Symbol	SE592 Min	SE592 Typ	SE592 Max	NE592 Min	NE592 Typ	NE592 Max	Units
Differential Voltage Gain — Figure 3 (R_L = 2 kΩ, e_{out} = 3 Vp-p) (Gain 1, Note 1) (Gain 2, Note 2)	A_{vd}	 300 90	 400 100	 500 110	 250 80	 400 100	 600 120	V/V
Bandwidth — Figure 3 (Gain 1, Note 1) (Gain 1, Note 2)	BW	 – –	 40 90	 – –	 – –	 40 90	 – –	MHz
Rise Time — Figure 3 (Gain 1, e_{out} = 1 Vp-p, Note 1) (Gain 2, e_{out} = 1 Vp-p, Note 2)	 t_{TLH} t_{THL}	 – –	 10.5 4.5	 – 10	 – –	 10.5 4.5	 – 12	ns
Propagation Delay — Figure 3 (Gain 1, e_{out} = 1 Vp-p, Note 1) (Gain 2, e_{out} = 1 Vp-p, Note 2)	 t_{PLH} t_{PHL}	 – –	 7.5 6.0	 – 10	 – –	 7.5 6.0	 – 10	ns
Input Resistance (Gain 1, Note 1) (Gain 2, Note 2)	R_{in}	 – 20	 4.0 30	 – –	 – 10	 4.0 30	 – –	kΩ
Input Capacitance (Gain 2, Note 2)	C_{in}	–	2.0	–	–	2.0	–	pF
Input Offset Current (Gain 3, Note 3) — Fig. 2	I_{IO}	–	0.4	3.0	–	0.4	5.0	μA
Input Bias Current (Gain 3, Note 3) — Fig. 2	I_{IB}	–	9.0	20	–	9.0	30	μA
Input Noise Voltage (Gain 1 and Gain 2) (BW = 1 kHz to 10 MHz) — Figure 1	V_n	–	12	–	–	12	–	μV(rms)
Input Voltage Range (Gain 2, Note 2) — Fig. 3	V_{in}	±1.0	–	–	±1.0	–	–	V
Common-Mode Rejection Ratio — Figure 3 (Gain 2, V_{CM} = ±1 V, f ≤ 100 kHz) (Gain 2, V_{CM} = ±1 V, f = 5 MHz)	CMRR	 60 –	 86 60	 – –	 60 –	 86 60	 – –	dB
Supply Voltage Rejection Ratio — Figure 2 (Gain 2, Δ V_s = ±0.5 V)	PSRR	 50	 70	 –	 50	 70	 –	dB
Output Offset Voltage — Figure 2 (Gain 3, R_L = ∞, Note 3)	V_{OO}	–	0.35	0.75	–	0.35	0.75	V
Output Common-Mode Voltage — Figure 2 (R_L = ∞, Gain 3, Note 3)	V_{CMO}	 2.4	 2.9	 3.4	 2.4	 2.9	 3.4	V
Output Voltage Swing — Figure 3 (R_L = 2k, Gain 2, Note 2)	V_O	 3.0	 4.0	 –	 3.0	 4.0	 –	Vp-p
Output Resistance	r_o	–	20	–	–	20	–	Ω
Power Supply Current — Figure 2 (R_L = ∞, Gain 2, Note 2)	I_D	–	18	24	–	18	24	mA

Note 1. Gain select pins $G1_A$ and $G1_B$ connected together.

Note 2. Gain select pins $G2_A$ and $G2_B$ connected together.

Note 3. All gain select pins open.

Input Resistance (Gain 2)	R_{in}	8.0	–	–	8.0	–	–	kΩ
Input Offset Current (Gain 3) – Figure 2	$\|I_{IO}\|$	–	–	5.0	–	–	6.0	μA
Input Bias Current (Gain 3) – Figure 2	I_{IB}	–	–	40	–	–	40	μA
Input Voltage Range (Gain 2) – Figure 3	V_{in}	±1.0	–	–	±1.0	–	–	V
Common-Mode Rejection Ratio – Figure 3 (Gain 2, V_{CM} = ±1 V, f ≤ 100 kHz)	CMRR	50	–	–	50	–	–	dB
Supply Voltage Rejection Ratio – Figure 2 (Gain 2, Δ V_s = ±0.5 V)	PSRR	50	–	–	50	–	–	dB
Output Offset Voltage (Gain 3) – Figure 2	V_{OO}	–	–	1.2	–	–	1.5	V
Output Voltage Swing (Gain 2) – Figure 3	V_O	2.5	–	–	2.5	–	–	Vp-p
Power Supply Current (Gain 2) – Figure 2	I_D	–	–	27	–	–	27	mA

*T_{low} = 0°C for NE592, -55°C for SE592
T_{high} = +70°C for NE592, +125°C for SE592

GENERAL TEST CIRCUITS

FIGURE 1

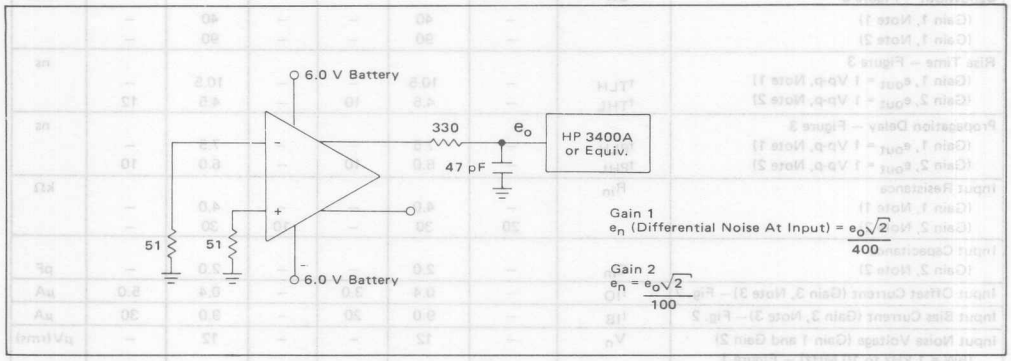


FIGURE 2

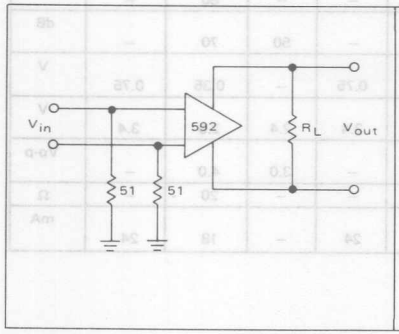


FIGURE 3

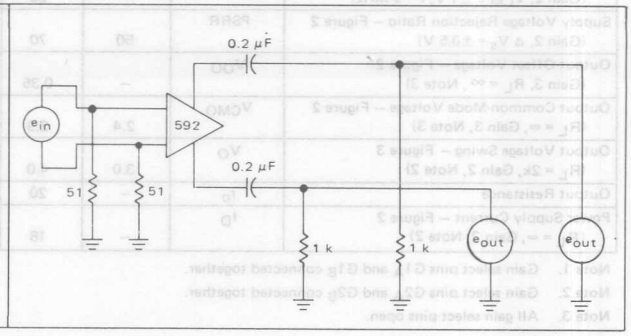


FIGURE 4 – GAIN 1 versus FREQUENCY

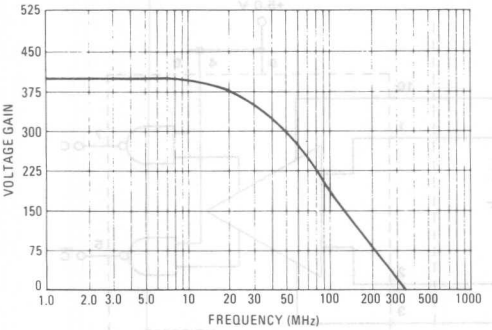


FIGURE 5 – GAIN 2 versus FREQUENCY

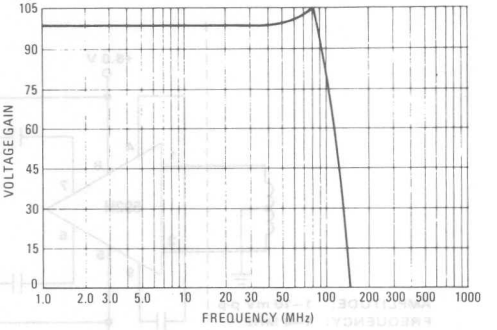


FIGURE 6 – OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY

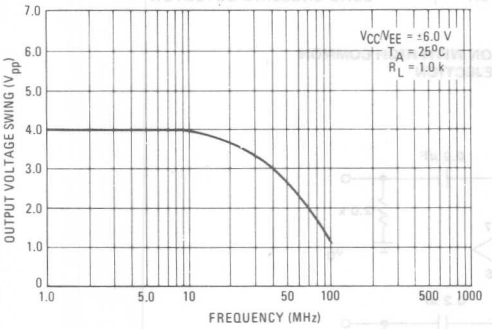


FIGURE 7 – OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

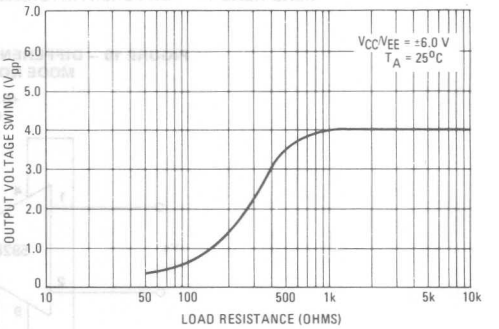
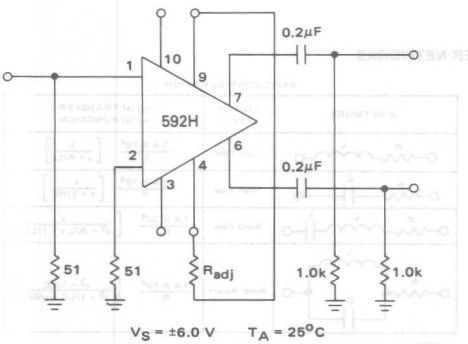
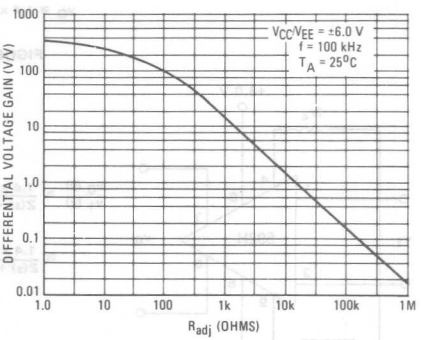


FIGURE 8 – VOLTAGE GAIN AS A FUNCTION OF R_{adj} RESISTANCE





2

FIGURE 9 – DISK/TAPE PHASE MODULATED READBACK SYSTEMS

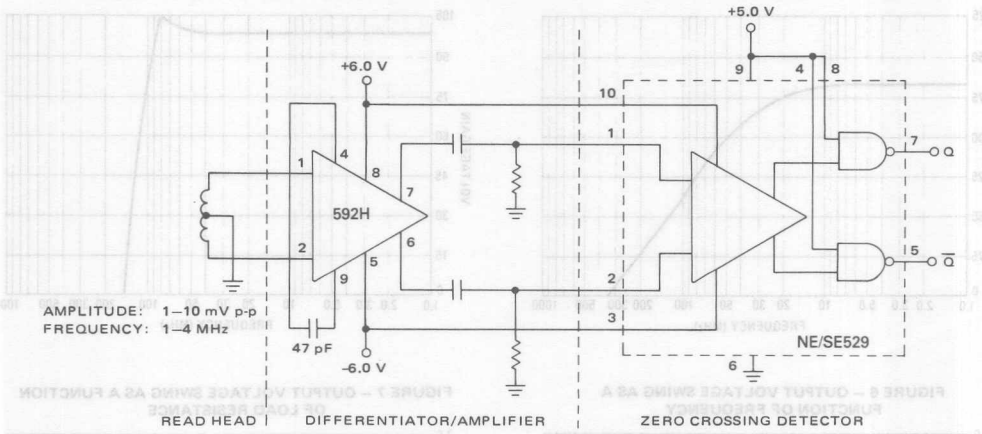
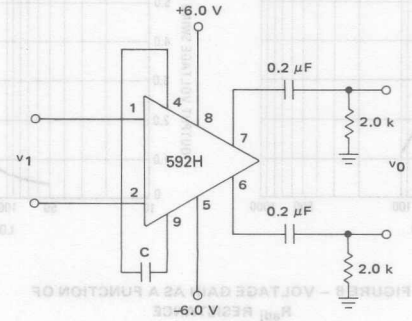


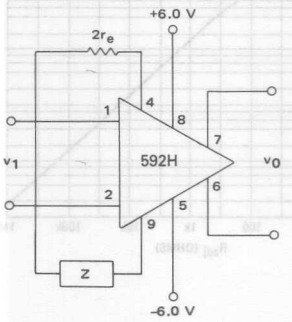
FIGURE 10 – DIFFERENTIATION WITH HIGH COMMON MODE NOISE REJECTION



FOR FREQUENCY $f_1 << 1/2\pi(32)C$

$$v_O \cong 1.4 \times 10^4 C \frac{dv_1}{dt}$$

FIGURE 11 – FILTER NETWORKS



$$\frac{v_0(s)}{v_1(s)} \cong \frac{1.4 \times 10^4}{Z(s) + 2r_e} \cong \frac{1.4 \times 10^4}{Z(s) + 32}$$

BASIC CONFIGURATION

Z NETWORK	FILTER TYPE	$v_0(s)$ TRANSFER $v_1(s)$ FUNCTION
R, L	Low Pass	$\frac{1.4 \times 10^4}{L}\left[\frac{1}{s + R/L}\right]$
R, C	High Pass	$\frac{1.4 \times 10^4}{R}\left[\frac{s}{s + 1/RC}\right]$
R, L, C	Band Pass	$\frac{1.4 \times 10^4}{L}\left[\frac{s}{s^2 + R/L\,s + 1/LC}\right]$
L; R, C	Band Reject	$\frac{1.4 \times 10^4}{R}\left[\frac{s^2 + 1/LC}{s^2 + 1/LC + s/RC}\right]$

NOTE:
In the networks above, the R value used is assumed to include 2 r_e, or approximately 30 Ohms.

OP-27

ULTRA-LOW NOISE PRECISION, HIGH SPEED OPERATIONAL AMPLIFIER

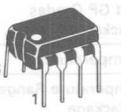
The OP-27 series of monolithic operational amplifiers combine low-noise, precision dc performance and high bandwidth in one device. Advanced Bipolar processing and innovative design techniques are used to produce this low noise precision operational amplifier. This device is trimmed for extremely low initial input offset voltage by utilizing a highly stable and reliable zener zap technique during factory testing which yields guaranteed V_{IO} limits as tight as 25 μV. A unique input bias current cancellation scheme maintains low I_{IB} and I_{IO} to typically $\pm$20 nA and 15 nA respectively over the full military temperature range. Other sources of input errors are reduced in excess of $-$120 dB due to extremely high common-mode and power supply rejection ratios. The OP-27 has a gain bandwidth product of 8.0 MHz and slew rate of 2.8 V/μs.

The precision, low noise and high speed characteristics of this device makes it ideal for amplifying transducer signals, RIAA phono, NAB tape head and microphone preamplifiers, wide band instrumentation amplifiers and high speed signal conditioning for data acquisition systems.

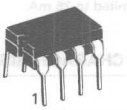
- Extremely Low-Noise — 3.0 nV/$\sqrt{Hz}$ at 1.0 kHz
  80 nVp-p, 0.1 Hz to 10 Hz
- Low Initial Input Offset Voltage — 10 μV
- Ultra Stable Input Offset Voltage — 0.2 μV/mo.
- High Gain Bandwidth Product and High Slew Rate — 8.0 MHz, 2.8 V/μs
- High Open-Loop Gain — 1.8 Million
- High Common-Mode Rejection — 126 dB

ULTRA-LOW NOISE PRECISION, HIGH SPEED OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

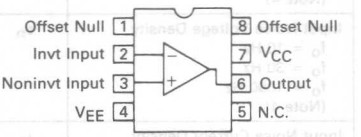


P SUFFIX
PLASTIC PACKAGE
CASE 626-05



Z SUFFIX
CERAMIC PACKAGE
CASE 693-02

(Top View)



ORDERING INFORMATION

Slew Rate	Device			Temperature Range	Package
	$V_{IO} \leq 25$ μV	$V_{IO} \leq 60$ μV	$V_{IO} \leq 100$ μV		
$\geq$ 1.7 V/μs	OP-27AZ	OP-27BZ	OP-27CZ	$-$55 to + 125°C	Ceramic DIP
	OP-27EZ	OP-27FZ	OP-27GZ	$-$25 to +85°C	Ceramic DIP
	OP-27EP	OP-27FP	OP-27GP	0 to +70°C	Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC} V_{EE}	+22 −22	V
Input Voltage Range (Note 1)	V_{IDR}	±22	V
Differential Input Voltage (Note 2)	V_{ID}	±0.7	V
Differential Input Current (Note 2)	I_{ID}	±25	mA
Output Short-Circuit Duration	t_s	Indefinite	
Power Dissipation and Thermal Characteristics Plastic Package (P Suffix) T_A = +36°C	P_D	500	mW
Derate above T_A = +75°C	$1/R_{\theta JA}$	6.7	mW/°C
Ceramic Package (Z Suffix) T_A = +75°C	P_D	500	mW
Derate above T_A = +80°C	$1/R_{\theta JA}$	7.1	mW/°C
Operating Ambient Temperature A,B and C Grades	T_A	−55 to +125	°C
E,F and G Grades (Ceramic Package)		−25 to +85	
EP, FP and GP Grades (Plastic Package)		0 to +70	
Junction Temperature	T_J	+150	°C
Storage Temperature Range Ceramic Package Plastic Package	T_{stg}	−65 to +150 −65 to +125	°C

NOTES:
1. For supply voltages less than ±22 V, the absolute maximum input voltage range is equal to the supply voltage.
2. The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7 V, the input current must be limited to 25 mA.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	OP-27A/E/EP			OP-27B/F/FP			OP-27C/G/GP			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	—	10	25	—	20	60	—	30	100	μV
Long Term Input Offset Voltage Stability (Note 3)	V_{IO}/t	—	0.2	1.0	—	0.3	1.5	—	0.4	2.0	μV/mo
Input Offset Current	I_{IO}	—	7.0	35	—	9.0	50	—	12	75	nA
Input Bias Current	I_{IB}	—	±10	±40	—	±12	±55	—	±15	±80	nA
Input Noise Voltage 0.1 to 10 Hz (Note 4)	e_{np-p}	—	0.08	0.18	—	0.08	0.18	—	0.09	0.25	μV_{p-p}
Input Noise Voltage Density	e_n										$nV/\sqrt{Hz}$
f_o = 10 Hz		—	3.5	5.5	—	3.5	5.5	—	3.8	8.0	
f_o = 30 Hz		—	3.1	4.5	—	3.1	4.5	—	3.3	5.6	
f_o = 1000 Hz (Note 4)		—	3.0	3.8	—	3.0	3.8	—	3.2	4.5	
Input Noise Current Density	i_n										$pA/\sqrt{Hz}$
f_o = 10 Hz		—	1.7	4.0	—	1.7	4.0	—	1.7	—	
f_o = 30 Hz		—	1.0	2.3	—	1.0	2.3	—	1.0	—	
f_o = 1000 Hz (Note 4)		—	0.4	0.6	—	0.4	0.6	—	0.4	0.6	
Input Resistance — Differential Mode	r_i	1.5	6.0	—	1.2	5.0	—	0.8	4.0	—	MΩ
Input Resistance — Common Mode	R_{incm}	—	3.0	—	—	2.5	—	—	2.0	—	GΩ
Input Voltage Range	V_{IR}	±11.0	±12.3	—	±11.0	±12.3	—	±11.0	±12.3	—	V

(continued)

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Symbol	OP-27A/E/EP			OP-27B/F/FP			OP-27C/G/GP			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Common Mode Rejection Ratio V_{CM} = ±11 V	CMRR	114	126	—	106	123	—	100	120	—	dB
Power Supply Rejection Ratio V_{CC}/V_{EE} = ±4.0 V to ±18 V	PSRR	100	120	—	100	120	—	94	114	—	dB
Large-Signal Voltage Gain	A_{VOL}										V/mV
$R_L \geq 2.0$ kΩ, V_O = ±10 V		1000	1800	—	1000	1800	—	700	1500	—	
$R_L \geq 1.0$ kΩ, V_O = ±10 V		800	1500	—	800	1500	—	—	1500	—	
R_L = 600 Ω, V_O = ±1.0 V, V_{CC}/V_{EE} = ±4.0 V to ±18 V		—	700	—	—	700	—	—	500	—	
Output Voltage Swing	V_O										V
$R_L \geq 2.0$ kΩ		±12	±13.8	—	±12	±13.8	—	±11.5	±13.5	—	
$R_L \geq 600$ Ω		±10	±11.5	—	±10	±11.5	—	±10	±11.5	—	
Slew Rate, $R_L \geq 2.0$ kΩ	SR	1.7	2.8	—	1.7	2.8	—	1.7	2.8	—	V/μs
Gain Bandwidth Product	GBW	5.0	8.0	—	5.0	8.0	—	5.0	8.0	—	MHz
Open Loop Output Resistance V_O = 0, I_O = 0	r_o	—	70	—	—	70	—	—	70	—	Ω
Power Dissipation V_O = 0, No Load	P_D	—	90	140	—	90	140	—	100	170	mW
Offset Adjustment Range R_P = 10 kΩ		—	±4.0	—	—	±4.0	—	—	±4.0	—	mV

NOTES (continued)

3. Long term input offset voltage stability for the OP-27 series, refers to the average trend line of V_{IO} versus time over extended periods after the first 30 days of operation. Excluding the first hour of operation, changes in V_{IO} during the first 30 days are typically 2.5 μV.
4. Sample tested.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = T_{low} to T_{high} [Note 5])

Characteristic	Symbol	OP-27A			OP-27B			OP-27C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	—	30	60	—	50	200	—	70	300	μV
Average Input Offset Drift (Note 6)	TCV_{IO}	—	0.2	0.6	—	0.3	1.3	—	0.4	1.8	μV/°C
Input Offset Current	I_{IO}	—	15	50	—	22	85	—	30	135	nA
Input Bias Current	I_{IB}	—	±20	±60	—	±28	±95	—	±35	±150	nA
Input Voltage Range	V_{IR}	±10.3	±11.5	—	±10.3	±11.5	—	±10.2	±11.5	—	V
Common Mode Rejection Ratio V_{CM} = ±10 V	CMRR	108	122	—	100	119	—	94	116	—	dB
Power Supply Rejection Ratio V_{CC}/V_{EE} = ±4.5 V to ±18 V	PSRR	96	114	—	94	114	—	86	108	—	dB
Large-Signal Voltage Gain $R_L \geq 2$ kΩ, V_O = ±10 V	A_{VOL}	600	1200	—	500	1000	—	300	800	—	V/mV
Output Voltage Swing $R_L \geq 2$ kΩ	V_O	±11.5	±13.5	—	±11.0	±13.2	—	±10.5	±13.0	—	V

2

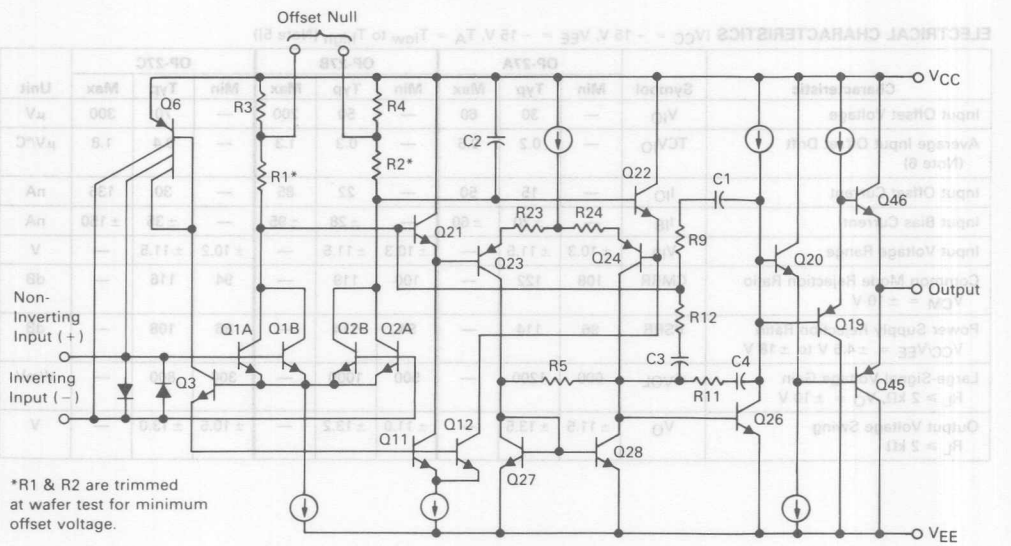
ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = T_{low} to T_{high} [Note 5])

Characteristic	Symbol	OP-27E/EP			OP-27F/FP			OP-27G/GP			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	—	20	50	—	40	140	—	55	220	μV
Average Input Offset Drift (Note 6)	TCV_{IO}	—	0.2	0.6	—	0.3	1.3	—	0.4	1.8	μV/°C
Input Offset Current	I_{IO}	—	10	50	—	14	85	—	20	135	nA
Input Bias Current	I_{IB}	—	±14	±60	—	±18	±95	—	±25	±150	nA
Input Voltage Range	V_{IR}	±10.5	±11.8	—	±10.5	±11.8	—	±10.5	±11.8	—	V
Common Mode Rejection Ratio V_{CM} = ±10 V	CMRR	110	124	—	102	121	—	96	118	—	dB
Power Supply Rejection Ratio V_{CC}/V_{EE} = ±4.5 V to ±18 V	PSRR	97	114	—	96	114	—	90	114	—	dB
Large-Signal Voltage Gain $R_L \geq 2.0$ kΩ, V_O = ±10 V	A_{VOL}	750	1500	—	700	1300	—	450	1000	—	V/mV
Output Voltage Swing $R_L \geq 2.0$ kΩ	V_O	±11.7	±13.6	—	±11.4	±13.5	—	±11	±13.3	—	V

NOTES (continued)

5. T_{low} = −55°C for OP-27A, OP-27B, OP-27C; = −25°C for OP-27E, OP-27F, OP-27G; = 0°C for OP-27EP, OP-27FP, OP-27GP
   T_{high} = +125°C for OP-27A, OP-27B, OP-27C; = +85°C for OP-27E, OP-27F, OP-27G; = +70°C for OP-27EP, OP-27FP, OP-27GP
6. TCV_{IO} performance is within specifications unnulled or when nulled with a potentiometer R_P = 8.0 kΩ to 20 kΩ.

ABBREVIATED CIRCUIT SCHEMATIC



TYPICAL CHARACTERISTICS

FIGURE 1 — VOLTAGE NOISE TESTER GAIN versus FREQUENCY

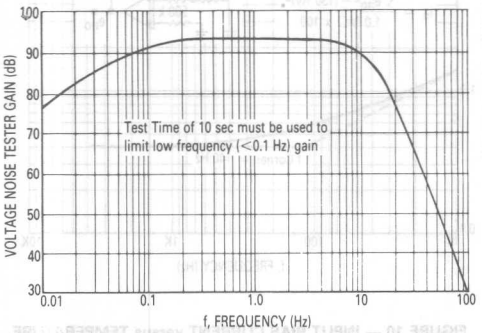
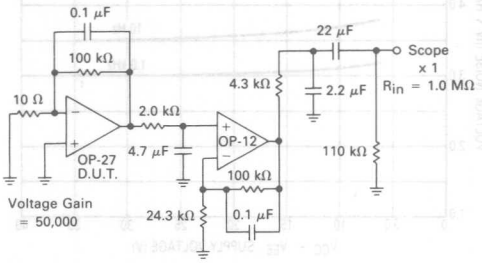


FIGURE 2 — VOLTAGE NOISE TEST CIRCUIT (0.1 Hz-TO-10 Hz)



Note: All capacitor values are for non polarized capacitors only.

FIGURE 3 — VOLTAGE NOISE versus FREQUENCY

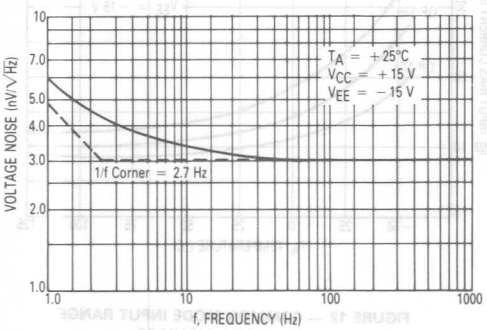


FIGURE 4 — INPUT WIDEBAND VOLTAGE NOISE versus BANDWIDTH (0.1 Hz TO FREQUENCY INDICATED)

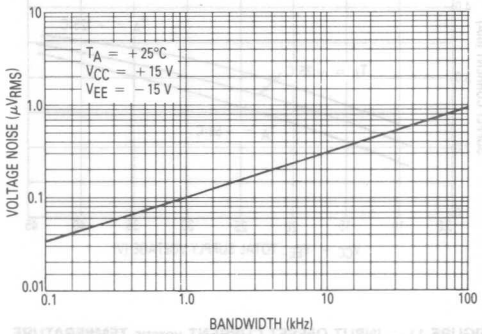


FIGURE 5 — TOTAL NOISE versus SOURCE RESISTANCE

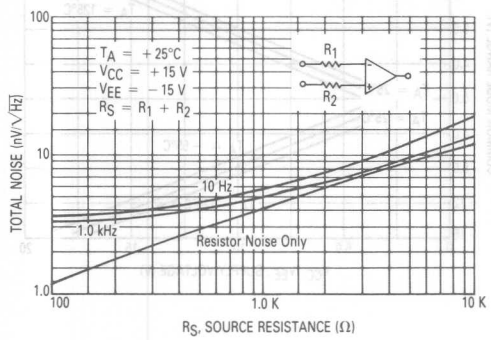


FIGURE 6 — VOLTAGE NOISE versus TEMPERATURE

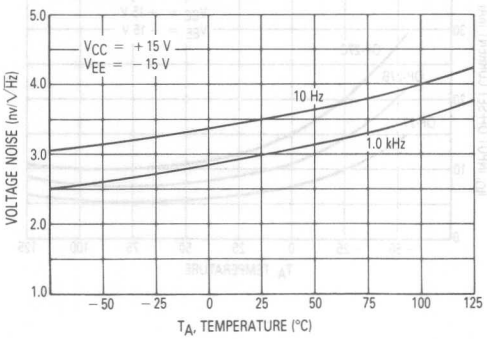


FIGURE 7 — VOLTAGE NOISE versus SUPPLY VOLTAGE

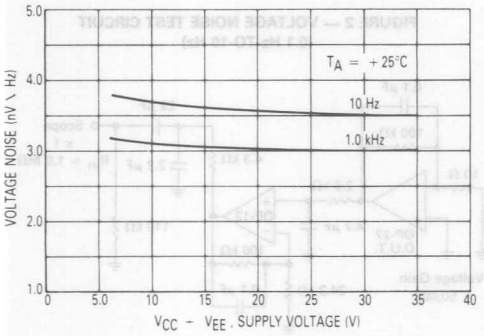


FIGURE 8 — CURRENT NOISE versus FREQUENCY

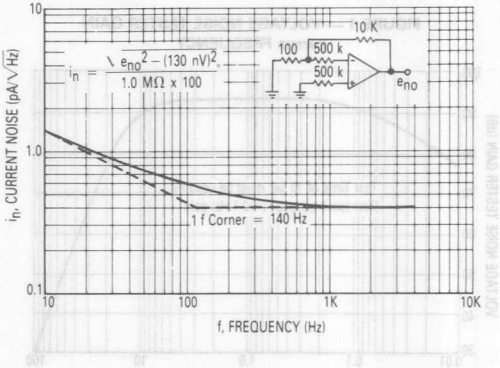


FIGURE 9 — SUPPLY CURRENT versus SUPPLY VOLTAGE

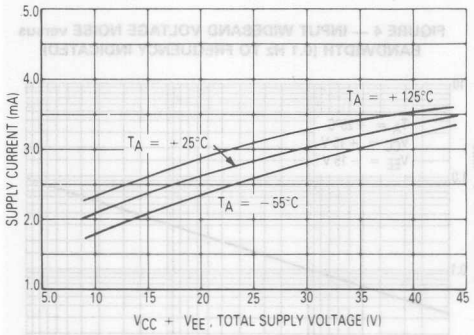


FIGURE 10 — INPUT BIAS CURRENT versus TEMPERATURE

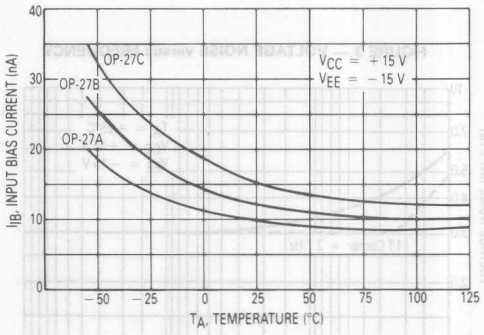


FIGURE 11 — INPUT OFFSET CURRENT versus TEMPERATURE

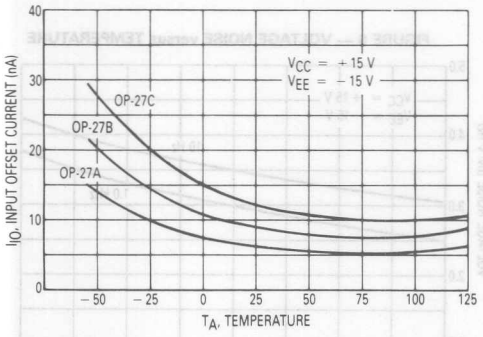


FIGURE 12 — COMMON MODE INPUT RANGE versus SUPPLY VOLTAGE

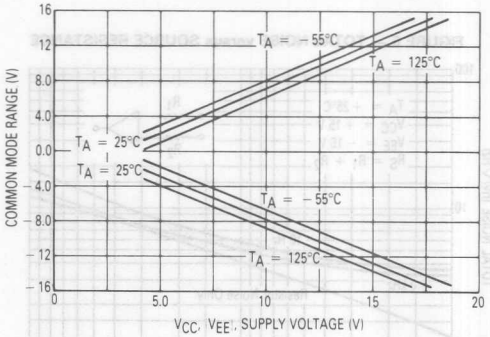


FIGURE 13 — OPEN LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE

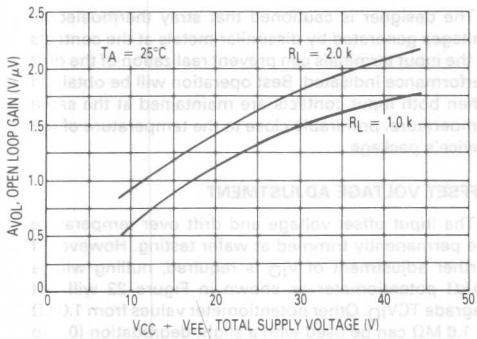


FIGURE 14 — OPEN LOOP VOLTAGE GAIN versus LOAD RESISTANCE

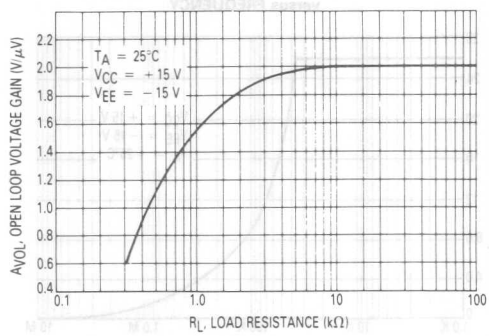


FIGURE 15 — MAXIMUM OUTPUT SWING versus RESISTIVE LOAD

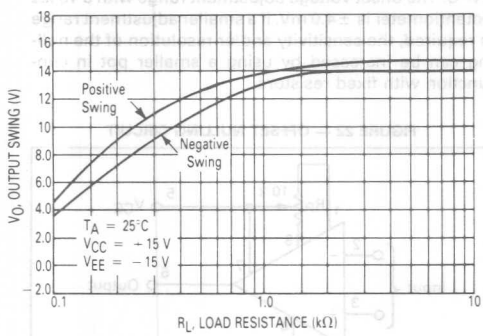


FIGURE 16 — POWER SUPPLY REJECTION RATIO versus FREQUENCY

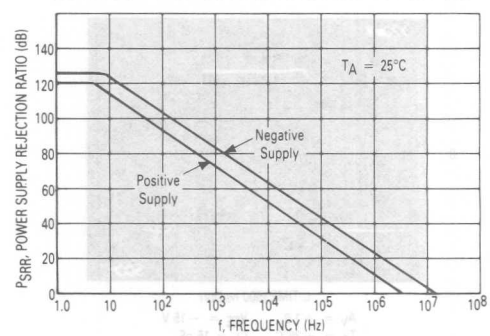


FIGURE 17 — COMMON MODE REJECTION RATIO versus FREQUENCY

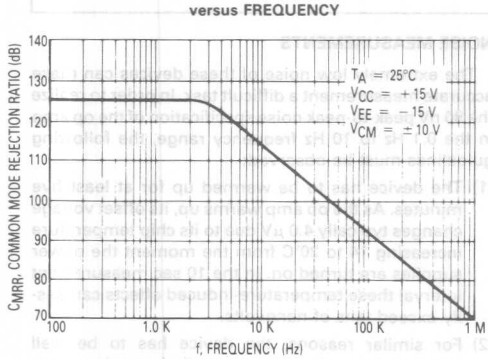
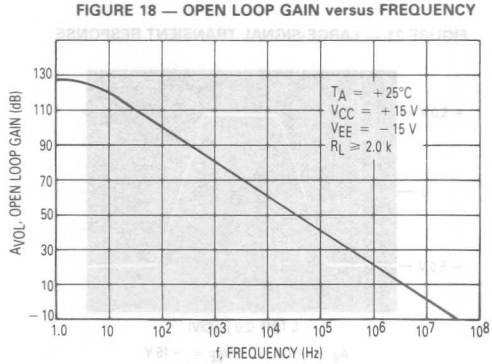


FIGURE 18 — OPEN LOOP GAIN versus FREQUENCY



2

FIGURE 19 — MAXIMUM UNDISTORTED OUTPUT versus FREQUENCY

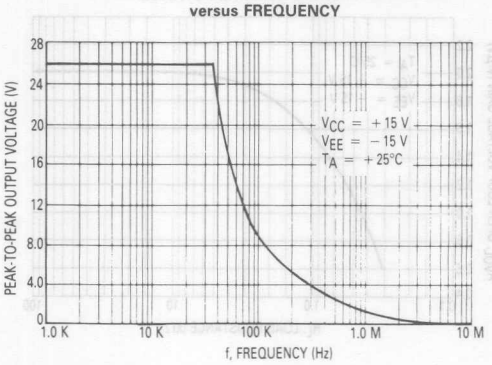


FIGURE 20 — SMALL-SIGNAL TRANSIENT RESPONSE

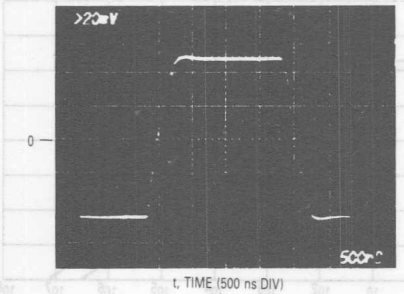
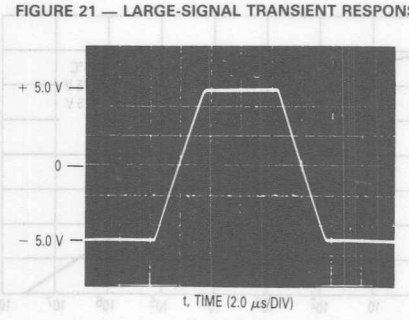


FIGURE 21 — LARGE-SIGNAL TRANSIENT RESPONSE



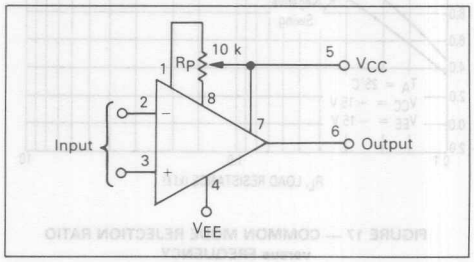
APPLICATIONS INFORMATION

The designer is cautioned that stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can prevent realization of the drift performance indicated. Best operation will be obtained when both input contacts are maintained at the same temperature, preferably close to the temperature of the device's package.

OFFSET VOLTAGE ADJUSTMENT

The input offset voltage and drift over temperature are permanently trimmed at wafer testing. However, if further adjustment of V_{IO} is required, nulling with a 10 kΩ potentiometer as shown in Figure 22 will not degrade TCV_{IO}. Other potentiometer values from 1.0 kΩ to 1.0 MΩ can be used with a slight degradation (0.1 to 0.2 µV/°C) of TCV_{IO}. Trimming to a value other than zero creates a drift of (V_{IO}/300) µV/°C, e.g. if V_{IO} is adjusted to 100 µV, the change in TCV_{IO} will be 0.33 µV/°C. The offset voltage adjustment range with a 10 kΩ potentiometer is ±4.0 mV. If a smaller adjustment range is required, the sensitivity and/or resolution of the nulling can be increased by using a smaller pot in conjunction with fixed resistors.

FIGURE 22 — OFFSET NULLING CIRCUIT



NOISE MEASUREMENTS

The extremely low noise of these devices can make accurate measurement a difficult task. In order to realize the 80 nV peak-to-peak noise specification of the op amp in the 0.1 Hz to 10 Hz frequency range, the following guidelines must be observed:

(1) The device has to be warmed up for at least five minutes. As the op amp warms up, its offset voltage changes typically 4.0 µV due to its chip temperature increasing 14 to 20°C from the moment the power supplies are turned on. In the 10 sec measurement interval these temperature-induced effects can easily exceed tens of nanovolts.

(2) For similar reasons, the device has to be well shielded from air currents to eliminate the possibility of thermoelectric effects in excess of several nanovolts.

(3) Sudden motion in the vicinity of the device can also "feed-through" to increase the observed noise.

(4) The test time to measure 0.1 Hz to 10 Hz noise should not exceed 10 sec. As shown in the noise tester frequency response curve (Figure 1) the 0.1 Hz corner is defined by only one zero. The test time of 10 sec acts as an additional zero to eliminate noise contributions from the frequency band below 0.1 Hz.

A noise-voltage density test is recommended when measuring noise on a large number of units. A 10 Hz noise-voltage density measurement will correlate well with a 0.1 Hz-to-10 Hz peak-to-peak noise reading since both results are determined by the white noise and the location of the 1/f corner frequency.

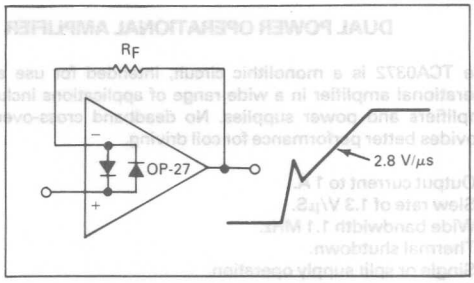
UNITY GAIN BUFFER APPLICATIONS

When $R_F \leq 100\ \Omega$ and the input is driven with a fast, large signal pulse (> 1.0 V), the output waveform will look as shown in Figure 23.

During the initial fast input step, the input protection diodes effectively short the output to the input and current limit only by the output short circuit protection of the op amp and the source resistance of the generator. With $R_F \geq 500\ \Omega$, the output is capable of handling the current requirements ($I_L \leq 20$ mA at 10 V) and the amplifier stays in its active mode and a smooth transition will occur.

As with all operational amplifiers when $R_F > 2.0\ k\Omega$, a pole will be created with R_F and the amplifier's input capacitance (8.0 pF), creating additional phase shift and reducing the phase margin. A small capacitor (20 to 50 pF) in parallel with R_F will eliminate this problem.

FIGURE 23 — PULSED OPERATION



MOTOROLA

TCA0372

Advance Information

DUAL POWER OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

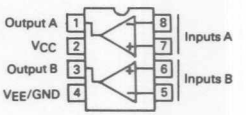
DUAL POWER OPERATIONAL AMPLIFIER

The TCA0372 is a monolithic circuit, intended for use as a power operational amplifier in a wide range of applications including servo amplifiers and power supplies. No deadband cross-over distortion provides better performance for coil driving.

- Output current to 1 A.
- Slew rate of 1.3 V/μS.
- Wide bandwidth 1.1 MHz.
- Thermal shutdown.
- Single or split supply operation.
- Excellent gain and phase margins.
- Common mode input includes ground.
- Zero deadband cross-over distortion.

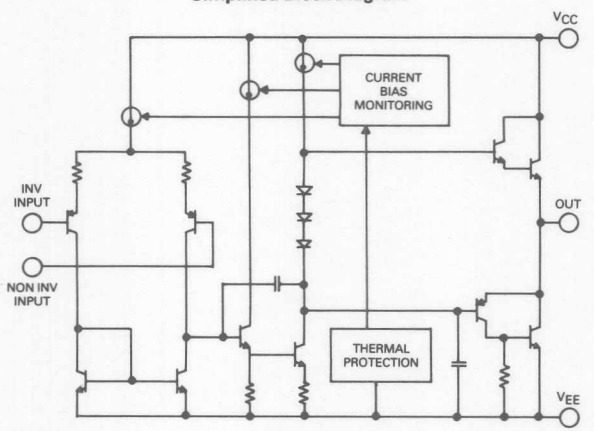


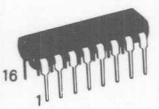
DP1 SUFFIX
PLASTIC PACKAGE
CASE 626-04



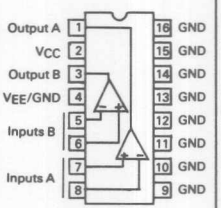
(Top view)

Simplified Block Diagram

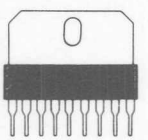




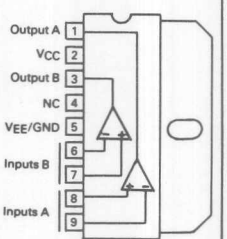
DP2 SUFFIX
PLASTIC PACKAGE
CASE 648-06



(Top view)



SP SUFFIX
PLASTIC MEDIUM POWER PACKAGE
CASE 762-01



(Top view)

ORDERING INFORMATION

Device	Temperature Range	Package
TCA0372DP1	T_j = -40°C to +125°C	DIP 8 pins plastic
TCA0372DP2	T_j = -40°C to +125°C	DIP 16 pins plastic
TCA0372SP	T_j = -40°C to +125°C	Single-in-line

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage (from V_{CC} to V_{EE})	V_S	40	V
Input differential voltage range	V_{IDR}	Note 1	V
Input voltage range	V_{IR}	Note 1	V
Operating junction temperature Plastic package	T_J	+125	°C
Storage temperature range Plastic package	T_{STG}	-55 to +125	°C
DC output current	I_O	1.0	A
Peak output current (non repetitive)	I_{MAX}	1.5	A

Notes
1. Either or both input voltages must not exceed the magnitude of V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, R_L connected to ground, $T_J = T_{low}$ to T_{high} [Note 3] unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Input offset voltage (V_{CM} = 0)	V_{IO}				mV
V_{CC} = +15 V, V_{EE} = -15 V, T_J = +25°C		-	3.0	15	
V_{CC} = +15 V, V_{EE} = -15 V, $T_J = T_{low}$ to T_{high}		-	-	20	
Average temperature coefficient of offset voltage	$\Delta V_{IO}/\Delta T$	-	20	-	µV/°C
Input bias current (V_{CM} = 0)	I_{IB}	-	100	500	nA
Input offset current (V_{CM} = 0)	I_{IO}	-	10	50	nA
Large signal voltage gain V_O = ±10 V, R_L = 2.0 K	A_{VOL}	30	100	-	V/mV
Output voltage swing I_L = 100 mA	V_{OH}				V
V_{CC} = +15 V, V_{EE} = -15 V, T = +25°C		14	14.2		
V_{CC} = +15 V, V_{EE} = -15 V, T = T_{low} to T_{high}		13.9			
	V_{OL}				V
V_{CC} = +15 V, V_{EE} = -15 V, T = +25°C		-	-14.2	-14	
V_{CC} = +15 V, V_{EE} = -15 V, T = T_{low} to T_{high}		-	-	-13.9	
Output voltage swing I_L = 1 A	V_{OH}				V
V_{CC} = +24 V, V_{EE} = 0 V, T_J = +25°C		22.5	22.7	-	
V_{CC} = +24 V, V_{EE} = 0 V, $T_J = T_{low}$ to T_{high}		22.5	-	-	
	V_{OL}				V
V_{CC} = +24 V, V_{EE} = 0, T_J = +25°C		-	1.3	1.5	
V_{CC} = +24 V, V_{EE} = 0 V, $T_J = T_{low}$ to T_{high}		-	-	1.5	
Input common mode voltage range	V_{ICR}				V
T_A = +25°C			V_{EE} to (V_{CC}-1)		
$T_A = T_{low}$ to T_{high}			V_{EE} to (V_{CC}-1.3)		
Common mode rejection ratio (R_S = 10 K)	CMRR	70	90		dB
Power supply rejection ratio (R_S = 100 Ω)	PSRR	70	90	-	dB
Power supply current	I_D				mA
V_{CC} = +15 V, V_{EE} = -15 V, T_J = +25°C		-	7	10	
V_{CC} = +15 V, V_{EE} = -15 V, $T_J = T_{low}$ to T_{high}		-	-	14	

Notes (continued)
3. T_{low} = -40°C, T_{high} = +125°C

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} connected to ground, T_J = +25°C unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Slew rate (V_{IN} = -10 V to + 10 V, R_L = 2.0 K, C_L = 100 pF) A_V = -1 $T_J = T_{low}$ to T_{high}	SR	1	1.4	-	V/μS
Gain bandwidth product (f = 100 KHz, C_L = 100 pF, RL = 2 K) T_J = 25°C	GBW	0.9	1.1	-	MHz
$T_J = T_{low}$ to T_{high}		0.7	-	-	
Phase margin $T_J = T_{low}$ to T_{high} R_L = 2.0 K, C_L = 100 pF	ϕ_m	-	80	-	Degrees
Gain margin R_L = 2.0 K, C_L = 100 pF		-	15	-	dB
Equivalent input noise voltage R_S = 100 ohms, f = 1.0 KHz to 100 KHz	e_n	-	22	-	nV/√Hz
Total harmonic distortion A_V = -1, R_L = 50 ohms, V_O = 0.5 VRMS, f = 1 KHz	T_{HD}	-	0.02	-	%
Thermal shutdown		-	1.60		°C

Note

If V_{EE} is disconnected before V_{CC}, a diode between V_{EE} and GROUND is recommended to avoid device damage.

TYPICAL PERFORMANCE CURVES

Figure 1.
Input Offset Voltage vs Temperature

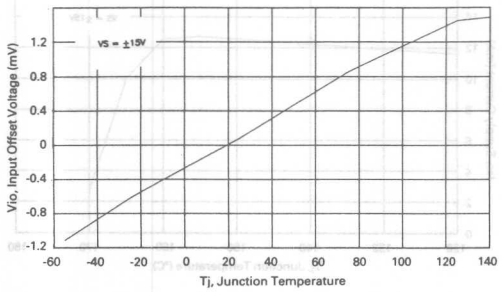


Figure 2.
Normalized Input Bias Current vs Temperature

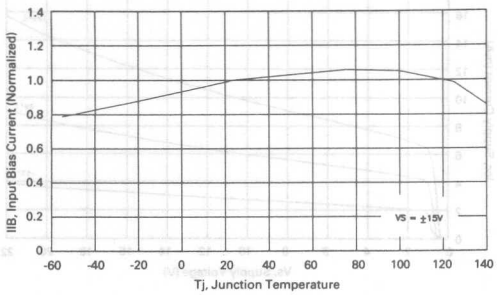


Figure 3.
High Output Saturation vs Load Current

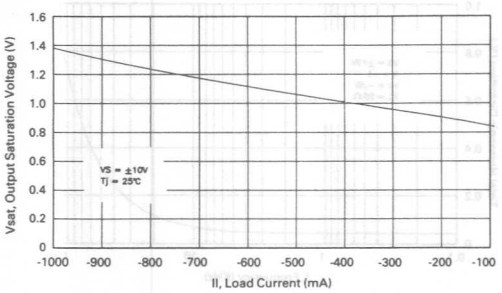


Figure 4.
High Output Saturation vs Load Current

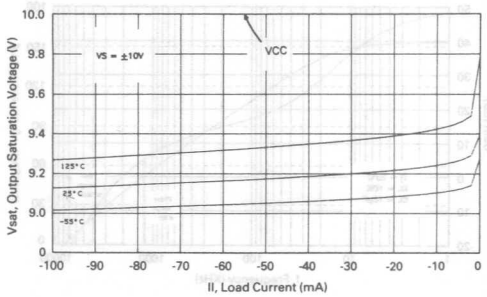


Figure 5.
Low Output Saturation vs Load Current

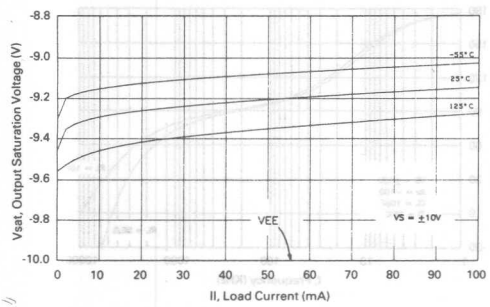
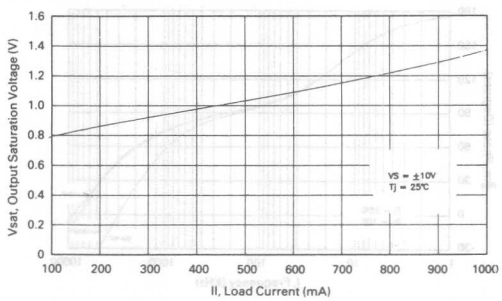


Figure 6.
Low Output Saturation vs Load Current



TYPICAL PERFORMANCE CURVES (continued)

Figure 7.
Supply Current vs Supply Voltage

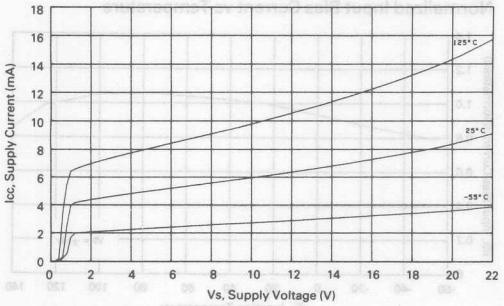


Figure 8.
Thermal Shutdown vs Temperature

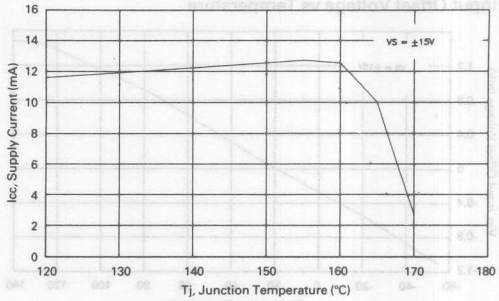


Figure 9.
Closed Loop Voltage Gain (40dB) and Phase vs Frequency

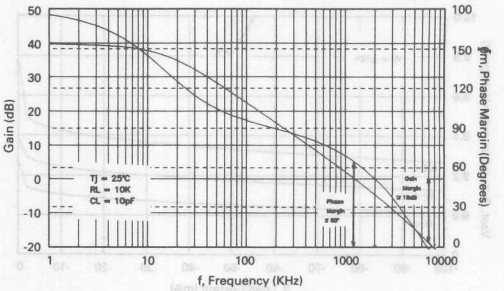


Figure 10.
Total Harmonic Distortion vs Frequency

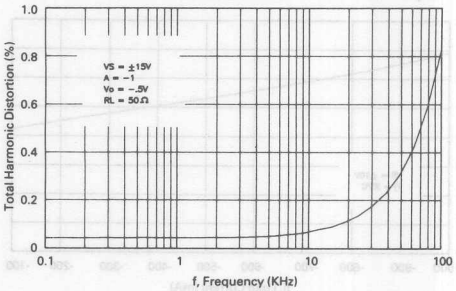


Figure 11.
Phase vs Frequency

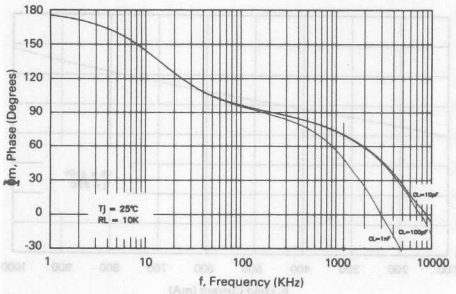
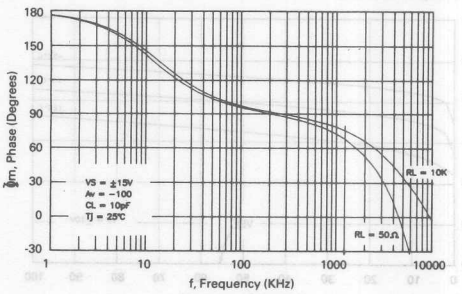


Figure 12.
Phase vs Frequency



TYPICAL PERFORMANCE CURVES (continued)

Figure 13.
Slew Rate ± vs Temperature

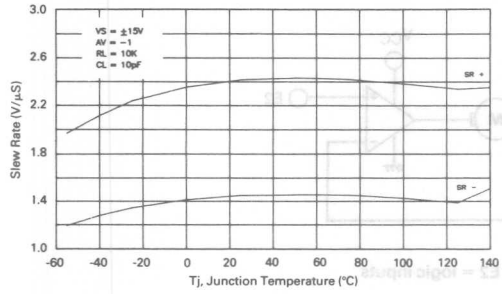


Figure 14.
Large Signal Transient Response

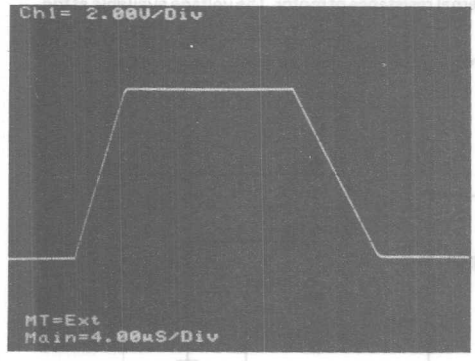
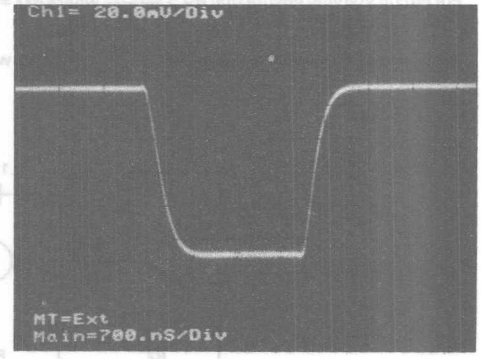


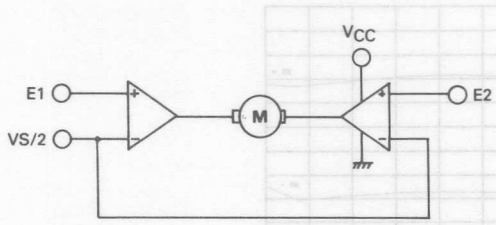
Figure 15.
Small Signal Transient Response



2

APPLICATION INFORMATION

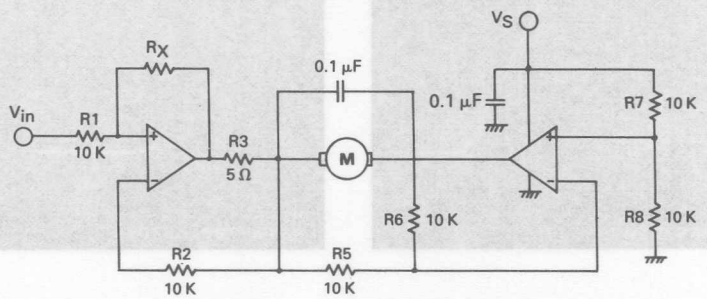
Figure 16. Bidirectional DC motor control with μP compatible inputs.



V_S = logic supply voltage Must be $V_{CC} > V_S$ E1, E2 = logic inputs

Figure 17. Bidirectional speed control of DC motors.

For circuit stability ensure that $R_X > \frac{2R3 \cdot R1}{R_M}$ where R_M = internal resistance of motor. The voltage available at the terminals of the motor is $V_M = 2(V_1 - \frac{V_S}{2}) + [R_O] \cdot I_M$ where $[R_O] = \frac{2R3 \cdot R1}{R_X}$ and I_M is the motor current.



THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature can be found from the equation:

$$P_{D(TA)} = \frac{T_J(max) - T_A}{R_{\theta JA}(typ)}$$

Where:

$P_{D(TA)}$ = Power dissipation allowable at a given operating temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_{J(Max)}$ = Maximum operating junction temperature as listed in the MAXIMUM RATINGS section.

T_A = Maximum desired operating ambient temperature.

$R_{\theta JA}$ = Typical thermal resistance junction to ambient.

MOTOROLA

TL061
TL062
TL064

LOW POWER JFET INPUT OPERATIONAL AMPLIFIERS

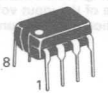
SILICON MONOLITHIC INTEGRATED CIRCUITS

LOW POWER JFET INPUT OPERATIONAL AMPLIFIER

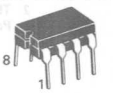
These JFET input operational amplifiers are designed for low power applications. They feature high input impedance, low input bias current and low input offset current. Advanced design techniques allow for higher slew rates, gain bandwidth products and output swing. The TL061 device provides for the external null adjustment of input offset voltage.

These devices are specified over the commercial, vehicular and military temperature ranges. The commercial and vehicular devices are available in Plastic dual in-line and SOIC packages. The military devices are available in Ceramic dual in-line packages.

- Low Supply Current — 200 μA/Amplifier
- Low Input Bias Current — 5.0 pA
- High Gain Bandwidth — 2.0 MHz
- High Slew Rate — 6.0 V/μs
- High Input Impedance — 10^{12} Ω
- Large Output Voltage Swing — ±14 V
- Output Short Circuit Protection



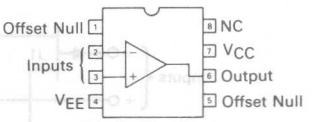
P SUFFIX
PLASTIC PACKAGE
CASE 626-05



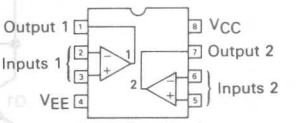
JG SUFFIX
CERAMIC PACKAGE
CASE 693-02



D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SO-8



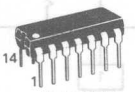
(Single, Top View)



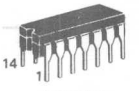
(Dual, Top View)

ORDERING INFORMATION

Op Amp Function	Device	Tested Temperature Range	Package
Single	TL061CD, ACD, BCD	0 to +70°C	SO-8
	TL061CP, ACP, BCP	0 to +70°C	Plastic DIP
	TL061VD	−40 to +85°C	SO-8
	TL061VP	−40 to +85°C	Plastic DIP
	TL061MJG	−55 to +125°C	Ceramic DIP
Dual	TL062CD, ACD, BCD	0 to +70°C	SO-8
	TL062CP, ACP, BCP	0 to +70°C	Plastic DIP
	TL062VD	−40 to +85°C	SO-8
	TL062VP	−40 to +85°C	Plastic DIP
	TL062MJG	−55 to +125°C	Ceramic DIP
Quad	TL064CD, ACD, BCD	0 to +70°C	SO-14
	TL064CN, ACN, BCN	0 to +70°C	Plastic DIP
	TL064VD	−40 to +85°C	SO-14
	TL064VP	−40 to +85°C	Plastic DIP
	TL064MJ	−55 to +125°C	Ceramic DIP



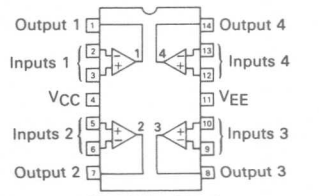
N SUFFIX
PLASTIC PACKAGE
CASE 646-06



J SUFFIX
CERAMIC PACKAGE
CASE 632-08



D SUFFIX
PLASTIC PACKAGE
CASE 751A-02
SO-14



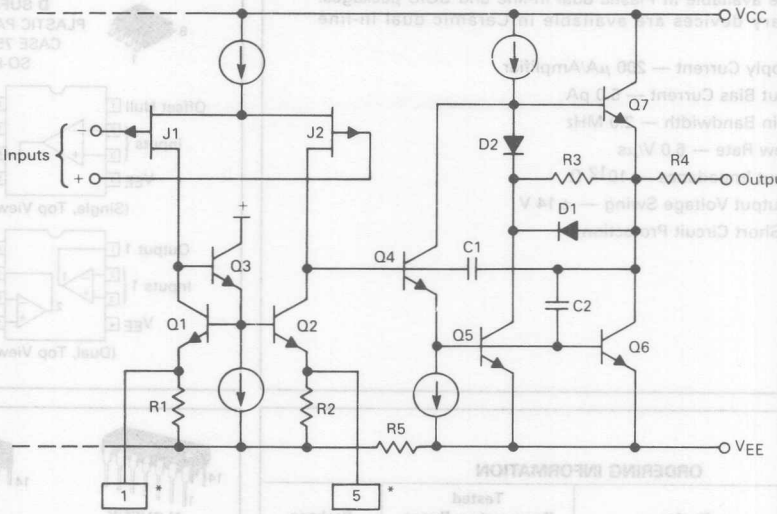
(Quad, Top View)

MAXIMUM RATINGS

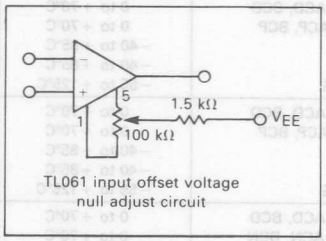
Rating	Symbol	Value	Unit
Supply Voltage (from V_{CC} to V_{EE})	V_S	+36	V
Input Differential Voltage Range (Note 1)	V_{IDR}	±30	V
Input Voltage Range (Notes 1 and 2)	V_{IR}	±15	V
Output Short-Circuit Duration (Note 3)	t_S	Indefinite	Seconds
Operating Junction Temperature (Note 3) Ceramic Package Plastic Package	T_J	 +160 +150	°C
Storage Temperature Range Ceramic Package Plastic Package	T_{stg}	 −65 to +160 −60 to +150	°C

NOTES:
1. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
2. The magnitude of the input voltage must never exceed the magnitude of the supply or 15 volts, whichever is less.
3. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded. (See Figure 1.)

EQUIVALENT CIRCUIT SCHEMATIC (EACH AMPLIFIER)



*Null adjustment pins for TL061 only.



TL061 input offset voltage null adjust circuit

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 0°C to +70°C, unless otherwise noted)

Characteristic	Symbol	TL061BC TL062BC TL064BC			TL061AC TL062AC TL064AC			TL061C TL062C TL064C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (R_S = 50 Ω, V_O = 0 V)	V_{IO}										mV
T_A = 25°C		—	2.0	3.0	—	3.0	6.0	—	3.0	15	
T_A = 0°C to +70°C		—	—	5.0	—	—	7.5	—	—	20	
Average Temperature Coefficient for Offset Voltage	$\Delta V_{IO}/\Delta T$										μV/°C
(R_S = 50 Ω, V_O = 0 V)		—	10	—	—	10	—	—	10	—	
Input Offset Current (V_{CM} = 0 V, V_O = 0 V)	I_{IO}										
T_A = 25°C		—	0.5	100	—	0.5	100	—	0.5	200	pA
T_A = 0°C to +70°C		—	—	2.0	—	—	2.0	—	—	2.0	nA
Input Bias Current (V_{CM} = 0 V, V_O = 0 V)	I_{IB}										
T_A = 25°C		—	3.0	200	—	3.0	200	—	3.0	200	pA
T_A = 0°C to +70°C		—	—	7.0	—	—	7.0	—	—	10	nA
Input Common Mode Voltage Range (T_A = 25°C)	V_{ICR}	—	+14.5	+11.5	—	+14.5	+11.5	—	+14.5	+11	V
		−11.5	−12	—	−11.5	−12	—	−11	−12	—	
Large Signal Voltage Gain (R_L = 10 kΩ, V_O = ±10 V)	A_{VOL}										V/mV
T_A = 25°C		4.0	58	—	4.0	58	—	3.0	58	—	
T_A = 0°C to +70°C		4.0	—	—	4.0	—	—	3.0	—	—	
Output Voltage Swing (R_L = 10 kΩ, V_{ID} = 1.0 V)											V
T_A = 25°C	V_O+	+10	+14	—	+10	+14	—	+10	+14	—	
	V_O-	—	−14	−10	—	−14	−10	—	−14	−10	
T_A = 0°C to +70°C	V_O+	+10	—	—	+10	—	—	+10	—	—	
	V_O-	—	—	−10	—	—	−10	—	—	−10	
Common Mode Rejection	CMR										dB
(R_S = 50 Ω, V_{CM} = V_{ICR} min, V_O = 0 V, T_A = 25°C)		80	84	—	80	84	—	70	84	—	
Power Supply Rejection	PSR										dB
(R_S = 50 Ω, V_{CM} = 0 V, V_O = 0, T_A = 25°C)		80	86	—	80	86	—	70	86	—	
Power Supply Current (each amplifier)	I_D										μA
(No Load, V_O = 0 V, T_A = 25°C)		—	200	250	—	200	250	—	200	250	
Total Power Dissipation (each amplifier)	P_D										mW
(No Load, V_O = 0 V, T_A = 25°C)		—	6.0	7.5	—	6.0	7.5	—	6.0	7.5	

2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = T_{low} to T_{high} (Note 4), unless otherwise noted)

Characteristic	Symbol	TL061M,V TL062M,V Min	Typ	Max	TL064M,V Min	Typ	Max	Unit
Input Offset Voltage (R_S = 50 Ω, V_O = 0 V)	V_{IO}							mV
T_A = 25°C		—	3.0	6.0	—	3.0	9.0	
T_A = T_{low} to T_{high}		—	—	9.0	—	—	15	
Average Temperature Coefficient of Offset Voltage (R_S = 50 Ω, V_O = 0 V)	$\Delta V_{IO}/\Delta T$	—	10	—	—	10	—	μV/°C
Input Offset Current (V_{CM} = 0 V, V_O = 0 V)	I_{IO}							
T_A = 25°C		—	5.0	100	—	5.0	100	pA
T_A = T_{low} to T_{high}		—	—	20	—	—	20	nA
Input Bias Current (V_{CM} = 0 V, V_O = 0 V)	I_{IB}							
T_A = 25°C		—	30	200	—	30	200	pA
T_A = T_{low} to T_{high}		—	—	50	—	—	50	nA
Input Common Mode Voltage Range (T_A = 25°C)	V_{ICR}	—	+14.5	+11.5	—	+14.5	+11.5	V
		−11.5	−12	—	−11.5	−12	—	
Large Signal Voltage Gain (R_L = 10 kΩ, V_O = ±10 V)	A_{VOL}							V/mV
T_A = 25°C		4.0	58	—	4.0	58	—	
T_A = T_{low} to T_{high}		4.0	—	—	4.0	—	—	
Output Voltage Swing (R_L = 10 kΩ, V_{ID} = 1.0 V)								V
T_A = 25°C	V_O+	+10	+14	—	+10	+14	—	
	V_O−	—	−14	−10	—	−14	−10	
T_A = T_{low} to T_{high}	V_O+	+10	—	—	+10	—	—	
	V_O−	—	—	−10	—	—	−10	
Common Mode Rejection (R_S = 50 Ω, V_{CM} = V_{ICR} min, V_O = 0 V, T_A = 25°C)	CMR	80	84	—	80	84	—	dB
Power Supply Rejection (R_S = 50 Ω, V_{CM} = 0 V, V_O = 0 V, T_A = 25°C)	PSR	80	86	—	80	86	—	dB
Power Supply Current (each Amplifier) (No Load, V_O = 0 V, T_A = 25°C)	I_D	—	200	250	—	200	250	μA
Total Power Dissipation (each Amplifier) (No Load, V_O = 0 V, T_A = 25°C)	P_D	—	6.0	7.5	—	6.0	7.5	mW

Note 4. TL06XM T_{low} = −55°C T_{high} = +125°C
TL06XV T_{low} = −40°C T_{high} = +85°C

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25°C, unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = −10 V to +10 V, R_L = 10 kΩ, C_L = 100 pF, A_V = +1.0)		SR	2.0	6.0	—	V/μs
Rise Time (V_{in} = 20 mV, R_L = 10 kΩ, C_L = 100 pF, A_V = +1.0)		t_r	—	0.1	—	μs
Overshoot (V_{in} = 20 mV, R_L = 10 kΩ, C_L = 100 pF, A_V = +1.0)		OS	—	10	—	%
Settling Time		t_S				μs
(V_{CC} = +15 V, V_{EE} = −15 V, A_V = −1.0,	To within 10 mV		—	1.6	—	
R_L = 10 kΩ, V_O = 0 V to +10 V step)	To within 1.0 mV		—	2.2	—	
Gain Bandwidth Product (f = 200 kHz)		GBW	—	2.0	—	MHz
Equivalent Input Noise (R_S = 100 Ω, f = 1.0 kHz)		e_n	—	47	—	nV/$\sqrt{Hz}$
Input Resistance		R_i	—	10^{12}	—	Ω
Channel Separation (f = 10 kHz)		CS	—	120	—	dB

TYPICAL PERFORMANCE CURVES

FIGURE 1 — MAXIMUM POWER DISSIPATION versus TEMPERATURE FOR PACKAGE VARIATIONS

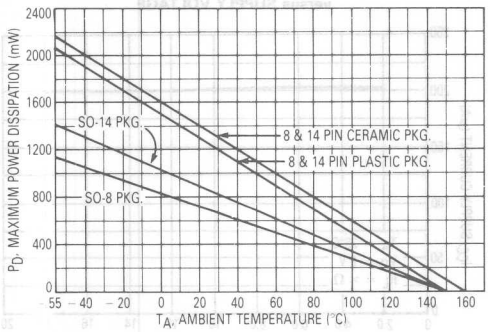


FIGURE 2 — OUTPUT VOLTAGE SWING versus SUPPLY VOLTAGE

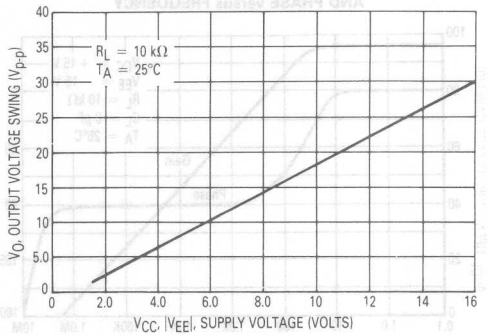


FIGURE 3 — OUTPUT VOLTAGE SWING versus TEMPERATURE

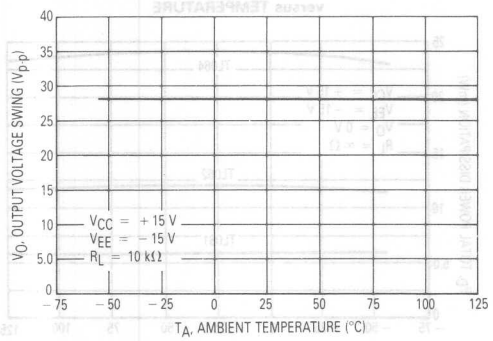


FIGURE 4 — OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

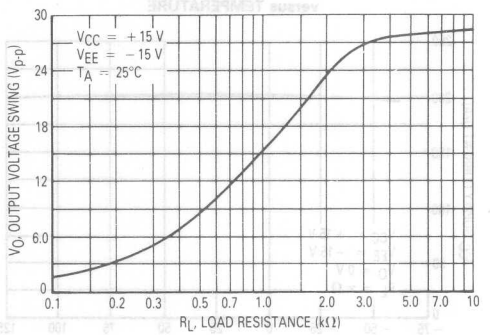


FIGURE 5 — OUTPUT VOLTAGE SWING versus FREQUENCY

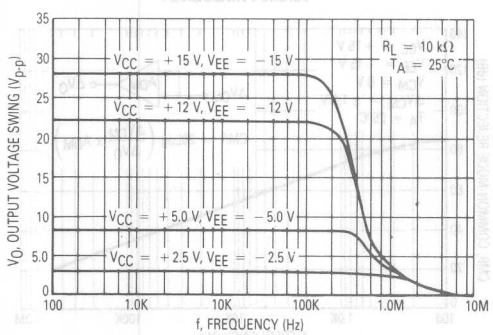


FIGURE 6 — LARGE SIGNAL VOLTAGE GAIN versus TEMPERATURE

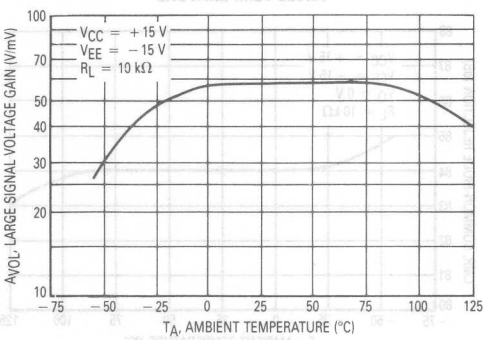


FIGURE 7 — OPEN-LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY

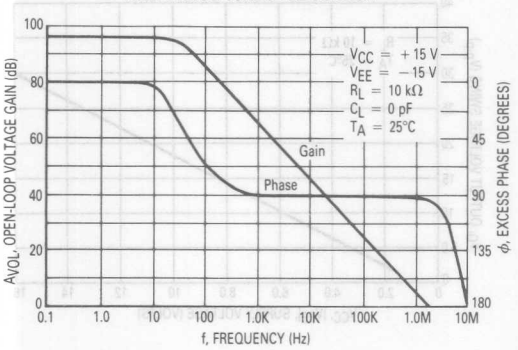


FIGURE 8 — SUPPLY CURRENT PER AMPLIFIER versus SUPPLY VOLTAGE

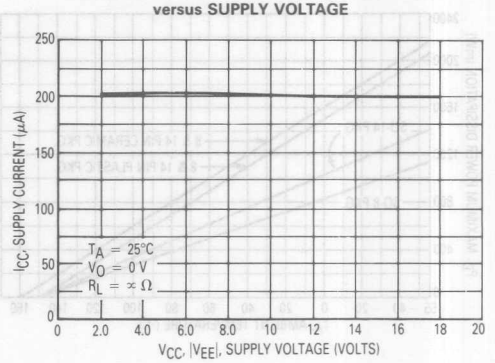


FIGURE 9 — SUPPLY CURRENT PER AMPLIFIER versus TEMPERATURE

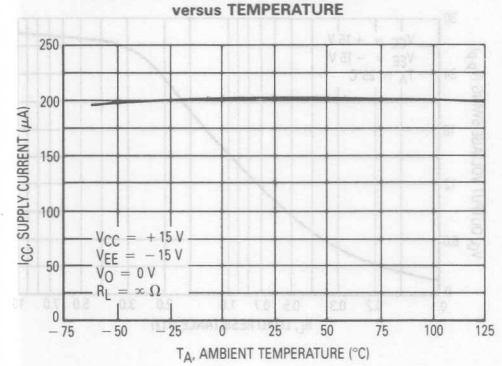


FIGURE 10 — TOTAL POWER DISSIPATION versus TEMPERATURE

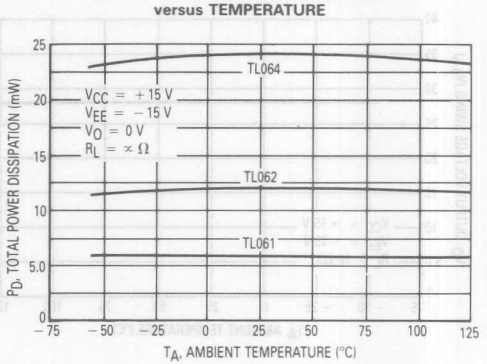


FIGURE 11 — COMMON-MODE REJECTION versus TEMPERATURE

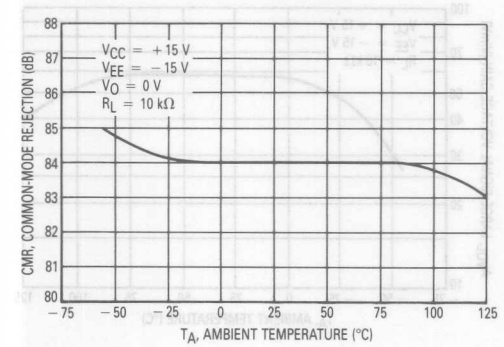


FIGURE 12 — COMMON-MODE REJECTION versus FREQUENCY

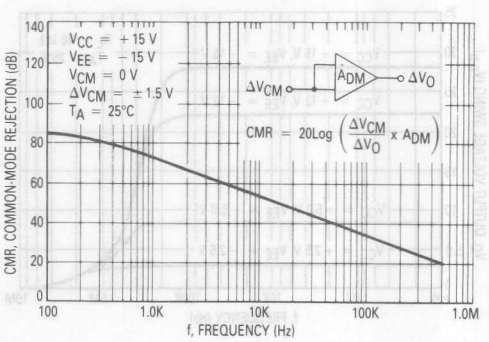


FIGURE 13 — POWER SUPPLY REJECTION versus FREQUENCY

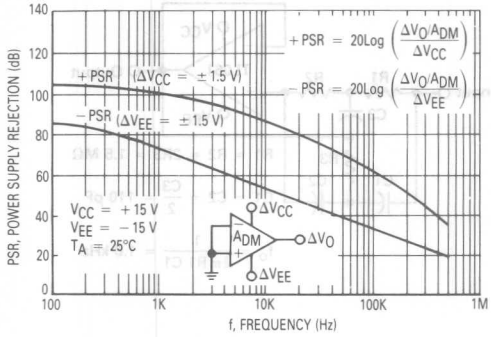


FIGURE 14 — NORMALIZED GAIN BANDWIDTH PRODUCT, SLEW RATE AND PHASE MARGIN versus TEMPERATURE

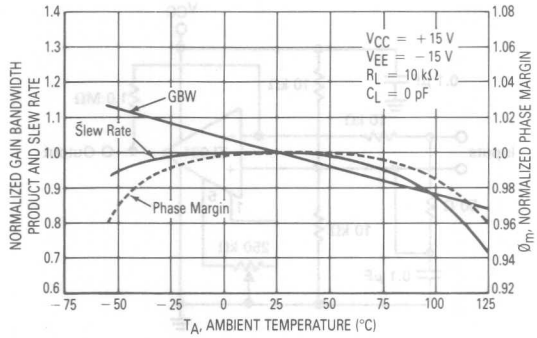


FIGURE 15 — INPUT BIAS CURRENT versus TEMPERATURE

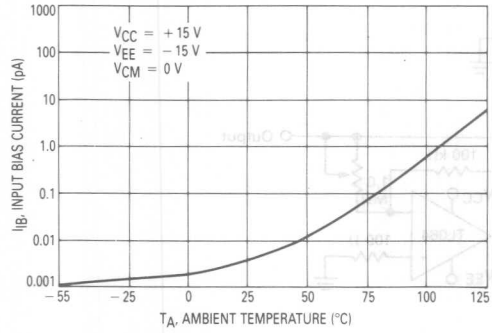


FIGURE 16 — INPUT NOISE VOLTAGE versus FREQUENCY

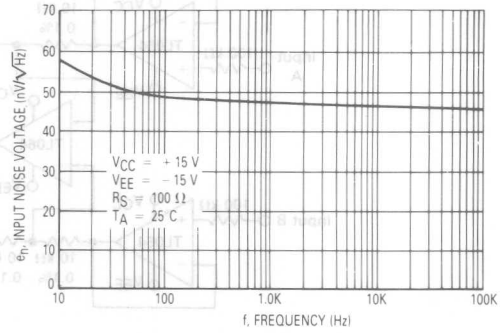


FIGURE 17 — SMALL SIGNAL RESPONSE

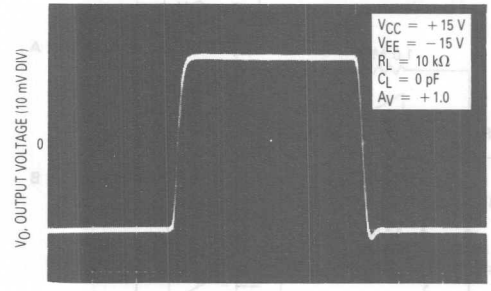
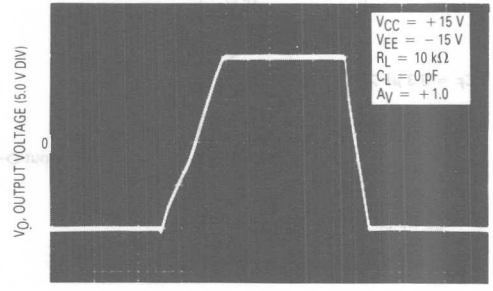


FIGURE 18 — LARGE SIGNAL RESPONSE



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FIGURE 19 — AC AMPLIFIER

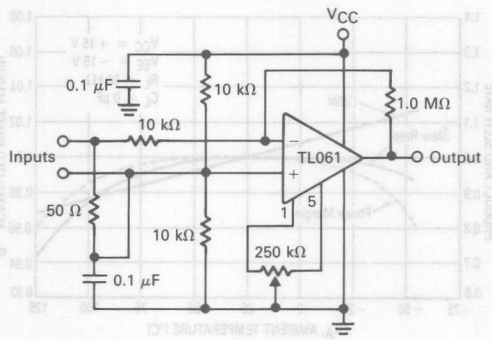


FIGURE 20 — HIGH-Q NOTCH FILTER

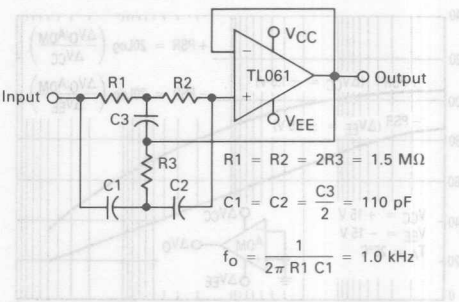


FIGURE 21 — INSTRUMENTATION AMPLIFIER

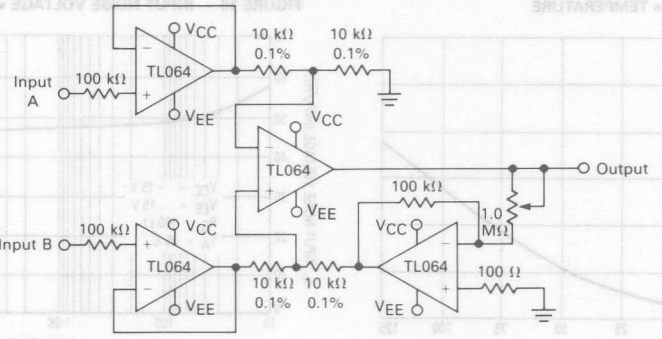


FIGURE 22 — 0.5 Hz SQUARE-WAVE OSCILLATOR

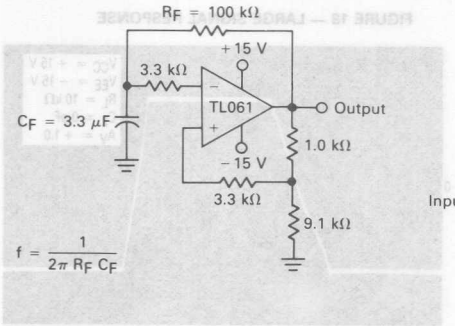
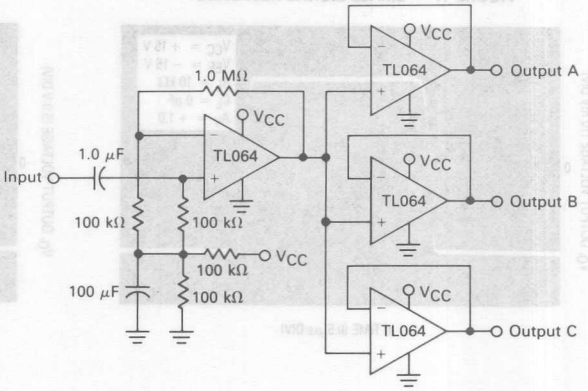


FIGURE 23 — AUDIO DISTRIBUTION AMPLIFIER



MOTOROLA

TL071
TL072
TL074

2

Specifications and Applications Information

LOW NOISE, JFET INPUT OPERATIONAL AMPLIFIERS

These low-noise JFET input operational amplifiers combine two state-of-the-art linear technologies on a single monolithic integrated circuit. Each internally compensated operational amplifier has well matched high voltage JFET input devices for low input offset voltage. The BIFET technology provides wide bandwidths and fast slew rates with low input bias currents, input offset currents, and supply currents. Moreover, the devices exhibit low-noise and low harmonic distortion making them ideal for use in high-fidelity audio amplifier applications.

These devices are available in single, dual and quad operational amplifiers which are pin-compatible with the industry standard MC1741, MC1458, and the MC3403/LM324 bipolar products. Devices with an "M" suffix are specified over the military operating temperature range of −55°C to +125°C and those with a "C" suffix are specified from 0°C to +70°C.

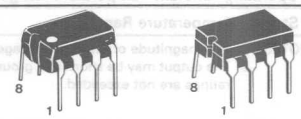
- Low Input Noise Voltage — 18 nV/$\sqrt{Hz}$ Typ
- Low Harmonic Distortion — 0.01% Typ
- Low Input Bias and Offset Currents
- High Input Impedance — 10^{12} Ω Typ
- High Slew Rate — 13 V/μs Typ
- Wide Gain Bandwidth — 4.0 MHz Typ
- Low Supply Current — 1.4 mA per Amp

ORDERING INFORMATION

Op Amp Function	Device	Temperature Range	Package
Single	TL071ACD, BCD, CD	0 to +70°C	SO-8
	TL071ACJG, BCJG, CJG		Ceramic DIP
	TL071ACP, BCP, CP		Plastic DIP
	TL071MJG	−55 to +125°C	Ceramic DIP
Dual	TL072ACD, BCD, CD	0 to +70°C	SO-8
	TL072ACJG, BCJG, CJG		Ceramic DIP
	TL072ACP, BCP, CP		Plastic DIP
	TL072MJG	−55 to +125°C	Ceramic DIP
Quad	TL074ACD, BCD, CD	0 to +70°C	SO-14
	TL074ACJ, BCJ, CJ		Ceramic DIP
	TL074ACN, BCN, CN		Plastic DIP
	TL074MJ	−55 to +125°C	Ceramic DIP

LOW NOISE, JFET INPUT OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUITS

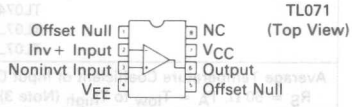


P SUFFIX
PLASTIC PACKAGE
CASE 626-05

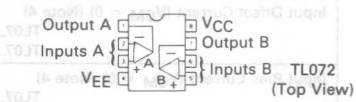
JG SUFFIX
CERAMIC PACKAGE
CASE 693-02



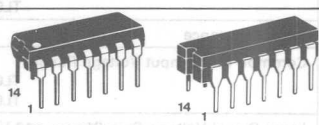
D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SO-8



TL071
(Top View)



TL072
(Top View)

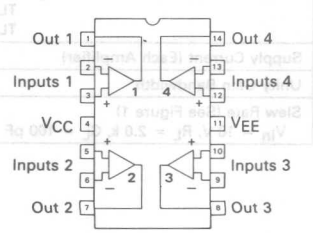


N SUFFIX
PLASTIC PACKAGE
CASE 646-06
(TL074 Only)

J SUFFIX
CERAMIC PACKAGE
CASE 632-08
(TL074 Only)



D SUFFIX
PLASTIC PACKAGE
CASE 751A-02
SO-14



TL074 (Top View)

MAXIMUM RATINGS

Rating	Symbol	TL07_ M	TL07_ C TL07_ AC TL07_ BC	Unit
Supply Voltage	V_{CC} V_{EE}	+18 −18	+18 −18	V
Differential Input Voltage	V_{ID}	±30	±30	V
Input Voltage Range (Note 1)	V_{IDR}	±15	±15	V
Output Short-Circuit Duration (Note 2)	t_S	Continuous		
Power Dissipation Plastic Package (N,P) Derate above T_A = +47°C Ceramic Package (J, JG) Derate above T_A = +82°C	 P_D $1/\theta_{JA}$ P_D $1/\theta_{JA}$	 — — 680 10	 680 10 680 10	 mW mW/°C mW mW/°C
Operating Ambient Temperature Range	T_A	−55 to +125	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	−65 to +150	°C

NOTES: 1. The magnitude of the input voltage must not exceed the magnitude of the supply voltage or 15 volts, whichever is less.
2. The output may be shorted to ground or either supply. Temperature and/or supply voltages must be limited to ensure that power dissipation ratings are not exceeded.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25° unless otherwise noted).

Characteristic	Symbol	TL07_ M Min	TL07_ M Typ	TL07_ M Max	TL07_ C / TL07_ AC / TL07_ BC Min	TL07_ C / TL07_ AC / TL07_ BC Typ	TL07_ C / TL07_ AC / TL07_ BC Max	Unit
Input Offset Voltage ($R_S \leq$ 10 k, V_{CM} = 0) TL071, TL072 TL074 TL07_ A TL07_ B	V_{IO}	 — — — —	 3.0 3.0 — —	 6.0 9.0 — —	 — — — —	 3.0 3.0 3.0 2.0	 10 10 6.0 3.0	mV
Average Temperature Coefficient of Input Offset Voltage R_S = 50 Ω, T_A = T_{low} to T_{high} (Note 3)	$\Delta V_{IO}/\Delta T$	—	10	—	—	10	—	μV/°C
Input Offset Current (V_{CM} = 0) (Note 4) TL07_ TL07_ A, TL07_ B	I_{IO}	 — —	 5.0 —	 50 —	 — —	 5.0 5.0	 50 50	pA
Input Bias Current (V_{CM} = 0) (Note 4) TL07_ TL07_ A, TL07_ B	I_{IB}	 — —	 30 —	 200 —	 — —	 30 30	 200 200	pA
Input Resistance	r_i	—	10^{12}	—	—	10^{12}	—	Ω
Common Mode Input Voltage Range TL07_ TL07_ A, TL07_ B	V_{ICR}	 ±11 —	 +15, −12 —	 — —	 ±10 ±11	 +15, −12 +15, −12	 — —	V
Large-Signal Voltage Gain (V_O = ±10 V, $R_L \geq$ 2.0 k) TL07_ TL07_ A, TL07_ B	A_{VOL}	 35 —	 150 —	 — —	 25 50	 150 150	 — —	V/mV
Output Voltage Swing (Peak-to-Peak) (R_L = 10 k)	V_O	24	28	—	24	28	—	V
Common Mode Rejection Ratio ($R_S \leq$ 10 k) TL07_ TL07_ A, TL07_ B	CMRR	 80 —	 100 —	 — —	 70 80	 100 100	 — —	dB
Supply Voltage Rejection Ratio ($R_S \leq$ 10 k) TL07_ TL07_ A, TL07_ B	PSRR	 80 —	 100 —	 — —	 70 80	 100 100	 — —	dB
Supply Current (Each Amplifier)	I_D	—	1.4	2.5	—	1.4	2.5	mA
Unity Gain Bandwidth	BW	—	4.0	—	—	4.0	—	MHz
Slew Rate (See Figure 1) V_{in} = 10 V, R_L = 2.0 k, C_L = 100 pF	SR	10	13	—	—	13	—	V/μs

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25° unless otherwise noted).

Characteristic	Symbol	TL07_ M			TL07_ C, TL07_ AC, TL07_ BC			Unit
		Min	Typ	Max	Min	Typ	Max	
Rise Time (See Figure 1)	t_r	—	0.1	—	—	0.1	—	μs
Overshoot Factor V_{in} = 20 mV, R_L = 2.0 k, C_L = 100 pF	—	—	10	—	—	10	—	%
Equivalent Input Noise Voltage R_S = 100 Ω, f = 1000 Hz	e_n	—	18	—	—	18	—	nV/√Hz
Equivalent Input Noise Current R_S = 100 Ω, f = 1000 Hz	i_n	—	0.01	—	—	0.01	—	pA/√Hz
Total Harmonic Distortion V_O (RMS) = 10 V, R_S ≤ 1.0 k R_L ≥ 2.0 k, f = 1000 Hz	THD	—	0.01	—	—	0.01	—	%
Channel Separation A_V = 100	—	—	120	—	—	120	—	dB

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = T_{high} to T_{low} [Note 3]).

Characteristic	Symbol	TL07_ M			TL07_ C, TL07_ AC, TL07_ BC			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (R_S ≤ 10 k, V_{CM} = 0)	V_{IO}							mV
TL071, TL072		—	—	9.0	—	—	13	
TL074		—	—	15	—	—	13	
TL07_ A		—	—	—	—	—	7.5	
TL07_ B		—	—	—	—	—	5.0	
Input Offset Current (V_{CM} = 0) (Note 4)	I_{IO}							nA
TL07_		—	—	20	—	—	2.0	
TL07_ A, TL07_ B		—	—	—	—	—	2.0	
Input Bias Current (V_{CM} = 0) (Note 4)	I_{IB}							nA
TL07_		—	—	50	—	—	7.0	
TL07_ A, TL07_ B		—	—	—	—	—	7.0	
Large-Signal Voltage Gain (V_O = ±10 V, R_L ≥ 2.0 k)	A_{VOL}							V/mV
TL07_		20	—	—	15	—	—	
TL07_ A, TL07_ B		—	—	—	25	—	—	
Output Voltage Swing (Peak-to-Peak)	V_O							V
(R_L ≥ 10 k)		24	—	—	24	—	—	
(R_L ≥ 2.0 k)		20	—	—	20	—	—	

NOTES (Continued):

3. T_{low} = −55°C for TL071M, TL072M, TL074M; T_{high} = +125°C for TL071M, TL072M, TL074M
   = 0°C for TL071C, TL071AC, TL071BC; = +70°C for TL071C, TL071AC, TL071BC
   TL072C, TL072AC, TL072BC; TL072C, TL072AC, TL072BC
   TL074C, TL074AC; TL074C, TL074AC

4. Input Bias currents of JFET input op amps approximately double for every 10°C rise in Junction Temperature as shown in Figure 3. To maintain Junction Temperature as close to ambient temperatures as possible, pulse techniques must be used during test.

TEST CIRCUITS

FIGURE 1 — UNITY GAIN VOLTAGE FOLLOWER

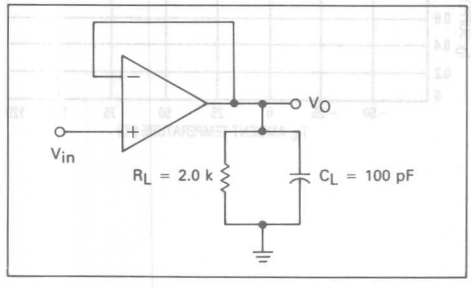
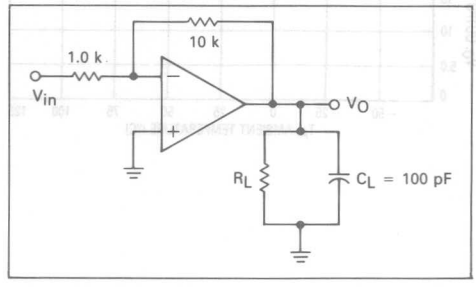


FIGURE 2 — INVERTING GAIN OF 10 AMPLIFIER



2

FIGURE 3 — INPUT BIAS CURRENT versus TEMPERATURE

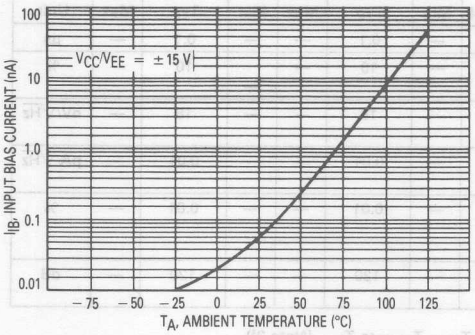


FIGURE 4 — OUTPUT VOLTAGE SWING versus FREQUENCY

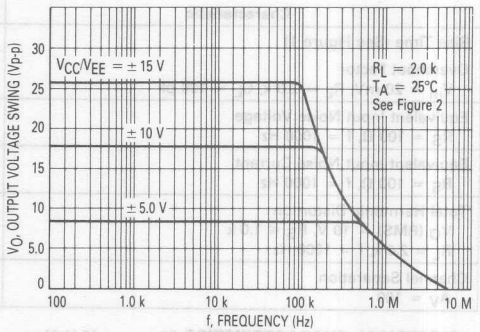


FIGURE 5 — OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

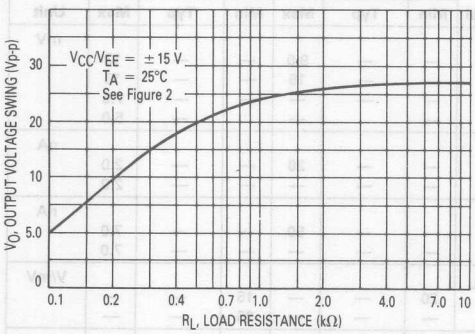


FIGURE 6 — OUTPUT VOLTAGE SWING versus SUPPLY VOLTAGE

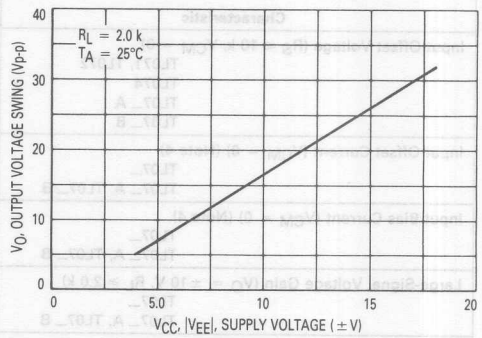


FIGURE 7 — OUTPUT VOLTAGE SWING versus TEMPERATURE

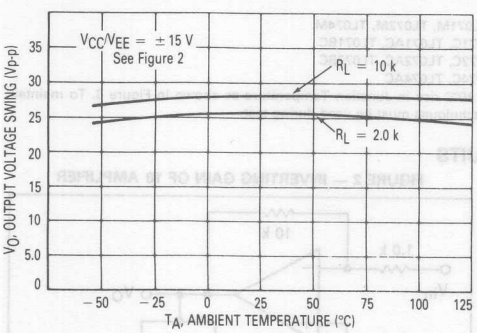


FIGURE 8 — SUPPLY CURRENT PER AMPLIFIER versus TEMPERATURE

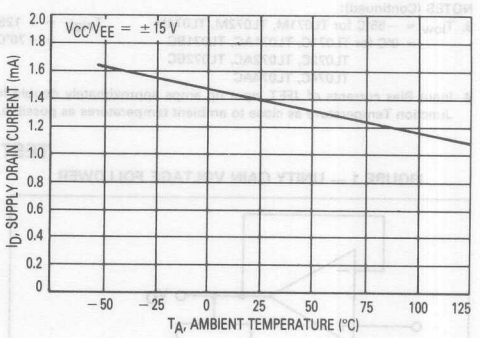


FIGURE 9 — LARGE-SIGNAL VOLTAGE GAIN AND PHASE SHIFT versus FREQUENCY

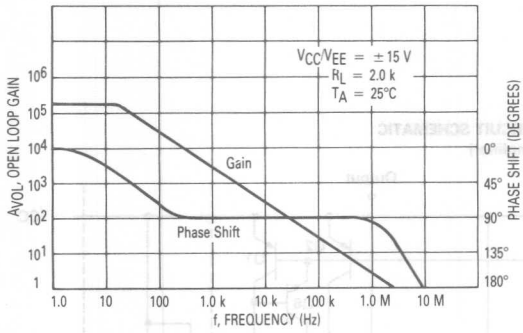


FIGURE 10 — LARGE-SIGNAL VOLTAGE GAIN versus TEMPERATURE

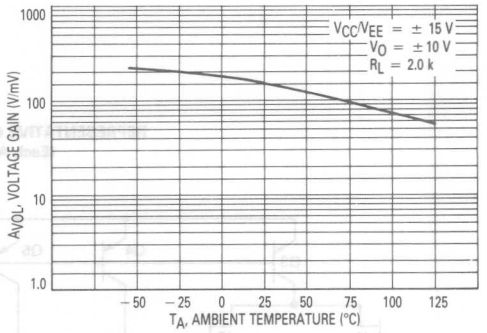


FIGURE 11 — NORMALIZED SLEW RATE versus TEMPERATURE

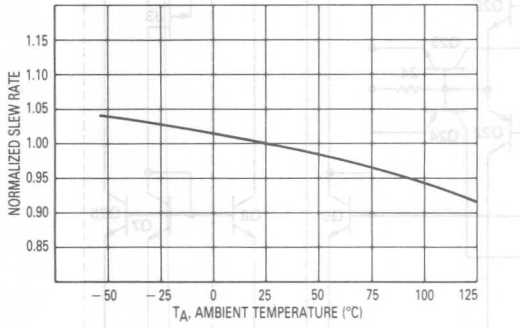


FIGURE 12 — EQUIVALENT INPUT NOISE VOLTAGE versus FREQUENCY

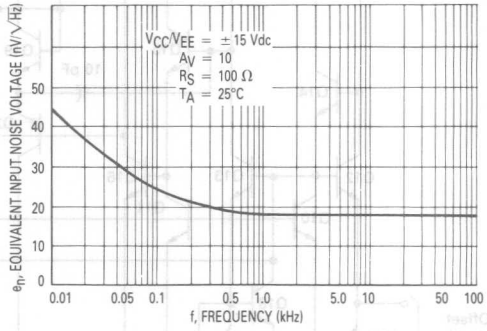
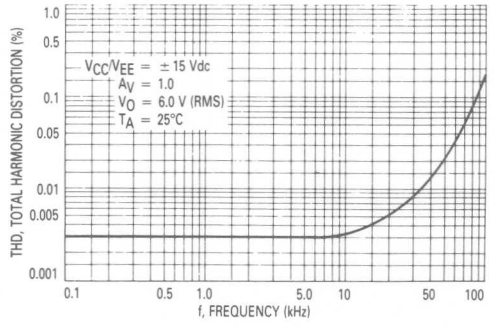


FIGURE 13 — TOTAL HARMONIC DISTORTION versus FREQUENCY



REPRESENTATIVE CIRCUIT SCHEMATIC
(Each Amplifier)

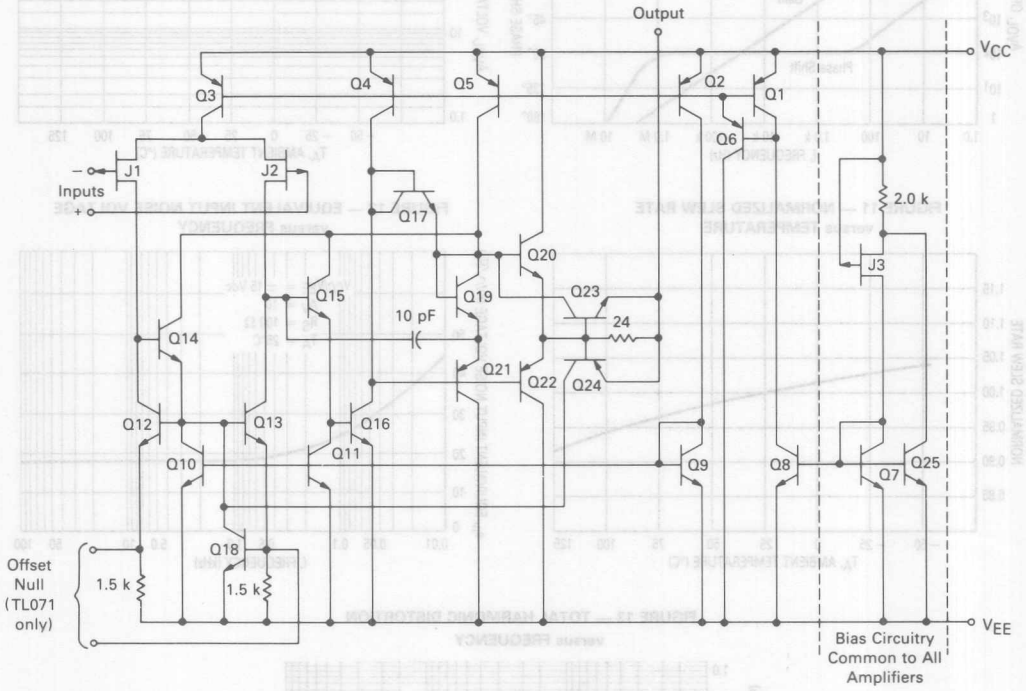


FIGURE 14 — AUDIO TONE CONTROL AMPLIFIER

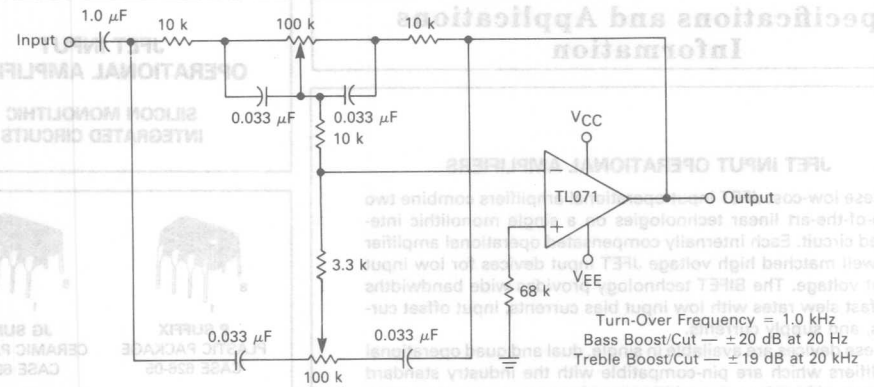
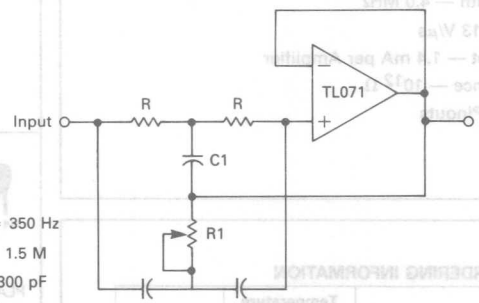


FIGURE 15 — HIGH Q NOTCH FILTER



$$f_o = \frac{1}{2\pi RC} = 350 \text{ Hz}$$

$$R = 2R1 = 1.5 \text{ M}$$

$$C = \frac{C1}{2} = 300 \text{ pF}$$

MOTOROLA

TL081
TL082
TL084

Specifications and Applications Information

JFET INPUT OPERATIONAL AMPLIFIERS

These low-cost JFET input operational amplifiers combine two state-of-the-art linear technologies on a single monolithic integrated circuit. Each internally compensated operational amplifier has well matched high voltage JFET input devices for low input offset voltage. The BIFET technology provides wide bandwidths and fast slew rates with low input bias currents, input offset currents, and supply currents.

These devices are available in single, dual and quad operational amplifiers which are pin-compatible with the industry standard MC1741, MC1458, and the MC3403/LM324 bipolar products. Devices with an "M" suffix are specified over the military operating temperature range of −55°C to +125°C and those with a "C" suffix are specified from 0°C to +70°C.

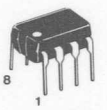
- Input Offset Voltage Options of 3.0, 6.0, and 15 mV Max
- Low Input Bias Current — 30 pA
- Low Input Offset Current — 5.0 pA
- Wide Gain Bandwidth — 4.0 MHz
- High Slew Rate — 13 V/μs
- Low Supply Current — 1.4 mA per Amplifier
- High Input Impedance — 10^{12} Ω
- Industry Standard Pinouts

ORDERING INFORMATION

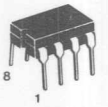
Op Amp Function	Device	Temperature Range	Package
Single	TL081ACD, BCD, CD	0 to +70°C	SO-8
	TL081ACJG, BCJG, CJG		Ceramic DIP
	TL081ACP, BCP, CP		Plastic DIP
	TL081MJG	−55 to +125°C	Ceramic DIP
Dual	TL082ACD, BCD, CD	0 to +70°C	SO-8
	TL082ACJG, BCJG, CJG		Ceramic DIP
	TL082ACP, BCP, CP		Plastic DIP
	TL082MJG	−55 to +125°C	Ceramic DIP
Quad	TL084ACD, BCD, CD	0 to +70°C	SO-14
	TL084ACJ, BCJ, CJ		Ceramic DIP
	TL084ACN, BCN, CN		Plastic DIP
	TL084MJ	−55 to +125°C	Ceramic DIP

JFET INPUT OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUITS



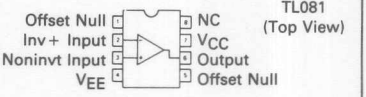
P SUFFIX
PLASTIC PACKAGE
CASE 626-05



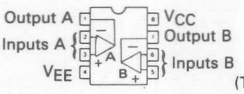
JG SUFFIX
CERAMIC PACKAGE
CASE 693-02



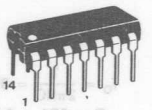
D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SO-8



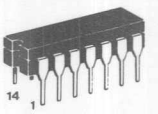
TL081 (Top View)



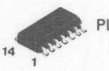
TL082 (Top View)



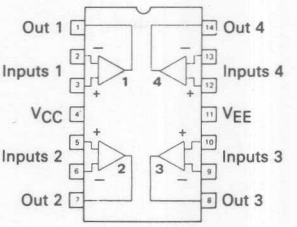
N SUFFIX
PLASTIC PACKAGE
CASE 646-06
(TL084 Only)



J SUFFIX
CERAMIC PACKAGE
CASE 632-08
(TL084 Only)



D SUFFIX
PLASTIC PACKAGE
CASE 751A-02
SO-14



TL084 (Top View)

MAXIMUM RATINGS

Rating	Symbol	TL08__M	TL08__C TL08__AC TL08__BC	Unit
Supply Voltage	V_{CC} V_{EE}	+18 −18	+18 −18	V
Differential Input Voltage	V_{ID}	±30	±30	V
Input Voltage Range (Note 1)	V_{IDR}	±15	±15	V
Output Short-Circuit Duration (Note 2)	t_S	Continuous		
Power Dissipation Plastic Package (N,P) Derate above T_A = +47°C Ceramic Package (J,JG) Derate above T_A = +82°C	 P_D $1/\theta_{JA}$ P_D $1/\theta_{JA}$	 — — 680 10	 680 10 680 10	 mW mW/°C mW mW/°C
Operating Ambient Temperature Range	T_A	−55 to +125	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	−65 to +150	°C

NOTES: 1. The magnitude of the input voltage must not exceed the magnitude of the supply voltage or 15 volts, whichever is less.
2. The output may be shorted to ground or either supply. Temperature and/or supply voltages must be limited to ensure that power dissipation ratings are not exceeded.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25°C unless otherwise noted).

Characteristic	Symbol	TL08__M			TL08__C TL08__AC TL08__BC			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq$ 10 k, V_{CM} = 0) TL081, TL082 TL084 TL08__A TL08__B	V_{IO}	 — — — —	 3.0 3.0 — —	 6.0 9.0 — —	 — — — —	 5.0 5.0 3.0 2.0	 15 15 6.0 3.0	mV
Average Temperature Coefficient of Input Offset Voltage R_S = 50 Ω, T_A = T_{low} to T_{high} (Note 3)	$\Delta V_{IO}/\Delta T$	—	10	—	—	10	—	μV/°C
Input Offset Current (V_{CM} = 0) (Note 4) TL08__ TL08__A, TL08__B	I_{IO}	 — —	 5.0 —	 100 —	 — —	 5.0 5.0	 200 100	pA
Input Bias Current (V_{CM} = 0) (Note 4) TL08__ TL08__A, TL08__B	I_{IB}	 — —	 30 —	 200 —	 — —	 30 30	 400 200	pA
Input Resistance	r_i	—	10^{12}	—	—	10^{12}	—	Ω
Common Mode Input Voltage Range TL08__ TL08__A, TL08__B	V_{ICR}	 ±11 —	 +15, −12 —	 — —	 ±10 ±11	 +15, −12 +15, −12	 — —	V
Large-Signal Voltage Gain (V_O = ±10 V, $R_L \geq$2.0 k) TL08__ TL08__A, TL08__B	A_{VOL}	 25 —	 150 —	 — —	 25 50	 150 150	 — —	V/mV
Output Voltage Swing (Peak-to-Peak) R_L = 10 k	V_O	24	28	—	24	28	—	V
Common Mode Rejection Ratio ($R_S \leq$10 k) TL08__ TL08__A, TL08__B	CMRR	 80 —	 100 —	 — —	 70 80	 100 100	 — —	dB
Supply Voltage Rejection Ratio ($R_S \leq$10 k) TL08__ TL08__A, TL08__B	PSRR	 80 —	 100 —	 — —	 70 80	 100 100	 — —	dB
Supply Current (Each Amplifier)	I_D	—	1.4	2.8	—	1.4	2.8	mA
Unity Gain Bandwidth	BW	—	4.0	—	—	4.0	—	MHz

Characteristic	Symbol	TL08__M Min	TL08__M Typ	TL08__M Max	TL08__C, TL08__AC, TL08__BC Min	TL08__C, TL08__AC, TL08__BC Typ	TL08__C, TL08__AC, TL08__BC Max	Unit
Slew Rate (See Figure 1) V_{in} = 10 V, R_L = 2.0 k, C_L = 100 pF	SR	8.0	13	—	—	13	—	V/μs
Rise Time (See Figure 1)	t_r	—	0.1	—	—	0.1	—	μs
Overshoot Factor V_{in} = 20 mV, R_L = 2.0 k, C_L = 100 pF	—	—	10	—	—	10	—	%
Equivalent Input Noise Voltage R_S = 100 Ω, f = 1000 Hz	e_n	—	25	—	—	25	—	nV/√Hz
Channel Separation A_V = 100	—	—	120	—	—	120	—	dB

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = T_{low} to T_{high} [Note 3].)

Characteristic	Symbol	TL08__M Min	TL08__M Typ	TL08__M Max	TL08__C, TL08__AC, TL08__BC Min	TL08__C, TL08__AC, TL08__BC Typ	TL08__C, TL08__AC, TL08__BC Max	Unit
Input Offset Voltage (R_S ≤10 k, V_{CM} = 0)	V_{IO}							mV
TL081, TL082		—	—	9.0	—	—	20	
TL084		—	—	15	—	—	20	
TL08__A		—	—	—	—	—	7.5	
TL08__B		—	—	—	—	—	5.0	
Input Offset Current (V_{CM} = 0) (Note 4)	I_{IO}							nA
TL08__		—	—	20	—	—	5.0	
TL08__A, TL08__B		—	—	—	—	—	3.0	
Input Bias Current (V_{CM} = 0) (Note 4)	I_{IB}							nA
TL08__		—	—	50	—	—	10	
TL08__A, TL08__B		—	—	—	—	—	7.0	
Large-Signal Voltage Gain (V_O = ±10 V, R_L≥2.0 k)	A_{VOL}							V/mV
TL08__		15	—	—	15	—	—	
TL08__A, TL08__B		—	—	—	25	—	—	
Output Voltage Swing (Peak-to-Peak)	V_O							V
(R_L≥10 k)		24	—	—	24	—	—	
(R_L≥2.0 k)		20	—	—	20	—	—	

NOTES (continued):

3. T_{low} = −55°C for TL081M, TL082M, TL084M; T_{high} = +125°C for TL081M, TL082M, TL084M
   = 0°C for TL081C, TL081AC, TL081BC; = +70°C for TL081C, TL081AC, TL081BC
   TL082C, TL082AC, TL082BC; TL082C, TL082AC, TL082BC
   TL084C, TL084AC, TL084BC; TL084C, TL084AC, TL084BC
4. Input Bias currents of JFET input Op Amps approximately double for every 10°C rise in junction temperature as shown in Figure 3. To maintain junction temperature as close to ambient temperature as possible, pulse techniques must be used during test.

TEST CIRCUITS

FIGURE 1 — UNITY GAIN VOLTAGE FOLLOWER

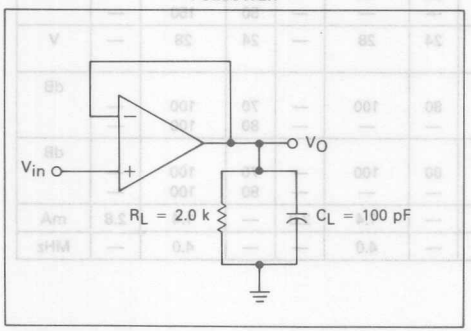


FIGURE 2 — INVERTING GAIN OF 10 AMPLIFIER

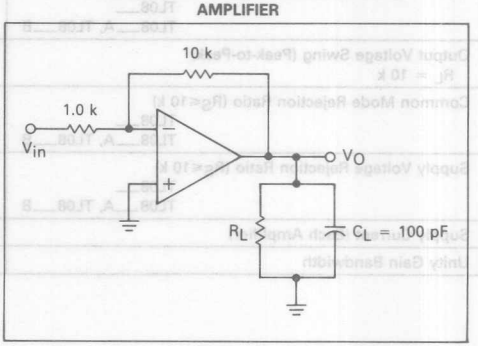


FIGURE 3 — INPUT BIAS CURRENT versus TEMPERATURE

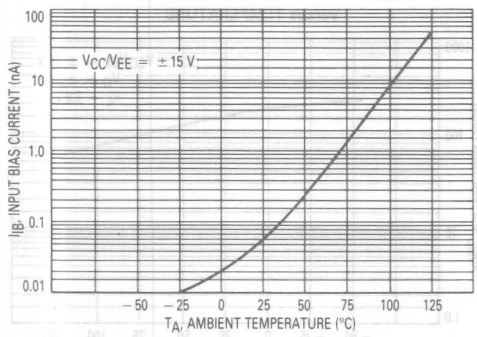


FIGURE 4 — OUTPUT VOLTAGE SWING versus FREQUENCY

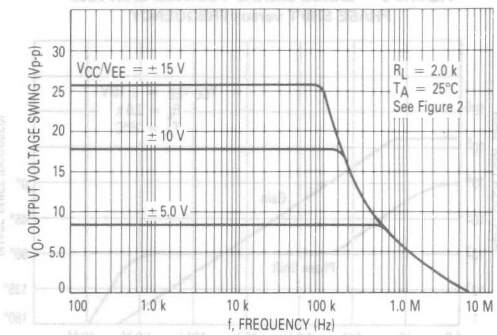


FIGURE 5 — OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

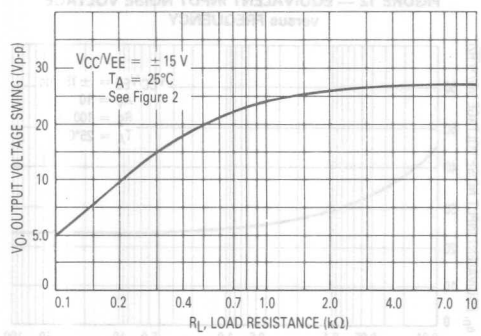


FIGURE 6 — OUTPUT VOLTAGE SWING versus SUPPLY VOLTAGE

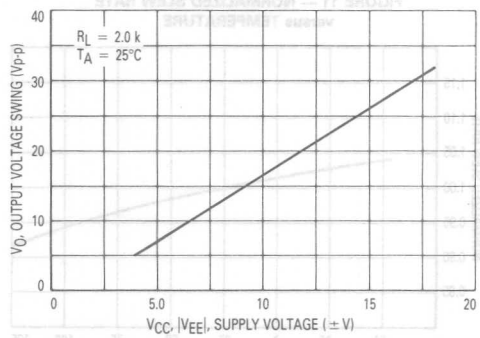


FIGURE 7 — OUTPUT VOLTAGE SWING versus TEMPERATURE

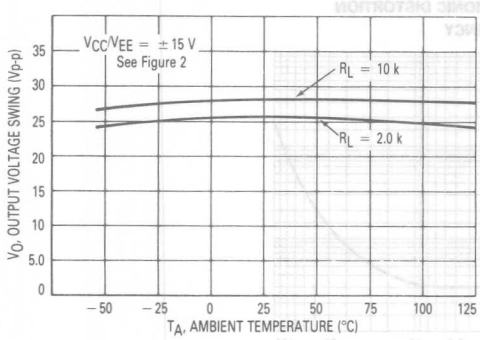
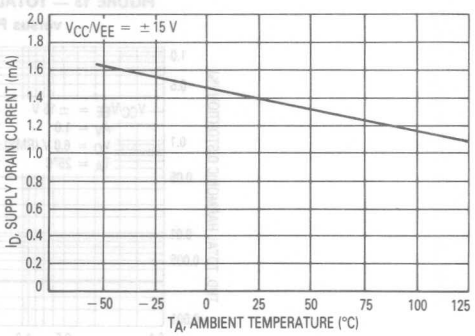


FIGURE 8 — SUPPLY CURRENT PER AMPLIFIER versus TEMPERATURE



2

FIGURE 9 — LARGE-SIGNAL VOLTAGE GAIN AND PHASE SHIFT versus FREQUENCY

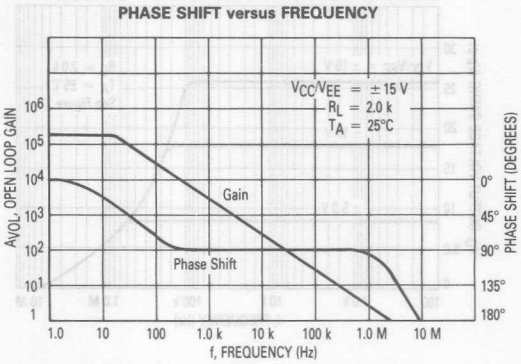


FIGURE 10 — LARGE-SIGNAL VOLTAGE GAIN versus TEMPERATURE

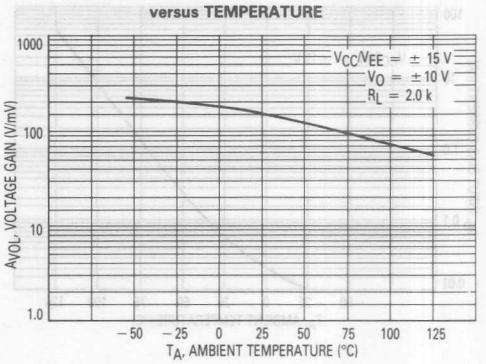


FIGURE 11 — NORMALIZED SLEW RATE versus TEMPERATURE

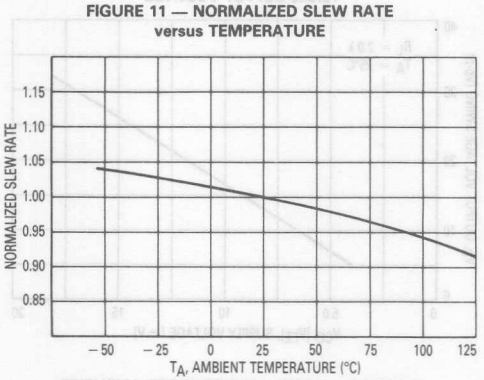


FIGURE 12 — EQUIVALENT INPUT NOISE VOLTAGE versus FREQUENCY

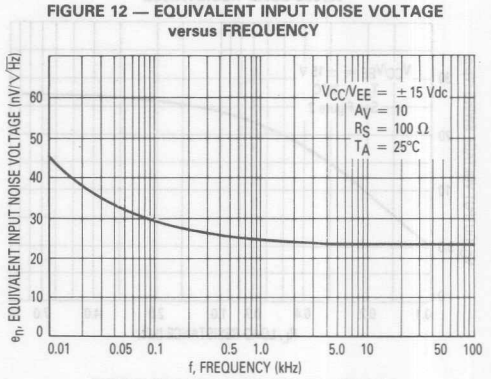
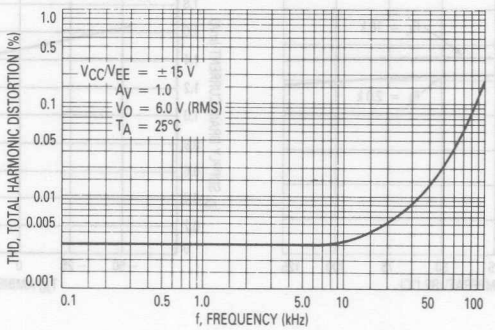
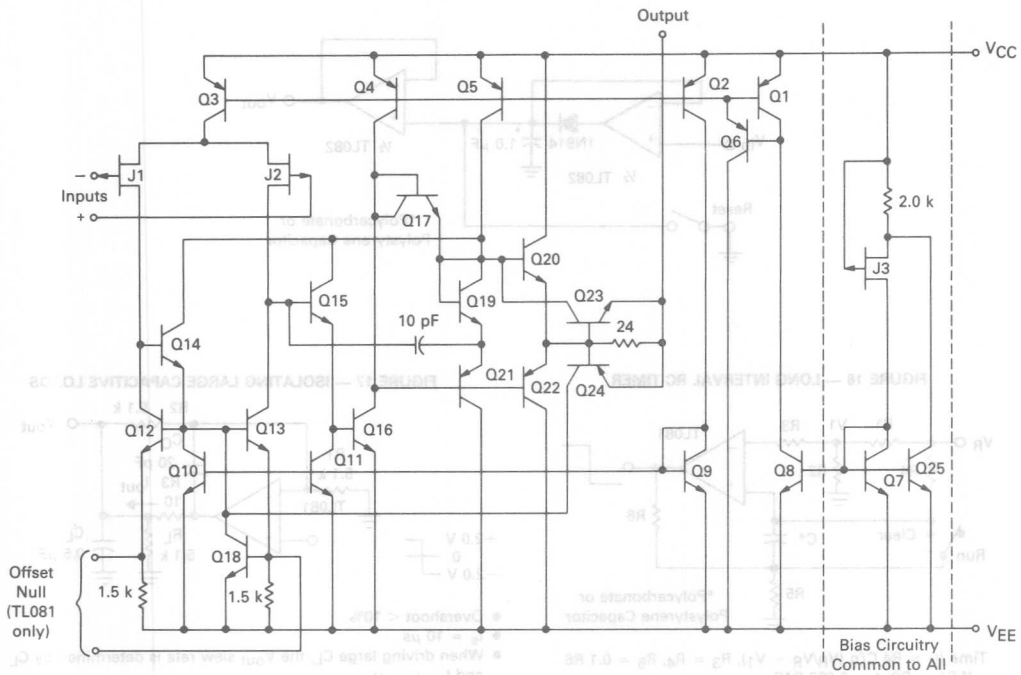


FIGURE 13 — TOTAL HARMONIC DISTORTION versus FREQUENCY

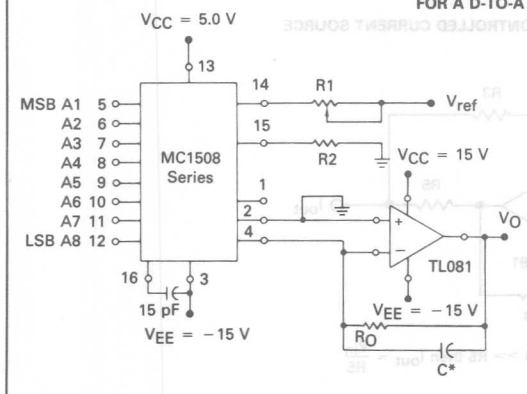


REPRESENTATIVE CIRCUIT SCHEMATIC
(Each Amplifier)



TYPICAL APPLICATIONS

FIGURE 14 — OUTPUT CURRENT TO VOLTAGE TRANSFORMATION FOR A D-TO-A CONVERTER



Settling time to within ½ LSB (± 19.5 mV) is approximately 4.0 μs from the time all bits are switched.

*The value of C may be selected to minimize overshoot and ringing (C ≈ 68 pF).

Theoretical V_O

$$V_O = \frac{V_{ref}}{R1}(R_O)\left[\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right]$$

Adjust V_{ref}, R1 or R_O so that V_O with all digital inputs at high level is equal to 9.961 volts.

V_{ref} = 2.0 Vdc
$R_1 = R2 \approx 1.0\ k\Omega$
$R_O = 5.0\ k\Omega$

$$V_O = \frac{2.0\ V}{1.0\ k}(5.0\ k)\left[\frac{1}{2}+\frac{1}{4}+\frac{1}{8}+\frac{1}{16}+\frac{1}{32}+\frac{1}{64}+\frac{1}{128}+\frac{1}{256}\right]$$

$$= 10\ V\left[\frac{255}{256}\right] = 9.961\ V$$

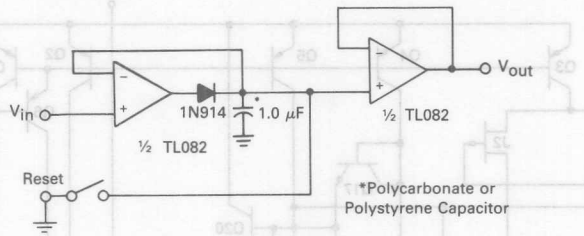
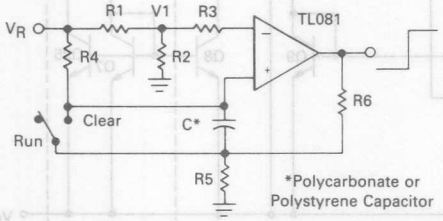


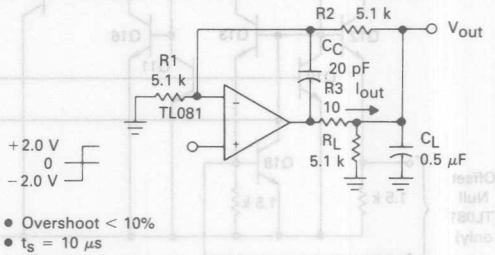
FIGURE 16 — LONG INTERVAL RC TIMER



Time (t) = R4 Cℓn ($V_R/V_R - V_1$), $R_3 = R_4$, $R_5 = 0.1\ R6$
If R1 = R2: t = 0.693 R4C
Design Example: 100 Second Timer

V_R = 10 V	C = 1.0 μF	R3 = R4 = 144 M
R6 = 20 k	R5 = 2.0 k	R1 = R2 = 1.0 k

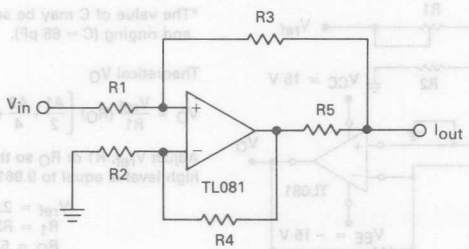
FIGURE 17 — ISOLATING LARGE CAPACITIVE LOADS



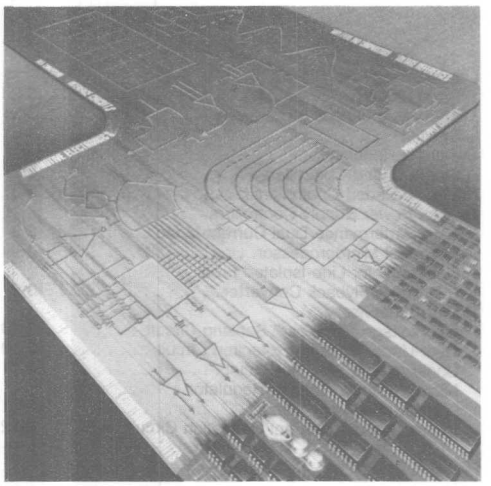
- Overshoot < 10%
- t_s = 10 μs
- When driving large C_L, the V_{out} slew rate is determined by C_L and $I_{out(max)}$:

$$\frac{\Delta V_{out}}{\Delta t} = \frac{I_{out}}{C_L} \cong \frac{0.02}{0.5}\ V/\mu s = 0.04\ V/\mu s \text{ (with } C_L \text{ shown)}$$

FIGURE 18 — VOLTAGE CONTROLLED CURRENT SOURCE



If R1 through R4 >> R5 then $I_{out} = \frac{V_{in}}{R5}$



Power Circuits

3

In Brief . . .

In most electronic systems some form of voltage regulation is required. Yesterday the task of voltage regulator design was tediously accomplished with discrete devices, and the results were quite often complex and costly. Today with bipolar monolithic regulators, this task has been reduced considerably. The designer now has a wide choice of fixed, low V_{diff}, adjustable, and tracking series-type regulators.

These devices incorporate many built-in protection features making them virtually immune to the catastrophic failures encountered in older discrete designs.

The Switching Power Supply continues to increase in popularity and is one of the fastest growing markets in the world of power conversion. They offer the designer several important advantages over that of linear series-pass regulators. These advantages include significant advancements in the areas of size and weight reduction, efficiency, and the ability to perform voltage step-up and voltage-inverting. Motorola offers an ever increasing diverse portfolio of full featured switching regulator control circuits which meet the needs of today's modern compact electronic equipment.

Selector Guide

- Linear Voltage Regulators 3-2
- Switching Regulators 3-7
- Special Power Controllers 3-9
- Power Supervisory 3-10

Alphanumeric Listing 3-13

Related Application Notes 3-14

Data Sheets 3-15

Power Circuits

Linear Voltage Regulators

Fixed Output

3

These low-cost monolithic circuits provide positive and/or negative regulation at currents from 100 mA to 3.0 A. They are ideal for on-card regulation employing current limiting and thermal shutdown. Low V_{diff} devices are offered for battery powered systems.

Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

Linear Voltage Regulators
- Fixed Output 3-2
- Adjustable Output 3-5
- Special 3-6

Switching Regulators
- Single-Ended Controllers 3-7
- Double-Ended Controllers 3-8

Special Power Supply Controllers
- High Performance Dual Current-Mode 3-9
- Universal Microprocessor 3-9
- Control IC for Line-Isolated Free Running Flyback Converter 3-9

Power Supervisory
- Overvoltage "Crowbar" Sensing Circuit 3-10
- Over-Under Voltage Protection Circuit 3-10
- Undervoltage Sensing Circuit 3-11
- Microprocessor Voltage Regulator and Supervisory Circuit 3-11
- Series Switch Transient Protection Circuit 3-12

Fixed-Voltage, 3-Terminal Regulators for Positive or Negative Polarity Power Supplies

V_{out} Volts	Tol.† Volts	I_O mA Max	Device Positive Output	Device Negative Output	V_{in} Min/Max	Reg_{line} mV	Reg_{load} mV	$\Delta V_O/\Delta T$ mV/°C Typ	Case Suffix
5	±0.5	100	LM2931-5.0	—	5.6/40	30	50	1.0	Z, T
	±0.25		MC78L05C	MC79L05C	6.7/30	200	60		P, G
			LM2931A-5.0	—	5.6/40	30	50		Z, T
			MC78L05AC	MC79L05AC	6.7/30	150	60		P, G
		500	MC78M05C	MC79M05C	7/35	100	100	1.0	G, T
	±0.4	1500	LM109	—				1.1	K, H
			LM209	—					
	±0.25		LM309	—		50		1.0	
	±0.35		MC7805*	—	8.0/35			0.6	K
	±0.25		MC7805B#	—	8/35	100		1.0	T
			MC7805C	MC7905C	7/35				K, T
	±0.2		MC7805A*	—	7.5/35	10	50	0.6	K
			MC7805AC	MC7905AC			100		K, T
	±0.25		LM140-5*	—	7.0/35	50	50		K
	±0.2		LM140A-5*	—		10	25		
	±0.25		LM340-5	—		50	50		K, T
	±0.2		LM340A-5	—		10	25		
	±0.1		TL780-05C	—	7.0/35	5.0	25	0.06	KC
	±0.25	3000	MC78T05C	—	7.3/35	25	30	0.1	K, T
	±0.2		MC78T05AC	—		10	25		

#T_J = −40° to +125°C †Output Voltage Tolerance for Worst Case *T_J = −55° to +150°C

(continued)

Fixed Output Voltage Regulators (continued)

V_{out} Volts	Tol.† Volts	I_O mA Max	Device Positive Output	Device Negative Output	V_{in} Min/Max	Reg_{line} mV	Reg_{load} mV	$\Delta V_O/\Delta T$ mV/°C Typ	Case Suffix
5	±0.4	3000	LM123*	—	7.5/20	25	100	0.1	K
			LM223	—					
	±0.25		LM323	—					T
	±0.2		LM123A	—					K
			LM223A	—		15	50		
			LM323A	—					T
5.2	±0.26	1500	—	MC7905.2C	7.2/35	105	105	1.0	T
6	±0.3	500	MC78M06C	—	8/35	100	120	1.0	T
	±0.35	1500	MC7806*	—	9/35	60	100	0.7	K
	±0.3		MC7806B#	—		120	120		T
			MC7806C	MC7906C	8/35				K, T
	±0.24		MC7806AC	—	8.6/35	11	100		T
			LM140-6*	—	8/35	60	60		K
	±0.3		LM340-6	—					K, T
8	±0.8	100	MC78L08C	—	9.7/30	200	80	—	P, G
			MC78L08AC	—		175			
	±0.4	500	MC78M08C	—	10/35	100	160	1.0	G, T
		1500	MC7808*	—	11.5/35	80	100		K
			MC7808B#	—		160	160		T
			MC7808C	MC7908C	10.5/35				K, T
	±0.3		MC7808AC	—	10.6/35	13	100		T
	±0.4		LM140-8*	—	10.5/35	80	80		K
			LM340-8	—					K, T
		3000	MC78T08C	—	10.4/35	35	30	0.16	
12	±1.2	100	MC78L12C	MC79L12C	13.7/35	250	100	—	P, G
	±0.6		MC78L12AC	MC79L12AC					
		500	MC78M12C	MC79M12C	14/35	100	240	1.0	G, T
		1500	MC7812*	—	15.5/35	120	120	1.5	K
			MC7812B#	—		240	240		T
			MC7812C	MC7912C	14.5/35				K, T
	±0.5		MC7812A*	—	14.8/35	18	50		K
			MC7812AC	—			100		T
	±0.6		LM140-12*	—	14.5/35	120	120	1.5	K
	±0.5		LM140A-12*	—		18	32		
	±0.6		LM340-12	—		120	120		K, T
	±0.5		LM340A-12	—		18	32		
	±0.24		TL780-12C	—		5.0		0.15	KC
	±0.6	3000	MC78T12C	—	14.5/35	45	30	0.24	K, T
	±0.5		MC78T12AC	—		18	25		

#T_J = −40° to +125°C †Output Voltage Tolerance for Worst Case *T_J = −55° to +150°C

(continued)

Fixed Output Voltage Regulators (continued)

V_{out} Volts	Tol.† Volts	I_O mA Max	Device Positive Output	Device Negative Output	V_{in} Min/Max	Reg_{line} mV	Reg_{load} mV	$\Delta V_O/\Delta T$ mV/°C Typ	Case Suffix
15	±1.5	100	MC78L15C	MC79L15C	16.7/35	300	150	—	P, G
	±0.75		MC78L15AC	MC79L15A					
		500	MC78M15C	MC79M15C	17/35	100	300	1.0	G, T
		1500	MC7815*	—	18.5/35	150	150	1.8	K
			MC7815B#	—		300	300		T
			MC7815C	MC7915C	17.5/35				K, T
	±0.6		MC7815A*	—	17.9/35	22	50		K
			MC7815AC	—			100		K, T
	±0.75		LM140-15*	—	17.5/35	150	150		K
	±0.6		LM140A-15*	—		22	35		
	±0.75		LM340-15	—		150	150		K, T
	±0.6		LM340A-15	—		22	35		
	±0.3		TL780-15C	—		15	60	0.18	KC
	±0.75	3000	MC78T15C	—	17.5/40	55	30	0.3	K, T
	±0.6		MC78T15AC	—		22	25		
18	±1.8	100	MC78L18C	MC79L18C	19.7/35	325	170	—	P
	±0.9		MC78L18AC	MC79L18AC					
		500	MC78M18C	—	20/35	100	360	1.0	G, T
		1500	MC7818*	—	22/35	180	180	2.3	K
			MC7818B#	—		360	360		T
	±0.7		MC7818C	MC7918C	21/35				K, T
			MC7818AC	—		31	100		T
	±0.9		LM340-18	—		180	180		T
20	±1.0	500	MC78M20C	—	22/40	10	400	1.1	G, T
24	±2.4	100	MC78L24C	MC79L24C	25.7/40	350	200	—	P
	±1.2		MC78L24AC	MC79L24AC		300			
		500	MC78M24C	—	26/40	100	480	1.2	G, T
		1500	MC7824*	—	28/40	240	240	3.0	K
			MC7824B#	—		480	480		T
			MC7824C	MC7924C	27/40				K, T
	±1.0		MC7824AC	—	27.3/40	36	100		T
	±1.2		LM340-24	—		240	240		T

#T_J = −40° to +125°C †Output Voltage Tolerance for Worst Case *T_J = −55° to +150°C

Adjustable Output Voltage Regulators

Motorola offers a broad line of adjustable output voltage regulators with a variety of output current capabilities. Adjustable voltage regulators provide users the capability of stocking a single integrated circuit providing a wide range of output voltages for industrial and communications applications. The three-terminal devices require only two external resistors to set the output voltage.

Positive Output Regulators

I_O mA Max	Device	Suffix	V_{out} Volts Min	V_{out} Volts Max	V_{in} Volts Min	V_{in} Volts Max	$V_{in} - V_{out}$ Differential Volts Min	P_D Watts Max T_A = 25°C	P_D Watts Max T_C = 25°C	Regulation % V_{out} @ T_A = 25°C Max Line	Regulation % V_{out} @ T_A = 25°C Max Load	TC V_{out} Typ %/°C	T_J = °C Max	Case
100	LM317L	H,Z	1.2	37	5.0	40	3.0	Internally Limited		0.04	0.5	0.006	125	29,79
	LM217L#									0.02	0.3	0.004	150	
	LM117L*											0.003		
	LM2931C	T	3.0	24	3.16		0.6			0.15	1.0	—	125	314D
150	MC1723	CP	2.0	37	9.5	40	3.0	1.25	—	0.1	0.3	0.003	150	646
		CG						1.0	2.1			0.003		603C
		G										0.002		
		CL						1.5	—			0.003	175	632
		L							—			0.002		
500	LM317M	T	1.2	37	5.0	40	3.0	Internally Limited		0.04	0.5	0.0056	125	221A
1500	LM317	T	1.2	37	5.0	40	3.0	Internally Limited		0.04	0.5	0.006	125	221A
	LM317	H, K												79, 1
	LM217#											0.004		
	LM117*									0.02	0.3	0.003	150	
3000	LM350	T	1.2	33	5.0	36	3.0	Internally Limited		0.03	0.5	0.008	125	221A
	LM350	K												1
	LM250#									0.01	0.3	0.0057	150	
	LM150*											0.0051		

Negative Output Regulators

I_O mA Max	Device	Suffix	V_{out} Volts Min	V_{out} Volts Max	V_{in} Volts Min	V_{in} Volts Max	$V_{in} - V_{out}$ Differential Volts Min	P_D Watts Max T_A = 25°C	P_D Watts Max T_C = 25°C	Regulation % V_{out} @ T_A = 25°C Max Line	Regulation % V_{out} @ T_A = 25°C Max Load	TC V_{out} Typ %/°C	T_J = °C Max	Case
500	LM337M	T	−1.2	−37	5.0	40	3.0	Internally Limited		0.04	1.0	0.0048	125	221A
1500	LM337	T	−1.2	−37	5.0	40	3.0	Internally Limited		0.04	1.0	0.0048	125	221A
	LM337	H, K												79, 1
	LM237#									0.02	0.5	0.0034	150	
	LM137*											0.0031		

#T_J = −25° to +150°C *T_J = −55° to +150°C

3

Floating Voltage and Current Regulators

Designed for laboratory type power supplies. Voltage is limited only by the break down voltage of associated, external, series-pass transistors.

V_{out} Volts		I_O mA			V_{aux} Volts		P_D Watts	$\Delta V_{ref}/V_{ref}$ %		$\Delta I_L/L_L$ %	TC V_{out} %/°C	
Min	Max	Max	Device	Suffix	Min	Max	Max	Line	Load	Max	Typ	Case
0	*	*	MC1466	L	21	30	0.75	0.015	0.015	0.2	0.001	632

*Dependent on characteristics of external series-pass elements.

Dual ±15 V Tracking Regulators

Internally, the device is set for ±15 V, but an external adjustment can change both outputs simultaneously, from 8.0 V to 20 V.

V_{out} Volts		I_O mA	V_{in} Volts				P_D Watts	Reg_{line}	Reg_{load}	TC %/°C (T_{low} to T_{high})	T_A	
Min	Max	Max	Min	Max	Device	Suffix	Max	mV	mV	Typ	°C	Case
14.8	15.2	±100	17	30	MC1468	G	0.8	10	10	3.0	0 to +75	603C
						L	1.0					632
					MC1568	G	0.8				−55 to +125	603C
						L	1.0					632

Microprocessor Voltage Regulator/Supervisory Circuit

A 5.0 V fixed output with many monitoring functions required in microprocessor-based systems.

V_{out}, V_{ref} Volts		I_{SINK} mA	V_{in} Volts		Reg_{line}	Reg_{load}			T_A	
Min	Max	Max	Min	Max	mV Max	mV Max	Device	Suffix	°C	Case
4.75	5.25	100	7.0	40	40	50	MC34160	P	0 to +70	648C
2.47	2.73	2.0	5.0		20	30	MC33160		−40 to +85	

Switching Regulators

Used as a control circuit in PWM, push-pull, bridge and series type Switchmode supplies, the devices include a voltage reference, oscillator, pulse-width modulator, phase splitter and output drive sections. Frequency and duty cycle are independently adjustable. Most of these devices also include one or two on-chip error amplifiers for voltage or current error signal feedback.

Single-Ended Controllers

These single-ended voltage- and current-mode controllers are designed for use in buck, boost, flyback, and forward converters. They are cost effective in applications that range from 0.1 to 200 watts power output.

I_O mA Max	V_{CC} Volts Min	V_{CC} Volts Max	V/I Operating Mode	Ref. Volts	Max Osc. Freq. (kHz)	Device	Suffix	T_A °C	Case
250	7.0	40	V	5.0 ± 5.0%	200	MC34060	P	0 to +70	646
							L		632
						MC35060	L	−55 to +125	
500				5.0 ± 1.5%		MC34060A	D	0 to +70	751A
							P		646
						MC33060A	D	−40 to +85	751A
							P		646
						MC35060A	L	−55 to +125	632
1000	4.2	12	I	1.25 ± 2.0%	300	MC34129	D	0 to +70	751A
							P		646
						MC33129	D	−40 to +85	751A
							P		646
	11.5	30		5.0 ± 2.0%	500	UC3842A	D	0 to +70	751A
							N		626
	11			5.0 ± 1.0%		UC2842A	D	−25 to +85	751A
							J		693
							N		626
	8.2			5.0 ± 2.0%		UC3843A	D	0 to +70	751A
							N		626
				5.0 ± 1.0%		UC2843A	D	−25 to +85	751A
							J		693
							N		626
1500	2.5	40	V	1.24 ± 5.2%#	100	μA78S40	PC	0 to +70	648
							DC		620
							PV	−40 to +85	648
							DM	−55 to +125	620
				1.25 ± 5.6%#		MC34063	P1	0 to +70	626
							U		693
						MC33063	P1	−40 to +85	626
							U		693
						MC35063	U	−55 to +125	
				1.25 ± 2.0%		MC34063A	D	0 to +70	751
							P1		626
						MC33063A	D	−40 to +85	751
							P1		626
						MC35063A	U	−55 to +125	693

Tolerance applies over the specified operating temperature range.

Double-Ended Controllers

These double-ended voltage-mode controllers are designed for use in push-pull, half-bridge, and full-bridge converters. They are cost effective in applications that range from 100 to 2000 watts power output.

I_O mA Max	V_{CC} Volts Min	V_{CC} Volts Max	V/I Operating Mode	Ref. Volts	Max Osc. Freq. (kHz)	Device	Suffix	T_A °C	Case
500	7.0	40	V	5.0 ± 5.0%#	200	TL494	CN	0 to +70	648
							CJ		620
							IN	−25 to +85	648
							IJ		620
							MJ	−55 to +125	
				5.0 ± 1.5%	300	TL594	CN	0 to +70	648
							IN	−25 to +85	
							MJ	−55 to +125	620
±500	8.0			5.1 ± 2.0%	400	SG3525A	N	0 to +70	648
							J		620
				5.1 ± 1.0%		SG2525A	N	−25 to +85	648
							J		620
						SG1525A	J	−55 to +125	
				5.1 ± 2.0%		SG3527A	N	0 to +70	648
							J		620
				5.1 ± 1.0%		SG2527A	N	−25 to +85	648
							J		620
						SG1527A	J	−55 to +125	
±200				5.0 ± 2.0%	350	SG3526	N	0 to +125*	707
							J		726
				5.0 ± 1.0%		SG2526	N	−25 to +150*	707
							J		726
						SG1526	J	−55 to +150*	

*Junction Temperature Range
#Tolerance applies over the specified operating temperature range.

Special Power Supply Controllers

High Performance Dual Current-Mode Controllers

Optimized for off-line AC-to-DC power supplies and DC-to-DC converters in the flyback topology. Applications include desktop computers, peripherals, televisions, games, and various consumer appliances.

I_O mA Max	V_{CC} Volts		V/I Operating Mode	Ref. Volts	Max Osc. Freq. (kHz)	Device	Suffix	T_A °C	Case
	Min	Max							
±1000	11	15.5	I	5.0±2.0%	500	MC34065	DW	0 to +70	751G
							P		648
						MC33065	DW	−40 to +85	751G
							P		648

Universal Microprocessor Power Supply Controller

TCA5600 — T_A = −40° to +75°C, Case 707

A versatile power supply control circuit for microprocessor-based systems which is mainly intended for automotive applications and battery powered instruments. The device provides a power-on RESET delay and a watchdog feature for orderly microprocessor operation.

Regulated Outputs	Output Current mA	V_{CC} Volts		Ref. Volts	Key Supervisory Features
		Min	Max		
E^2PROM Programmable Output: 24 Volts (Write Mode) 5.0 Volts (Read Mode)	150 peak	6.0	35	2.5±3.2%	MPU Reset and Watchdog Circuit
Fixed Linear Output: 5.0 Volts	10 to external buffer transistor				

Control IC for Line-Isolated Free Running Flyback Converter

Regulates and monitors the switching transistor in power supplies based on the free oscillating flyback converter principle. Provides excellent Switchmode performance in Hi-Fi equipment, active loudspeakers, as well as applications in TV receivers and video recorders.

I_O mA Max	V_{CC} Volts		V/I Operating Mode	Ref. Volts	Max Osc. Freq. (kHz)	Device	Suffix	T_A °C	Case
	Min	Max							
±1500	12.3	20	V	4.2±5.0%	100	TDA4601	—	−15 to +85	762
							B		707

Power Supervisory

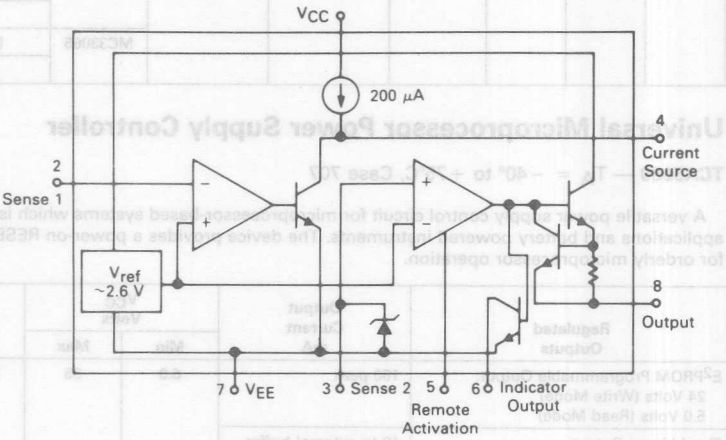
A variety of Power Supervisory Circuits are offered. Overvoltage sensing circuits which drive "crowbar" SCR's are provided in several configurations from a low cost three-terminal version to 8-pin devices which provide pin-programmable trip-voltages or additional features such as an indicator output drive and remote activation capability. An over-under-voltage protection circuit is also offered.

3

Overvoltage "Crowbar" Sensing Circuit

MC3523U — T_A = −55° to +125°C, Case 693
MC3423P1,U — T_A = 0° to +70°C, Case 626, 693

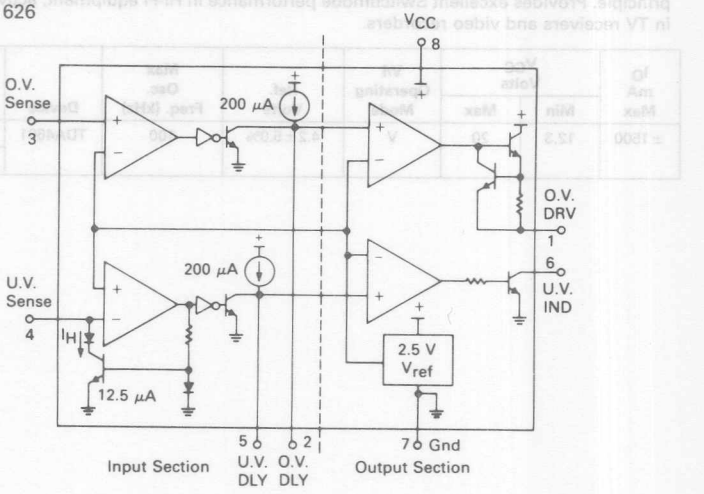
This device can protect sensitive circuitry from power supply transients or regulator failure when used with an external "Crowbar" SCR. The device senses voltage and compares it to an internal 2.6 V reference. Overvoltage trip is adjustable by means of an external resistive voltage divider. A minimum duration before trip is programmable with an external capacitor. Other features include a 300 mA high current output for driving the gate of a "Crowbar" SCR, an open-collector indicator output and remote activation capability.



Over-Under Voltage Protection Circuit

MC3425P1 — T_A = 0° to +70°C, Case 626

The MC3425 is a power supply supervisory circuit containing all the necessary functions required to monitor over- and under-voltage fault conditions. This device features dedicated over- and under-voltage sensing channels with independently programmable time delays. The over-voltage channel has a high current Drive Output for use in conjunction with an external SCR "Crowbar" for shutdown. The under-voltage channel input comparator has hysteresis which is externally programmable, and an open-collector output for fault indication.

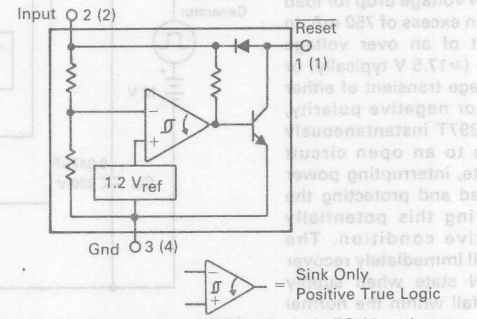


Undervoltage Sensing Circuit

MC34064P-5, D-5 — T_A = 0° to +70°C, Case 29, 751
MC33064P-5, D-5 — T_A = −40° to +85°C, Case 29, 751

The MC34064 is an undervoltage sensing circuit specifically designed for use as a reset controller in microprocessor-based systems. It offers the designer an economical solution for low voltage detection with a single external resistor. The MC34064 features a trimmed-in-package bandgap reference, and a comparator with precise thresholds and built-in hysteresis to prevent erratic reset operation. The open collector reset output is capable of sinking in excess of 10 mA, and operation is guaranteed down to 1.0 volt input with low standby current. These devices are packaged in 3-pin TO-92 and 8-pin surface mount packages.

Applications include direct monitoring of the 5.0 volt MPU/logic power supply used in appliance, automotive, consumer, and industrial equipment.



Pin numbers adjacent to terminals are for the 3 pin TO-92 package.
Pin numbers in parenthesis are for the D suffix SO-8 package.

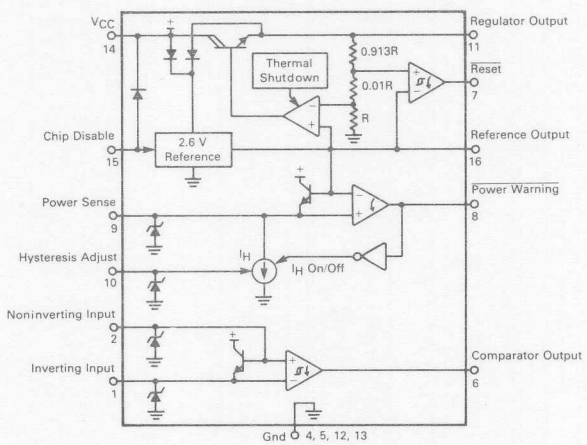
Microprocessor Voltage Regulator and Supervisory Circuit

MC34160P — T_A = 0° to +70°C, Case 648C
MC33160P — T_A = −40° to +85°C, Case 648C

The MC34160 Series is a voltage regulator and supervisory circuit containing many of the necessary monitoring functions required in microprocessor based systems. It is specifically designed for appliance and industrial applications offering the designer a cost effective solution with minimal external components. These integrated circuits feature a 5.0 V, 100 mA regulator with short circuit current limiting, pinned out 2.6 V bandgap reference, low voltage reset comparator, power warning comparator with programmable hysteresis, and an uncommitted comparator ideally suited for microprocessor line synchronization.

Additional features include a chip disable input for low standby current, and internal thermal shut-down for over temperature protection.

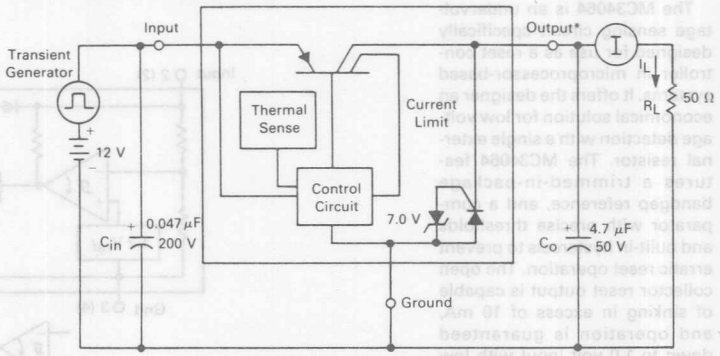
These devices are contained in a 16 pin dual-in-line heat tab plastic package for improved thermal conduction.



Series Switch Transient Protection Circuit

MC3397T — T_J = −40° to +125°C, Case 221A

This device acts as a saturated series pass element with a very low voltage drop for load currents in excess of 750 mA. In the event of an over voltage condition (≥17.5 V typically) or high voltage transient of either positive or negative polarity, the MC3397T instantaneously switches to an open circuit (OFF) state, interrupting power to the load and protecting the load during this potentially destructive condition. The device will immediately recover to an ON state when supply voltages fall within the normal operating range.



NOTE:
*Depending on Load Current and Transient Duration, an Output Capacitor (C_O) of sufficient value may be used to hold up Output Voltage during the Transient, and absorb Turn-off Delay Voltage Overshoot.

Linear Voltage Regulators

Device	Function	Page
LM109	Positive Voltage Regulator	3-15
LM117	3-Terminal Adjustable Positive Voltage Regulator	3-20
LM117L	Low-Current 3-Terminal Adjustable Positive Voltage Regulator	3-28
LM123,A	3-Ampere, 5 Volt Positive Voltage Regulator	3-36
LM137	3-Terminal Adjustable Negative Voltage Regulator	3-42
LM140,A	Three-Terminal Positive Fixed Voltage Regulators	3-49
LM150	3-Terminal Adjustable Positive Voltage Regulator	3-65
LM209	Positive Voltage Regulator	3-15
LM217	3-Terminal Adjustable Positive Voltage Regulator	3-20
LM217L	Low-Current 3-Terminal Adjustable Positive Voltage Regulator	3-28
LM223,A	3-Ampere, 5 Volt Positive Voltage Regulator	3-36
LM237	3-Terminal Adjustable Negative Voltage Regulator	3-42
LM250	3-Terminal Adjustable Positive Voltage Regulator	3-65
LM309	Positive Voltage Regulator	3-15
LM317	3-Terminal Adjustable Positive Voltage Regulator	3-20
LM317L	Low-Current 3-Terminal Adjustable Positive Voltage Regulator	3-28
LM317M	Medium-Current 3-Terminal Adjustable Positive Voltage Regulator	3-73
LM323,A	3-Ampere, 5 Volt Positive Voltage Regulator	3-36
LM337	3-Terminal Adjustable Negative Voltage Regulator	3-42
LM337M	Medium-Current 3-Terminal Adjustable Negative Voltage Regulator	3-81
LM340,A	Three-Terminal Positive Fixed Voltage Regulators	3-49
LM350	3-Terminal Adjustable Positive Voltage Regulator	3-65
LM2931 Series	Low Dropout Voltage Regulators	3-88
MC1466L	Voltage and Current Regulator	3-95
MC1468	Dual ± 15-Volt Tracking Regulator	3-105
MC1568	Dual ± 15-Volt Regulator	3-105
MC1723,C	Adjustable Positive or Negative Voltage Regulator	3-111
MC7800 Series	3-Terminal Positive Voltage Regulators	3-132
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Switching Regulators (continued)

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RELATED APPLICATION NOTES

Application Note	Title	Related Device
AN703	Designing Digitally-Controlled Power Supplies	MC1466, MC1723
AN920A	Theory and Applications of the MC34063 and μA78S40 Switching Regulator Control Circuits	MC34063, μA78S40
AN778	Mounting Techniques for Power Semiconductors	LM317, LM337, MC7800, MC78M00, MC7900, MC79M00
AN954	A Unique Converter Configuration	MC34063
AN976	A New High Performance Current-Mode Controller Teams Up with Current Sensing Power MOSFETs	MC34129
AN983	A Simplified Power Supply Design Using the TL494 Control Circuit	TL494
ANE002	130 W Ringing Choice Power Supply Using TDA4601	TDA4601,B

MOTOROLA

LM109
LM209
LM309

POSITIVE VOLTAGE REGULATOR

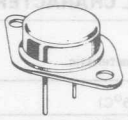
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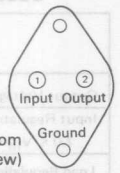
MONOLITHIC POSITIVE THREE-TERMINAL FIXED VOLTAGE REGULATOR

A versatile positive fixed +5.0-volt regulator designed for easy application as on on-card, local voltage regulator for digital logic systems. Current limiting and thermal shutdown are provided to make the units extremely rugged.

In most applications only one external component, a capacitor, is required in conjunction with the LM109 Series devices. Even this component may be omitted if the power-supply filter is not located an appreciable distance from the regulator.

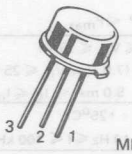
- High Maximum Output Current — Over 1.0 Ampere in TO-204AA type Package — Over 200 mA in TO-205AD type Package.
- Minimum External Components Required
- Internal Short-Circuit Protection
- Internal Thermal Overload Protection
- Excellent Line and Load Transient Rejection
- Designed for Use with Popular MDTL and MTTL Logic

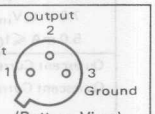




K SUFFIX
METAL PACKAGE
CASE 1-03
(Bottom View)

Pins 1 and 2 electrically isolated from case. Case is third electrical connection.

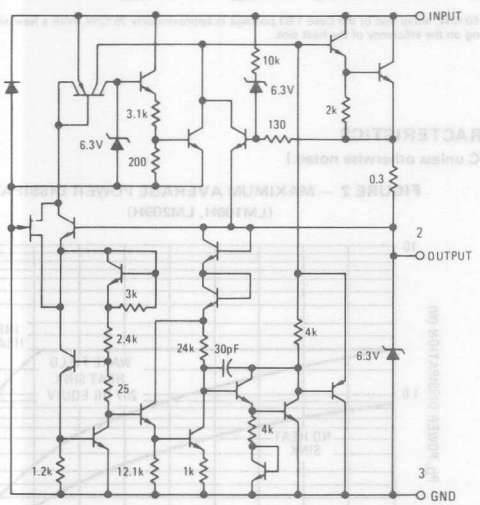




(Bottom View)

H SUFFIX
METAL PACKAGE
CASE 79-05

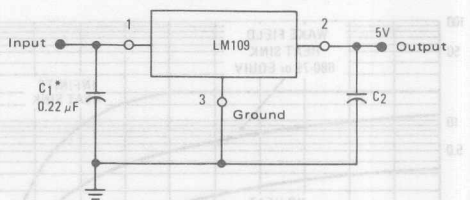
CIRCUIT SCHEMATIC



ORDERING INFORMATION		
Device	Tested Operating Temperature Range	Package
LM109H	T_J = −55°C to +150°C	Metal Can
LM109K	T_J = −55°C to +150°C	Metal Power
LM209H	T_J = −25°C to +150°C	Metal Can
LM209K	T_J = −25°C to +150°C	Metal Power
LM309H	T_J = 0°C to +125°C	Metal Can
LM309K	T_J = 0°C to +125°C	Metal Power

TYPICAL APPLICATION

FIXED 5.0 V REGULATOR



*Required if regulator is located an appreciable distance from power supply filter. Although no output capacitor is needed for stability, it does improve transient response.

Junction Temperature Range LM109 LM209 LM309	T_J	 −55 to +150 −25 to +150 0 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Lead Temperature (soldering, t = 60 s)	T_S	300	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	LM109/LM209[1] Min	Typ	Max	LM309[2] Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	4.7	5.05	5.3	4.8	5.05	5.2	Vdc
Input Regulation (T_J = +25°C) 7.0 ≤ V_{in} ≤ 25 V	Reg_{line}		4.0	50		4.0	50	mV
Load Regulation (T_J = +25°C) Case 1-03 5.0 mA ≤ I_O ≤ 1.5A Case 79-05 5.0 mA ≤ I_O ≤ 0.5A	Reg_{load}		50 20	100 50		50 20	100 50	mV
Output Voltage Range 7.0 V ≤ V_{in} ≤ 25 V 5.0 mA ≤ I_O ≤ I_{max}, P ≤ P_{max}	V_O	4.6	–	5.4	4.75	–	5.25	Vdc
Quiescent Current (7.0 V ≤ V_{in} ≤ 25 V)	I_B	–	5.2	10	–	5.2	10	mAdc
Quiescent Current Change (7.0 V ≤ V_{in} ≤ 25 V) 5.0 mA ≤ I_O ≤ I_{max}	ΔI_B	–	–	0.5 0.8	–	–	0.5 0.8	
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_N		40	–		40		μV
Long Term Stability	S	–	–	10	–	–	20	mV
Thermal Resistance, Junction to Case[3] Case 1-03 (TO-204AA) Case 79-05 (TO-205AD)	θJC	 – –	 3.0 15	 – –	 – –	 3.0 15	 – –	°C/W

NOTES:
1. Unless otherwise specified, these specifications apply for −55°C ≤ T_J ≤ +150°C (−25°C ≤ T_J ≤ +150°C for the LM209). For Case 79-05, V_{in} = 10 V, I_O = 0.1 A, I_{max} = 0.2 A and P_{max} = 2.0 W. For Case 1-03, V_{in} = 10 V, I_O = 0.5 A, I_{max} = 1.0 A and P_{max} = 20 W.
2. Unless otherwise specified, these specifications apply for 0°C ≤ T_J ≤ +125°C, V_{in} = 10 V. For Case 79-05, I_O = 0.1 A, I_{max} = 0.2 A and P_{max} = 2.0 W. For Case 1-03, I_O = 0.5 A, I_{max} = 1.0 A and P_{max} = 20 W.
3. Without a heat sink, the thermal resistance of the Case 79-05 package is about 150°C/W, while that of the Case 1-03 package is approximately 35°C/W. With a heat sink, the effective thermal resistance can only approach the values specified, depending on the efficiency of the heat sink.

TYPICAL CHARACTERISTICS

(V_{in} = 10 V, T_A = +25°C unless otherwise noted.)

FIGURE 1 – MAXIMUM AVERAGE POWER DISSIPATION (LM109K, LM209K)

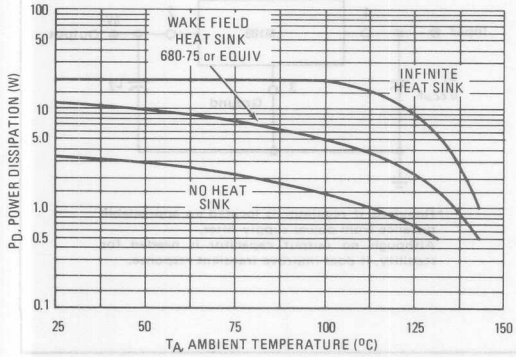
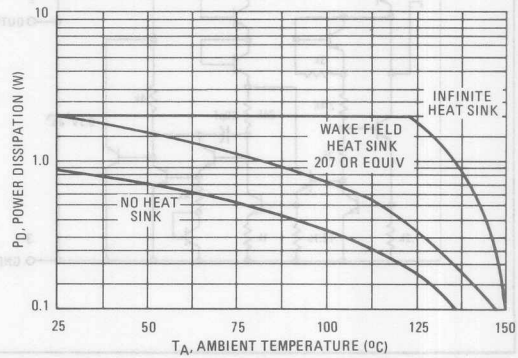


FIGURE 2 – MAXIMUM AVERAGE POWER DISSIPATION (LM109H, LM209H)



TYPICAL CHARACTERISTICS (continued)

(V_{in} = 10 V, T_A = +25°C unless otherwise noted.)

FIGURE 3 – MAXIMUM AVERAGE POWER DISSIPATION (LM309K)

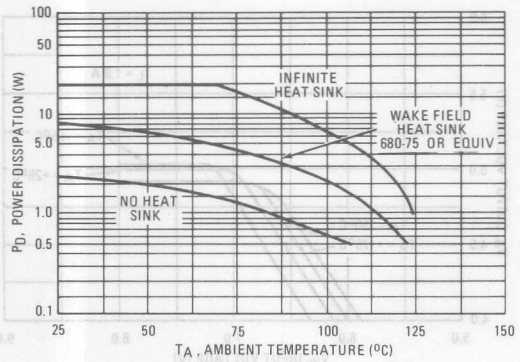


FIGURE 4 – MAXIMUM AVERAGE POWER DISSIPATION (LM309H)

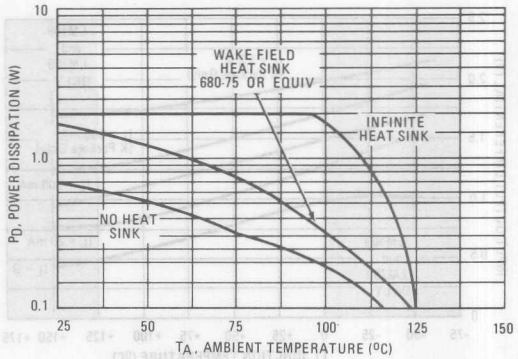


FIGURE 5 - OUTPUT IMPEDANCE versus FREQUENCY

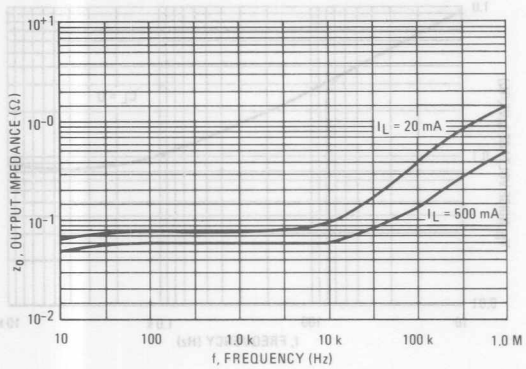


FIGURE 6 – PEAK OUTPUT CURRENT (K PACKAGE)

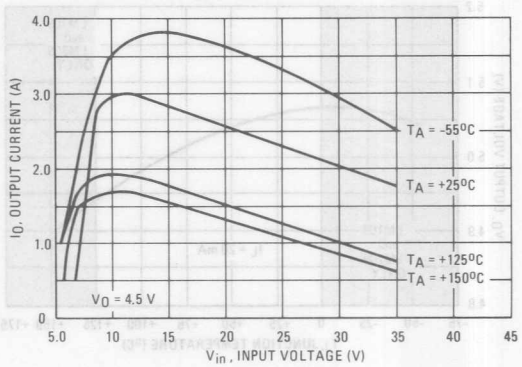


FIGURE 7 – PEAK OUTPUT CURRENT (H PACKAGE)

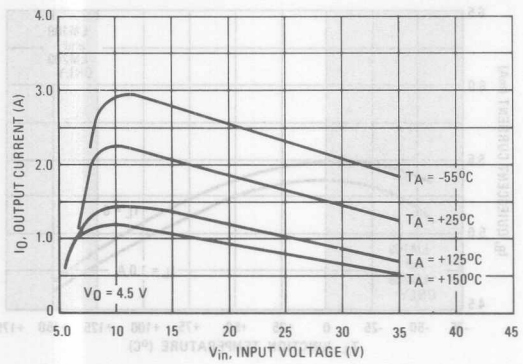
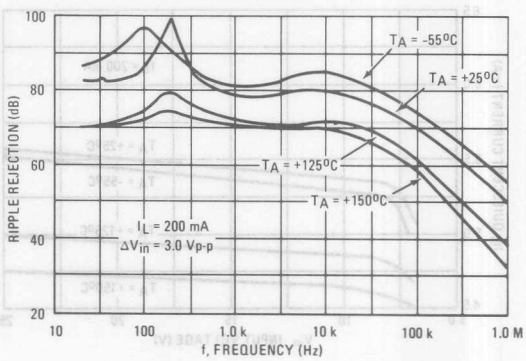


FIGURE 8 – RIPPLE REJECTION



3

TYPICAL CHARACTERISTICS (continued)

FIGURE 9 – DROPOUT VOLTAGE

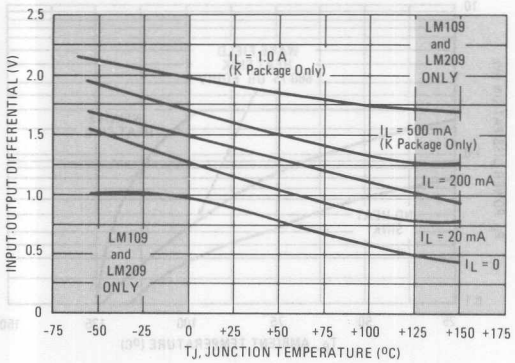


FIGURE 10 – DROPOUT CHARACTERISTIC (K PACKAGE)

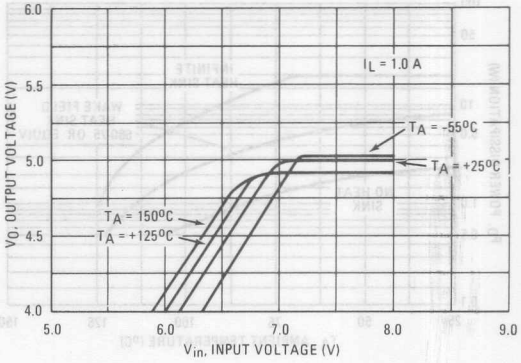


FIGURE 11 – OUTPUT VOLTAGE

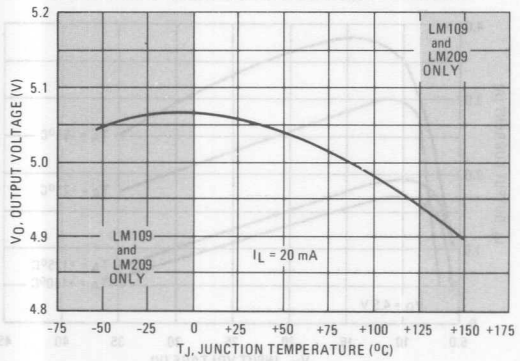


FIGURE 12 – OUTPUT NOISE VOLTAGE

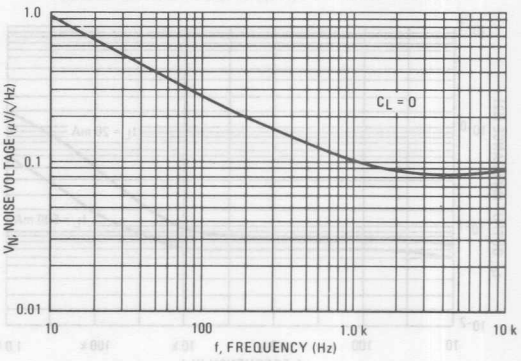


FIGURE 13 – QUIESCENT CURRENT

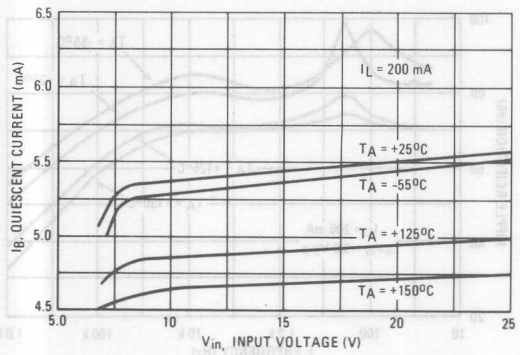
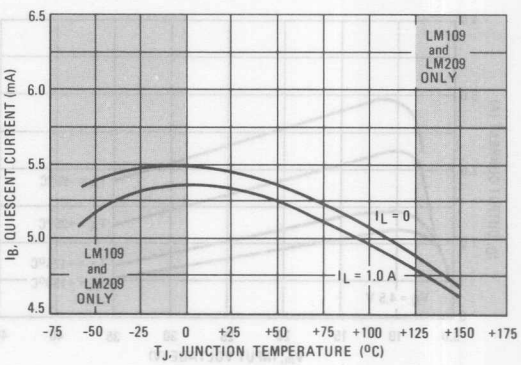


FIGURE 14 – QUIESCENT CURRENT



TYPICAL APPLICATIONS

FIGURE 15 – ADJUSTABLE OUTPUT REGULATOR

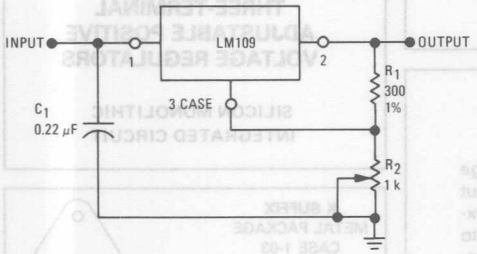
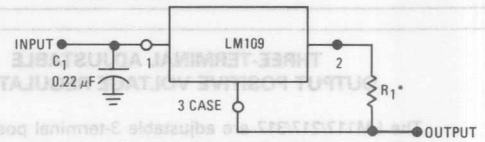


FIGURE 16 – CURRENT REGULATOR



*DETERMINES OUTPUT CURRENT.

FIGURE 17 – 5.0-VOLT, 3.0-AMPERE REGULATOR
(with plastic boost transistor)

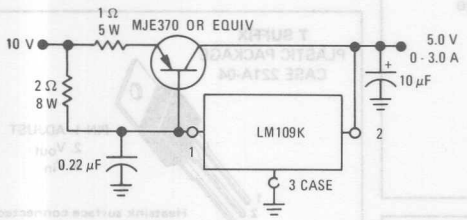


FIGURE 18 – 5.0 VOLT, 4.0-AMPERE TRANSISTOR
(with plastic Darlington boost transistor)

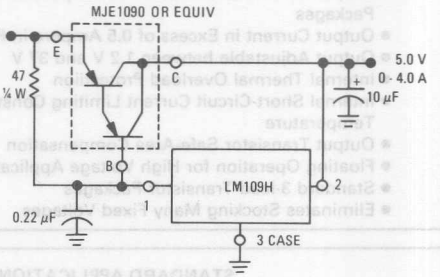


FIGURE 19 – 5.0-VOLT, 10-AMPERE REGULATOR

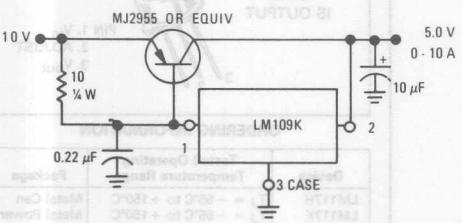
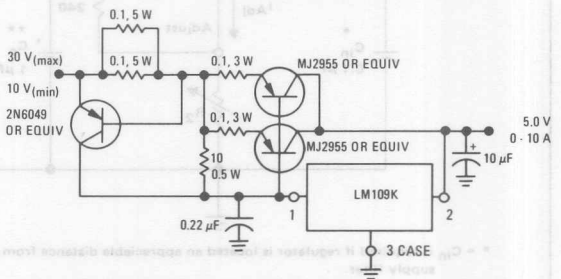


FIGURE 20 – 5.0-VOLT, 10-AMPERE REGULATOR
(with Short-Circuit Current Limiting for
Safe-Area Protection of pass transistors)



3

Specifications and Applications Information

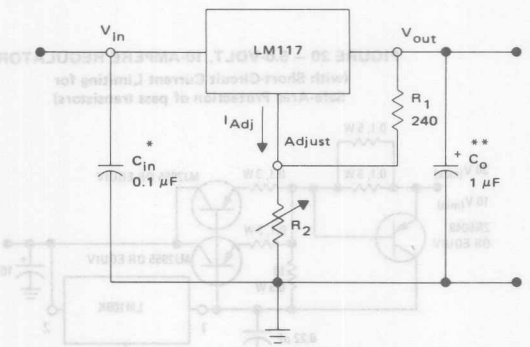
THREE-TERMINAL ADJUSTABLE OUTPUT POSITIVE VOLTAGE REGULATORS

The LM117/217/317 are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 1.5 A over an output voltage range of 1.2 V to 37 V. These voltage regulators are exceptionally easy to use and require only two external resistors to set the output voltage. Further, they employ internal current limiting, thermal shutdown and safe area compensation, making them essentially blow-out proof.

The LM117 series serve a wide variety of applications including local, on card regulation. This device can also be used to make a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM117 series can be used as a precision current regulator.

- Output Current in Excess of 1.5 Ampere in K and T Suffix Packages
- Output Current in Excess of 0.5 Ampere in H Suffix Package
- Output Adjustable between 1.2 V and 37 V
- Internal Thermal Overload Protectiion
- Internal Short-Circuit Current Limiting Constant with Temperature
- Output Transistor Safe-Area Compensation
- Floating Operation for High Voltage Applications
- Standard 3-lead Transistor Packages
- Eliminates Stocking Many Fixed Voltages

STANDARD APPLICATION



* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_o is not needed for stability, however it does improve transient response.

$$V_{out} = 1.25\ V\ (1 + \frac{R_2}{R_1}) + I_{Adj}\ R_2$$

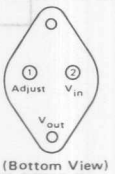
Since I_{Adj} is controlled to less than 100 μA, the error associated with this term is negligible in most applications

THREE-TERMINAL ADJUSTABLE POSITIVE VOLTAGE REGULATORS

SILICON MONOLITHIC INTEGRATED CIRCUIT

K SUFFIX
METAL PACKAGE
CASE 1-03



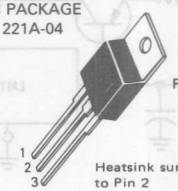


(Bottom View)

CASE IS OUTPUT

Pins 1 and 2 electrically isolated from case. Case is third electrical connection.

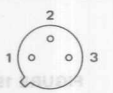
T SUFFIX
PLASTIC PACKAGE
CASE 221A-04



PIN 1. ADJUST
2. V_{out}
3. V_{in}

Heatsink surface connected to Pin 2

H SUFFIX
METAL PACKAGE
CASE 79-05



(Bottom View)

CASE IS OUTPUT



PIN 1. V_{in}
2. ADJUST
3. V_{out}

ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
LM117H	T_J = −55°C to +150°C	Metal Can
LM117K	T_J = −55°C to +150°C	Metal Power
LM217H	T_J = −25°C to +150°C	Metal Can
LM217K	T_J = −25°C to +150°C	Metal Power
LM317H	T_J = 0°C to +125°C	Metal Can
LM317K	T_J = 0°C to +125°C	Metal Power
LM317T	T_J = 0°C to +125°C	Plastic Power
LM317BT#	T_J = −40°C to +125°C	Plastic Power

#Automotive temperature range selections are available with special test conditions and additional tests. Contact your local Motorola sales office for information.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input-Output Voltage Differential	V_I-V_O	40	Vdc
Power Dissipation	P_D	Internally Limited	
Operating Junction Temperature Range LM117 LM217 LM317	T_J	 −55 to +150 −25 to +150 0 to +150	°C
Storage Temperature Range	T_{stg}	−65 to +125	°C

ELECTRICAL CHARACTERISTICS (V_I-V_O = 5.0 V; I_O = 0.5 A for K and T packages; I_O = 0.1 A for H package; T_J = T_{low} to T_{high} [see Note 1]; I_{max} and P_{max} per Note 2; unless otherwise specified.)

Characteristic	Figure	Symbol	LM117/217 Min	LM117/217 Typ	LM117/217 Max	LM317 Min	LM317 Typ	LM317 Max	Unit
Line Regulation (Note 3) T_A = 25°C, 3.0 V ≤ V_I-V_O ≤ 40 V	1	Reg_{line}	—	0.01	0.02	—	0.01	0.04	%/V
Load Regulation (Note 3) T_A = 25°C, 10 mA ≤ I_O ≤ I_{max} V_O ≤ 5.0 V V_O ≥ 5.0 V	2	Reg_{load}	 — —	 5.0 0.1	 15 0.3	 — —	 5.0 0.1	 25 0.5	 mV % V_O
Thermal Regulation (T_A = +25°C) 20 ms Pulse		—	—	0.02	0.07	—	0.03	0.07	%/W
Adjustment Pin Current	3	I_{Adj}	—	50	100	—	50	100	μA
Adjustment Pin Current Change 2.5 V ≤ V_I-V_O ≤ 40 V 10 mA ≤ I_L ≤ I_{max}, P_D ≤ P_{max}	1,2	ΔI_{Adj}	—	0.2	5.0	—	0.2	5.0	μA
Reference Voltage (Note 4) 3.0 V ≤ V_I-V_O ≤ 40 V 10 mA ≤ I_O ≤ I_{max}, P_D ≤ P_{max}	3	V_{ref}	1.20	1.25	1.30	1.20	1.25	1.30	V
Line Regulation (Note 3) 3.0 V ≤ V_I-V_O ≤ 40 V	1	Reg_{line}	—	0.02	0.05	—	0.02	0.07	%/V
Load Regulation (Note 3) 10 mA ≤ I_O ≤ I_{max} V_O ≤ 5.0 V V_O ≥ 5.0 V	2	Reg_{load}	 — —	 20 0.3	 50 1.0	 — —	 20 0.3	 70 1.5	 mV % V_O
Temperature Stability (T_{low} ≤ T_J ≤ T_{high})	3	T_S	—	0.7	—	—	0.7	—	% V_O
Minimum Load Current to Maintain Regulation (V_I-V_O = 40 V)	3	I_{Lmin}	—	3.5	5.0	—	3.5	10	mA
Maximum Output Current V_I-V_O ≤ 15 V, P_D ≤ P_{max} K and T Packages H Package V_I-V_O = 40 V, P_D ≤ P_{max}, T_A = 25°C K and T Packages H Package	3	I_{max}	 1.5 0.5 0.25 —	 2.2 0.8 0.4 0.07	 — — — —	 1.5 0.5 0.15 —	 2.2 0.8 0.4 0.07	 — — — —	A
RMS Noise, % of V_O T_A = 25°C, 10 Hz ≤ f ≤ 10 kHz	—	N	—	0.003	—	—	0.003	—	% V_O
Ripple Rejection, V_O = 10 V, f = 120 Hz (Note 5) Without C_{Adj} C_{Adj} = 10 μF	4	RR	 — 66	 65 80	 — —	 — 66	 65 80	 — —	dB
Long-Term Stability, T_J = T_{high} (Note 6) T_A = 25°C for Endpoint Measurements	3	S	—	0.3	1.0	—	0.3	1.0	%/1.0 k Hrs.
Thermal Resistance Junction to Case H Package K Package T Package	—	$R_{\theta JC}$	 — — —	 12 2.3 —	 15 3.0 —	 — — —	 12 2.3 5.0	 15 3.0 —	°C/W

NOTES: (1) T_{low} = −55°C for LM117 T_{high} = +150°C for LM117
= −25°C for LM217 = +150°C for LM217
= 0°C for LM317 = +125°C for LM317

(2) I_{max} = 1.5 A for K and T Packages
= 0.5 A for H Package
P_{max} = 20 W for K Package
= 20 W for T Package
= 2.0 W for H Package

(3) Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

(4) Selected devices with tightened tolerance reference voltage available.

(5) C_{ADJ}, when used, is connected between the adjustment pin and ground.

(6) Since Long-Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

3

SCHEMATIC DIAGRAM

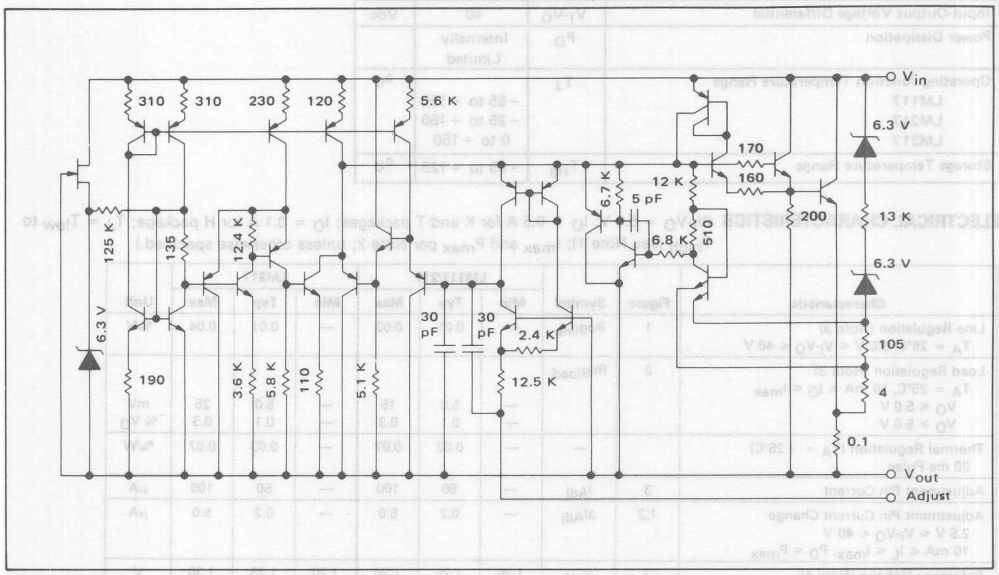


FIGURE 1 – LINE REGULATION AND ΔI_{Adj}/LINE TEST CIRCUIT

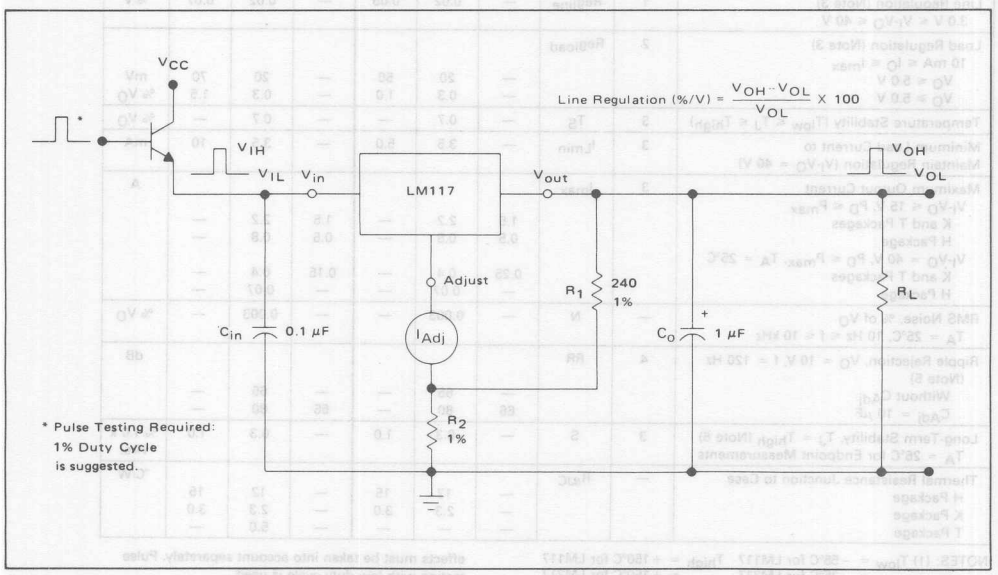


FIGURE 2 – LOAD REGULATION AND ΔI_{Adj}/LOAD TEST CIRCUIT

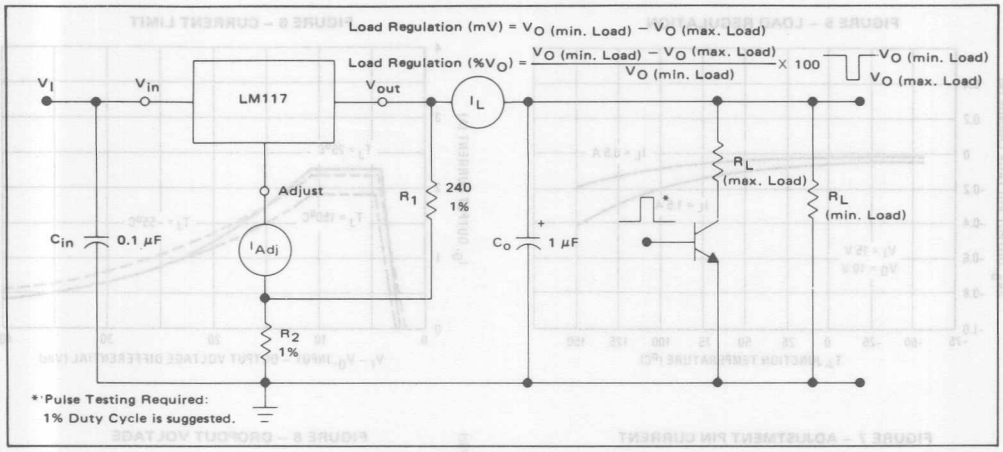


FIGURE 3 – STANDARD TEST CIRCUIT

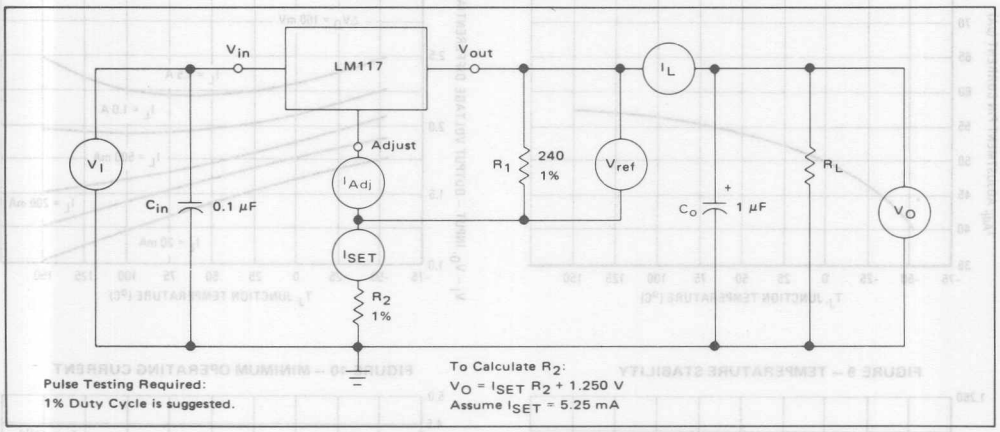
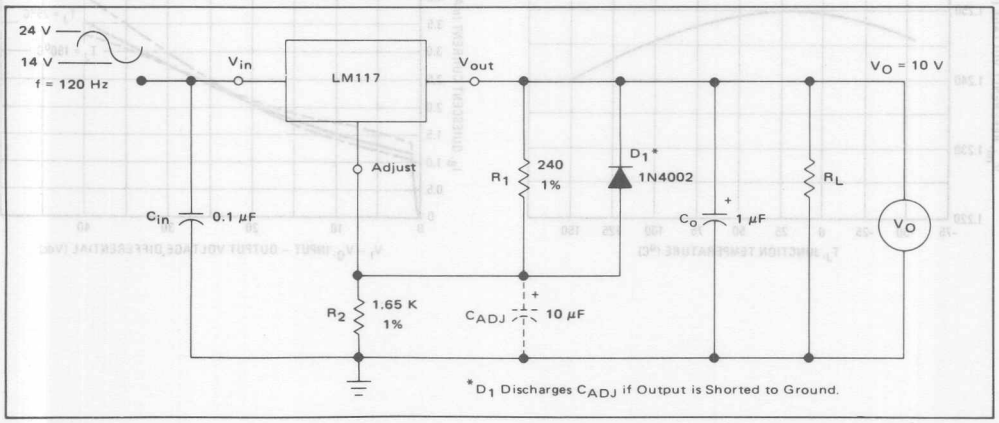


FIGURE 4 – RIPPLE REJECTION TEST CIRCUIT



3

FIGURE 5 – LOAD REGULATION

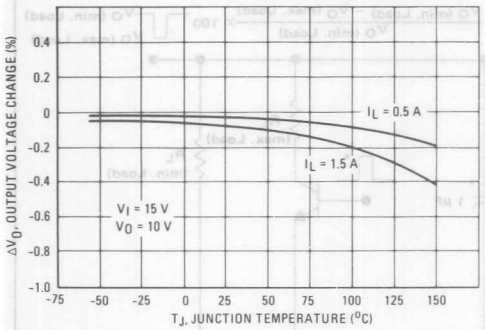


FIGURE 6 – CURRENT LIMIT

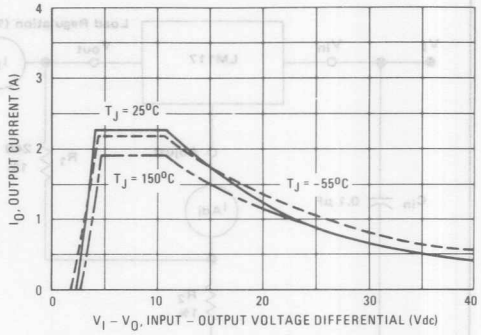


FIGURE 7 – ADJUSTMENT PIN CURRENT

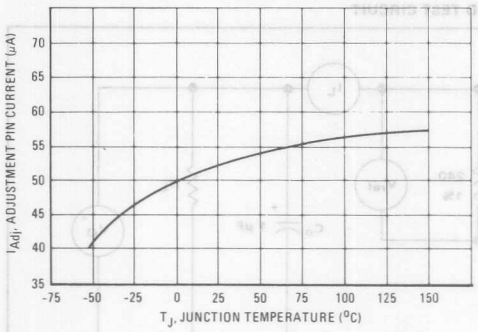


FIGURE 8 – DROPOUT VOLTAGE

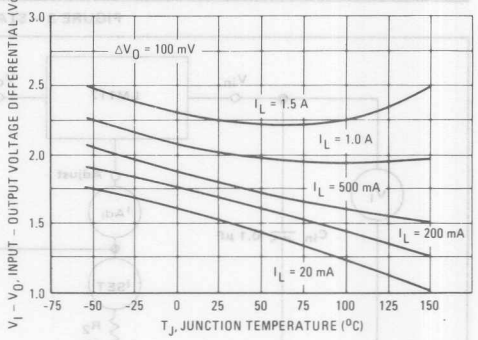


FIGURE 9 – TEMPERATURE STABILITY

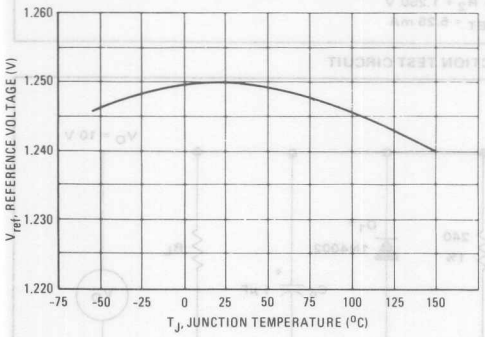


FIGURE 10 – MINIMUM OPERATING CURRENT

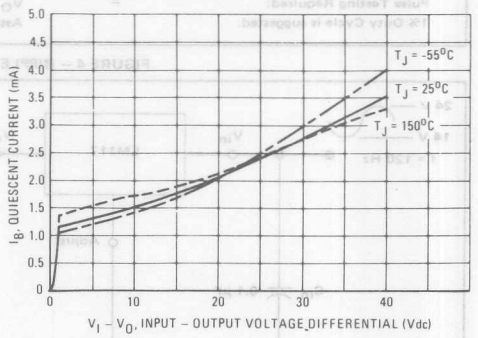


FIGURE 11 — RIPPLE REJECTION versus OUTPUT VOLTAGE

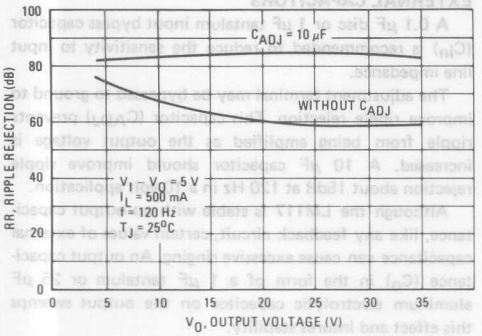


FIGURE 12 — RIPPLE REJECTION versus OUTPUT CURRENT

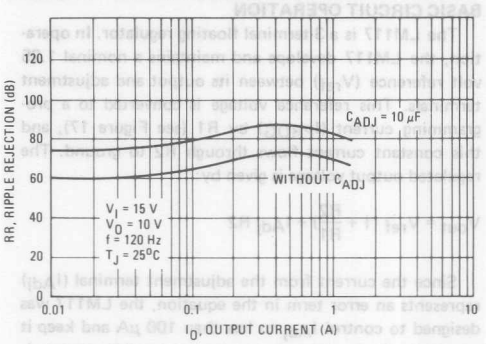


FIGURE 13 — RIPPLE REJECTION versus FREQUENCY

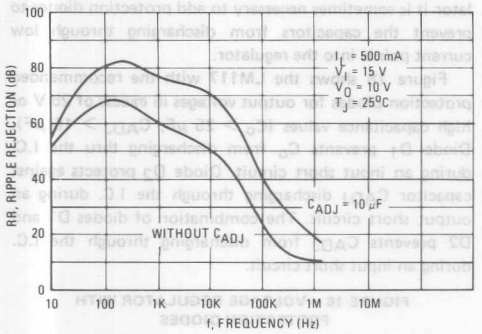


FIGURE 14 – OUTPUT IMPEDANCE

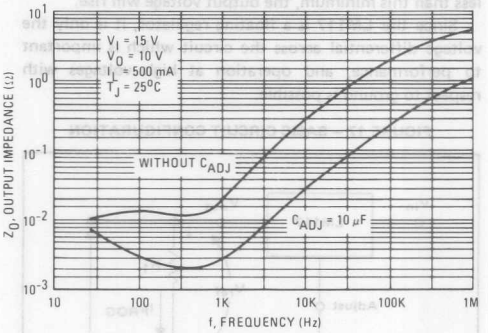


FIGURE 15 – LINE TRANSIENT RESPONSE

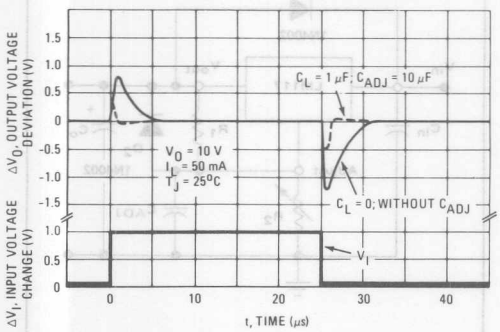
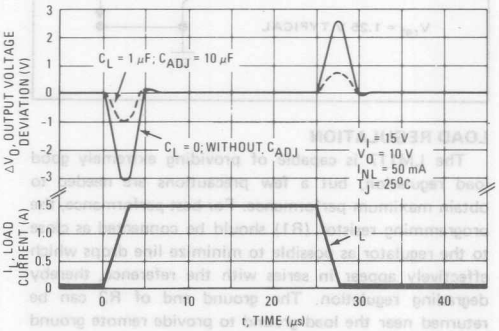


FIGURE 16 – LOAD TRANSIENT RESPONSE



3

APPLICATIONS INFORMATION

BASIC CIRCUIT OPERATION

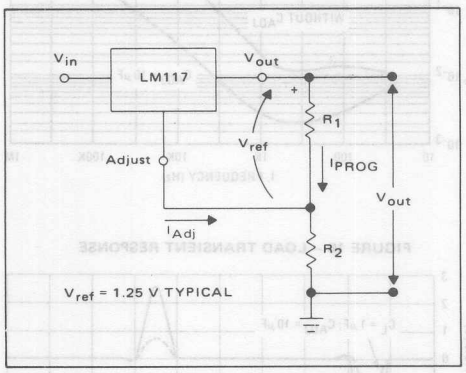
The LM117 is a 3-terminal floating regulator. In operation, the LM117 develops and maintains a nominal 1.25 volt reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by R1 (see Figure 17), and this constant current flows through R2 to ground. The regulated output voltage is given by:

$$V_{out} = V_{ref}\,(1 + \frac{R2}{R1}) + I_{Adj}\,R2$$

Since the current from the adjustment terminal (I_{Adj}) represents an error term in the equation, the LM117 was designed to control I_{Adj} to less than 100 μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM117 is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.

FIGURE 17 – BASIC CIRCUIT CONFIGURATION



LOAD REGULATION

The LM117 is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

EXTERNAL CAPACITORS

A 0.1 μF disc or 1 μF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{ADJ}) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15dB at 120 Hz in a 10 volt application.

Although the LM117 is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance (C_o) in the form of a 1 μF tantalum or 25 μF aluminum electrolytic capacitor on the output swamps this effect and insures stability.

PROTECTION DIODES

When external capacitors are used with any I.C. regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 18 shows the LM117 with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values ($C_o > 25\ \mu F$, $C_{ADJ} > 10\ \mu F$). Diode D_1 prevents C_o from discharging thru the I.C. during an input short circuit. Diode D_2 protects against capacitor C_{ADJ} discharging through the I.C. during an output short circuit. The combination of diodes D1 and D2 prevents C_{ADJ} from discharging through the I.C. during an input short circuit.

FIGURE 18 – VOLTAGE REGULATOR WITH PROTECTION DIODES

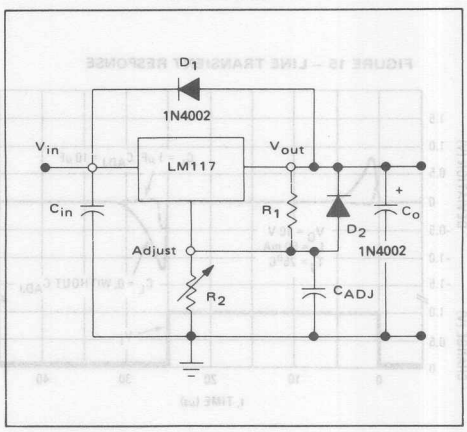


FIGURE 19 – "LABORATORY" POWER SUPPLY WITH ADJUSTABLE CURRENT LIMIT AND OUTPUT VOLTAGE

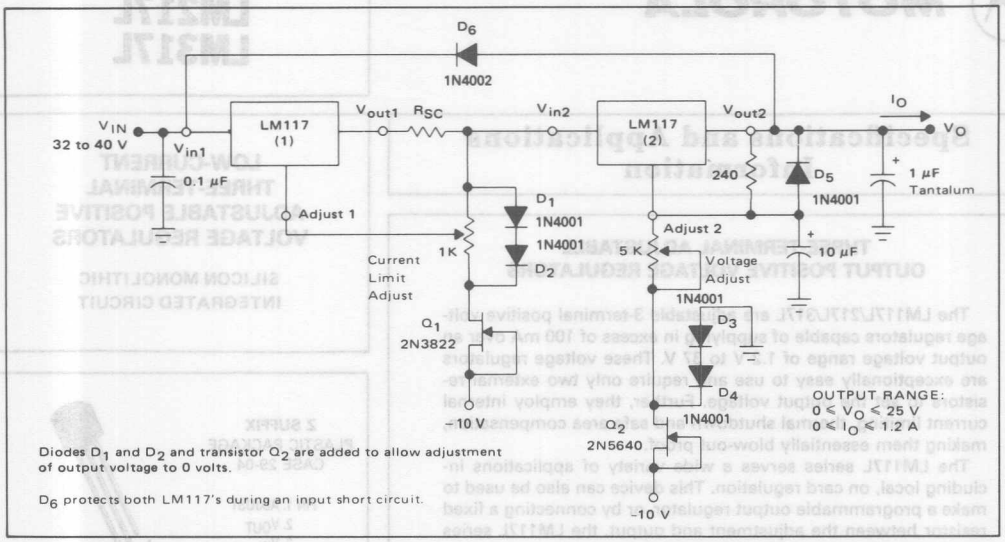


FIGURE 20 – ADJUSTABLE CURRENT LIMITER

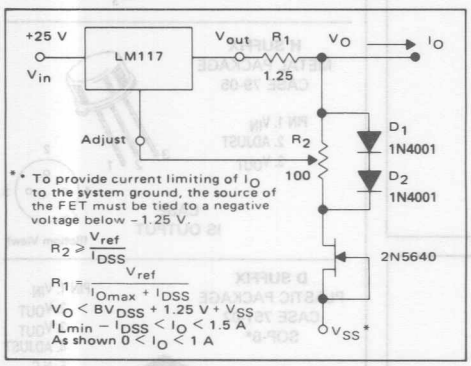


FIGURE 21 – 5 V ELECTRONIC SHUT DOWN REGULATOR

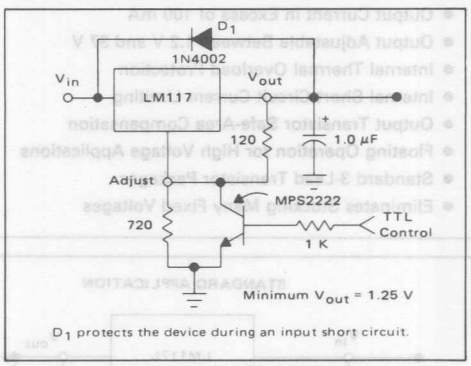


FIGURE 22 – SLOW TURN-ON REGULATOR

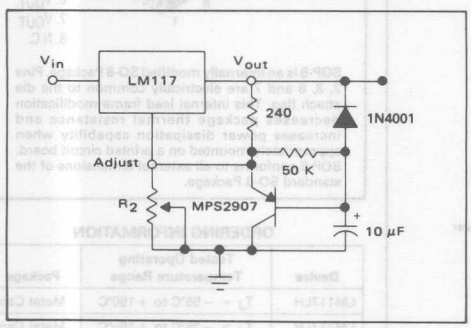
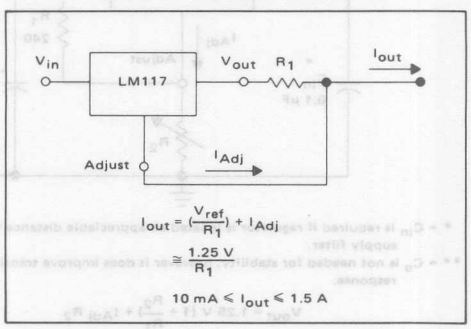


FIGURE 23 – CURRENT REGULATOR



Specifications and Applications Information

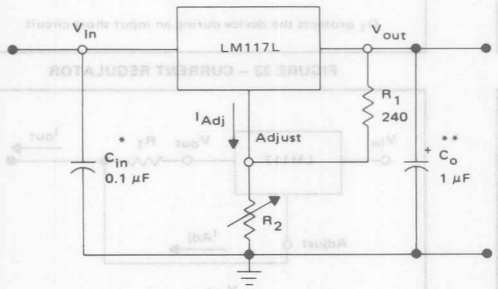
THREE-TERMINAL ADJUSTABLE OUTPUT POSITIVE VOLTAGE REGULATORS

The LM117L/217L/317L are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 100 mA over an output voltage range of 1.2 V to 37 V. These voltage regulators are exceptionally easy to use and require only two external resistors to set the output voltage. Further, they employ internal current limiting, thermal shutdown and safe area compensation, making them essentially blow-out proof.

The LM117L series serves a wide variety of applications including local, on card regulation. This device can also be used to make a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM117L series can be used as a precision current regulator.

- Output Current in Excess of 100 mA
- Output Adjustable Between 1.2 V and 37 V
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Floating Operation for High Voltage Applications
- Standard 3-Lead Transistor Packages
- Eliminates Stocking Many Fixed Voltages

STANDARD APPLICATION



* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_o is not needed for stability, however it does improve transient response.

$$V_{out} = 1.25\ V\ (1 + \frac{R_2}{R_1}) + I_{Adj}\ R_2$$

Since I_{Adj} is controlled to less than 100 μA, the error associated with this term is negligible in most applications

#Automotive temperature range selections are available with special test conditions and additional tests. Contact your local Motorola sales office for information.

LOW-CURRENT THREE-TERMINAL ADJUSTABLE POSITIVE VOLTAGE REGULATORS

SILICON MONOLITHIC INTEGRATED CIRCUIT

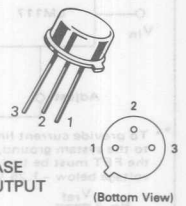
Z SUFFIX
PLASTIC PACKAGE
CASE 29-04

PIN 1. ADJUST
2. V_{OUT}
3. V_{IN}



H SUFFIX
METAL PACKAGE
CASE 79-05

PIN 1. V_{IN}
2. ADJUST
3. V_{OUT}



CASE IS OUTPUT

(Bottom View)

D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SOP-8*

PIN 1. V_{IN}
2. V_{OUT}
3. V_{OUT}
4. ADJUST
5. N.C.
6. V_{OUT}
7. V_{OUT}
8. N.C.



SOP-8 is an internally modified SO-8 Package. Pins 2, 3, 6 and 7 are electrically common to the die attach flag. This internal lead frame modification decreases package thermal resistance and increases power dissipation capability when appropriately mounted on a printed circuit board. SOP-8 conforms to all external dimensions of the standard SO-8 Package.

ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
LM117LH	T_J = −55°C to +150°C	Metal Can
LM217LH	T_J = −25°C to +150°C	Metal Can
LM317LD	T_J = 0°C to +125°C	SOP-8
LM317LH		Metal Can
LM317LZ		Plastic
LM317LBZ#	T_J = −40°C to +125°C	Plastic

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Input-Output Voltage Differential		V_I-V_O	40	Vdc
Power Dissipation		P_D	Internally Limited	
Operating Junction Temperature Range	LM117L	T_J	−55 to +150	°C
	LM217L		−25 to +150	
	LM317L		0 to +125	
Storage Temperature Range		T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS

($V_I - V_O$ = 5.0 V; I_O = 40 mA; $T_J = T_{low}$ to T_{high} [see Note 1]; I_{max} and P_{max} per Note 2; unless otherwise specified.)

Characteristic	Figure	Symbol	LM117L/217L Min	LM117L/217L Typ	LM117L/217L Max	LM317L Min	LM317L Typ	LM317L Max	Unit
Line Regulation (Note 3) T_A = 25°C, 3.0 V ≤ $V_I - V_O$ ≤ 40 V	1	Reg_{line}	—	0.01	0.02	—	0.01	0.04	%/V
Load Regulation (Note 3), T_A = 25°C 5.0 mA ≤ I_O ≤ I_{max} — LM117L/217L 10 mA ≤ I_O ≤ I_{max} — LM317L	2	Reg_{load}							
V_O ≤ 5.0 V			—	5.0	15	—	5.0	25	mV
V_O ≥ 5.0 V			—	0.1	0.3	—	0.1	0.5	% V_O
Adjustment Pin Current	3	I_{Adj}	—	50	100	—	50	100	μA
Adjustment Pin Current Change 2.5 V ≤ $V_I - V_O$ ≤ 40 V, P_D ≤ P_{max} 5.0 mA ≤ I_O ≤ I_{max} — LM117L/217L 10 mA ≤ I_O ≤ I_{max} — LM317L	1,2	ΔI_{Adj}	—	0.2	5.0	—	0.2	5.0	μA
Reference Voltage (Note 4) 3.0 V ≤ $V_I - V_O$ ≤ 40 V, P_D ≤ P_{max} 5.0 mA ≤ I_O ≤ I_{max} — LM117L/217L 10 mA ≤ I_O ≤ I_{max} — LM317L	3	V_{ref}	1.20	1.25	1.30	1.20	1.25	1.30	V
Line Regulation (Note 3) 3.0 V ≤ $V_I - V_O$ ≤ 40 V	1	Reg_{line}	—	0.02	0.05	—	0.02	0.07	%/V
Load Regulation (Note 3) 5.0 mA ≤ I_O ≤ I_{max} — LM117L/217L 10 mA ≤ I_O ≤ I_{max} — LM317L	2	Reg_{load}							
V_O ≤ 5.0 V			—	20	50	—	20	70	mV
V_O ≥ 5.0 V			—	0.3	1.0	—	0.3	1.5	% V_O
Temperature Stability (T_{low} ≤ T_J ≤ T_{high})	3	T_S	—	0.7	—	—	0.7	—	% V_O
Minimum Load Current to Maintain Regulation ($V_I - V_O$ = 40 V)	3	I_{Lmin}	—	3.5	5.0	—	3.5	10	mA
Maximum Output Current	3	I_{max}							mA
$V_I - V_O$ ≤ 20 V, P_D ≤ P_{max}, H Package			100	200	—	100	200	—	
$V_I - V_O$ ≤ 6.25 V, P_D ≤ P_{max}, Z Package			100	200	—	100	200	—	
$V_I - V_O$ = 40 V, P_D ≤ P_{max}, T_A = 25°C									
H Package			—	50	—	—	50	—	
Z Package			—	20	—	—	20	—	
RMS Noise, % of V_O T_A = 25°C, 10 Hz ≤ f ≤ 10 kHz	—	N	—	0.003	—	—	0.003	—	% V_O
Ripple Rejection (Note 5)	4	RR							dB
V_O = 1.25 V, f = 120 Hz			66	80	—	60	80	—	
C_{ADJ} = 10 μF V_O = 10.0 V			—	80	—	—	80	—	
Long Term Stability, $T_J = T_{high}$ (Note 6) T_A = 25°C for Endpoint Measurements	3	S	—	0.3	1.0	—	0.3	1.0	%/1.0 k Hrs.
Thermal Resistance Junction to Case	—	$R_{\theta JC}$							°C/W
H Package			—	40	—	—	40	—	
Z Package			—	—	—	—	83	—	
Thermal Resistance Junction to Air	—	$R_{\theta JA}$							°C/W
H Package			—	185	—	—	185	—	
Z Package			—	—	—	—	160	—	

NOTES:

(1) T_{low} = −55°C for LM117L, −25°C for LM217L, 0°C for LM317L; T_{high} = +150°C for LM117L, +150°C for LM217L, +125°C for LM317L

(2) I_{max} = 100 mA
P_{max} = 2 W for H Package
= 625 mW for Z Package

(3) Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

(4) Selected devices with tightened tolerance reference voltage available.

(5) C_{ADJ}, when used, is connected between the adjustment pin and ground.

(6) Since Long Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

3

SCHEMATIC DIAGRAM

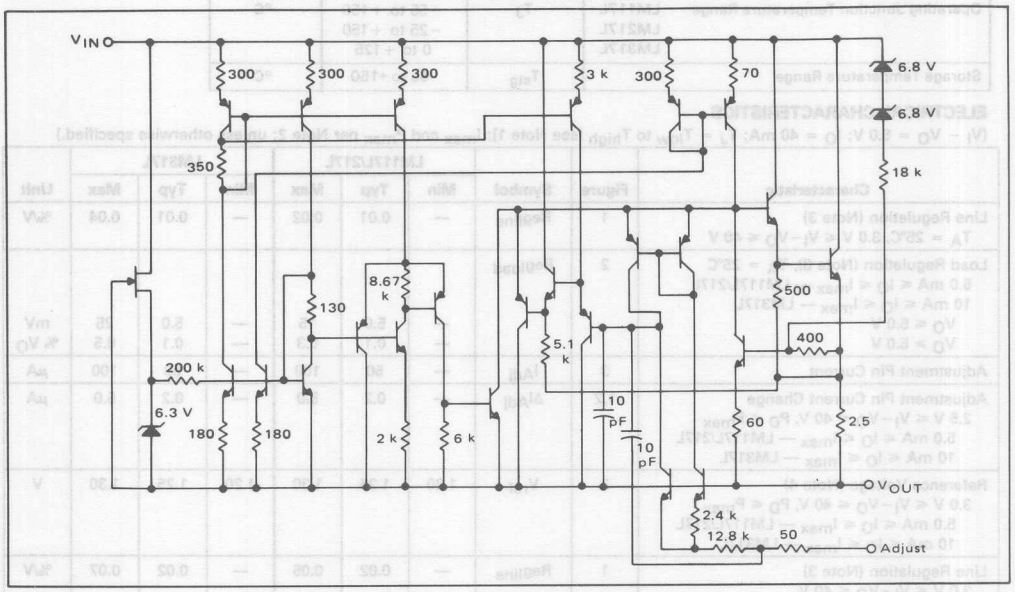


FIGURE 1 – LINE REGULATION AND ΔI_{Adj}/LINE TEST CIRCUIT

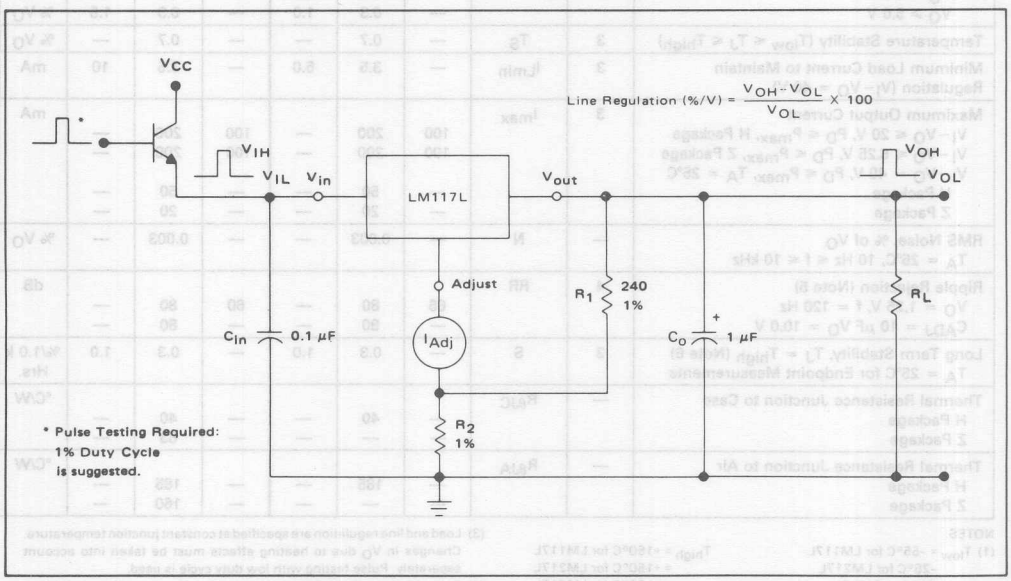


FIGURE 2 – LOAD REGULATION AND ΔI_{Adj}/LOAD TEST CIRCUIT

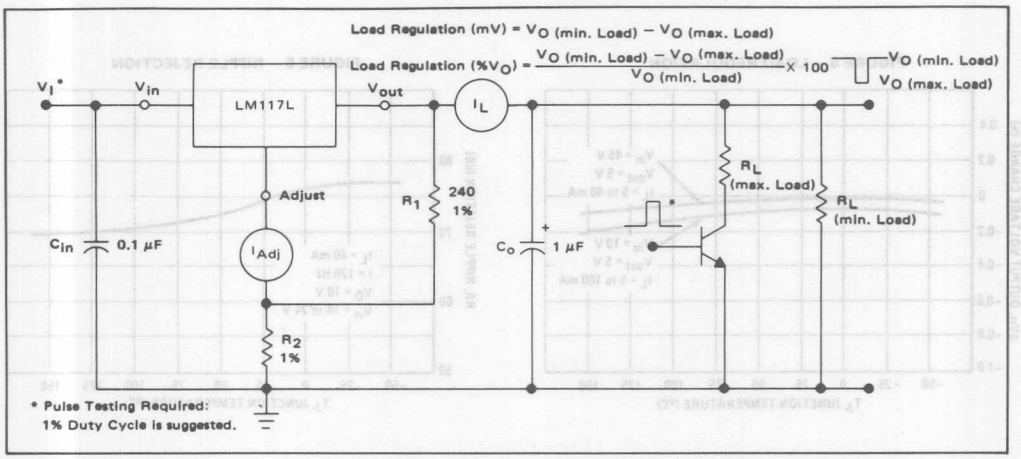


FIGURE 3 – STANDARD TEST CIRCUIT

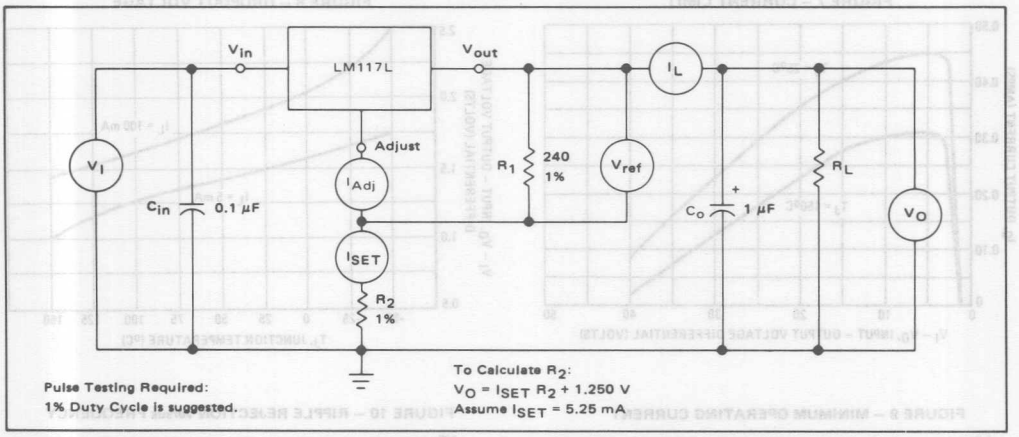


FIGURE 4 – RIPPLE REJECTION TEST CIRCUIT

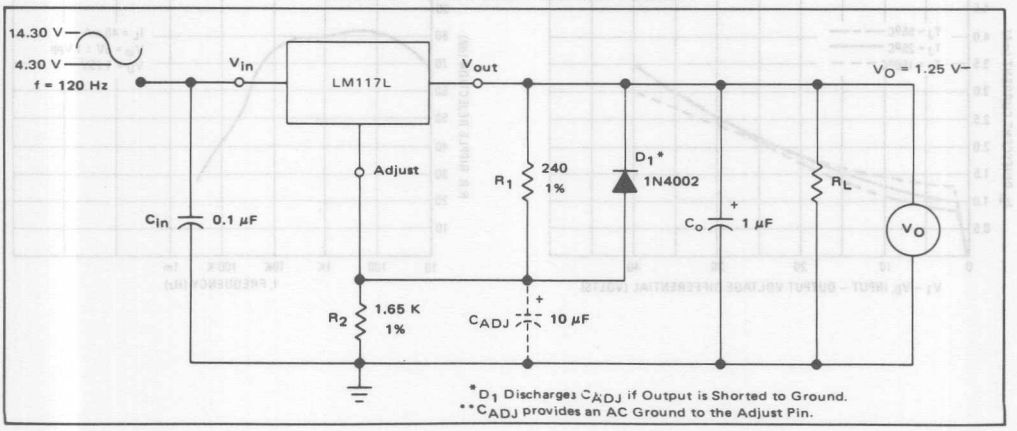


FIGURE 5 – LOAD REGULATION

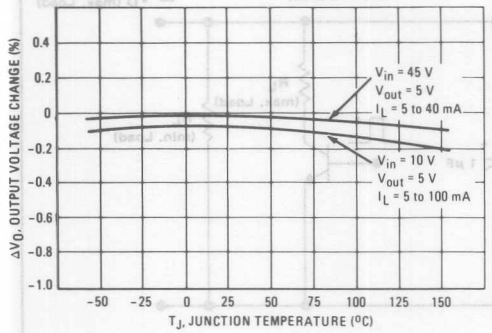


FIGURE 6 – RIPPLE REJECTION

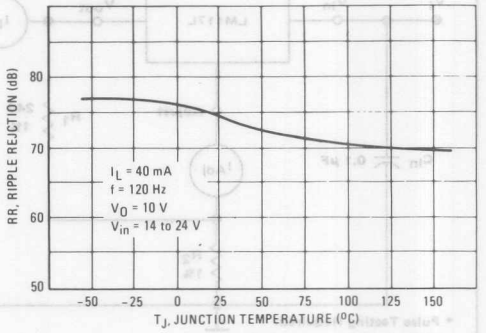


FIGURE 7 – CURRENT LIMIT

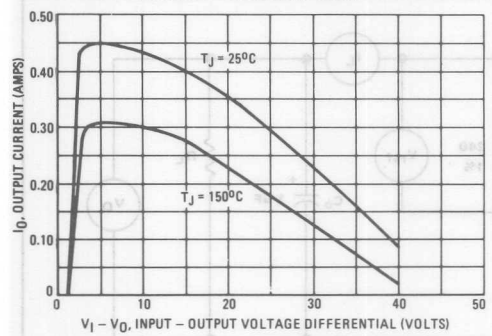


FIGURE 8 – DROPOUT VOLTAGE

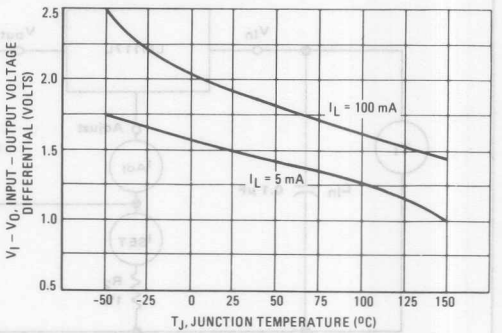


FIGURE 9 – MINIMUM OPERATING CURRENT

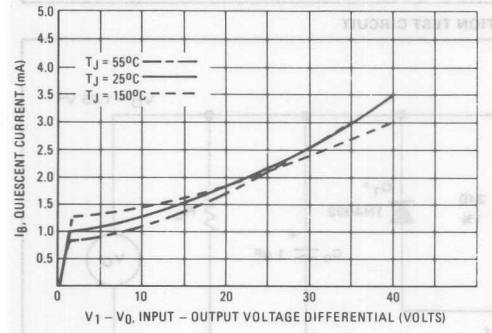


FIGURE 10 – RIPPLE REJECTION versus FREQUENCY

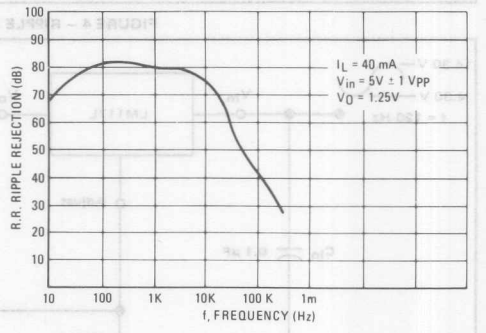


FIGURE 11 – TEMPERATURE STABILITY

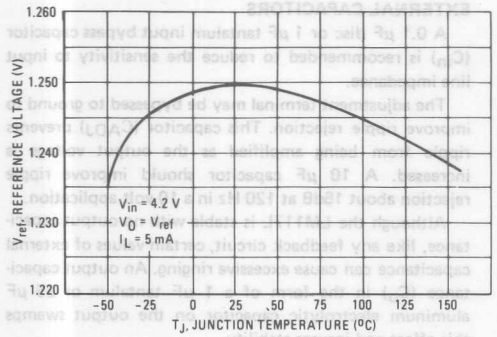


FIGURE 12 – ADJUSTMENT PIN CURRENT

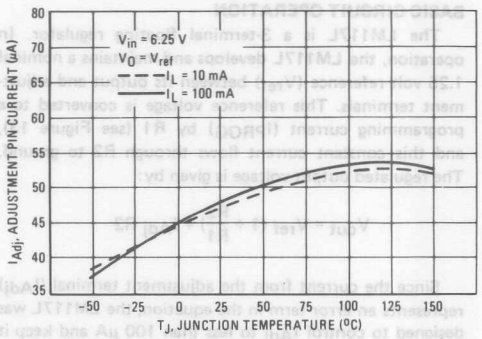


FIGURE 13 – LINE REGULATION

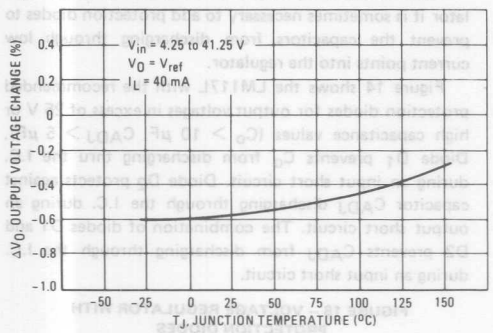


FIGURE 14 – OUTPUT NOISE

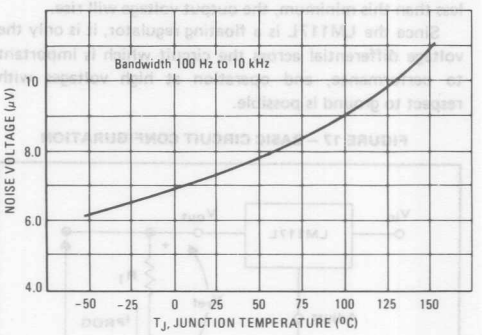


FIGURE 15 – LINE TRANSIENT RESPONSE

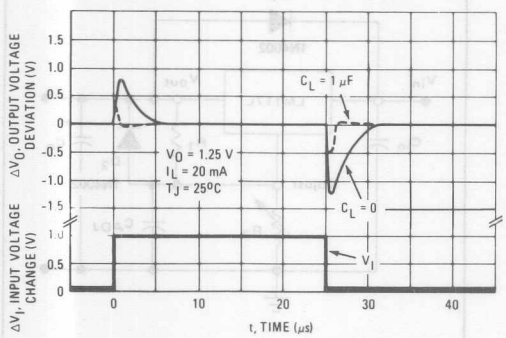
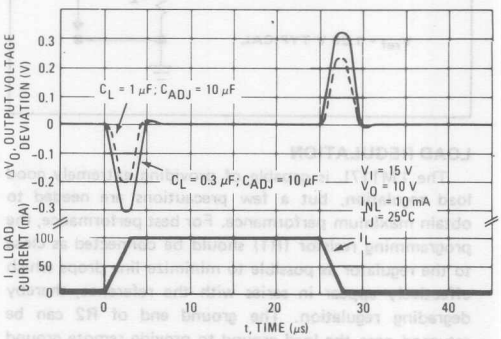


FIGURE 16 – LOAD TRANSIENT RESPONSE



3

APPLICATIONS INFORMATION

BASIC CIRCUIT OPERATION

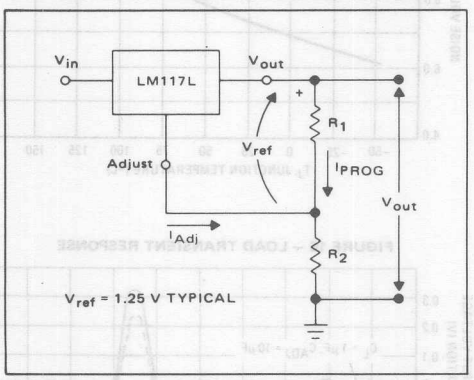
The LM117L is a 3-terminal floating regulator. In operation, the LM117L develops and maintains a nominal 1.25 volt reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by R1 (see Figure 13), and this constant current flows through R2 to ground. The regulated output voltage is given by:

$$V_{out} = V_{ref}\left(1 + \frac{R2}{R1}\right) + I_{Adj}\,R2$$

Since the current from the adjustment terminal (I_{Adj}) represents an error term in the equation, the LM117L was designed to control I_{Adj} to less than 100 μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM117L is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.

FIGURE 17 – BASIC CIRCUIT CONFIGURATION



LOAD REGULATION

The LM117L is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

EXTERNAL CAPACITORS

A 0.1 μF disc or 1 μF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{ADJ}) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15dB at 120 Hz in a 10 volt application.

Although the LM117L is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance (C_o) in the form of a 1 μF tantalum or 25 μF aluminum electrolytic capacitor on the output swamps this effect and insures stability.

PROTECTION DIODES

When external capacitors are used with any I.C. regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 14 shows the LM117L with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values ($C_o > 10$ μF, $C_{ADJ} > 5$ μF). Diode D_1 prevents C_o from discharging thru the I.C. during an input short circuit. Diode D_2 protects against capacitor C_{ADJ} discharging through the I.C. during an output short circuit. The combination of diodes D1 and D2 prevents C_{ADJ} from discharging through the I.C. during an input short circuit.

FIGURE 18 – VOLTAGE REGULATOR WITH PROTECTION DIODES

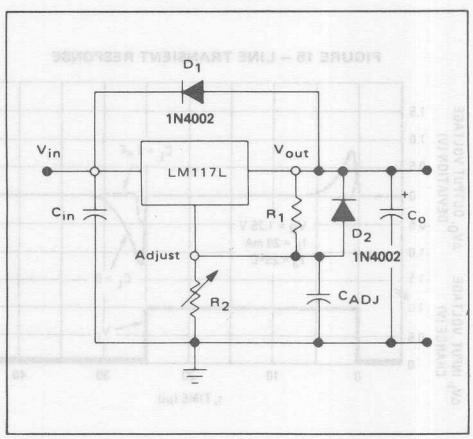


FIGURE 19 – ADJUSTABLE CURRENT LIMITER

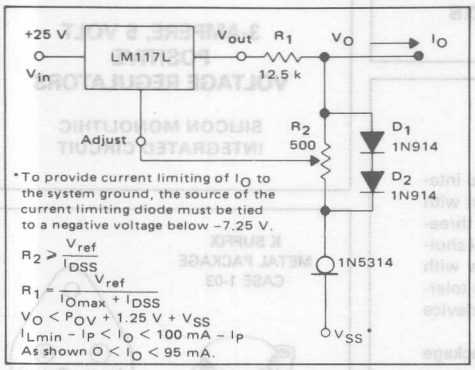


FIGURE 20 – 5 V ELECTRONIC SHUTDOWN REGULATOR

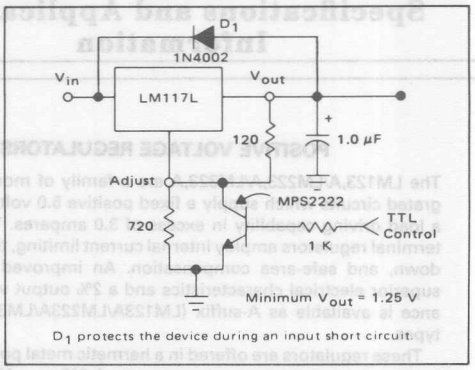


FIGURE 21 – SLOW TURN-ON REGULATOR

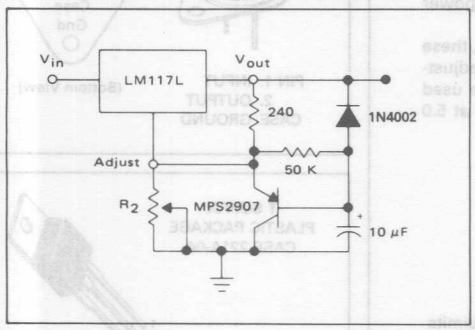
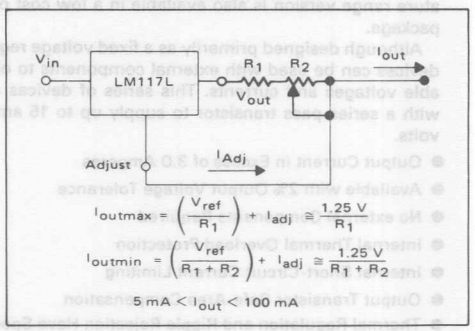


FIGURE 22 – CURRENT REGULATOR



LM223, LM223A
LM323, LM323A

3

Specifications and Applications Information

3-AMPERE, 5 VOLT POSITIVE VOLTAGE REGULATORS

SILICON MONOLITHIC INTEGRATED CIRCUIT

POSITIVE VOLTAGE REGULATORS

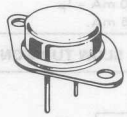
The LM123,A/LM223,A/LM323,A are a family of monolithic integrated circuits which supply a fixed positive 5.0 volt output with a load driving capability in excess of 3.0 amperes. These three-terminal regulators employ internal current limiting, thermal shutdown, and safe-area compensation. An improved series with superior electrical characteristics and a 2% output voltage tolerance is available as A-suffix (LM123A/LM223A/LM323A) device types.

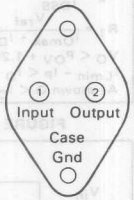
These regulators are offered in a hermetic metal power package in three operating temperature ranges. A 0°C to +125°C temperature range version is also available in a low cost plastic power package.

Although designed primarily as a fixed voltage regulator, these devices can be used with external components to obtain adjustable voltages and currents. This series of devices can be used with a series pass transistor to supply up to 15 amperes at 5.0 volts.

- Output Current in Excess of 3.0 Amperes
- Available with 2% Output Voltage Tolerance
- No external Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Thermal Regulation and Ripple Rejection Have Specified Limits

K SUFFIX
METAL PACKAGE
CASE 1-03

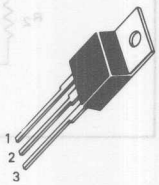




PIN 1. INPUT
2. OUTPUT
CASE GROUND

(Bottom View)

T SUFFIX
PLASTIC PACKAGE
CASE 221A-04



PIN 1. INPUT
2. GROUND
3. OUTPUT

(Heatsink surface connected to Pin 2)

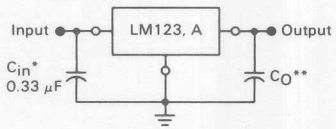
MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Input Voltage		V_{in}	20	Vdc
Power Dissipation		P_D	Internally Limited	
Operating Junction Temperature Range	LM123, A	T_J	−55 to +150	°C
	LM223, A		−25 to +150	
	LM323, A		0 to +150	
Storage Temperature Range		T_{stg}	−65 to +125	°C
Lead Temperature (Soldering, 10 s)		T_{solder}	300	°C

ORDERING INFORMATION

Device	Output Voltage Tolerance	Tested Operating Junction Temp. Range	Package
LM123K	6%	-55 to +150°C	Metal Power
LM123AK	2%		
LM223K	6%	-25 to +150°C	
LM223AK	2%		
LM323K	4%	0 to +125°C	
LM323AK	2%		
LM323T	4%		Plastic Power
LM323AT	2%		

STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.5 V above the output voltage even during the low point on the input ripple voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter. (See Applications Information for details.)

** = C_O is not needed for stability; however, it does improve transient response.

ELECTRICAL CHARACTERISTICS ($T_J = T_{low}$ to T_{high} [see Note 1] unless otherwise specified.)

Characteristic	Symbol	LM123A/LM223A/LM323A			LM123/LM223			LM323			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage (V_{in} = 7.5 V, 0 ≤ I_{out} ≤ 3.0 A, T_J = 25°C)	V_O	4.9	5.0	5.1	4.7	5.0	5.3	4.8	5.0	5.2	V
Output Voltage (7.5 V ≤ V_{in} ≤ 15 V, 0 ≤ I_{out} ≤ 3.0 A, P ≤ P_{max} [Note 2])	V_O	4.8	5.0	5.2	4.6	5.0	5.4	4.75	5.0	5.25	V
Line Regulation (7.5 V ≤ V_{in} ≤ 15 V, T_J = 25°C) (Note 3)	Reg_{line}	—	1.0	15	—	1.0	25	—	1.0	25	mV
Load Regulation (V_{in} = 7.5 V, 0 ≤ I_{out} ≤ 3.0 A, T_J = 25°C) (Note 3)	Reg_{load}	—	10	50	—	10	100	—	10	100	mV
Thermal Regulation (Pulse = 10 ms, P = 20 W, T_A = 25°C)	Reg_{therm}	—	0.001	0.01	—	0.002	0.03	—	0.002	0.03	%V_O/W
Quiescent Current (7.5 V ≤ V_{in} ≤ 15 V, 0 ≤ I_{out} ≤ 3.0 A)	I_B	—	3.5	10	—	3.5	20	—	3.5	20	mA
Output Noise Voltage (10 Hz ≤ f ≤ 100 kHz, T_J = 25°C)	V_N	—	40	—	—	40	—	—	40	—	μV_{rms}
Ripple Rejection (8.0 V ≤ V_{in} ≤ 18 V, I_{out} = 2.0 A, f = 120 Hz, T_J = 25°C)	RR	62	75	—	62	75	—	62	75	—	dB
Short Circuit Current Limit (V_{in} = 15 V, T_J = 25°C)	I_{SC}	—	4.5	—	—	4.5	—	—	4.5	—	A
(V_{in} = 7.5 V, T_J = 25°C)		—	5.5	—	—	5.5	—	—	5.5	—	
Long Term Stability	S	—	—	35	—	—	35	—	—	35	mV
Thermal Resistance Junction to Case (Note 4)	$R_{\theta JC}$	—	2.0	—	—	2.0	—	—	2.0	—	°C/W

Note 1. T_{low} = −55°C for LM123, A; = −25°C for LM223, A; = 0°C for LM323, A
T_{high} = +150°C for LM123, A; = +150°C for LM223, A; = +125°C for LM323, A

Note 2. Although power dissipation is internally limited, specifications apply only for P ≤ P_{max}
P_{max} = 30 W for K package
P_{max} = 25 W for T package

Note 3. Load and line regulation are specified at constant junction temperature. Pulse testing is required with a pulse width ≤ 1.0 ms and a duty cycle ≤ 5%.

Note 4. Without a heat sink, the thermal resistance ($R_{\theta JA}$ is 35°C/W for the K package, and 65°C/W for the T package. With a heat sink, the effective thermal resistance can approach the specified values of 2.0°C/W, depending on the efficiency of the heat sink.

VOLTAGE REGULATOR PERFORMANCE

The performance of a voltage regulator is specified by its immunity to changes in load, input voltage, power dissipation, and temperature. Line and load regulation are tested with a pulse of short duration (< 100 μs) and are strictly a function of electrical gain. However, pulse widths of longer duration (> 1.0 ms) are sufficient to affect temperature gradients across the die. These temperature gradients can cause a change in the output voltage, in addition to changes caused by line and load regulation. Longer pulse widths and thermal gradients make it desirable to specify thermal regulation.

Thermal regulation is defined as the change in output voltage caused by a change in dissipated power for a specified time, and is expressed as a percentage output voltage change per watt. The change in dissipated power can be caused by a change in either the input voltage or the load current. Thermal regulation is a function of I.C. layout and die attach techniques, and usually occurs within 10 ms of a change in power dissipation. After 10 ms, additional changes in the output voltage are due to the temperature coefficient of the device.

Figure 1 shows the line and thermal regulation response of a typical LM123A to a 20 watt input pulse. The variation of the output voltage due to line regulation is labeled (1) and the thermal regulation component is labeled (2). Figure 2 shows the load and thermal regulation response of a typical LM123A to a 20 watt load pulse. The output voltage variation due to load regulation is labeled (1) and the thermal regulation component is labeled (2).

3

SCHEMATIC DIAGRAM

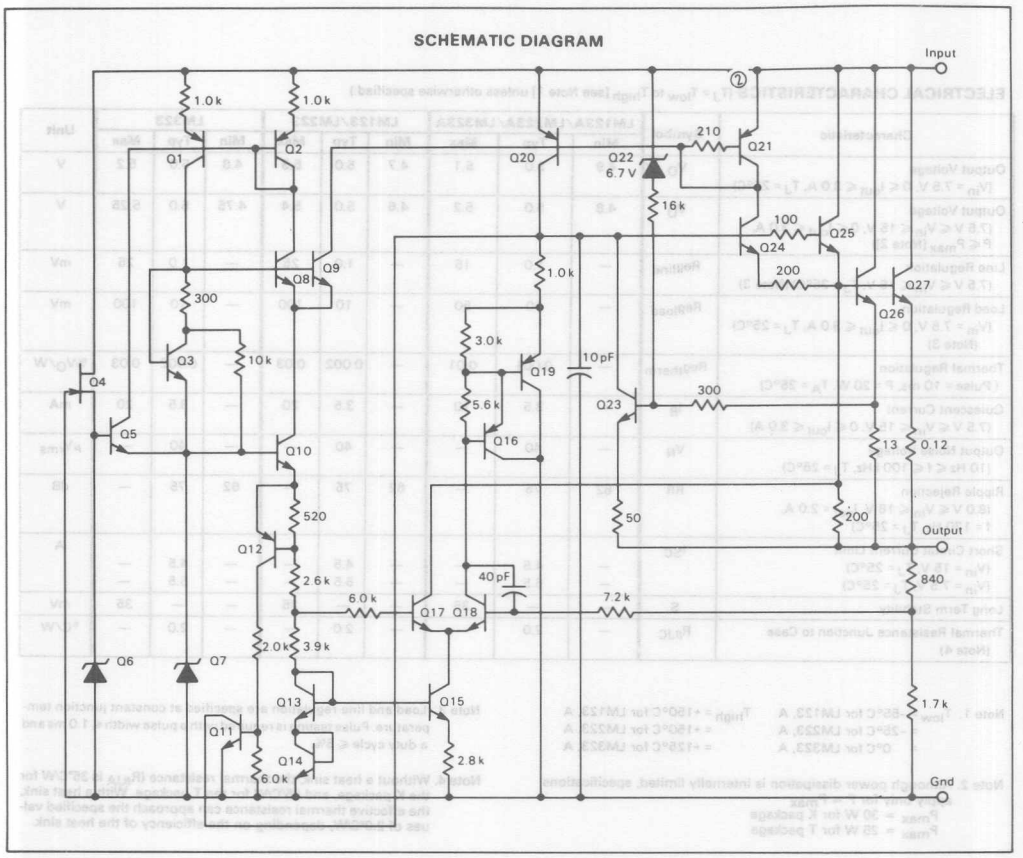
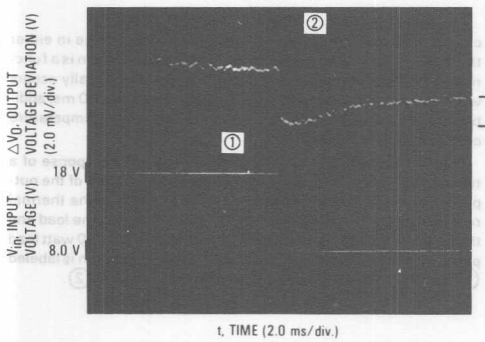
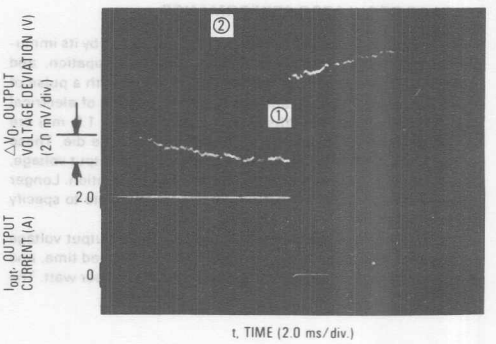


FIGURE 1 — LINE AND THERMAL REGULATION



LM123A
V_O = 5.0 V
V_{in} = 8.0 V → 18 V → 8.0 V ① = Reg_{line} = 2.4 mV
I_{out} = 2.0 A ② = Reg_{therm} = 0.0015%V_O/W

FIGURE 2 — LOAD AND THERMAL REGULATION



LM123A
V_O = 5.0 V
V_{in} = 15 ① = Reg_{load} = 4.4 mV
I_{out} = 0 A → 2.0 A → 0 A ② = Reg_{therm} = 0.0015%V_O/W

FIGURE 3 — TEMPERATURE STABILITY

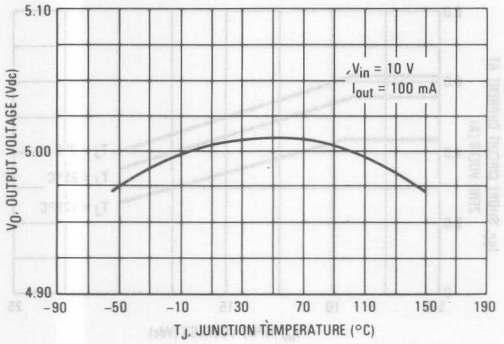


FIGURE 4 — OUTPUT IMPEDANCE

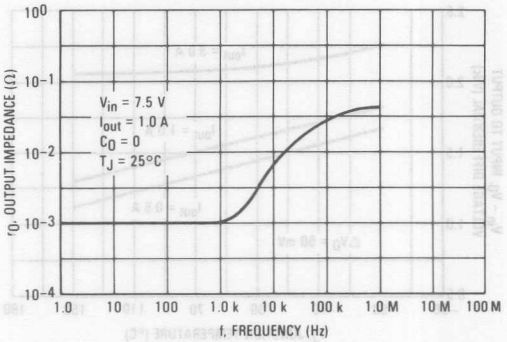


FIGURE 5 — RIPPLE REJECTION versus FREQUENCY

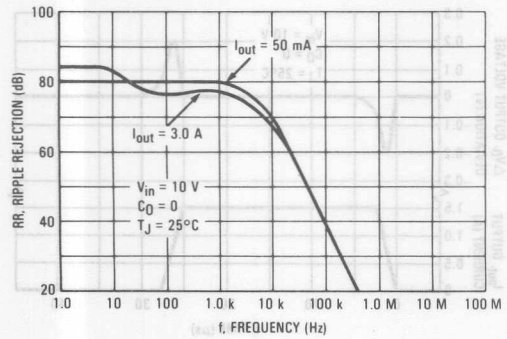


FIGURE 6 — RIPPLE REJECTION versus OUTPUT CURRENT

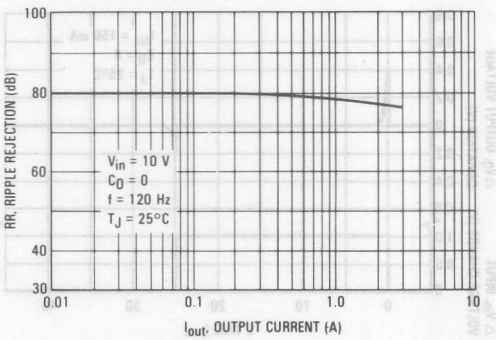


FIGURE 7 — QUIESCENT CURRENT versus INPUT VOLTAGE

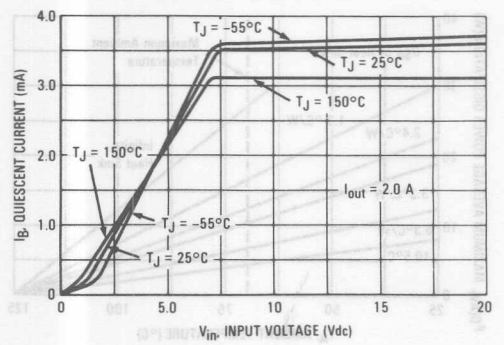


FIGURE 8 — QUIESCENT CURRENT versus OUTPUT CURRENT

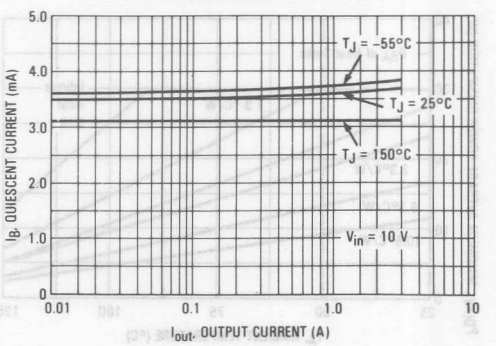


FIGURE 9 — DROPOUT VOLTAGE

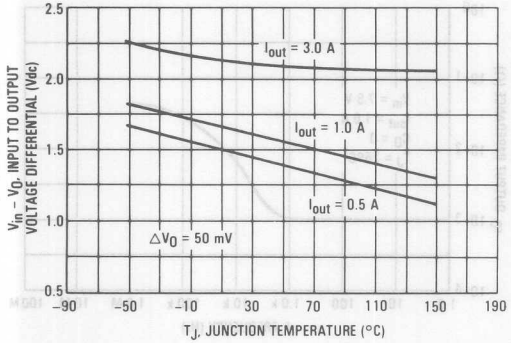


FIGURE 10 — SHORT CIRCUIT CURRENT

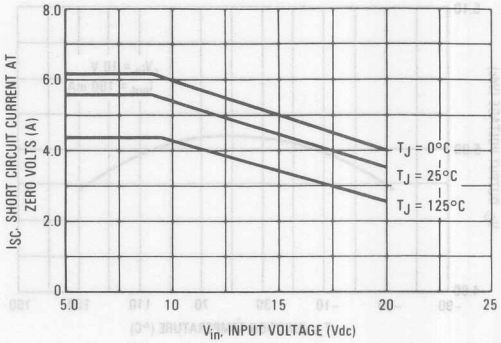


FIGURE 11 — LINE TRANSIENT RESPONSE

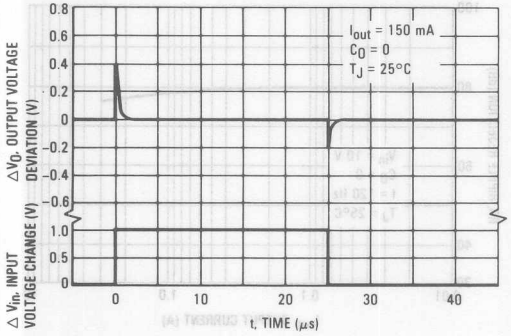


FIGURE 12 — LOAD TRANSIENT RESPONSE

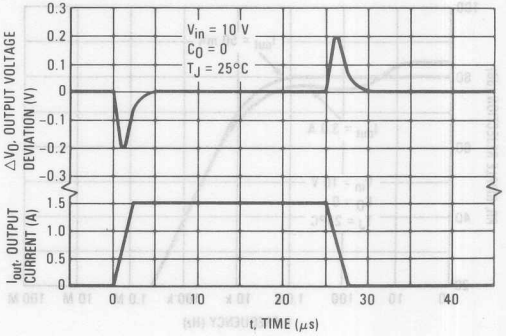


FIGURE 13 — MAXIMUM AVERAGE POWER DISSIPATION FOR LM123K and LM223K

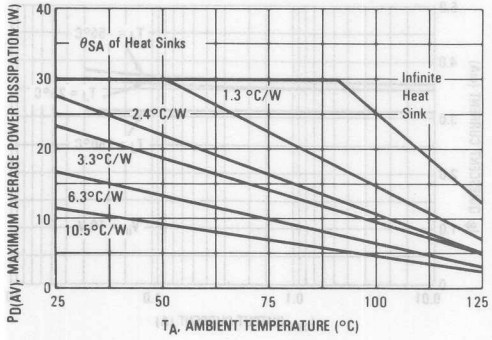
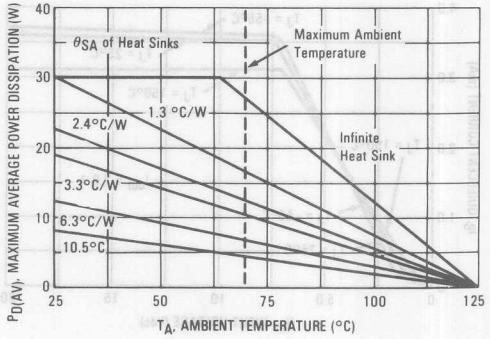


FIGURE 14 — MAXIMUM AVERAGE POWER DISSIPATION FOR LM323K



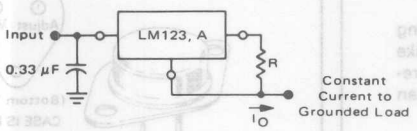
APPLICATIONS INFORMATION

Design Considerations

The LM123,A Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulator's input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

FIGURE 15 — CURRENT REGULATOR



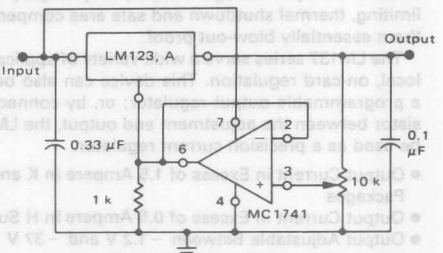
The LM123,A regulator can also be used as a current source when connected as above. Resistor R determines the current as follows:

$$I_O = \frac{5.0\ V}{R} + I_B$$

$\Delta I_B \cong 0.7$ mA over line, load and temperature changes
$I_B \cong 3.5$ mA

For example, a 2-ampere current source would require R to be a 2.5 ohm, 15 W resistor and the output voltage compliance would be the input voltage less 7.5 volts.

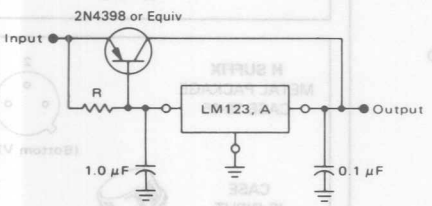
FIGURE 16 — ADJUSTABLE OUTPUT REGULATOR



V_O, 8.0 V to 20 V
$V_{in} - V_O \geq 2.5$ V

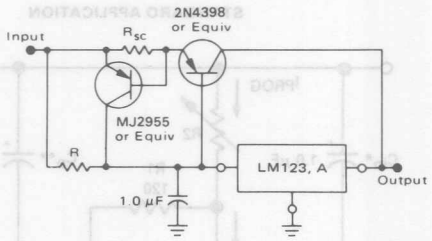
The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 3.0 volts greater than the regulator voltage.

FIGURE 17 — CURRENT BOOST REGULATOR



The LM123,A series can be current boosted with a PNP transistor. The 2N4398 provides current to 15 amperes. Resistor R in conjunction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short-circuit proof. Input-output differential voltage minimum is increased by the V_{BE} of the pass transistor.

FIGURE 18 — CURRENT BOOST WITH SHORT-CIRCUIT PROTECTION



The circuit of Figure 17 can be modified to provide supply protection against short circuits by adding a short-circuit sense resistor, R_{SC}, and an additional PNP transistor. The current sensing PNP must be able to handle the short-circuit current of the three-terminal regulator. Therefore, an eight-ampere power transistor is specified.

MOTOROLA

LM137
LM237
LM337

3

Specifications and Applications Information

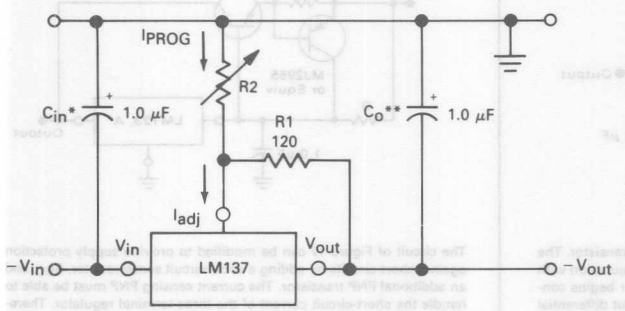
THREE-TERMINAL ADJUSTABLE OUTPUT NEGATIVE VOLTAGE REGULATORS

The LM137/237/337 are adjustable 3-terminal negative voltage regulators capable of supplying in excess of 1.5 A over an output voltage range of −1.2 V to −37 V. These voltage regulators are exceptionally easy to use and require only two external resistors to set the output voltage. Further, they employ internal current limiting, thermal shutdown and safe area compensation, making them essentially blow-out proof.

The LM137 series serve a wide variety of applications including local, on-card regulation. This device can also be used to make a programmable output regulator; or, by connecting a fixed resistor between the adjustment and output, the LM137 series can be used as a precision current regulator.

- Output Current in Excess of 1.5 Ampere in K and T Suffix Packages
- Output Current in Excess of 0.5 Ampere in H Suffix Package
- Output Adjustable Between −1.2 V and −37 V
- Internal Thermal Overload Protection
- Internal Short-Circuit-Current Limiting, Constant with Temperature
- Output Transistor Safe-Area Compensation
- Floating Operation for High Voltage Applications
- Standard 3-Lead Transistor Packages
- Eliminates Stocking Many Fixed Voltages

STANDARD APPLICATION



*C_{in} is required if regulator is located more than 4 inches from power supply filter. A 1 μF solid tantalum or 10 μF aluminum electrolytic is recommended.

**C_O is necessary for stability. A 1 μF solid tantalum or 10 μF aluminum electrolytic is recommended.

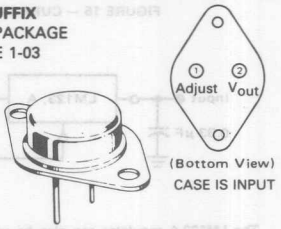
$$V_{out} = -1.25\ V\left(1 + \frac{R2}{R1}\right)$$

#Automotive temperature range selections are available with special test conditions and additional tests. Contact your local Motorola sales office for information.

THREE-TERMINAL ADJUSTABLE NEGATIVE VOLTAGE REGULATORS

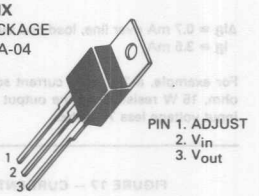
SILICON MONOLITHIC INTEGRATED CIRCUIT

K SUFFIX
METAL PACKAGE
CASE 1-03



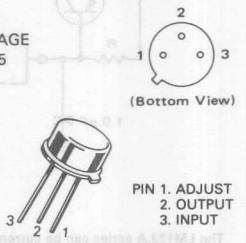
Pins 1 and 2 electrically isolated from case.
Case is third electrical connection.

T SUFFIX
PLASTIC PACKAGE
CASE 221A-04



Heatsink surface connected to Pin 2

H SUFFIX
METAL PACKAGE
CASE 79-05



ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
LM137H	T_J = −55°C to +150°C	Metal Can
LM137K	T_J = −55°C to +150°C	Metal Power
LM237H	T_J = −25°C to +150°C	Metal Can
LM237K	T_J = −25°C to +150°C	Metal Power
LM337H	T_J = 0°C to +125°C	Metal Can
LM337K	T_J = 0°C to +125°C	Metal Power
LM337T	T_J = 0°C to +125°C	Plastic Power
LM337BT#	T_J = −40°C to +125°C	Plastic Power

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Input-Output Voltage Differential		V_I-V_O	40	Vdc
Power Dissipation		P_D	Internally Limited	
Operating Junction Temperature Range	LM137 LM237 LM337	T_J	−55 to +150 −25 to +150 0 to +125	°C
Storage Temperature Range		T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS ($|V_I - V_O|$ = 5.0 V, I_O = 0.5 A for K and T packages; I_O = 0.1 A for H package; $T_J = T_{low}$ to T_{high} [see Note 1], I_{max} and P_{max} per Note 2, unless otherwise specified.)

Characteristic	Figure	Symbol	LM137/237 Min	LM137/237 Typ	LM137/237 Max	LM337 Min	LM337 Typ	LM337 Max	Unit
Line Regulation (Note 3) T_A = 25°C, 3.0 V ≤ $\|V_I$-$V_O\|$ ≤ 40 V	1	Reg_{line}	—	0.01	0.02	—	0.01	0.04	%/V
Load Regulation (Note 3) T_A = 25°C, 10 mA ≤ I_O ≤ I_{max} $\|V_O\|$ ≤ 5.0 V $\|V_O\|$ ≥ 5.0 V	2	Reg_{load}	 — —	 15 0.3	 25 0.5	 — —	 15 0.3	 50 1.0	 mV % V_O
Thermal Regulation 10 ms Pulse, T_A = 25°C	—	Reg_{therm}	—	0.002	0.02	—	0.003	0.04	% V_O/W
Adjustment Pin Current	3	I_{Adj}	—	65	100	—	65	100	μA
Adjustment Pin Current Change 2.5 V ≤ $\|V_I$-$V_O\|$ ≤ 40 V 10 mA ≤ I_L ≤ I_{max}, P_D ≤ P_{max}, T_A = 25°C	1,2	ΔI_{Adj}	—	2.0	5.0	—	2.0	5.0	μA
Reference Voltage (Note 4) T_A = +25°C 3.0 V ≤ $\|V_I$-$V_O\|$ ≤ 40 V, 10 mA ≤ I_O ≤ I_{max}, P_D ≤ P_{max}, $T_J = T_{low}$ to T_{high}	3	V_{ref}	−1.225 −1.20	−1.250 −1.25	−1.275 −1.30	−1.213 −1.20	−1.250 −1.25	−1.287 −1.30	V
Line Regulation (Note 3) 3.0 V ≤ $\|V_I$-$V_O\|$ ≤ 40 V	1	Reg_{line}	—	0.02	0.05	—	0.02	0.07	%/V
Load Regulation (Note 3) 10 mA ≤ I_O ≤ I_{max} $\|V_O\|$ ≤ 5.0 V $\|V_O\|$ ≥ 5.0 V	2	Reg_{load}	 — —	 20 0.3	 50 1.0	 — —	 20 0.3	 70 1.5	 mV % V_O
Temperature Stability (T_{low} ≤ T_J ≤ T_{high})	3	T_S	—	0.6	—	—	0.6	—	% V_O
Minimum Load Current to Maintain Regulation ($\|V_I$-$V_O\|$ ≤ 10 V) ($\|V_I$-$V_O\|$ ≤ 40 V)	3	I_{Lmin}	 — —	 1.2 2.5	 3.0 5.0	 — —	 1.5 2.5	 6.0 10	mA
Maximum Output Current $\|V_I$-$V_O\|$ ≤ 15 V, P_D ≤ P_{max} K and T Packages H Package $\|V_I$-$V_O\|$ = 40 V, P_D ≤ P_{max}, T_J = 25°C K and T Packages H Package	3	I_{max}	 1.5 0.5 0.24 0.15	 2.2 0.8 0.4 0.2	 — — — —	 1.5 0.5 0.15 0.1	 2.2 0.8 0.4 0.2	 — — — —	A
RMS Noise, % of V_O T_A = 25°C, 10 Hz ≤ f ≤ 10 kHz	—	N	—	0.003	—	—	0.003	—	% V_O
Ripple Rejection, V_O = −10 V, f = 120 Hz (Note 5) Without C_{Adj} C_{Adj} = 10 μF	4	RR	 — 66	 60 77	 — —	 — 66	 60 77	 — —	dB
Long-Term Stability, $T_J = T_{high}$ (Note 6) T_A = 25°C for Endpoint Measurements	3	S	—	0.3	1.0	—	0.3	1.0	%/1.0 k Hrs.
Thermal Resistance Junction to Case H Package K Package T Package	—	$R_{\theta JC}$	 — — —	 12 2.3 —	 15 3.0 —	 — — —	 12 2.3 4.0	 15 3.0 —	°C/W

NOTES:

(1) T_{low} = −55°C for LM137 = −25°C for LM237 = 0°C for LM337; T_{high} = +150°C for LM137 = +150°C for LM237 = +125°C for LM337

(2) I_{max} = 1.5 A for K and T Packages = 0.5 A for H Package
P_{max} = 20 W for K and T Packages = 2 W for H Package

(3) Load and line regulation are specified at a constant junction temperature. Pulse testing with a low duty cycle is used. Change in V_O because of heating effects is covered under the Thermal Regulation specification.

(4) Selected devices with tightened tolerance reference voltage available.

(5) C_{adj}, when used, is connected between the adjustment pin and ground.

(6) Since Long Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

(7) Power dissipation within an I.C. voltage regulator produces a temperature gradient on the die, affecting individual I.C. components on the die. These effects can be minimized by proper integrated circuit design and layout techniques. Thermal Regulation is the effect of these temperature gradients on the output voltage and is expressed in percentage of output change per watt of power change in a specified time.

SCHEMATIC DIAGRAM

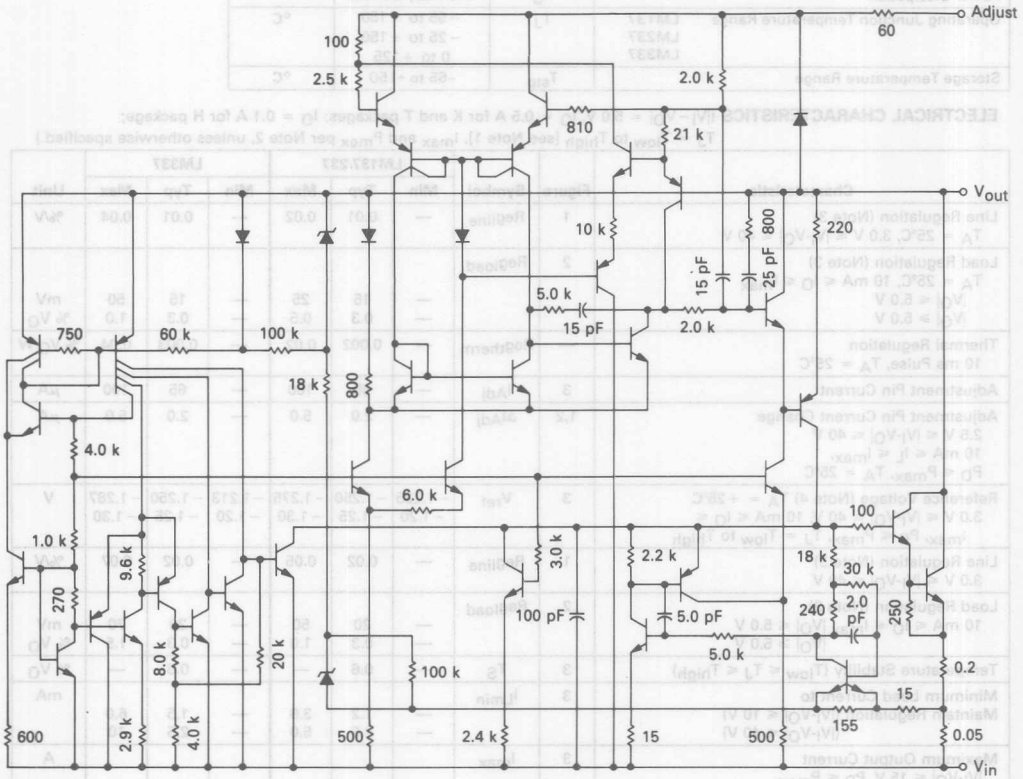


FIGURE 1 — LINE REGULATION AND ΔI_{Adj}/LINE TEST CIRCUIT

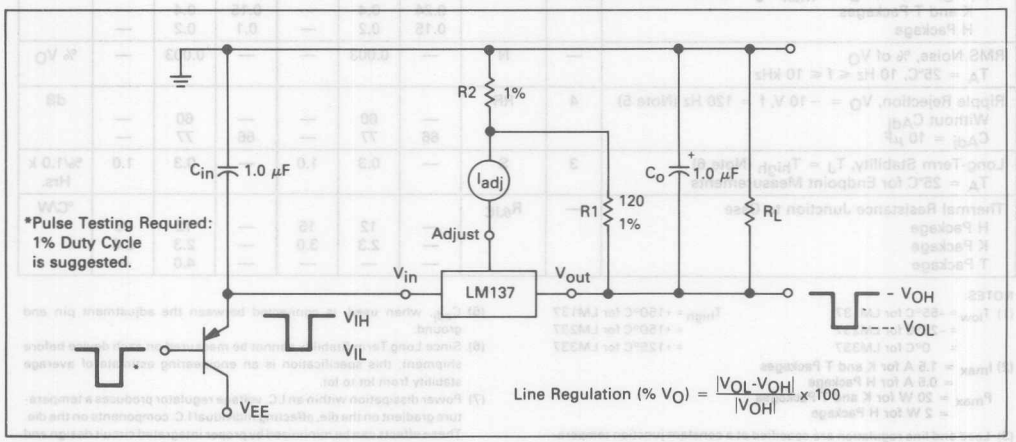


FIGURE 2 — LOAD REGULATION AND ΔI_{Adj}/LOAD TEST CIRCUIT

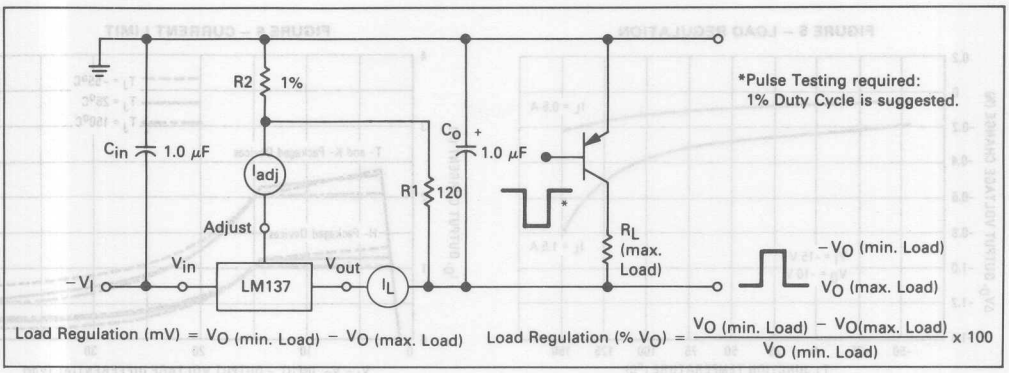


FIGURE 3 — STANDARD TEST CIRCUIT

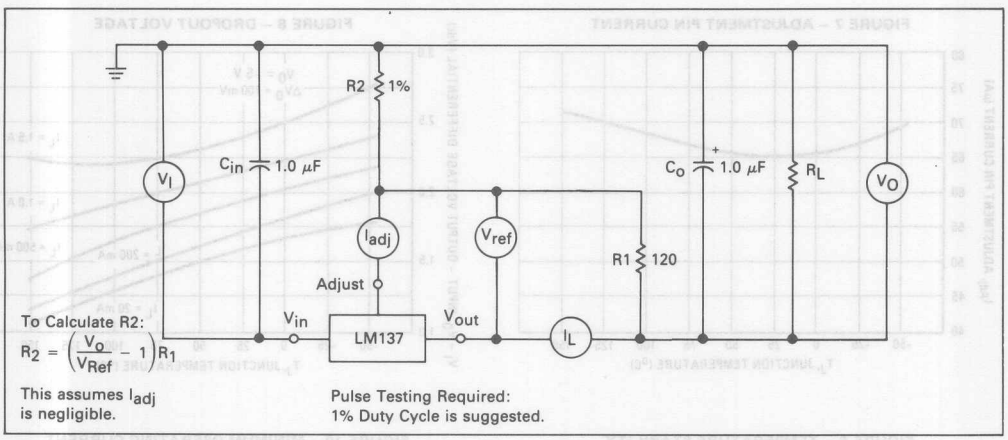
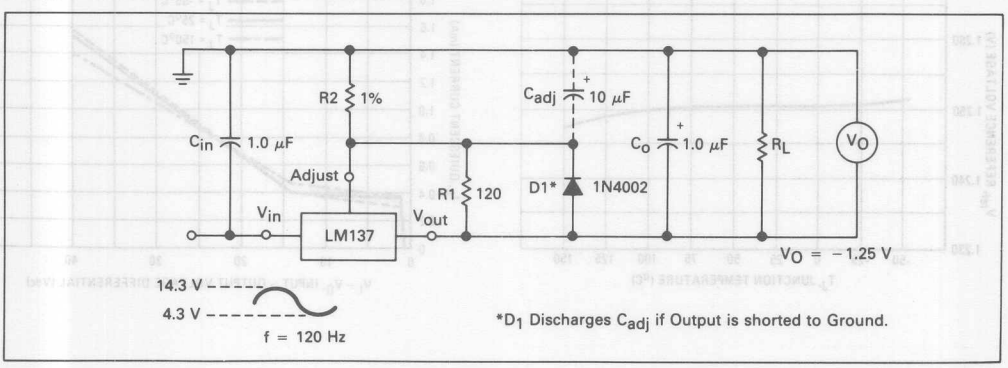


FIGURE 4 — RIPPLE REJECTION TEST CIRCUIT



3

FIGURE 5 – LOAD REGULATION

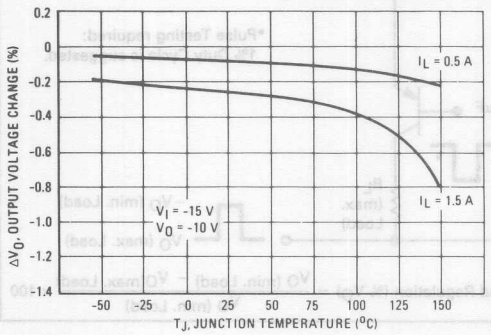


FIGURE 6 – CURRENT LIMIT

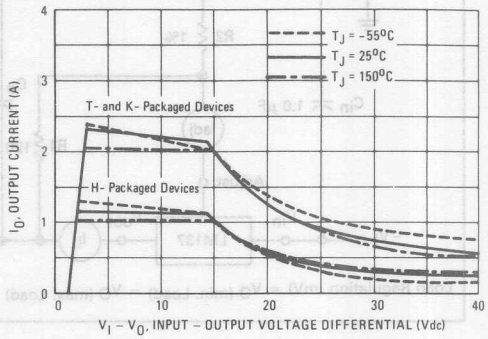


FIGURE 7 – ADJUSTMENT PIN CURRENT

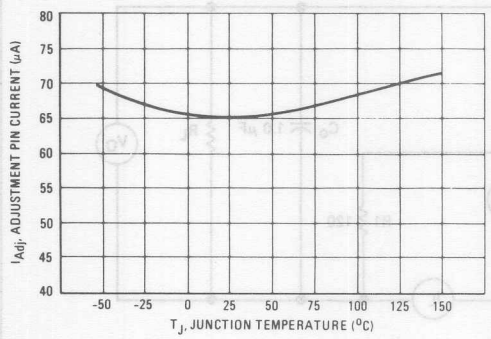


FIGURE 8 – DROPOUT VOLTAGE

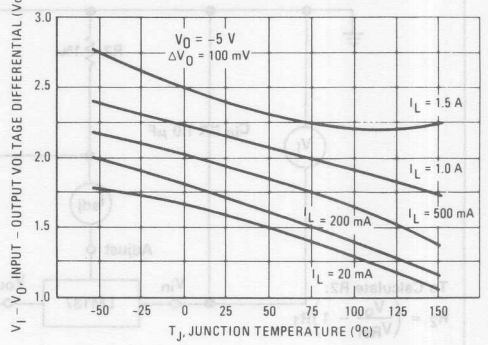


FIGURE 9 – TEMPERATURE STABILITY

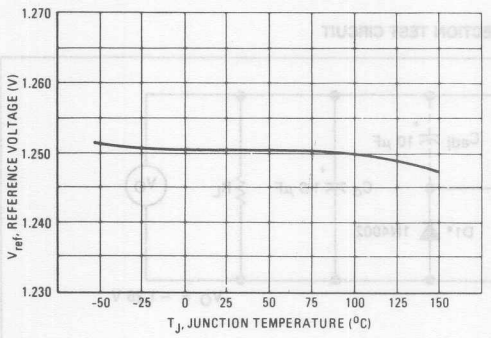


FIGURE 10 – MINIMUM OPERATING CURRENT

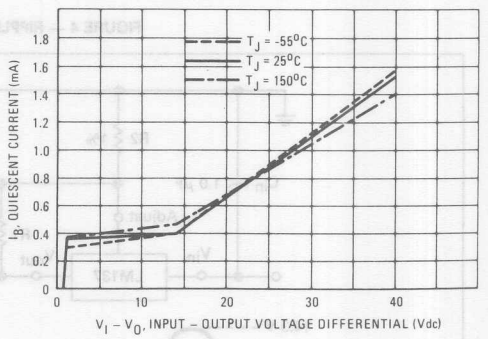


FIGURE 11 — RIPPLE REJECTION versus OUTPUT VOLTAGE

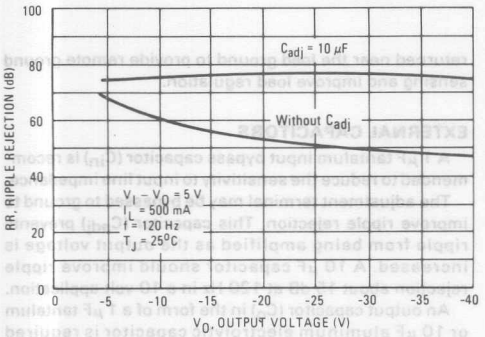


FIGURE 12 — RIPPLE REJECTION versus OUTPUT CURRENT

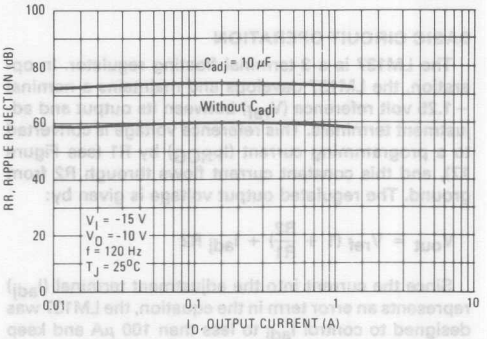


FIGURE 13 — RIPPLE REJECTION versus FREQUENCY

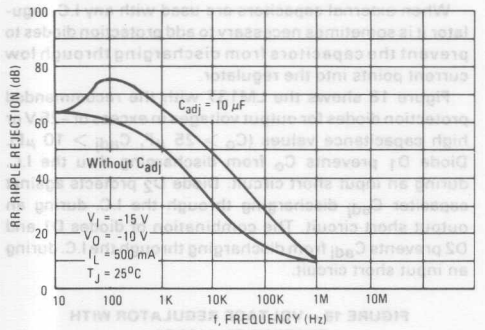


FIGURE 14 — OUTPUT IMPEDANCE

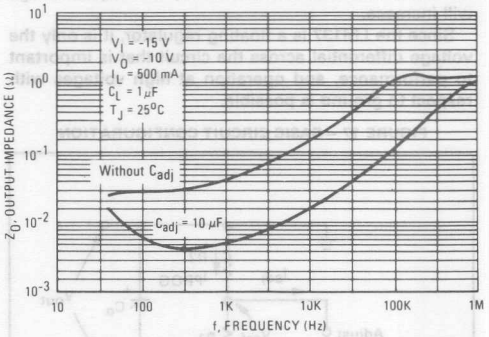


FIGURE 15 — LINE TRANSIENT RESPONSE

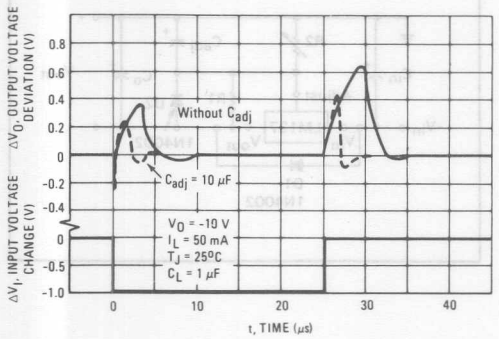
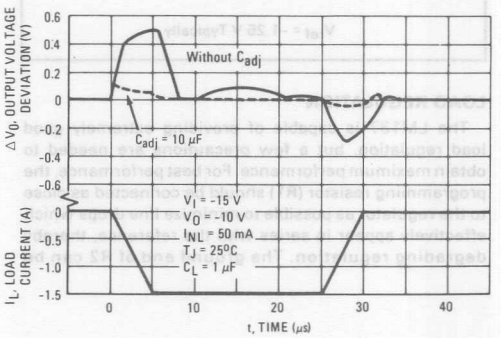


FIGURE 16 — LOAD TRANSIENT RESPONSE



3

BASIC CIRCUIT OPERATION

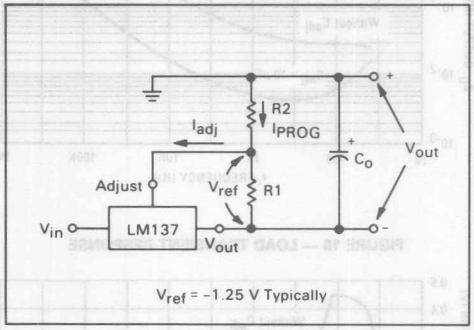
The LM137 is a 3-terminal floating regulator. In operation, the LM137 develops and maintains a nominal −1.25 volt reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by R1 (see Figure 17), and this constant current flows through R2 from ground. The regulated output voltage is given by:

$$V_{out} = V_{ref}\left(1 + \frac{R2}{R1}\right) + I_{adj}\,R2$$

Since the current into the adjustment terminal (I_{adj}) represents an error term in the equation, the LM137 was designed to control I_{adj} to less than 100 μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will increase.

Since the LM137 is a floating regulator, it is only the voltage differential across the circuit that is important to performance, and operation at high voltages with respect to ground is possible.

FIGURE 17 – BASIC CIRCUIT CONFIGURATION



LOAD REGULATION

The LM137 is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

EXTERNAL CAPACITORS

A 1 μF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{adj}) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 volt application.

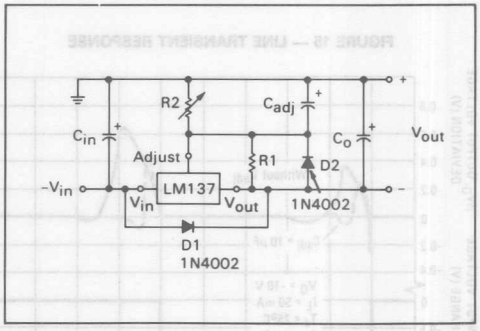
An output capacitor (C_o) in the form of a 1 μF tantalum or 10 μF aluminum electrolytic capacitor is required for stability.

PROTECTION DIODES

When external capacitors are used with any I.C. regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 18 shows the LM137 with the recommended protection diodes for output voltages in excess of −25 V or high capacitance values ($C_o > 25$ μF, $C_{adj} > 10$ μF). Diode D_1 prevents C_o from discharging thru the I.C. during an input short circuit. Diode D_2 protects against capacitor C_{adj} discharging through the I.C. during an output short circuit. The combination of diodes D1 and D2 prevents C_{adj} from discharging through the I.C. during an input short circuit.

FIGURE 18 – VOLTAGE REGULATOR WITH PROTECTION DIODES



MOTOROLA

LM140,A Series
LM340,A Series

Specifications and Applications Information

THREE-TERMINAL POSITIVE VOLTAGE REGULATORS

This family of fixed voltage regulators are monolithic integrated circuits capable of driving loads in excess of 1.0 ampere. These three-terminal regulators employ internal current limiting, thermal shutdown, and safe-area compensation. Devices are available with improved specifications, including a 2% output voltage tolerance, on A-suffix 5.0, 12 and 15 volt device types.

Although designed primarily as a fixed voltage regulator, these devices can be used with external components to obtain adjustable voltages and currents. This series of devices can be used with a series-pass transistor to boost output current capability at the nominal output voltage.

- Output Current in Excess of 1.0 Ampere
- No External Components Required
- Output Voltage Offered in 2% and 4% Tolerance*
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation

ORDERING INFORMATION

Device	Output Voltage and Tolerance	Tested Operating Junction Temp. Range	Package
LM140K-5.0	5.0 V ± 4%	−55°C to +150°C	Metal Power
LM140AK-5.0	5.0 V ± 2%	−55°C to +150°C	Metal Power
LM140K-8.0	8.0 V ± 4%	−55°C to +150°C	Metal Power
LM140K-12	12 V ± 4%	−55°C to +150°C	Metal Power
LM140AK-12	12 V ± 2%	−55°C to +150°C	Metal Power
LM140K-15	15 V ± 4%	−55°C to +150°C	Metal Power
LM140AK-15	15 V ± 2%	−55°C to +150°C	Metal Power
LM340K-5.0	5.0 V ± 4%	0°C to +125°C	Metal Power
LM340AK-5.0	5.0 V ± 2%	0°C to +125°C	
LM340T-5.0	5.0 V ± 4%	0°C to +125°C	Plastic Power
LM340AT-5.0	5.0 V ± 2%	0°C to +125°C	
LM340T-6.0	6.0 V ± 4%	0°C to +125°C	Plastic Power
LM340K-8.0	8.0 V ± 4%	0°C to +125°C	Metal Power
LM340T-8.0	8.0 V ± 4%	0°C to +125°C	Plastic Power
LM340K-12	12 V ± 4%	0°C to +125°C	Metal Power
LM340AK-12	12 V ± 2%	0°C to +125°C	
LM340T-12	12 V ± 4%	0°C to +125°C	Plastic Power
LM340AT-12	12 V ± 2%	0°C to +125°C	
LM340K-15	15 V ± 4%	0°C to +125°C	Metal Power
LM340AK-15	15 V ± 2%	0°C to +125°C	
LM340T-15	15 V ± 4%	0°C to +125°C	Plastic Power
LM340AT-15	15 V ± 2%	0°C to +125°C	
LM340T-18	18 V ± 4%	0°C to +125°C	Plastic Power
LM340T-24	24 V ± 4%	0°C to +125°C	Plastic Power

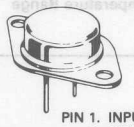
*2% regulators are available in 5, 12 and 15 volt devices

THREE-TERMINAL POSITIVE FIXED VOLTAGE REGULATORS

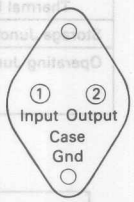
SILICON MONOLITHIC INTEGRATED CIRCUIT

3

K SUFFIX
METAL PACKAGE
CASE 1-03

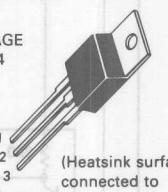


PIN 1. INPUT
2. OUTPUT
CASE GROUND



(Bottom View)

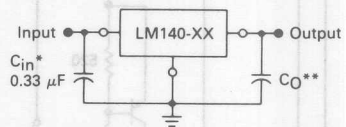
T SUFFIX
PLASTIC PACKAGE
CASE 221A-04



PIN 1. INPUT
2. GROUND
3. OUTPUT

(Heatsink surface connected to Pin 2)

STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 1.7 V above the output voltage even during the low point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

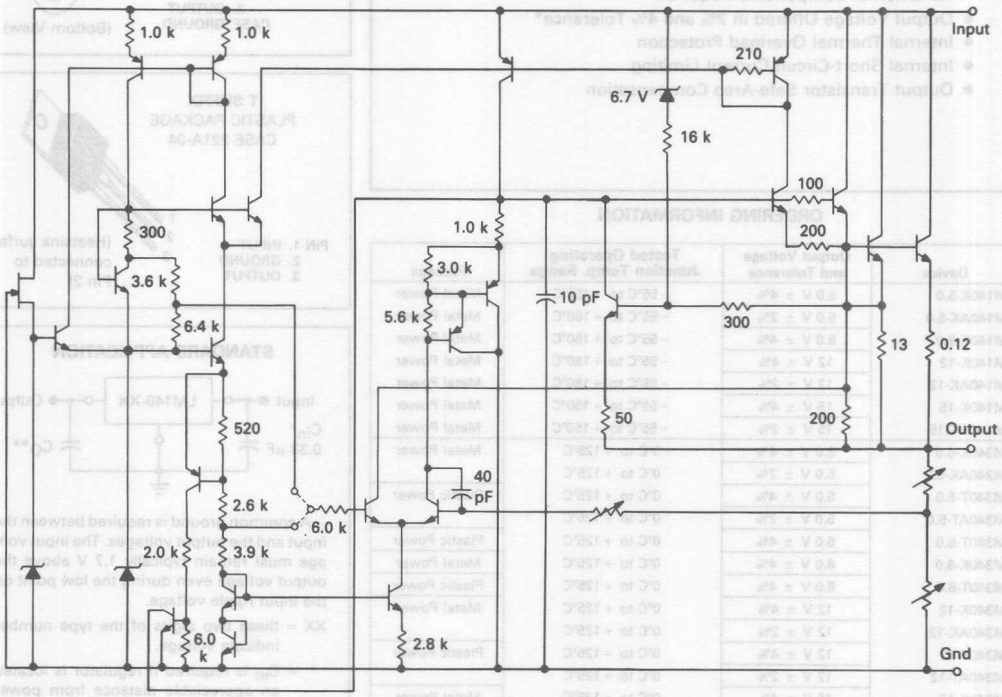
** = C_O is not needed for stability; however, it does improve transient response. If needed, use a 0.1 μF ceramic disc.

3

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (5.0 V – 18 V) (24 V)	V_{in}	35 40	Vdc
Power Dissipation and Thermal Characteristics			
Plastic Package			
T_A = +25°C	P_D	Internally Limited	Watts
Derate above T_A = +25°C	$1/\theta_{JA}$	15.4	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	65	°C/W
T_C = +25°C	P_D	Internally Limited	Watts
Derate above T_C = +75°C (See Figure 1)	$1/\theta_{JC}$	200	mW/°C
Thermal Resistance, Junction to Case	θ_{JC}	5.0	°C/W
Metal Package			
T_C = +25°C	P_D	Internally Limited	Watts
Derate above T_A = +25°C	$1/\theta_{JA}$	22.5	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	45	°C/W
T_C = +25°C	P_D	Internally Limited	Watts
Derate above T_C = +65°C (See Figure 2)	$1/\theta_{JC}$	182	mW/°C
Thermal Resistance, Junction to Case	θ_{JC}	5.5	°C/W
Storage Junction Temperature Range	T_{stg}	– 65 to +150	°C
Operating Junction Temperature Range	T_J		°C
LM140,A		– 55 to +150	
LM340,A		0 to +150	

EQUIVALENT SCHEMATIC DIAGRAM



DEFINITIONS

Line Regulation — The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation — The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation — The maximum total device dissipation for which the regulator will operate within specifications.

Quiescent Current — That part of the input current that is not delivered to the load.

Output Noise Voltage — The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

LM140/340 — 5.0

ELECTRICAL CHARACTERISTICS (V_{in} = 10 V, I_O = 500 mA, T_J = T_{low} to T_{high} (Note 1), unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	4.8	5.0	5.2	Vdc
Line Regulation (Note 2)	Reg_{line}				mV
8.0 to 20 Vdc		—	—	50	
7.0 to 25 Vdc (T_J = +25°C)		—	—	50	
8.0 to 12 Vdc, I_O = 1.0 A		—	—	25	
7.3 to 20 Vdc, I_O = 1.0 A (T_J = +25°C)		—	—	50	
Load Regulation (Note 2)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.0 A		—	—	50	
5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C)		—	—	50	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		—	—	25	
Output Voltage	V_O				Vdc
LM140					
8.0 ≤ V_{in} ≤ 20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W		4.75	—	5.25	
LM340					
7.0 ≤ V_{in} ≤ 20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W		4.75	—	5.25	
Quiescent Current	I_B				mA
I_O = 1.0 A					
LM140		—	—	7.0	
LM340		—	—	8.5	
LM140 (T_J = +25°C)		—	4.0	6.0	
LM340 (T_J = +25°C)		—	4.0	8.0	
Quiescent Current Change	ΔI_B				mA
8.0 ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA LM140		—	—	0.8	
7.0 ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA LM340		—	—	1.0	
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 10 V LM140, LM340		—	—	0.5	
8.0 ≤ V_{in} ≤ 20 Vdc, I_O = 1.0 A LM140		—	—	0.8	
7.5 ≤ V_{in} ≤ 20 Vdc, I_O = 1.0 A LM340		—	—	1.0	
Ripple Rejection	RR				dB
LM140		68	—	—	
LM340		62	—	—	
I_O = 1.0 A (T_J = +25°C)					
LM140		68	80	—	
LM340		62	80	—	
Dropout Voltage	$V_{in} - V_O$	—	1.7	—	Vdc
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	mΩ
Short Circuit Current Limit (T_J = +25°C)	I_{sc}	—	2.0	—	mA
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	40	—	μV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	—	±0.6	—	mV/°C
Peak Output Current (T_J = +25°C)	I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1.0 A		7.3	—	—	Vdc

NOTES: 1. T_{low} = −55°C for LM140 T_{high} = +150°C for LM140
= 0°C for LM340 = +125°C for LM340

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

LM140A/340A — 5.0

ELECTRICAL CHARACTERISTICS (V_{in} = 10 V, I_O = 1.0 A, T_J = T_{low} to T_{high} (Note 1), unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	4.9	5.0	5.1	Vdc
Line Regulation (Note 2) 7.5 to 20 Vdc, I_O = 500 mA 7.3 to 20 Vdc (T_J = +25°C) 8.0 to 12 Vdc 8.0 to 12 Vdc (T_J = +25°C)	Reg_{line}	 — — — —	 — 3.0 — —	 10 10 12 4.0	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.0 A 5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C) 250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)	Reg_{load}	 — — —	 — — —	 25 25 15	mV
Output Voltage 7.5 ≤ V_{in} ≤ 20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W	V_O	4.8	—	5.2	Vdc
Quiescent Current (T_J = +25°C)	I_B	— —	— 3.5	6.5 6.0	mA
Quiescent Current Change 5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 10 V 8.0 ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA 7.5 ≤ V_{in} ≤ 20 Vdc, I_O = 1.0 A (T_J = +25°C)	ΔI_B	 — — —	 — — —	 0.5 0.8 0.8	mA
Ripple Rejection 8.0 ≤ V_{in} ≤ 18 Vdc, f = 120 Hz I_O = 500 mA I_O = 1.0 A (T_J = +25°C)	RR	 68 68	 — 80	 — —	dB
Dropout Voltage	$V_{in} - V_O$	—	1.7	—	Vdc
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	mΩ
Short Circuit Current Limit (T_J = +25°C)	I_{sc}	—	2.0	—	mA
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	40	—	μV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	—	±0.6	—	mV/°C
Peak Output Current (T_J = +25°C)	I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation (T_J = +25°C)		7.3	—	—	Vdc

NOTES:

1. T_{low} = −55°C for LM140A T_{high} = +150°C for LM140A
   = 0°C for LM340A = +125°C for LM340A
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

LM140/340 — 6.0

ELECTRICAL CHARACTERISTICS (V_{in} = 11 V, I_O = 500 mA, T_J = T_{low} to T_{high} (Note 1), unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	5.75	6.0	6.25	Vdc
Line Regulation (Note 2)	Reg_{line}				mV
9.0 to 21 Vdc		—	—	60	
8.0 to 25 Vdc (T_J = +25°C)		—	—	60	
9.0 to 13 Vdc, I_O = 1.0 A		—	—	30	
8.3 to 21 Vdc, I_O = 1.0 A (T_J = +25°C)		—	—	60	
Load Regulation (Note 2)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.0 A		—	—	60	
5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C)		—	—	60	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		—	—	30	
Output Voltage	V_O				Vdc
LM140					
9.0 ≤ V_{in} ≤ 21 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W		5.7	—	6.3	
LM340					
8.0 ≤ V_{in} ≤ 21 Vdc, 6.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W		5.7	—	6.3	
Quiescent Current	I_B				mA
I_O = 1.0 A					
LM140		—	—	7.0	
LM340		—	—	8.5	
LM140 (T_J = +25°C)		—	4.0	6.0	
LM340 (T_J = +25°C)		—	4.0	8.0	
Quiescent Current Change	ΔI_B				mA
9.0 ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA LM140		—	—	0.8	
8.0 ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA LM340		—	—	1.0	
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 11 V LM140, LM340		—	—	0.5	
9.0 ≤ V_{in} ≤ 21 Vdc, I_O = 1.0 A LM140		—	—	0.8	
8.6 ≤ V_{in} ≤ 21 Vdc, I_O = 1.0 A LM340		—	—	1.0	
Ripple Rejection	RR				dB
LM140		65	—	—	
LM340		59	—	—	
I_O = 1.0 A (T_J = +25°C)					
LM140		65	78	—	
LM340		59	78	—	
Dropout Voltage	$V_{in} - V_O$	—	1.7	—	Vdc
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	mΩ
Short Circuit Current Limit (T_J = +25°C)	I_{sc}	—	1.9	—	mA
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	45	—	μV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	—	±0.7	—	mV/°C
Peak Output Current (T_J = +25°C)	I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1.0 A		8.3	—	—	Vdc

NOTES:

1. T_{low} = −55°C for LM140 T_{high} = +150°C for LM140
   = 0°C for LM340 = +125°C for LM340
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

3

LM140/340 — 8.0

ELECTRICAL CHARACTERISTICS (V_{in} = 14 V, I_O = 500 mA, T_J = T_{low} to T_{high} (Note 1), unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	7.7	8.0	8.3	Vdc
Line Regulation (Note 2)	Reg_{line}				mV
11 to 23 Vdc		—	—	80	
10.5 to 25 Vdc (T_J = +25°C)		—	—	80	
11 to 17 Vdc, I_O = 1.0 A		—	—	40	
10.5 to 23 Vdc, I_O = 1.0 A (T_J = +25°C)		—	—	80	
Load Regulation (Note 2)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.0 A		—	—	80	
5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C)		—	—	80	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		—	—	40	
Output Voltage	V_O				Vdc
LM140					
11.5 ≤ V_{in} ≤ 23 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W		7.6	—	8.4	
LM340					
10.5 ≤ V_{in} ≤ 23 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W		7.6	—	8.4	
Quiescent Current	I_B				mA
I_O = 1.0 A					
LM140		—	—	7.0	
LM340		—	—	8.5	
LM140 (T_J = +25°C)		—	4.0	6.0	
LM340 (T_J = +25°C)		—	4.0	8.0	
Quiescent Current Change	ΔI_B				mA
11.5 ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA LM140		—	—	0.8	
10.5 ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA LM340		—	—	1.0	
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 14 V LM140, LM340		—	—	0.5	
11.5 ≤ V_{in} ≤ 23 Vdc, I_O = 1.0 A LM140		—	—	0.8	
10.6 ≤ V_{in} ≤ 23 Vdc, I_O = 1.0 A LM340		—	—	1.0	
Ripple Rejection	RR				dB
LM140		62	—	—	
LM340		56	—	—	
I_O = 1.0 A (T_J = +25°C)					
LM140		62	76	—	
LM340		56	76	—	
Dropout Voltage	$V_{in} - V_O$	—	1.7	—	Vdc
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	mΩ
Short Circuit Current Limit (T_J = +25°C)	I_{sc}	—	1.5	—	mA
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	52	—	μV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	—	±1.0	—	mV/°C
Peak Output Current (T_J = +25°C)	I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1.0 A		10.5	—	—	Vdc

NOTES:

1. T_{low} = −55°C for LM140 T_{high} = +150°C for LM140
   = 0°C for LM340 = +125°C for LM340
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

LM140/340 — 12

ELECTRICAL CHARACTERISTICS (V_{in} = 19 V, I_O = 500 mA, T_J = T_{low} to T_{high} (Note 1), unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	11.5	12	12.5	Vdc
Line Regulation (Note 2)	Reg_{line}				mV
15 to 27 Vdc		—	—	120	
14.6 to 30 Vdc (T_J = +25°C)		—	—	120	
16 to 22 Vdc, I_O = 1.0 A		—	—	60	
14.6 to 27 Vdc, I_O = 1.0 A (T_J = +25°C)		—	—	120	
Load Regulation (Note 2)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.0 A		—	—	120	
5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C)		—	—	120	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		—	—	60	
Output Voltage	V_O				Vdc
LM140					
15.5 ≤ V_{in} ≤ 27 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W		11.4	—	12.6	
LM340					
14.5 ≤ V_{in} ≤ 27 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W		11.4	—	12.6	
Quiescent Current	I_B				mA
I_O = 1.0 A					
LM140		—	—	7.0	
LM340		—	—	8.5	
LM140 (T_J = +25°C)		—	4.0	6.0	
LM340 (T_J = +25°C)		—	4.0	8.0	
Quiescent Current Change	ΔI_B				mA
15 ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA LM140		—	—	0.8	
14.5 ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA LM340		—	—	1.0	
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 19 V LM140, LM340		—	—	0.5	
15 ≤ V_{in} ≤ 27 Vdc, I_O = 1.0 A LM140		—	—	0.8	
14.8 ≤ V_{in} ≤ 27 Vdc, I_O = 1.0 A LM340		—	—	1.0	
Ripple Rejection	RR				dB
LM140		61	—	—	
LM340		55	—	—	
I_O = 1.0 A (T_J = +25°C)					
LM140		61	72	—	
LM340		55	72	—	
Dropout Voltage	$V_{in} - V_O$	—	1.7	—	Vdc
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	mΩ
Short Circuit Current Limit (T_J = +25°C)	I_{sc}	—	1.1	—	mA
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	75	—	μV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	—	±1.5	—	mV/°C
Peak Output Current (T_J = +25°C)	I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1.0 A		14.6	—	—	Vdc

NOTES:

1. T_{low} = −55°C for LM140 T_{high} = +150°C for LM140
   = = +125°C for LM340
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS (V_{in} = 19 V, I_O = 1.0 A, T_J = T_{low} to T_{high} (Note 1), unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	11.75	12	12.25	Vdc
Line Regulation (Note 2) 14.8 to 27 Vdc, I_O = 500 mA 14.5 to 27 Vdc (T_J = +25°C) 16 to 22 Vdc 16 to 22 Vdc (T_J = +25°C)	Reg_{line}	— — — —	— 4.0 — —	18 18 30 9.0	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.0 A 5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C) 250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)	Reg_{load}	— — —	— — —	60 32 19	mV
Output Voltage 14.8 ≤ V_{in} ≤ 27 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W	V_O	11.5	—	12.5	Vdc
Quiescent Current (T_J = +25°C)	I_B	— —	— 3.5	6.5 6.0	mA
Quiescent Current Change 5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 19 V 15 ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA 14.8 ≤ V_{in} ≤ 27 Vdc, I_O = 1.0 A (T_J = +25°C)	ΔI_B	— — —	— — —	0.5 0.8 0.8	mA
Ripple Rejection 15 ≤ V_{in} ≤ 25 Vdc, f = 120 Hz I_O = 500 mA I_O = 1.0 A, (T_J = +25°C)	RR	61 61	— 72	— —	dB
Dropout Voltage	$V_{in} - V_O$	—	1.7	—	Vdc
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	mΩ
Short Circuit Current Limit (T_J = +25°C)	I_{sc}	—	1.1	—	mA
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	75	—	μV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	—	±1.5	—	mV/°C
Peak Output Current (T_J = +25°C)	I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation (T_J = +25°C)		14.5	—	—	Vdc

NOTES:

1. T_{low} = −55°C for LM140A T_{high} = +150°C for LM140A
   = 0°C for LM340A = +125°C for LM340A
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

LM140A/340 — 15

ELECTRICAL CHARACTERISTICS (V_{in} = 23 V, I_O = 500 mA, T_J = T_{low} to T_{high} (Note 1), unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	14.4	15	15.6	Vdc
Line Regulation (Note 2)	Reg_{line}				mV
18.5 to 30 Vdc		—	—	150	
17.5 to 30 Vdc (T_J = +25°C)		—	—	150	
20 to 26 Vdc, I_O = 1.0 A		—	—	75	
17.7 to 30 Vdc, I_O = 1.0 A (T_J = +25°C)		—	—	150	
Load Regulation (Note 2)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.0 A		—	—	150	
5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C)		—	—	150	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		—	—	75	
Output Voltage	V_O				Vdc
LM140					
18.5 ≤ V_{in} ≤ 30 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W		14.25	—	15.75	
LM340					
17.5 ≤ V_{in} ≤ 30 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W		14.25	—	15.75	
Quiescent Current	I_B				mA
I_O = 1.0 A					
LM140		—	—	7.0	
LM340		—	—	8.5	
LM140 (T_J = +25°C)		—	4.0	6.0	
LM340 (T_J = +25°C)		—	4.0	8.0	
Quiescent Current Change	ΔI_B				mA
18.5 ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA LM140		—	—	0.8	
17.5 ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA LM340		—	—	1.0	
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 23 V LM140, LM340		—	—	0.5	
18.5 ≤ V_{in} ≤ 30 Vdc, I_O = 1.0 A LM140		—	—	0.8	
17.9 ≤ V_{in} ≤ 30 Vdc, I_O = 1.0 A LM340		—	—	1.0	
Ripple Rejection	RR				dB
LM140		60	—	—	
LM340		54	—	—	
I_O = 1.0 A (T_J = +25°C)					
LM140		60	70	—	
LM340		54	70	—	
Dropout Voltage	$V_{in} - V_O$	—	1.7	—	Vdc
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	mΩ
Short Circuit Current Limit (T_J = +25°C)	I_{sc}	—	800	—	mA
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	90	—	μV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	—	±1.8	—	mV/°C
Peak Output Current (T_J = +25°C)	I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1.0 A		17.7	—	—	Vdc

NOTES:

1. T_{low} = −55°C for LM140 T_{high} = +150°C for LM140
   = = +125°C for LM340
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

LM140A/340A — 15

ELECTRICAL CHARACTERISTICS (V_{in} = 23 V, I_O = 1.0 A, T_J = T_{low} to T_{high} (Note 1), unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	14.7	15	15.3	Vdc
Line Regulation (Note 2) 17.9 to 30 Vdc, I_O = 500 mA 17.5 to 30 Vdc (T_J = +25°C) 20 to 26 Vdc, I_O = 1.0 A 20 to 26 Vdc, I_O = 1.0 A (T_J = +25°C)	Reg_{line}	 — — — —	 — 4.0 — —	 22 22 30 10	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.0 A 5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C) 250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)	Reg_{load}	 — — —	 — 12 —	 75 35 21	mV
Output Voltage 17.9 ≤ V_{in} ≤ 30 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W	V_O	14.4	—	15.6	Vdc
Quiescent Current (T_J = +25°C)	I_B	— —	— 3.5	6.5 6.0	mA
Quiescent Current Change 5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 23 V 17.9 ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA 17.9 ≤ V_{in} ≤ 30 Vdc, I_O = 1.0 A (T_J = +25°C)	ΔI_B	 — — —	 — — —	 0.5 0.8 0.8	mA
Ripple Rejection 18.5 ≤ V_{in} ≤ 28.5 Vdc, f = 120 Hz I_O = 500 mA I_O = 1.0 A, (T_J = +25°C)	RR	 60 60	 — 70	 — —	dB
Dropout Voltage	$V_{in} - V_O$	—	1.7	—	Vdc
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	mΩ
Short Circuit Current Limit (T_J = +25°C)	I_{sc}	—	800	—	mA
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	90	—	μV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	—	±1.8	—	mV/°C
Peak Output Current (T_J = +25°C)	I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation (T_J = +25°C)		17.5	—	—	Vdc

NOTES:

1. T_{low} = −55°C for LM140A T_{high} = +150°C for LM140A
   = 0°C for LM340A = +125°C for LM340A
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

LM140/340 — 18

ELECTRICAL CHARACTERISTICS (V_{in} = 27 V, I_O = 500 mA, T_J = T_{low} to T_{high} (Note 1), unless otherwise noted).

Characteristic		Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A		V_O	17.3	18	18.7	Vdc
Line Regulation (Note 2) 21.5 to 33 Vdc 21 to 33 Vdc (T_J = +25°C) 24 to 30 Vdc, I_O = 1.0 A 21 to 33 Vdc, I_O = 1.0 A (T_J = +25°C)		Reg_{line}	 — — — —	 — — — —	mV 180 180 90 180	
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.0 A 5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C) 250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		Reg_{load}	 — — —	 — — —	mV 180 180 90	
Output Voltage LM140 22 ≤ V_{in} ≤ 33 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W LM340 21 ≤ V_{in} ≤ 33 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W		V_O	 17.1 17.1	 — —	Vdc 18.9 18.9	
Quiescent Current I_O = 1.0 A LM140 LM340 LM140 (T_J = +25°C) LM340 (T_J = +25°C)		I_B	 — — — —	 — — 4.0 4.0	mA 7.0 8.5 6.0 8.0	
Quiescent Current Change 22 ≤ V_{in} ≤ 33 Vdc, I_O = 500 mA 21 ≤ V_{in} ≤ 33 Vdc, I_O = 500 mA 5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 27 V 22 ≤ V_{in} ≤ 33 Vdc, I_O = 1.0 A 21 ≤ V_{in} ≤ 33 Vdc, I_O = 1.0 A	 LM140 LM340 LM140, LM340 LM140 LM340	ΔI_B	 — — — — —	 — — — — —	mA 0.8 1.0 0.5 0.8 1.0	
Ripple Rejection LM140 LM340 I_O = 1.0 A (T_J = +25°C) LM140 LM340		RR	 59 53 59 53	 — — 69 69	dB — — — —	
Dropout Voltage		$V_{in} - V_O$	—	1.7	—	Vdc
Output Resistance (f = 1.0 kHz)		r_O	—	2.0	—	mΩ
Short Circuit Current Limit (T_J = +25°C)		I_{sc}	—	500	—	mA
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz		V_n	—	110	—	μV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA		TCV_O	—	±2.3	—	mV/°C
Peak Output Current (T_J = +25°C)		I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1.0 A			21	—	—	Vdc

NOTES:

1. T_{low} = −55°C for LM140 T_{high} = +150°C for LM140
   = 0°C for LM340 = +125°C for LM340
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

Characteristic		Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A		V_O	23	24	25	Vdc
Line Regulation (Note 2)		Reg_{line}				mV
28 to 38 Vdc			—	—	240	
27 to 38 Vdc (T_J = +25°C)			—	—	240	
30 to 36 Vdc, I_O = 1.0 A			—	—	120	
27.1 to 38 Vdc, I_O = 1.0 A (T_J = +25°C)			—	—	240	
Load Regulation (Note 2)		Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.0 A			—	—	240	
5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C)			—	—	240	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)			—	—	120	
Output Voltage		V_O				Vdc
LM140						
28 ≤ V_{in} ≤ 38 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W			22.8	—	25.2	
LM340						
27 ≤ V_{in} ≤ 38 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W			22.8	—	25.2	
Quiescent Current		I_B				mA
I_O = 1.0 A						
LM140			—	—	7.0	
LM340			—	—	8.5	
LM140 (T_J = +25°C)			—	4.0	6.0	
LM340 (T_J = +25°C)			—	4.0	8.0	
Quiescent Current Change		ΔI_B				mA
28 ≤ V_{in} ≤ 38 Vdc, I_O = 500 mA	LM140		—	—	0.8	
27 ≤ V_{in} ≤ 38 Vdc, I_O = 500 mA	LM340		—	—	1.0	
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 33 V	LM140, LM340		—	—	0.5	
28 ≤ V_{in} ≤ 38 Vdc, I_O = 1.0 A	LM140		—	—	0.8	
27.3 ≤ V_{in} ≤ 38 Vdc, I_O = 1.0 A	LM340		—	—	1.0	
Ripple Rejection		RR				dB
LM140			56	—	—	
LM340			50	—	—	
I_O = 1.0 A (T_J = +25°C)						
LM140			56	66	—	
LM340			50	66	—	
Dropout Voltage		$V_{in} - V_O$	—	1.7	—	Vdc
Output Resistance (f = 1.0 kHz)		r_O	—	2.0	—	mΩ
Short Circuit Current Limit (T_J = +25°C)		I_{sc}	—	200	—	mA
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz		V_n	—	170	—	μV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA		TCV_O	—	±3.0	—	mV/°C
Peak Output Current (T_J = +25°C)		I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1.0 A			27.1	—	—	Vdc

NOTES:

1. T_{low} = −55°C for LM140 T_{high} = +150°C for LM140
   = 0°C for LM340 = +125°C for LM340
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

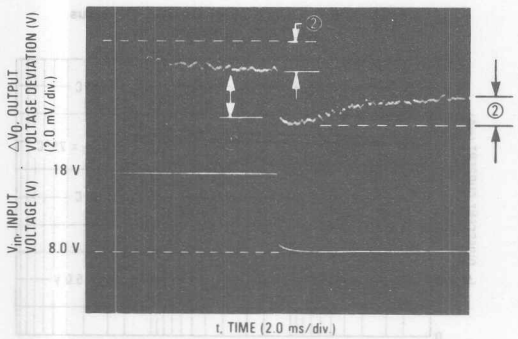
VOLTAGE REGULATOR PERFORMANCE

The performance of a voltage regulator is specified by its immunity to changes in load, input voltage, power dissipation, and temperature. Line and load regulation are tested with a pulse of short duration (< 100 μs) and are strictly a function of electrical gain. However, pulse widths of longer duration (> 1.0 ms) are sufficient to affect temperature gradients across the die. These temperature gradients can cause a change in the output voltage, in addition to changes caused by line and load regulation. Longer pulse widths and thermal gradients make it desirable to specify thermal regulation.

Thermal regulation is defined as the change in output voltage caused by a change in dissipated power for a specified time, and is expressed as a percentage output voltage change per watt. The change in dissipated power can be caused by a change in either the input voltage or the load current. Thermal regulation is a function of IC layout and die attach techniques, and usually occurs within 10 ms of a change in power dissipation. After 10 ms, additional changes in the output voltage are due to the temperature coefficient of the device.

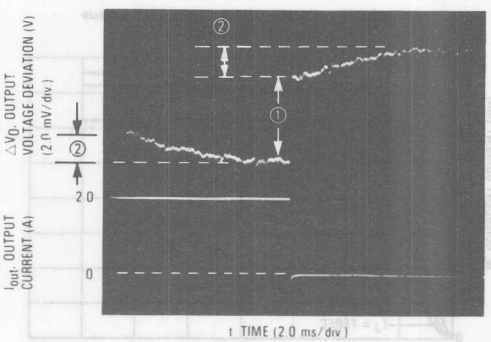
Figure 1 shows the line and thermal regulation response of a typical LM140AK-5.0 to a 10 watt input pulse. The variation of the output voltage due to line regulation is labeled ① and the thermal regulation component is labeled ②. Figure 2 shows the load and thermal regulation response of a typical LM140AK-5.0 to a 15 watt load pulse. The output voltage variation due to load regulation is labeled ① and the thermal regulation component is labeled ②.

FIGURE 1 — LINE AND THERMAL REGULATION



LM140AK-5.0
V_O = 5.0 V
V_{in} = 8.0 V → 18 V → 8.0 V ① = Reg_{line} = 2.4 mV
I_{out} = 1.0 A ② = Reg_{therm} = 0.0030%V_O/W

FIGURE 2 — LOAD AND THERMAL REGULATION



LM140AK-5.0
V_O = 5.0 V
V_{in} = 15 ① = Reg_{load} = 4.4 mV
I_{out} = 0 A → 1.5 A → 0 A ② = Reg_{therm} = 0.0020%V_O/W

FIGURE 3 — TEMPERATURE STABILITY

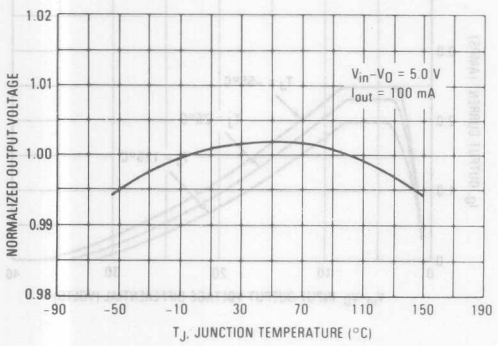
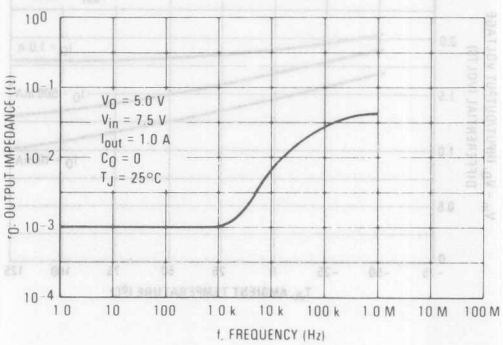


FIGURE 4 — OUTPUT IMPEDANCE



3

FIGURE 5 — RIPPLE REJECTION versus FREQUENCY

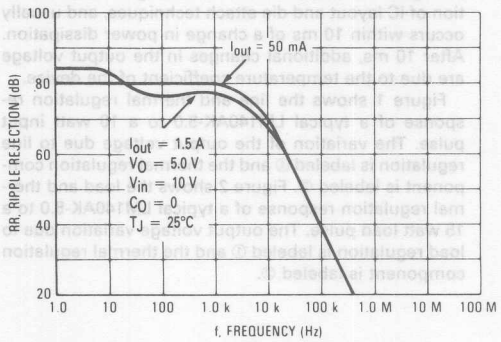


FIGURE 6 — RIPPLE REJECTION versus OUTPUT CURRENT

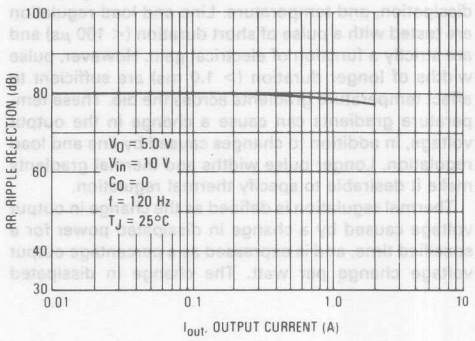


FIGURE 7 — QUIESCENT CURRENT versus INPUT VOLTAGE

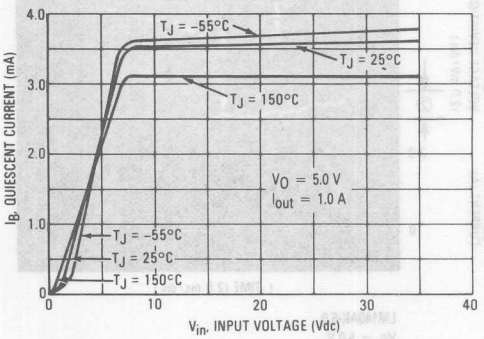


FIGURE 8 — QUIESCENT CURRENT versus OUTPUT CURRENT

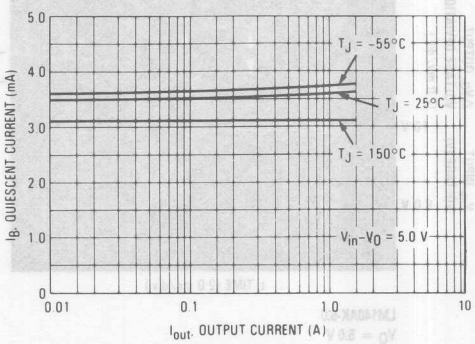


FIGURE 9 — DROPOUT VOLTAGE

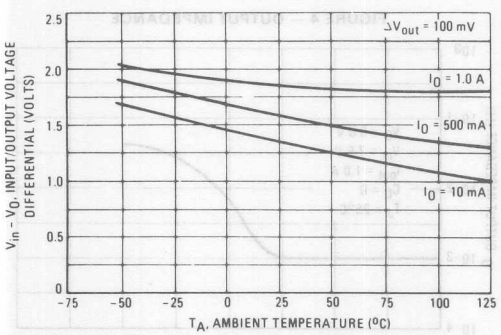


FIGURE 10 — PEAK OUTPUT CURRENT

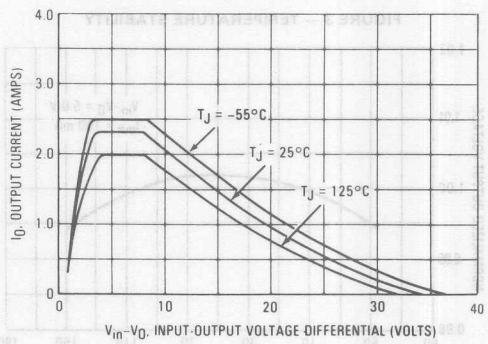


FIGURE 11 — LINE TRANSIENT RESPONSE

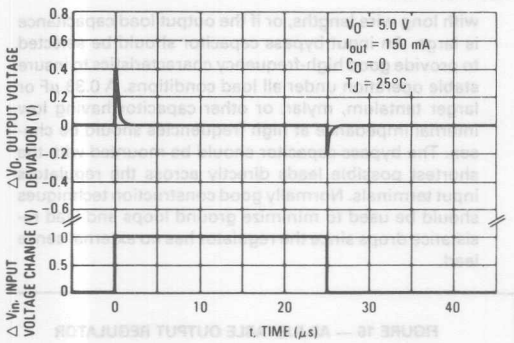


FIGURE 12 — LOAD TRANSIENT RESPONSE

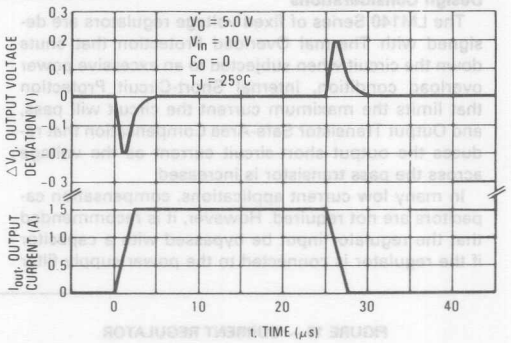


FIGURE 13 — WORST CASE POWER DISSIPATION versus AMBIENT TEMPERATURE (Case 221A)

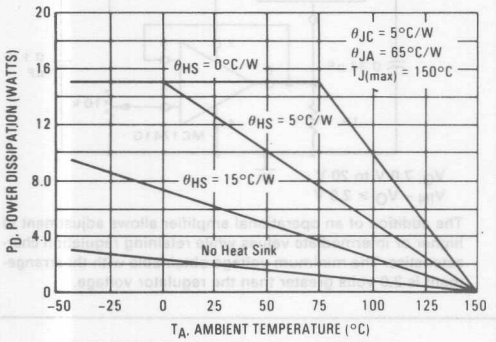
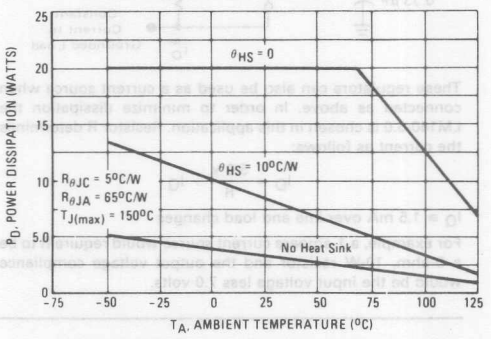


FIGURE 14 — WORST CASE POWER DISSIPATION versus AMBIENT TEMPERATURE (Case 1)



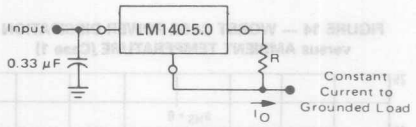
APPLICATIONS INFORMATION

Design Considerations

The LM140 Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

FIGURE 15 — CURRENT REGULATOR



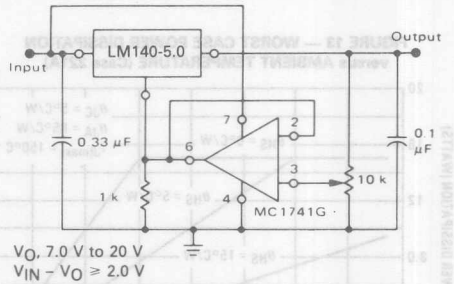
These regulators can also be used as a current source when connected as above. In order to minimize dissipation the LM140-5.0 is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5.0\ V}{R} + I_Q$$

$I_Q \cong 1.5$ mA over line and load changes

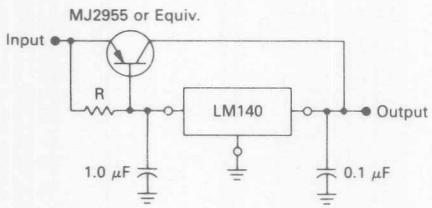
For example, a 1-ampere current source would require R to be a 5-ohm, 10-W resistor and the output voltage compliance would be the input voltage less 7.0 volts.

FIGURE 16 — ADJUSTABLE OUTPUT REGULATOR



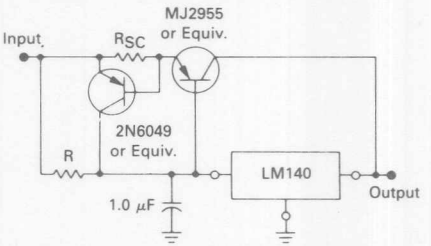
The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with thi arrangement is 2.0 volts greater than the regulator voltage.

FIGURE 17 — CURRENT BOOST REGULATOR



The LM140 series can be current boosted with a PNP transistor. The MJ2955 provides current to 5.0 amperes. Resistor R in conjunction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short-circuit proof. Input-output differential voltage minimum is increased by V_{BE} of the pass transistor.

FIGURE 18 — SHORT-CIRCUIT PROTECTION



The circuit of Figure 17 can be modified to provide supply protection against short circuits by adding a short-circuit sense resistor, R_{SC}, and an additional PNP transistor. The current sensing PNP must be able to handle the short-circuit current of the three-terminal regulator. Therefore, a four-ampere plastic power transistor is specified.

MOTOROLA

LM150
LM250
LM350

3

Specifications and Applications Information

THREE-TERMINAL ADJUSTABLE OUTPUT POSITIVE VOLTAGE REGULATORS

The LM150/250/350 are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 3.0 A over an output voltage range of 1.2 V to 33 V. These voltage regulators are exceptionally easy to use and require only two external resistors to set the output voltage. Further, they employ internal current limiting, thermal shutdown and safe area compensation, making them essentially blow-out proof.

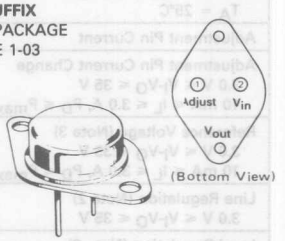
The LM150 series serve a wide variety of applications including local, on card regulation. This device also makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM150 series can be used as a precision current regulator.

- Guaranteed 3.0 Amps Output Current
- Output Adjustable between 1.2 V and 33 V
- Load Regulation Typically 0.1%
- Line Regulation Typically 0.005%/V
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting Constant with Temperature
- Output Transistor Safe-area Compensation
- Floating Operation for High Voltage Applications
- Standard 3-lead Transistor Packages
- Eliminates Stocking Many Fixed Voltages

THREE-TERMINAL ADJUSTABLE POSITIVE VOLTAGE REGULATORS

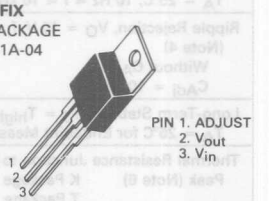
SILICON MONOLITHIC INTEGRATED CIRCUIT

K SUFFIX
METAL PACKAGE
CASE 1-03



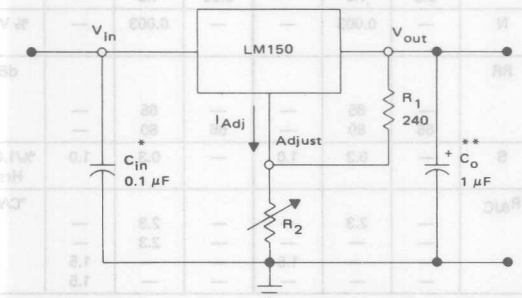
Pins 1 and 2 electrically isolated from case.
Case is third electrical connection.

T SUFFIX
PLASTIC PACKAGE
CASE 221A-04



Heatsink surface connected to Pin 2

STANDARD APPLICATION



* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_o is not needed for stability, however it does improve transient response.

$$V_{out} = 1.25\ V\ (1 + \frac{R_2}{R_1}) + I_{Adj}\ R_2$$

Since I_{Adj} is controlled to less than 100 μA, the error associated with this term is negligible in most applications

#Automotive temperature range selections are available with special test conditions and additional tests. Contact your local Motorola sales office for information.

ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
LM150K	T_J = −55°C to +150°C	Metal Power
LM250K	T_J = −25°C to +150°C	Metal Power
LM350K	T_J = 0°C to +125°C	Metal Power
LM350T	T_J = 0°C to +125°C	Plastic Power
LM350BT#	T_J = −40°C to +125°C	Plastic Power

3

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Input-Output Voltage Differential		V_I-V_O	35	Vdc
Power Dissipation		P_D	Internally Limited	
Operating Junction Temperature Range	LM150 LM250 LM350	T_J	−55 to +150 −25 to +150 0 to +125	°C
Storage Temperature Range		T_{stg}	−65 to +150	°C
Soldering Lead Temperature (10 seconds)			300	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, V_I-V_O = 5.0 V; I_L = 1.5 A; T_J = T_{low} to T_{high}; P_{max} [see Note 1].)

Characteristic	Figure	Symbol	LM150/250 Min	LM150/250 Typ	LM150/250 Max	LM350 Min	LM350 Typ	LM350 Max	Unit
Line Regulation (Note 2) T_A = 25°C, 3.0 V ≤ V_I-V_O ≤ 35 V	1	Reg_{line}	—	0.005	0.01	—	0.005	0.03	%/V
Load Regulation (Note 2) T_A = 25°C, 10 mA ≤ I_L ≤ 3.0 A V_O ≤ 5.0 V V_O ≥ 5.0 V	2	Reg_{load}	— —	5.0 0.1	15 0.3	— —	5.0 0.1	25 0.5	mV % V_O
Thermal Regulation, Pulse = 20 ms, T_A = 25°C	—	Reg_{therm}	—	0.002	—	—	0.002	—	% V_O/W
Adjustment Pin Current	3	I_{Adj}	—	50	100	—	50	100	μA
Adjustment Pin Current Change 3.0 V ≤ V_I-V_O ≤ 35 V 10 mA ≤ I_L ≤ 3.0 A, P_D ≤ P_{max}	1,2	ΔI_{Adj}	—	0.2	5.0	—	0.2	5.0	μA
Reference Voltage (Note 3) 3.0 V ≤ V_I-V_O ≤ 35 V 10 mA ≤ I_L ≤ 3.0 A, P_D ≤ P_{max}	3	V_{ref}	1.20	1.25	1.30	1.20	1.25	1.30	V
Line Regulation (Note 2) 3.0 V ≤ V_I-V_O ≤ 35 V	1	Reg_{line}	—	0.02	0.05	—	0.02	0.07	%/V
Load Regulation (Note 2) 10 mA ≤ I_L ≤ 3.0 A V_O ≤ 5.0 V V_O ≥ 5.0 V	2	Reg_{load}	— —	20 0.3	50 1.0	— —	20 0.3	70 1.5	mV % V_O
Temperature Stability (T_{low} ≤ T_J ≤ T_{high})	3	T_S	—	1.0	—	—	1.0	—	% V_O
Minimum Load Current to Maintain Regulation (V_I-V_O = 35 V)	3	I_{Lmin}	—	3.5	5.0	—	3.5	10	mA
Maximum Output Current V_I-V_O ≤ 10 V, P_D ≤ P_{max} V_I-V_O = 30 V, P_D ≤ P_{max}, T_A = 25°C	3	I_{max}	3.0 0.3	4.5 1.0	— —	3.0 0.25	4.5 1.0	— —	A
RMS Noise, % of V_O T_A = 25°C, 10 Hz ≤ f ≤ 10 kHz	—	N	—	0.003	—	—	0.003	—	% V_O
Ripple Rejection, V_O = 10 V, f = 120 Hz (Note 4) Without C_{Adj} C_{Adj} = 10 μF	4	RR	— 66	65 80	— —	— 66	65 80	— —	dB
Long-Term Stability, T_J = T_{high} (Note 5) T_A = 25°C for Endpoint Measurements	3	S	—	0.3	1.0	—	0.3	1.0	%/1.0 k Hrs.
Thermal Resistance Junction to Case Peak (Note 6) K Package T Package Average (Note 7) K Package T Package	—	$R_{\theta JC}$	— — — —	2.3 — — —	— — 1.5 —	— — — —	2.3 2.3 — —	— — 1.5 1.5	°C/W

NOTES:

(1) T_{low} = −55°C for LM150, −25°C for LM250, 0°C for LM350; T_{high} = +150°C for LM150, +150°C for LM250, +125°C for LM350
P_{max} = 30 W for K suffix
P_{max} = 25 W for T suffix

(2) Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

(3) Selected devices with tightened tolerance reference voltage available.

(4) C_{Adj}, when used, is connected between the adjustment pin and ground.

(5) Since Long-Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

(6) Thermal Resistance evaluated measuring the hottest temperature on the die using an infrared scanner. This method of evaluation yields very accurate thermal resistance values which are conservative when compared to other measurement techniques.

(7) The average die temperature is used to derive the value of thermal resistance junction to case (average).

SCHEMATIC DIAGRAM

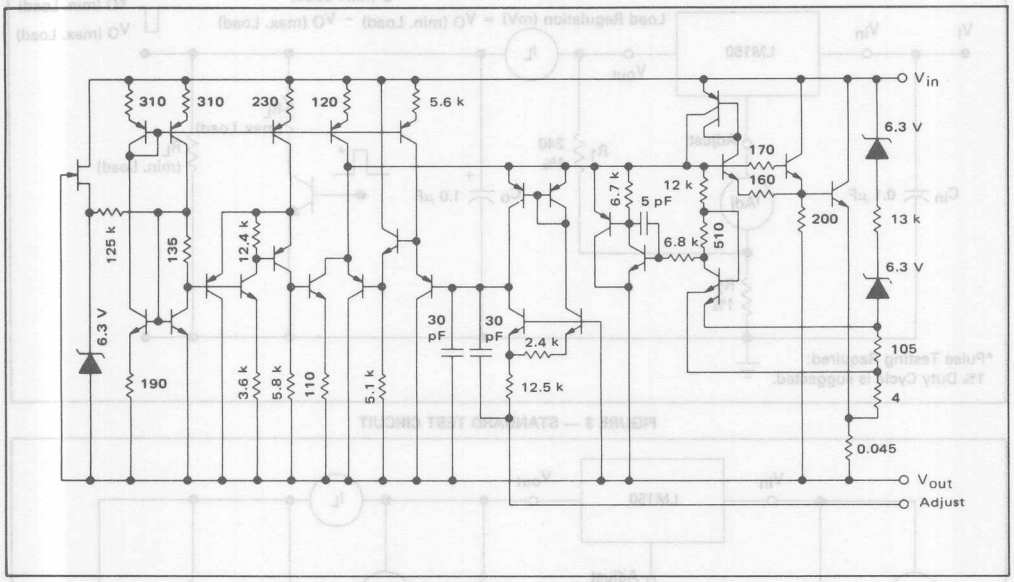
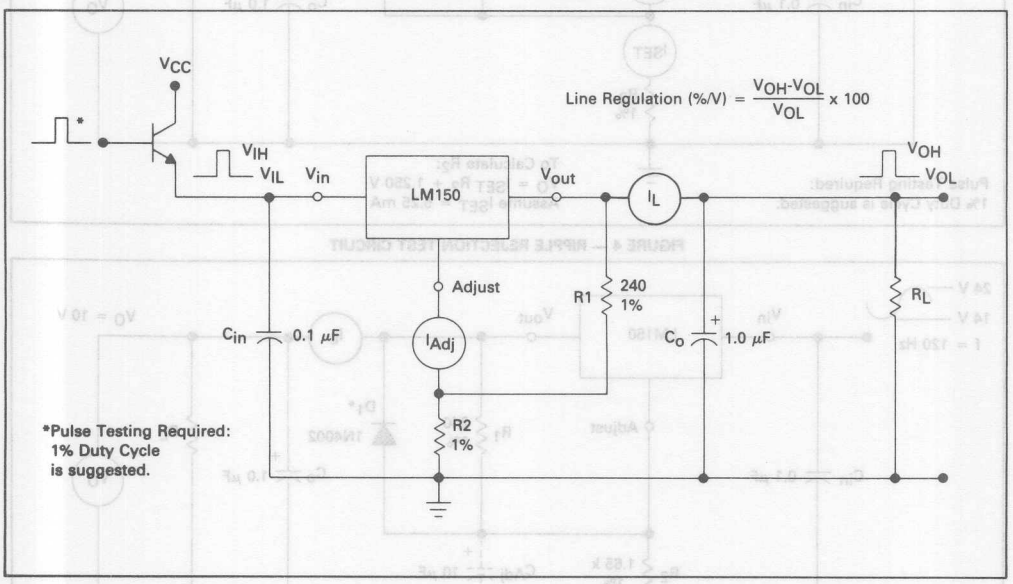


FIGURE 1 — LINE REGULATION AND ΔI_{Adj}/LINE TEST CIRCUIT



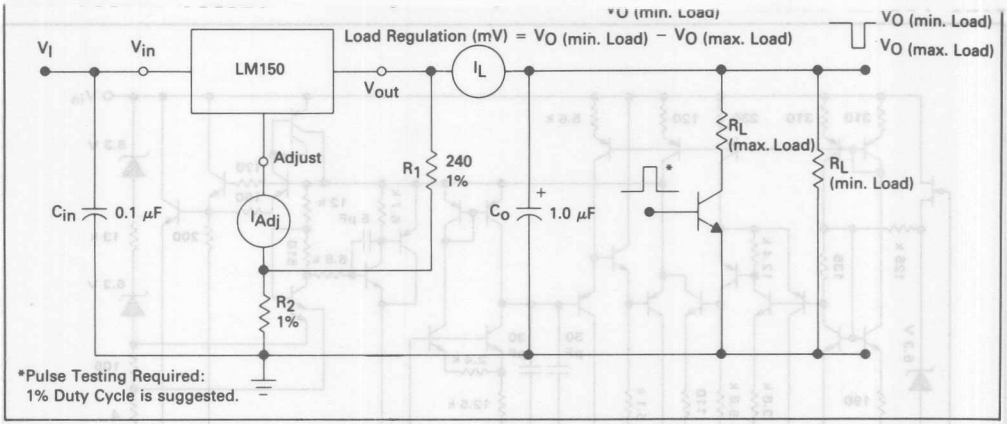


FIGURE 3 — STANDARD TEST CIRCUIT

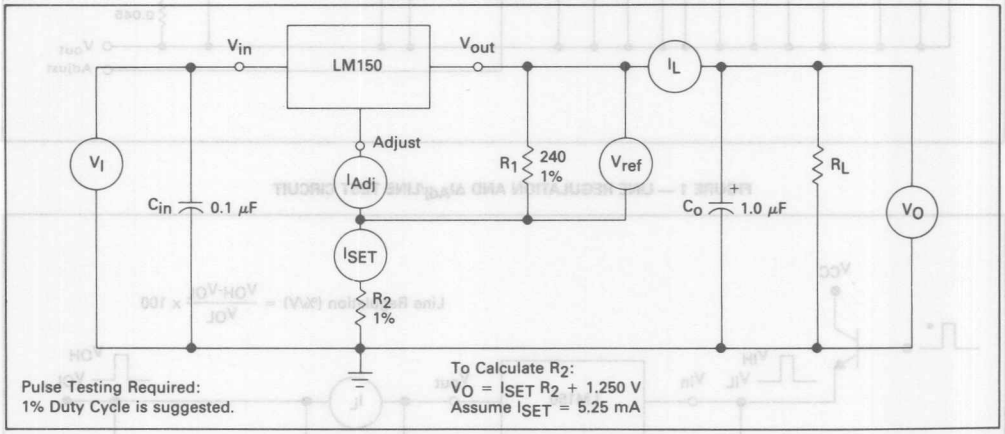


FIGURE 4 — RIPPLE REJECTION TEST CIRCUIT

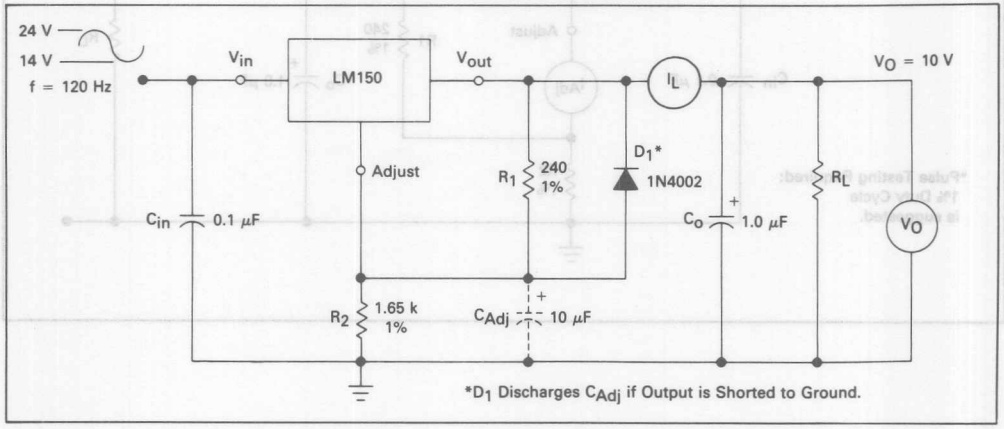


FIGURE 5 – LOAD REGULATION

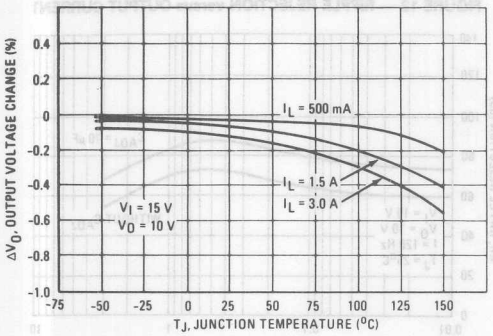


FIGURE 6 – CURRENT LIMIT

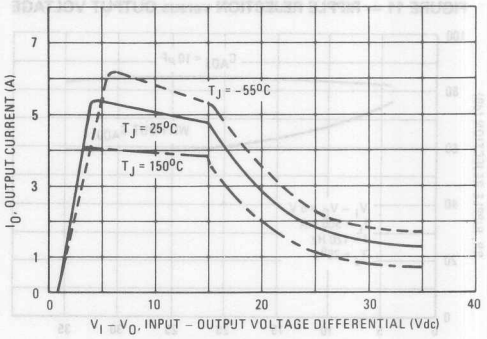


FIGURE 7 – ADJUSTMENT PIN CURRENT

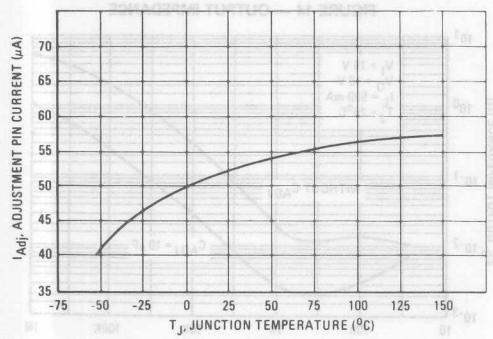


FIGURE 8 – DROPOUT VOLTAGE

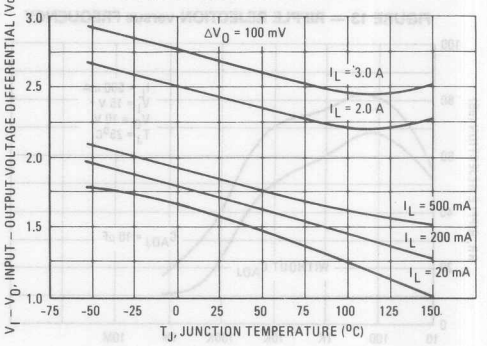


FIGURE 9 – TEMPERATURE STABILITY

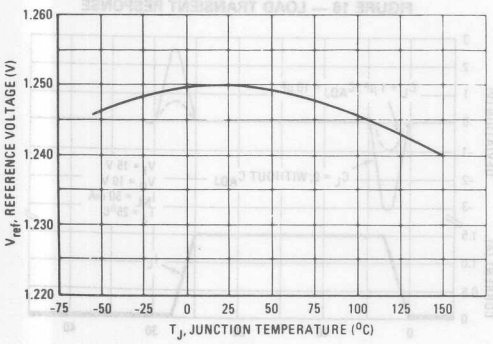
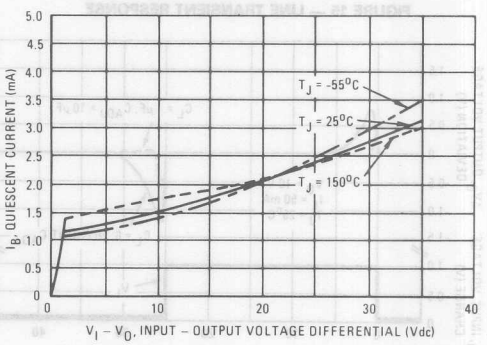


FIGURE 10 – MINIMUM OPERATING CURRENT



3

FIGURE 11 — RIPPLE REJECTION versus OUTPUT VOLTAGE

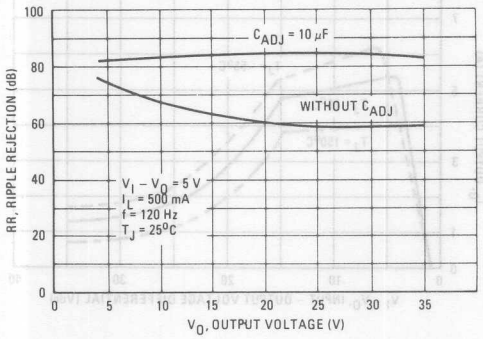


FIGURE 12 — RIPPLE REJECTION versus OUTPUT CURRENT

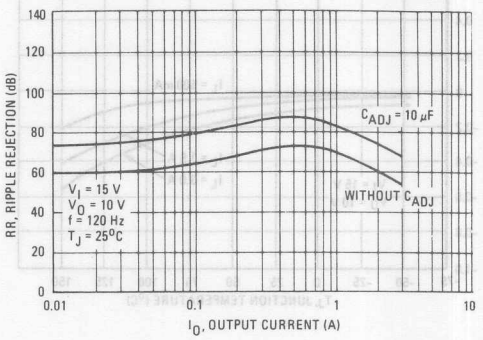


FIGURE 13 — RIPPLE REJECTION versus FREQUENCY

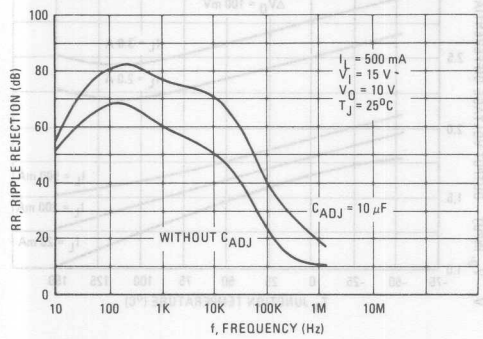


FIGURE 14 — OUTPUT IMPEDANCE

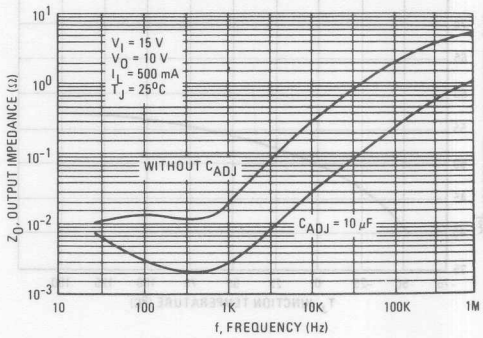


FIGURE 15 — LINE TRANSIENT RESPONSE

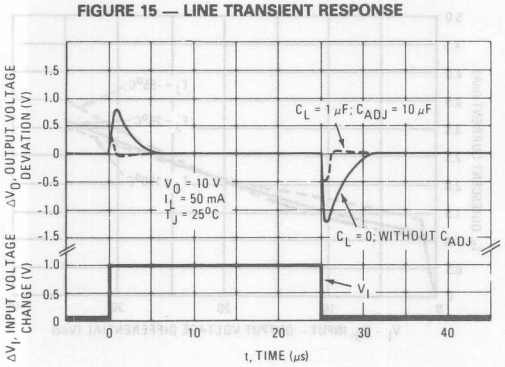
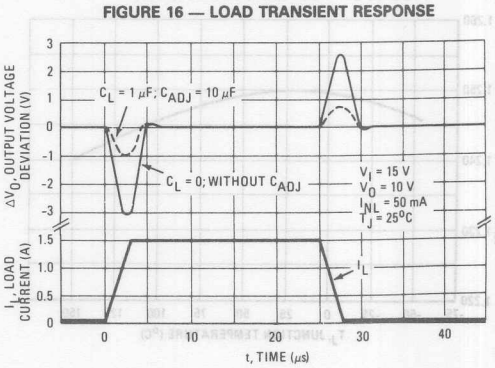


FIGURE 16 — LOAD TRANSIENT RESPONSE



APPLICATIONS INFORMATION

BASIC CIRCUIT OPERATION

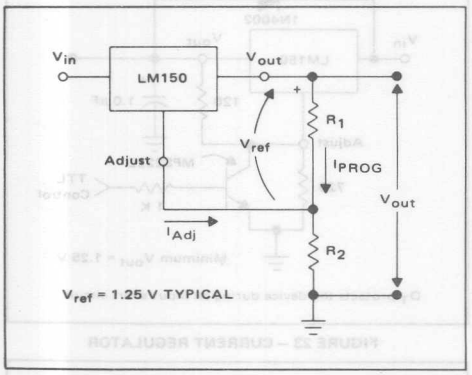
The LM150 is a 3-terminal floating regulator. In operation, the LM150 develops and maintains a nominal 1.25 volt reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by R1 (see Figure 17), and this constant current flows through R2 to ground. The regulated output voltage is given by:

$$V_{out} = V_{ref}\left(1 + \frac{R2}{R1}\right) + I_{Adj}\,R2$$

Since the current from the adjustment terminal (I_{Adj}) represents an error term in the equation, the LM150 was designed to control I_{Adj} to less than 100 μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM150 is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.

FIGURE 17 – BASIC CIRCUIT CONFIGURATION



LOAD REGULATION

The LM150 is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

EXTERNAL CAPACITORS

A 0.1 μF disc or 1 μF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{ADJ}) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 volt application.

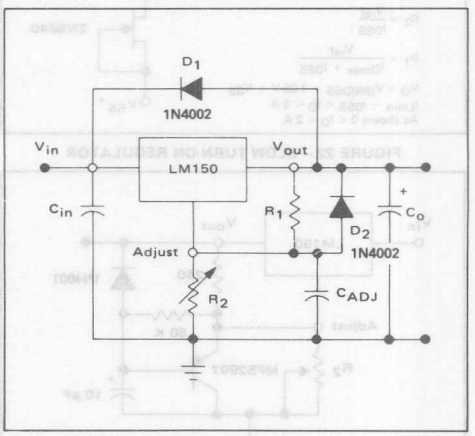
Although the LM150 is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance (C_o) in the form of a 1 μF tantalum or 25 μF aluminum electrolytic capacitor on the output swamps this effect and insures stability.

PROTECTION DIODES

When external capacitors are used with any I.C. regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 18 shows the LM150 with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values ($C_o > 25$ μF, $C_{ADJ} > 10$ μF). Diode D_1 prevents C_o from discharging thru the I.C. during an input short circuit. Diode D_2 protects against capacitor C_{ADJ} discharging through the I.C. during an output short circuit. The combination of diodes D1 and D2 prevents C_{ADJ} from discharging through the I.C. during an input short circuit.

FIGURE 18 – VOLTAGE REGULATOR WITH PROTECTION DIODES



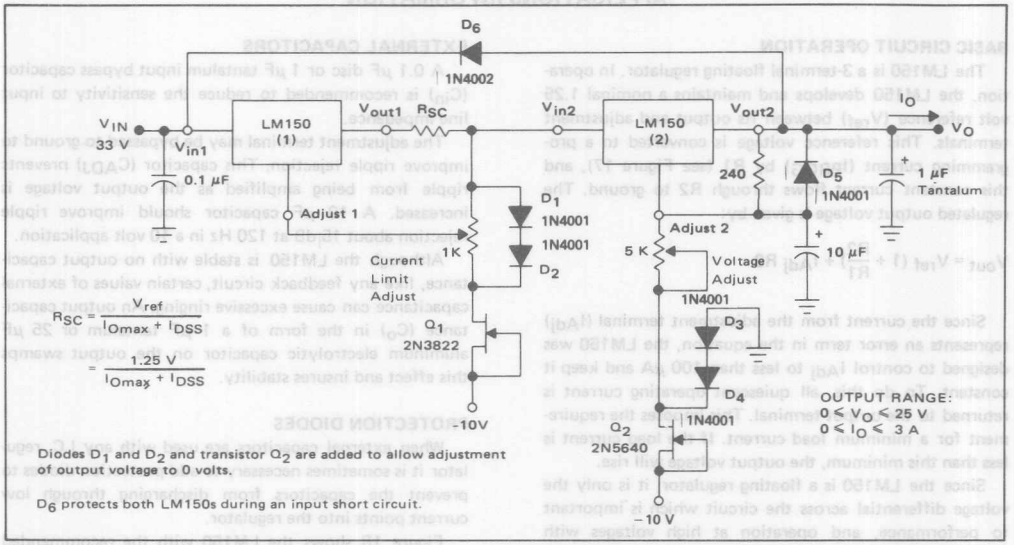


FIGURE 20 – ADJUSTABLE CURRENT LIMITER

FIGURE 21 – 5 V ELECTRONIC SHUT DOWN REGULATOR

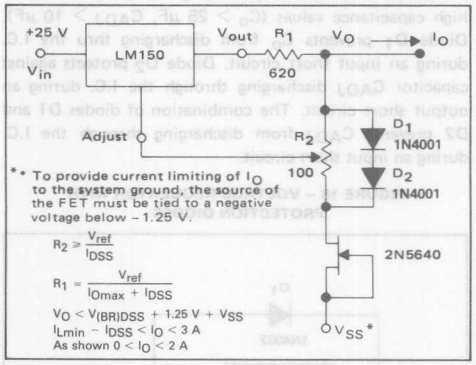


FIGURE 22 – SLOW TURN-ON REGULATOR

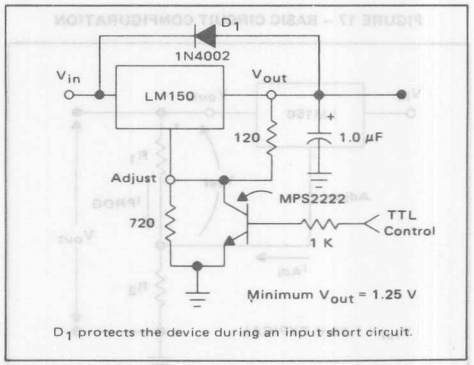
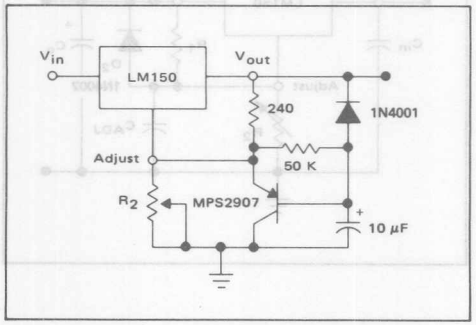
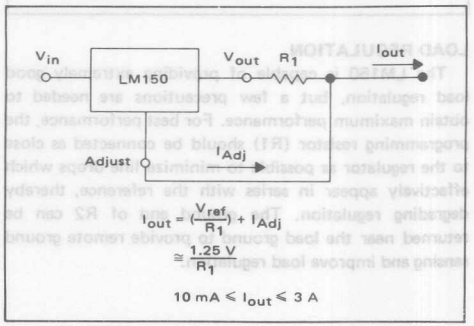


FIGURE 23 – CURRENT REGULATOR





MOTOROLA

LM317M

3

THREE-TERMINAL ADJUSTABLE OUTPUT POSITIVE VOLTAGE REGULATOR

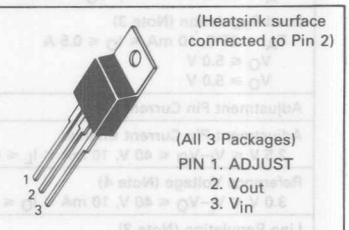
The LM317M is an adjustable 3-terminal positive voltage regulator capable of supplying in excess of 500 mA over an output voltage range of 1.2 V to 37 V. This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, it employs internal current limiting, thermal shutdown and safe area compensation, making it essentially blow-out proof.

The LM317M serves a wide variety of applications including local, on-card regulation. This device also makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM317M can be used as a precision current regulator.

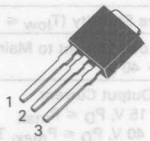
- Output Current in Excess of 500 mA
- Output Adjustable Between 1.2 V and 37 V
- Internal Thermal Overload Protection
- Internal Short-Circuit-Current Limiting
- Output Transistor Safe-Area Compensation
- Floating Operation for High Voltage Applications
- Standard 3-Lead Transistor Packages
- Eliminates Stocking Many Fixed Voltages

MEDIUM-CURRENT THREE-TERMINAL ADJUSTABLE POSITIVE VOLTAGE REGULATOR

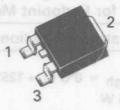
SILICON MONOLITHIC INTEGRATED CIRCUIT



T SUFFIX
PLASTIC PACKAGE
CASE 221A-04

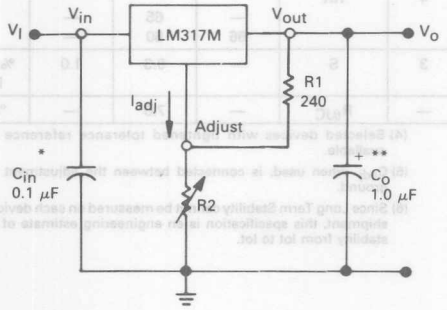


DT-1 SUFFIX
PLASTIC PACKAGE
CASE 369-03
DPAK



DT SUFFIX
PLASTIC PACKAGE
CASE 369A-03
DPAK

STANDARD APPLICATION



*C_{in} is required if regulator is located in appreciable distance from power supply filter.

**C_o is not needed for stability, however it does improve transient response.

$$V_O = 1.25\ V\ (1 + \frac{R_2}{R_1}) + I_{adj}\ R_2$$

Since I_{adj} is controlled to less than 100 μA, the error associated with this term is negligible in most applications.

ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
LM317MT	T_J = 0°C to +125°C	Plastic Power
LM317MBT#	T_J = −40°C to +125°C	Plastic Power

#Automotive temperature range selections are available with special test conditions and additional tests. Contact your local Motorola sales office for information.

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input-Output Voltage Differential	V_I-V_O	40	Vdc
Power Dissipation	P_D	Internally Limited	
Operating Junction Temperature Range	T_J	0 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS

(V_I–V_O = 5.0 V, I_O = 0.1 A, T_J = T_{low} to T_{high} [see Note 1], P_{max} per Note 2, unless otherwise specified.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Line Regulation (Note 3) T_A = 25°C, 3.0 V ≤ V_I–V_O ≤ 40 V	1	Reg_{line}	—	0.01	0.04	%/V
Load Regulation (Note 3) T_A = 25°C, 10 mA ≤ I_O ≤ 0.5 A V_O ≤ 5.0 V V_O ≥ 5.0 V	2	Reg_{load}	 — —	 5.0 0.1	 25 0.5	 mV % V_O
Adjustment Pin Current	3	I_{adj}	—	50	100	μA
Adjustment Pin Current Change 2.5 V ≤ V_I–V_O ≤ 40 V, 10 mA ≤ I_L ≤ 0.5 A, P_D ≤ P_{max}	1,2	ΔI_{adj}	—	0.2	5.0	μA
Reference Voltage (Note 4) 3.0 V ≤ V_I–V_O ≤ 40 V, 10 mA ≤ I_O ≤ 0.5 A, P_D ≤ P_{max}	3	V_{ref}	1.20	1.25	1.30	V
Line Regulation (Note 3) 3.0 V ≤ V_I–V_O ≤ 40 V	1	Reg_{line}	—	0.02	0.07	%/V
Load Regulation (Note 3) 10 mA ≤ I_O ≤ 0.5 A V_O ≤ 5.0 V V_O ≥ 5.0 V	2	Reg_{load}	 — —	 20 0.3	 70 1.5	 mV % V_O
Temperature Stability (T_{low} ≤ T_J ≤ T_{high})	3	T_S	—	0.7	—	% V_O
Minimum Load Current to Maintain Regulation (V_I–V_O = 40 V)	3	I_{Lmin}	—	3.5	10	mA
Maximum Output Current V_I–V_O ≤ 15 V, P_D ≤ P_{max} V_I–V_O = 40 V, P_D ≤ P_{max}, T_A = 25°C	3	I_{max}	 0.5 0.15	 0.9 0.25	 — —	A
RMS Noise, % of V_O T_A = 25°C, 10 Hz ≤ f ≤ 10 kHz	—	N	—	0.003	—	% V_O
Ripple Rejection, V_O = 10 V, f = 120 Hz (Note 5) Without C_{adj} C_{adj} = 10 μF	4	RR	 — 66	 65 80	 — —	dB
Long Term Stability, T_J = T_{high} (Note 6) T_A = 25°C for Endpoint Measurements	3	S	—	0.3	1.0	%/1.0 k Hrs.
Thermal Resistance Junction to Case	—	$R_{\theta JC}$	—	7.0	—	°C/W

NOTES:
(1) T_{low} to T_{high} = 0°C to +125°C
(2) P_{max} = 7.5 W
(3) Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.
(4) Selected devices with tightened tolerance reference voltage available.
(5) C_{adj}, when used, is connected between the adjustment pin and ground.
(6) Since Long Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

SCHEMATIC DIAGRAM

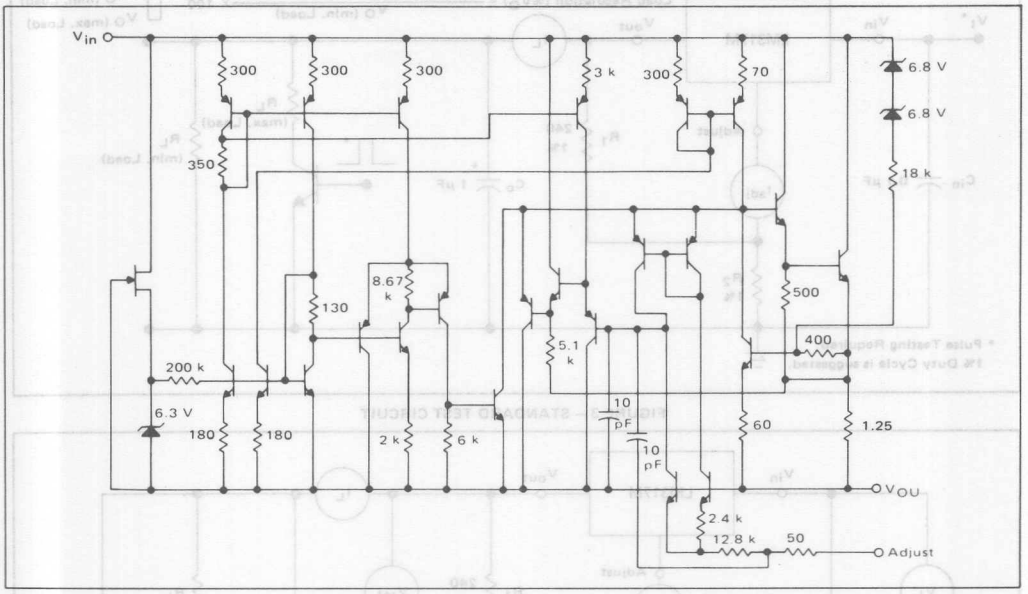
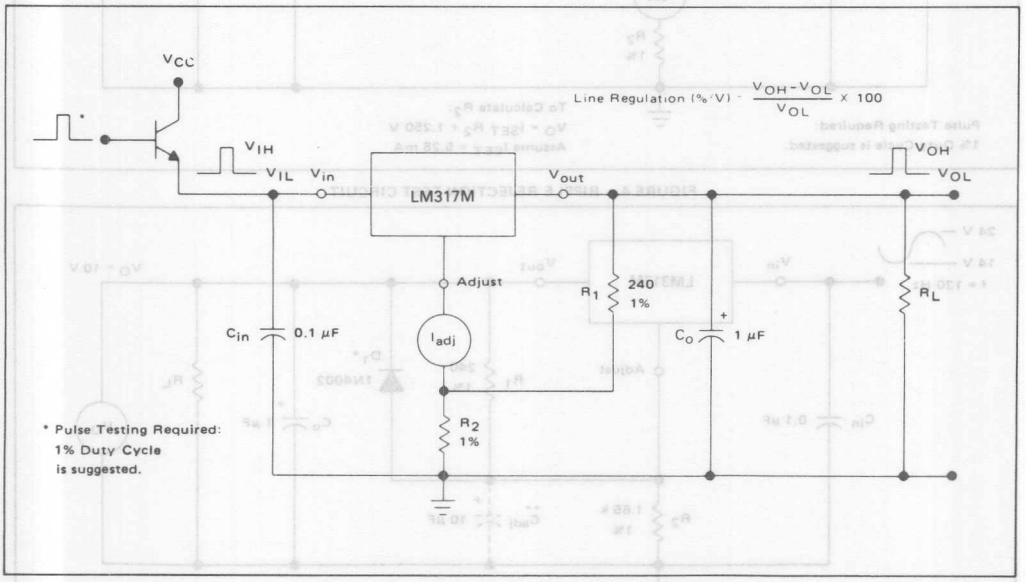


FIGURE 1 – LINE REGULATION AND ΔI_{Adj}/LINE TEST CIRCUIT



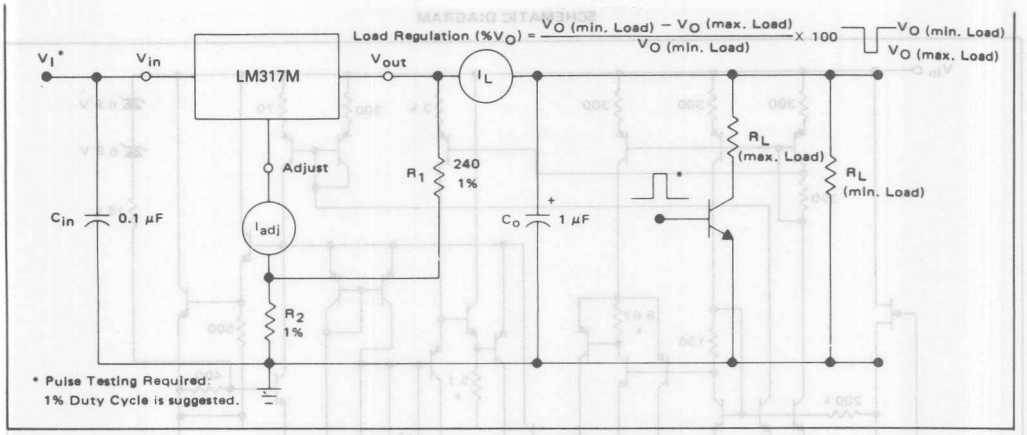


FIGURE 3 – STANDARD TEST CIRCUIT

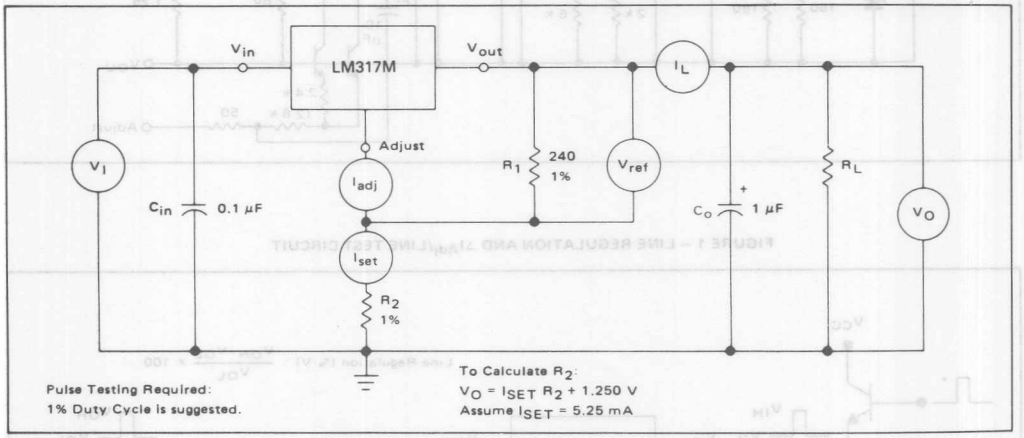


FIGURE 4 – RIPPLE REJECTION TEST CIRCUIT

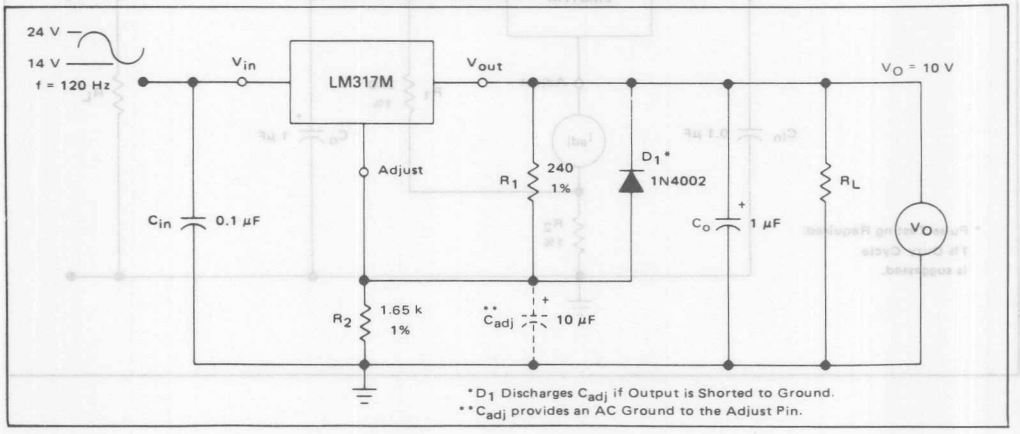


FIGURE 5 – LOAD REGULATION

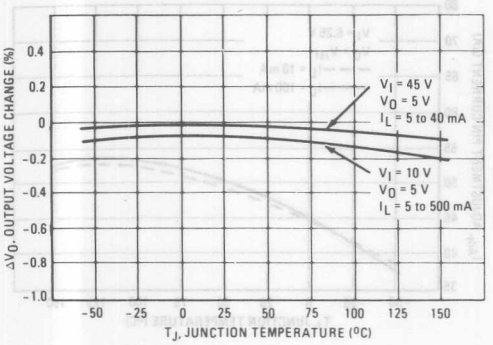


FIGURE 6 – RIPPLE REJECTION

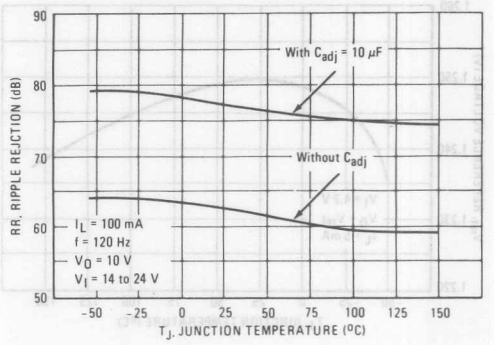


FIGURE 7 – CURRENT LIMIT

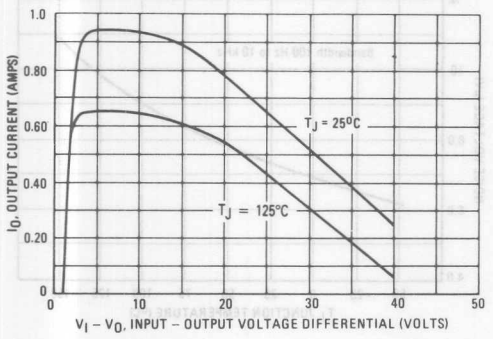


FIGURE 8 – DROPOUT VOLTAGE

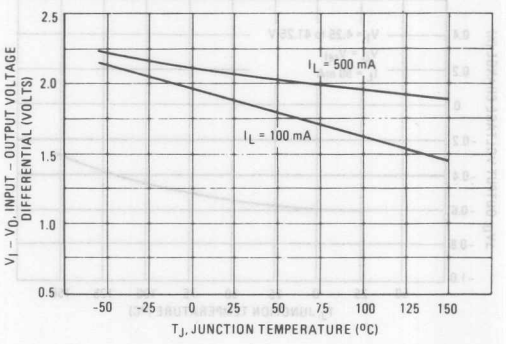


FIGURE 9 – MINIMUM OPERATING CURRENT

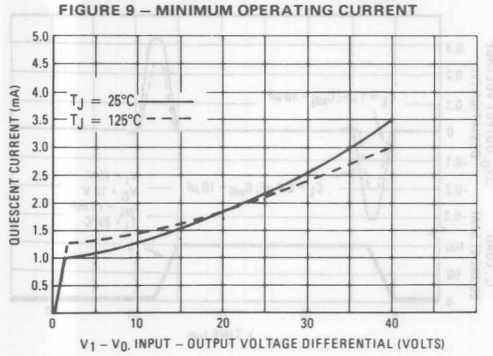


FIGURE 10 – RIPPLE REJECTION versus FREQUENCY

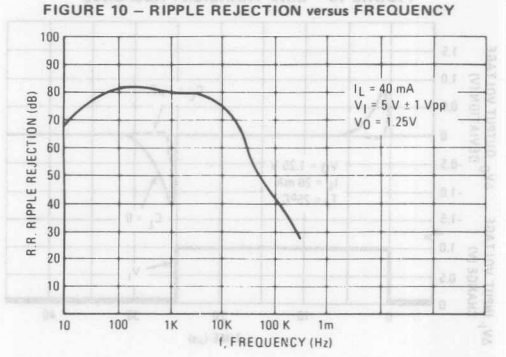


FIGURE 11 – TEMPERATURE STABILITY

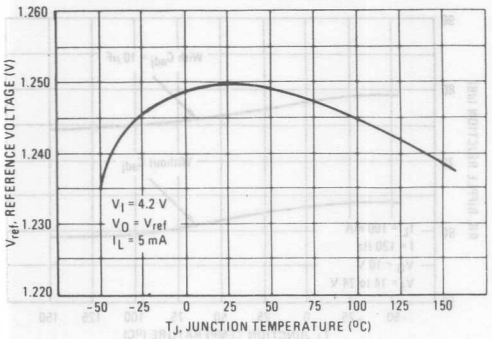


FIGURE 12 – ADJUSTMENT PIN CURRENT

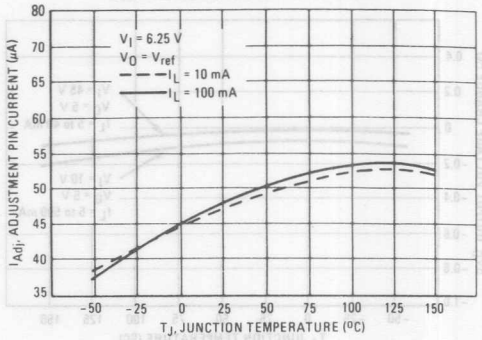


FIGURE 13 – LINE REGULATION

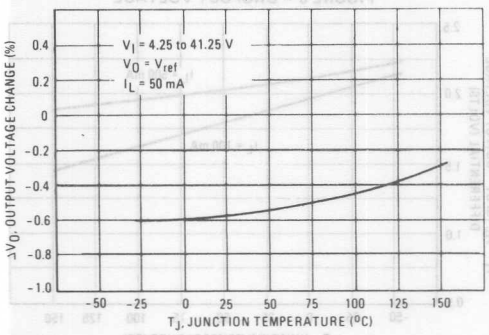


FIGURE 14 – OUTPUT NOISE

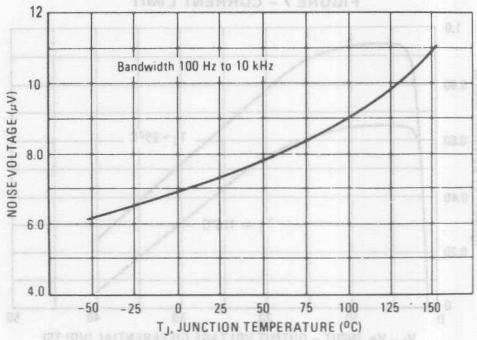


FIGURE 15 – LINE TRANSIENT RESPONSE

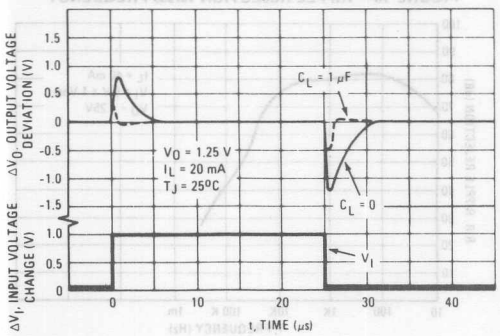
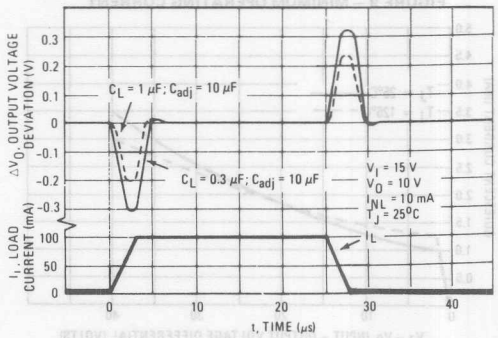


FIGURE 16 – LOAD TRANSIENT RESPONSE



APPLICATIONS INFORMATION

BASIC CIRCUIT OPERATION

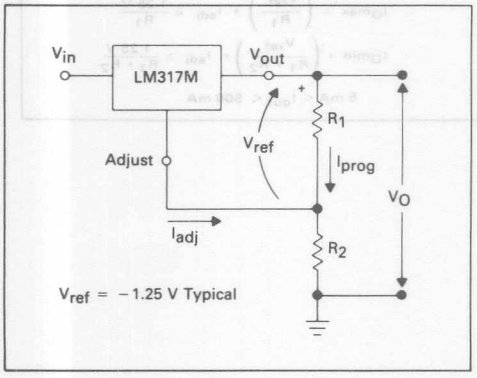
The LM317M is a 3-terminal floating regulator. In operation, the LM317M develops and maintains a nominal 1.25 volt reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{prog}) by R1 (see Figure 17), and this constant current flows through R2 to ground. The regulated output voltage is given by:

$$V_O = V_{ref}\left(1 + \frac{R2}{R1}\right) + I_{adj}R2$$

Since the current from the adjustment terminal (I_{adj}) represents an error term in the equation, the LM317M was designed to control I_{adj} to less than 100 μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM317M is a floating regulator, it is only the voltage differential across the circuit that is important to performance, and operation at high voltages with respect to ground is possible.

FIGURE 17 — BASIC CIRCUIT CONFIGURATION



LOAD REGULATION

The LM317M is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

EXTERNAL CAPACITORS

A 0.1 μF disc or 1 μF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{adj}) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 volt application.

Although the LM317M is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance (C_O) in the form of a 1 μF tantalum or 25 μF aluminum electrolytic capacitor on the output swamps this effect and insures stability.

PROTECTION DIODES

When external capacitors are used with any I.C. regulator it is sometimes necessary to add protection diodes to prevent the capcitors from discharging through low current points into the regulator.

Figure 18 shows the LM317M with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values ($C_O > 25$ μF, $C_{adj} > 5.0$ μF). Diode D1 prevents C_O from discharging thru the I.C. during an input short circuit. Diode D2 protects against capacitor C_{adj} discharging through the I.C. during an output short circuit. The combination of diodes D1 and D2 prevents C_{adj} from discharging through the I.C. during an input short circuit.

FIGURE 18 — VOLTAGE REGULATOR WITH PROTECTION DIODES

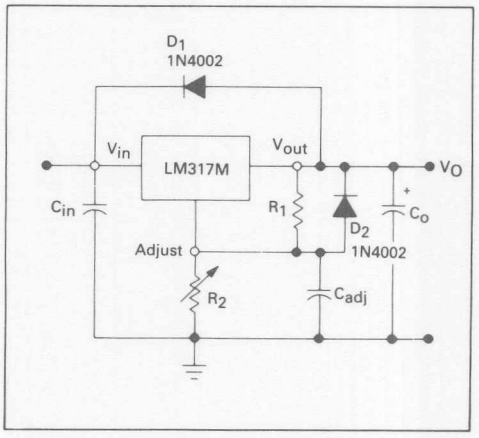


FIGURE 19 – ADJUSTABLE CURRENT LIMITER

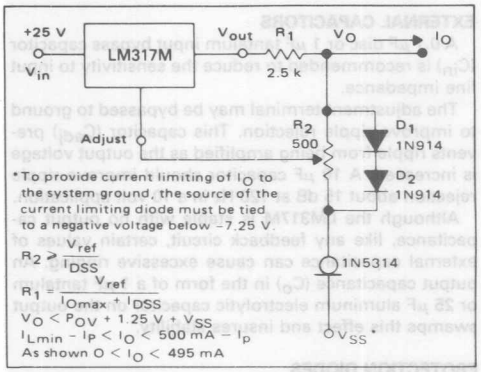


FIGURE 20 – 5 V ELECTRONIC SHUTDOWN REGULATOR

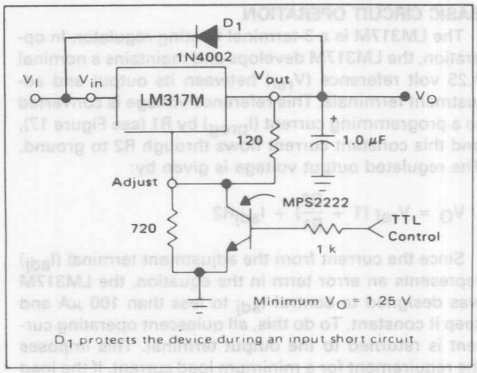


FIGURE 21 – SLOW TURN-ON REGULATOR

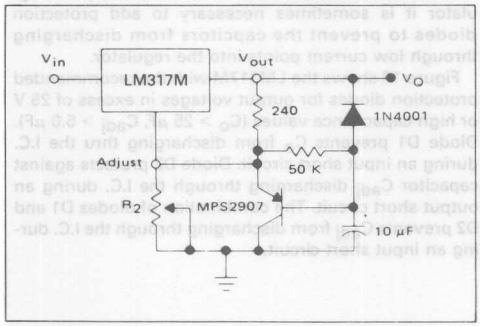
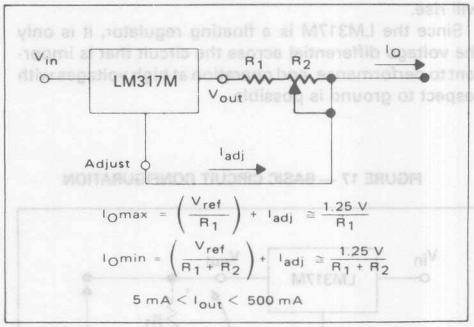


FIGURE 22 – CURRENT REGULATOR



MOTOROLA

LM337M

Specifications and Applications Information

THREE-TERMINAL ADJUSTABLE OUTPUT NEGATIVE VOLTAGE REGULATOR

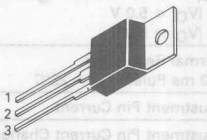
The LM337M is an adjustable 3-terminal negative voltage regulator capable of supplying in excess of 500 mA over an output voltage range of −1.2 V to −37 V. This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, it employs internal current limiting, thermal shutdown and safe area compensation, making it essentially blow-out proof.

The LM337M serves a wide variety of applications including local, on-card regulation. This device can also be used to make a programmable output regulator; or, by connecting a fixed resistor between the adjustment and output, the LM337M can be used as a precision current regulator.

- Output Current in Excess of 500 mA
- Output Adjustable Between −1.2 V and −37 V
- Internal Thermal Overload Protection
- Internal Short-Circuit-Current Limiting
- Output Transistor Safe-Area Compensation
- Floating Operation for High Voltage Applications
- Standard 3-Lead Transistor Packages
- Eliminates Stocking Many Fixed Voltages

MEDIUM-CURRENT THREE-TERMINAL ADJUSTABLE NEGATIVE VOLTAGE REGULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT



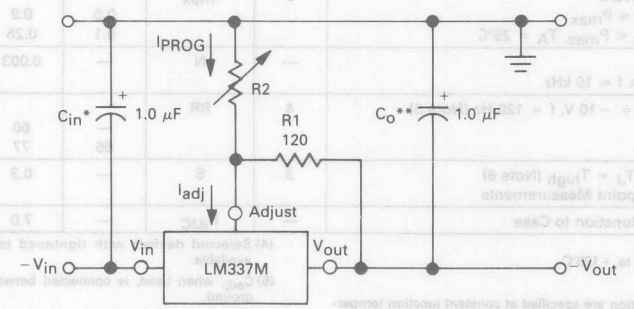
PIN 1. ADJUST
2. V_{in}
3. V_{out}

T SUFFIX
PLASTIC PACKAGE
CASE 221A-04

ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
LM337MT	T_J = 0°C to +125°C	Plastic Power
LM337MBT	T_J = −40°C to +125°C	Plastic Power

STANDARD APPLICATION



*C_{in} is required if regulator is located more than 4 inches from power supply filter. A 1.0 μF solid tantalum or 10 μF aluminum electrolytic is recommended.

**C_o is necessary for stability. A 1.0 μF solid tantalum or 10 μF aluminum electrolytic is recommended.

$$V_{out} = -1.25\ V\left(1 + \frac{R2}{R1}\right)$$

#Automotive temperature range selections are available with special test conditions and additional tests. Contact your local Motorola sales office for information.

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input-Output Voltage Differential	V_I-V_O	40	Vdc
Power Dissipation	P_D	Internally Limited	
Operating Junction Temperature Range	T_J	0 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS ($|V_I-V_O|$ = 5.0 V, I_O = 0.1; T_J = T_{low} to T_{high} [see Note 1], P_{max} per Note 2, unless otherwise specified.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Line Regulation (Note 3) T_A = 25°C, 3.0 V ≤ $\|V_I-V_O\|$ ≤ 40 V	1	Reg_{line}	—	0.01	0.04	%/V
Load Regulation (Note 3) T_A = 25°C, 10 mA ≤ I_O ≤ 0.5 A $\|V_O\|$ ≤ 5.0 V $\|V_O\|$ ≥ 5.0 V	2	Reg_{load}	— —	15 0.3	50 1.0	mV % V_O
Thermal Regulation 10 ms Pulse, T_A = 25°C	—	Reg_{therm}	—	0.03	0.04	%V_O/W
Adjustment Pin Current	3	I_{adj}	—	65	100	μA
Adjustment Pin Current Change 2.5 V ≤ $\|V_I-V_O\|$ ≤ 40 V, 10 mA ≤ I_L ≤ 0.5 A, P_D ≤ P_{max}, T_A = 25°C	1,2	ΔI_{adj}	—	2.0	5.0	μA
Reference Voltage (Note 4) 3.0 V ≤ $\|V_I-V_O\|$ ≤ 40 V, 10 mA ≤ I_O ≤ 0.5 A, P_D ≤ P_{max}, T_A = 25°C T_{low} to T_{high}	3	V_{ref}	 −1.213 −1.20	 −1.250 −1.25	 −1.287 −1.30	V
Line Regulation (Note 3) 3.0 V ≤ $\|V_I-V_O\|$ ≤ 40 V	1	Reg_{line}	—	0.02	0.07	% V
Load Regulation (Note 3) 10 mA ≤ I_O ≤ 0.5 A $\|V_O\|$ ≤ 5.0 V $\|V_O\|$ ≥ 5.0 V	2	Reg_{load}	 — —	 20 0.3	 70 1.5	 mV % V_O
Temperature Stability (T_{low} ≤ T_J ≤ T_{high})	3	T_S	—	0.6	—	% V_O
Minimum Load Current to Maintain Regulation ($\|V_I-V_O\|$ ≤ 10 V) ($\|V_I-V_O\|$ ≤ 40 V)	3	I_{Lmin}	 — —	 1.5 2.5	 6.0 10	mA
Maximum Output Current $\|V_I-V_O\|$ ≤ 15 V, P_D ≤ P_{max} $\|V_I-V_O\|$ = 40 V, P_D ≤ P_{max}, T_A = 25°C	3	I_{max}	 0.5 0.1	 0.9 0.25	 — —	A
RMS Noise, % of V_O T_A = 25°C, 10 Hz ≤ f ≤ 10 kHz	—	N	—	0.003	—	% V_O
Ripple Rejection, V_O = −10 V, f = 120 Hz (Note 5) Without C_{adj} C_{adj} = 10 μF	4	RR	 — 66	 60 77	 — —	dB
Long Term Stability, T_J = T_{high} (Note 6) T_A = 25°C for Endpoint Measurements	3	S	—	0.3	1.0	%, 1.0 k Hrs.
Thermal Resistance Junction to Case	—	$R_{\theta JC}$	—	7.0	—	°C/W

NOTES:
(1) T_{low} to T_{high} = 0°C to +125°C
(2) P_{max} = 7.5 W
(3) Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.
(4) Selected devices with tightened tolerance reference voltage available.
(5) C_{adj}, when used, is connected between the adjustment pin and ground.
(6) Since Long Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

SCHEMATIC DIAGRAM

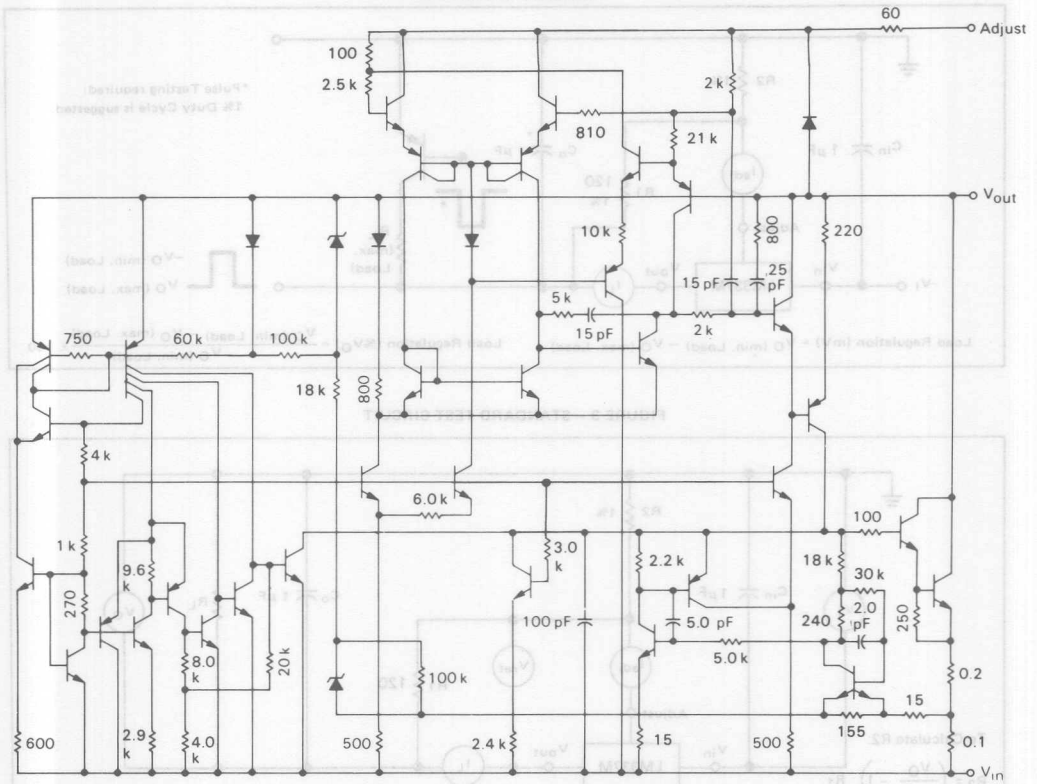
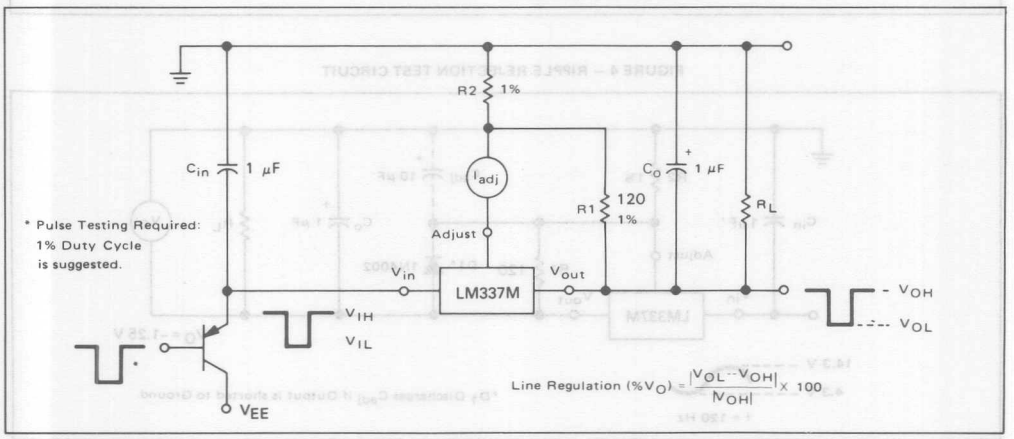


FIGURE 1 – LINE REGULATION AND ΔI_{adj}/LINE TEST CIRCUIT



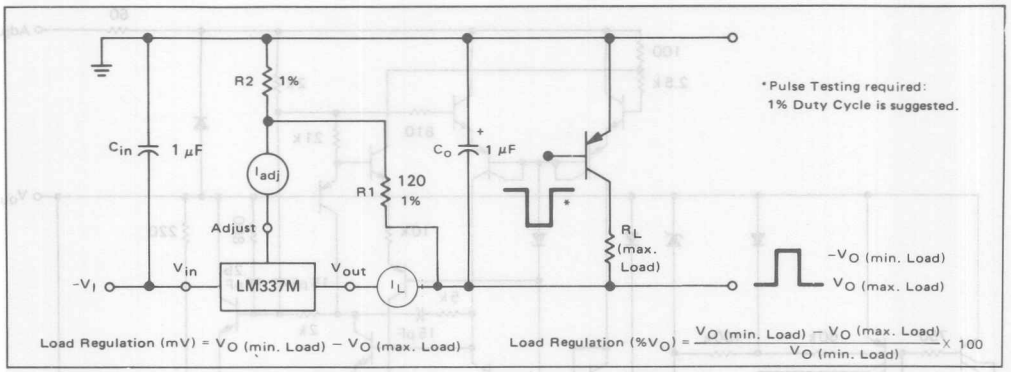


FIGURE 3 – STANDARD TEST CIRCUIT

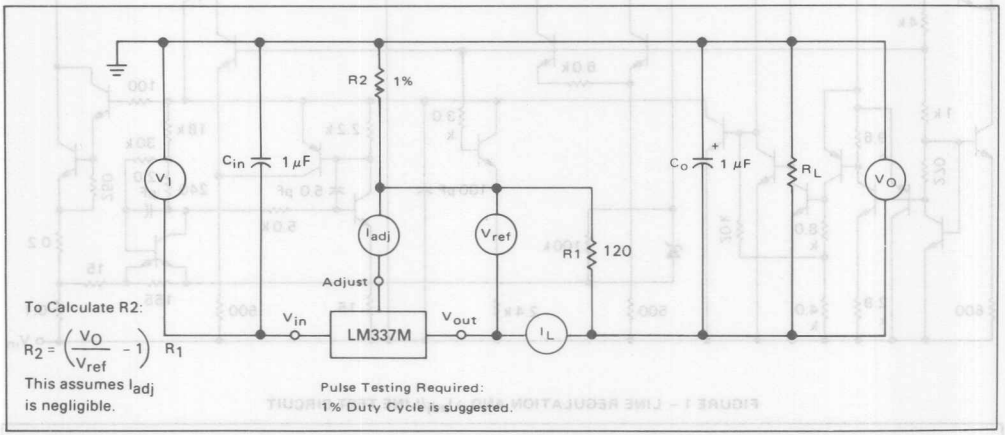


FIGURE 4 – RIPPLE REJECTION TEST CIRCUIT

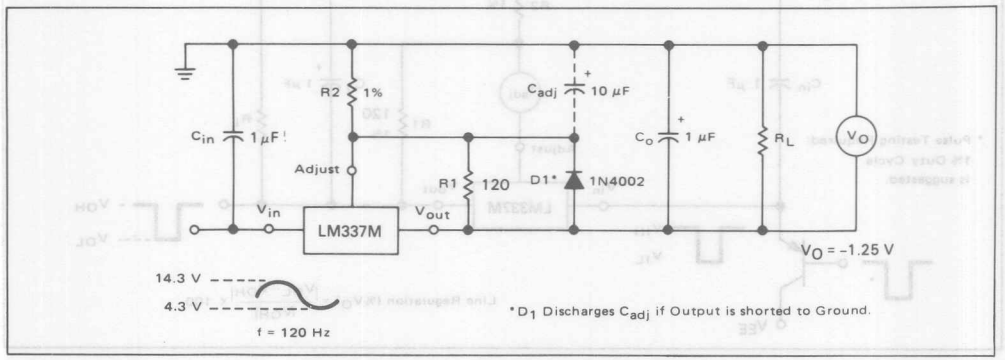


FIGURE 5 – LOAD REGULATION

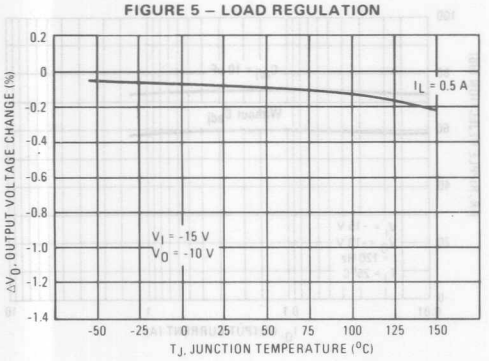


FIGURE 6 – CURRENT LIMIT

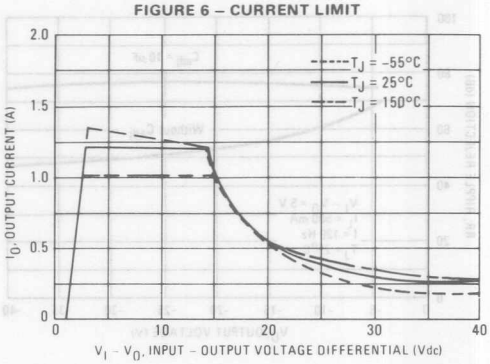


FIGURE 7 – ADJUSTMENT PIN CURRENT

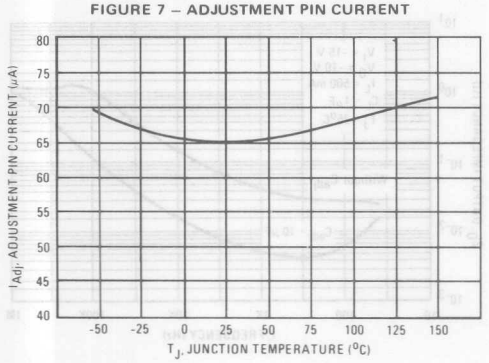


FIGURE 8 – DROPOUT VOLTAGE

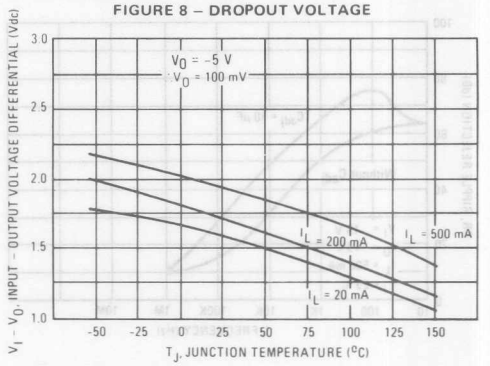


FIGURE 9 – TEMPERATURE STABILITY

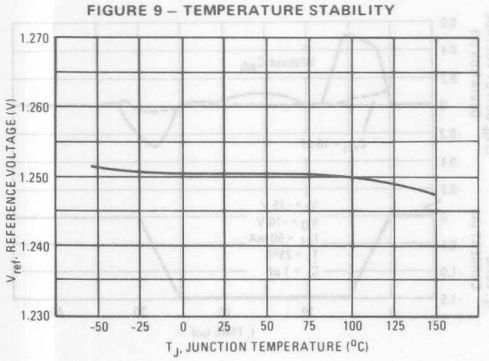
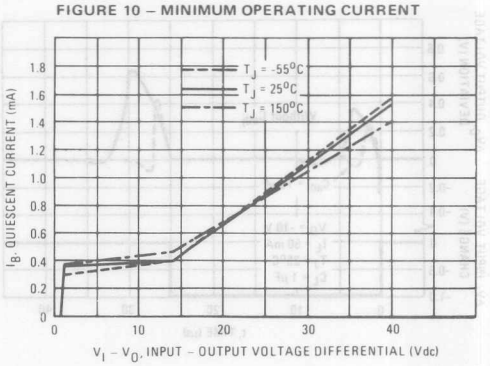


FIGURE 10 – MINIMUM OPERATING CURRENT



3

FIGURE 11 — RIPPLE REJECTION versus OUTPUT VOLTAGE

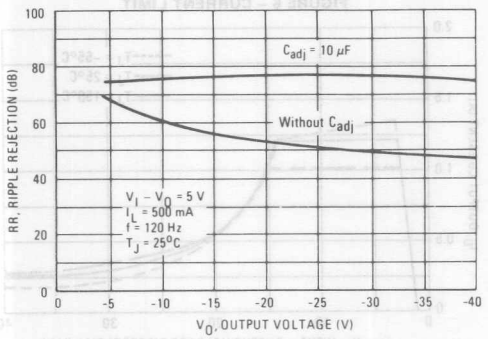


FIGURE 12 — RIPPLE REJECTION versus OUTPUT CURRENT

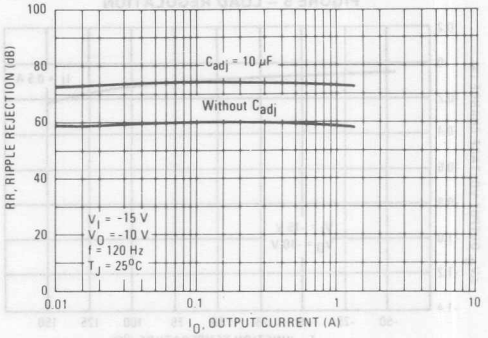


FIGURE 13 — RIPPLE REJECTION versus FREQUENCY

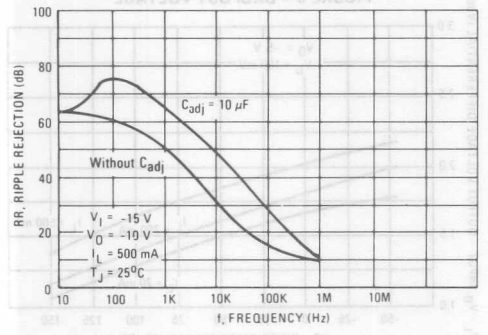


FIGURE 14 — OUTPUT IMPEDANCE

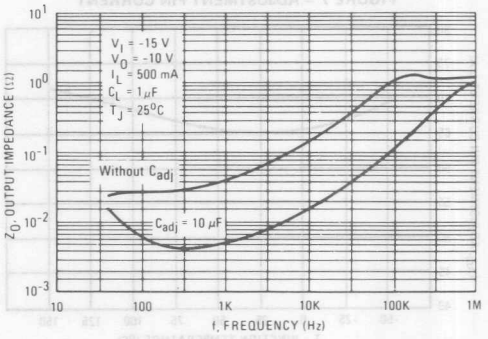


FIGURE 15 — LINE TRANSIENT RESPONSE

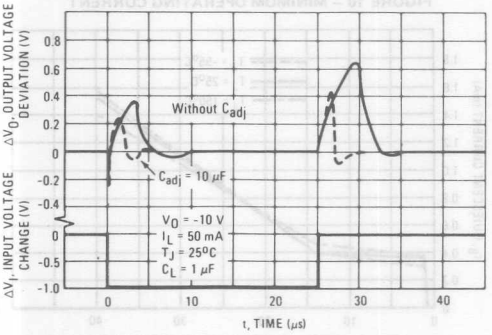
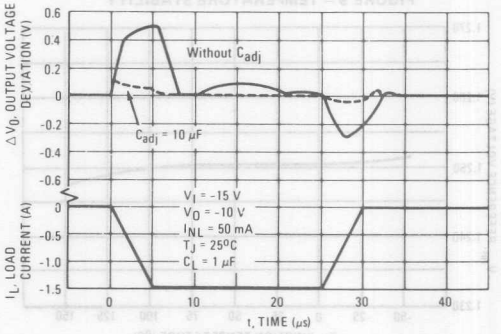


FIGURE 16 — LOAD TRANSIENT RESPONSE



APPLICATIONS INFORMATION

BASIC CIRCUIT OPERATION

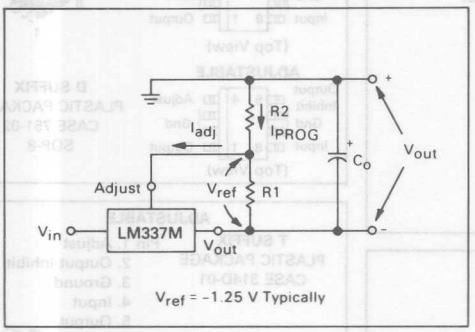
The LM337M is a 3-terminal floating regulator. In operation, the LM337M develops and maintains a nominal −1.25 volt reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by R1 (see Figure 17), and this constant current flows through R2 from ground. The regulated output voltage is given by:

$$V_{out} = V_{ref}\left(1 + \frac{R2}{R1}\right) + I_{adj}R2$$

Since the current into the adjustment terminal (I_{adj}) represents an error term in the equation, the LM337M was designed to control I_{adj} to less than 100 μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will increase.

Since the LM337M is a floating regulator, it is only the voltage differential across the circuit that is important to performance, and operation at high voltages with respect to ground is possible.

FIGURE 17— BASIC CIRCUIT CONFIGURATION



LOAD REGULATION

The LM337M is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

EXTERNAL CAPACITORS

A 1.0 μF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{adj}) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 volt application.

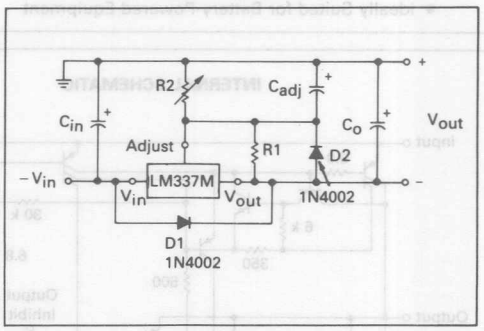
An output capacitor (C_o) in the form of a 1.0 μF tantalum or 10 μF aluminum electrolytic capacitor is required for stability.

PROTECTION DIODES

When external capacitors are used with any I.C. regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 18 shows the LM337M with the recommended protection diodes for output voltages in excess of −25 V or high capacitance values (C_o > 25 μF, C_{adj} > 10 μF). Diode D_1 prevents C_o from discharging thru the I.C. during an input short circuit. Diode D_2 protects against capacitor C_{adj} discharging through the I.C. during an output short circuit. The combination of diodes D1 and D2 prevents C_{adj} from discharging through the I.C. during an input short circuit.

FIGURE 18— VOLTAGE REGULATOR WITH PROTECTION DIODES



3

LOW DROPOUT VOLTAGE REGULATORS

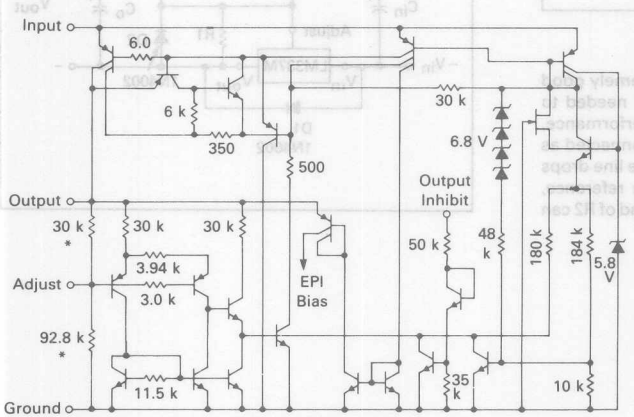
The LM2931 series consists of positive fixed and adjustable output voltage regulators that are specifically designed to maintain proper regulation with an extremely low input-to-output voltage differential. These devices are capable of supplying output currents in excess of 100 mA and feature a low bias current of 0.4 mA at 10 mA output.

Designed primarily to survive in the harsh automotive environment, these devices will protect all external load circuitry from input fault conditions caused by reverse battery connection, two battery jump starts, and excessive line transients during load dump. This series also includes internal current limiting, thermal shutdown, and additionally, is able to withstand temporary power-up with mirror-image insertion.

Due to the low dropout voltage and bias current specifications, the LM2931 series is ideally suited for battery powered industrial and consumer equipment where an extension of useful battery life is desirable. The 'C' suffix adjustable output regulators feature an output inhibit pin which is extremely useful in microprocessor-based systems.

- Input-to-Output Voltage Differential of Less Than 0.6 V at 100 mA
- Output Current in Excess of 100 mA
- Low Bias Current
- 60 V Load Dump Protection
- −50 V Reverse Transient Protection
- Internal Current Limiting with Thermal Shutdown
- Temporary Mirror-Image Protection
- Ideally Suited for Battery-Powered Equipment

INTERNAL SCHEMATIC



*Deleted on Adjustable Regulators

LOW DROPOUT VOLTAGE REGULATORS

SILICON MONOLITHIC INTEGRATED CIRCUITS

Z SUFFIX
PLASTIC PACKAGE
CASE 29-04

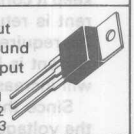
Pin 1. Output
2. Ground
3. Input



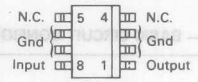
T SUFFIX
PLASTIC PACKAGE
CASE 221A-04

Pin 1. Input
2. Ground
3. Output

(Heatsink surface connected to Pin 2)



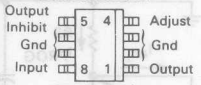
FIXED



(Top View)



ADJUSTABLE



(Top View)

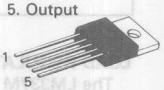
D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SOP-8

ADJUSTABLE

T SUFFIX
PLASTIC PACKAGE
CASE 314D-01

Pin 1. Adjust
2. Output Inhibit
3. Ground
4. Input
5. Output

(Heatsink surface connected to Pin 3)



ORDERING INFORMATION

Device	Output Voltage	Output Tolerance	Package Case Number
LM2931AD-5.0	5.0 V	±2.5%	751
LM2931AT-5.0	5.0 V	±2.5%	221A-02
LM2931AZ-5.0	5.0 V	±2.5%	29-02
LM2931D-5.0	5.0 V	±5.0%	751
LM2931T-5.0	5.0 V	±5.0%	221A-02
LM2931Z-5.0	5.0 V	±5.0%	29-02
LM2931ACD	Adjustable	±2.5%	751
LM2931ACT	Adjustable	±2.5%	314D-01
LM2931CD	Adjustable	±5.0%	751
LM2931CT	Adjustable	±5.0%	314D-01

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage Continuous	V_{in}	40	Vdc
Transient Input Voltage ($\tau \leq 100$ ms)	$V_{in(\tau)}$	60	V_{pk}
Transient Reverse Polarity Input Voltage 1.0% Duty Cycle, $\tau \leq 100$ ms	$-V_{in(\tau)}$	−50	V_{pk}
Power Dissipation			
Case 29-04 (TO-92)			
T_A = 25°C	P_D	Internally Limited	Watts
Thermal Resistance Junction to Ambient	θ_{JA}	178	°C/W
Thermal Resistance Junction to Case	θ_{JC}	83	°C/W
Case 751-02 (SOP-8)			
T_A = 25°C	P_D	Internally Limited	Watts
Thermal Resistance Junction to Ambient	θ_{JA}	180	°C/W
Thermal Resistance Junction to Case	θ_{JC}	45	°C/W
Case 221A-03 and 314D-01 (TO-220 Type)			
T_A = 25°C	P_D	Internally Limited	Watts
Thermal Resistance Junction to Ambient	θ_{JA}	65	°C/W
Thermal Resistance Junction to Case	θ_{JC}	5.0	°C/W
Junction Temperature Range	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{in} = 14 V, I_O = 10 mA, C_O = 100 μF, $C_{O(ESR)}$ = 0.3 Ω, T_J = 25°C, Note 1, unless otherwise noted.)

Characteristic	Symbol	LM2931A-5.0 Min	LM2931A-5.0 Typ	LM2931A-5.0 Max	LM2931-5.0 Min	LM2931-5.0 Typ	LM2931-5.0 Max	Unit
FIXED OUTPUT								
Output Voltage	V_O							V
V_{in} = 14 V, I_O = 10 mA, T_J = 25°C		4.875	5.0	5.125	4.75	5.0	5.25	
V_{in} = 6.0 V to 26 V, $I_O \leq$ 100 mA, T_J = −40 to 125°C		4.75	—	5.25	4.50	—	5.50	
Line Regulation	Reg_{line}							mV
V_{in} = 9.0 V to 16 V		—	2.0	10	—	2.0	10	
V_{in} = 6.0 V to 26 V		—	4.0	30	—	4.0	30	
Load Regulation (I_O = 5.0 mA to 100 mA)	Reg_{load}	—	14	50	—	14	50	mV
Output Impedance I_O = 10 mA, ΔI_O = 1.0 mA, f = 100 Hz to 10 kHz	Z_O	—	200	—	—	200	—	mΩ
Bias Current	I_B							mA
V_{in} = 14 V, I_O = 100 mA, T_J = 25°C		—	5.8	30	—	5.8	30	
V_{in} = 6.0 V to 26 V, I_O = 10 mA, T_J = −40 to 125°C		—	0.4	1.0	—	0.4	1.0	
Output Noise Voltage (f = 10 Hz to 100 kHz)	V_n	—	700	—	—	700	—	μVrms
Long-Term Stability	S	—	20	—	—	20	—	mV/ kHR
Ripple Rejection (f = 120 Hz)	RR	60	90	—	60	90	—	dB
Dropout Voltage	V_{in}-V_O							V
I_O = 10 mA		—	0.015	0.2	—	0.015	0.2	
I_O = 100 mA		—	0.16	0.6	—	0.16	0.6	
Over-Voltage Shutdown Threshold	$V_{th(OV)}$	26	29.5	40	26	29.5	40	V
Output Voltage with Reverse Polarity Input (V_{in} = −15 V)	$-V_O$	−0.3	0	—	−0.3	0	—	V

NOTES:
1) Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
2) The reference voltage on the adjustable device is measured from the output to the adjust pin across R_1.

ELECTRICAL CHARACTERISTICS (V_{in} = 14 V, V_O = 3.0 V, I_O = 10 mA, R_1 = 27 k, C_O = 100 μF, $C_{O(ESR)}$ = 0.3 Ω, T_J = 25°C, Note 1, unless otherwise noted.)

Characteristic	Symbol	LM2931AC Min	LM2931AC Typ	LM2931AC Max	LM2931C Min	LM2931C Typ	LM2931C Max	Unit
ADJUSTABLE OUTPUT								
Reference Voltage (Note 2, Figure 18) I_O = 10 mA, T_J = 25°C $I_O \leq$ 100 mA, T_J = −40 to 125°C	V_{ref}	 1.17 1.14	 1.20 —	 1.23 1.26	 1.14 1.08	 1.20 —	 1.26 1.32	V
Output Voltage Range	V_{Orange}	3.0	2.7 to 29.5	24	3.0	2.7 to 29.5	24	V
Line Regulation (V_{in} = V_O + 0.6 V to 26 V)	Reg_{line}	—	0.2	1.5	—	0.2	1.5	mV/V
Load Regulation (I_O = 5.0 mA to 100 mA)	Reg_{load}	—	0.3	1.0	—	0.3	1.0	%/V
Output Impedance I_O = 10 mA, ΔI_O = 1.0 mA, f = 10 Hz to 10 kHz	Z_O	—	40	—	—	40	—	mΩ/V
Bias Current I_O = 100 mA I_O = 10 mA Output Inhibited ($V_{th(OI)}$ = 2.5 V)	I_B	 — — —	 6.0 0.4 0.2	 — 1.0 1.0	 — — —	 6.0 0.4 0.2	 — 1.0 1.0	mA
Adjustment Pin Current	I_{Adj}	—	0.2	—	—	0.2	—	μA
Output Noise Voltage (f = 10 Hz to 100 kHz)	V_n	—	140	—	—	140	—	μVrms/V
Long-Term Stability	S	—	0.4	—	—	0.4	—	%/kHR
Ripple Rejection (f = 120 Hz)	RR	0.10	0.003	—	0.10	0.003	—	%/V
Dropout Voltage I_O = 10 mA I_O = 100 mA	V_{in}-V_O	 — —	 0.015 0.16	 0.2 0.6	 — —	 0.015 0.16	 0.2 0.6	V
Over-Voltage Shutdown Threshold	$V_{th(OV)}$	26	29.5	40	26	29.5	40	V
Output Voltage with Reverse Polarity Input (V_{in} = −15 V)	$-V_O$	−0.3	0	—	−0.3	0	—	V
Output Inhibit Threshold Voltages Output "On," T_J = 25°C T_J = −40 to 125°C Output "Off," T_J = 25°C T_J = −40 to 125°C	$V_{th(OI)}$	 — — 2.50 3.25	 2.15 — 2.26 —	 1.90 1.20 — —	 — — 2.50 3.25	 2.15 — 2.26 —	 1.90 1.20 — —	V
Output Inhibit Threshold Current ($V_{th(OI)}$ = 2.5 V)	$I_{th(OI)}$	—	30	50	—	30	50	μA

DEFINITIONS

Dropout Voltage — The input/output voltage differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output decreases 100 mV from nominal value at 14 V input, dropout voltage is affected by junction temperature and load current.

Line Regulation — The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation — The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation — The maximum total device dissipation for which the regulator will operate within specifications.

Bias Current — That part of the input current that is not delivered to the load.

Output Noise Voltage — The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long-Term Stability — Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices electrical characteristics and maximum power dissipation.

FIGURE 1 — DROPOUT VOLTAGE versus OUTPUT CURRENT

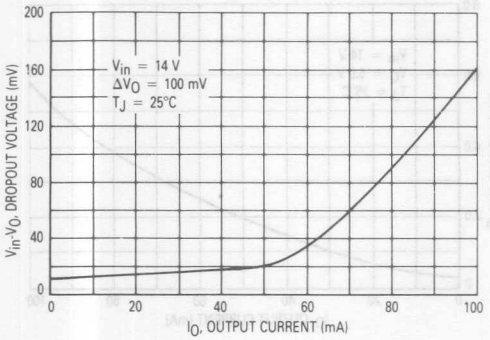


FIGURE 2 — DROPOUT VOLTAGE versus JUNCTION TEMPERATURE

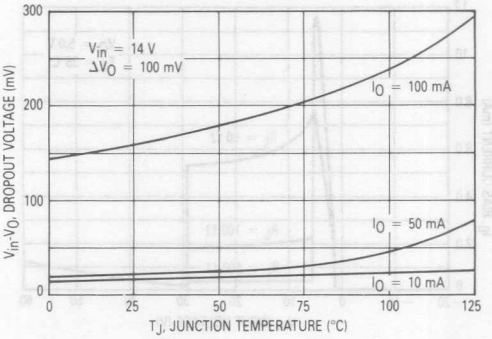


FIGURE 3 — PEAK OUTPUT CURRENT versus INPUT VOLTAGE

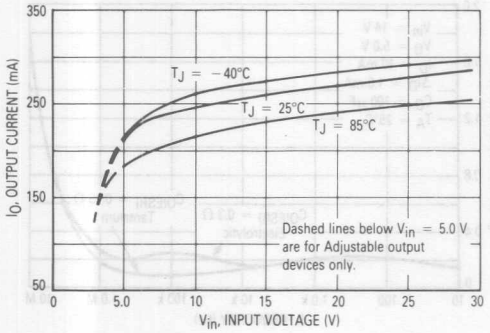


FIGURE 4 — OUTPUT VOLTAGE versus INPUT VOLTAGE

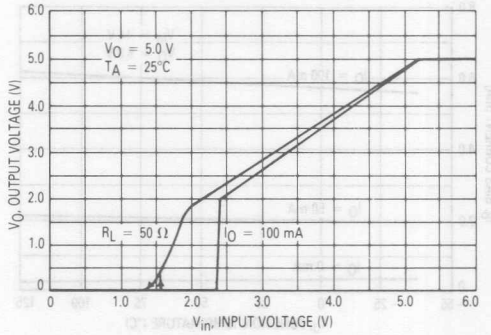


FIGURE 5 — OUTPUT VOLTAGE versus INPUT VOLTAGE

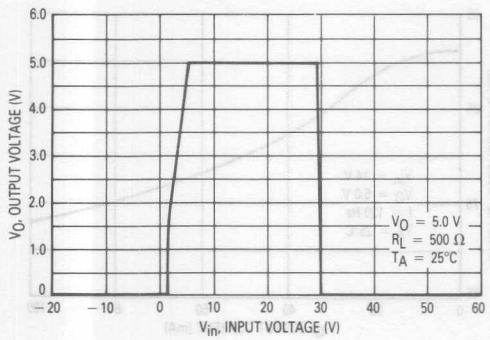


FIGURE 6 — LOAD DUMP CHARACTERISTICS

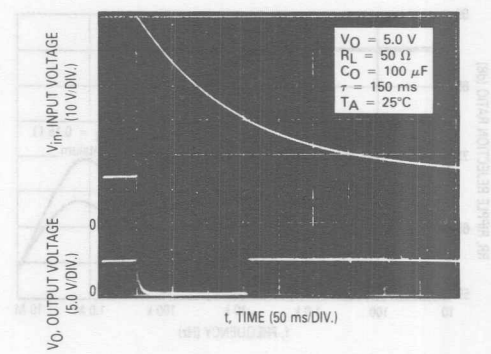


FIGURE 7 — BIAS CURRENT versus INPUT VOLTAGE

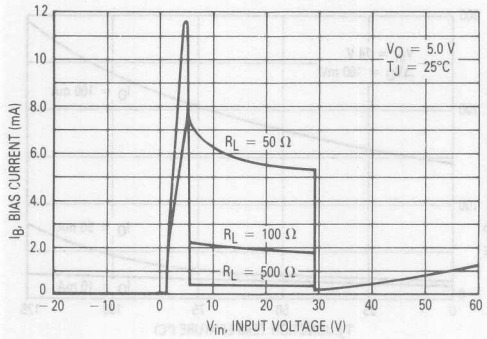


FIGURE 8 — BIAS CURRENT versus OUTPUT CURRENT

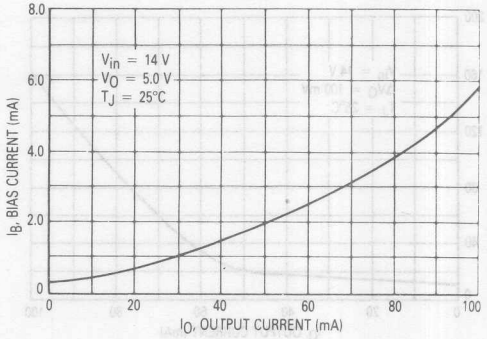


FIGURE 9 — BIAS CURRENT versus JUNCTION TEMPERATURE

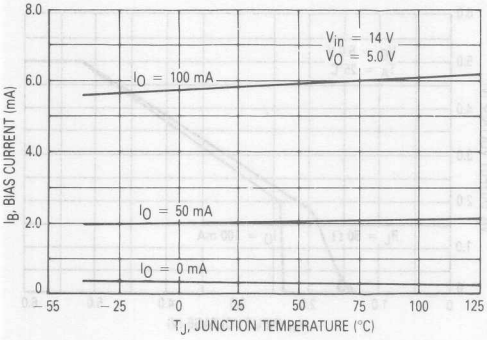


FIGURE 10 — OUTPUT IMPEDANCE versus FREQUENCY

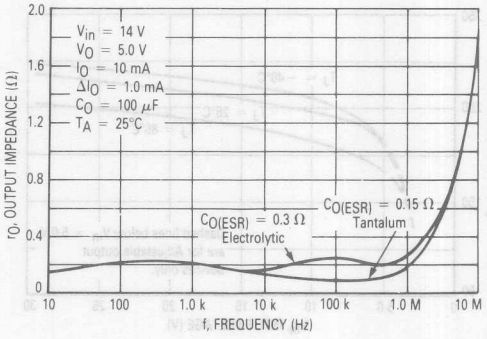


FIGURE 11 — RIPPLE REJECTION versus FREQUENCY

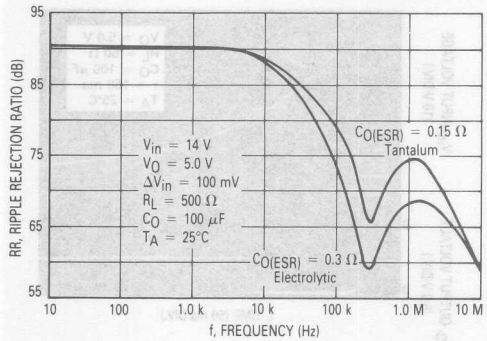


FIGURE 12 — RIPPLE REJECTION versus OUTPUT CURRENT

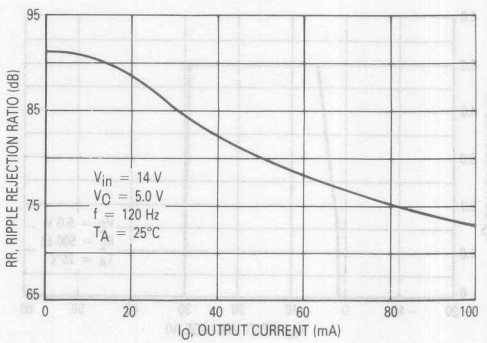


FIGURE 13 — LINE REGULATION

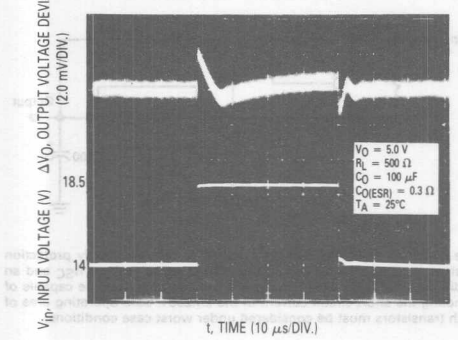


FIGURE 14 — LOAD REGULATION

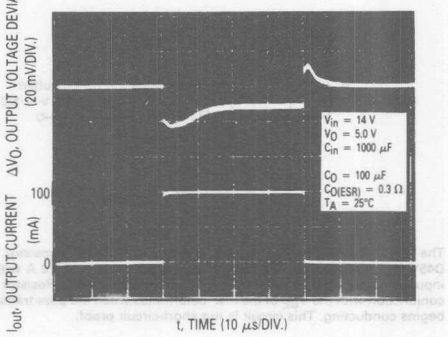


FIGURE 15 — REFERENCE VOLTAGE versus OUTPUT VOLTAGE

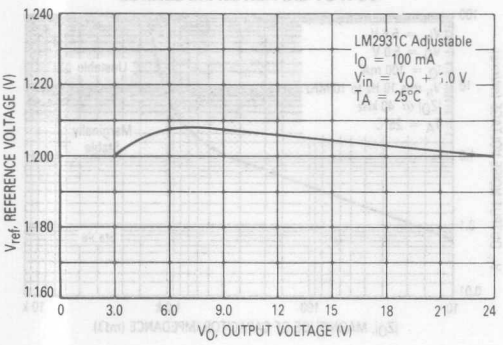
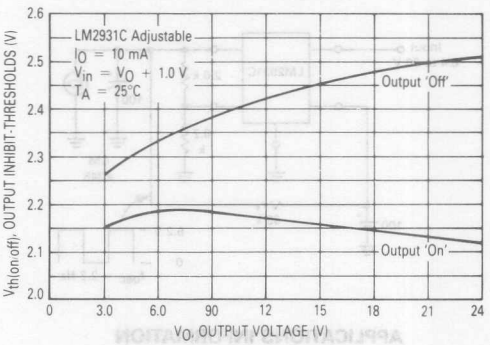


FIGURE 16 — OUTPUT INHIBIT-THRESHOLDS versus OUTPUT VOLTAGE



TYPICAL APPLICATIONS

FIGURE 17 — FIXED OUTPUT REGULATOR

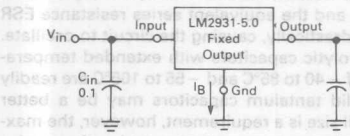
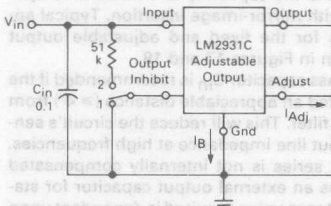


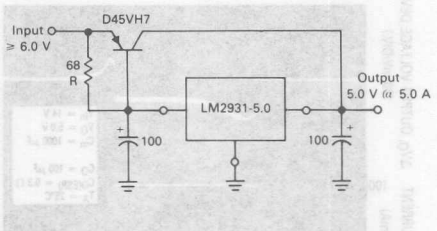
FIGURE 18 — ADJUSTABLE OUTPUT REGULATOR



Switch Position 1 = Output 'On,' 2 = Output 'Off'

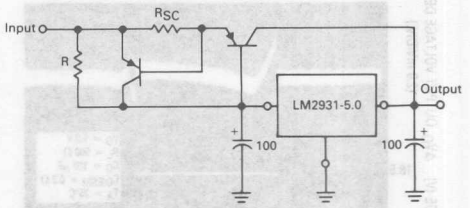
$$V_O = V_{ref}\left(1 + \frac{R2}{R1}\right) + I_{Adj}\,R2 \qquad 22.5\ k \geq \frac{R1\ R2}{R1 + R2}$$

FIGURE 19 — 5.0 A LOW DIFFERENTIAL VOLTAGE REGULATOR



The LM2931 series can be current boosted with a PNP transistor. The D45VH7, on a heatsink, will provide an output current of 5.0 A with an input to output voltage differential of approximately 1.0 V. Resistor R in conjunction with the V_{BE} of the PNP determines when the pass transistor begins conducting. This circuit is not short-circuit proof.

FIGURE 20 — CURRENT BOOST REGULATOR WITH SHORT-CIRCUIT PROJECTION



The circuit of Figure 19 can be modified to provide supply protection against short circuits by adding the current sense resistor R_{SC} and an additional PNP transistor. The current sensing PNP must be capable of handling the short-circuit current of the LM2931. Safe operating area of both transistors must be considered under worst case conditions.

FIGURE 21 — CONSTANT INTENSITY LAMP FLASHER

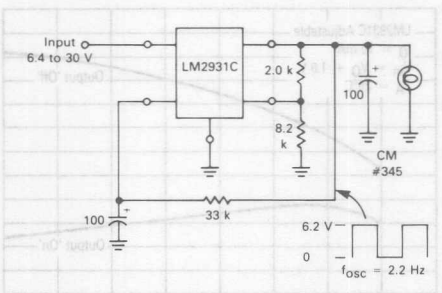
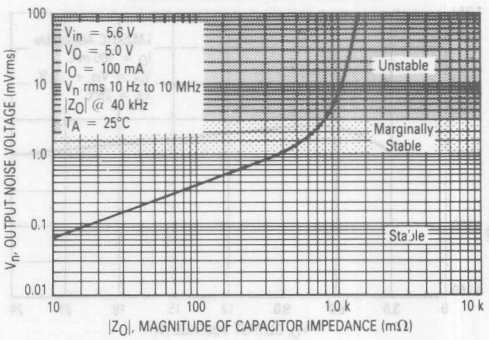


FIGURE 22 — OUTPUT NOISE VOLTAGE versus OUTPUT CAPACITOR IMPEDANCE



APPLICATIONS INFORMATION

The LM2931 series regulators are designed with many protection features making them essentially blow-out proof. These features include internal current limiting, thermal shutdown, overvoltage and reverse polarity input protection, and the capability to withstand temporary power-up with mirror-image insertion. Typical application circuits for the fixed and adjustable output device are shown in Figures 17 and 18.

The input bypass capacitor C_{in} is recommended if the regulator is located an appreciable distance (≥ 4") from the supply input filter. This will reduce the circuit's sensitivity to the input line impedance at high frequencies.

This regulator series is not internally compensated and thus requires an external output capacitor for stability. The capacitance value required is dependent upon the load current, output voltage for the adjustable regulator, and the type of capacitor selected. The least-stable condition is encountered at maximum load current and minimum output voltage. Figure 22 shows that for operation in the "Stable" region, under the conditions specified, the magnitude of the output capacitor impedance $|Z_O|$ must not exceed 0.4 Ω. This limit must be observed over the entire operating temperature range of the regulator circuit.

With economical electrolytic capacitors, cold temperature operation can pose a serious stability problem. As the electrolyte freezes, around −30°C, the capacitance will decrease and the equivalent series resistance ESR will increase drastically, causing the circuit to oscillate. Quality electrolytic capacitors with extended temperature ranges of −40 to 85°C and −55 to 105°C are readily available. Solid tantalum capacitors may be a better choice if small size is a requirement, however, the maximum $|Z_O|$ limit over temperature must be observed.

Note that in the stable region, the output noise voltage is linearly proportional to $|Z_O|$. In effect, C_O dictates the high frequency roll-off point of the circuit. Operation in the area titled "Marginally Stable" will cause the output of the regulator to exhibit random bursts of oscillation that decay in an under-damped fashion. Continuous oscillation occurs when operating in the area titled "Unstable." It is suggested that oven testing of the entire circuit be performed with maximum load, minimum input voltage, and minimum ambient temperature.

MOTOROLA

MC1466L

Specifications and Applications Information

3

PRECISION WIDE RANGE VOLTAGE and CURRENT REGULATOR

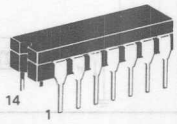
SILICON MONOLITHIC INTEGRATED CIRCUIT

PRECISION WIDE RANGE VOLTAGE AND CURRENT REGULATOR

This unique "floating" regulator can deliver hundreds of volts — limited only by the breakdown voltage of the external series pass transistor. Output voltage and output current are adjustable. The MC1466 integrated circuit voltage and current regulator is designed to give "laboratory" power-supply performance.

- Voltage/Current Regulation with Automatic Crossover
- Excellent Line Voltage Regulation, 0.03% +3.0 mV (Max)
- Excellent Load Voltage Regulation, 0.03% +3.0 mV (Max)
- Excellent Current Regulation, 0.2% +1.0 mA
- Short-Circuit Protection
- Output Voltage Adjustable to Zero Volts
- Internal Reference Voltage
- Adjustable Internal Current Source

L SUFFIX
CERAMIC PACKAGE
CASE 632-08



ORDERING INFORMATION		
Device	Temperature Range	Package
MC1466L	0°C to +70° C	Ceramic DIP

TYPICAL APPLICATIONS

FIGURE 1 – 0-TO-15 VDC, 10-AMPERES REGULATOR

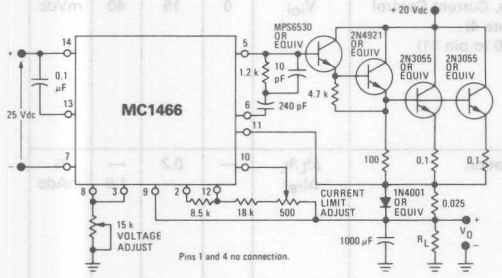


FIGURE 2 – 0-TO-40 VDC, 0.5-AMPERE REGULATOR

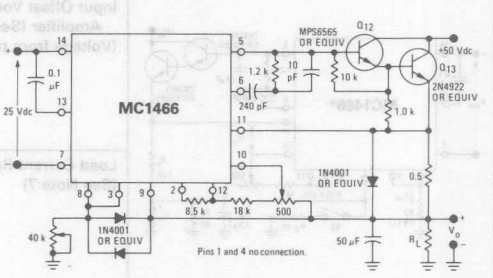


FIGURE 3 – 0-TO-250 VDC, 0.1-AMPERE REGULATOR

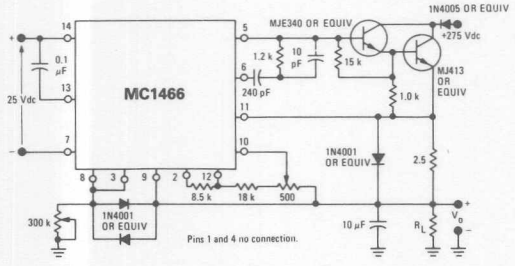
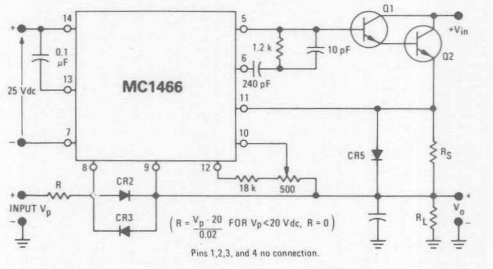


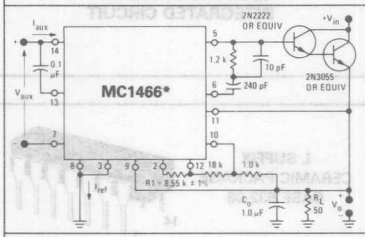
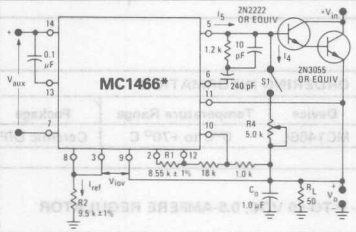
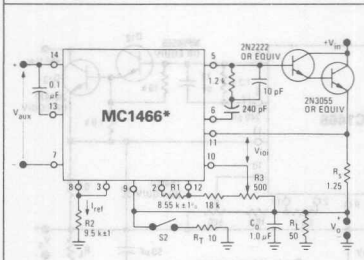
FIGURE 4 – REMOTE PROGRAMMING



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Auxiliary Voltage	V_{aux}	30	Vdc
Power Dissipation (Package Limitation) Derate above T_A = +50°C	P_D $1/\theta_{JA}$	750 6.0	mW mW/°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{aux} = +25 Vdc unless otherwise noted)

Characteristic Definition	Characteristic	Symbol	Min	Typ	Max	Units
	Auxiliary Voltage (See Notes 1 & 2) (Voltage from pin 14 to pin 7)	V_{aux}	21	—	30	Vdc
	Auxiliary Current	I_{aux}	—	9.0	12	mAdc
	Internal Reference Voltage (Voltage from pin 12 to pin 7)	V_{IR}	17.3	18.2	19.7	Vdc
	Reference Current (See Note 3)	I_{ref}	0.8	1.0	1.2	mAdc
	Input Current — Pin 8	I_8	—	6.0	12	μAdc
	Power Dissipation	P_D	—	—	360	mW
	Input Offset Voltage, Voltage Control Amplifier (See Note 4)	V_{iov}	0	15	40	mVdc
	Load Voltage Regulation (See Note 5)	ΔV_{iov} $\Delta V_{ref}/V_{ref}$	— —	1.0 0.015	3.0 0.03	mV %
	Line Voltage Regulation (See Note 6)	ΔV_{iov} $\Delta V_{ref}/V_{ref}$	— —	1.0 0.015	3.0 0.03	mV %
	Temperature Coefficient of Output Voltage (T_A = 0 to +75°C)	TCV_o	—	0.01	—	%/°C
	Input Offset Voltage, Current Control Amplifier (See Note 4) (Voltage from pin 10 to pin 11)	V_{ioi}	0	15	40	mVdc
	Load Current Regulation (See Note 7)	$\Delta I_L/I_L$ ΔI_{ref}	— —	0.2 —	— 1.0	% mAdc

*Pins 1 and 4 no connection.

NOTE 1:
The instantaneous input voltage, V_{aux}, must not exceed the maximum value of 30 volts for the MC1466. The instantaneous value of V_{aux} must be greater than 21 volts for the MC1466 for proper internal regulation.

NOTE 2:
The auxiliary supply voltage V_{aux}, must "float" and be electrically isolated from the unregulated high voltage supply, V_{in}.

NOTE 3:
Reference current may be set to any value of current less than 1.2 mAdc by applying the relationship:

$$I_{ref}\ (mA) = \frac{8.55}{R_1\ (k\Omega)}.$$

NOTE 4:
A built-in offset voltage (15 mVdc nominal) is provided so that the power supply output voltage or current may be adjusted to zero.

NOTE 5:
Load Voltage Regulation is a function of two additive components, ΔV_{iov} and ΔV_{ref}, where ΔV_{iov} is the change in input offset voltage (measured between pins 8 and 9) and ΔV_{ref} is the change in voltage across R2 (measured between pin 8 and ground). Each component may be measured separately or the sum may be measured across the load. The measurement procedure for the test circuit shown is:

a. With S1 open ($I_4 = 0$) measure the value of $V_{iov\ (1)}$ and $V_{ref\ (1)}$.
b. Close S1, adjust R4 so that $I_4 = 500\ \mu A$ and note $V_{iov\ (2)}$ and $V_{ref\ (2)}$.

Then $\Delta V_{iov} = V_{iov\ (1)} - V_{iov\ (2)}$

% Reference Regulation =

$$\frac{[V_{ref\ (1)} - V_{ref\ (2)}]}{V_{ref\ (1)}}\ (100\%) = \frac{\Delta V_{ref}}{V_{ref}}\ (100\%)$$

Load Voltage Regulation =

$$\frac{\Delta V_{ref}}{V_{ref}}\ (100\%) + \Delta V_{iov}.$$

NOTE 6:
Line Voltage Regulation is a function of the same two additive components as Load Voltage Regulation, ΔV_{iov} and ΔV_{ref} (see Note 5). The measurement procedure is:

a. Set the auxiliary voltage, V_{aux}, to 22 volts. Read the value of $V_{iov\ (1)}$ and $V_{ref\ (1)}$.
b. Change the V_{aux} to 28 volts and note the value of $V_{iov\ (2)}$ and $V_{ref\ (2)}$. Then compute Line Voltage Regulation:

$\Delta V_{iov} = \Delta V_{iov\ (1)} - V_{iov\ (2)}$

% Reference Regulation =

$$\frac{[V_{ref\ (1)} - V_{ref\ (2)}]}{V_{ref\ (1)}}\ (100\%) = \frac{\Delta V_{ref}}{V_{ref}}\ (100\%)$$

Line Voltage Regulation =

$$\frac{\Delta V_{ref}}{V_{ref}}\ (100\%) + \Delta V_{iov}.$$

NOTE 7:
Load Current Regulation is measured by the following procedure:

a. With S2 open, adjust R3 for an initial load current, $I_{L(1)}$, such that V_o is 8.0 Vdc.
b. With S2 closed, adjust R_T for $V_o = 1.0$ Vdc and read $I_{L(2)}$. Then Load Current Regulation =

$$\frac{[I_{L(2)} - I_{L(1)}]}{I_{L(1)}}\ (100\%) + I_{ref}$$

where I_{ref} is 1.0 mAdc, Load Current Regulation is specified in this manner because I_{ref} passes through the load in a direction opposite that of load current and does not pass through the current sense resistor, R_S.

FIGURE 5

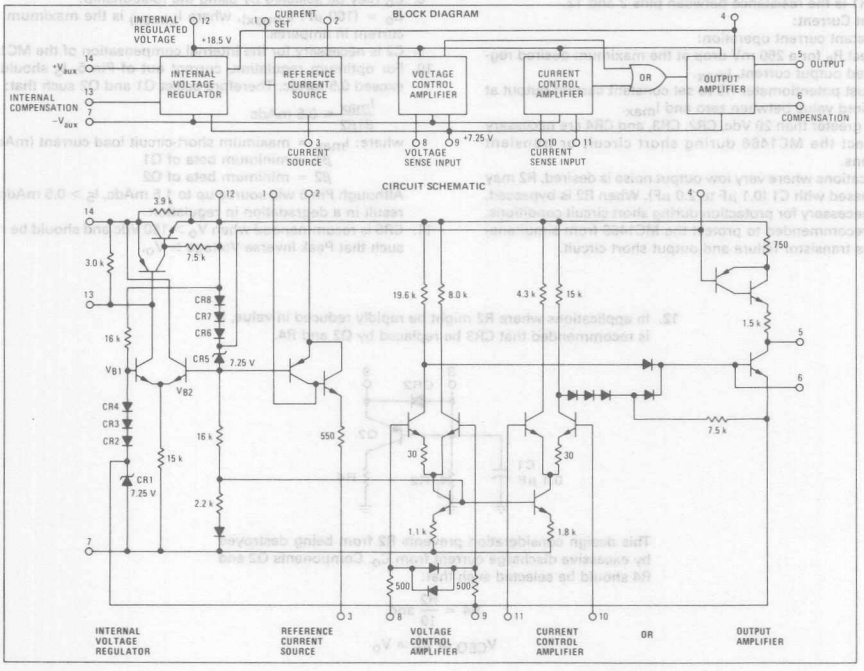
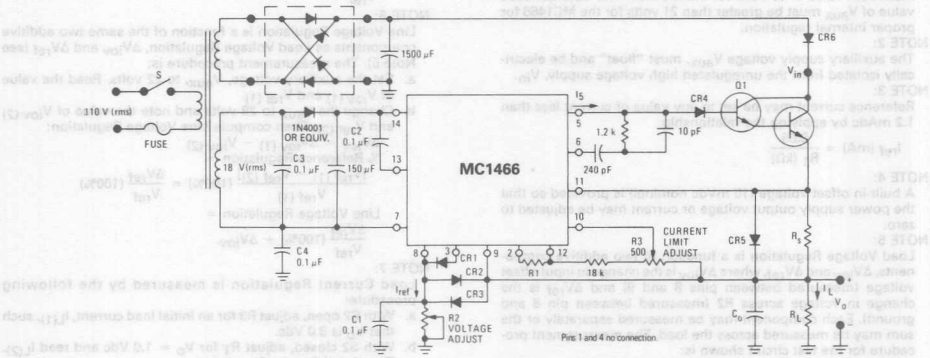
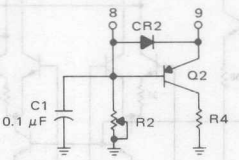


FIGURE 6 – TYPICAL CIRCUIT CONNECTION



NORMAL DESIGN PROCEDURE AND DESIGN CONSIDERATIONS

1. Constant Voltage:
   For constant voltage operation, output voltage V_O is given by:
   $V_O = (I_{ref})(R_2)$
   where R2 is the resistance from pin 8 to ground and I_{ref} is the output current of pin 3.
   The recommended value of I_{ref} is 1.0 mAdc. Resistor R1 sets the value of I_{ref}:
   $$I_{ref} = \frac{8.5}{R_1}$$
   where R1 is the resistance between pins 2 and 12.
2. Constant Current:
   For constant current operation:
   (a) Select R_s for a 250 mV drop at the maximum desired regulated output current, I_{max}.
   (b) Adjust potentiometer R3 to set constant current output at desired value between zero and I_{max}.
3. If V_{in} is greater than 20 Vdc, CR2, CR3, and CR4 are necessary to protect the MC1466 during short circuit or transient conditions.
4. In applications where very low output noise is desired, R2 may be bypassed with C1 (0.1 μF to 2.0 μF). When R2 is bypassed, CR1 is necessary for protection during short circuit conditions.
5. CR5 is recommended to protect the MC1466 from simultaneous pass transistor failure and output short circuit.
6. The RC network (10 pF, 240 pF, 1.2 kΩ) is used for compensation. The values shown are valid for all applications. However, the 10 pF capacitor may be omitted if f_T of Q1 and Q2 is greater than 0.5 MHz.
7. For remote sense applications, the positive voltage sense terminal (Pin 9) is connected to the positive load terminal through a separate sense lead; and the negative sense terminal (the ground side of R2) is connected to the negative load terminal through a separate sense lead.
8. C_O may be selected by using the relationship:
   $C_O = (100\ \mu F)\ I_{L(max)}$, where $I_{L(max)}$ is the maximum load current in amperes.
9. C2 is necessary for the internal compensation of the MC1466.
10. For optimum regulation, current out of Pin 5, I_5 should not exceed 0.5 mAdc. Therefore select Q1 and Q2 such that:
    $$\frac{I_{max}}{\beta 1 \beta 2} \leq 0.5\ \text{mAdc}$$
    where: I_{max} = maximum short-circuit load current (mAdc)
    $\beta 1$ = minimum beta of Q1
    $\beta 2$ = minimum beta of Q2
    Although Pin 5 will source up to 1.5 mAdc, $I_5 > 0.5$ mAdc will result in a degradation in regulation.
11. CR6 is recommended when $V_O > 150$ Vdc and should be rated such that Peak Inverse Voltage $> V_O$.
12. In applications where R2 might be rapidly reduced in value, it is recommended that CR3 be replaced by Q2 and R4.



This design consideration prevents R2 from being destroyed by excessive discharge current from C_O. Components Q2 and R4 should be selected such that:

$$R4 = \frac{R2}{10} \text{ and}$$

$$V_{CEO} \text{ of Q2} \geq V_O$$

OPERATION AND APPLICATIONS

This section describes the operation and design of the MC1466 voltage and current regulator and also provides information on useful applications.

SUBJECT SEQUENCE

Theory of Operation
Applications
Transient Failures
Voltage/Current Mode Indicator

THEORY OF OPERATION

The schematic of Figure 5 can be simplified by breaking it down into basic functions, beginning with a simplified version of the voltage reference, Figure 7. Zener diodes CR1 and CR5 with their associated forward biased diodes CR2 through CR4 and CR6 through CR8 form the stable reference needed to balance the differential amplifier. At balance ($V_{B1} = V_{B2}$), the output voltage, ($V_{12} - V_7$), is at a value that is twice the drop across either of the two diode strings: $V_{12} - V_7 = 2\,(V_{CR1} + V_{CR2} + V_{CR3} + V_{CR4})$. Other voltages, temperature compensated or otherwise, are also derived from these diodes strings for use in other parts of the circuit.

The voltage controlled current source (Figure 8) is a PNP-NPN composite which, due to the high NPN beta, yields a good working PNP from a lateral device working at a collector current of only a few microamperes. Its base voltage (V_{B_2}) is derived from a temperature compensated portion of the diode string and consequently the overall current is dependent on the value of emitter resistor R1. Temperature compensation of the base emitter junction of Q3 is not important because approximately 9 volts exists between V_{B_2} and V_{12}, making the ΔV_{BE}'s very small in percentage. Circuit reference voltage is derived from the product of I_R and R_R; if I_R is set at 1 mA (R1 = 8.5 kΩ), then R_R (in kΩ) = V_O. Other values of current may be used as long as the following restraints are kept in mind: 1) package dissipation will be increased by about 11 mW/mA and 2) bias current for the voltage control amplifier is 3 μA, temperature dependent, and is extracted from the reference current. The reference current should

FIGURE 7 – REFERENCE VOLTAGE REGULATOR

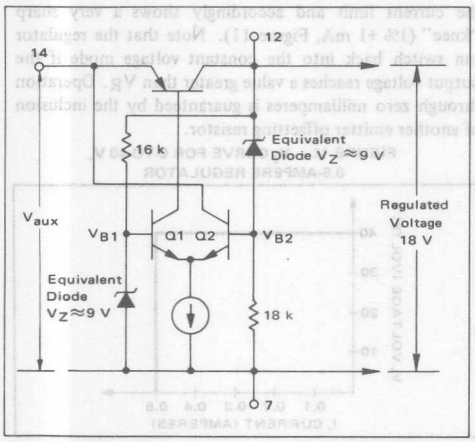
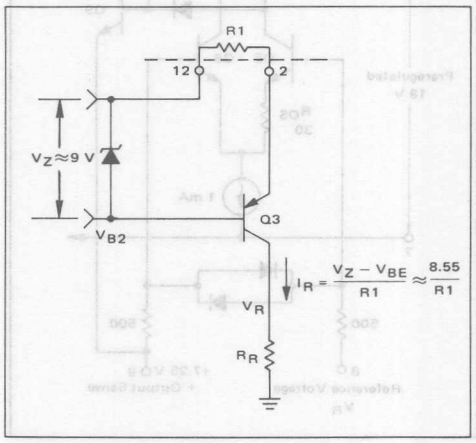


FIGURE 8 – VOLTAGE CONTROLLED CURRENT SOURCE



pected bias current.

Loop amplification in the constant voltage mode is supplied by the voltage controlled amplifier (Figure 9), a standard high gain differential amplifier. The inputs are diode-protected against differential overvoltages and an emitter degenerating resistor, R_{OS}, has been added to one of the transistors. For an emitter current in both Q5 and Q6 of 1/2 milliampere there will exist a preset offset voltage in this differential amplifier of 15 mV to insure that the output voltage will be zero when the reference voltage is zero. Without R_{OS}, the output voltage could be a few millivolts above zero due to the inherent offset. Since the load resistor is so large in this stage compared with the load (Q9) it will be more instructive to look at the gain on a transconductance basis rather than voltage gain. Transconductance of the differential stage is defined for small signals as:

$$g_m = \frac{1}{2r_e + R_E} \quad (1)$$

where

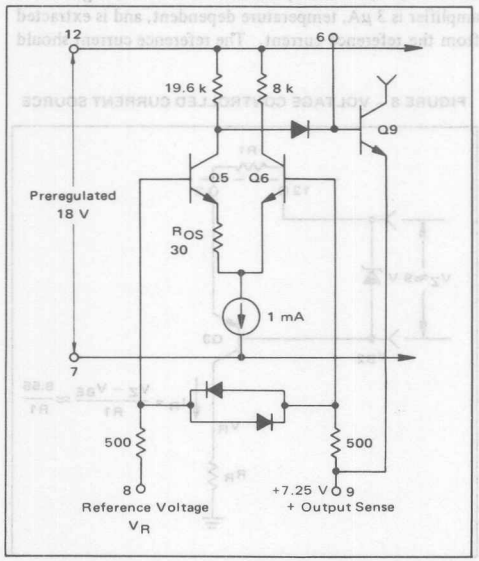
$$r_e \approx \frac{0.026}{I_E} \text{ and}$$

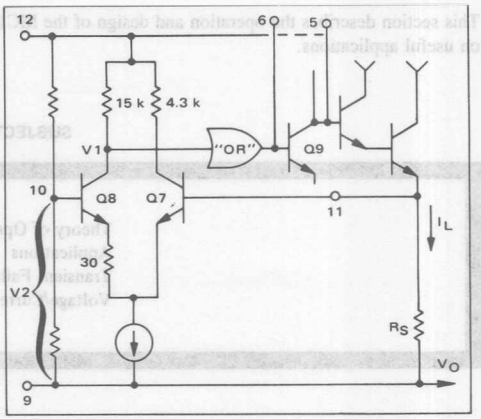
R_E = added emitter degenerating resistance.

For I_E = 0.5 mA,

$$g_m = \frac{1}{104 + 30} = \frac{1}{134} = 7.5 \text{ mA/volt.} \quad (2)$$

FIGURE 9 – VOLTAGE CONTROL AMPLIFIER

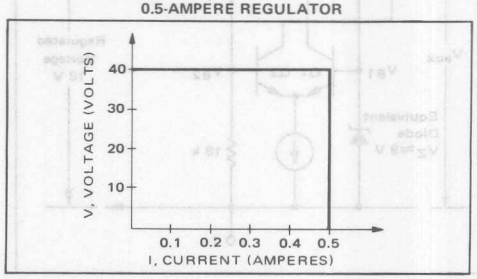




This level is further boosted by the output stage such that in the constant voltage mode overall transconductance is about 300 mA/volt.

A second differential stage nearly identical to the first stage, serves as the current control amplifier (Figure 10). The gain of this stage insures a rapid crossover from the constant voltage to constant current modes and provides a convenient point to control the maximum deliverable load current. In use, a reference voltage derived from the preregulator and a voltage divider is applied to pin 10 while the output current is sampled across R_S by pin 11. When I_L R_S is 15 mV below the reference value, voltage V_1 begins to rapidly rise, eventually gaining complete control of Q9 and limiting output current to a value of V_2/R_S. If V_2 is derived from a variable source, short circuit current may be controlled over the complete output current capability of the regulator. Since the constant-voltage to constant-current change-over requires only a few millivolts the voltage regulation maintains its quality to the current limit and accordingly shows a very sharp "knee" (1% +1 mA, Figure 11). Note that the regulator can switch back into the constant voltage mode if the output voltage reaches a value greater than V_R. Operation through zero milliamperes is guaranteed by the inclusion of another emitter offsetting resistor.

FIGURE 11 – V_I CURVE FOR 0-TO-40 V, 0.5-AMPERE REGULATOR



Transistor Q9 and five diodes comprise the essential parts of the output stage (Figure 12). The diodes perform an "OR" function which allows only one mode of operation at a time - constant current or constant voltage. However, an additional stage (Q9) must be included to invert the logic and make it compatible with the driving requirements of series pass transistors as well as provide additional gain. A 1.5 mA collector current source sets the maximum deliverable output current and boosts the output impedance to that of the current source.

Note that the negative (substrate) side of the MC1466 is 7.25 volts lower than the output voltage, and the reference regulator guarantees that the positive side is 11 volts above the output. Thus the IC remains at a voltage (relative to ground) solely dependent on the output, "floating" above and below V_O. V_{CE} across Q9 is only two or three V_{BE}'s depending on the number of transistors used in the series pass configuration.

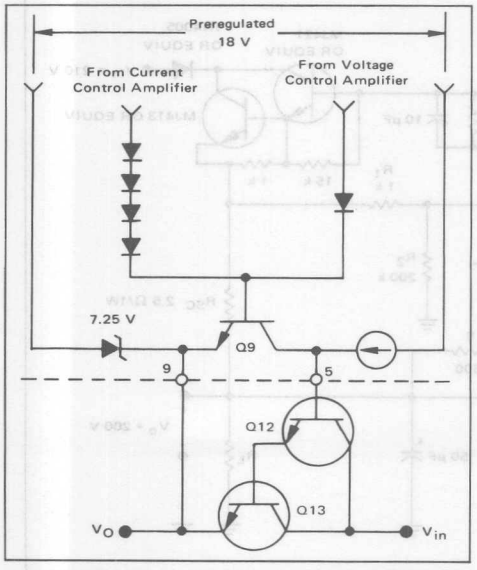
Performance characteristics of the regulator may be approximately calculated for a given circuit (Figure 2). Assuming that the two added transistors (Q12 and Q13) have minimum betas of 20, then the overall regulator transconductance will be:

$$g_{mT} = (400)\,300\ \text{mA/volt} = 120\ \text{A/volt}. \quad (3)$$

For a change in current of 500 mA the output voltage will drop only:

$$\Delta V = \frac{0.5}{120} = 4.2\ \text{mV}. \quad (4)$$

FIGURE 12 — MC1466 OUTPUT STAGE



The analysis thus far does not consider changes in V_R due to output current changes. If I_L increases by 500 mA the collector current of Q9 decreases by 1.25 mA, causing the collector current of Q5 to increase by 30 μA. Accordingly, I_R will be decreased by $\approx$0.30 μA which will drop the output by 0.03%. This figure may be improved considerably by either using high beta devices as the pass transistors, or by increasing I_R. Note again, however, that the maximum power rating of the package must be kept in mind. For example if I_R = 4 mA, power dissipation is

$$P_D = 20\ \text{V}\,(8\ \text{mA}) + (11\ \text{V} \times 3\ \text{mA}) = 193\ \text{mW}. \quad (5)$$

This indicates that the circuit may be safely operated up to 118°C using 20 volts at the auxiliary supply voltage. If, however, the auxiliary supply voltage is 35 volts,

$$P_D = 35\ \text{V}\,(8\ \text{mA}) + 26\ \text{V}\,(3\ \text{mA}) = 358\ \text{mW}. \quad (6)$$

which dictates that the maximum operating temperature must be less than 91°C to keep package dissipation within specified limits.

Line voltage regulation is also a function of the voltage change between pins 8 and 9, and the change of V_{ref}. In this case, however, these voltages change due to changes in the internal regulator's voltages, which in turn are caused by changes in V_{aux}. Note that line voltage regulation is not a function of V_{in}. Note also that the instantaneous value of V_{aux} must always be between 20 and 35 volts.

Figure 6 shows six external diodes (CR_1 to CR_6) added for protective purposes. CR_1 should be used if the output voltage is less than 20 volts and CR_2, CR_3 are absent. For V_O higher than 20 volts, CR_1 should be discarded in favor of CR_2 and CR_3. Diode CR_4 prevents IC failure if the series pass transistors develop collector-base shorts while the main power transistor suffers a simultaneous open emitter. If the possibility of such a transistor failure mode seems remote, CR_4 may be deleted. To prevent instantaneous differential and common mode breakdown of the current sense amplifier, CR_5 must be placed across the current limit resistor R_S.

Load transients occasionally produce a damaging reversal of current flow from output to input $V_O > 150$ volts (which will destroy the IC). Diode CR_6 prevents such reversal and renders the circuit immune from destruction for such conditions, e.g., adding a large output capacitor after the supply is turned "on". Diodes CR_1, CR_2, CR_3, and CR_5 may be general purpose silicon units such as 1N4001 or equivalent whereas CR_4 and CR_6 should have a peak inverse voltage rating equal to V_{in} or greater.

APPLICATIONS

Figure 2 shows a typical 0-to-40 volts, 0.5-ampere regulator with better than 0.01% performance. The RC network between pins 5 and 6 and the capacitor between pins 13 and 14 provide frequency compensation for the MC1466. The external pass transistors are used to boost load current, since the output current of the regulator is less than 2 mA.

3

Figure 1 is a 0-to-15 volts, 10-ampere regulator with the pass transistor configuration necessary to boost the load current to 10 amperes. Note that C_O has been increased to 1000 μF following the general rule:

$$C_O = 100\ \mu F/A\ I_L.$$

The prime advantage of the MC1466 is its use as a high voltage regulator, as shown in Figure 3. This 0-to-250 volts 0.1-ampere regulator is typical of high voltage applications, limited only by the breakdown and safe areas of the output pass transistors.

The primary limiting factor in high voltage series regulators is the pass transistor. Figure 13 shows a safe area curve for the MJ413. Looking at Figure 3, we see that if the output is shorted, the transistor will have a collector current of 100 mA, with a V_{CE} approximately equal to 260 volts. Thus this point falls on the dc line of the safe area curve, insuring that the transistor will not enter secondary breakdown.

In this respect (Safe Operating Area) the foldback circuit of Figure 14 is superior for handling high voltages and yet is short-circuit protected. This is due to the fact that load current is diminished as output voltage drops (V_{CE} increases as V_O drops) as seen in Figure 15. By careful design the load current at a short, I_{SC} can be made low enough such that the combined V_{CE} (V_{in}) and I_{SC} still falls within the dc safe operating area of the transistor. For the illustrated design (Figure 14), an input voltage of 210 volts is compatible with a short circuit current of 100 mA. Yet current foldback allows us to design for a maximum regulated load current of 500 mA. the pertinent design equations are:

$$\text{Let } R_2\ (k\Omega) = V_O$$

$$\alpha = \frac{0.25}{V_O}\left[\frac{I_k}{I_{SC}} - 1\right]$$

$$R_1\ (k\Omega) = \frac{\alpha}{1-\alpha}\ V_O$$

$$R_{SC} = \frac{0.25}{(1-\alpha)\ I_{SC}}.$$

FIGURE 13 – SAFE AREA CURVE FOR THE MJ413

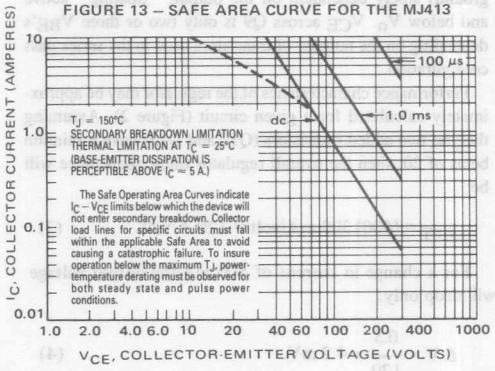
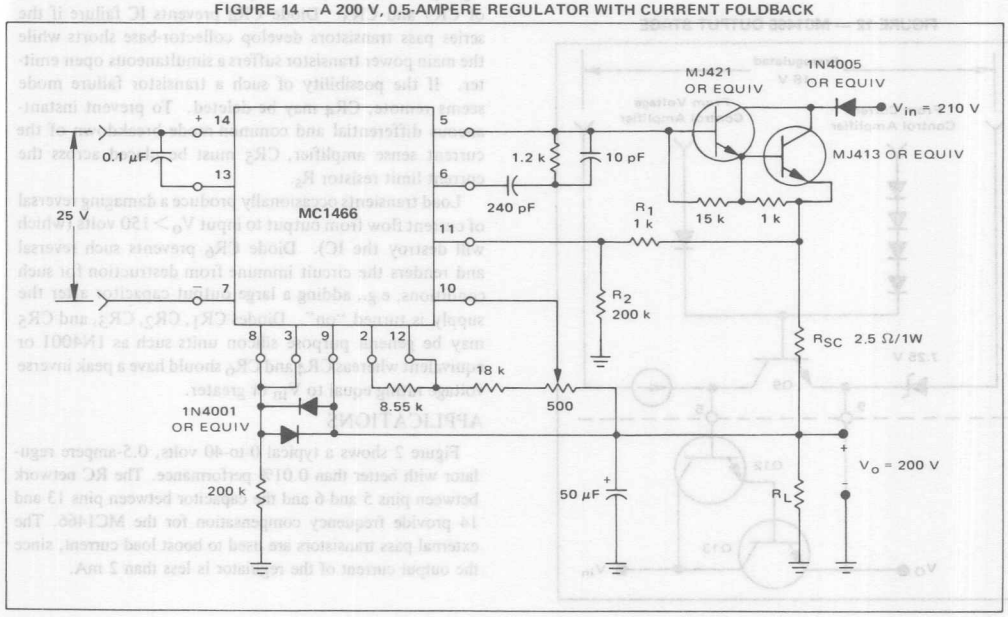


FIGURE 14 – A 200 V, 0.5-AMPERE REGULATOR WITH CURRENT FOLDBACK



The terms I_{SC} and I_k correspond to the short-circuit current and maximum available load current as shown in Figure 15.

FIGURE 15 – TYPICAL FOLDBACK PERFORMANCE

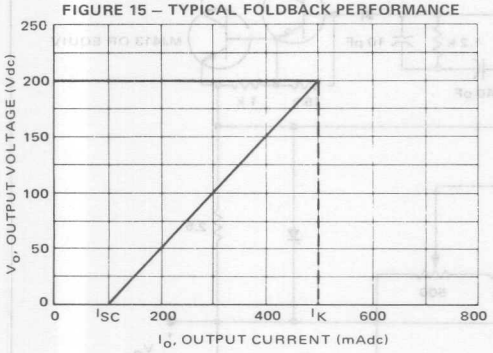


Figure 16 shows a remote sense application which should be used when high current or long wire lengths are used. This type of wiring is recommended for any application where the best possible regulation is desired. Since the sense lines draw only a small current, large voltage drops do not destroy the excellent regulation of the MC1466.

TRANSIENT FAILURES

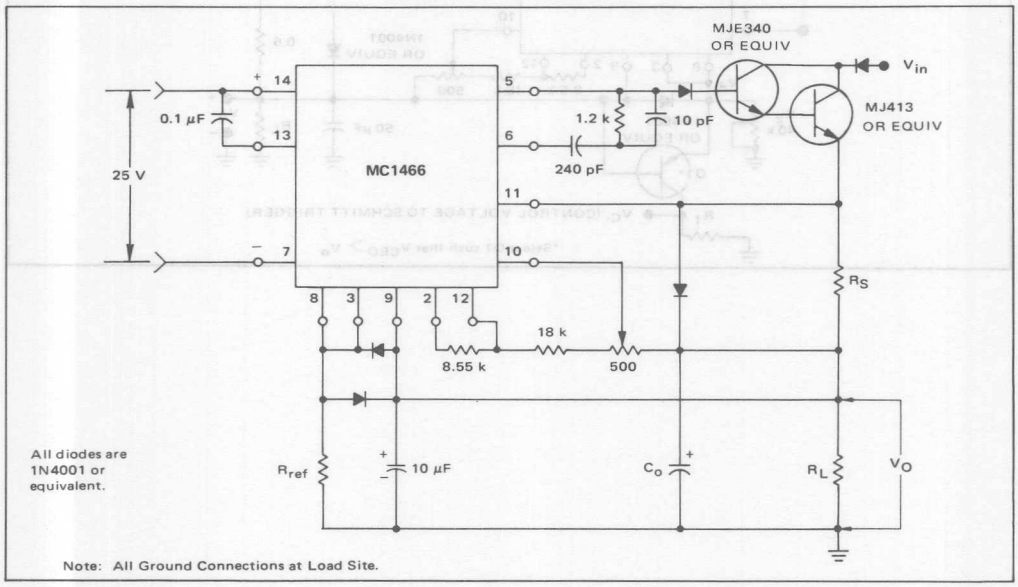
In industrial areas where electrical machinery is used the normal ac line often contains bursts of voltage running from hundreds to thousands of volts in magnitude and only microseconds in duration. Under some conditions this energy is dissipated across the internal zener connected between pins 9 and 7. This transient condition may produce a total failure of the regulator device without any apparent explanation. This type of failure is identified by absence of the 7 volt zener (CR1) between pin 9 and pin 7. To prevent this failure mode the use of a shielded power transformer is recommended, as shown in Figure 6. In addition, it is recommended that C1, C3 and C4 be included to aid in transient repression. These capacitors should have good high frequency characteristics.

If the possibility of transients on the output exists, the addition of a resistor and zener diode between pins 9 and 7 as shown on Figure 17 should be added.

VOLTAGE/CURRENT MODE INDICATOR

There may be times when it is desirable to know when the MC1466 is in the constant current mode or constant voltage mode. A mode indicator can be easily added to provide this feature. Figure 18 shows how a PNP transistor has replaced a protection diode between pins 8 and 9 of Figure 2. When the MC1466 goes from constant voltage mode to constant current mode, V_O will drop below V_8 and the PNP transistor will turn on. The 1 mA current supplied by pin 8 will now be shunted to base of Q2 thereby turning on the indicator device I1.

FIGURE 16 – REMOTE SENSE



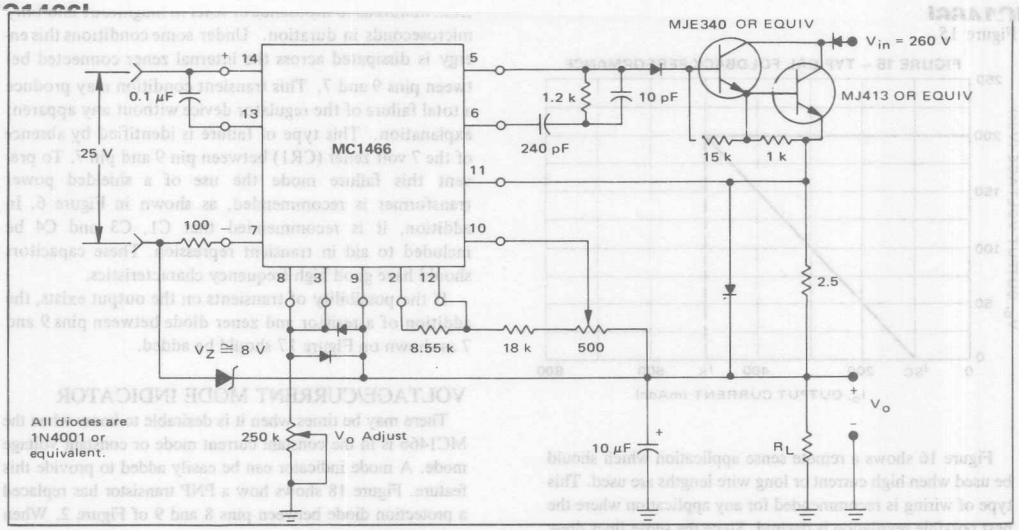
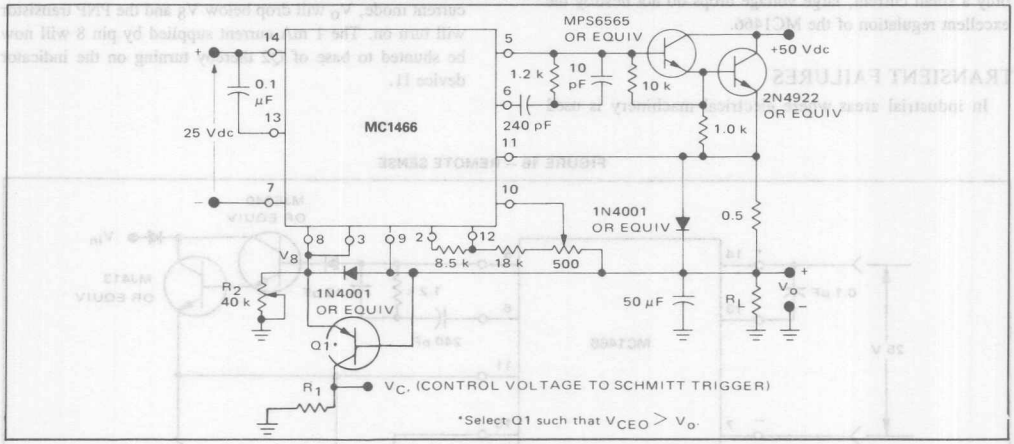


FIGURE 18 – 0-TO-40 Vdc, 0.5-AMPERE REGULATOR WITH MODE INDICATOR



MOTOROLA

MC1468
MC1568

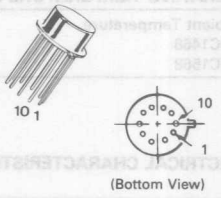
DUAL ±15-VOLT REGULATOR

The MC1568/MC1468 is a dual polarity tracking regulator designed to provide balanced positive and negative output voltages at currents to 100 mA. Internally, the device is set for ±15-volt outputs but an external adjustment can be used to change both outputs simultaneously from 8.0 to 20 volts. Input voltages up to ±30 volts can be used and there is provision for adjustable current limiting.

- Internally Set to ±15 V Tracking Outputs
- Output Currents to 100 mA
- Outputs Balanced to within 1.0% (MC1568)
- Line and Load Regulation of 0.06%
- 1.0% Maximum Output Variation Due to Temperature Changes
- Standby Current Drain of 3.0 mA
- Externally Adjustable Current Limit
- Remote Sensing Provisions

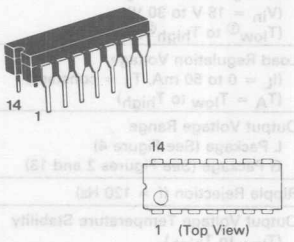
DUAL ±15-VOLT TRACKING REGULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT



(Bottom View)

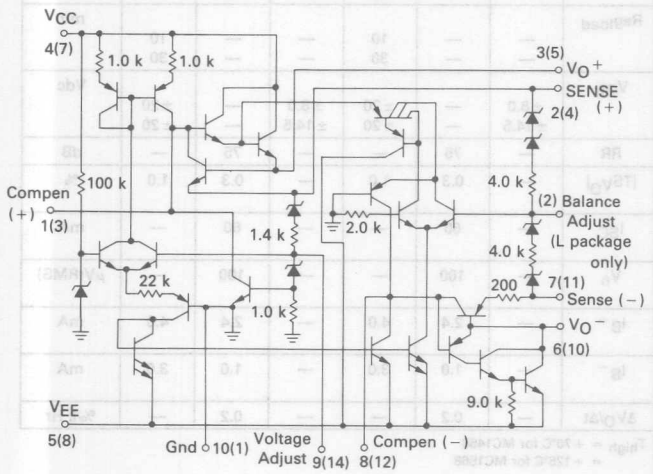
G SUFFIX
METAL PACKAGE
CASE 603C-01



(Top View)

L SUFFIX
CERAMIC PACKAGE
CASE 632-08

CIRCUIT SCHEMATIC



Pin numbers adjacent to terminals are for the G suffix package and pin numbers in parentheses are for the L suffix package.

ORDERING INFORMATION

Device	Temperature Range	Package
MC1468G	0°C to +70°C	Metal Can
MC1468L	0°C to +70°C	Ceramic DIP
MC1568G	−55°C to +125°C	Metal Can
MC1568L	−55°C to +125°C	Ceramic DIP

3

MAXIMUM RATINGS (T_C = +25°C unless otherwise noted.)

Rating	Symbol	Value		Unit
Input Voltage	V_{CC},$\lvert V_{EE}\rvert$	30		Vdc
Peak Load Current	I_{pk}	100		mA
Power Dissipation and Thermal Characteristics		G Package	L Package	
T_A = +25°C	P_D	0.83	1.25	Watts
Derate above T_A = +25°C	$1/\theta_{JA}$	6.6	10	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	150	100	°C/W
T_C = +25°C	P_D	1.8	2.5	Watts
Derate above T_C = +25°C	$1/\theta_{JC}$	14.3	20	mW/°C
Thermal Resistance, Junction to Case	θ_{JC}	70	50	°C/W
Storage Junction to Temperature Range	T_J, T_{stg}	−65 to +150		°C
Minimum Short-Circuit Resistance	R_{SC}(min)	4.0		Ohms

OPERATING TEMPERATURE RANGE

Ambient Temperature	T_A		°C
MC1468		0 to +70	
MC1568		−55 to +125	

ELECTRICAL CHARACTERISTICS (V_{CC} = +20 V, V_{EE} = −20 V, C1 = C2 = 1500 pF, C3 = C4 = 1.0 μF, R_{SC}^+ = R_{SC}^- = 4.0 Ω, I_L^+ = I_L^- = 0, T_C = +25°C unless otherwise noted.) (See Figure 1.)

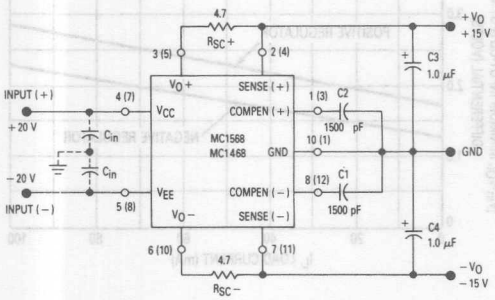
Characteristic	Symbol	MC1568			MC1468			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_O	±14.5	±15	±15.5	±14.5	±15	±15.5	Vdc
Input Voltage	V_{in}	—	—	±30	—	—	±30	Vdc
Input-Output Voltage Differential	$\lvert V_{in}$-$V_O\rvert$	2.0	—	—	2.0	—	—	Vdc
Output Voltage Balance (L package only)	V_{Bal}	—	±50	±150	—	±50	±300	mV
Line Regulation Voltage	Reg_{line}							mV
(V_{in} = 18 V to 30 V)		—	—	10	—	—	10	
(T_{low}① to T_{high}②)		—	—	20	—	—	20	
Load Regulation Voltage	Reg_{load}							mV
(I_L = 0 to 50 mA, T_J = constant)		—	—	10	—	—	10	
(T_A = T_{low} to T_{high})		—	—	30	—	—	30	
Output Voltage Range	V_{OR}							Vdc
L Package (See Figure 4)		±8.0	—	±20	±8.0	—	±20	
G Package (See Figures 2 and 13)		±14.5	—	±20	±14.5	—	±20	
Ripple Rejection (f = 120 Hz)	RR	—	75	—	—	75	—	dB
Output Voltage Temperature Stability (T_{low} to T_{high})	$\lvert TS_{VO}\rvert$	—	0.3	1.0	—	0.3	1.0	%
Short-Circuit Current Limit (R_{SC} = 10 ohms)	I_{SC}	—	60	—	—	60	—	mA
Output Noise Voltage (BW = 100 Hz–10 kHz)	V_n	—	100	—	—	100	—	μV(RMS)
Positive Standby Current (V_{in} = +30 V)	I_B^+	—	2.4	4.0	—	2.4	4.0	mA
Negative Standby Current (V_{in} = −30 V)	I_B^-	—	1.0	3.0	—	1.0	3.0	mA
Long-Term Stability	$\Delta V_O/\Delta t$	—	0.2	—	—	0.2	—	%/k Hr

① T_{low} = 0°C for MC1468
= −55°C for MC1568

② T_{high} = +70°C for MC1468
= +125°C for MC1568

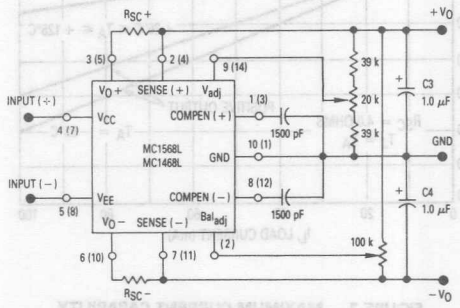
TYPICAL APPLICATIONS

FIGURE 1 — BASIC 50-mA REGULATOR



C1 and C2 should be located as close to the device as possible. A 0.1 μF ceramic capacitor (C_{in}) may be required on the input lines if the device is located an appreciable distance from the rectifier filter capacitors. C3 and C4 may be increased to improve load transient response and to reduce the output noise voltage. At low temperature operation, it may be necessary to bypass C4 with a 0.1 μF ceramic disc capacitor.

FIGURE 2 — VOLTAGE ADJUST AND BALANCE ADJUST CIRCUIT
(14.5 V ≤ V_{out} ≤ 20 V)



Balance adjust available in MC1568L, MC1468L ceramic dual in-line package only.

FIGURE 3 — ±1.5-AMPERE REGULATOR
(Short-Circuit Protected, with Proper Heatsinking)

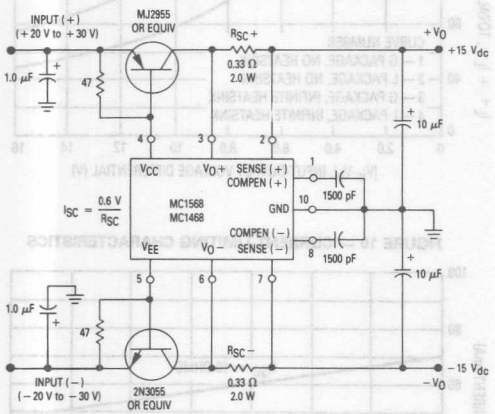
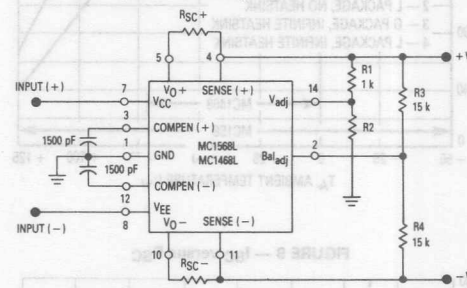


FIGURE 4 — OUTPUT VOLTAGE ADJUSTMENT FOR 8.0 V ≤ |±V_O| ≤ 14.5 V
(Ceramic-Packaged Devices Only)



The presence of Bal_{adj}, pin 2, on devices housed in the dual in-line package (L suffix) allows the user to adjust the output voltages down to ±8.0 V. The required value of resistor R2 can be calculated from

$$R2 = \frac{R1\,R_{int}\,(\phi + V_z)}{R_{int}\,(V_O - \phi - V_z) - \phi\,R1}$$

Where: R_{int} = An Internal Resistor = R1 = 1.0 kΩ
ϕ = 0.68 V
V_z = 6.6 V

Some common design values are listed below:

±V_O(V)	R2	T_C V_O (%/°C)	I_B + (mA)
14	1.2 k	0.003	10
12	1.8 k	0.022	7.2
10	3.5 k	0.025	5.0
8.0	∞	0.028	2.6

TYPICAL CHARACTERISTICS

(V_{CC} = +20 V, V_{EE} = −20 V, V_O = ±15 V, T_A = +25°C unless otherwise noted.)

FIGURE 5 — LOAD REGULATION

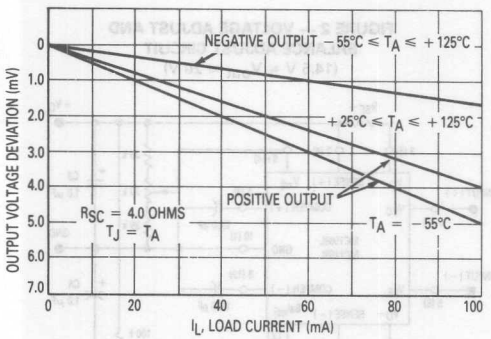


FIGURE 6 — REGULATOR DROPOUT VOLTAGE

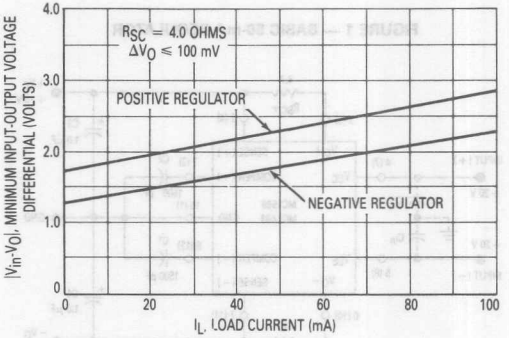


FIGURE 7 — MAXIMUM CURRENT CAPABILITY

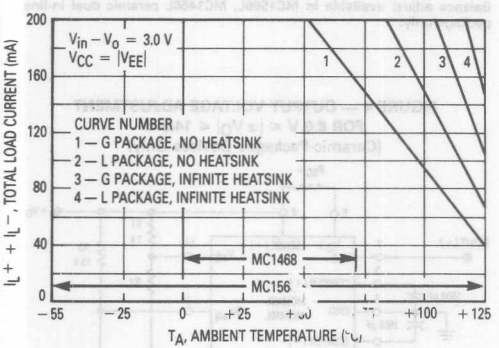


FIGURE 8 — MAXIMUM CURRENT CAPABILITY

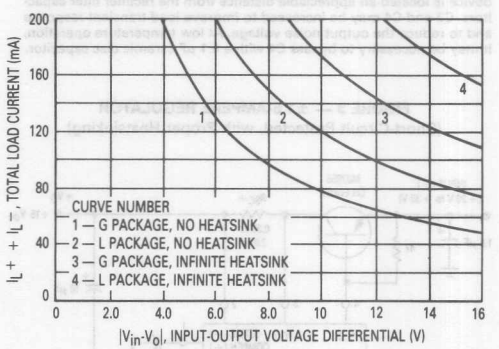


FIGURE 9 — I_{SC} versus R_{SC}

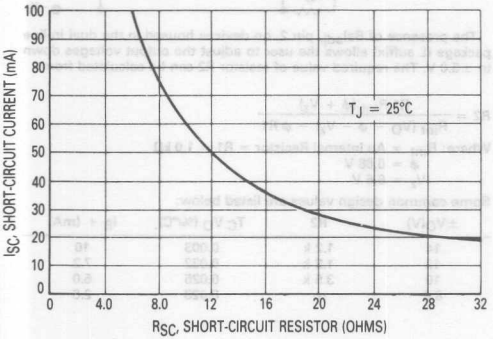
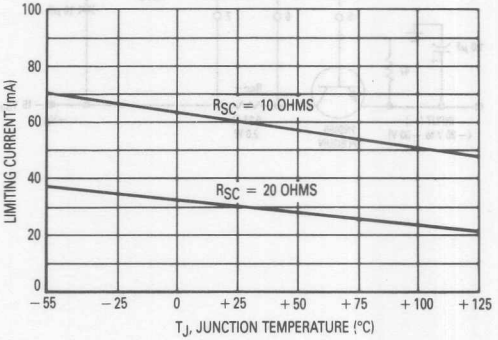


FIGURE 10 — CURRENT-LIMITING CHARACTERISTICS



TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +20 V, V_{EE} = −20 V, V_O = ±15 V, T_A = +25°C unless otherwise noted.)

FIGURE 11 — STANDBY CURRENT DRAIN

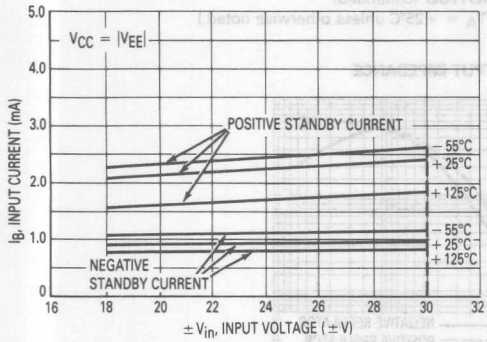


FIGURE 12 — STANDBY CURRENT DRAIN

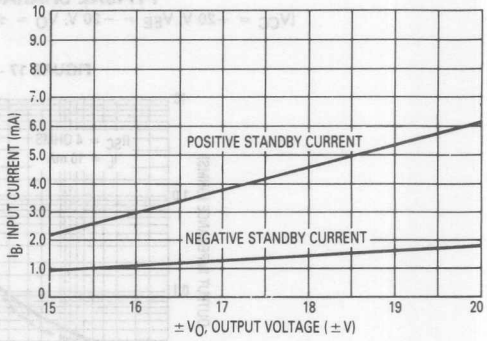


FIGURE 13 — TEMPERATURE COEFFICIENT OF OUTPUT VOLTAGE

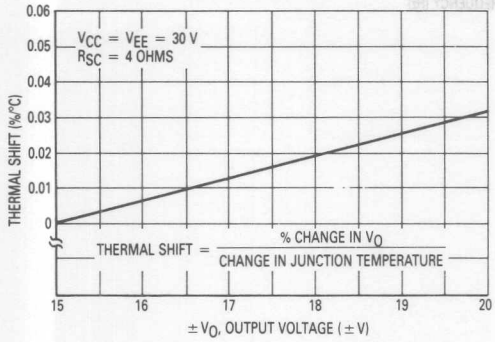


FIGURE 14 — LOAD TRANSIENT RESPONSE

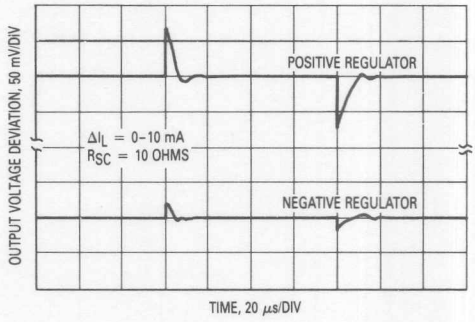


FIGURE 15 — LINE TRANSIENT RESPONSE

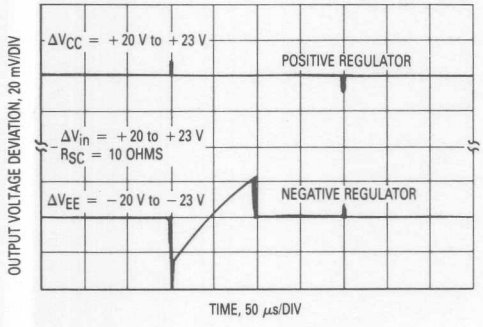
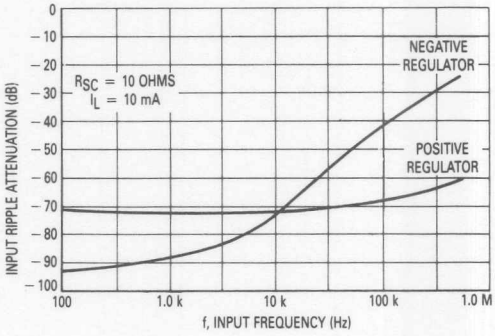


FIGURE 16 — RIPPLE REJECTION

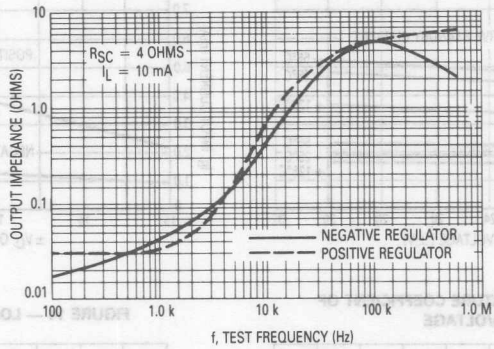


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TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +20 V, V_{EE} = −20 V, V_O = ±15 V, T_A = +25°C unless otherwise noted.)

FIGURE 17 — OUTPUT IMPEDANCE



ORDERING INFORMATION

Device	Alternate	Temperature Range	Package
MC1723CD		0°C to +70°C	SO-14
MC1723CG	LM723CH, μA723HC	0°C to +70°C	Metal Can
MC1723CL	LM723CD, μA723DC	0°C to +70°C	Ceramic DIP
MC1723CP	LM723CN, μA723PC	0°C to +70°C	Plastic DIP
MC1723G		−55°C to +125°C	Metal Can
MC1723L		−55°C to +125°C	Ceramic DIP

MC1723
MC1723C

VOLTAGE REGULATOR

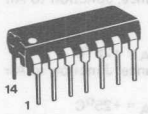
SILICON MONOLITHIC INTEGRATED CIRCUIT

3

MONOLITHIC VOLTAGE REGULATOR

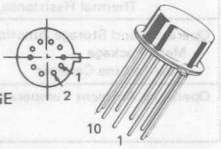
The MC1723 is a positive or negative voltage regulator designed to deliver load current to 150 mAdc. Output current capability can be increased to several amperes through use of one or more external pass transistors. MC1723 is specified for operation over the military temperature range (-55°C to +125°C) and the MC1723C over the commercial temperature range (0 to +70°C).

- Output Voltage Adjustable from 2 Vdc to 37 Vdc
- Output Current to 150 mAdc Without External Pass Transistors
- 0.01% Line and 0.03% Load Regulation
- Adjustable Short-Circuit Protection

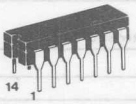


P SUFFIX
PLASTIC PACKAGE
CASE 646-06

(Bottom View)



G SUFFIX
METAL PACKAGE
CASE 603-04

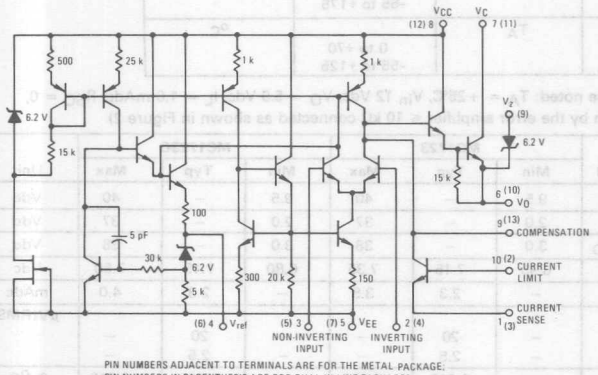


L SUFFIX
CERAMIC PACKAGE
CASE 632-08

D SUFFIX
PLASTIC PACKAGE
CASE 751A-02
SO-14

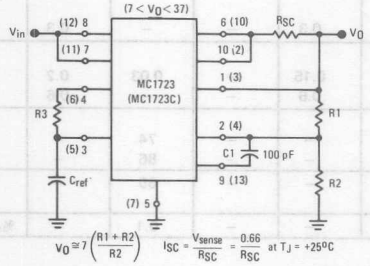


FIGURE 1 – CIRCUIT SCHEMATIC



PIN NUMBERS ADJACENT TO TERMINALS ARE FOR THE METAL PACKAGE.
PIN NUMBERS IN PARENTHESIS ARE FOR DUAL IN-LINE PACKAGES.

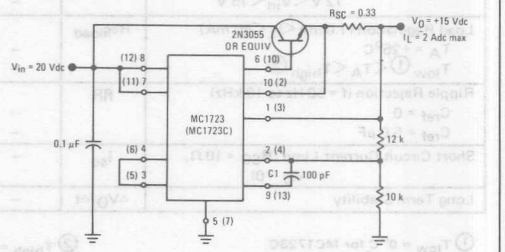
FIGURE 2 – TYPICAL CIRCUIT CONNECTION



$V_O \cong 7\left(\frac{R1 + R2}{R2}\right)$ $I_{SC} = \frac{V_{sense}}{R_{SC}} = \frac{0.66}{R_{SC}}$ at $T_J = +25°C$

For best results 10 k < R2 < 100 k
For minimum drift R3 = R1||R2

FIGURE 3 – TYPICAL NPN CURRENT BOOST CONNECTION



Pulse Voltage from V_{CC} to V_{EE} (50 ms)	$V_{in(p)}$	50	V_{peak}
Continuous Voltage from V_{CC} to V_{EE}	V_{in}	40	Vdc
Input-Output Voltage Differential	$V_{in} - V_O$	40	Vdc
Maximum Output Current	I_L	150	mAdc
Current from V_{ref}	I_{ref}	15	mAdc
Current from V_z	I_z	25	mA
Voltage Between Non-Inverting Input and V_{EE}	V_{ie}	8.0	Vdc
Differential Input Voltage	V_{id}	±5.0	Vdc
Power Dissipation and Thermal Characteristics			
Plastic Package			
T_A = +25°C	P_D	1.25	W
Derate above T_A = +25°C	$1/\theta_{JA}$	10	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	100	°C/W
Metal Package			
T_A = +25°C	P_D	1.0	Watt
Derate above T_A = +25°C	$1/\theta_{JA}$	6.6	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	150	°C/W
T_C = +25°C	P_D	2.1	Watts
Derate above T_A = +25°C	$1/\theta_{JA}$	14	mW/°C
Thermal Resistance, Junction to Case	θ_{JC}	35	°C/W
Dual In-Line Ceramic Package	P_D	1.5	Watt
Derate above T_A = +25°C	$1/\theta_{JA}$	10	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	100	°C/W
Operating and Storage Junction Temperature Range	T_J, T_{stg}		°C
Metal Package		-65 to +150	
Dual In-Line Ceramic		-65 to +175	
Operating Ambient Temperature Range	T_A		°C
MC1723C		0 to +70	
MC1723		-55 to +125	

ELECTRICAL CHARACTERISTICS (Unless otherwise noted: T_A = +25°C, V_{in} 12 Vdc, V_O = 5.0 Vdc, I_L = 1.0 mAdc, R_{SC} = 0, C1 = 100 pF, C_{ref} = 0 and divider impedance as seen by the error amplifier ≤ 10 kΩ connected as shown in Figure 2)

Characteristic	Symbol	MC1723 Min	MC1723 Typ	MC1723 Max	MC1723C Min	MC1723C Typ	MC1723C Max	Unit
Input Voltage Range	V_{in}	9.5	–	40	9.5	–	40	Vdc
Output Voltage Range	V_O	2.0	–	37	2.0	–	37	Vdc
Input-Output Voltage Differential	$V_{in}-V_O$	3.0	–	38	3.0	–	38	Vdc
Reference Voltage	V_{ref}	6.95	7.15	7.35	6.80	7.15	7.50	Vdc
Standby Current Drain (I_L = 0, V_{in} = 30 V)	I_{IB}	–	2.3	3.5	–	2.3	4.0	mAdc
Output Noise Voltage (f = 100 Hz to 10 kHz)	V_n							μV(RMS)
C_{ref} = 0		–	20	–	–	20	–	
C_{ref} = 5.0 μF		–	2.5	–	–	2.5	–	
Average Temperature Coefficient of Output Voltage (T_{low} ① < T_A < T_{high} ②)	TCV_O	–	0.002	0.015	–	0.003	0.015	%/°C
Line Regulation	Reg_{line}							%V_O
(T_A = +25°C) 12 V ≤ V_{in} ≤ 15 V		–	0.01	0.1	–	0.01	0.1	
(T_A = +25°C) 12 V ≤ V_{in} ≤ 40 V		–	0.02	0.2	–	0.1	0.5	
(T_{low} ① < T_A < T_{high} ②) 12 V ≤ V_{in} ≤ 15 V		–	–	0.3	–	–	0.3	
Load Regulation (1.0 mA ≤ I_L ≤ 50 mA)	Reg_{load}							%V_O
T_A = +25°C		–	0.03	0.15	–	0.03	0.2	
T_{low} ① < T_A < T_{high} ②		–	–	0.6	–	–	0.6	
Ripple Rejection (f = 50 Hz to 10 kHz)	RR							dB
C_{ref} = 0		–	74	–	–	74	–	
C_{ref} = 5.0 μF		–	86	–	–	86	–	
Short Circuit Current Limit (R_{SC} = 10 Ω, V_O = 0)	I_{sc}	–	65	–	–	65	–	mAdc
Long Term Stability	$\Delta V_O/\Delta t$	–	0.1	–	–	0.1	–	%/1000 Hr

① T_{low} = 0°C for MC1723C
= -55°C for MC1723

② T_{high} = +70°C for MC1723C
= +125°C for MC1723

3

TYPICAL CHARACTERISTICS

(V_{in} = 12 Vdc, V_O = 5.0 Vdc, I_L = 1.0 mAdc, R_{SC} = 0, T_A = +25°C unless otherwise noted.)

FIGURE 4 – MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

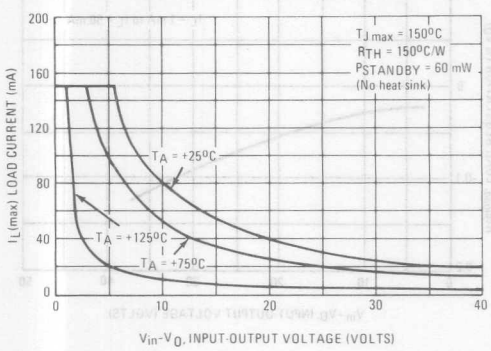


FIGURE 5 – LOAD REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING

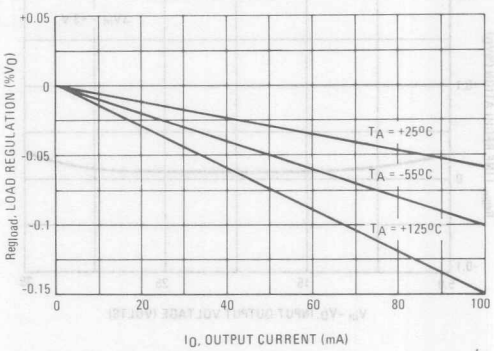


FIGURE 6 – LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING

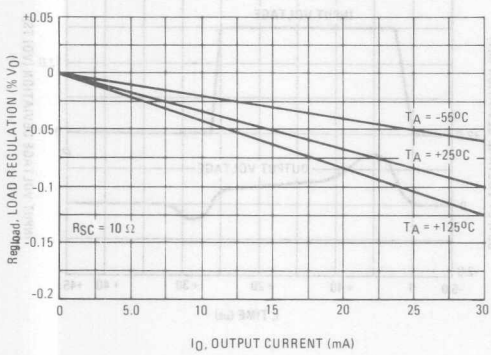


FIGURE 7 – LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING

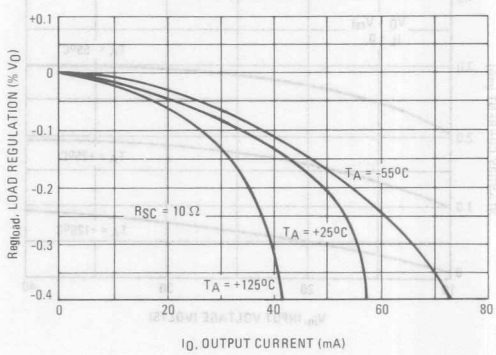


FIGURE 8 – CURRENT LIMITING CHARACTERISTICS

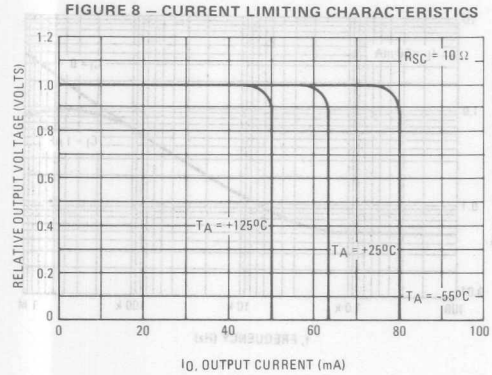
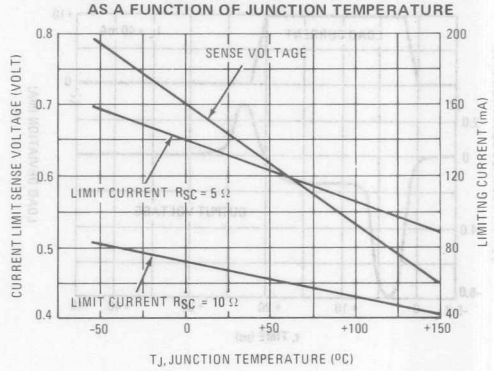


FIGURE 9 – CURRENT LIMITING CHARACTERISTICS AS A FUNCTION OF JUNCTION TEMPERATURE



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TYPICAL CHARACTERISTICS (continued)

FIGURE 10 – LINE REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

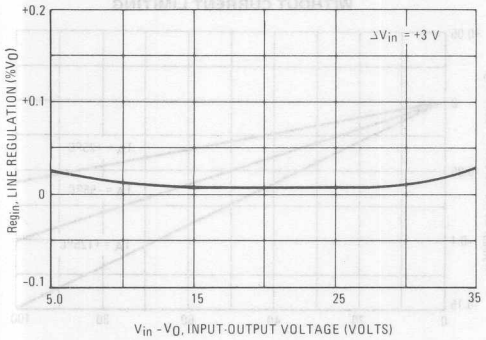


FIGURE 11 – LOAD REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

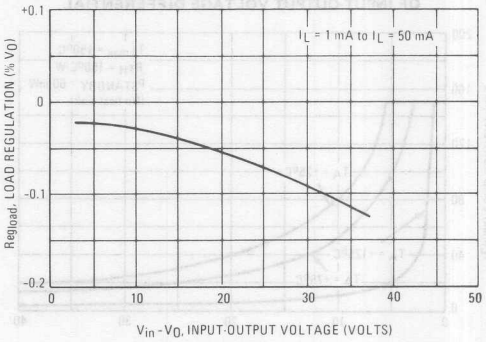


FIGURE 12 – STANDBY CURRENT DRAIN AS A FUNCTION OF INPUT VOLTAGE

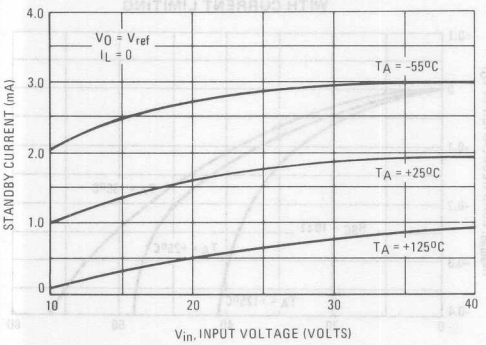


FIGURE 13 – LINE TRANSIENT RESPONSE

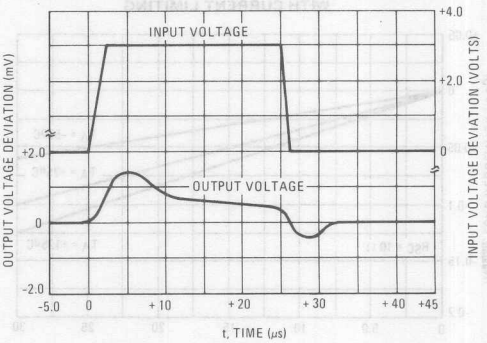


FIGURE 14 – LOAD TRANSIENT RESPONSE

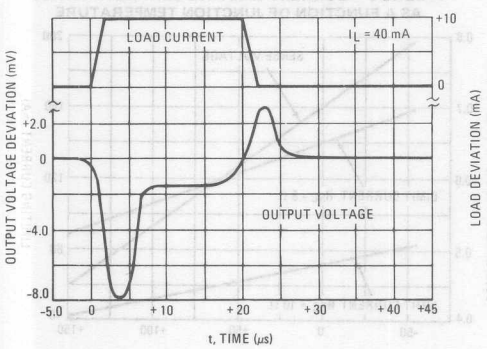
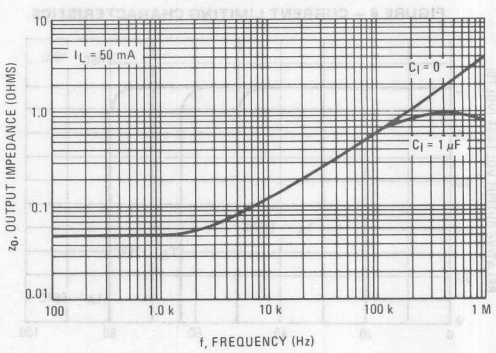


FIGURE 15 – OUTPUT IMPEDANCE AS FUNCTION OF FREQUENCY



TYPICAL APPLICATIONS

Pin numbers adjacent to terminals are for the metal package;
pin numbers in parenthesis are for the dual in-line packages.

FIGURE 16 – TYPICAL CONNECTION FOR $2 < V_O < 7$

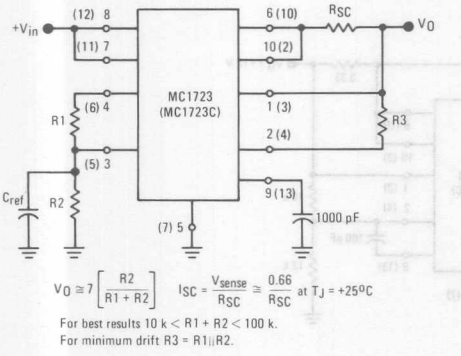


FIGURE 17 – MC1723,C FOLDBACK CONNECTION

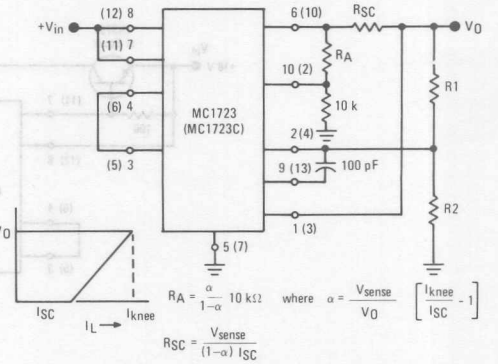


FIGURE 18 – +5 V, 1-AMPERE SWITCHING REGULATOR

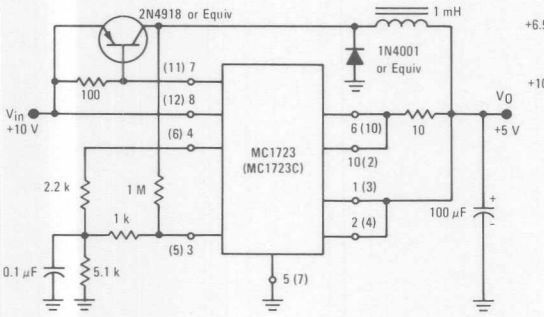


FIGURE 19 – +5 V, 1-AMPERE HIGH EFFICIENCY REGULATOR

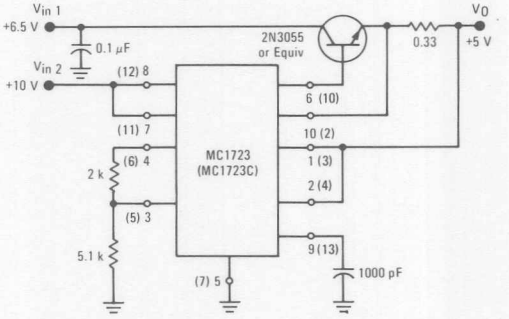


FIGURE 20 – +15 V, 1-AMPERE REGULATOR WITH REMOTE SENSE

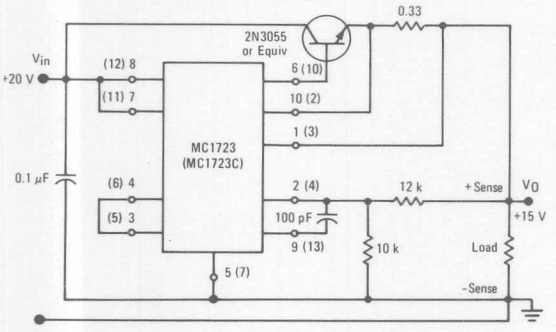


FIGURE 21 – -15 V NEGATIVE REGULATOR

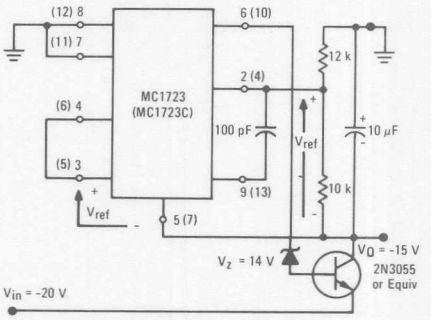
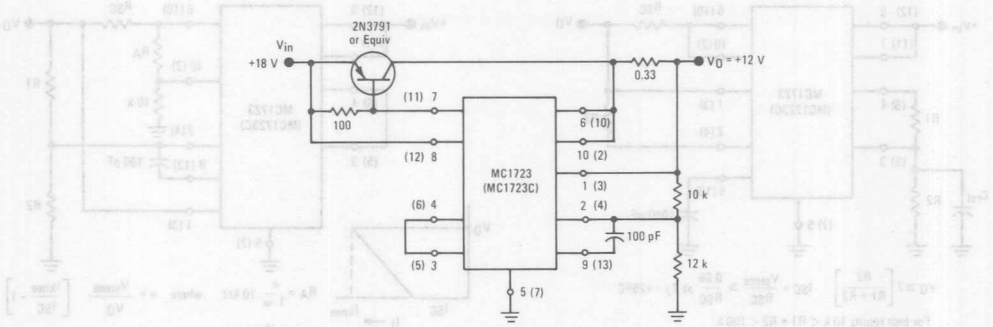


FIGURE 22 – +12 V, 1-AMPERE REGULATOR

USING PNP CURRENT BOOST



MOTOROLA

MC3423
MC3523

Specifications and Applications Information

OVERVOLTAGE SENSING CIRCUIT

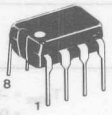
SILICON MONOLITHIC INTEGRATED CIRCUIT

OVERVOLTAGE "CROWBAR" SENSING CIRCUIT

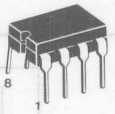
These overvoltage protection circuits (OVP) protect sensitive electronic circuitry from overvoltage transients or regulator failures when used in conjunction with an external "crowbar" SCR. They sense the overvoltage condition and quickly "crowbar" or short circuit the supply, forcing the supply into current limiting or opening the fuse or circuit breaker.

The protection voltage threshold is adjustable and the MC3423/3523 can be programmed for minimum duration of overvoltage condition before tripping, thus supplying noise immunity.

The MC3423/3523 is essentially a "two terminal" system, therefore it can be used with either positive or negative supplies.



P1 SUFFIX
PLASTIC PACKAGE
CASE 626-05
(MC3423 only)



U SUFFIX
CERAMIC PACKAGE
CASE 693-02

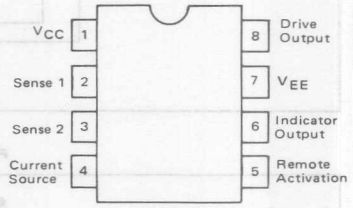


D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SO-8

MAXIMUM RATINGS

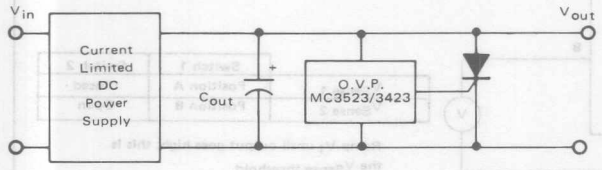
Rating	Symbol	Value	Unit
Differential Power Supply Voltage	V_{CC}-V_{EE}	40	Vdc
Sense Voltage (1)	$V_{Sense\ 1}$	6.5	Vdc
Sense Voltage (2)	$V_{Sense\ 2}$	6.5	Vdc
Remote Activation Input Voltage	V_{act}	7.0	Vdc
Output Current	I_O	300	mA
Operating Ambient Temperature Range MC3423 MC3523	T_A	 0 to +70 −55 to +125	°C
Operating Junction Temperature Plastic Package Ceramic Package	T_J	 125 150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

PIN CONNECTIONS



(Top View)

TYPICAL APPLICATION



ORDERING INFORMATION

Device	Temperature Range	Package
MC3423D	0 to +70°C	SO-8
MC3423P1		Plastic DIP
MC3423U		Ceramic DIP
MC3523U	−55 to +125°C	Ceramic DIP

3

ELECTRICAL CHARACTERISTICS ($5\ V \leq V_{CC} - V_{EE} \leq 36\ V$, $T_{low} < T_A < T_{high}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage Range	V_{CC}-V_{EE}	4.5	–	40	Vdc
Output Voltage (I_O = 100 mA)	V_O	V_{CC}-2.2	V_{CC}-1.8	–	Vdc
Indicator Output Voltage ($I_{O(Ind)}$ = 1.6 mA)	$V_{OL(Ind)}$	–	0.1	0.4	Vdc
Sense Trip Voltage (T_A = 25°C)	$V_{Sense\ 1}$, $V_{Sense\ 2}$	2.45	2.6	2.75	Vdc
Temperature Coefficient of $V_{Sense\ 1}$ (Figure 2)	TCV_{S1}	–	0.06	–	%/°C
Remote Activation Input Current (V_{IH} = 2.0 V, V_{CC}-V_{EE} = 5.0 V) (V_{IL} = 0.8 V, V_{CC}-V_{EE} = 5.0 V)	I_{IH} I_{IL}	– –	5.0 -120	40 -180	μA
Source Current	I_{Source}	0.1	0.2	0.3	mA
Output Current Risetime (T_A = 25°C)	t_r	–	400	–	mA/μs
Propagation Delay Time (T_A = 25°C)	t_{pd}	–	0.5	–	μs
Supply Current MC3423 MC3523	I_D	– –	6.0 5.0	10 7.0	mA

T_{low} = -55°C for MC3523
= 0°C for MC3423

T_{high} = +125°C for MC3523
= +70°C for MC3423

FIGURE 1 – BLOCK DIAGRAM

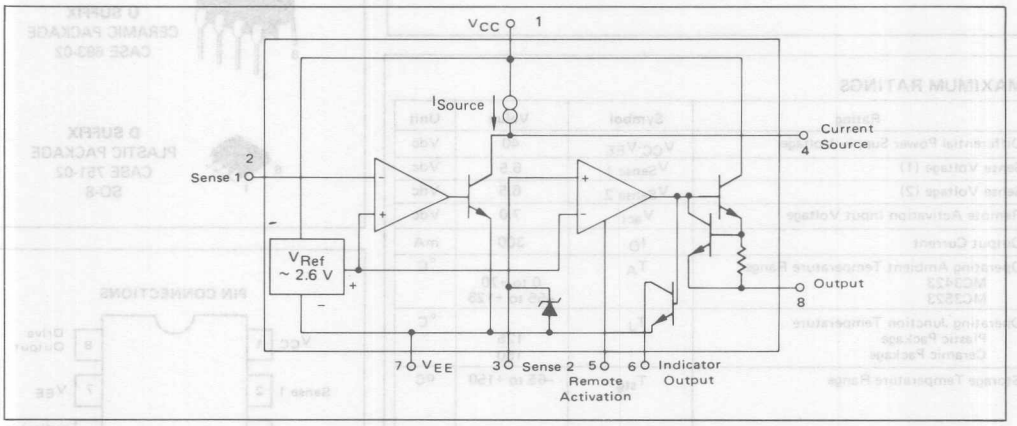
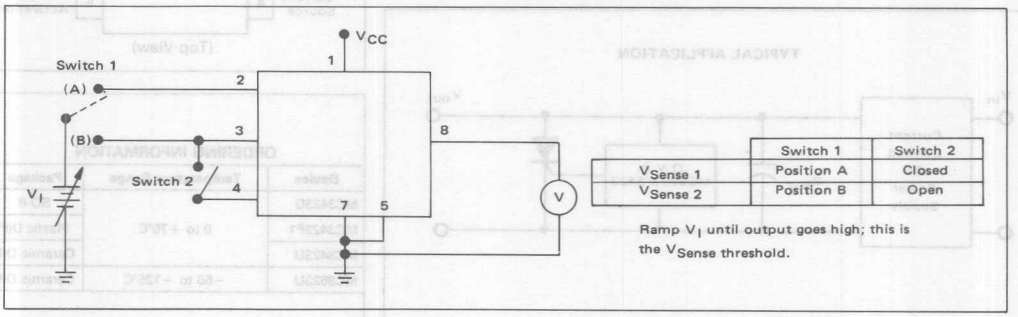


FIGURE 2 – SENSE VOLTAGE TEST CIRCUIT



	Switch 1	Switch 2
$V_{Sense\ 1}$	Position A	Closed
$V_{Sense\ 2}$	Position B	Open

Ramp V_I until output goes high; this is the V_{Sense} threshold.

FIGURE 3 – BASIC CIRCUIT CONFIGURATION

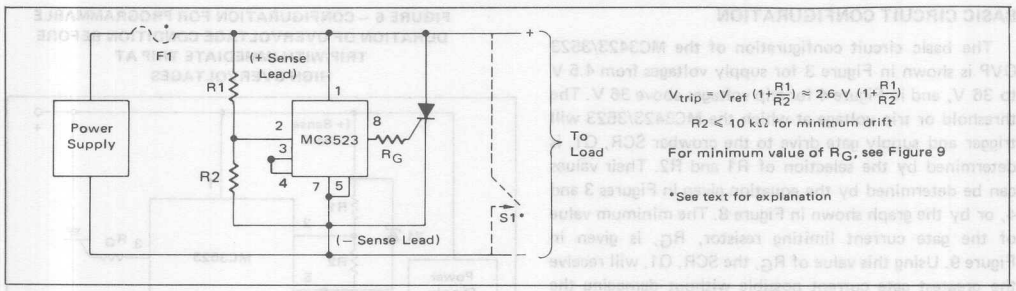


FIGURE 4 – CIRCUIT CONFIGURATION FOR SUPPLY VOLTAGE ABOVE 36 V

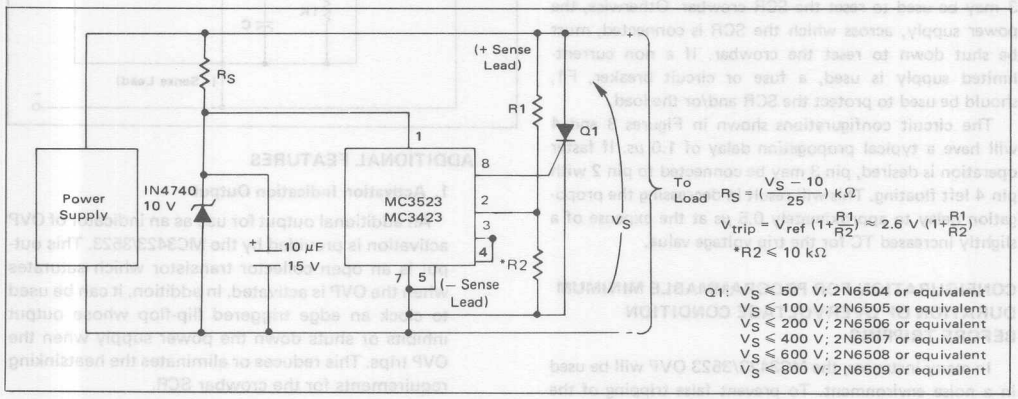
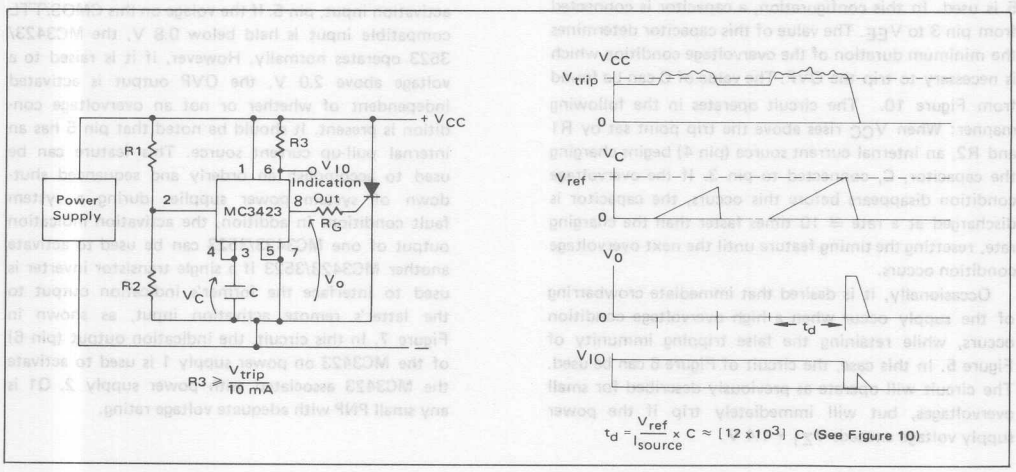


FIGURE 5 – BASIC CONFIGURATION FOR PROGRAMMABLE DURATION OF OVERVOLTAGE CONDITION BEFORE TRIP



BASIC CIRCUIT CONFIGURATION

The basic circuit configuration of the MC3423/3523 OVP is shown in Figure 3 for supply voltages from 4.5 V to 36 V, and in Figure 4 for trip voltages above 36 V. The threshold or trip voltage at which the MC3423/3523 will trigger and supply gate drive to the crowbar SCR, Q1, is determined by the selection of R1 and R2. Their values can be determined by the equation given in Figures 3 and 4, or by the graph shown in Figure 8. The minimum value of the gate current limiting resistor, R_G, is given in Figure 9. Using this value of R_G, the SCR, Q1, will receive the greatest gate current possible without damaging the MC3423/3523. If lower output currents are required, R_G can be increased in value. The switch, S1, shown in Figure 3 may be used to reset the SCR crowbar. Otherwise, the power supply, across which the SCR is connected, must be shut down to reset the crowbar. If a non current-limited supply is used, a fuse or circuit breaker, F1, should be used to protect the SCR and/or the load.

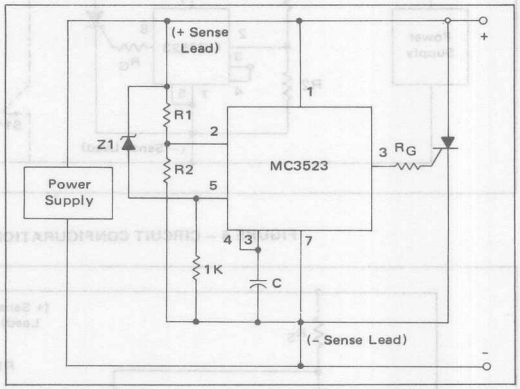
The circuit configurations shown in Figures 3 and 4 will have a typical propogation delay of 1.0 μs. If faster operation is desired, pin 3 may be connected to pin 2 with pin 4 left floating. This will result in decreasing the propogation delay to approximately 0.5 μs at the expense of a slightly increased TC for the trip voltage value.

CONFIGURATION FOR PROGRAMMABLE MINIMUM DURATION OF OVERVOLTAGE CONDITION BEFORE TRIPPING

In many instances, the MC3423/3523 OVP will be used in a noise environment. To prevent false tripping of the OVP circuit by noise which would not normally harm the load, MC3423/3523 has a programmable delay feature. To implement this feature, the circuit configuration of Figure 5 is used. In this configuration, a capacitor is connected from pin 3 to V_{EE}. The value of this capacitor determines the minimum duration of the overvoltage condition which is necessary to trip the OVP. The value of C can be found from Figure 10. The circuit operates in the following manner: When V_{CC} rises above the trip point set by R1 and R2, an internal current source (pin 4) begins charging the capacitor, C, connected to pin 3. If the overvoltage condition disappears before this occurs, the capacitor is discharged at a rate ≅ 10 times faster than the charging rate, resetting the timing feature until the next overvoltage condition occurs.

Occasionally, it is desired that immediate crowbarring of the supply occur when a high overvoltage condition occurs, while retaining the false tripping immunity of Figure 5. In this case, the circuit of Figure 6 can be used. The circuit will operate as previously described for small overvoltages, but will immediately trip if the power supply voltage exceeds V_{Z1} + 1.4 V.

FIGURE 6 – CONFIGURATION FOR PROGRAMMABLE DURATION OF OVERVOLTAGE CONDITION BEFORE TRIP/WITH IMMEDIATE TRIP AT HIGH OVERVOLTAGES



ADDITIONAL FEATURES

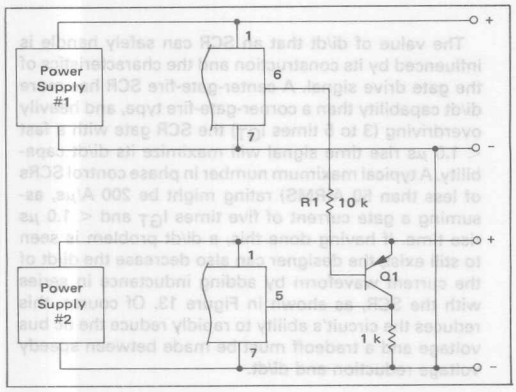
1. Activation Indication Output

An additional output for use as an indicator of OVP activation is provided by the MC3423/3523. This output is an open collector transistor which saturates when the OVP is activated. In addition, it can be used to clock an edge triggered flip-flop whose output inhibits or shuts down the power supply when the OVP trips. This reduces or eliminates the heatsinking requirements for the crowbar SCR.

2. Remote Activation Input

Another feature of the MC3423/3523 is its remote activation input, pin 5. If the volage on this CMOS/TTL compatible input is held below 0.8 V, the MC3423/3523 operates normally. However, if it is raised to a voltage above 2.0 V, the OVP output is activated independent of whether or not an overvoltage condition is present. It should be noted that pin 5 has an internal pull-up current source. This feature can be used to accomplish an orderly and sequenced shutdown of system power supplies during a system fault condition. In addition, the activation indication output of one MC3423/3523 can be used to activate another MC3423/3523 if a single transistor inverter is used to interface the former's indication output to the latter's remote activation input, as shown in Figure 7. In this circuit, the indication output (pin 6) of the MC3423 on power supply 1 is used to activate the MC3423 associated with power supply 2. Q1 is any small PNP with adequate voltage rating.

FIGURE 7 – CIRCUIT CONFIGURATION FOR ACTIVATING ONE MC3523 FROM ANOTHER



Note that both supplies have their negative output leads tied together (i.e., both are positive supplies). If their positive leads are common (two negative supplies) the emitter of Q1 would be moved to the positive lead of supply 1 and R1 would therefore have to be resized to deliver the appropriate drive to Q1.

CROWBAR SCR CONSIDERATIONS

Referring to Figure 11, it can be seen that the crowbar SCR, when activated, is subject to a large current surge from the output capacitance, C_{out}. This capacitance consists of the power supply output caps, the load's decoupling caps, and in the case of Figure 11A, the supply's input filter caps. This surge current is illustrated in Figure 12, and can cause SCR failure or degradation by any one of three mechanisms: di/dt, absolute peak surge, or I^2t. The interrelationship of these failure methods and the breadth of the applications make specification of the SCR by the semiconductor manufacturer difficult and expensive. Therefore, the designer must empirically determine the SCR and circuit elements which result in reliable and effective OVP operation. However, an understanding of the factors which influence the SCR's di/dt and surge capabilities simplifies this task.

1. di/dt

As the gate region of the SCR is driven on, its area of conduction takes a finite amount of time to grow, starting as a very small region and gradually spreading. Since the anode current flows through this turned-on gate region, very high current densities can occur in the gate region if high anode currents appear quickly (di/dt). This can result in immediate destruction of the SCR or gradual degradation of its forward blocking voltage capabilities – depending on the severity of the occasion.

FIGURE 8 – R1 versus TRIP VOLTAGE

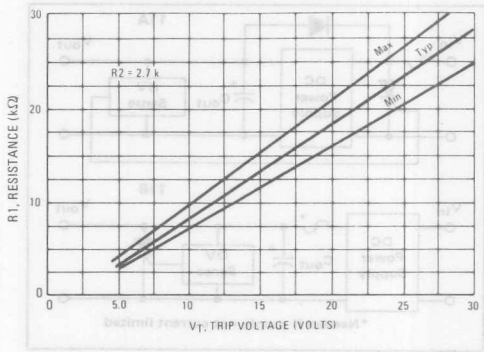


FIGURE 9 – MINIMUM R_G versus SUPPLY VOLTAGE

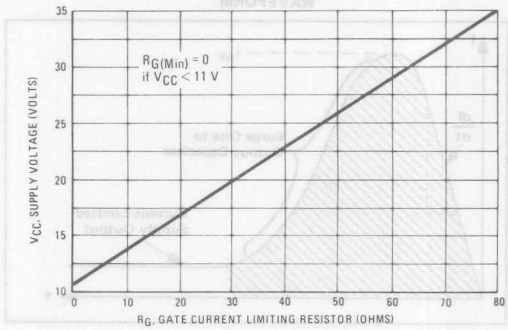
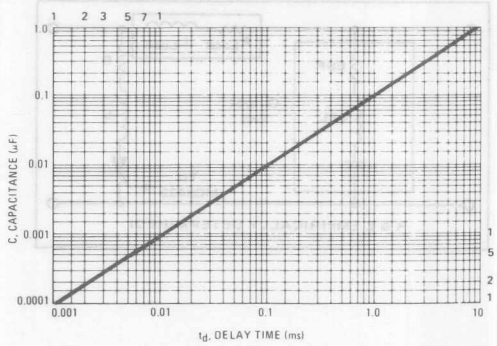


FIGURE 10 – CAPACITANCE versus MINIMUM OVERVOLTAGE DURATION



3

FIGURE 11 – TYPICAL CROWBAR OVP CIRCUIT CONFIGURATIONS

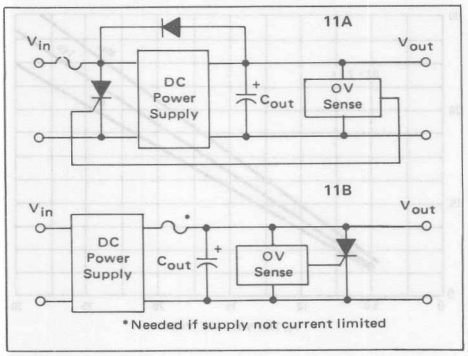


FIGURE 12 – CROWBAR SCR SURGE CURRENT WAVEFORM

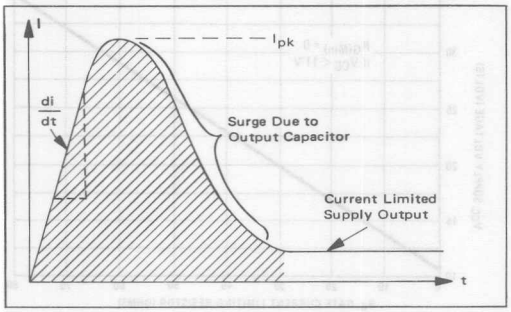
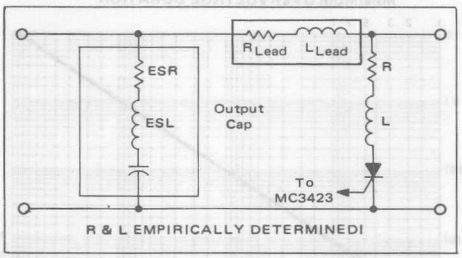


FIGURE 13 – CIRCUIT ELEMENTS AFFECTING SCR SURGE & di/dt



The value of di/dt that an SCR can safely handle is influenced by its construction and the characteristics of the gate drive signal. A center-gate-fire SCR has more di/dt capability than a corner-gate-fire type, and heavily overdriving (3 to 5 times I_{GT}) the SCR gate with a fast $< 1.0\ \mu s$ rise time signal will maximize its di/dt capability. A typical maximum number in phase control SCRs of less than 50 A(RMS) rating might be 200 A/μs, assuming a gate current of five times I_{GT} and $< 1.0\ \mu s$ rise time. If having done this, a di/dt problem is seen to still exist, the designer can also decrease the di/dt of the current waveform by adding inductance in series with the SCR, as shown in Figure 13. Of course, this reduces the circuit's ability to rapidly reduce the dc bus voltage and a tradeoff must be made between speedy voltage reduction and di/dt.

2. Surge Current

If the peak current and/or the duration of the surge is excessive, immediate destruction due to device overheating will result. The surge capability of the SCR is directly proportional to its die area. If the surge current cannot be reduced (by adding series resistance — see Figure 13) to a safe level which is consistent with the system's requirements for speedy bus voltage reduction, the designer must use a higher current SCR. This may result in the average current capability of the SCR exceeding the steady state current requirements imposed by the dc power supply.

A WORD ABOUT FUSING

Before leaving the subject of the crowbar SCR, a few words about fuse protection are in order. Referring back to Figure 11A, it will be seen that a fuse is necessary if the power supply to be protected is not output current limited. This fuse is not meant to prevent SCR failure but rather to prevent a fire!

In order to protect the SCR, the fuse would have to possess an I^2t rating less than that of the SCR and yet have a high enough continuous current rating to survive normal supply output currents. In addition, it must be capable of successfully clearing the high short circuit currents from the supply. Such a fuse as this is quite expensive, and may not even be available.

The usual design compromise then is to use a garden variety fuse (3AG or 3AB style) which cannot be relied on to blow before the thyristor does, and trust that if the SCR does fail, it will fail short circuit. In the majority of the designs, this will be the case, though this is difficult to guarantee. Of course, a sufficiently high surge will cause an open. These comments also apply to the fuse in Figure 11B.

For a complete and detailed treatment of SCR and fuse selection, refer to Motorola Application Note AN-789.

CROWBAR SCR SELECTION GUIDE

As an aid in selecting an SCR for crowbar use, the following selection guide is presented.

DEVICE	I_{RMS}	I_{FSM}	PACKAGE
2N6400 Series	16A	160A	TO220 Plastic
2N6504 Series	25A	160A	TO220 Plastic
2N1842 Series	16A	125A	Metal Stud
2N2573 Series	25A	260A	Metal TO-3 Type
2N681 Series	25A	200A	Metal Stud
MCR3935-1 Series	35A	350A	Metal Stud
MCR81-5 Series	80A	1000A	Metal Stud

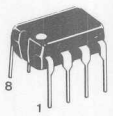
POWER SUPPLY SUPERVISORY/OVER-UNDER-VOLTAGE PROTECTION CIRCUIT

The MC3425 is a power supply supervisory circuit containing all the necessary functions required to monitor over- and under-voltage fault conditions. These integrated circuits contain dedicated over- and under-voltage sensing channels with independently programmable time delays. The over-voltage channel has a high current Drive Output for use in conjunction with an external SCR "Crowbar" for shutdown. The under-voltage channel input comparator has hysteresis which is externally programmable, and an open-collector output for fault indication.

- Dedicated Over- And Under-Voltage Sensing
- Programmable Hysteresis Of Under-Voltage Comparator
- Internal 2.5 V Reference
- 300 mA Over-Voltage Drive Output
- 30 mA Under-Voltage Indicator Output
- Programmable Time Delays
- 4.5 V to 40 V Operation

POWER SUPPLY SUPERVISORY/ OVER-UNDER-VOLTAGE PROTECTION CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT



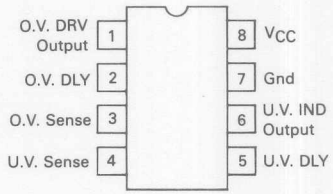
P1 SUFFIX
PLASTIC PACKAGE
CASE 626-05

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	Vdc
Comparator Input Voltage Range (Note 1)	V_{IR}	−0.3 to +40	Vdc
Drive Output Short-Circuit Current	$I_{OS(DRV)}$	Internally Limited	mA
Indicator Output Voltage	V_{IND}	0 to 40	Vdc
Indicator Output Sink Current	I_{IND}	30	mA
Power Dissipation and Thermal Characteristics Maximum Power Dissipation @ T_A = 70°C Thermal Resistance Junction to Air	 P_D $R_{\theta JA}$	 1000 80	 mW °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

NOTE: (1) The input signal voltage should not be allowed to go negative by more than 300 mV or positive by more than 40 V, independent of V_{CC}, without device destruction.

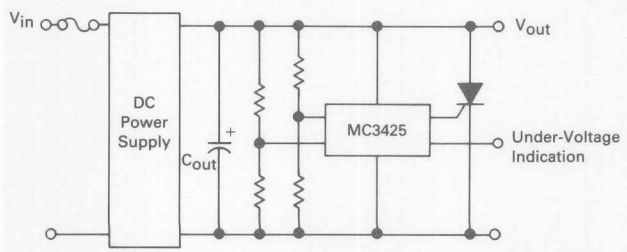
PIN CONNECTIONS



(Top View)

TYPICAL APPLICATION

Over-Voltage Crowbar Protection, Under-Voltage Indication



ORDERING INFORMATION

Device	Temperature Range	Package
MC3425P1	0 to +70°C	Plastic DIP

ELECTRICAL CHARACTERISTICS ($4.5\ V \leq V_{CC} \leq 40\ V$; $T_A = T_{low}$ to T_{high} [see Note 2] unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Sense Trip Voltage (Reference Voltage) V_{CC} = 15 V T_A = 25°C T_{low} to T_{high} (Note 2)	V_{Sense}	 2.4 2.33	 2.5 2.5	 2.6 2.63	Vdc
Line Regulation of V_{Sense} $4.5\ V \leq V_{CC} \leq 40\ V$; T_J = 25°C	Reg_{line}	—	7.0	15	mV
Power Supply Voltage Operating Range	V_{CC}	4.5	—	40	Vdc
Power Supply Current V_{CC} = 40 V; T_A = 25°C; No Output Loads O.V. Sense (Pin 3) = 0 V; U.V. Sense (Pin 4) = V_{CC}	$I_{CC(off)}$	—	8.5	10	mA
O.V. Sense (Pin 3) = V_{CC}; U.V. Sense (Pin 4) = 0 V	$I_{CC(on)}$	—	16.5	19	mA
INPUT SECTION					
Input Bias Current, O.V. and U.V. Sense	I_{IB}	—	1.0	2.0	μA
Hysteresis Activation Voltage, U.V. Sense V_{CC} = 15 V; T_A = 25°C; I_H = 10% I_H = 90%	$V_{H(act)}$	 — —	 0.6 0.8	 — —	V
Hysteresis Current, U.V. Sense V_{CC} = 15 V; T_A = 25°C; U.V. Sense (Pin 4) = 2.5 V	I_H	9.0	12.5	16	μA
Delay Pin Voltage (I_{DLY} = 0 mA) Low State High State	 $V_{OL(DLY)}$ $V_{OH(DLY)}$	 — $V_{CC}-0.5$	 0.2 $V_{CC}-0.15$	 0.5 —	V
Delay Pin Source Current V_{CC} = 15 V; V_{DLY} = 0 V	$I_{DLY(source)}$	140	200	260	μA
Delay Pin Sink Current V_{CC} = 15 V; V_{DLY} = 2.5 V	$I_{DLY(sink)}$	1.8	3.0	—	mA
OUTPUT SECTION					
Drive Output Peak Current (T_A = 25°C)	$I_{DRV(peak)}$	200	300	—	mA
Drive Output Voltage I_{DRV} = 100 mA; T_A = 25°C	$V_{OH(DRV)}$	$V_{CC}-2.5$	$V_{CC}-2.0$	—	V
Drive Output Leakage Current V_{DRV} = 0 V	$I_{DRV(leak)}$	—	15	200	nA
Drive Output Current Slew Rate (T_A = 25°C)	di/dt	—	2.0	—	A/μs
Drive Output V_{CC} Transient Rejection V_{CC} = 0 V to 15 V at dV/dt = 200 V/μs; O.V. Sense (Pin 3) = 0 V; T_A = 25°C	$I_{DRV(trans)}$	—	1.0	—	mA (Peak)
Indicator Output Saturation Voltage I_{IND} = 30 mA; T_A = 25°C	$V_{IND(sat)}$	—	560	800	mV
Indicator Output Leakage Current $V_{OH(IND)}$ = 40 V	$I_{IND(leak)}$	—	25	200	nA
Output Comparator Threshold Voltage (Note 3)	$V_{th(OC)}$	2.33	2.5	2.63	V
Propagation Delay Time (V_{CC} = 15 V; T_A = 25°C) Input to Drive Output or Indicator Output 100 mV Overdrive, C_{DLY} = 0 μF	$t_{PLH(IN/OUT)}$	—	1.7	—	μs
Input to Delay 2.5 V Overdrive (0 V to 5.0 V Step)	$t_{PLH(IN/DLY)}$	—	700	—	ns

NOTES:
(2) T_{low} = 0°C T_{high} = +70°C
(3) The $V_{th(OC)}$ limits are approximately the V_{Sense} limits over the applicable temperature range.

3

FIGURE 1 — HYSTERESIS CURRENT versus HYSTERESIS ACTIVATION VOLTAGE

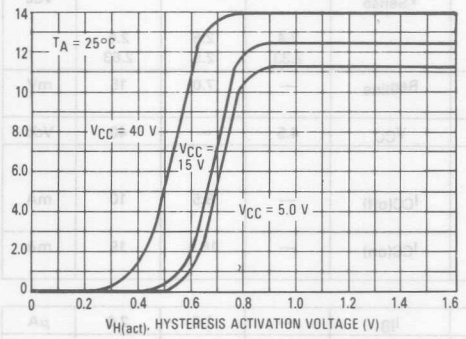


FIGURE 2 — HYSTERESIS ACTIVATION VOLTAGE versus TEMPERATURE

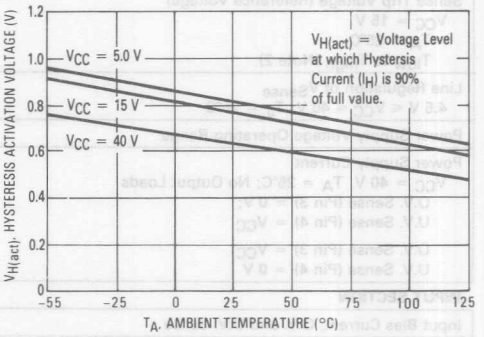


FIGURE 3 — HYSTERESIS CURRENT versus TEMPERATURE

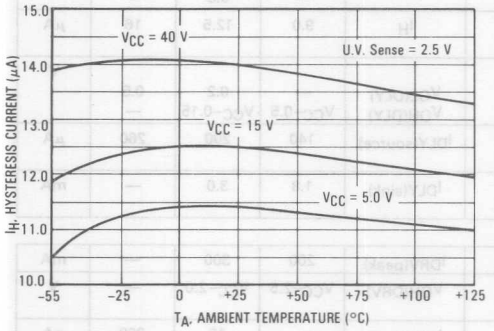


FIGURE 4 — SENSE TRIP VOLTAGE CHANGE versus TEMPERATURE

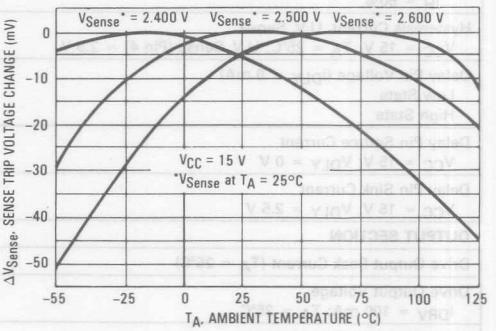


FIGURE 5 — OUTPUT DELAY TIME versus DELAY CAPACITANCE

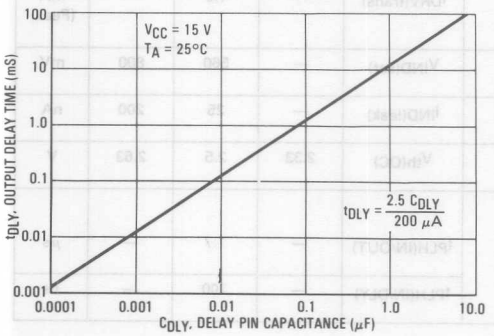


FIGURE 6 — DELAY PIN SOURCE CURRENT versus TEMPERATURE

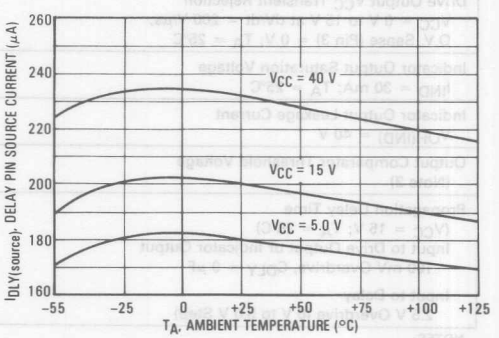


FIGURE 7 — DRIVE OUTPUT SATURATION VOLTAGE versus OUTPUT PEAK CURRENT

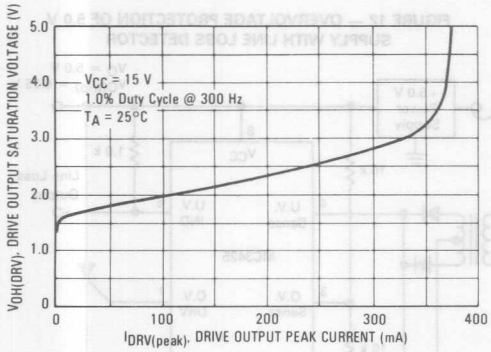


FIGURE 8 — INDICATOR OUTPUT SATURATION VOLTAGE versus OUTPUT SINK CURRENT

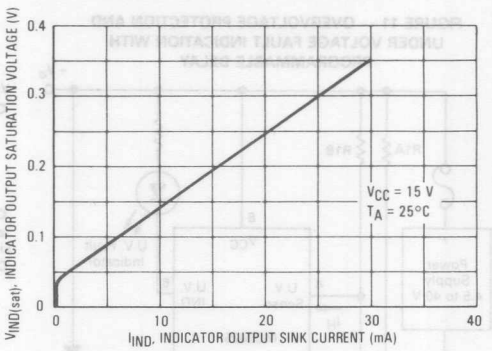


FIGURE 9 — DRIVE OUTPUT SATURATION VOLTAGE versus TEMPERATURE

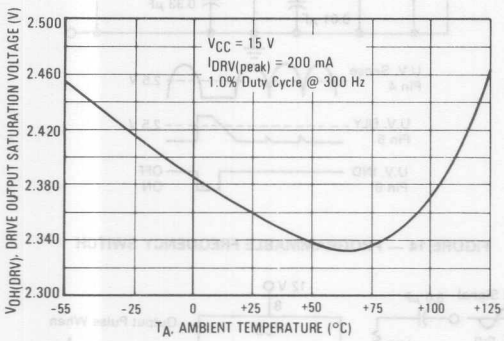


FIGURE 10 — POWER SUPPLY CURRENT versus VOLTAGE

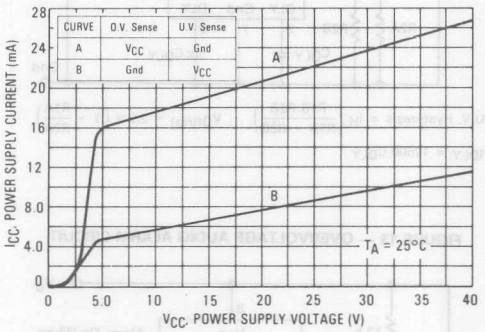
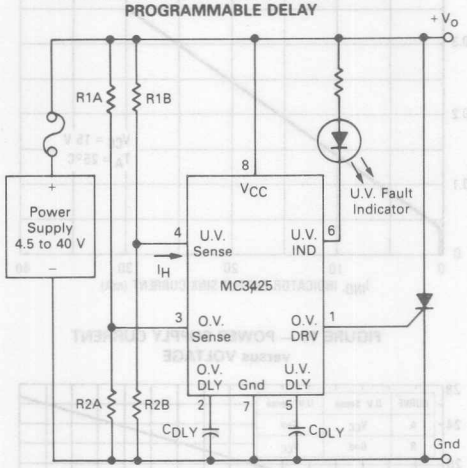


FIGURE 11 — OVERVOLTAGE PROTECTION AND UNDER VOLTAGE FAULT INDICATION WITH PROGRAMMABLE DELAY



$$\text{U.V. Hysteresis} = I_H\left(\frac{R1B\ R2B}{R1B + R2B}\right) \qquad V_{O(trip)} = 2.5\ V\left(1 + \frac{R1A}{R2A}\right)$$

$$t_{DLY} = 12500\ C_{DLY}$$

FIGURE 12 — OVERVOLTAGE PROTECTION OF 5.0 V SUPPLY WITH LINE LOSS DETECTOR

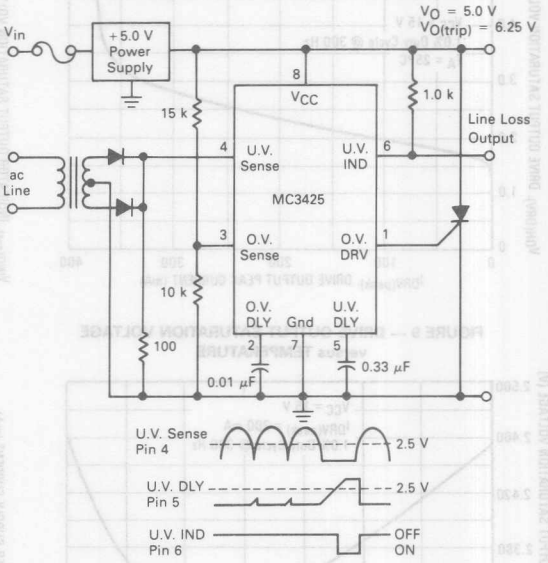


FIGURE 13 — OVERVOLTAGE AUDIO ALARM CIRCUIT

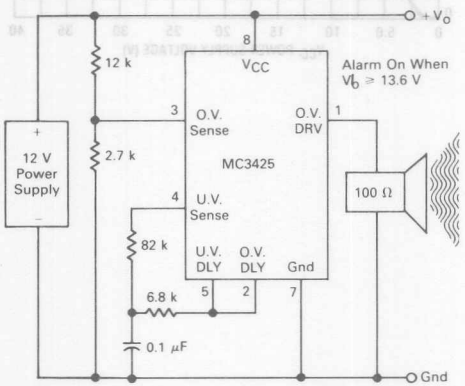
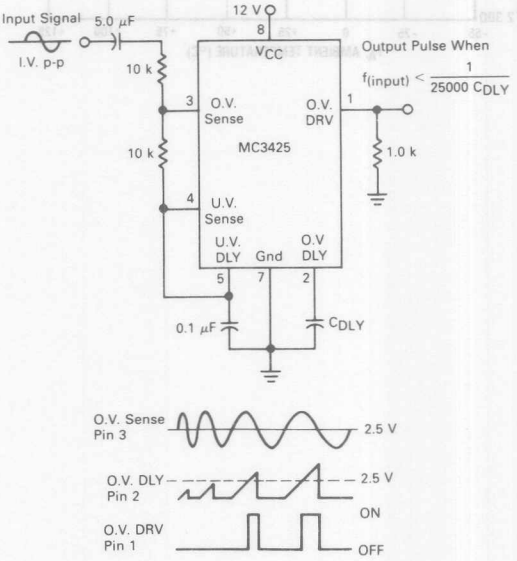


FIGURE 14 — PROGRAMMABLE FREQUENCY SWITCH



CIRCUIT DESCRIPTION

The MC3425 is a power supply supervisory circuit containing all the necessary functions required to monitor over- and under-voltage fault conditions. The block diagram is shown below in Figure 15. The Over-Voltage (O.V.) and Under-Voltage (U.V.) Input Comparators are both referenced to an internal 2.5 V regulator. The U.V. Input Comparator has a feedback activated 12.5 μA current sink (I_H) which is used for programming the input hysteresis voltage (V_H). The source resistance feeding this input (R_H) determines the amount of hysteresis voltage by $V_H = I_H R_H = 12.5 \times 10^{-6} R_H$.

Separate Delay pins (O.V. DLY, U.V. DLY) are provided for each channel to independently delay the Drive and Indicator outputs, thus providing greater input noise immunity. The two Delay pins are essentially the outputs of the respective input comparators, and provide a constant current source, $I_{DLY(source)}$, of typically 200 μA when the non-inverting input voltage is greater than the inverting input level. A capacitor connected from these Delay pins to ground, will establish a predictable delay time (t_{DLY}) for the Drive and Indicator outputs. The Delay pins are internally connected to the non-inverting inputs of the O.V. and U.V. Output Comparators, which are referenced to the internal 2.5 V regulator. Therefore, delay time (t_{DLY}) is based on the constant current source, $I_{DLY(source)}$, charging the external delay capacitor (C_{DLY}) to 2.5 volts.

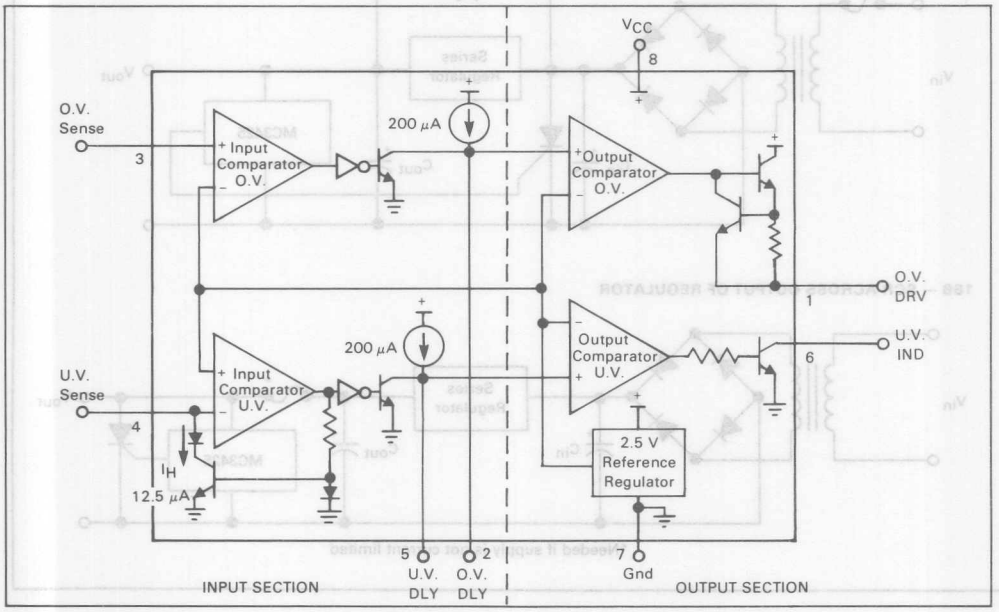
$$t_{DLY} = \frac{V_{ref}\, C_{DLY}}{I_{DLY(source)}} = \frac{2.5\, C_{DLY}}{200\ \mu A} = 12500\, C_{DLY}$$

Figure 5 provides C_{DLY} values for a wide range of time delays. The Delay pins are pulled low when the respective input comparator's non-inverting input is less than the inverting input. The sink current, $I_{DLY(sink)}$, capability of the Delay pins is $\geq$ 1.8 mA and is much greater than the typical 200 μA source current, thus enabling a relatively fast delay capacitor discharge time.

The Over-Voltage Drive Output is a current-limited emitter-follower capable of sourcing 300 mA at a turn-on slew rate of 2.0 A/μs, ideal for driving "Crowbar" SCR's. The Under-Voltage Indicator Output is an open-collector, NPN transistor, capable of sinking 30 mA to provide sufficient drive for LED's, small relays or shut-down circuitry. These current capabilities apply to both channels operating simultaneously, providing device power dissipation limits are not exceeded.

The MC3425 has an internal 2.5 V bandgap reference regulator with an accuracy of $\pm$4.0% for the basic devices and $\pm$1.0% for the A-suffix device types at 25°C. The reference has a typical temperature coefficient of 30 ppm/°C for A-suffix devices.

FIGURE 15 — BLOCK DIAGRAM



Note: All voltages and currents are nominal.

3

CROWBAR SCR CONSIDERATIONS

Referring to Figure 16, it can be seen that the crowbar SCR, when activated, is subject to a large current surge from the output capacitance, C_{out}. This capacitance consists of the power supply output capacitors, the load's decoupling capacitors, and in the case of Figure 16A, the supply's input filter capacitors. This surge current is illustrated in Figure 17, and can cause SCR failure or degradation by any one of three mechanisms: di/dt, absolute peak surge, or I^2t. The interrelationship of these failure methods and the breadth of the applications make specification of the SCR by the semiconductor manufacturer difficult and expensive. Therefore, the designer must empirically determine the SCR and circuit elements which result in reliable and effective OVP operation. However, an understanding of the factors which influence the SCR's di/dt and surge capabilities simplifies this task.

1. di/dt

As the gate region of the SCR is driven on, its area of conduction takes a finite amount of time to grow, starting as a very small region and gradually spreading. Since the anode current flows through this turned-on gate region, very high current densities can occur in the gate region if high anode currents appear quickly (di/dt). This can result in immediate destruction of the SCR or gradual degradation of its forward blocking voltage capabilities — depending on the severity of the occasion.

The value of di/dt that an SCR can safely handle is influenced by its construction and the characteristics of the gate drive signal. A center-gate-fire SCR has more di/dt capability than a corner-gate-fire type, and heavily overdriving (3 to 5 times I_{GT}) the SCR gate with a fast $<1.0\ \mu s$ rise time signal will maximize its di/dt capability. A typical maximum number in phase control SCRs of less than 50 A(RMS) rating might be 200 $A/\mu s$, assuming a gate current of five times I_{GT} and $<1.0\ \mu s$ rise time. If having done this, a di/dt problem is seen to still exist, the designer can also decrease the di/dt of the current waveform by adding inductance in series with the SCR, as shown in Figure 18. Of course, this reduces the circuit's ability to rapidly reduce the dc bus voltage and a tradeoff must be made between speedy voltage reduction and di/dt.

FIGURE 16 — TYPICAL CROWBAR CIRCUIT CONFIGURATIONS

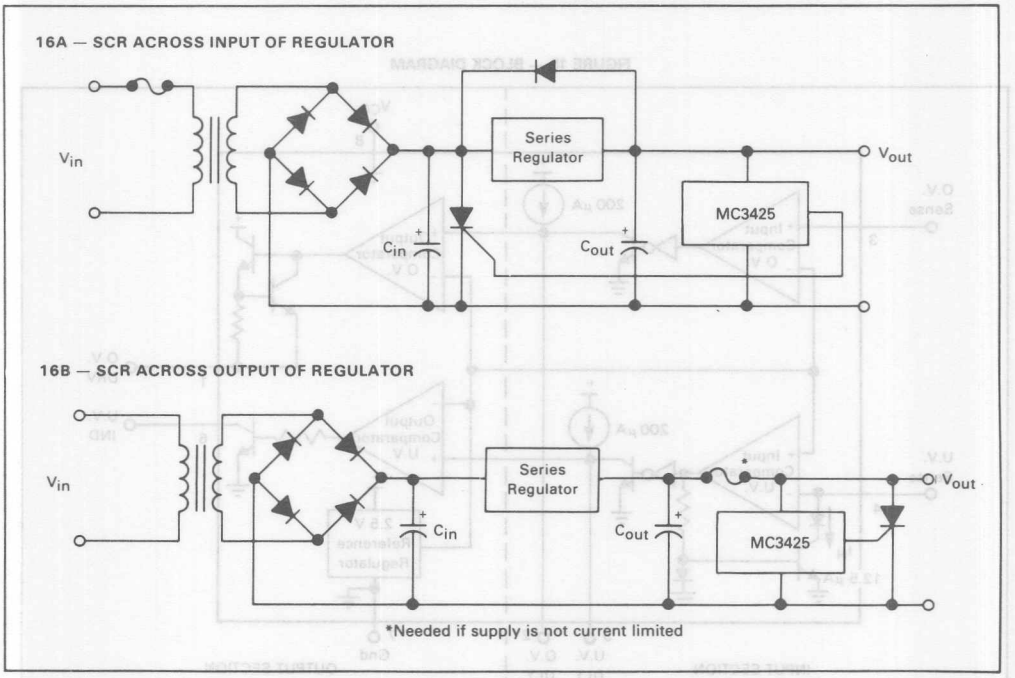
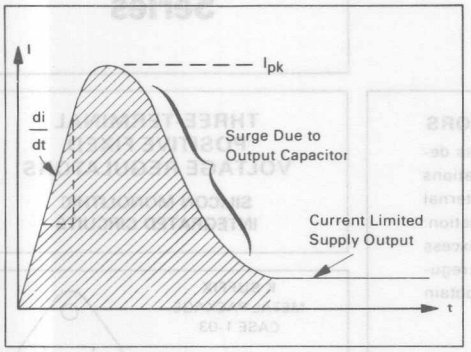


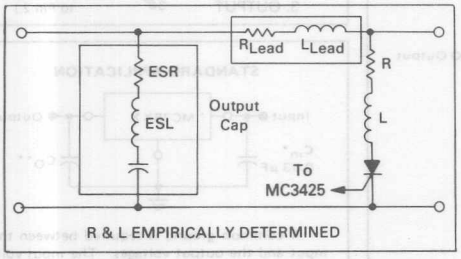
FIGURE 17 — CROWBAR SCR SURGE CURRENT WAVEFORM



2. Surge Current

If the peak current and/or the duration of the surge is excessive, immediate destruction due to device overheating will result. The surge capability of the SCR is directly proportional to its die area. If the surge current cannot be reduced (by adding series resistance — see Figure 18) to a safe level which is consistent with the system's requirements for speedy bus voltage reduction, the designer must use a higher current SCR. This may result in the average current capability of the SCR exceeding the steady state current requirements imposed by the dc power supply.

FIGURE 18 — CIRCUIT ELEMENTS AFFECTING SCR SURGE & di/dt



A WORD ABOUT FUSING

Before leaving the subject of the crowbar SCR, a few words about fuse protection are in order. Referring back to Figure 16A, it will be seen that a fuse is necessary if the power supply to be protected is not output current limited. This fuse is not meant to prevent SCR failure but rather to prevent a fire!

In order to protect the SCR, the fuse would have to possess an I^2t rating less than that of the SCR and yet have a high enough continuous current rating to survive normal supply output currents. In addition, it must be capable of successfully clearing the high short circuit currents from the supply. Such a fuse as this is quite expensive, and may not even be available.

The usual design compromise then is to use a garden variety fuse (3AG or 3AB style) which cannot be relied on to blow before the thyristor does, and trust that if the SCR does fail, it will fail short circuit. In the majority of the designs, this will be the case, though this is difficult to guarantee. Of course, a sufficiently high surge will cause an open. These comments also apply to the fuse in Figure 16B.

CROWBAR SCR SELECTION GUIDE

As an aid in selecting an SCR for crowbar use, the following selection guide is presented.

DEVICE	I_{RMS}	I_{FSM}	PACKAGE
MCR67 Series	12 A	100 A	Metal Stud
MCR68 Series	12 A	100 A	TO-220 Plastic
2N1842 Series	16 A	125 A	Metal Stud
2N6400 Series	16 A	160 A	TO-220 Plastic
2N6504 Series	25 A	160 A	TO-220 Plastic
2N681 Series	25 A	200 A	Metal Stud
2N2573 Series	25 A	260 A	TO-3 Metal Can
MCR69 Series	25 A	300 A	TO-220 Plastic
MCR70 Series	35 A	350 A	Metal Stud
MCR71 Series	55 A	550 A	Metal Stud

For a complete and detailed treatment of SCR and fuse selection refer to Motorola Application Note AN789.

Series

3

THREE-TERMINAL POSITIVE VOLTAGE REGULATORS

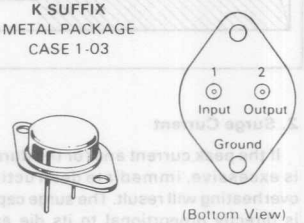
These voltage regulators are monolithic integrated circuits designed as fixed-voltage regulators for a wide variety of applications including local, on-card regulation. These regulators employ internal current limiting, thermal shutdown, and safe-area compensation. With adequate heatsinking they can deliver output currents in excess of 1.0 ampere. Although designed primarily as a fixed voltage regulator, these devices can be used with external components to obtain adjustable voltages and currents.

- Output Current in Excess of 1.0 Ampere
- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Output Voltage Offered in 2% and 4% Tolerance

THREE-TERMINAL POSITIVE FIXED VOLTAGE REGULATORS

SILICON MONOLITHIC INTEGRATED CIRCUITS

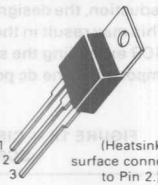
K SUFFIX
METAL PACKAGE
CASE 1-03



(Bottom View)

Pins 1 and 2 electrically isolated from case. Case is third electrical connection

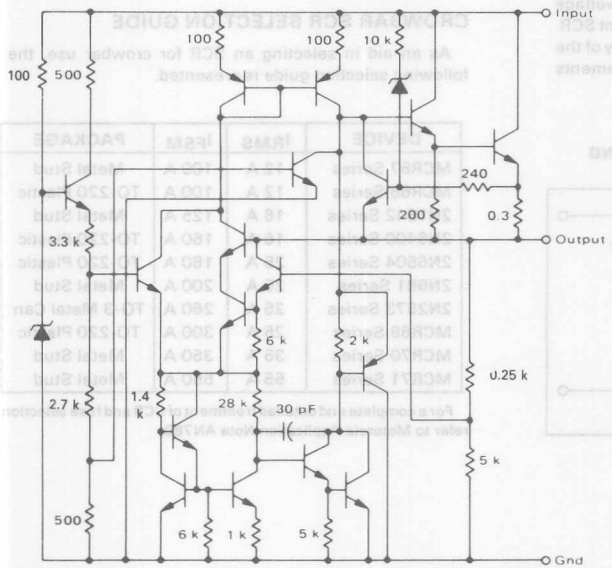
T SUFFIX
PLASTIC PACKAGE
CASE 221A-04



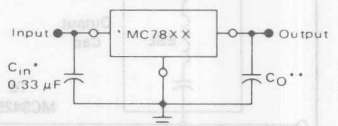
PIN 1. INPUT
2. GROUND
3. OUTPUT

(Heatsink surface connected to Pin 2.)

REPRESENTATIVE SCHEMATIC DIAGRAM



STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O is not needed for stability; however, it does improve transient response.

XX indicates nominal voltage

ORDERING INFORMATION

Device	Output Voltage Tolerance	Tested Operating Junction Temp. Range	Package
MC78XXK MC78XXAK*	4% 2%	−55 to +150°C	Metal Power
MC78XXCK MC78XXACK*	4% 2%	0 to +125°C	Metal Power
MC78XXCT MC78XXACT	4% 2%	0 to +125°C	Plastic Power
MC78XXBT	4%	−40 to +125°C	Plastic Power

*2% regulators in Metal Power packages are available in 5, 12 and 15 volt devices.

TYPE NO./VOLTAGE			
MC7805	5.0 Volts	MC7812	12 Volts
MC7806	6.0 Volts	MC7815	15 Volts
MC7808	8.0 Volts	MC7818	18 Volts
MC7809	9.0 Volts	MC7824	24 Volts

Rating		Symbol	Value	Unit
Input Voltage (5.0 V – 18 V) (24 V)		V_{in}	35 40	Vdc
Power Dissipation and Thermal Characteristics				
Plastic Package				
T_A = +25°C		P_D	Internally Limited	Watts
Derate above T_A = +25°C		$1/\theta_{JA}$	15.4	mW/°C
Thermal Resistance, Junction to Air		θ_{JA}	65	°C/W
T_C = +25°C		P_D	Internally Limited	Watts
Derate above T_C = +75°C (See Figure 1)		$1/\theta_{JC}$	200	mW/°C
Thermal Resistance, Junction to Case		θ_{JC}	5.0	°C/W
Metal Package				
T_A = +25°C		P_D	Internally Limited	Watts
Derate above T_A = +25°C		$1/\theta_{JA}$	22.5	mW/°C
Thermal Resistance, Junction to Air		θ_{JA}	45	°C/W
T_C = +25°C		P_D	Internally Limited	Watts
Derate above T_C = +65°C (See Figure 2)		$1/\theta_{JC}$	182	mW/°C
Thermal Resistance, Junction to Case		θ_{JC}	5.5	°C/W
Storage Junction Temperature Range		T_{stg}	–65 to +150	°C
Operating Junction Temperature Range		T_J		°C
	MC7800,A		–55 to +150	
	MC7800C,AC		0 to +150	
	MC7800B		–40 to +150	

DEFINITIONS

Line Regulation — The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation — The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation — The maximum total device dissipation for which the regulator will operate within specifications.

Quiescent Current — That part of the input current that is not delivered to the load.

Output Noise Voltage — The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long Term Stability — Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices' electrical characteristics and maximum power dissipation.

MC7805, B, C

ELECTRICAL CHARACTERISTICS (V_{in} = 10 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1] unless otherwise noted).

Characteristic	Symbol	MC7805			MC7805B			MC7805C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	4.8	5.0	5.2	4.8	5.0	5.2	4.8	5.0	5.2	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W) 7.0 Vdc ≤ V_{in} ≤ 20 Vdc 8.0 Vdc ≤ V_{in} ≤ 20 Vdc	V_O	— 4.65	— 5.0	— 5.35	— 4.75	— 5.0	— 5.25	4.75 —	5.0 —	5.25 —	Vdc
Line Regulation (T_J = +25°C, Note 2) 7.0 Vdc ≤ V_{in} ≤ 25 Vdc 8.0 Vdc ≤ V_{in} ≤ 12 Vdc	Reg_{line}	— —	2.0 1.0	50 25	— —	7.0 2.0	100 50	— —	7.0 2.0	100 50	mV
Load Regulation (T_J = +25°C, Note 2) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	— —	25 8.0	100 25	— —	40 15	100 50	— —	40 15	100 50	mV
Quiescent Current (T_J = +25°C)	I_B	—	3.2	6.0	—	4.3	8.0	—	4.3	8.0	mA
Quiescent Current Change 7.0 Vdc ≤ V_{in} ≤ 25 Vdc 8.0 Vdc ≤ V_{in} ≤ 25 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	— — —	— 0.3 0.04	— 0.8 0.5	— — —	— — —	— 1.3 0.5	— — —	— — —	1.3 — 0.5	mA
Ripple Rejection 8.0 Vdc ≤ V_{in} ≤ 18 Vdc, f = 120 Hz	RR	68	75	—	—	68	—	—	68	—	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	V_{in} - V_O	—	2.0	2.5	—	2.0	—	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	40	—	10	—	—	10	—	μV/V_O
Output Resistance f = 1.0 kHz	r_O	—	17	—	—	17	—	—	17	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	1.2	—	0.2	—	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2.5	3.3	—	2.2	—	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	±0.6	—	—	-1.1	—	—	-1.1	—	mV/°C

MC7805A, AC

ELECTRICAL CHARACTERISTICS (V_{in} = 10 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1] unless otherwise noted)

Characteristics	Symbol	MC7805A			MC7805AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	4.9	5.0	5.1	4.9	5.0	5.1	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W) 7.5 Vdc ≤ V_{in} ≤ 20 Vdc	V_O	4.8	5.0	5.2	4.8	5.0	5.2	Vdc
Line Regulation (Note 2) 7.5 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA 8.0 Vdc ≤ V_{in} ≤ 12 Vdc 8.0 Vdc ≤ V_{in} ≤ 12 Vdc, T_J = +25°C 7.3 Vdc ≤ V_{in} ≤ 20 Vdc, T_J = +25°C	Reg_{line}	— — — —	2.0 3.0 1.0 2.0	10 10 4.0 10	— — — —	7.0 10 2.0 7.0	50 50 25 50	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A 250 mA ≤ I_O ≤ 750mA, T_J = +25°C 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	— — — —	2.0 2.0 1.0 1.0	25 25 15 25	— — — —	25 25 — 8.0	100 100 — 50	mV
Quiescent Current T_J = +25°C	I_B	— —	— 3.2	5.0 4.0	— —	— 4.3	6.0 6.0	mA
Quiescent Current Change 8.0 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA 7.5 Vdc ≤ V_{in} ≤ 20 Vdc, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	— — —	0.3 0.2 0.04	0.5 0.5 0.2	— — —	— — —	0.8 0.8 0.5	mA
Ripple Rejection 8.0 Vdc ≤ V_{in} ≤ 18 Vdc, f = 120 Hz, T_J = +25°C 8.0 Vdc ≤ V_{in} ≤ 18 Vdc, f = 120 Hz, I_O = 500 mA	RR	68 68	75 75	— —	— —	— 68	— —	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	V_{in} - V_O	—	2.0	2.5	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	40	—	10	—	μV/V_O
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	—	17	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	1.2	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2.5	3.3	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	±0.6	—	—	-1.1	—	mV/°C

NOTES: 1. T_{low} = -55°C for MC78XX, A
= 0° for MC78XXC, AC
= -40°C for MC78XXB
T_{high} = +150°C for MC78XX, A
= +125°C for MC78XXC, AC, B

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7806, B, C

ELECTRICAL CHARACTERISTICS (V_{in} = 11 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1] unless otherwise noted).

Characteristic	Symbol	MC7806			MC7806B			MC7806C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	5.75	6.0	6.25	5.75	6.0	6.25	5.75	6.0	6.25	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W) 8.0 Vdc ≤ V_{in} ≤ 21 Vdc 9.0 Vdc ≤ V_{in} ≤ 21 Vdc	V_O	— 5.65	— 6.0	— 6.35	— 5.7	— 6.0	— 6.3	5.7 —	6.0 —	6.3 —	Vdc
Line Regulation (T_J = +25°C, Note 2) 8.0 Vdc ≤ V_{in} ≤ 25 Vdc 9.0 Vdc ≤ V_{in} ≤ 13 Vdc	Reg_{line}	— —	3.0 2.0	60 30	— —	9.0 3.0	120 60	— —	9.0 3.0	120 60	mV
Load Regulation (T_J = +25°C, Note 2) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	— —	27 9.0	100 30	— —	43 16	120 60	— —	43 16	120 60	mV
Quiescent Current (T_J = +25°C)	I_B	—	3.2	6.0	—	4.3	8.0	—	4.3	8.0	mA
Quiescent Current Change 8.0 Vdc ≤ V_{in} ≤ 25 Vdc 9.0 Vdc ≤ V_{in} ≤ 25 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	— — —	— 0.3 0.04	— 0.8 0.5	— — —	— — —	— 1.3 0.5	— — —	— — —	1.3 — 0.5	mA
Ripple Rejection 9.0 Vdc ≤ V_{in} ≤ 19 Vdc, f = 120 Hz	RR	65	73	—	—	65	—	—	65	—	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	V_{in}–V_O	—	2.0	2.5	—	2.0	—	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	40	—	10	—	—	10	—	μV/V_O
Output Resistance f = 1.0 kHz	r_O	—	17	—	—	17	—	—	17	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	1.2	—	0.2	—	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2.5	3.3	—	2.2	—	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	±0.7	—	—	−0.8	—	—	−0.8	—	mV/°C

MC7806AC

ELECTRICAL CHARACTERISTICS (V_{in} = 11 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1] unless otherwise noted).

Characteristics	Symbol	MC7806AC			Unit
		Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	5 88	6.0	6.12	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W) 8.6 Vdc ≤ V_{in} ≤ 21 Vdc	V_O	5.76	6.0	6.24	Vdc
Line Regulation (Note 2) 8.6 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA 9.0 Vdc ≤ V_{in} ≤ 13 Vdc 9.0 Vdc ≤ V_{in} ≤ 13 Vdc, T_J = +25°C 8.3 Vdc ≤ V_{in} ≤ 21 Vdc, T_J = +25°C	Reg_{line}	— — — —	9.0 11 3.0 9.0	60 60 30 60	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A 250 mA ≤ I_O ≤ 750 mA, T_J = +25°C 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	— — — —	43 43 — 16	100 100 — 50	mV
Quiescent Current T_J = +25°C	I_B	— —	— 4.3	6.0 6.0	mA
Quiescent Current Change 9.0 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA 8.6 Vdc ≤ V_{in} ≤ 21 Vdc, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	— — —	— — —	0.8 0.8 0.5	mA
Ripple Rejection 9.0 Vdc ≤ V_{in} ≤ 19 Vdc, f = 120 Hz, T_J = +25°C 9.0 Vdc ≤ V_{in} ≤ 19 Vdc, f = 120 Hz, I_O = 500 mA	RR	— —	— 65	— —	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	V_{in}–V_O	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	—	μV/V_O
Output Resistance (f = 1.0 kHz)	r_O	—	17	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	−0.8	—	mV/°C

NOTES: 1. T_{low} = −55°C for MC78XX
= 0° for MC78XXC, AC
= −40°C for MC78XXB
T_{high} = +150°C for MC78XX
= +125°C for MC78XXC, AC, B

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

3

Output Voltage (T_J = +25°C)	V_O	7.7	8.0	8.3	7.7	8.0	8.3	7.7	8.0	8.3	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W) 10.5 Vdc ≤ V_{in} ≤ 23 Vdc 11.5 Vdc ≤ V_{in} ≤ 23 Vdc	V_O	— 7.6	— 8.0	— 8.4	— 7.6	— 8.0	— 8.4	7.6 —	8.0 —	8.4 —	Vdc
Line Regulation (T_J = +25°C, Note 2) 10.5 Vdc ≤ V_{in} ≤ 25 Vdc 11 Vdc ≤ V_{in} ≤ 17 Vdc	Reg_{line}	— —	3.0 2.0	80 40	— —	12 5.0	160 80	— —	12 5.0	160 80	mV
Load Regulation (T_J = +25°C, Note 2) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	— —	28 9.0	100 40	— —	45 16	160 80	— —	45 16	160 80	mV
Quiescent Current (T_J = +25°C)	I_B	—	3.2	6.0	—	4.3	8.0	—	4.3	8.0	mA
Quiescent Current Change 10.5 Vdc ≤ V_{in} ≤ 25 Vdc 11.5 Vdc ≤ V_{in} ≤ 25 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	— — —	— 0.3 0.04	— 0.8 0.5	— — —	— — —	— 1.0 0.5	— — —	— — —	1.0 — 0.5	mA
Ripple Rejection 11.5 Vdc ≤ V_{in} ≤ 21.5 Vdc, f = 120 Hz	RR	62	70	—	—	62	—	—	62	—	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_{in}-V_O$	—	2.0	2.5	—	2.0	—	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	40	—	10	—	—	10	—	μV/V_O
Output Resistance f = 1.0 kHz	r_O	—	18	—	—	18	—	—	18	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	1.2	—	0.2	—	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2.5	3.3	—	2.2	—	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	±1.0	—	—	−0.8	—	—	−0.8	—	mV/°C

MC7808AC

ELECTRICAL CHARACTERISTICS (V_{in} = 14 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1] unless otherwise noted).

Characteristics	Symbol	MC7808AC			Unit
		Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	7.84	8.0	8.16	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W) 10.6 Vdc ≤ V_{in} ≤ 23 Vdc	V_O	7.7	8.0	8.3	Vdc
Line Regulation (Note 2) 10.6 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA 11 Vdc ≤ V_{in} ≤ 17 Vdc 11 Vdc ≤ V_{in} ≤ 17 Vdc, T_J = +25°C 10.4 Vdc ≤ V_{in} ≤ 23 Vdc, T_J = +25°C	Reg_{line}	— — — —	12 15 5.0 12	80 80 40 80	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A 250 mA ≤ I_O ≤ 750 mA, T_J = +25°C 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	— — — —	45 45 — 16	100 100 — 50	mV
Quiescent Current T_J = +25°C	I_B	— —	— 4.3	6.0 6.0	mA
Quiescent Current Change 11 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA 10.6 Vdc ≤ V_{in} ≤ 23 Vdc, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	— — —	— — —	0.8 0.8 0.5	mA
Ripple Rejection 11.5 Vdc ≤ V_{in} ≤ 21.5 Vdc, f = 120 Hz, T_J = +25°C 11.5 Vdc ≤ V_{in} ≤ 21.5 Vdc, f = 120 Hz, I_O = 500 mA	RR	— —	— 62	— —	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_{in}-V_O$	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	—	μV/V_O
Output Resistance (f = 1.0 kHz)	r_O	—	18	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	−0.8	—	mV/°C

NOTES: 1. T_{low} = −55°C for MC78XX
= 0° for MC78XXC, AC
= −40°C for MC78XXB
T_{high} = +150°C for MC78XX
= +125°C for MC78XXC, AC, B

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7809CT

ELECTRICAL CHARACTERISTICS (V_{in} = 15 V, I_O = 500 mA, T_J = 0°C to +125°C unless otherwise noted).

Characteristic	Symbol	MC7809CT			Unit
		Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	8.65	9.0	9.35	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W) 11.5 Vdc ≤ V_{in} ≤ 24 Vdc	V_O	8.55	9.0	9.45	Vdc
Line Regulation (T_J = +25°C, Note 1) 11.5 Vdc ≤ V_{in} ≤ 26 Vdc 11.5 Vdc ≤ V_{in} ≤ 17 Vdc	Reg_{line}	— —	12 5.0	50 25	mV
Load Regulation (T_J = +25°C, Note 1) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	— —	35 12	50 25	mV
Quiescent Current (T_J = +25°C)	I_B	—	4.3	8.0	mA
Quiescent Current Change 11.5 Vdc ≤ V_{in} ≤ 26 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	— —	— —	1.0 0.5	mA
Ripple Rejection 11.5 Vdc ≤ V_{in} ≤ 21.5 Vdc, f = 120 Hz	RR	—	61	—	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_{in} - V_O$	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	—	$\mu V/V_O$
Output Resistance f = 1.0 kHz	r_O	—	18	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	−1.0	—	mV/°C

NOTE 1: Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

3

MC7812, B, C

ELECTRICAL CHARACTERISTICS (V_{in} = 19 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1] unless otherwise noted)

Characteristic	Symbol	MC7812			MC7812B			MC7812C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	11.5	12	12.5	11.5	12	12.5	11.5	12	12.5	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W) 14.5 Vdc ≤ V_{in} ≤ 27 Vdc 15.5 Vdc ≤ V_{in} ≤ 27 Vdc	V_O	— 11.4	— 12	— 12.6	— 11.4	— 12	— 12.6	11.4 —	12 —	12.6 —	Vdc
Line Regulation (T_J = +25°C, Note 2) 14.5 Vdc ≤ V_{in} ≤ 30 Vdc 16 Vdc ≤ V_{in} ≤ 22 Vdc	Reg_{line}	— —	5.0 3.0	120 60	— —	13 6.0	240 120	— —	13 6.0	240 120	mV
Load Regulation (T_J = +25°C, Note 2) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	— —	30 10	120 60	— —	46 17	240 120	— —	46 17	240 120	mV
Quiescent Current (T_J = +25°C)	I_B	—	3.4	6.0	—	4.4	8.0	—	4.4	8.0	mA
Quiescent Current Change 14.5 Vdc ≤ V_{in} ≤ 30 Vdc 15 Vdc ≤ V_{in} ≤ 30 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	— — —	— 0.3 0.04	— 0.8 0.5	— — —	— — —	— 1.0 0.5	— — —	— — —	1.0 — 0.5	mA
Ripple Rejection 15 Vdc ≤ V_{in} ≤ 25 Vdc, f = 120 Hz	RR	61	68	—	—	60	—	—	60	—	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_{in} - V_O$	—	2.0	2.5	—	2.0	—	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	40	—	10	—	—	10	—	$\mu V/V_O$
Output Resistance f = 1.0 kHz	r_O	—	18	—	—	18	—	—	18	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	1.2	—	0.2	—	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2.5	3.3	—	2.2	—	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	±1.5	—	—	-1.0	—	—	-1.0	—	mV/°C

MC7812A, AC

ELECTRICAL CHARACTERISTICS (V_{in} = 19 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1] unless otherwise noted)

Characteristics	Symbol	MC7812A			MC7812AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	11.75	12	12.25	11.75	12	12.25	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W) 14.8 Vdc ≤ V_{in} ≤ 27 Vdc	V_O	11.5	12	12.5	11.5	12	12.5	Vdc
Line Regulation (Note 2) 14.8 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA 16 Vdc ≤ V_{in} ≤ 22 Vdc 16 Vdc ≤ V_{in} ≤ 22 Vdc, T_J = +25°C 14.5 Vdc ≤ V_{in} ≤ 27 Vdc, T_J = +25°C	Reg_{line}	— — — —	5.0 8.0 3.0 5.0	18 30 9.0 18	— — — —	13 16 6.0 13	120 120 60 120	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A 250 mA ≤ I_O ≤ 750mA, T_J = +25°C 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	— — — —	2.0 2.0 1.0 1.0	25 25 15 25	— — — —	46 46 — 17	100 100 — 50	mV
Quiescent Current T_J = +25°C	I_B	— —	— 3.4	5.0 4.0	— —	— 4.4	6.0 6.0	mA
Quiescent Current Change 15 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA 14.8 Vdc ≤ V_{in} ≤ 27 Vdc, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	— — —	0.3 0.2 0.04	0.5 0.5 0.2	— — —	— — —	0.8 0.8 0.5	mA
Ripple Rejection 15 Vdc ≤ V_{in} ≤ 25 Vdc, f = 120 Hz, T_J = +25°C 15 Vdc ≤ V_{in} ≤ 25 Vdc, f = 120 Hz, I_O = 500 mA	RR	61 61	68 68	— —	— —	— 60	— —	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_{in} - V_O$	—	2.0	2.5	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	40	—	10	—	$\mu V/V_O$
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	—	18	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	1.2	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2.5	3.3	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	±1.5	—	—	-1.0	—	mV/°C

NOTES: 1. T_{low} = -55°C for MC78XX, A
= 0° for MC78XXC, AC
= -40°C for MC78XXB
T_{high} = +150°C for MC78XX, A
= +125°C for MC78XXC, AC, B

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7815, B, C

ELECTRICAL CHARACTERISTICS (V_{in} = 23 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1] unless otherwise noted)

Characteristic	Symbol	MC7815			MC7815B			MC7815C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	14.4	15	15.6	14.4	15	15.6	14.4	15	15.6	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W) 17.5 Vdc ≤ V_{in} ≤ 30 Vdc 18.5 Vdc ≤ V_{in} ≤ 30 Vdc	V_O	— 14.25	— 15	— 15.75	— 14.25	— 15	— 15.75	14.25 —	15 —	15.75 —	Vdc
Line Regulation (T_J = +25°C, Note 2) 17.5 Vdc ≤ V_{in} ≤ 30 Vdc 20 Vdc ≤ V_{in} ≤ 26 Vdc	Reg_{line}	— —	6.0 3.0	150 75	— —	13 6.0	300 150	— —	13 6.0	300 150	mV
Load Regulation (T_J = +25°C, Note 2) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	— —	32 10	150 75	— —	52 20	300 150	— —	52 20	300 150	mV
Quiescent Current (T_J = +25°C)	I_B	—	3.4	6.0	—	4.4	8.0	—	4.4	8.0	mA
Quiescent Current Change 17.5 Vdc ≤ V_{in} ≤ 30 Vdc 18.5 Vdc ≤ V_{in} ≤ 30 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	— —	— 0.3	— 0.8	— —	— —	— 1.0	— —	— —	1.0 —	mA
Ripple Rejection 18.5 Vdc ≤ V_{in} ≤ 28.5 Vdc, f = 120 Hz	RR	60	66	—	—	58	—	—	58	—	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_{in} - V_O$	—	2.0	2.5	—	2.0	—	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	40	—	10	—	—	10	—	μV/V_O
Output Resistance f = 1.0 kHz	r_O	—	19	—	—	19	—	—	19	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	1.2	—	0.2	—	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2.5	3.3	—	2.2	—	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	±1.8	—	—	-1.0	—	—	-1.0	—	mV/°C

MC7815A, AC

ELECTRICAL CHARACTERISTICS (V_{in} = 23 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1] unless otherwise noted)

Characteristics	Symbol	MC7815A			MC7815AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	14.7	15	15.3	14.7	15	15.3	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W) 17.9 Vdc ≤ V_{in} ≤ 30 Vdc	V_O	14.4	15	15.6	14.4	15	15.6	Vdc
Line Regulation (Note 2) 17.9 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA 20 Vdc ≤ V_{in} ≤ 26 Vdc 20 Vdc ≤ V_{in} ≤ 26 Vdc, T_J = +25°C 17.5 Vdc ≤ V_{in} ≤ 30 Vdc, T_J = +25°C	Reg_{line}	— — — —	6.0 6.0 3.0 6.0	22 22 10 22	— — — —	13 16 6.0 13	150 150 75 150	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A 250 mA ≤ I_O ≤ 750mA, T_J = +25°C 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	— — — —	2.0 2.0 1.0 1.0	25 25 15 25	— — — —	52 52 — 20	100 100 — 50	mV
Quiescent Current T_J = +25°C	I_B	— —	— 3.4	5.5 4.5	— —	— 4.4	6.0 6.0	mA
Quiescent Current Change 17.5 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA 17.5 Vdc ≤ V_{in} ≤ 30 Vdc, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	— — —	0.3 0.2 0.04	0.5 0.5 0.2	— — —	— — —	0.8 0.8 0.5	mA
Ripple Rejection 18.5 Vdc ≤ V_{in} ≤ 28.5 Vdc, f = 120 Hz, T_J = +25°C 18.5 Vdc ≤ V_{in} ≤ 28.5 Vdc, f = 120 Hz, I_O = 500 mA	RR	60 60	66 66	— —	— —	— 58	— —	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_{in} - V_O$	—	2.0	2.5	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	40	—	10	—	μV/V_O
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	—	19	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	1.2	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2.5	3.3	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	±1.8	—	—	-1.0	—	mV/°C

NOTES: 1. T_{low} = −55°C for MC78XX, A
= 0° for MC78XXC, AC
= −40°C for MC78XXB
T_{high} = +150°C for MC78XX, A
= +125°C for MC78XXC, AC, B

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

Characteristic	Symbol	MC7818			MC7818B			MC7818C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	17.3	18	18.7	17.3	18	18.7	17.3	18	18.7	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W) 21 Vdc ≤ V_{in} ≤ 33 Vdc 22 Vdc ≤ V_{in} ≤ 33 Vdc	V_O	— 17.1	— 18	— 18.9	— 17.1	— 18	— 18.9	17.1 —	18 —	18.9 —	Vdc
Line Regulation (T_J = +25°C, Note 2) 21 Vdc ≤ V_{in} ≤ 33 Vdc 24 Vdc ≤ V_{in} ≤ 30 Vdc	Reg_{line}	— —	7.0 4.0	180 90	— —	25 10	360 180	— —	25 10	360 180	mV
Load Regulation (T_J = +25°C, Note 2) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	— —	35 12	180 90	— —	55 22	360 180	— —	55 22	360 180	mV
Quiescent Current (T_J = +25°C)	I_B	—	3.5	6.0	—	4.5	8.0	—	4.5	8.0	mA
Quiescent Current Change 21 Vdc ≤ V_{in} ≤ 33 Vdc 22 Vdc ≤ V_{in} ≤ 33 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	— — —	— 0.3 0.04	— 0.8 0.5	— — —	— — —	— 1.0 0.5	— — —	— — —	1.0 — 0.5	mA
Ripple Rejection 22 Vdc ≤ V_{in} ≤ 33 Vdc, f = 120 Hz	RR	59	65	—	—	57	—	—	57	—	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_{in}-V_O$	—	2.0	2.5	—	2.0	—	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	40	—	10	—	—	10	—	μV/V_O
Output Resistance f = 1.0 kHz	r_O	—	19	—	—	19	—	—	19	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	1.2	—	0.2	—	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2.5	3.3	—	2.2	—	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	±2.3	—	—	−1.0	—	—	−1.0	—	mV/°C

MC7818AC

ELECTRICAL CHARACTERISTICS (V_{in} = 27 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1] unless otherwise noted).

Characteristics	Symbol	MC7818AC			Unit
		Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	17.64	18	18.36	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W) 21 Vdc ≤ V_{in} ≤ 33 Vdc	V_O	17.3	18.7	17.3	Vdc
Line Regulation (Note 2) 21 Vdc ≤ V_{in} ≤ 33 Vdc, I_O = 500 mA 24 Vdc ≤ V_{in} ≤ 30 Vdc 24 Vdc ≤ V_{in} ≤ 30 Vdc, T_J = +25°C 20.6 Vdc ≤ V_{in} ≤ 33 Vdc, T_J = +25°C	Reg_{line}	— — — —	25 28 10 25	180 180 90 180	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A 250 mA ≤ I_O ≤ 750 mA, T_J = +25°C 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	— — — —	55 55 — 22	100 100 — 50	mV
Quiescent Current T_J = +25°C	I_B	— —	— 4.5	6.0 6.0	mA
Quiescent Current Change 21 Vdc ≤ V_{in} ≤ 33 Vdc, I_O = 500 mA 21 Vdc ≤ V_{in} ≤ 33 Vdc, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	— — —	— — —	0.8 0.8 0.5	mA
Ripple Rejection 22 Vdc ≤ V_{in} ≤ 32 Vdc, f = 120 Hz, T_J = +25°C 22 Vdc ≤ V_{in} ≤ 32 Vdc, f = 120 Hz, I_O = 500 mA	RR	— —	— 57	— —	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_{in}-V_O$	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	—	μV/V_O
Output Resistance (f = 1.0 kHz)	r_O	—	19	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	−1.0	—	mV/°C

NOTES: 1. T_{low} = −55°C for MC78XX
= 0° for MC78XXC, AC
= −40°C for MC78XXB
T_{high} = +150°C for MC78XX
= +125°C for MC78XXC, AC, B

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7824, B, C

ELECTRICAL CHARACTERISTICS (V_{in} = 33 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1] unless otherwise noted).

Characteristic	Symbol	MC7824			MC7824B			MC7824C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	23	24	25	23	24	25	23	24	25	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W) 27 Vdc ≤ V_{in} ≤ 38 Vdc 28 Vdc ≤ V_{in} ≤ 38 Vdc	V_O	 — 22.8	 — 24	 — 25.2	 — 22.8	 — 24	 — 25.2	 22.8 —	 24 —	 25.2 —	Vdc
Line Regulation (T_J = +25°C, Note 2) 27 Vdc ≤ V_{in} ≤ 38 Vdc 30 Vdc ≤ V_{in} ≤ 36 Vdc	Reg_{line}	 — —	 10 5.0	 240 120	 — —	 31 14	 480 240	 — —	 31 14	 480 240	mV
Load Regulation (T_J = +25°C, Note 2) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 — —	 40 15	 240 120	 — —	 60 25	 480 240	 — —	 60 25	 480 240	mV
Quiescent Current (T_J = +25°C)	I_B	—	3.6	6.0	—	4.6	8.0	—	4.6	8.0	mA
Quiescent Current Change 27 Vdc ≤ V_{in} ≤ 38 Vdc 28 Vdc ≤ V_{in} ≤ 38 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 — — —	 — 0.3 0.04	 — 0.8 0.5	 — — —	 — — —	 — 1.0 0.5	 — — —	 — — —	 1.0 — 0.5	mA
Ripple Rejection 28 Vdc ≤ V_{in} ≤ 38 Vdc, f = 120 Hz	RR	56	62	—	—	54	—	—	54	—	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_{in}-V_O$	—	2.0	2.5	—	2.0	—	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	40	—	10	—	—	10	—	μV/V_O
Output Resistance f = 1.0 kHz	r_O	—	20	—	—	20	—	—	20	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	1.2	—	0.2	—	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2.5	3.3	—	2.2	—	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	±3.0	—	—	−1.5	—	—	−1.5	—	mV/°C

MC7824AC

ELECTRICAL CHARACTERISTICS (V_{in} = 33 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1] unless otherwise noted).

Characteristics	Symbol	MC7824AC			Unit
		Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	23.5	24	24.5	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W) 27.3 Vdc ≤ V_{in} ≤ 38 Vdc	V_O	 23	 24	 25	Vdc
Line Regulation (Note 2) 27 Vdc ≤ V_{in} ≤ 38 Vdc, I_O = 500 mA 30 Vdc ≤ V_{in} ≤ 36 Vdc 30 Vdc ≤ V_{in} ≤ 36 Vdc, T_J = +25°C 26.7 Vdc ≤ V_{in} ≤ 38 Vdc, T_J = +25°C	Reg_{line}	 — — — —	 31 35 14 31	 240 240 120 240	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A 250 mA ≤ I_O ≤ 750 mA, T_J = +25°C 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 — — — —	 60 60 — 25	 100 100 — 50	mV
Quiescent Current T_J = +25°C	I_B	— —	— 4.6	6.0 6.0	mA
Quiescent Current Change 27.3 Vdc ≤ V_{in} ≤ 38 Vdc, I_O = 500 mA 27.3 Vdc ≤ V_{in} ≤ 38 Vdc, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 — — —	 — — —	 0.8 0.8 0.5	mA
Ripple Rejection 28 Vdc ≤ V_{in} ≤ 38 Vdc, f = 120 Hz, T_J = +25°C 28 Vdc ≤ V_{in} ≤ 38 Vdc, f = 120 Hz, I_O = 500 mA	RR	 — —	 — 54	 — —	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_{in}-V_O$	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	—	μV/V_O
Output Resistance (f = 1.0 kHz)	r_O	—	20	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	−1.5	—	mV/°C

NOTES: 1. T_{low} = −55°C for MC78XX
= 0° for MC78XXC, AC
= −40°C for MC78XXB
T_{high} = +150°C for MC78XX
= +125°C for MC78XXC, AC, B

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

3

TYPICAL CHARACTERISTICS
(T_A = +25°C unless otherwise noted.)

FIGURE 1 — WORST CASE POWER DISSIPATION versus AMBIENT TEMPERATURE (Case 221A)

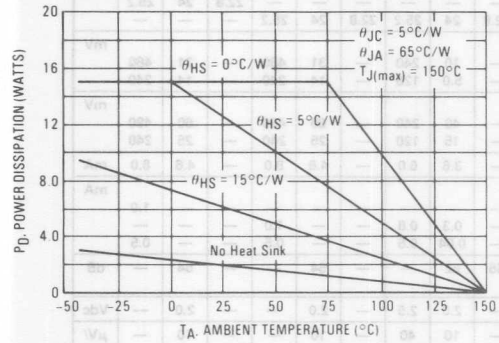


FIGURE 2 – WORST CASE POWER DISSIPATION versus AMBIENT TEMPERATURE (Case 1)

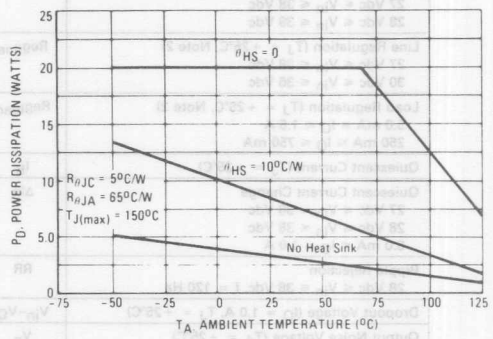


FIGURE 3 — INPUT OUTPUT DIFFERENTIAL AS A FUNCTION OF JUNCTION TEMPERATURE (MC78XXC, AC, B)

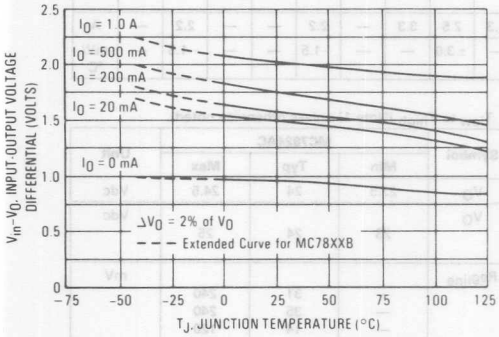


FIGURE 4 – INPUT OUTPUT DIFFERENTIAL AS A FUNCTION OF JUNCTION TEMPERATURE (MC78XX, A)

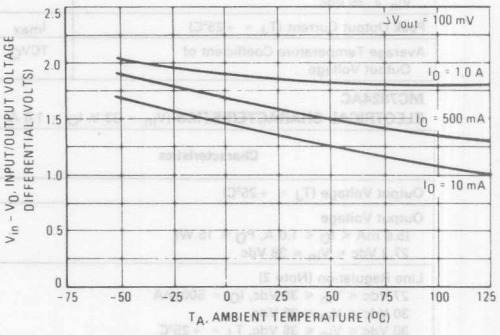


FIGURE 5 — PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE (MC78XXC, AC, B)

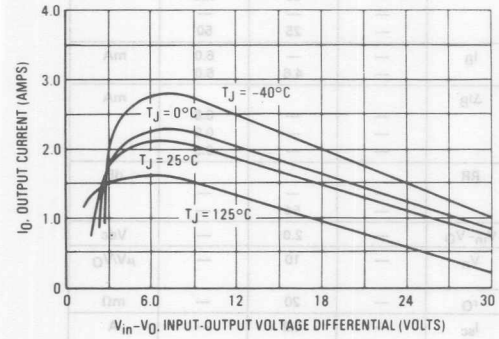
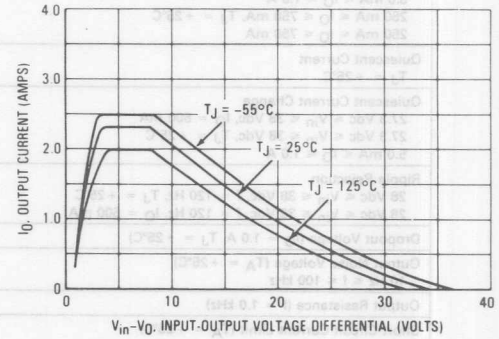


FIGURE 6 — PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE (MC78XX, A)



TYPICAL CHARACTERISTICS (continued)
(T_A = 25°C unless otherwise noted.)

FIGURE 7 – RIPPLE REJECTION AS A FUNCTION OF OUTPUT VOLTAGES (MC78XXC, AC)

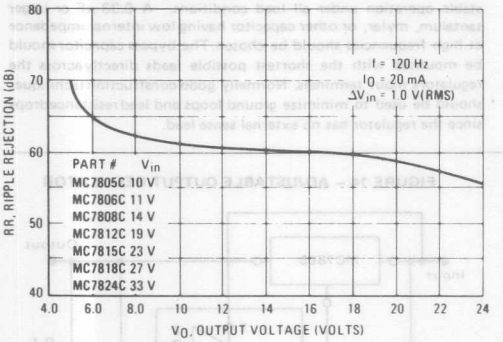


FIGURE 8 – RIPPLE REJECTION AS A FUNCTION OF FREQUENCY (MC78XXC, AC, A)

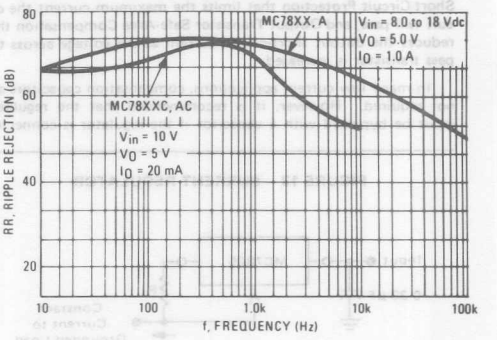


FIGURE 9 – OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE (MC78XXC, AC, B)

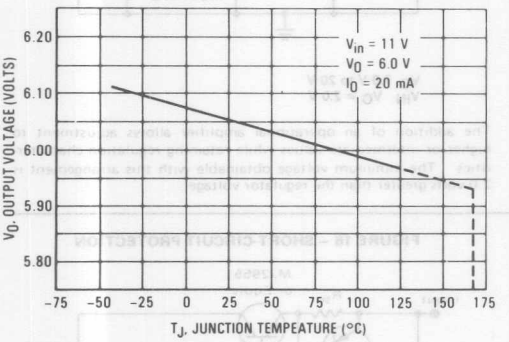


FIGURE 10 – OUTPUT IMPEDANCE AS A FUNCTION OF OUTPUT VOLTAGE (MC78XXC, AC)

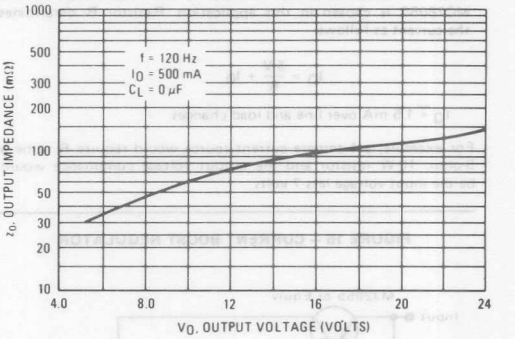


FIGURE 11 – QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE (MC78XXC, AC, B)

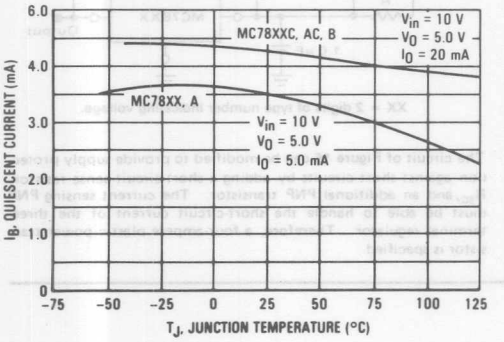
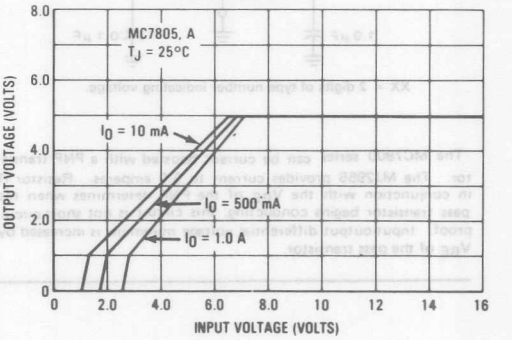


FIGURE 12 – DROPOUT CHARACTERISTICS (MC78XX, A)

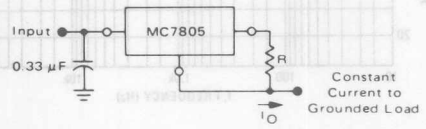


Design Considerations

The MC7800 Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

FIGURE 13 – CURRENT REGULATOR



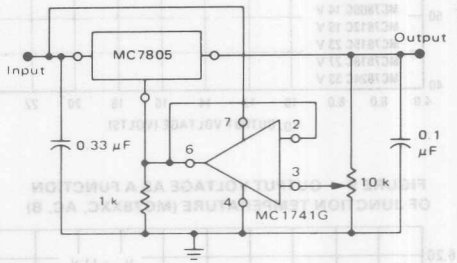
The MC7800 regulators can also be used as a current source when connected as above. In order to minimize dissipation the MC7805C is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5\ V}{R} + I_Q$$

$I_Q \cong 1.5$ mA over line and load changes

For example, a 1-ampere current source would require R to be a 5-ohm, 10-W resistor and the output voltage compliance would be the input voltage less 7 volts.

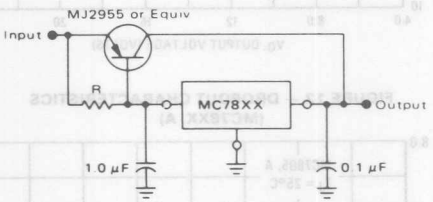
FIGURE 14 – ADJUSTABLE OUTPUT REGULATOR



V_O, 7.0 V to 20 V
V_{IN} $V_O \geq 2.0$ V

The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 2.0 volts greater than the regulator voltage.

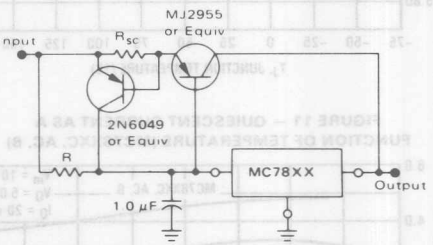
FIGURE 15 – CURRENT BOOST REGULATOR



XX = 2 digits of type number indicating voltage.

The MC7800 series can be current boosted with a PNP transistor. The MJ2955 provides current to 5.0 amperes. Resistor R in conjunction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short-circuit proof. Input-output differential voltage minimum is increased by V_{BE} of the pass transistor.

FIGURE 16 – SHORT-CIRCUIT PROTECTION



XX = 2 digits of type number indicating voltage.

The circuit of Figure 15 can be modified to provide supply protection against short circuits by adding a short-circuit sense resistor, R_{sc}, and an additional PNP transistor. The current sensing PNP must be able to handle the short-circuit current of the three-terminal regulator. Therefore, a four-ampere plastic power transistor is specified.

MOTOROLA

MC78L00,A Series

THREE-TERMINAL LOW CURRENT POSITIVE VOLTAGE REGULATORS

The MC78L00 Series of positive voltage regulators are inexpensive, easy-to-use devices suitable for a multitude of applications that require a regulated supply of up to 100 mA. Like their higher powered MC7800 and MC78M00 Series cousins, these regulators feature internal current limiting and thermal shutdown making them remarkably rugged. No external components are required with the MC78L00 devices in many applications.

These devices offer a substantial performance advantage over the traditional zener diode-resistor combination, as output impedance and quiescent current are substantially reduced.

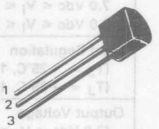
- Wide Range of Available, Fixed Output Voltages
- Low Cost
- Internal Short Circuit Current Limiting
- Internal Thermal Overload Protection
- No External Components Required
- Complementary Negative Regulators Offered (MC79L00 Series)
- Available in Either ±5% (AC) or ±10% (C) Selections

THREE-TERMINAL LOW CURRENT POSITIVE FIXED VOLTAGE REGULATORS

3

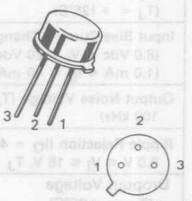
P SUFFIX
CASE 29-04

PIN 1. OUTPUT
2. GROUND
3. INPUT



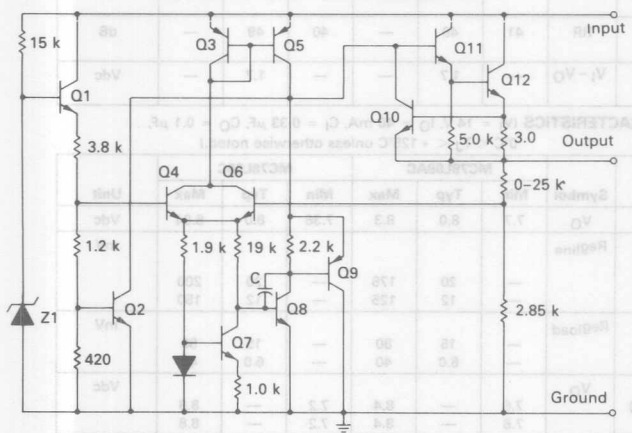
G SUFFIX
CASE 79-05

PIN 1. INPUT
2. OUTPUT
3. GROUND



(Bottom View)
(Case Connected To Pin 3)

REPRESENTATIVE CIRCUIT SCHEMATIC



D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SOP-8



PIN 1. V_{OUT}
2. GND
3. GND
4. NC
5. NC
6. GND
7. GND
8. V_{IN}

SOP-8 is an internally modified SO-8 Package. Pins 2, 3, 6 and 7 are electrically common to the die attach flag. This internal lead frame modification decreases package thermal resistance and increases power dissipation capability when appropriately mounted on a printed circuit board. SOP-8 conforms to all external dimensions of the standard SO-8 Package.

ORDERING INFORMATION

Device	Junction Temperature Range	Package
MC78LXXACD	T_J = 0°C to +125°C	SOP-8
MC78LXXACG		Metal Can
MC78LXXACP		Plastic Power
MC78LXXCD		SOP-8
MC78LXXCG		Metal Can
MC78LXXCP		Plastic Power
MC78LXXABP#	T_J = −40°C to +125°C	Plastic Power
XX indicates nominal voltage		

#Automotive temperature range selections are available with special test conditions and additional tests in 5, 8, 12 and 15 volts devices. Contact your local Motorola sales office for information.

Device No. ±10%	Device No. ±5%	Nominal Voltage
MC78L05C	MC78L05AC	5.0
MC78L08C	MC78L08AC	8.0
MC78L12C	MC78L12AC	12
MC78L15C	MC78L15AC	15
MC78L18C	MC78L18AC	18
MC78L24C	MC78L24AC	24

MC78L00 Series MAXIMUM RATINGS (T_A = +125°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (2.6 V–8.0 V) (12 V–18 V) (24 V)	V_I	30 35 40	Vdc
Storage Junction Temperature Range	T_{stg}	−65 to +150	°C
Operating Junction Temperature Range	T_J	0 to +150	°C

MC78L05C, MC78L05AC ELECTRICAL CHARACTERISTICS (V_I = 10 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	MC78L05AC Min	MC78L05AC Typ	MC78L05AC Max	MC78L05C Min	MC78L05C Typ	MC78L05C Max	Unit
Output Voltage (T_J = +25°C)	V_O	4.8	5.0	5.2	4.6	5.0	5.4	Vdc
Line Regulation (T_J = +25°C, I_O = 40 mA) 7.0 Vdc ≤ V_I ≤ 20 Vdc 8.0 Vdc ≤ V_I ≤ 20 Vdc	Reg_{line}	 — —	 55 45	 150 100	 — —	 55 45	 200 150	mV
Load Regulation (T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA) (T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)	Reg_{load}	 — —	 11 5.0	 60 30	 — —	 11 5.0	 60 30	mV
Output Voltage (7.0 Vdc ≤ V_I ≤ 20 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (V_I = 10 V, 1.0 mA ≤ I_O ≤ 70 mA)	V_O	 4.75 4.75	 — —	 5.25 5.25	 4.5 4.5	 — —	 5.5 5.5	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 — —	 3.8 —	 6.0 5.5	 — —	 3.8 —	 6.0 5.5	mA
Input Bias Current Change (8.0 Vdc ≤ V_I ≤ 20 Vdc) (1.0 mA ≤ I_O ≤ 40 mA)	ΔI_{IB}	 — —	 — —	 1.5 0.1	 — —	 — —	 1.5 0.2	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	40	—	—	40	—	μV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 8.0 V ≤ V_I ≤ 18 V, T_J = +25°C)	RR	41	49	—	40	49	—	dB
Dropout Voltage (T_J = +25°C)	$V_I - V_O$	—	1.7	—	—	1.7	—	Vdc

MC78L08C, MC78L08AC ELECTRICAL CHARACTERISTICS (V_I = 14 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	MC78L08AC Min	MC78L08AC Typ	MC78L08AC Max	MC78L08C Min	MC78L08C Typ	MC78L08C Max	Unit
Output Voltage (T_J = +25°C)	V_O	7.7	8.0	8.3	7.36	8.0	8.64	Vdc
Line Regulation (T_J = +25°C, I_O = 40 mA) 10.5 Vdc ≤ V_I ≤ 23 Vdc 11 Vdc ≤ V_I ≤ 23 Vdc	Reg_{line}	 — —	 20 12	 175 125	 — —	 20 12	 200 150	mV
Load Regulation (T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA) (T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)	Reg_{load}	 — —	 15 8.0	 80 40	 — —	 15 6.0	 80 40	mV
Output Voltage (10.5 Vdc ≤ V_I ≤ 23 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (V_I = 14 V, 1.0 mA ≤ I_O ≤ 70 mA)	V_O	 7.6 7.6	 — —	 8.4 8.4	 7.2 7.2	 — —	 8.8 8.8	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 — —	 3.0 —	 6.0 5.5	 — —	 3.0 —	 6.0 5.5	mA
Input Bias Current Change (11 Vdc ≤ V_I ≤ 23 Vdc) (1.0 mA ≤ I_O ≤ 40 mA)	ΔI_{IB}	 — —	 — —	 1.5 0.1	 — —	 — —	 1.5 0.2	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	60	—	—	52	—	μV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 12 V ≤ V_I ≤ 23 V, T_J = +25°C)	RR	37	57	—	36	55	—	dB
Dropout Voltage (T_J = +25°C)	V_I-V_O	—	1.7	—	—	1.7	—	Vdc

MC78L12C, MC78L12AC ELECTRICAL CHARACTERISTICS (V_I = 19 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	MC78L12AC			MC78L12C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	11.5	12	12.5	11.1	12	12.9	Vdc
Line Regulation (T_J = +25°C, I_O = 40 mA) 14.5 Vdc ≤ V_I ≤ 27 Vdc 16 Vdc ≤ V_I ≤ 27 Vdc	Reg_{line}	 — —	 120 100	 250 200	 — —	 120 100	 250 200	mV
Load Regulation (T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA) (T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)	Reg_{load}	 — —	 20 10	 100 50	 — —	 20 10	 100 50	mV
Output Voltage (14.5 Vdc ≤ V_I ≤ 27 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (V_I = 19 V, 1.0 mA ≤ I_O ≤ 70 mA)	V_O	 11.4 11.4	 — —	 12.6 12.6	 10.8 10.8	 — —	 13.2 13.2	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 — —	 4.2 —	 6.5 6.0	 — —	 4.2 —	 6.5 6.0	mA
Input Bias Current Change (16 Vdc ≤ V_I ≤ 27 Vdc) (1.0 mA ≤ I_O ≤ 40 mA)	ΔI_{IB}	 — —	 — —	 1.5 0.1	 — —	 — —	 1.5 0.2	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	80	—	—	80	—	μV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 15 V ≤ V_I ≤ 25 V, T_J = +25°C)	RR	37	42	—	36	42	—	dB
Dropout Voltage (T_J = +25°C)	V_I-V_O	—	1.7	—	—	1.7	—	Vdc

MC78L15C, MC78L15AC ELECTRICAL CHARACTERISTICS (V_I = 23 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	MC78L15AC			MC78L15C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	14.4	15	15.6	13.8	15	16.2	Vdc
Line Regulation (T_J = +25°C, I_O = 40 mA) 17.5 Vdc ≤ V_I ≤ 30 Vdc 20 Vdc ≤ V_I ≤ 30 Vdc	Reg_{line}	 — —	 130 110	 300 250	 — —	 130 110	 300 250	mV
Load Regulation (T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA) (T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)	Reg_{load}	 — —	 25 12	 150 75	 — —	 25 12	 150 75	mV
Output Voltage (17.5 Vdc ≤ V_I ≤ 30 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (V_I = 23 V, 1.0 mA ≤ I_O ≤ 70 mA)	V_O	 14.25 14.25	 — —	 15.75 15.75	 13.5 13.5	 — —	 16.5 16.5	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 — —	 4.4 —	 6.5 6.0	 — —	 4.4 —	 6.5 6.0	mA
Input Bias Current Change (20 Vdc ≤ V_I ≤ 30 Vdc) (1.0 mA ≤ I_O ≤ 40 mA)	ΔI_{IB}	 — —	 — —	 1.5 0.1	 — —	 — —	 1.5 0.2	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	90	—	—	90	—	μV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 18.5 V ≤ V_I ≤ 28.5 V, T_J = +25°C)	RR	34	39	—	33	39	—	dB
Dropout Voltage (T_J = +25°C)	V_I-V_O	—	1.7	—	—	1.7	—	Vdc

0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	MC78L18AC Min	MC78L18AC Typ	MC78L18AC Max	MC78L18C Min	MC78L18C Typ	MC78L18C Max	Unit
Output Voltage (T_J = +25°C)	V_O	17.3	18	18.7	16.6	18	19.4	Vdc
Line Regulation	Reg_{line}							mV
(T_J = +25°C, I_O = 40 mA)								
21.4 Vdc ≤ V_I ≤ 33 Vdc					—	32	325	
20.7 Vdc ≤ V_I ≤ 33 Vdc		—	45	325				
22 Vdc ≤ V_I ≤ 33 Vdc					—	27	275	
21 Vdc ≤ V_I ≤ 33 Vdc		—	35	275				
Load Regulation	Reg_{load}							mV
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA)		—	30	170	—	30	170	
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)		—	15	85	—	15	85	
Output Voltage	V_O							Vdc
(21.4 Vdc ≤ V_I ≤ 33 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)					16.2	—	19.8	
(20.7 Vdc ≤ V_I ≤ 33 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)		17.1	—	18.9				
(V_I = 27 V, 1.0 mA ≤ I_O ≤ 70 mA)					16.2	—	19.8	
(V_I = 27 V, 1.0 mA ≤ I_O ≤ 70 mA)		17.1	—	18.9				
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		—	3.1	6.5	—	3.1	6.5	
(T_J = +125°C)		—	—	6.0	—	—	6.0	
Input Bias Current Change	ΔI_{IB}							mA
(22 Vdc ≤ V_I ≤ 33 Vdc)					—	—	1.5	
(21 Vdc ≤ V_I = 33 Vdc)		—	—	1.5				
(1.0 mA ≤ I_O ≤ 40 mA)		—	—	0.1	—	—	0.2	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	150	—	—	150	—	μV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 23 V ≤ V_I ≤ 33 V, T_J = +25°C)	RR	33	48	—	32	46	—	dB
Dropout Voltage (T_J = +25°C)	V_I-V_O	—	1.7	—	—	1.7	—	Vdc

MC78L24C, MC78L24AC ELECTRICAL CHARACTERISTICS (V_I = 33 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	MC78L24AC Min	MC78L24AC Typ	MC78L24AC Max	MC78L24C Min	MC78L24C Typ	MC78L24C Max	Unit
Output Voltage (T_J = +25°C)	V_O	23	24	25	22.1	24	25.9	Vdc
Line Regulation	Reg_{line}							mV
(T_J = +25°C, I_O = 40 mA)								
27.5 Vdc ≤ V_I ≤ 38 Vdc		—	—	—	—	35	350	
28 Vdc ≤ V_I ≤ 80 Vdc		—	50	300	—	30	300	
27 Vdc ≤ V_I ≤ 38 Vdc		—	60	350	—	—	—	
Load Regulation	Reg_{load}							mV
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA)		—	40	200	—	40	200	
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)		—	20	100	—	20	100	
Output Voltage	V_O							Vdc
(28 Vdc ≤ V_I ≤ 38 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)					21.6	—	26.4	
(27 Vdc ≤ V_I ≤ 38 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)		22.8	—	25.2				
(28 Vdc ≤ V_I = 33 V, 1.0 mA ≤ I_O ≤ 70 mA)					21.6	—	26.4	
(27 Vdc ≤ V_I ≤ 33 V, 1.0 mA ≤ I_O ≤ 70 mA)		22.8	—	25.2				
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		—	3.1	6.5	—	3.1	6.5	
(T_J = +125°C)		—	—	6.0	—	—	6.0	
Input Bias Current Change	ΔI_{IB}							mA
(28 Vdc ≤ V_I ≤ 38 Vdc)		—	—	1.5	—	—	1.5	
(1.0 mA ≤ I_O ≤ 40 mA)		—	—	0.1	—	—	0.2	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	200	—	—	200	—	μV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 29 V ≤ V_I ≤ 35 V, T_J = +25°C)	RR	31	45	—	30	43	—	dB
Dropout Voltage (T_J = +25°C)	V_I-V_O	—	1.7	—	—	1.7	—	Vdc

TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted.)

FIGURE 1 – DROPOUT CHARACTERISTICS

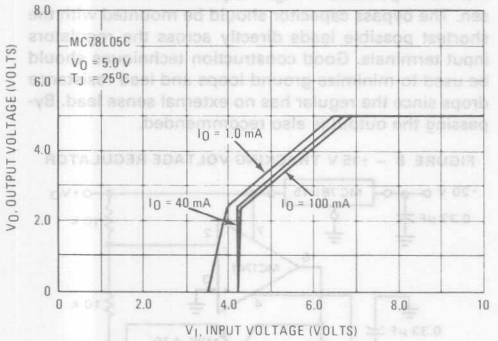


FIGURE 2 – DROPOUT VOLTAGE versus JUNCTION TEMPERATURE

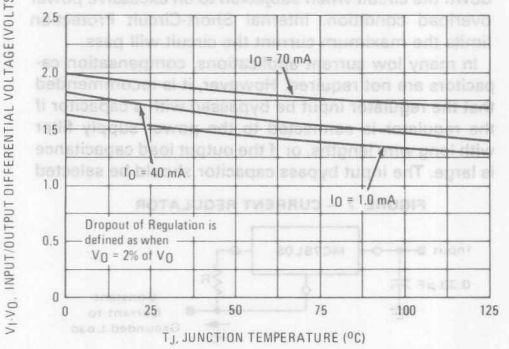


FIGURE 3 – INPUT BIAS CURRENT versus AMBIENT TEMPERATURE

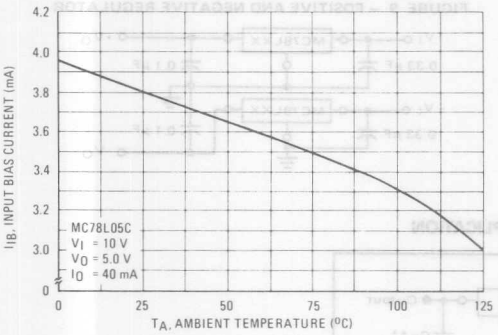


FIGURE 4 – INPUT BIAS CURRENT versus INPUT VOLTAGE

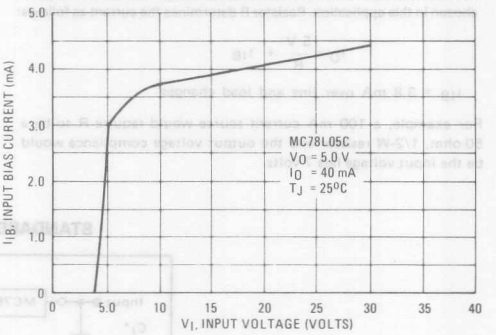


FIGURE 5 – MAXIMUM AVERAGE POWER DISSIPATION versus AMBIENT TEMPERATURE – TO-92 Type Package

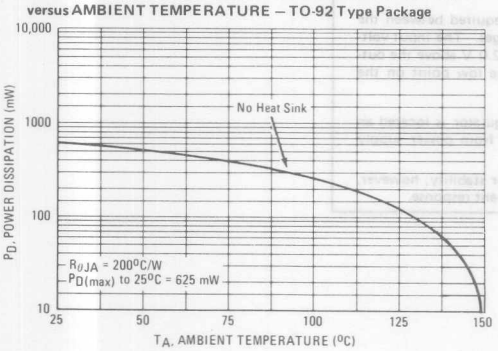
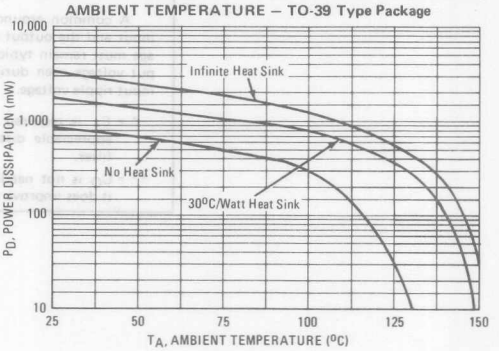


FIGURE 6 – MAXIMUM AVERAGE POWER DISSIPATION versus AMBIENT TEMPERATURE – TO-39 Type Package



3

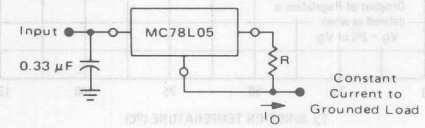
APPLICATIONS INFORMATION

Design Considerations

The MC78L00 Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition. Internal Short-Circuit Protection limits the maximum current the circuit will pass.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. The input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Good construction techniques should be used to minimize ground loops and lead resistance drops since the regular has no external sense lead. Bypassing the output is also recommended.

FIGURE 7 – CURRENT REGULATOR



The MC78L00 regulators can also be used as a current source when connected as above. In order to minimize dissipation the MC78L05C is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5\ V}{R} + I_{IB}$$

I_{IB} = 3.8 mA over line and load changes

For example, a 100 mA current source would require R to be a 50-ohm, 1/2-W resistor and the output voltage compliance would be the input voltage less 7 volts.

FIGURE 8 – ±15 V TRACKING VOLTAGE REGULATOR

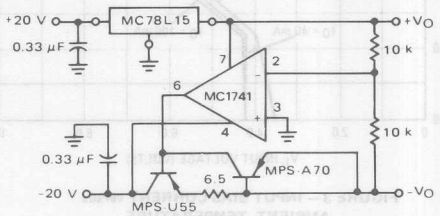
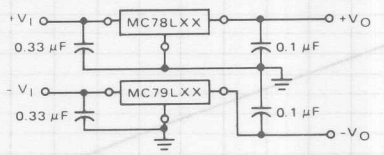
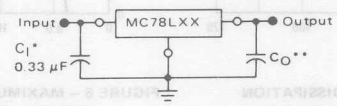


FIGURE 9 – POSITIVE AND NEGATIVE REGULATOR



STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

* = C_I is required if regulator is located an appreciable distance from power supply filter.

** = C_O is not needed for stability; however, it does improve transient response.

MOTOROLA

MC78M00 Series

3

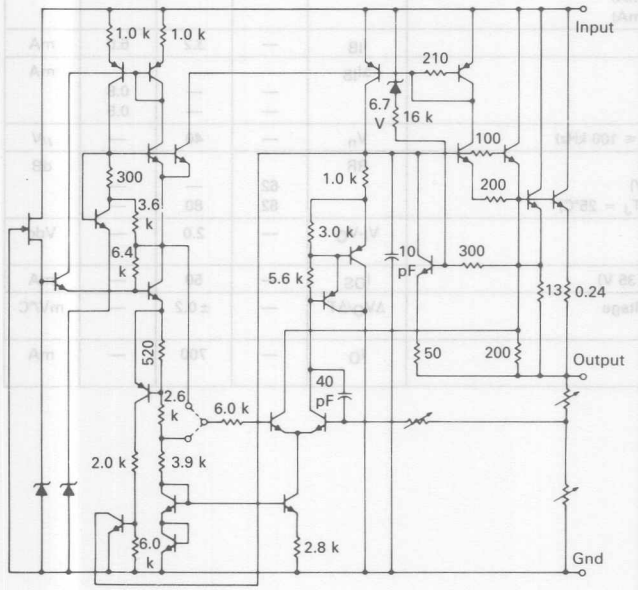
THREE-TERMINAL MEDIUM CURRENT POSITIVE VOLTAGE REGULATORS

The MC78M00 Series positive voltage regulators are identical to the popular MC7800 Series devices, except that they are specified for only half the output current. Like the MC7800 devices, the MC78M00 three-terminal regulators are intended for local, on-card voltage regulation.

Internal current limiting, thermal shutdown circuitry and safe-area compensation for the internal pass transistor combine to make these devices remarkably rugged under most operating conditions. Maximum output current, with adequate heatsinking is 500 mA.

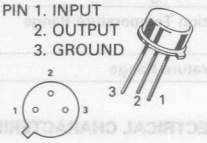
- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation

EQUIVALENT SCHEMATIC DIAGRAM



THREE-TERMINAL MEDIUM CURRENT POSITIVE FIXED VOLTAGE REGULATORS

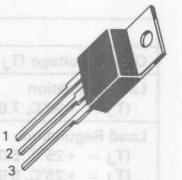
PIN 1. INPUT
2. OUTPUT
3. GROUND



G SUFFIX
METAL PACKAGE
CASE 79-05

(Case connected to Pin 3)

(Bottom View)

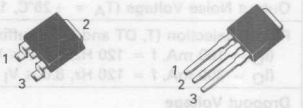


T SUFFIX
PLASTIC PACKAGE
CASE 221A-04

(All 3 Plastic Types)

PIN 1. INPUT
2. GROUND
3. OUTPUT

(Heatsink surface connected to Pin 2)



DT SUFFIX
PLASTIC PACKAGE
CASE 369A-03
DPAK

DT-1 SUFFIX
PLASTIC PACKAGE
CASE 369-03
DPAK

TYPE NO./VOLTAGE		
MC78M05B,C 5.0 Volts	MC78M12B,C 12 Volts	MC78M20B,C 20 Volts
MC78M06B,C 6.0 Volts	MC78M15B,C 15 Volts	MC78M24B,C 24 Volts
MC78M08B,C 8.0 Volts	MC78M18B,C 18 Volts	

ORDERING INFORMATION

Device	Tested Operating Junction Temp. Range	Package
MC78MXXCG*	T_J = 0°C to +125°C	Metal Can
MC78MXXCDT**		DPAK
MC78MXXCDT-1**		
MC78MXXCT		Plastic Power
MC78MXXBT#	T_J = −40°C to +125°C	Plastic Power

XX Indicates nominal voltage.
* Available in 5, 8, 12 and 15 volt devices.
** Available in 5, 12 and 15 volt devices.
\# Automotive temperature range selections are available with special test conditions and additional tests in 5, 8, 12 and 15 volt devices. Contact your local Motorola sales office for information.

Input Voltage (5.0 V–18 V) (20 V–24 V)		V_I	35 40	Vdc
Power Dissipation (Package Limitation) Plastic Package T_A = 25°C Derate above T_A = 25°C T_C = 25°C Derate above T_C = 110°C Metal Package T_A = 25°C Derate above T_A = 25°C T_C = 25°C Derate above T_C = 85°C		 P_D θ_{JA} P_D θ_{JC} P_D θ_{JA} P_D θ_{JC}	 Internally Limited 70 Internally Limited 5.0 Internally Limited 185 Internally Limited 25	 °C/W °C/W °C/W °C/W
Operating Junction Temperature Range	MC78MXXC MC78MXXB	T_J	0 to +150 −40 to +150	°C
Storage Temperature Range		T_{stg}	−65 to +150	°C

MC78M05 ELECTRICAL CHARACTERISTICS (V_I = 10 V, I_O = 350 mA, 0°C < T_J < +125°C, $P_D \leq$ 5.0 W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	4.8	5.0	5.2	Vdc
Line Regulation (T_J = +25°C, 7.0 Vdc ≤ V_I ≤ 25 Vdc, I_O = 200 mA)	Reg_{line}	—	3.0	50	mV
Load Regulation (T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 — —	 20 10	 100 50	mV
Output Voltage (7.0 Vdc ≤ V_I ≤ 25 Vdc, 5.0 mA ≤ I_O ≤ 200 mA) (7.0 Vdc ≤ V_I ≤ 20 Vdc, 5.0 mA ≤ I_O ≤ 350 mA)	V_O	4.75	—	5.25	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	3.2	6.0	mA
Quiescent Current Change (8.0 Vdc ≤ V_I ≤ 25 Vdc, I_O = 200 mA) (5.0 mA ≤ I_O ≤ 350 mA)	ΔI_{IB}	 — —	 — —	 0.8 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	40	—	μV
Ripple Rejection (T, DT and DT-1 suffixes only) (I_O = 100 mA, f = 120 Hz, 8.0 V ≤ V_I ≤ 18 V) (I_O = 300 mA, f = 120 Hz, 8.0 ≤ V_I ≤ 18 V, T_J = 25°C)	RR	 62 62	 — 80	 — —	dB
Dropout Voltage (T_J = +25°C)	V_I-V_O	—	2.0	—	Vdc
Short Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	—	50	—	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	—	±0.2	—	mV/°C
Peak Output Current (T_J = 25°C)	I_O	—	700	—	mA

MC78M06 ELECTRICAL CHARACTERISTICS (V_I = 11 V, I_O = 350 mA, 0°C < T_J < +125°C, P_D ≤ 5.0 W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	5.75	6.0	6.25	Vdc
Line Regulation (T_J = +25°C, 8.0 Vdc ≤ V_I ≤ 25 Vdc, I_O = 200 mA)	Reg_{line}	—	5.0	50	mV
Load Regulation (T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	— —	20 10	120 60	mV
Output Voltage (8.0 Vdc ≤ V_I ≤ 25 Vdc, 5.0 mA ≤ I_O ≤ 200 mA) (8.0 Vdc ≤ V_I ≤ 21 Vdc, 5.0 mA ≤ I_O ≤ 350 mA)	V_O	5.7	—	6.3	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	3.2	6.0	mA
Quiescent Current Change (9.0 Vdc ≤ V_I ≤ 25 Vdc, I_O = 200 mA) (5.0 mA ≤ I_O ≤ 350 mA)	ΔI_{IB}	— —	— —	0.8 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	45	—	μV
Ripple Rejection (T suffix only) (I_O = 100 mA, f = 120 Hz, 9.0 V ≤ V_I ≤ 19 V) (I_O = 300 mA, f = 120 Hz, 9.0 V ≤ V_I ≤ 19 V, T_J = 25°C)	RR	59 59	— 80	— —	dB
Dropout Voltage (T_J = +25°C)	V_I-V_O	—	2.0	—	Vdc
Short Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	—	50	—	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	—	±0.2	—	mV/°C
Peak Output Current (T_J = 25°C)	I_O	—	700	—	mA

MC78M08 ELECTRICAL CHARACTERISTICS (V_I = 14 V, I_O = 350 mA, 0°C < T_J < +125°C, P_D ≤ 5.0 W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	7.7	8.0	8.3	Vdc
Line Regulation (T_J = +25°C, 10.5 Vdc ≤ V_I ≤ 25 Vdc, I_O = 200 mA)	Reg_{line}	—	6.0	50	mV
Load Regulation (T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	— —	25 10	160 80	mV
Output Voltage (10.5 Vdc ≤ V_I ≤ 25 Vdc, 5.0 mA ≤ I_O ≤ 200 mA) (10.5 Vdc ≤ V_I ≤ 23 Vdc, 5.0 mA ≤ I_O ≤ 350 mA)	V_O	7.6	—	8.4	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	3.2	6.0	mA
Quiescent Current Change (10.5 Vdc ≤ V_I ≤ 25 Vdc, I_O = 200 mA) (5.0 mA ≤ I_O ≤ 350 mA)	ΔI_{IB}	— —	— —	0.8 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	52	—	μV
Ripple Rejection (T suffix only) (I_O = 100 mA, f = 120 Hz, 11.5 V ≤ V_I ≤ 21.5 V) (I_O = 300 mA, f = 120 Hz, 11.5 V ≤ V_I ≤ 21.5 V, T_J = 25°C)	RR	56 56	— 80	— —	dB
Dropout Voltage (T_J = +25°C)	V_I-V_O	—	2.0	—	Vdc
Short Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	—	50	—	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	—	±0.2	—	mV/°C
Peak Output Current (T_J = 25°C)	I_O	—	700	—	mA

MC78M12 ELECTRICAL CHARACTERISTICS (V_I = 19 V, I_O = 350 mA, 0°C < T_J < +125°C, P_D ≤ 5.0 W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	11.5	12	12.5	Vdc
Line Regulation (T_J = +25°C, 14.5 Vdc ≤ V_I ≤ 30 Vdc, I_O = 200 mA)	Reg_{line}	—	8.0	50	mV
Load Regulation (T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	— —	25 10	240 120	mV
Output Voltage (14.5 Vdc ≤ V_I ≤ 27 Vdc, 5.0 mA ≤ I_O ≤ 350 mA)	V_O	11.4	—	12.6	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	3.2	6.0	mA
Quiescent Current Change (14.5 Vdc ≤ V_I ≤ 30 Vdc, I_O = 200 mA) (5.0 mA ≤ I_O ≤ 350 mA)	ΔI_{IB}	— —	— —	0.8 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	75	—	μV
Ripple Rejection (T, DT and DT-1 suffixes only) (I_O = 100 mA, f = 120 Hz, 15 V ≤ V_I ≤ 25 V) (I_O = 300 mA, f = 120 Hz, 15 V ≤ V_I ≤ 25 V, T_J = 25°C)	RR	55 55	— 80	— —	dB
Dropout Voltage (T_J = +25°C)	V_I-V_O	—	2.0	—	Vdc
Short Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	—	50	—	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	—	±0.3	—	mV/°C
Peak Output Current (T_J = 25°C)	I_O	—	700	—	mA

MC78M15 ELECTRICAL CHARACTERISTICS (V_I = 23 V, I_O = 350 mA, 0°C < T_J < +125°C, P_D ≤ 5.0 W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	14.4	15	15.6	Vdc
Input Regulation (T_J = +25°C, 17.5 Vdc ≤ V_I ≤ 30 Vdc, I_O = 200 mA)	Reg_{line}	—	10	50	mV
Load Regulation (T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	— —	25 10	300 150	mV
Output Voltage (17.5 Vdc ≤ V_I ≤ 30 Vdc, 5.0 mA ≤ I_O ≤ 350 mA)	V_O	14.25	—	15.75	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	3.2	6.0	mA
Quiescent Current Change (17.5 Vdc ≤ V_I ≤ 30 Vdc, I_O = 200 mA) (5.0 mA ≤ I_O ≤ 350 mA)	ΔI_{IB}	— —	— —	0.8 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	90	—	μV
Ripple Rejection (T, DT and DT-1 suffixes only) (I_O = 100 mA, f = 120 Hz, 18.5 V ≤ V_I ≤ 28.5 V) (I_O = 300 mA, f = 120 Hz, 18.5 V ≤ V_I ≤ 28.5 V, T_J = 25°C)	RR	54 54	— 70	— —	dB
Dropout Voltage (T_J = +25°C)	V_I-V_O	—	2.0	—	Vdc
Short Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	—	50	—	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	—	±0.3	—	mV/°C
Peak Output Current (T_J = 25°C)	I_O	—	700	—	mA

MC78M18 ELECTRICAL CHARACTERISTICS (V_I = 27 V, I_O = 350 mA, 0°C < T_J < +125°C, P_D ≤ 5.0 W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	17.3	18	18.7	Vdc
Line Regulation (T_J = +25°C, 21 Vdc ≤ V_I ≤ 33 Vdc, I_O = 200 mA)	Reg_{line}	—	10	50	mV
Load Regulation (T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	— —	30 10	360 180	mV
Output Voltage (21 Vdc ≤ V_I ≤ 33 Vdc, 5.0 mA ≤ I_O ≤ 350 mA)	V_O	17.1	—	18.9	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	3.2	6.5	mA
Quiescent Current Change (21 Vdc ≤ V_I ≤ 33 Vdc, I_O = 200 mA) (5.0 mA ≤ I_O ≤ 350 mA)	ΔI_{IB}	— —	— —	0.8 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	100	—	μV
Ripple Rejection (T suffix only) (I_O = 100 mA, f = 120 Hz, 22 V ≤ V_I ≤ 32 V) (I_O = 300 mA, f = 120 Hz, 22 V ≤ V_I ≤ 32 V, T_J = 25°C)	RR	53 53	— 70	— —	dB
Dropout Voltage (T_J = +25°C)	V_I-V_O	—	2.0	—	Vdc
Short Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	—	50	—	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	—	±0.3	—	mV/°C
Peak Output Current (T_J = 25°C)	I_O	—	700	—	mA

MC78M20 ELECTRICAL CHARACTERISTICS (V_I = 29 V, I_O = 350 mA, 0°C < T_J < +125°C, P_D ≤ 5.0 W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	19.2	20	20.8	Vdc
Line Regulation (T_J = +25°C, 23 Vdc ≤ V_I ≤ 35 Vdc, I_O = 200 mA)	Reg_{line}	—	10	50	mV
Load Regulation (T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	— —	30 10	400 200	mV
Output Voltage (23 Vdc ≤ V_I ≤ 35 Vdc, 5.0 mA ≤ I_O ≤ 350 mA)	V_O	19	—	21	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	3.2	6.5	mA
Quiescent Current Change (23 Vdc ≤ V_I ≤ 35 Vdc, I_O = 200 mA) (5.0 mA ≤ I_O ≤ 350 mA)	ΔI_{IB}	— —	— —	0.8 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	110	—	μV
Ripple Rejection (T suffix only) (I_O = 100 mA, f = 120 Hz, 24 V ≤ V_I ≤ 34 V) (I_O = 300 mA, f = 120 Hz, 24 V ≤ V_I ≤ 34 V, T_J = 25°C)	RR	52 52	— 70	— —	dB
Dropout Voltage (T_J = +25°C)	V_I-V_O	—	2.0	—	Vdc
Short Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	—	50	—	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	—	±0.5	—	mV/°C
Peak Output Current (T_J = 25°C)	I_O	—	700	—	mA

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	23	24	25	Vdc
Line Regulation (T_J = +25°C, 27 Vdc ≤ V_I ≤ 38 Vdc, I_O = 200 mA)	Reg_{line}	—	10	50	mV
Load Regulation (T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	— —	30 10	480 240	mV
Output Voltage (27 Vdc ≤ V_I ≤ 38 Vdc, 5.0 mA ≤ I_O ≤ 350 mA)	V_O	22.8	—	25.2	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	3.2	7.0	mA
Quiescent Current Change (27 Vdc ≤ V_I ≤ 38 Vdc, I_O = 200 mA) (5.0 mA ≤ I_O ≤ 350 mA)	ΔI_{IB}	— —	— —	0.8 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	170	—	μV
Ripple Rejection (T suffix only) (I_O = 100 mA, f = 120 Hz, 28 V ≤ V_I ≤ 38 V) (I_O = 300 mA, f = 120 Hz, 28 V ≤ V_I ≤ 38 V, T_J = 25°C)	RR	50 50	— 70	— —	dB
Dropout Voltage (T_J = +25°C)	V_I-V_O	—	2.0	—	Vdc
Short Circuit Current Limit (T_J = +25°C)	I_{OS}	—	50	—	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	—	±0.5	—	mV/°C
Peak Output Current (T_J = 25°C)	I_O	—	700	—	mA

DEFINITIONS

Line Regulation — The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation — The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation — The maximum total device dissipation for which the regulator will operate within specifications.

Input Bias Current — That part of the input current that is not delivered to the load.

Output Noise Voltage — The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long Term Stability — Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices' electrical characteristics and maximum power dissipation.

TYPICAL PERFORMANCE CURVES

FIGURE 1 — WORST CASE POWER DISSIPATION versus AMBIENT TEMPERATURE TO-220AB (CASE 221A)

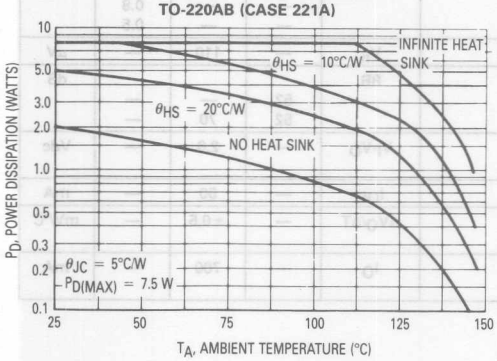
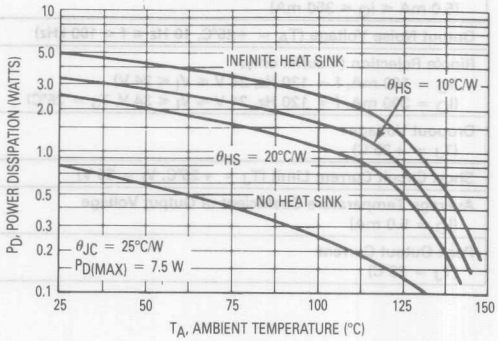


FIGURE 2 — WORST CASE POWER DISSIPATION versus AMBIENT TEMPERATURE (CASE 79)



TYPICAL PERFORMANCE CURVES

FIGURE 3 — PEAK OUTPUT CURRENT versus DROPOUT VOLTAGE

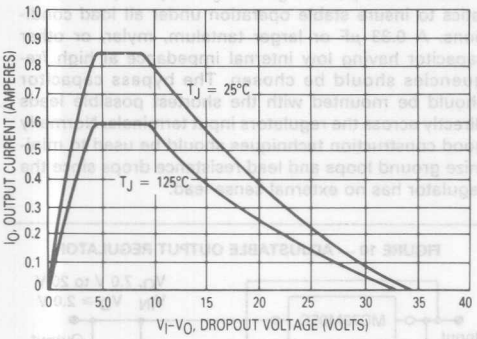


FIGURE 4 — DROPOUT VOLTAGE versus JUNCTION TEMPERATURE

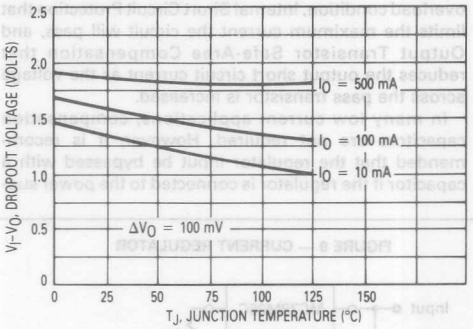


FIGURE 5 — RIPPLE REJECTION versus FREQUENCY

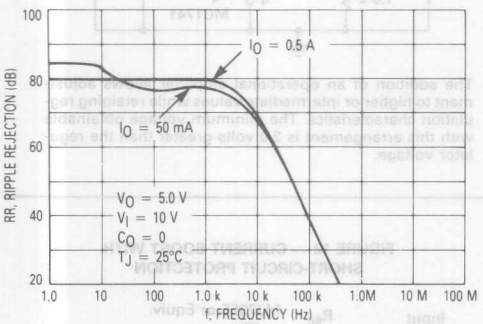


FIGURE 6 — RIPPLE REJECTION versus OUTPUT CURRENT

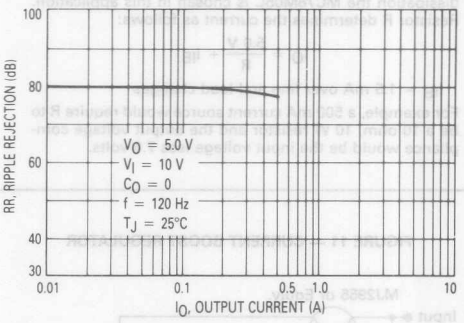


FIGURE 7 — BIAS CURRENT versus INPUT VOLTAGE

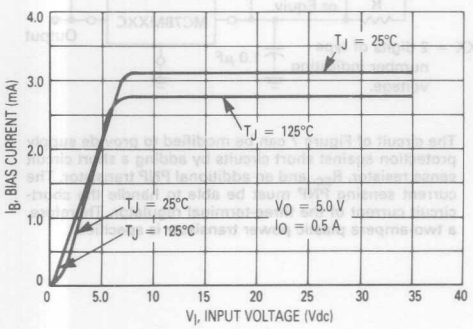
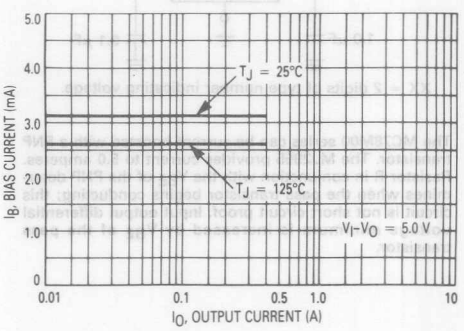


FIGURE 8 — BIAS CURRENT versus OUTPUT CURRENT



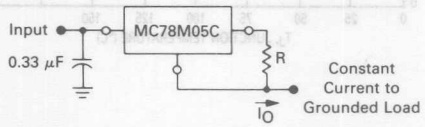
APPLICATIONS INFORMATION

DESIGN CONSIDERATIONS

The MC78M00 Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

FIGURE 9 — CURRENT REGULATOR



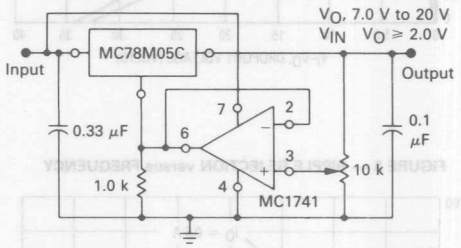
The MC78M00 regulators can also be used as a current source when connected as above. In order to minimize dissipation the MC78M05C is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5.0\ V}{R} + I_{IB}$$

I_{IB} = 1.5 mA over line and load changes

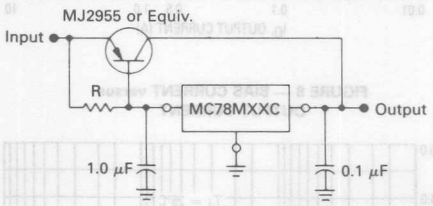
For example, a 500 mA current source would require R to be a 10 ohm, 10 W resistor and the output voltage compliance would be the input voltage less 7.0 volts.

FIGURE 10 — ADJUSTABLE OUTPUT REGULATOR



The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 2.0 volts greater than the regulator voltage.

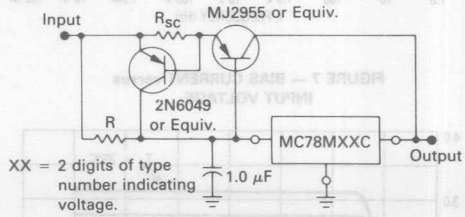
FIGURE 11 — CURRENT BOOST REGULATOR



XX = 2 digits of type number indicating voltage.

The MC78M00 series can be current boosted with a PNP transistor. The MJ2955 provides current to 5.0 amperes. Resistor R in conjunction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short circuit proof. Input output differential voltage minimum is increased by V_{BE} of the pass transistor.

FIGURE 12 — CURRENT BOOST WITH SHORT-CIRCUIT PROTECTION



XX = 2 digits of type number indicating voltage.

The circuit of Figure 7 can be modified to provide supply protection against short circuits by adding a short circuit sense resistor, R_{SC}, and an additional PNP transistor. The current sensing PNP must be able to handle the short-circuit current of the three-terminal regulator. Therefore, a two-ampere plastic power transistor is specified.

MOTOROLA

MC78T00 Series

Specifications and Applications Information

3

THREE-AMPERE POSITIVE VOLTAGE REGULATORS

This family of fixed voltage regulators are monolithic integrated circuits capable of driving loads in excess of 3.0 amperes. These three-terminal regulators employ internal current limiting, thermal shutdown, and safe-area compensation. Devices are available with improved specifications, including a 2% output voltage tolerance, on AC-suffix 5.0, 12 and 15 volt device types.

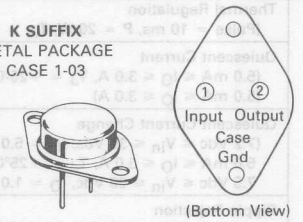
Although designed primarily as a fixed voltage regulator, these devices can be used with external components to obtain adjustable voltages and currents. This series of devices can be used with a series-pass transistor to supply up to 15 amperes at the nominal output voltage.

- Output Current in Excess of 3.0 Amperes
- Power Dissipation: 30 W (K-Suffix), 25 W (T-Suffix)
- No External Components Required
- Output Voltage Offered in 2% and 4% Tolerance*
- Thermal Regulation is Specified
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation

THREE-AMPERE POSITIVE FIXED VOLTAGE REGULATORS

SILICON MONOLITHIC INTEGRATED CIRCUIT

K SUFFIX
METAL PACKAGE
CASE 1-03



PIN 1. INPUT
2. OUTPUT
CASE GROUND

T SUFFIX
PLASTIC PACKAGE
CASE 221A-04



(Heatsink surface connected to Pin 2)

PIN 1. INPUT
2. GROUND
3. OUTPUT

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (5.0 V–12 V) (15 V)	V_{in}	35 40	Vdc
Power Dissipation and Thermal Characteristics			
Plastic Package (Note 1)			
T_A = +25°C	P_D	Internally Limited	
Thermal Resistance, Junction to Air	$R_{\theta JA}$	65	°C/W
T_C = +25°C	P_D	Internally Limited	
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W
Metal Package (Note 1)			
T_A = +25°C	P_D	Internally Limited	
Thermal Resistance, Junction to Air	$R_{\theta JA}$	35	°C/W
T_C = +25°C	P_D	Internally Limited	
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W
Storage Junction Temperature Range	T_{stg}	−65 to +150	°C
Operating Junction Temperature Range MC78T00C, AC	T_J	0 to +150	°C

NOTE:
1. Although power dissipation is internally limited, specifications apply only for $P_O \leq P_{max}$.
P_{max} = 30 W for K package
P_{max} = 25 W for T package.

TYPE NO./VOLTAGE			
MC78T05	5.0 Volts	MC78T12	12 Volts
MC78T08	8.0 Volts	MC78T15	15 Volts

ORDERING INFORMATION

Device	Output Voltage Tolerance	Tested Operating Junction Temp. Range	Package
MC78TXXCK MC78TXXACK	4% 2%*	0 to +125°C	Metal Power
MC78TXXCT MC78TXXACT	4% 2%*	0 to +125°C	Plastic Power
MC78TXXBT# MC78TXXABT#	4% 2%*	−40 to +125°C	Plastic Power

XX Indicates nominal voltage.
* 2% regulators are available in 5, 12 and 15 volt devices.
#Automotive temperature range selections are available with special test conditions and additional tests. Contact your local Motorola sales office for information.

ELECTRICAL CHARACTERISTICS (V_{in} = 10 V, I_O = 3.0 A, 0°C ≤ T_J ≤ 125°C, P_O ≤ P_{max} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC78T05AC			MC78T05C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A; 5.0 mA ≤ I_O ≤ 2.0 A, 7.3 Vdc ≤ V_{in} ≤ 20 Vdc)	V_O	 4.9 4.8	 5.0 5.0	 5.1 5.2	 4.8 4.75	 5.0 5.0	 5.2 5.25	Vdc
Line Regulation (Note 2) (7.2 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 5.0 mA, T_J = +25°C; 7.2 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 1.0 A, T_J = +25°C; 8.0 Vdc ≤ V_{in} ≤ 12 Vdc, I_O = 3.0 A, T_J = +25°C; 7.5 Vdc ≤ V_{in} ≤ 20 Vdc, I_O = 1.0 A)	Reg_{line}	—	3.0	25	—	3.0	25	mV
Load Regulation (Note 2) (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A)	Reg_{load}	 —	 10	 30	 —	 10	 30	mV
		—	15	80	—	15	80	
Thermal Regulation (Pulse = 10 ms, P = 20 W, T_A = +25°C)	Reg_{therm}	—	0.001	0.01	—	0.002	0.03	%V_O/W
Quiescent Current (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A)	I_B	 —	 3.5	 5.0	 —	 3.5	 5.0	mA
		—	4.0	6.0	—	4.0	6.0	
Quiescent Current Change (7.2 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 5.0 mA, T_J = +25°C; 5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C; 7.5 Vdc ≤ V_{in} ≤ 20 Vdc, I_O = 1.0 A)	ΔI_B	—	0.3	1.0	—	0.3	1.0	mA
Ripple Rejection (8.0 Vdc ≤ V_{in} ≤ 18 Vdc, f = 120 Hz, I_O = 2.0 A, T_J = 25°C)	RR	62	75	—	62	75	—	dB
Dropout Voltage (I_O = 3.0 A, T_J = +25°C)	V_{in}–V_O	—	2.2	2.5	—	2.2	2.5	Vdc
Output Noise Voltage (10 Hz ≤ f ≤ 100 kHz, T_J = +25°C)	V_n	—	10	—	—	10	—	μV/V_O
Output Resistance (f = 1.0 kHz)	R_O	—	2.0	—	—	2.0	—	mΩ
Short Circuit Current Limit (V_{in} = 35 Vdc, T_J = +25°C)	I_{SC}	—	1.5	—	—	1.5	—	A
Peak Output Current (T_J = +25°C)	I_{max}	—	5.0	—	—	5.0	—	A
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	TCV_O	—	0.2	—	—	0.2	—	mV/°C

NOTES:

1. Although power dissipation is internally limited, specifications apply only for P_O ≤ P_{max}.
   P_{max} = 30 W for K package P_{max} = 25 W for T package
2. Line and load regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC78T08C

ELECTRICAL CHARACTERISTICS (V_{in} = 13 V, I_O = 3.0 A, 0°C ≤ T_J ≤ 125°C, P_O ≤ P_{max} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC78T08C Min	MC78T08C Typ	MC78T08C Max	Unit
Output Voltage (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A; 5.0 mA ≤ I_O ≤ 2.0 A, 10.4 Vdc ≤ V_{in} ≤ 23 Vdc)	V_O	 7.7 7.6	 8.0 8.0	 8.3 8.4	Vdc
Line Regulation (Note 2) (10.3 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 5.0 mA, T_J = +25°C; 10.3 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 1.0 A, T_J = +25°C; 11 Vdc ≤ V_{in} ≤ 17 Vdc, I_O = 3.0 A, T_J = +25°C; 10.7 Vdc ≤ V_{in} ≤ 23 Vdc, I_O = 1.0 A)	Reg_{line}	—	4.0	35	mV
Load Regulation (Note 2) (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A)	Reg_{load}	 —	 10	 30	mV
		—	15	80	
Thermal Regulation (Pulse = 10 ms, P = 20 W, T_A = +25°C)	Reg_{therm}	—	0.002	0.03	%V_O/W
Quiescent Current (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A)	I_B	 —	 3.5	 5.0	mA
		—	4.0	6.0	
Quiescent Current Change (10.3 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 5.0 mA, T_J = +25°C; 5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C; 10.7 Vdc ≤ V_{in} ≤ 23 Vdc, I_O = 1.0 A)	ΔI_B	—	0.3	1.0	mA
Ripple Rejection (11 Vdc ≤ V_{in} ≤ 21 Vdc, f = 120 Hz, I_O = 2.0 A, T_J = 25°C)	RR	60	71	—	dB
Dropout Voltage (I_O = 3.0 A, T_J = +25°C)	V_{in}–V_O	—	2.2	2.5	Vdc
Output Noise Voltage (10 Hz ≤ f ≤ 100 kHz, T_J = +25°C)	V_n	—	10	—	μV/V_O
Output Resistance (f = 1.0 kHz)	R_O	—	2.0	—	mΩ
Short Circuit Current Limit (V_{in} = 35 Vdc, T_J = +25°C)	I_{SC}	—	1.5	—	A
Peak Output Current (T_J = +25°C)	I_{max}	—	5.0	—	A
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	TCV_O	—	0.3	—	mV/°C

NOTES:

1. Although power dissipation is internally limited, specifications apply only for P_O ≤ P_{max}.
   P_{max} = 30 W for K package P_{max} = 25 W for T package
2. Line and load regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

3

MC78T12AC, C

ELECTRICAL CHARACTERISTICS (V_{in} = 17 V, I_O = 3.0 A, 0°C ≤ T_J ≤ 125°C, P_O ≤ P_{max} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC78T12AC			MC78T12C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A; 5.0 mA ≤ I_O ≤ 2.0 A, 14.5 Vdc ≤ V_{in} ≤ 27 Vdc)	V_O	11.75 11.5	12 12	12.25 12.5	11.5 11.4	12 12	12.5 12.6	Vdc
Line Regulation (Note 2) (14.5 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 5.0 mA, T_J = +25°C; 14.5 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 1.0 A, T_J = +25°C; 16 Vdc ≤ V_{in} ≤ 22 Vdc, I_O = 3.0 A, T_J = +25°C; 14.9 Vdc ≤ V_{in} ≤ 27 Vdc, I_O = 1.0 A)	Reg_{line}	—	6.0	45	—	6.0	45	mV
Load Regulation (Note 2) (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A)	Reg_{load}	— —	10 15	30 80	— —	10 15	30 80	mV
Thermal Regulation (Pulse = 10 ms, P = 20 W, T_A = +25°C)	Reg_{therm}	—	0.001	0.01	—	0.002	0.03	%V_O/W
Quiescent Current (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A)	I_B	— —	3.5 4.0	5.0 6.0	— —	3.5 4.0	5.0 6.0	mA
Quiescent Current Change (14.5 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 5.0 mA, T_J = +25°C; 5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C; 14.9 Vdc ≤ V_{in} ≤ 27 Vdc, I_O = 1.0 A)	ΔI_B	—	0.3	1.0	—	0.3	1.0	mA
Ripple Rejection (15 Vdc ≤ V_{in} ≤ 25 Vdc, f = 120 Hz, I_O = 2.0 A, T_J = 25°C)	RR	57	67	—	57	67	—	dB
Dropout Voltage (I_O = 3.0 A, T_J = +25°C)	V_{in}–V_O	—	2.2	2.5	—	2.2	2.5	Vdc
Output Noise Voltage (10 Hz ≤ f ≤ 100 kHz, T_J = +25°C)	V_n	—	10	—	—	10	—	μV/V_O
Output Resistance (f = 1.0 kHz)	R_O	—	2.0	—	—	2.0	—	mΩ
Short Circuit Current Limit (V_{in} = 35 Vdc, T_J = +25°C)	I_{SC}	—	1.5	—	—	1.5	—	A
Peak Output Current (T_J = +25°C)	I_{max}	—	5.0	—	—	5.0	—	A
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	TCV_O	—	0.5	—	—	0.5	—	mV/°C

NOTES:
1. Although power dissipation is internally limited, specifications apply only for P_O ≤ P_{max}.
   P_{max} = 30 W for K package P_{max} = 25 W for T package
2. Line and load regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

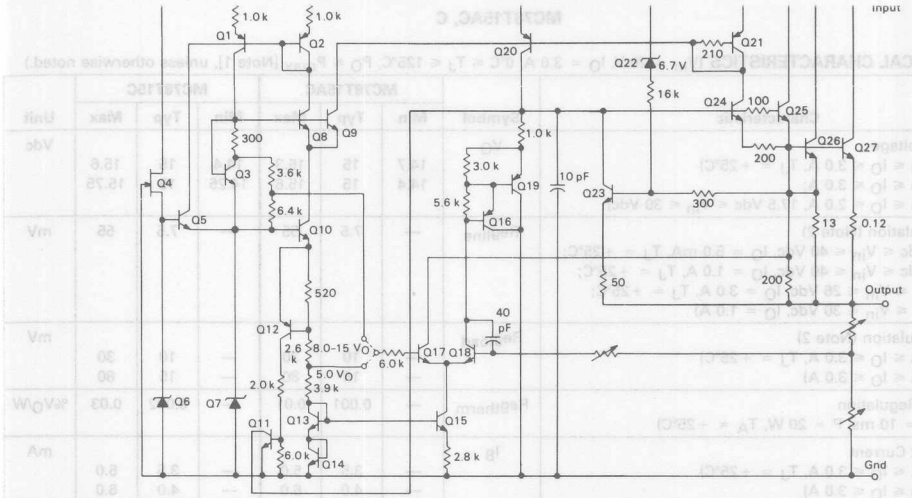
MC78T15AC, C

ELECTRICAL CHARACTERISTICS (V_{in} = 20 V, I_O = 3.0 A, 0°C ≤ T_J ≤ 125°C, P_O ≤ P_{max} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC78T15AC			MC78T15C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A; 5.0 mA ≤ I_O ≤ 2.0 A, 17.5 Vdc ≤ V_{in} ≤ 30 Vdc)	V_O	 14.7 14.4	 15 15	 15.3 15.6	 14.4 14.25	 15 15	 15.6 15.75	Vdc
Line Regulation (Note 2) (17.6 Vdc ≤ V_{in} ≤ 40 Vdc, I_O = 5.0 mA, T_J = +25°C; 17.6 Vdc ≤ V_{in} ≤ 40 Vdc, I_O = 1.0 A, T_J = +25°C; 20 Vdc ≤ V_{in} ≤ 26 Vdc, I_O = 3.0 A, T_J = +25°C; 18 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 1.0 A)	Reg_{line}	—	7.5	55	—	7.5	55	mV
Load Regulation (Note 2) (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A)	Reg_{load}	 — —	 10 15	 30 80	 — —	 10 15	 30 80	mV
Thermal Regulation (Pulse = 10 ms, P = 20 W, T_A = +25°C)	Reg_{therm}	—	0.001	0.01	—	0.002	0.03	%V_O/W
Quiescent Current (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A)	I_B	 — —	 3.5 4.0	 5.0 6.0	 — —	 3.5 4.0	 5.0 6.0	mA
Quiescent Current Change (17.6 Vdc ≤ V_{in} ≤ 40 Vdc, I_O = 5.0 mA, T_J = +25°C; 5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C; 18 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 1.0 A)	ΔI_B	—	0.3	1.0	—	0.3	1.0	mA
Ripple Rejection (18.5 Vdc ≤ V_{in} ≤ 28.5 Vdc, f = 120 Hz, I_O = 2.0 A, T_J = 25°C)	RR	55	65	—	55	65	—	dB
Dropout Voltage (I_O = 3.0 A, T_J = +25°C)	V_{in}–V_O	—	2.2	2.5	—	2.2	2.5	Vdc
Output Noise Voltage (10 Hz ≤ f ≤ 100 kHz, T_J = +25°C)	V_n	—	10	—	—	10	—	μV/V_O
Output Resistance (f = 1.0 kHz)	R_O	—	2.0	—	—	2.0	—	mΩ
Short Circuit Current Limit (V_{in} = 40 Vdc, T_J = +25°C)	I_{SC}	—	1.0	—	—	1.0	—	A
Peak Output Current (T_J = +25°C)	I_{max}	—	5.0	—	—	5.0	—	A
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	TCV_O	—	0.6	—	—	0.6	—	mV/°C

NOTES:

1. Although power dissipation is internally limited, specifications apply only for P_O ≤ P_{max}.
   P_{max} = 30 W for K package P_{max} = 25 W for T package
2. Line and load regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.



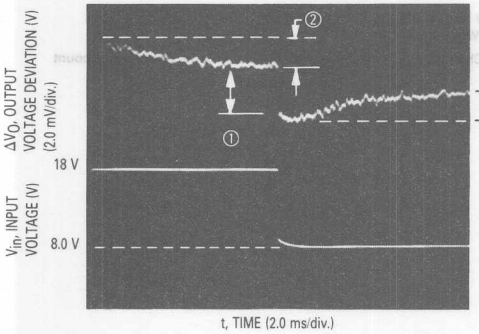
VOLTAGE REGULATOR PERFORMANCE

The performance of a voltage regulator is specified by its immunity to changes in load, input voltage, power dissipation, and temperature. Line and load regulation are tested with a pulse of short duration ($< 100\ \mu s$) and are strictly a function of electrical gain. However, pulse widths of longer duration (> 1.0 ms) are sufficient to affect temperature gradients across the die. These temperature gradients can cause a change in the output voltage, in addition to changes caused by line and load regulation. Longer pulse widths and thermal gradients make it desirable to specify thermal regulation.

Thermal regulation is defined as the change in output voltage caused by a change in dissipated power for a specified time, and is expressed as a percentage output voltage change per watt. The change in dissipated power can be caused by a change in either the input voltage or the load current. Thermal regulation is a function of I.C. layout and die attach techniques, and usually occurs within 10 ms of a change in power dissipation. After 10 ms, additional changes in the output voltage are due to the temperature coefficient of the device.

Figure 1 shows the line and thermal regulation response of a typical MC78T05AC to a 20 watt input pulse. The variation of the output voltage due to line regulation is labeled ① and the thermal regulation component is labeled ②. Figure 2 shows the load and thermal regulation response of a typical MC78T05AC to a 20 watt load pulse. The output voltage variation due to load regulation is labeled ① and the thermal regulation component is labeled ②.

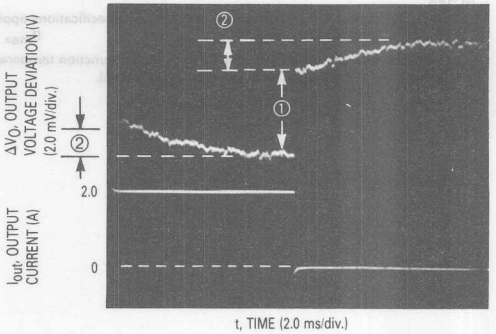
FIGURE 1 — LINE AND THERMAL REGULATION



MC78T05AC
$V_O = 5.0$ V
$V_{in} = 8.0$ V → 18 V → 8.0 V
$I_{out} = 2.0$ A

① = Reg_{line} = 2.4 mV
② = Reg_{therm} = 0.0015%V_O/W

FIGURE 2 — LOAD AND THERMAL REGULATION



MC78T05AC
$V_O = 5.0$ V
$V_{in} = 15$
$I_{out} = 0$ A → 2.0 A → 0 A

① = Reg_{load} = 4.4 mV
② = Reg_{therm} = 0.0015%V_O/W

FIGURE 3 — TEMPERATURE STABILITY

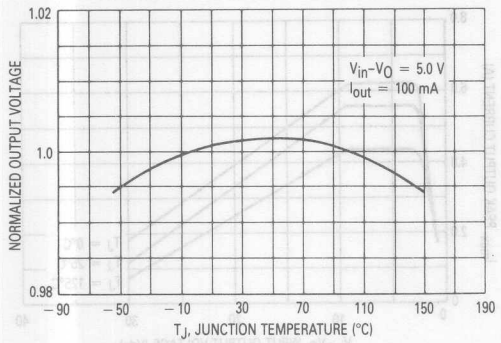


FIGURE 4 — OUTPUT IMPEDANCE

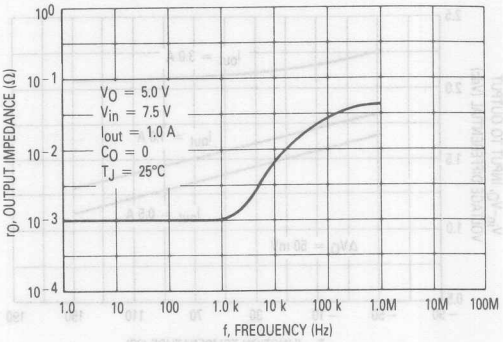


FIGURE 5 — RIPPLE REJECTION versus FREQUENCY

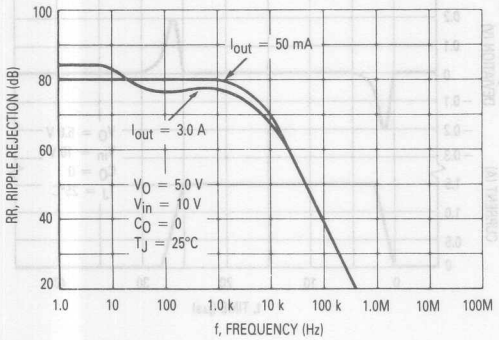


FIGURE 6 — RIPPLE REJECTION versus OUTPUT CURRENT

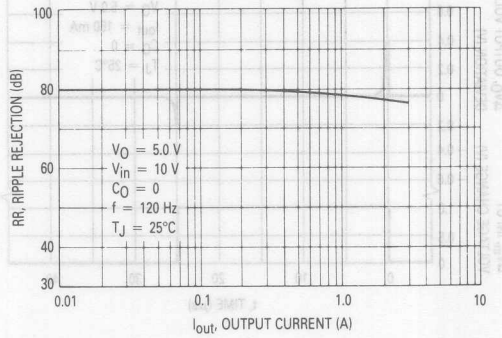


FIGURE 7 — QUIESCENT CURRENT versus INPUT VOLTAGE

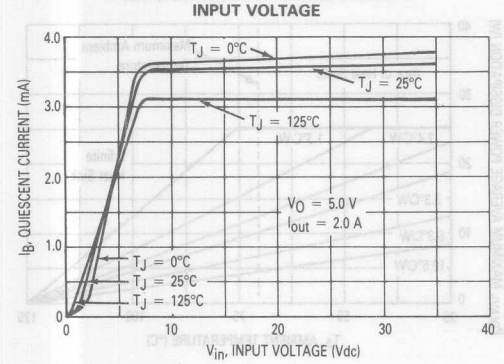
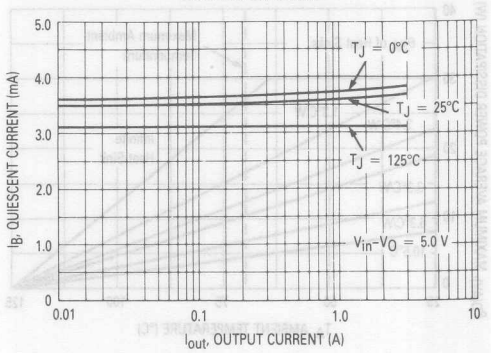


FIGURE 8 — QUIESCENT CURRENT versus OUTPUT CURRENT



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FIGURE 9 — DROPOUT VOLTAGE

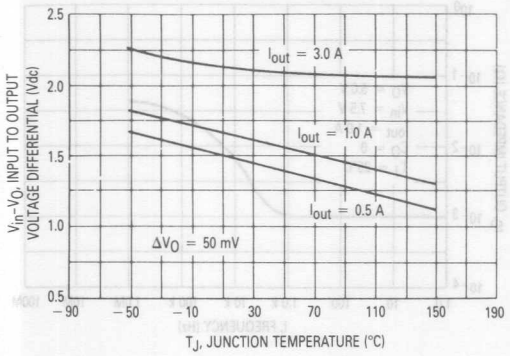


FIGURE 10 — PEAK OUTPUT CURRENT

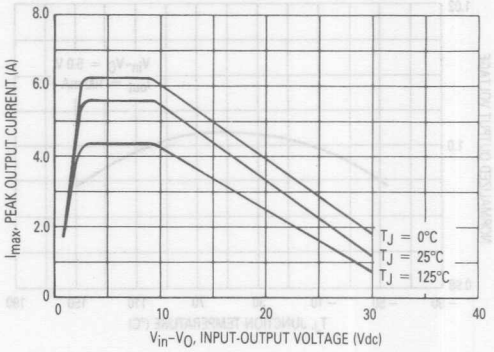


FIGURE 11 — LINE TRANSIENT RESPONSE

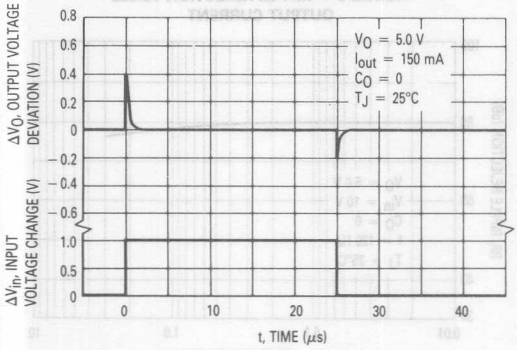


FIGURE 12 — LOAD TRANSIENT RESPONSE

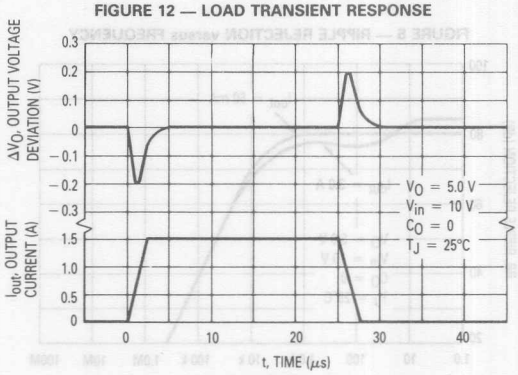


FIGURE 13 — MAXIMUM AVERAGE POWER DISSIPATION FOR MC78T00CK, ACK

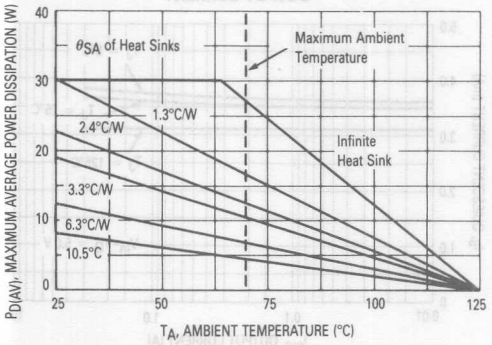
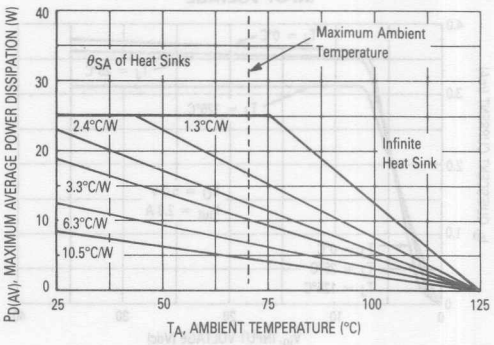


FIGURE 14 — MAXIMUM AVERAGE POWER DISSIPATION FOR MC78T00CT, ACT



APPLICATIONS INFORMATION

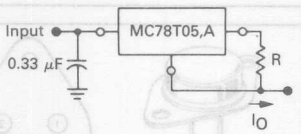
DESIGN CONSIDERATIONS

The MC78T00,A Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulator's input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

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FIGURE 15 — CURRENT REGULATOR



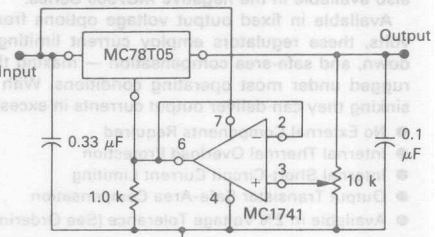
The MC78T05 regulator can also be used as a current source when connected as above. In order to minimize dissipation, the MC78T05 is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5.0\ V}{R} + I_B$$

$\Delta I_B \cong 0.7$ mA over line, load and temperature changes
$I_B \cong 3.5$ mA

For example, a 2-ampere current source would require R to be a 2.5 ohm, 15 W resistor and the output voltage compliance would be the input voltage less 7.5 volts.

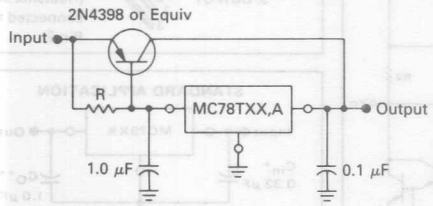
FIGURE 16 — ADJUSTABLE OUTPUT REGULATOR



V_O, 8.0 V to 20 V
$V_{in}-V_O \geq 2.5$ V

The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 3.0 volts greater than the regulator voltage.

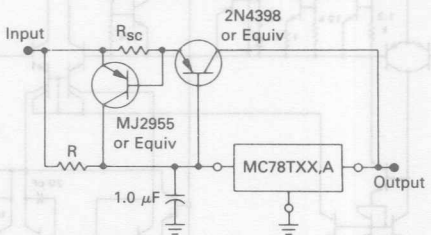
FIGURE 17 — CURRENT BOOST REGULATOR



XX = 2 digits of type number indicating voltage.

The MC78T00,A series can be current boosted with a PNP transistor. The 2N4398 provides current to 15 amperes. Resistor R in conjunction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short-circuit proof. Input-output differential voltage minimum is increased by the V_{BE} of the pass transistor.

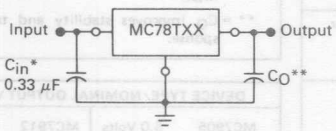
FIGURE 18 — CURRENT BOOST WITH SHORT-CIRCUIT PROTECTION



XX = 2 digits of type number indicating voltage.

The circuit of Figure 17 can be modified to provide supply protection against short circuits by adding a short-circuit sense resistor, R_{SC}, and an additional PNP transistor. The current sensing PNP must be able to handle the short-circuit current of the three-terminal regulator. Therefore, an eight-ampere power transistor is specified.

STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.2 V above the output voltage even during the low point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter. (See Applications Information for details.)

** = C_O is not needed for stability; however, it does improve transient response.

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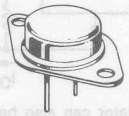
THREE-TERMINAL NEGATIVE VOLTAGE REGULATORS

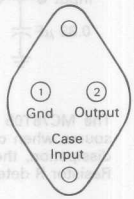
The MC7900 Series of fixed output negative voltage regulators are intended as complements to the popular MC7800 Series devices. These negative regulators are available in the same seven-voltage options as the MC7800 devices. In addition, one extra voltage option commonly employed in MECL systems is also available in the negative MC7900 Series.

Available in fixed output voltage options from −5.0 to −24 volts, these regulators employ current limiting, thermal shutdown, and safe-area compensation — making them remarkably rugged under most operating conditions. With adequate heat-sinking they can deliver output currents in excess of 1.0 ampere.

- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Available in 2% Voltage Tolerance (See Ordering Information)

THREE-TERMINAL NEGATIVE FIXED VOLTAGE REGULATORS

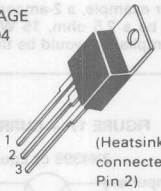




K SUFFIX
METAL PACKAGE
CASE 1-03

(Bottom View)

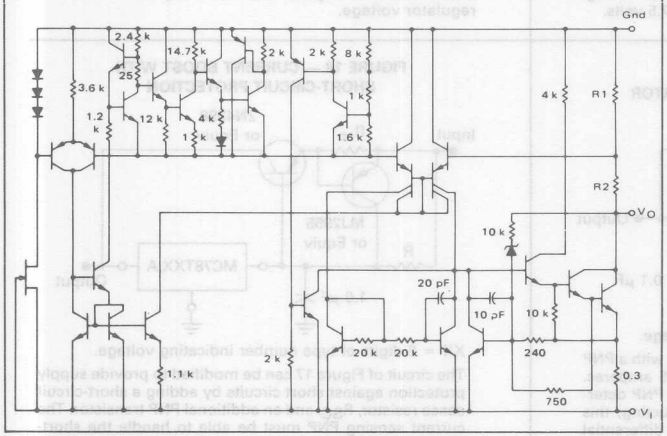
T SUFFIX
PLASTIC PACKAGE
CASE 221A-04



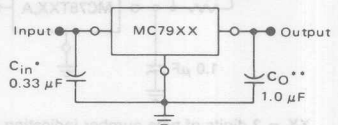
PIN 1. GROUND
2. INPUT
3. OUTPUT

(Heatsink surface connected to Pin 2)

SCHEMATIC DIAGRAM



STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V more negative even during the high point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O improves stability and transient response.

ORDERING INFORMATION

Device	Output Voltage Tolerance	Tested Operating Junction Temp. Range	Package
MC79XXCK	4%	T_J = 0°C to +125°C	Metal Power**
MC79XXACK*	2%		
MC79XXCT	4%		Plastic Power
MC79XXACT*	2%		
MC79XXBT#	4%	T_J = −40°C to +125°C	

XX indicates nominal voltage.
*2% output voltage tolerance available in 5, 12 and 15 volt devices.
**Metal power package available in 5, 12 and 15 volt devices.
#Automotive temperature range selections are available with special test conditions and additional tests in 5, 12 and 15 volt devices. Contact your local Motorola sales office for information.

DEVICE TYPE/NOMINAL OUTPUT VOLTAGE			
MC7905	5.0 Volts	MC7912	12 Volts
MC7905.2	5.2 Volts	MC7915	15 Volts
MC7906	6.0 Volts	MC7918	18 Volts
MC7908	8.0 Volts	MC7924	24 Volts

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (-5.0 V ≥ V_o ≥ -18 V) (24 V)	V_I	-35 -40	Vdc
Power Dissipation Plastic Package T_A = +25°C Derate above T_A = +25°C	P_D $1/R_{\theta JA}$	Internally Limited 15.4	Watts mW/°C
T_C = +25°C Derate above T_C = +95°C (See Figure 1)	P_D $1/R_{\theta JC}$	Internally Limited 200	Watts mW/°C
Metal Package T_A = +25°C Derate above T_A = +25°C	P_D $1/R_{\theta JA}$	Internally Limited 22.2	Watts mW/°C
T_C = +25°C Derate above T_C = +65°C	P_D $1/R_{\theta JC}$	Internally Limited 182	Watts mW/°C
Storage Junction Temperature Range	T_{stg}	-65 to +150	°C
Junction Temperature Range	T_J	0 to +150	°C

THERMAL CHARACTERISTICS

Characteristic		Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	— Plastic Package — Metal Package	$R_{\theta JA}$	65 45	°C/W
Thermal Resistance, Junction to Case	— Plastic Package — Metal Package	$R_{\theta JC}$	5.0 5.5	°C/W

MC7905C ELECTRICAL CHARACTERISTICS (V_I = -10 V, I_O = 500 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-4.8	-5.0	-5.2	Vdc
Line Regulation (Note 1) (T_J = +25°C, I_O = 100 mA) -7.0 Vdc ≥ V_I ≥ -25 Vdc -8.0 Vdc ≥ V_I ≥ -12 Vdc (T_J = +25°C, I_O = 500 mA) -7.0 Vdc ≥ V_I ≥ -25 Vdc -8.0 Vdc ≥ V_I ≥ -12 Vdc	Reg_{line}	 — — — —	 7.0 2.0 35 8.0	 50 25 100 50	mV
Load Regulation (T_J = +25°C) (Note 1) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 — —	 11 4.0	 100 50	mV
Output Voltage -7.0 Vdc ≥ V_I ≥ -20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	-4.75	—	-5.25	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	4.3	8.0	mA
Input Bias Current Change -7.0 Vdc ≥ V_I ≥ -25 Vdc 5.0 mA ≤ I_O ≤ 1.5 A	ΔI_{IB}	 — —	 — —	 1.3 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	—	40	—	μV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	—	70	—	dB
Dropout Voltage I_O = 1.0 A, T_J = +25°C	V_I-V_O	—	2.0	—	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	—	-1.0	—	mV/°C

Note:
1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7905AC ELECTRICAL CHARACTERISTICS (V_I = -10 V, I_O = 500 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-4.9	-5.0	-5.1	Vdc
Line Regulation (Note 1)	Reg_{line}				mV
-8.0 Vdc ≥ V_I ≥ -12 Vdc; I_O = 1.0 A, T_J = 25°C		—	2.0	25	
-8.0 Vdc ≥ V_I ≥ -12 Vdc; I_O = 1.0 A		—	7.0	50	
-7.5 Vdc ≥ V_I ≥ -25 Vdc; I_O = 500 mA		—	7.0	50	
-7.0 Vdc ≥ V_I ≥ -20 Vdc; I_O = 1.0 A, T_J = +25°C		—	6.0	50	
Load Regulation (Note 1)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C		—	11	100	
250 mA ≤ I_O ≤ 750 mA		—	4.0	50	
5.0 mA ≤ I_O ≤ 1.0 A		—	9.0	100	
Output Voltage -7.5 Vdc ≥ V_I ≥ -20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	-4.80	—	-5.20	Vdc
Input Bias Current	I_{IB}	—	4.4	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
-7.5 Vdc ≥ V_I ≥ -25 Vdc		—	—	1.3	
5.0 mA ≤ I_O ≤ 1.0 A		—	—	0.5	
5.0 mA ≤ I_O ≤ 1.5 A, T_J = 25°C		—	—	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	—	40	—	μV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	—	70	—	dB
Dropout Voltage I_O = 1.0 A, T_J = +25°C	V_I-V_O	—	2.0	—	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	—	-1.0	—	mV/°C

MC7905.2C ELECTRICAL CHARACTERISTICS (V_I = -10 V, I_O = 500 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-5.0	-5.2	-5.4	Vdc
Line Regulation (Note 1)	Reg_{line}				mV
(T_J = +25°C, I_O = 100 mA)					
-7.2 Vdc ≥ V_I ≥ -25 Vdc		—	8.0	52	
-8.0 Vdc ≥ V_I ≥ -12 Vdc		—	2.2	27	
(T_J = +25°C, I_O = 500 mA)					
-7.2 Vdc ≥ V_I ≥ -25 Vdc		—	37	105	
-8.0 Vdc ≥ V_I ≥ -12 Vdc		—	8.5	52	
Load Regulation (T_J = +25°C) (Note 1)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.5 A		—	12	105	
250 mA ≤ I_O ≤ 750 mA		—	4.5	52	
Output Voltage -7.2 Vdc ≥ V_I ≥ -20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	-4.95	—	-5.45	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	4.3	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
-7.2 Vdc ≥ V_I ≥ -25 Vdc		—	—	1.3	
5.0 mA ≤ I_O ≤ 1.5 A		—	—	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	—	42	—	μV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	—	68	—	dB
Dropout Voltage I_O = 1.0 A, T_J = +25°C	V_I-V_O	—	2.0	—	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	—	-1.0	—	mV/°C

Note:
1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7906C ELECTRICAL CHARACTERISTICS (V_I = -11 V, I_O = 500 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-5.75	-6.0	-6.25	Vdc
Line Regulation (Note 1)	Reg_{line}				mV
(T_J = +25°C, I_O = 100 mA)					
-8.0 Vdc ≥ V_I ≥ -25 Vdc		—	9.0	60	
-9.0 Vdc ≥ V_I ≥ -13 Vdc		—	3.0	30	
(T_J = +25°C, I_O = 500 mA)					
-8.0 Vdc ≥ V_I ≥ -25 Vdc		—	43	120	
-9.0 Vdc ≥ V_I ≥ -13 Vdc		—	10	60	
Load Regulation (T_J = +25°C) (Note 1)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.5 A		—	13	120	
250 mA ≤ I_O ≤ 750 mA		—	5.0	60	
Output Voltage	V_O	-5.7	—	-6.3	Vdc
-8.0 Vdc ≥ V_I ≥ -21 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W					
Input Bias Current (T_J = +25°C)	I_{IB}	—	4.3	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
-8.0 Vdc ≥ V_I ≥ -25 Vdc		—	—	1.3	
5.0 mA ≤ I_O ≤ 1.5 A		—	—	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	—	45	—	μV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	—	65	—	dB
Dropout Voltage	V_I-V_O	—	2.0	—	Vdc
I_O = 1.0 A, T_J = +25°C					
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$	—	-1.0	—	mV/°C
I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C					

MC7908C ELECTRICAL CHARACTERISTICS (V_I = -14 V, I_O = 500 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-7.7	-8.0	-8.3	Vdc
Line Regulation (Note 1)	Reg_{line}				mV
(T_J = +25°C, I_O = 100 mA)					
-10.5 Vdc ≥ V_I ≥ -25 Vdc		—	12	80	
-11 Vdc ≥ V_I ≥ -17 Vdc		—	5.0	40	
(T_J = +25°C, I_O = 500 mA)					
-10.5 Vdc ≥ V_I ≥ -25 Vdc		—	50	160	
-11 Vdc ≥ V_I ≥ -17 Vdc		—	22	80	
Load Regulation (T_J = +25°C) (Note 1)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.5 A		—	26	160	
250 mA ≤ I_O ≤ 750 mA		—	9.0	80	
Output Voltage	V_O	-7.6	—	-8.4	Vdc
-10.5 Vdc ≥ V_I ≥ -23 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W					
Input Bias Current (T_J = +25°C)	I_{IB}	—	4.3	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
-10.5 Vdc ≥ V_I ≥ -25 Vdc		—	—	1.0	
5.0 mA ≤ I_O ≤ 1.5 A		—	—	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	—	52	—	μV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	—	62	—	dB
Dropout Voltage	V_I-V_O	—	2.0	—	Vdc
I_O = 1.0 A, T_J = +25°C					
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$	—	-1.0	—	mV/°C
I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C					

Note:
1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7912C ELECTRICAL CHARACTERISTICS (V_I = -19 V, I_O = 500 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-11.5	-12	-12.5	Vdc
Line Regulation (Note 1)	Reg_{line}				mV
(T_J = +25°C, I_O = 100 mA)					
-14.5 Vdc ≥ V_I ≥ -30 Vdc		—	13	120	
-16 Vdc ≥ V_I ≥ -22 Vdc		—	6.0	60	
(T_J = +25°C, I_O = 500 mA)					
-14.5 Vdc ≥ V_I ≥ -30 Vdc		—	55	240	
-16 Vdc ≥ V_I ≥ -22 Vdc		—	24	120	
Load Regulation (T_J = +25°C) (Note 1)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.5 A		—	46	240	
250 mA ≤ I_O ≤ 750 mA		—	17	120	
Output Voltage	V_O	-11.4	—	-12.6	Vdc
-14.5 Vdc ≥ V_I ≥ -27 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W					
Input Bias Current (T_J = +25°C)	I_{IB}	—	4.4	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
-14.5 Vdc ≥ V_I ≥ -30 Vdc		—	—	1.0	
5.0 mA ≤ I_O ≤ 1.5 A		—	—	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	—	75	—	μV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	—	61	—	dB
Dropout Voltage	V_I-V_O	—	2.0	—	Vdc
I_O = 1.0 A, T_J = +25°C					
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$	—	-1.0	—	mV/°C
I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C					

MC7912AC ELECTRICAL CHARACTERISTICS (V_I = -19 V, I_O = 500 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-11.75	-12	-12.25	Vdc
Line Regulation (Note 1)	Reg_{line}				mV
-16 Vdc ≥ V_I ≥ -22 Vdc; I_O = 1.0 A, T_J = 25°C		—	6.0	60	
-16 Vdc ≥ V_I ≥ -22 Vdc; I_O = 1.0 A,		—	24	120	
-14.8 Vdc ≥ V_I ≥ -30 Vdc; I_O = 500 mA		—	24	120	
-14.5 Vdc ≥ V_I ≥ -27 Vdc; I_O = 1.0 A, T_J = 25°C		—	13	120	
Load Regulation (Note 1)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.5 A, T_J = 25°C		—	46	150	
250 mA ≤ I_O ≤ 750 mA		—	17	75	
5.0 mA ≤ I_O ≤ 1.0 A		—	35	150	
Output Voltage	V_O	-11.5	—	-12.5	Vdc
-14.8 Vdc ≥ V_I ≥ -27 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W					
Input Bias Current	I_{IB}	—	4.4	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
-15 Vdc ≥ V_I ≥ -30 Vdc		—	—	0.8	
5.0 mA ≤ I_O ≤ 1.0 A		—	—	0.5	
5.0 mA ≤ I_O ≤ 1.5 A, T_J = 25°C		—	—	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	—	75	—	μV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	—	61	—	dB
Dropout Voltage	V_I-V_O	—	2.0	—	Vdc
I_O = 1.0 A, T_J = +25°C					
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$	—	-1.0	—	mV/°C
I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C					

Note:
1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7915C ELECTRICAL CHARACTERISTICS (V_I = -23 V, I_O = 500 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-14.4	-15	-15.6	Vdc
Line Regulation (Note 1)	Reg_{line}				mV
(T_J = +25°C, I_O = 100 mA)					
-17.5 Vdc ≥ V_I ≥ -30 Vdc		—	14	150	
-20 Vdc ≥ V_I ≥ -26 Vdc		—	6.0	75	
(T_J = +25°C, I_O = 500 mA)					
-17.5 Vdc ≥ V_I ≥ -30 Vdc		—	57	300	
-20 Vdc ≥ V_I ≥ -26 Vdc		—	27	150	
Load Regulation (T_J = +25°C) (Note 1)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.5 A		—	68	300	
250 mA ≤ I_O ≤ 750 mA		—	25	150	
Output Voltage	V_O	-14.25	—	-15.75	Vdc
-17.5 Vdc ≥ V_I ≥ -30 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W					
Input Bias Current (T_J = +25°C)	I_{IB}	—	4.4	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
-17.5 Vdc ≥ V_I ≥ -30 Vdc		—	—	1.0	
5.0 mA ≤ I_O ≤ 1.5 A		—	—	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	—	90	—	μV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	—	60	—	dB
Dropout Voltage	V_I-V_O	—	2.0	—	Vdc
I_O = 1.0 A, T_J = +25°C					
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$	—	-1.0	—	mV/°C
I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C					

MC7915AC ELECTRICAL CHARACTERISTICS (V_I = -23 V, I_O = 500 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-14.7	-15	-15.3	Vdc
Line Regulation (Note 1)	Reg_{line}				mV
-20 Vdc ≥ V_I ≥ -26 Vdc; I_O = 1.0 A, T_J = 25°C		—	27	75	
-20 Vdc ≥ V_I ≥ -26 Vdc; I_O = 1.0 A,		—	57	150	
-17.9 Vdc ≥ V_I ≥ -30 Vdc; I_O = 500 mA		—	57	150	
-17.5 Vdc ≥ V_I ≥ -30 Vdc; I_O = 1.0 A, T_J = 25°C		—	57	150	
Load Regulation (Note 1)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.5 A, T_J = 25°C		—	68	150	
250 mA ≤ I_O ≤ 750 mA		—	25	75	
5.0 mA ≤ I_O ≤ 1.0 A		—	40	150	
Output Voltage	V_O	-14.4	—	-15.6	Vdc
-17.9 Vdc ≥ V_I ≥ -30 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W					
Input Bias Current	I_{IB}	—	4.4	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
-17.5 Vdc ≥ V_I ≥ -30 Vdc		—	—	0.8	
5.0 mA ≤ I_O ≤ 1.0 A		—	—	0.5	
5.0 mA ≤ I_O ≤ 1.5 A, T_J = 25°C		—	—	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	—	90	—	μV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	—	60	—	dB
Dropout Voltage	V_I-V_O	—	2.0	—	Vdc
I_O = 1.0 A, T_J = +25°C					
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$	—	-1.0	—	mV/°C
I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C					

Note:
1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7918C ELECTRICAL CHARACTERISTICS (V_I = -27 V, I_O = 500 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-17.3	-18	-18.7	Vdc
Line Regulation (Note 1)	Reg_{line}				mV
(T_J = +25°C, I_O = 100 mA)					
-21 Vdc ≥ V_I ≥ -33 Vdc		—	25	180	
-24 Vdc ≥ V_I ≥ -30 Vdc		—	10	90	
(T_J = +25°C, I_O = 500 mA)					
-21 Vdc ≥ V_I ≥ -33 Vdc		—	90	360	
-24 Vdc ≥ V_I ≥ -30 Vdc		—	50	180	
Load Regulation (T_J = +25°C) (Note 1)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.5 A		—	110	360	
250 mA ≤ I_O ≤ 750 mA		—	55	180	
Output Voltage	V_O	-17.1	—	-18.9	Vdc
-21 Vdc ≥ V_I ≥ -33 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W					
Input Bias Current (T_J = +25°C)	I_{IB}	—	4.5	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
-21 Vdc ≥ V_I ≥ -33 Vdc		—	—	1.0	
5.0 mA ≤ I_O ≤ 1.5 A		—	—	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	—	110	—	μV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	—	59	—	dB
Dropout Voltage	V_I-V_O	—	2.0	—	Vdc
I_O = 1.0 A, T_J = +25°C					
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$	—	-1.0	—	mV/°C
I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C					

MC7924C ELECTRICAL CHARACTERISTICS (V_I = -33 V, I_O = 500 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-23	-24	-25	Vdc
Line Regulation (Note 1)	Reg_{line}				mV
(T_J = +25°C, I_O = 100 mA)					
-27 Vdc ≥ V_I ≥ -38 Vdc		—	31	240	
-30 Vdc ≥ V_I ≥ -36 Vdc		—	14	120	
(T_J = +25°C, I_O = 500 mA)					
-27 Vdc ≥ V_I ≥ -38 Vdc		—	118	480	
-30 Vdc ≥ V_I ≥ -36 Vdc		—	70	240	
Load Regulation (T_J = +25°C) (Note 1)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.5 A		—	150	480	
250 mA ≤ I_O ≤ 750 mA		—	85	240	
Output Voltage	V_O	-22.8	—	-25.2	Vdc
-27 Vdc ≥ V_I ≥ -38 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W					
Input Bias Current (T_J = +25°C)	I_{IB}	—	4.6	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
-27 Vdc ≥ V_I ≥ -38 Vdc		—	—	1.0	
5.0 mA ≤ I_O ≤ 1.5 A		—	—	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	—	170	—	μV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	—	56	—	dB
Dropout Voltage	V_I-V_O	—	2.0	—	Vdc
I_O = 1.0 A, T_J = +25°C					
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$	—	-1.0	—	mV/°C
I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C					

Note:
1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

TYPICAL CHARACTERISTICS
(T_A = +25°C unless otherwise noted.)

FIGURE 1 – WORST CASE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE

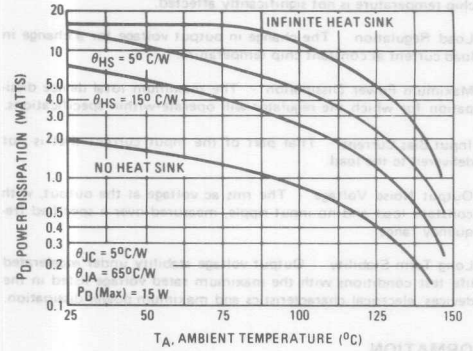


FIGURE 2 – WORST CASE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE

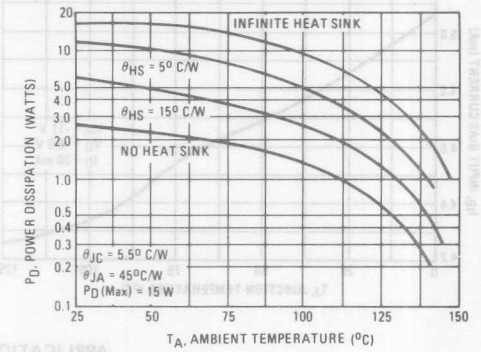


FIGURE 3 – PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE

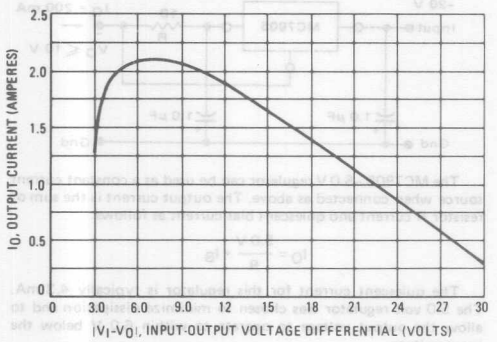


FIGURE 4 – RIPPLE REJECTION AS A FUNCTION OF FREQUENCY

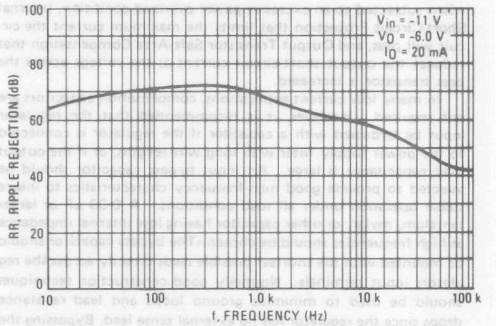


FIGURE 5 – RIPPLE REJECTION AS A FUNCTION OF OUTPUT VOLTAGES

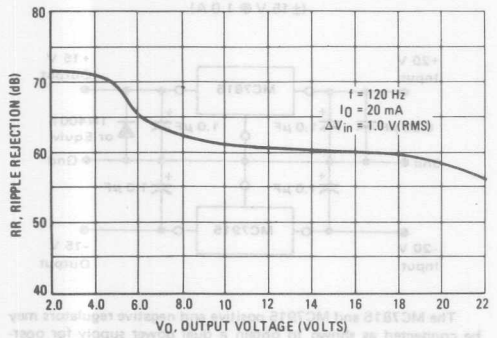


FIGURE 6 – OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE

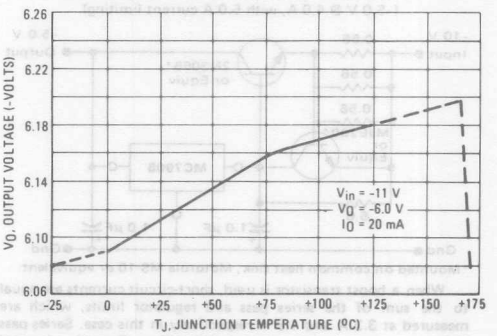
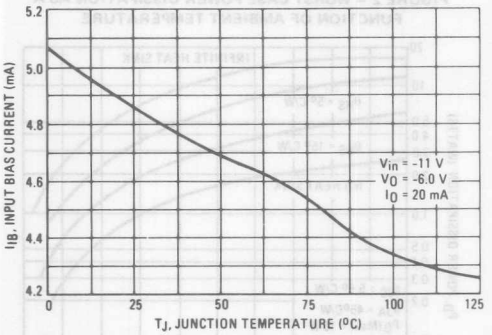


FIGURE 7 – QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE



DEFINITIONS

Line Regulation – The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation – The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation – The maximum total device dissipation for which the regulator will operate within specifications.

Input Bias Current – That part of the input current that is not delivered to the load.

Output Noise Voltage – The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long Term Stability – Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices' electrical characteristics and maximum power dissipation.

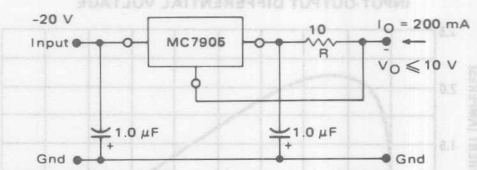
APPLICATIONS INFORMATION

Design Considerations

The MC7900 Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.

FIGURE 8 – CURRENT REGULATOR

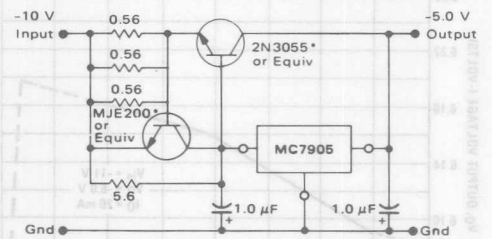


The MC7905,-5.0 V regulator can be used as a constant current source when connected as above. The output current is the sum of resistor R current and quiescent bias current as follows:

$$I_O = \frac{5.0\ V}{R} + I_B$$

The quiescent current for this regulator is typically 4.3 mA. The 5.0 volt regulator was chosen to minimize dissipation and to allow the output voltage to operate to within 6.0 V below the input voltage.

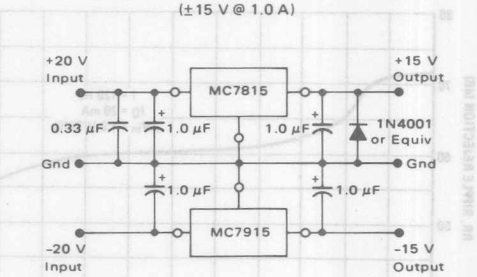
FIGURE 9 – CURRENT BOOST REGULATOR
(-5.0 V @ 4.0 A, with 5.0 A current limiting)



*Mounted on common heat sink, Motorola MS-10 or equivalent.

When a boost transistor is used, short-circuit currents are equal to the sum of the series pass and regulator limits, which are measured at 3.2 A and 1.8 A respectively in this case. Series pass limiting is approximately equal to 0.6 V/R_{SC}. Operation beyond this point to the peak current capability of the MC7905C is possible if the regulator is mounted on a heat sink; otherwise thermal shutdown will occur when the additional load current is picked up by the regulator.

FIGURE 10 – OPERATIONAL AMPLIFIER SUPPLY
(±15 V @ 1.0 A)



The MC7815 and MC7915 positive and negative regulators may be connected as shown to obtain a dual power supply for operational amplifiers. A clamp diode should be used at the output of the MC7815 to prevent potential latch-up problems whenever the output of the positive regulator (MC7815) is drawn below ground with an output current greater than 200 mA.

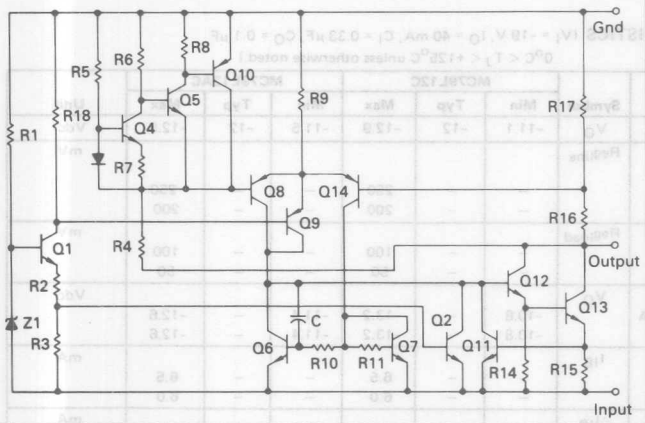
THREE-TERMINAL LOW CURRENT NEGATIVE VOLTAGE REGULATORS

The MC79L00 Series negative voltage regulators are inexpensive, easy-to-use devices suitable for numerous applications requiring up to 100 mA. Like the higher powered MC7900 Series negative regulators, this series features thermal shutdown and current limiting, making them remarkably rugged. In most applications, no external components are required for operation.

The MC79L00 devices are useful for on-card regulation or any other application where a regulated negative voltage at a modest current level is needed. These regulators offer substantial advantage over the common resistor/zener diode approach.

- No External Components Required
- Internal Short-Circuit Current Limiting
- Internal Thermal Overload Protection
- Low Cost
- Complementary Positive Regulators Offered (MC78L00 Series)
- Available in Either ±5% (AC) or ±10% (C) Selections

REPRESENTATIVE CIRCUIT SCHEMATIC



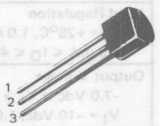
Device No. ±10%	Device No. ±5%	Nominal Voltage
MC79L05C	MC79L05AC	−5.0
MC79L12C	MC79L12AC	−12
MC79L15C	MC79L15AC	−15
MC79L18C	MC79L18AC	−18
MC79L24C	MC79L24AC	−24

#Automotive temperature range selections are available with special test conditions and additional tests in 5, 12 and 15 volt devices. Contact your local Motorola sales office for information.

THREE-TERMINAL LOW CURRENT NEGATIVE FIXED VOLTAGE REGULATORS

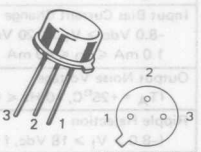
P SUFFIX
PLASTIC PACKAGE
CASE 29-04

PIN 1. GROUND
2. INPUT
3. OUTPUT



G SUFFIX
METAL PACKAGE
CASE 79-05

PIN 1. GROUND
2. OUTPUT
3. INPUT



(Bottom View)
(Case Connected To Pin 3)

D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SOP-8



PIN 1. V_{OUT}	5. GND
2. V_{IN}	6. V_{IN}
3. V_{IN}	7. V_{IN}
4. NC	8. NC

SOP-8 is an internally modified SO-8 Package. Pins 2, 3, 6 and 7 are electrically common to the die attach flag. This internal lead frame modification decreases package thermal resistance and increases power dissipation capability when appropriately mounted on a printed circuit board. SOP-8 conforms to all external dimensions of the standard SO-8 Package.

ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
MC79LXXACD*	T_J = 0°C to +125°C	SOP-8
MC79LXXACG*		Metal Can
MC79LXXACP		Plastic Power
MC79LXXCG*		Metal Can
MC79LXXCP		Plastic Power
MC79LXXABP#	T_J = −40°C to +125°C	

XX indicates nominal voltage
*Available in 5, 12 and 15 volt devices

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (−5 V) (−12, −15, −18 V) (−24 V)	V_I	−30 −35 −40	Vdc
Storage Temperature Range	T_{stg}	−65 to +150	°C
Junction Temperature Range	T_J	0 to +150	°C

3

MC79L05C, AC Series ELECTRICAL CHARACTERISTICS (V_I = −10 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	MC79L05C Min	MC79L05C Typ	MC79L05C Max	MC79L05AC Min	MC79L05AC Typ	MC79L05AC Max	Unit
Output Voltage (T_J = +25°C)	V_O	-4.6	-5.0	-5.4	-4.8	-5.0	-5.2	Vdc
Input Regulation (T_J = +25°C) -7.0 Vdc ≥ V_I ≥ -20 Vdc -8.0 Vdc ≥ V_I ≥ -20 Vdc	Reg_{line}	– –	– –	200 150	– –	– –	150 100	mV
Load Regulation T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA 1.0 mA ≤ I_O ≤ 40 mA	Reg_{load}	– –	– –	60 30	– –	– –	60 30	mV
Output Voltage -7.0 Vdc ≥ V_I ≥ -20 Vdc, 1.0 mA ≤ I_O ≤ 40 mA V_I = -10 Vdc, 1.0 mA ≤ I_O ≤ 70 mA	V_O	-4.5 -4.5	– –	-5.5 -5.5	-4.75 -4.75	– –	-5.25 -5.25	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	– –	– –	6.0 5.5	– –	– –	6.0 5.5	mA
Input Bias Current Change -8.0 Vdc ≥ V_I ≥ -20 Vdc 1.0 mA ≤ I_O ≤ 40 mA	ΔI_{IB}	– –	– –	1.5 0.2	– –	– –	1.5 0.1	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	40	–	–	40	–	μV
Ripple Rejection (-8.0 ≥ V_I ≥ 18 Vdc, f = 120 Hz, T_J = 25°C)	RR	40	49	–	41	49	–	dB
Dropout Voltage I_O = 40 mA, T_J = +25°C	$\lvert V_I - V_O \rvert$	–	1.7	–	–	1.7	–	Vdc

MC79L12C, AC ELECTRICAL CHARACTERISTICS (V_I = −19 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	MC79L12C Min	MC79L12C Typ	MC79L12C Max	MC79L12AC Min	MC79L12AC Typ	MC79L12AC Max	Unit
Output Voltage (T_J = +25°C)	V_O	-11.1	-12	-12.9	-11.5	-12	-12.5	Vdc
Input Regulation (T_J = +25°C) -14.5 Vdc ≥ V_I ≥ -27 Vdc -16 Vdc ≥ V_I ≥ -27 Vdc	Reg_{line}	– –	– –	250 200	– –	– –	250 200	mV
Load Regulation T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA 1.0 mA ≤ I_O ≤ 40 mA	Reg_{load}	– –	– –	100 50	– –	– –	100 50	mV
Output Voltage -14.5 Vdc ≥ V_I ≥ -27 Vdc, 1.0 mA ≤ I_O ≤ 40 mA V_I = -19 Vdc, 1.0 mA ≤ I_O ≤ 70 mA	V_O	-10.8 -10.8	– –	-13.2 -13.2	-11.4 -11.4	– –	-12.6 -12.6	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	– –	– –	6.5 6.0	– –	– –	6.5 6.0	mA
Input Bias Current Change -16 Vdc ≥ V_I ≥ -27 Vdc 1.0 mA ≤ I_O ≤ 40 mA	ΔI_{IB}	– –	– –	1.5 0.2	– –	– –	1.5 0.1	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	80	–	–	80	–	μV
Ripple Rejection (-15 ≤ V_I ≤ -25 Vdc, f = 120 Hz, T_J = +25°C)	RR	36	42	–	37	42	–	dB
Dropout Voltage I_O = 40 mA, T_J = +25°C	$\lvert V_I - V_O \rvert$	–	1.7	–	–	1.7	–	Vdc

MC79L15C, AC ELECTRICAL CHARACTERISTICS (V_I = -23 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, $0^oC < T_J < +125^oC$ unless otherwise noted.)

Characteristic	Symbol	MC79L15C			MC79L15AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	-13.8	-15	-16.2	-14.4	-15	-15.6	Vdc
Input Regulation (T_J = +25°C) -17.5 Vdc ≥ V_I ≥ -30 Vdc -20 Vdc ≥ V_I ≥ -30 Vdc	Reg_{line}	 – –	 – –	 300 250	 – –	 – –	 300 250	mV
Load Regulation T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA 1.0 mA ≤ I_O ≤ 40 mA	Reg_{load}	 – –	 – –	 150 75	 – –	 – –	 150 75	mV
Output Voltage -17.5 Vdc ≥ V_I ≥ -30 Vdc, 1.0 mA ≤ I_O ≤ 40 mA V_I = -23 Vdc, 1.0 mA ≤ I_O ≤ 70 mA	V_O	 -13.5 -13.5	 – –	 -16.5 -16.5	 -14.25 -14.25	 – –	 -15.75 -15.75	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 – –	 – –	 6.5 6.0	 – –	 – –	 6.5 6.0	mA
Input Bias Current Change -20 Vdc ≥ V_I ≥ -30 Vdc 1.0 mA ≤ I_O ≤ 40 mA	ΔI_{IB}	 – –	 – –	 1.5 0.2	 – –	 – –	 1.5 0.1	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	90	–	–	90	–	μV
Ripple Rejection (-18.5 ≤ V_I ≤ -28.5 Vdc, f = 120 Hz)	RR	33	39	–	34	39	–	dB
Dropout Voltage I_O = 40 mA, T_J = +25°C	$\lvert V_I - V_O \rvert$	–	1.7	–	–	1.7	–	Vdc

MC79L18C, AC ELECTRICAL CHARACTERISTICS (V_I = -27 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, $0^oC < T_J < +125^oC$ unless otherwise noted.)

Characteristic	Symbol	MC79L18C			MC79L18AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	-16.6	-18	-19.4	-17.3	-18	-18.7	Vdc
Input Regulation (T_J = +25°C) -20.7 Vdc ≥ V_I ≥ -33 Vdc -21.4 Vdc ≥ V_I ≥ -33 Vdc -22 Vdc ≥ V_I ≥ -33 Vdc -21 Vdc ≥ V_I ≥ -33 Vdc	Reg_{line}	 – – – –	 – – – –	 – 325 275 –	 – – – –	 – – – –	 325 – – 275	mV
Load Regulation T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA 1.0 mA ≤ I_O ≤ 40 mA	Reg_{load}	 – –	 – –	 170 85	 – –	 – –	 170 85	mV
Output Voltage -20.7 Vdc ≥ V_I ≥ -33 Vdc, 1.0 mA ≤ I_O ≤ 40 mA -21.4 Vdc ≥ V_I ≥ -33 Vdc, 1.0 mA ≤ I_O ≤ 40 mA V_I = -27 Vdc, 1.0 mA ≤ I_O ≤ 70 mA	V_O	 – -16.2 -16.2	 – – –	 – -19.8 -19.8	 -17.1 – -17.1	 – – –	 -18.9 – -18.9	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 – –	 – –	 6.5 6.0	 – –	 – –	 6.5 6.0	mA
Input Bias Current Change -21 Vdc ≥ V_I ≥ -33 Vdc -27 Vdc ≥ V_I ≥ -33 Vdc 1.0 mA ≤ I_O ≤ 40 mA	ΔI_{IB}	 – – –	 – – –	 – 1.5 0.2	 – – –	 – – –	 1.5 – 0.1	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	150	–	–	150	–	μV
Ripple Rejection (-23 ≤ V_I ≤ -33 Vdc, f = 120 Hz, T_J = +25°C)	RR	32	46	–	33	48	–	dB
Dropout Voltage I_O = 40 mA, T_J = +25°C	$\lvert V_I - V_O \rvert$	–	1.7	–	–	1.7	–	Vdc

Characteristic	Symbol	MC79L24C Min	MC79L24C Typ	MC79L24C Max	MC79L24AC Min	MC79L24AC Typ	MC79L24AC Max	Unit
Output Voltage (T_J = +25°C)	V_O	-22.1	-24	-25.9	-23	-24	-25	Vdc
Input Regulation (T_J = +25°C)	Reg_{line}							mV
-27 Vdc ≥ V_I ≥ -38 V		–	–	–	–	–	350	
-27.5 Vdc ≥ V_I ≥ -38 Vdc		–	–	350	–	–	–	
-28 Vdc ≥ V_I ≥ -38 Vdc		–	–	300	–	–	300	
Load Regulation	Reg_{load}							mV
T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA		–	–	200	–	–	200	
1.0 mA ≤ I_O ≤ 40 mA		–	–	100	–	–	100	
Output Voltage	V_O							Vdc
-27 Vdc ≥ V_I ≥ -38 V, 1.0 mA ≤ I_O ≤ 40 mA		–	–	–	-22.8	–	-25.2	
-28 Vdc ≥ V_I ≥ -38 Vdc, 1.0 mA ≤ I_O ≤ 40 mA		-21.4	–	-26.4	–	–	–	
V_I = -33 Vdc, 1.0 mA ≤ I_O ≤ 70 mA		-21.4	–	-26.4	-22.8	–	-25.2	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	–	6.5	–	–	6.5	
(T_J = +125°C)		–	–	6.0	–	–	6.0	
Input Bias Current Change	ΔI_{IB}							mA
-28 Vdc ≥ V_I ≥ -38 Vdc		–	–	1.5	–	–	1.5	
1.0 mA ≤ I_O ≤ 40 mA		–	–	0.2	–	–	0.1	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	200	–	–	200	–	μV
Ripple Rejection (-29 ≤ V_I ≤ -35 Vdc, f = 120 Hz, T_J = 25°C)	RR	30	43	–	31	47	–	dB
Dropout Voltage I_O = 40 mA, T_J = +25°C	$\lvert V_I - V_O \rvert$	–	1.7	–	–	1.7	–	Vdc

APPLICATIONS INFORMATION

Design Considerations

The MC79L00 Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulator's input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.

FIGURE 1 — POSITIVE AND NEGATIVE REGULATOR

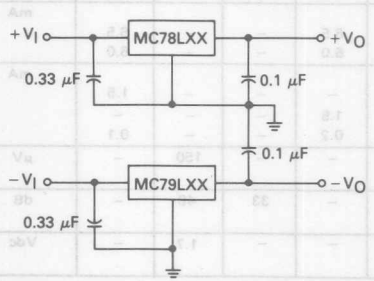
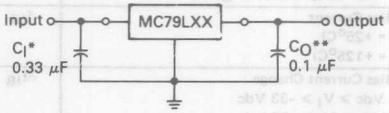


FIGURE 2 — STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

* = C_I is required if regulator is located an appreciable distance from power supply filter.

** = C_O improves stability and transient response.

TYPICAL CHARACTERISTICS
(T_A = +25°C unless otherwise noted.)

FIGURE 3 — DROPOUT CHARACTERISTICS

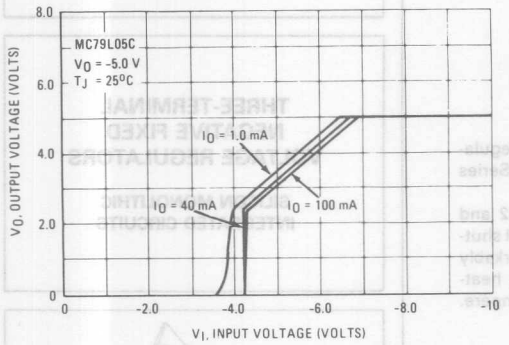


FIGURE 4 — DROPOUT VOLTAGE versus JUNCTION TEMPERATURE

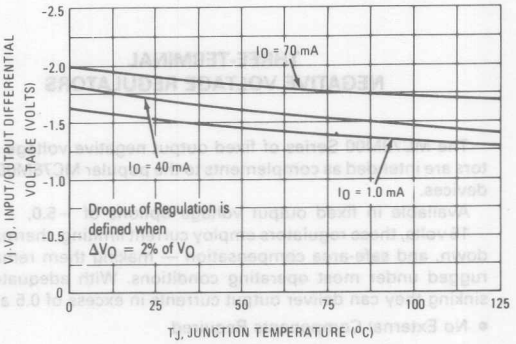


FIGURE 5 — INPUT BIAS CURRENT versus AMBIENT TEMPERATURE

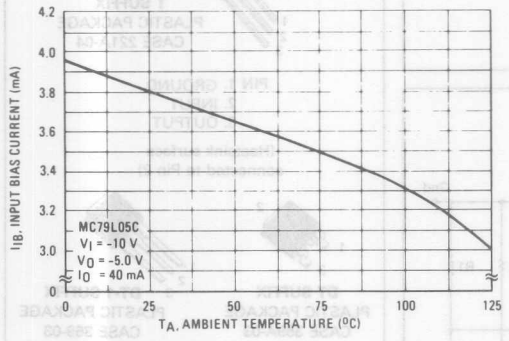


FIGURE 6 — INPUT BIAS CURRENT versus INPUT VOLTAGE

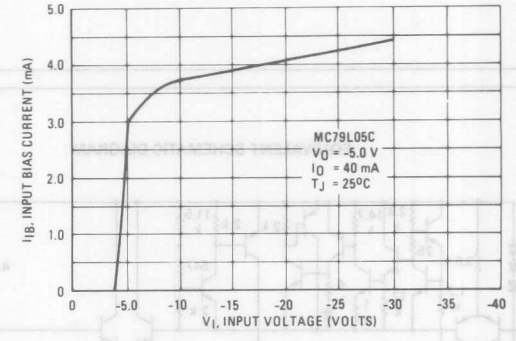


FIGURE 7 — MAXIMUM AVERAGE POWER DISSIPATION versus AMBIENT TEMPERATURE — TO-92 Type Package

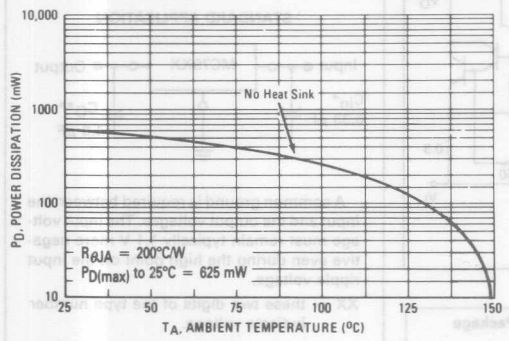
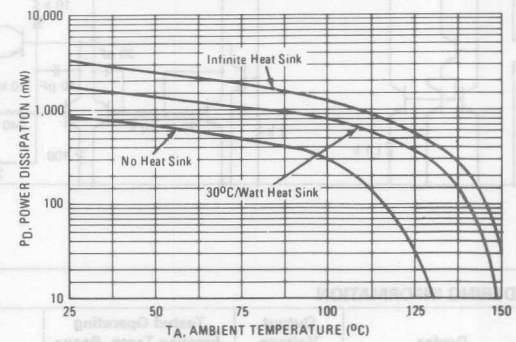


FIGURE 8 — MAXIMUM AVERAGE POWER DISSIPATION versus AMBIENT TEMPERATURE — TO-39 Type Package



MOTOROLA

MC79M00 Series

THREE-TERMINAL NEGATIVE VOLTAGE REGULATORS

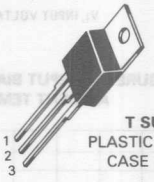
The MC79M00 Series of fixed output negative voltage regulators are intended as complements to the popular MC78M00 Series devices.

Available in fixed output voltage options of −5.0, −12 and −15 volts, these regulators employ current limiting, thermal shutdown, and safe-area compensation — making them remarkably rugged under most operating conditions. With adequate heatsinking they can deliver output currents in excess of 0.5 ampere.

- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation

THREE-TERMINAL NEGATIVE FIXED VOLTAGE REGULATORS

SILICON MONOLITHIC INTEGRATED CIRCUITS



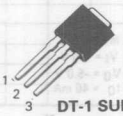
T SUFFIX
PLASTIC PACKAGE
CASE 221A-04

PIN 1. GROUND
2. INPUT
3. OUTPUT

(Heatsink surface connected to Pin 2)

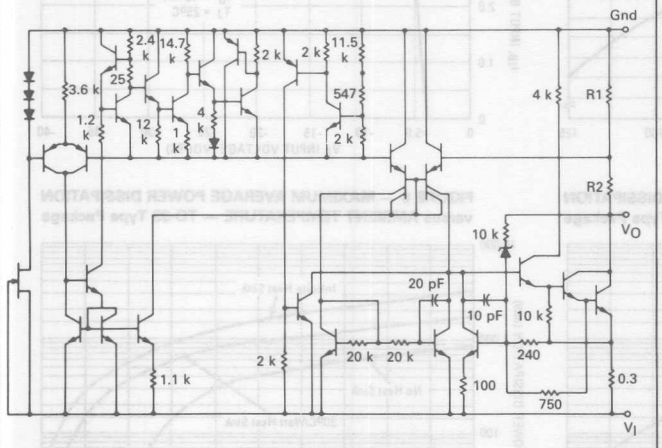


DT SUFFIX
PLASTIC PACKAGE
CASE 369A-03
DPAK

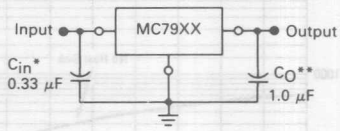


DT-1 SUFFIX
PLASTIC PACKAGE
CASE 369-03
DPAK

EQUIVALENT SCHEMATIC DIAGRAM



STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 1.1 V more negative even during the high point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O improves stability and transient response.

ORDERING INFORMATION

Device	Output Voltage	Tested Operating Junction Temp. Range	Package
MC79M05CDT, CDT-1	−5.0 Volts	0°C to +125°C	DPAK
MC79M05CT			PLASTIC POWER
MC79M12CDT, CDT-1	−12 Volts		DPAK
MC79M12CT			PLASTIC POWER
MC79M15CDT, CDT-1	−15 Volts		DPAK
MC79M15CT			PLASTIC POWER

MC79MXX Series MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage	V_I	−35	Vdc
Power Dissipation Plastic Package T_A = +25°C Derate above T_A = +25°C T_C = +25°C Derate above T_C = +95°C	 P_D $1/R\theta_{JA}$ P_D $1/R\theta_{JC}$	 Internally Limited 14.2 Internally Limited 200	 Watts mW/°C Watts mW/°C
Storage Junction Temperature Range	T_{stg}	−65 to +150	°C
Junction Temperature Range	T_J	0 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R\theta_{JA}$	65	°C/W
Thermal Resistance, Junction to Case	$R\theta_{JC}$	5.0	°C/W

MC79MO5C ELECTRICAL CHARACTERISTICS (V_I = −10 V, I_O = 350 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	−4.8	−5.0	−5.2	Vdc
Line Regulation (T_J = +25°C) (Note 1) −7.0 Vdc ≥ V_I ≥ −25 Vdc −8.0 Vdc ≥ V_I ≥ −18 Vdc	Reg_{line}	 — —	 7.0 2.0	 50 30	mV
Load Regulation (T_J = +25°C) (Note 1) 5.0 mA ≤ I_O ≤ 500 mA	Reg_{load}	—	30	100	mV
Output Voltage −7.0 Vdc ≥ V_I ≥ −25 Vdc, 5.0 mA ≤ I_O ≤ 350 mA	V_O	−4.75	—	−5.25	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	4.3	8.0	mA
Input Bias Current Change −8.0 Vdc ≥ V_I ≥ −25 Vdc, I_O = 350 mA 5.0 mA ≤ I_O ≤ 350 mA, V_I = −10 V	ΔI_{IB}	 — —	 — —	 0.4 0.4	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	40	—	μV
Ripple Rejection (f = 120 Hz)	RR	54	66	—	dB
Dropout Voltage I_O = 500 mA, T_J = +25°C	V_I-V_O	—	1.1	—	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	—	0.2	—	mV/°C

Note:
1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC79M12C ELECTRICAL CHARACTERISTICS (V_I = −19 V, I_O = 350 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	−11.5	−12	−12.5	Vdc
Line Regulation (T_J = +25°C) (Note 1) −14.5 Vdc ≥ V_I ≥ −30 Vdc −15 Vdc ≥ V_I ≥ −25 Vdc	Reg_{line}	 — —	 5.0 3.0	 80 50	mV mV mV
Load Regulation (T_J = +25°C) (Note 1) 5.0 mA ≤ I_O ≤ 500 mA	Reg_{load}	—	30	240	mV
Output Voltage −14.5 Vdc ≥ V_I ≥ −30 Vdc, 5.0 mA ≤ I_O ≤ 350 mA	V_O	−11.4	—	−12.6	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	4.4	8.0	mA
Input Bias Current Change −14.5 Vdc ≥ V_I ≥ −30 Vdc, I_O = 350 mA 5.0 mA ≤ I_O ≤ 350 mA, V_I = −19 V	ΔI_{IB}	 — —	 — —	 0.4 0.4	mA mA mA
Output Noise Voltage (T_A = +25°C, 10Hz ≤ f ≤ 100 kHz)	V_n	—	75	—	μV
Ripple Rejection (f = 120 Hz)	RR	54	60	—	dB
Dropout Voltage I_O = 500 mA, T_J = +25°C	V_I-V_O	—	1.1	—	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	—	−0.8	—	mV/°C

MC79M15C ELECTRICAL CHARACTERISTICS (V_I = −23 V, I_O = 350 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	−14.4	−15	−15.6	Vdc
Line Regulation (T_J = +25°) (Note 1) −17.5 Vdc ≥ V_I ≥ −30 Vdc −18 Vdc ≥ V_I ≥ −28 Vdc	Reg_{line}	 — —	 5.0 3.0	 80 50	mV mV mV
Load Regulation (T_J = +25°C) (Note 1) 5.0 mA ≤ I_O ≤ 500 mA	Reg_{load}	—	30	240	mV
Output Voltage −17.5 Vdc ≥ V_I ≥ −30 Vdc, 5.0 mA ≤ I_O ≤ 350 mA	V_O	−14.25	—	−15.75	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	4.4	8.0	mA
Input Bias Current Change −17.5 Vdc ≥ V_I ≥ −30 Vdc, I_O = 350 mA 5.0 mA ≤ I_O ≤ 350 mA, V_I = −23 V	ΔI_{IB}	 — —	 — —	 0.4 0.4	mA mA mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	90	—	μV
Ripple Rejection (f = 120 Hz)	RR	54	60	—	dB
Dropout Voltage I_O = 500 mA, T_J = +25°C	V_I-V_O	—	1.1	—	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	—	−1.0	—	mV/°C

Note:
1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MOTOROLA

MC34060
MC35060

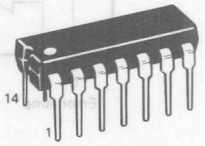
SWITCHMODE PULSE WIDTH MODULATION CONTROL CIRCUITS

The MC35060 and MC34060 are low cost fixed frequency, pulse width modulation control circuits designed primarily for single ended SWITCHMODE power supply control. These devices feature:

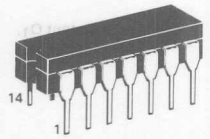
- Complete Pulse Width Modulation Control Circuitry
- On-Chip Oscillator With Master or Slave Operation
- On-Chip Error Amplifiers
- On-Chip 5.0 Volt Reference
- Adjustable Dead Time Control
- Uncommitted Output Transistor for 200 mA Source or Sink

SWITCHMODE PULSE WIDTH MODULATION CONTROL CIRCUITS

SILICON MONOLITHIC INTEGRATED CIRCUITS

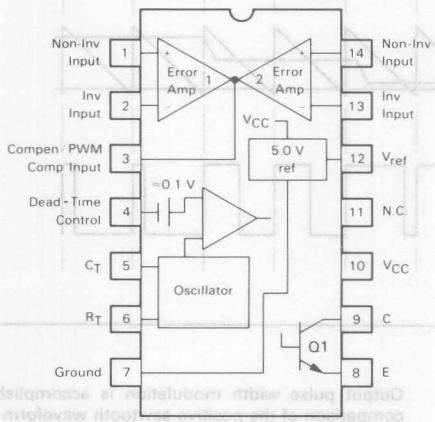


P SUFFIX
PLASTIC PACKAGE
CASE 646-06



L SUFFIX
CERAMIC PACKAGE
CASE 632-08

PIN CONNECTIONS



(Top View)

The MC34060 is specified over the commercial operating range of 0°C to +70°C. The MC35060 is specified over the full military range of -55 to +125°C.

ORDERING INFORMATION

Device	Temperature Range	Package
MC35060L	-55 to +125°C	Ceramic DIP
MC34060P	0 to +70°C	Plastic DIP
MC34060L	0 to +70°C	Ceramic DIP

3

FIGURE 1 — BLOCK DIAGRAM

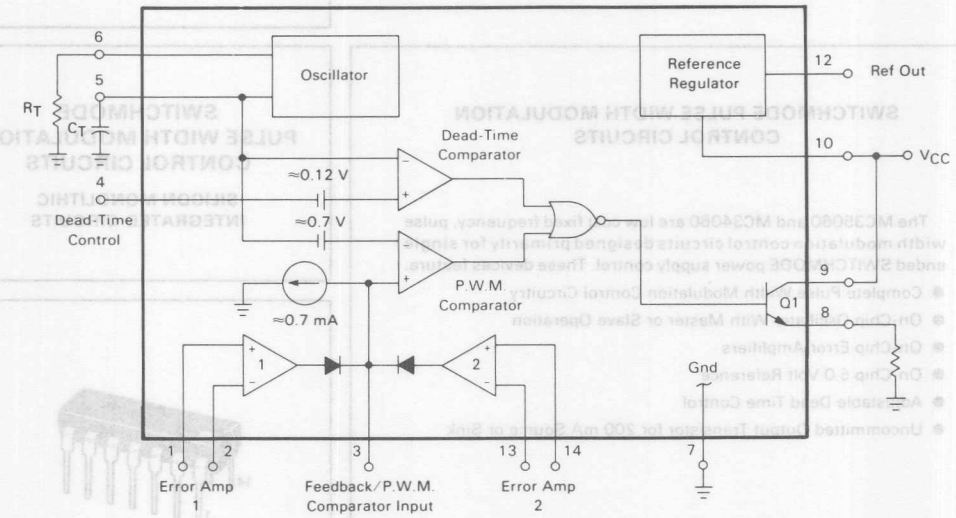
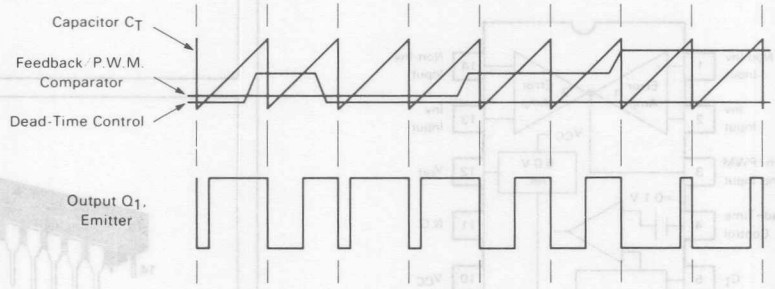


FIGURE 2 — TIMING DIAGRAM



Description

The MC35060/34060 is a fixed-frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply. (See Figure 1.) An internal-linear sawtooth oscillator is frequency-programmable by two external components, R_T and C_T. The approximate oscillator frequency is determined by:

$$f_{osc} \cong \frac{1.1}{R_T \bullet C_T}$$

For more information refer to Figure 3.

Output pulse width modulation is accomplished by comparison of the positive sawtooth waveform across capacitor C_T to either of two control signals. The output is enabled only during that portion of time when the sawtooth voltage is greater than the control signals. Therefore, an increase in control-signal amplitude causes a corresponding linear decrease of output pulse width. (Refer to the timing diagram shown in Figure 2.)

The control signals are external inputs that can be fed into the dead-time control, the error amplifier inputs, or the feed-back input. The dead-time control comparator has an effective 120 mV input offset which limits the minimum output dead time to approximately the first 4% of the sawtooth-cycle time. This would result in a maximum duty cycle of 96%. Additional dead time may be imposed on the output by setting the dead time-control input to a fixed voltage, ranging between 0 to 3.3 V.

The pulse width modulator comparator provides a means for the error amplifiers to adjust the output pulse width from the maximum percent on-time, established by the dead time control input, down to zero, as the voltage at the feedback pin varies from 0.5 to 3.5 V. Both error amplifiers have a common-mode input range from −0.3 V to (V_{CC} − 2 V), and may be used to sense power supply output voltage and current. The error-amplifier outputs are active high and are ORed together at the non-inverting input of the pulse-width modulator comparator. With this configuration, the amplifier that demands minimum output on time, dominates control of the loop.

The MC35060/34060 has an internal 5.0 V reference capable of sourcing up to 10 mA of load currents for external bias circuits. The reference has an internal accuracy of ±5% with a typical thermal drift of less than 50 mV over an operating temperature range of 0 to +70°C.

MAXIMUM RATINGS (Full operating ambient temperature range applies unless otherwise noted)

Rating	Symbol	MC35060	MC34060	Unit
Power Supply Voltage	V_{CC}	42	42	V
Collector Output Voltage	V_C	42	42	V
Collector Output Current	I_C	250	250	mA
Amplifier Input Voltage	V_{in}	V_{CC} + 0.3	V_{CC} + 0.3	V
Power Dissipation @ $T_A \leq 45°C$	P_D	1000	1000	mW
Operating Junction Temperature Plastic Package Ceramic Package	T_J	 — 150	 125 150	°C
Operating Ambient Temperature Range	T_A	-55 to 125	0 to 70	°C
Storage Temperature Range Plastic Package Ceramic Package	T_{stg}	 — -65 to 150	 -55 to 125 -65 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	L Suffix Ceramic Package	P Suffix Plastic Package	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	100	80	°C/W
Power Derating Factor	$1/R_{\theta JA}$	10	12.5	mW/°C
Derating Ambient Temperature	T_A	50	45	°C

RECOMMENDED OPERATING CONDITIONS

Condition/Value	Symbol	MC35060/MC34060			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	7.0	15	40	V
Collector Output Voltage	V_C	—	30	40	V
Collector Output Current	I_C	—	—	200	mA
Amplifier Input Voltage	V_{in}	-0.3	—	V_{CC} - 2	V
Current Into Feedback Terminal	I_{fb}	—	—	0.3	mA
Reference Output Current	I_{ref}	—	—	10	mA
Timing Resistor	R_T	1.8	47	500	kΩ
Timing Capacitor	C_T	0.0047	0.001	10	μF
Oscillator Frequency	f_{osc}	1.0	25	200	kHz

ELECTRICAL CHARACTERISTICS V_{CC} = 15 V, C_T = 0.01 μF, R_T = 12 kΩ unless otherwise noted. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies unless otherwise noted.

Characteristic	Symbol	MC35060			MC34060			Unit
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION								
Reference Voltage (I_O = 1.0 mA)	V_{ref}	4.75	5.0	5.25	4.75	5.0	5.25	V
Input Regulation (V_{CC} = 7.0 V to 40 V)	Reg_{line}	—	2.0	25	—	2.0	25	mV
Output Regulation (I_O = 1.0 mA to 10 mA)	Reg_{load}	—	3.0	15	—	3.0	15	mV
Short-Circuit Output Current (V_{ref} = 0 V)	I_{SC}	15	35	75	15	35	75	mA
OUTPUT SECTION								
Collector Off-State Current (V_{CC} = 40 V, V_{CE} = 40 V)	$I_{C(off)}$	—	2.0	100	—	2.0	100	μA
Emitter Off-State Current (V_{CC} = 40 V, V_C = 40 V, V_E = 0 V)	$I_{E(off)}$	—	—	-150	—	—	-100	μA
Collector-Emitter Saturation Voltage								
Common-Emitter (V_E = 0 V, I_C = 200 mA)	$V_{sat(C)}$	—	1.1	1.5	—	1.1	1.3	V
Emitter-Follower (V_C = 15 V, I_E = -200 mA)	$V_{sat(E)}$	—	1.5	2.5	—	1.5	2.5	V
Output Voltage Rise Time (T_A = 25°C)								
Common-Emitter (See Figure 12)	t_r	—	100	200	—	100	200	ns
Emitter-Follower (See Figure 13)		—	100	200	—	100	200	ns
Output Voltage Fall Time (T_A = 25°C)								
Common-Emitter (See Figure 12)	t_f	—	25	100	—	25	100	ns
Emitter-Follower (See Figure 13)		—	40	100	—	40	100	ns

Characteristic	Symbol	MC35060/MC34060			Unit
		Min	Typ	Max	
ERROR AMPLIFIER SECTIONS					
Input Offset Voltage ($V_{O[Pin\ 3]}$ = 2.5 V)	V_{IO}	—	2.0	10	mV
Input Offset Current ($V_{C[Pin\ 3]}$ = 2.5 V)	I_{IO}	—	5.0	250	nA
Input Bias Current ($V_{O[Pin\ 3]}$ = 2.5 V)	I_{IB}	—	-0.1	-1.0	μA
Input Common-Mode Voltage Range (V_{CC} = 40 V, T_A = 25°C)	V_{ICR}	-0.3 to V_{CC} - 2.0	—	—	V
Open Loop Voltage Gain (ΔV_O = 3.0 V, V_O = 0.5 to 3.5 V, R_L = 2.0 kΩ)	A_{VOL}	70	95	—	dB

ELECTRICAL CHARACTERISTICS V_{CC} = 15 V, C_T = 0.01 μF, R_T = 12 kΩ unless otherwise noted. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies unless otherwise noted.

Characteristic	Symbol	MC35060/MC34060			Unit
		Min.	Typ.	Max.	
ERROR AMPLIFIER SECTIONS (Continued)					
Unity-Gain Crossover Frequency (V_O = 0.5, to 3.5 V, R_L = 2.0 kΩ)	f_c	—	350	—	kHz
Phase Margin at Unity-Gain (V_O = 0.5 to 3.5 V, R_L = 2.0 kΩ)	ϕ_m	—	65	—	deg.
Common-Mode Rejection Ratio (V_{CC} = 40 V)	CMRR	65	90	—	dB
Power Supply Rejection Ratio (ΔV_{CC} = 33 V, V_O = 2.5 V, R_L = 2.0 kΩ)	PSRR	—	100	—	dB
Output Sink Current ($V_{O[Pin\ 3]}$ = 0.7 V)	I_O^-	0.3	0.7	—	mA
Output Source Current ($V_{O[Pin\ 3]}$ = 3.5 V)	I_O^+	-2.0	-4.0	—	mA
PWM COMPARATOR SECTION (Test circuit Figure 11)					
Input Threshold Voltage (Zero Duty Cycle)	V_{TH}	—	3.5	4.5	V
Input Sink Current ($V_{[Pin\ 3]}$ = 0.7 V)	I_I^-	0.3	0.7	—	mA
DEAD-TIME CONTROL SECTION (Test Circuit Figure 11)					
Input Bias Current (Pin 4) (V_{in} = 0 to 5.25 V)	$I_{IB(DT)}$	—	-2.0	-10	μA
Maximum Output Duty Cycle (V_{in} = 0 V, C_T = 0.01 μF, R_T = 12 kΩ) (V_{in} = 0 V, C_T = 0.001 μF, R_T = 47 kΩ)	DC_{max}	 90 —	 96 92	 100 100	%
Input Threshold Voltage (Pin 4) (Zero Duty Cycle) (Maximum Duty Cycle)	V_{TH}	 — 0	 2.8 —	 3.3 —	V
OSCILLATOR SECTION					
Frequency (C_T = 0.001 μF, R_T = 47 kΩ)	f_{osc}	—	25	—	kHz
Standard Deviation of Frequency* (C_T = 0.001 μF, R_T = 47 kΩ)	σf_{osc}	—	3.0	—	%
Frequency Change with Voltage (V_{CC} = 7.0 V to 40 V, T_A = 25°C)	$\Delta f_{osc}(\Delta V)$	—	0.1	—	%
Frequency Change with Temperature (ΔT_A = T_{low} to T_{high}) (C_T = 0.01 μF, R_T = 12 kΩ)	$\Delta f_{osc}(\Delta T)$	 — —	 —	 12	%
TOTAL DEVICE					
Standby Supply Current (Pin 6 at V_{ref}, all other inputs and outputs open) (V_{CC} = 15 V) (V_{CC} = 40 V)	I_{CC}	 — —	 5.5 7.0	 10 15	mA
Average Supply Current ($V_{[Pin\ 4]}$ = 2.0 V, C_T = 0.001, R_T = 47 kΩ). See Figure 11.	I_S	—	7.0	—	mA

*Standard deviation is a measure of the statistical distribution about the mean as derived from the formula, $\sigma = \sqrt{\frac{\sum_{n=1}^{N} (X_n - \bar{x})^2}{N-1}}$

3

FIGURE 3 — OSCILLATOR FREQUENCY versus TIMING RESISTANCE

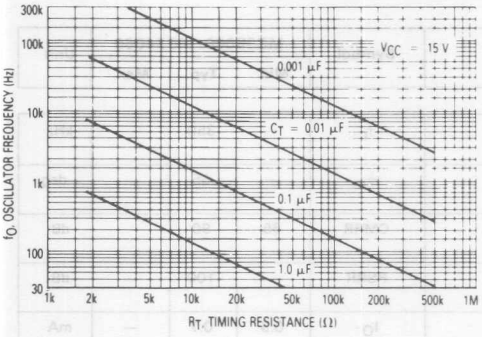


FIGURE 4 — OPEN LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY

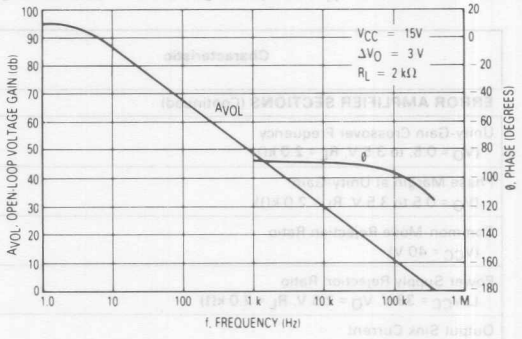


FIGURE 5 — PERCENT DEAD-TIME versus OSCILLATOR FREQUENCY

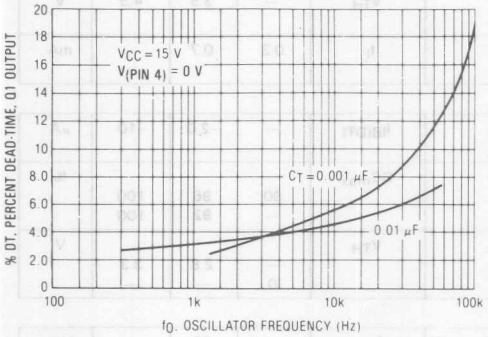


FIGURE 6 — PERCENT DUTY CYCLE versus DEAD-TIME CONTROL VOLTAGE

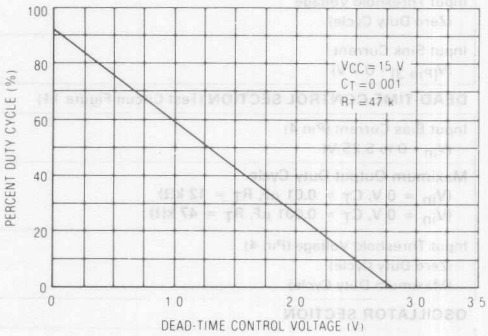


FIGURE 7 — EMITTER FOLLOWER CONFIGURATION OUTPUT-SATURATION VOLTAGE versus EMITTER CURRENT

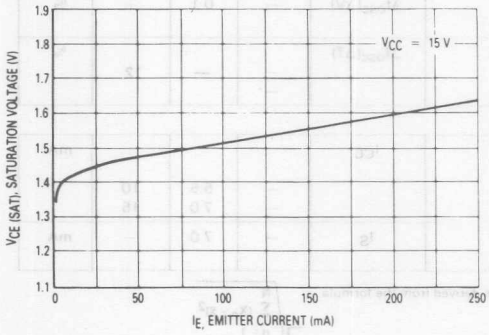


FIGURE 8 — COMMON EMITTER CONFIGURATION OUTPUT-SATURATION VOLTAGE versus COLLECTOR CURRENT

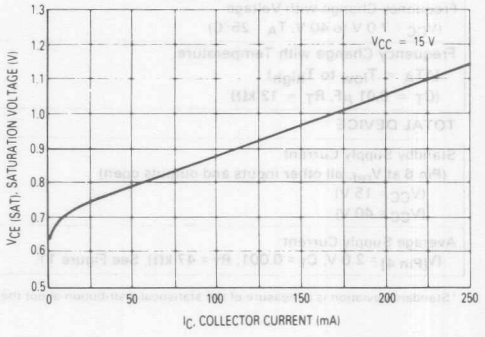


FIGURE 9 — STANDBY-SUPPLY CURRENT versus SUPPLY VOLTAGE

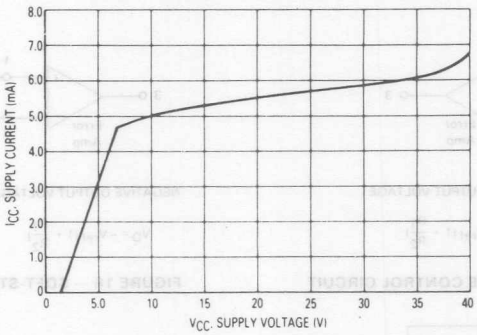


FIGURE 10 — ERROR AMPLIFIER CHARACTERISTICS

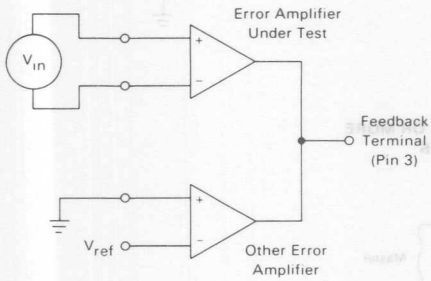


FIGURE 11 — DEAD-TIME AND FEEDBACK CONTROL TEST CIRCUIT

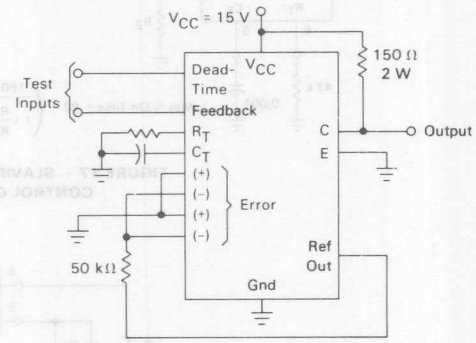


FIGURE 12 — COMMON-EMITTER CONFIGURATION TEST CIRCUIT AND WAVEFORM

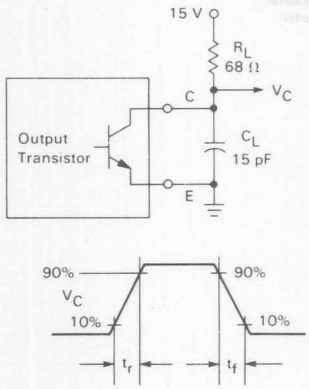


FIGURE 13 — EMITTER-FOLLOWER CONFIGURATION TEST CIRCUIT AND WAVEFORM

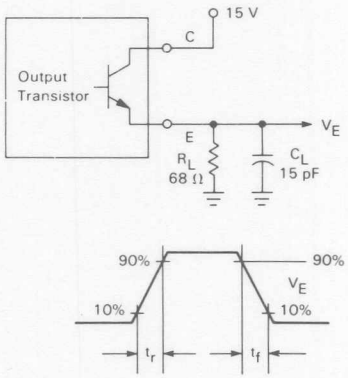


FIGURE 14 — ERROR AMPLIFIER SENSING TECHNIQUES

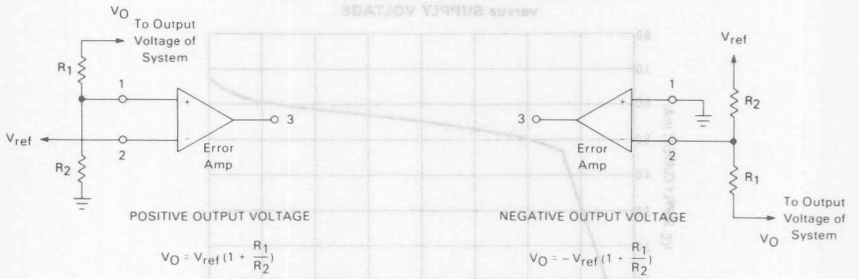


FIGURE 15 — DEAD-TIME CONTROL CIRCUIT

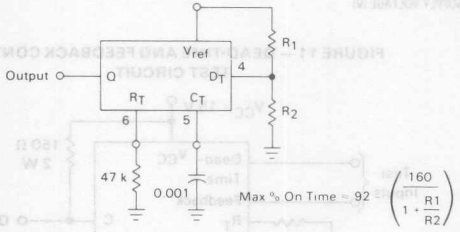


FIGURE 16 — SOFT-START CIRCUIT

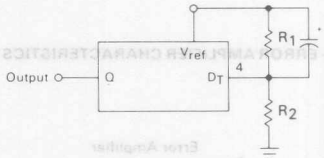


FIGURE 17 — SLAVING TWO OR MORE CONTROL CIRCUITS

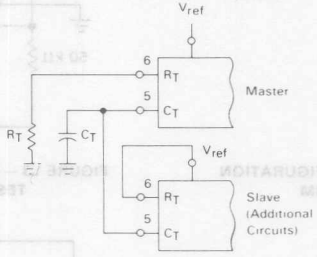
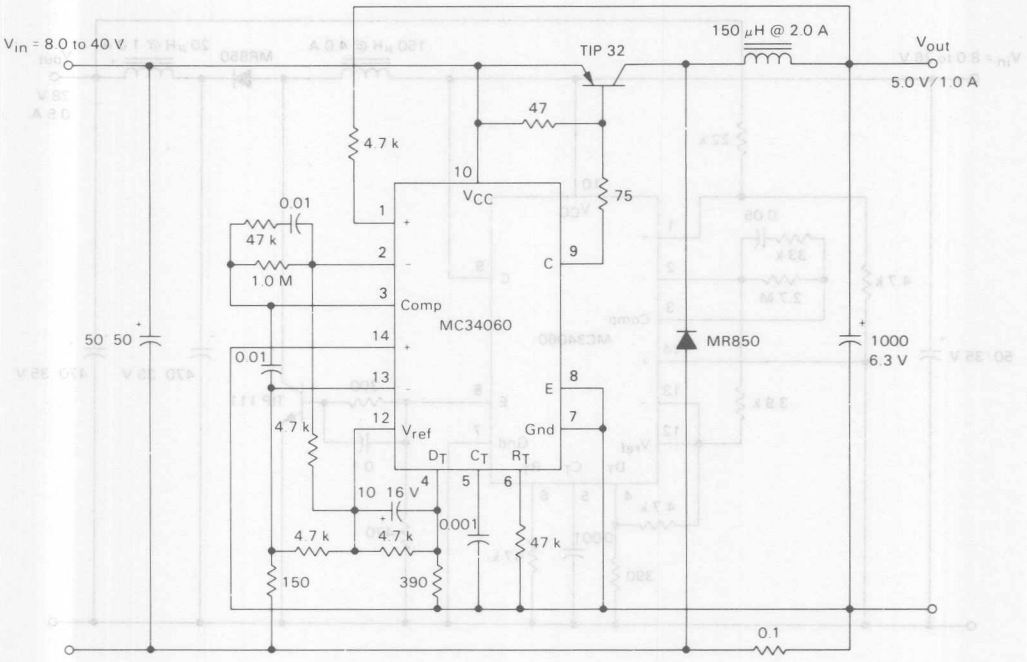
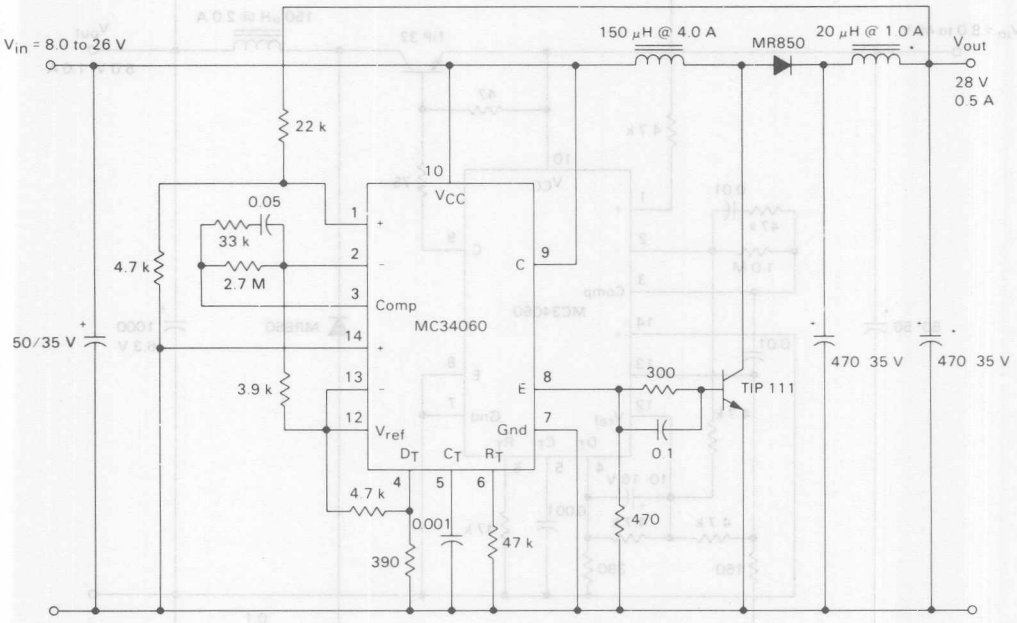


FIGURE 18 — STEP-DOWN CONVERTER WITH SOFT-START AND OUTPUT CURRENT LIMITING



TEST	CONDITIONS	RESULTS
Line Regulation	V_{in} = 8.0 V to 40 V, I_O = 1.0 A	25 mV 0.5%
Load Regulation	V_{in} = 12 V, I_O = 1.0 mA to 1.0 A	3.0 mV 0.06%
Output Ripple	V_{in} = 12 V, I_O = 1.0 A	75 mV p-p P.A.R.D.
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	1.6 A
Efficiency	V_{in} = 12 V, I_O = 1.0 A	73%

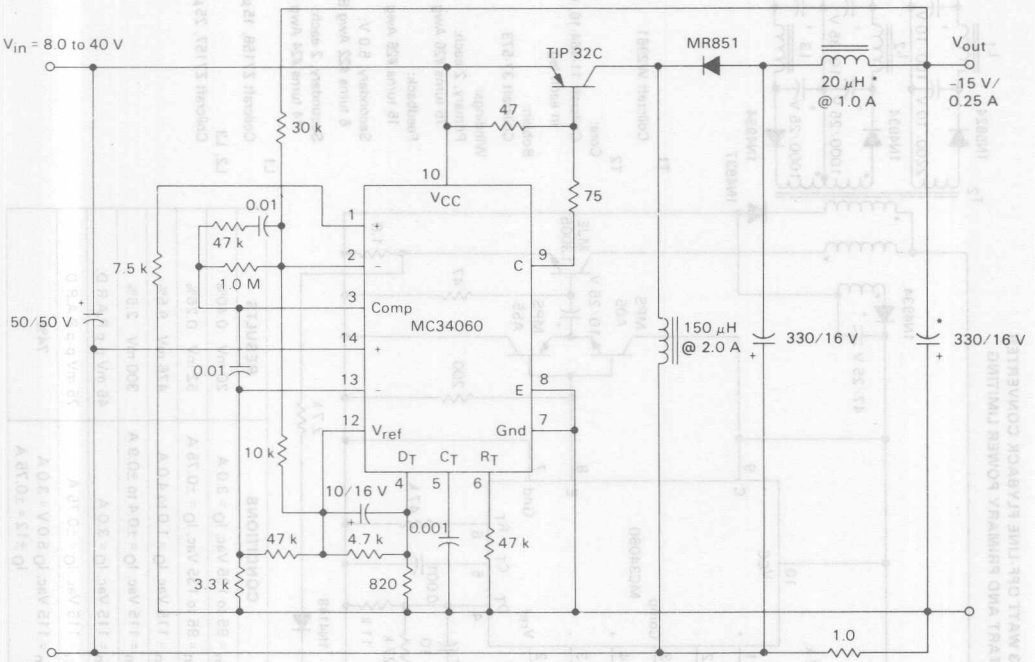
FIGURE 19 — STEP-UP CONVERTER



TEST	CONDITIONS	RESULTS
Line Regulation	V_{in} = 8.0 V to 26 V, I_O = 0.5 A	40 mV 0.14%
Load Regulation	V_{in} = 12 V, I_O = 1.0 mA to 0.5 A	5.0 mV 0.18%
Output Ripple	V_{in} = 12 V, I_O = 0.5 A	24 mV p-p P.A.R.D
Efficiency	V_{in} = 12 V, I_O = 0.5 A	75%

*Optional circuit to minimize output ripple

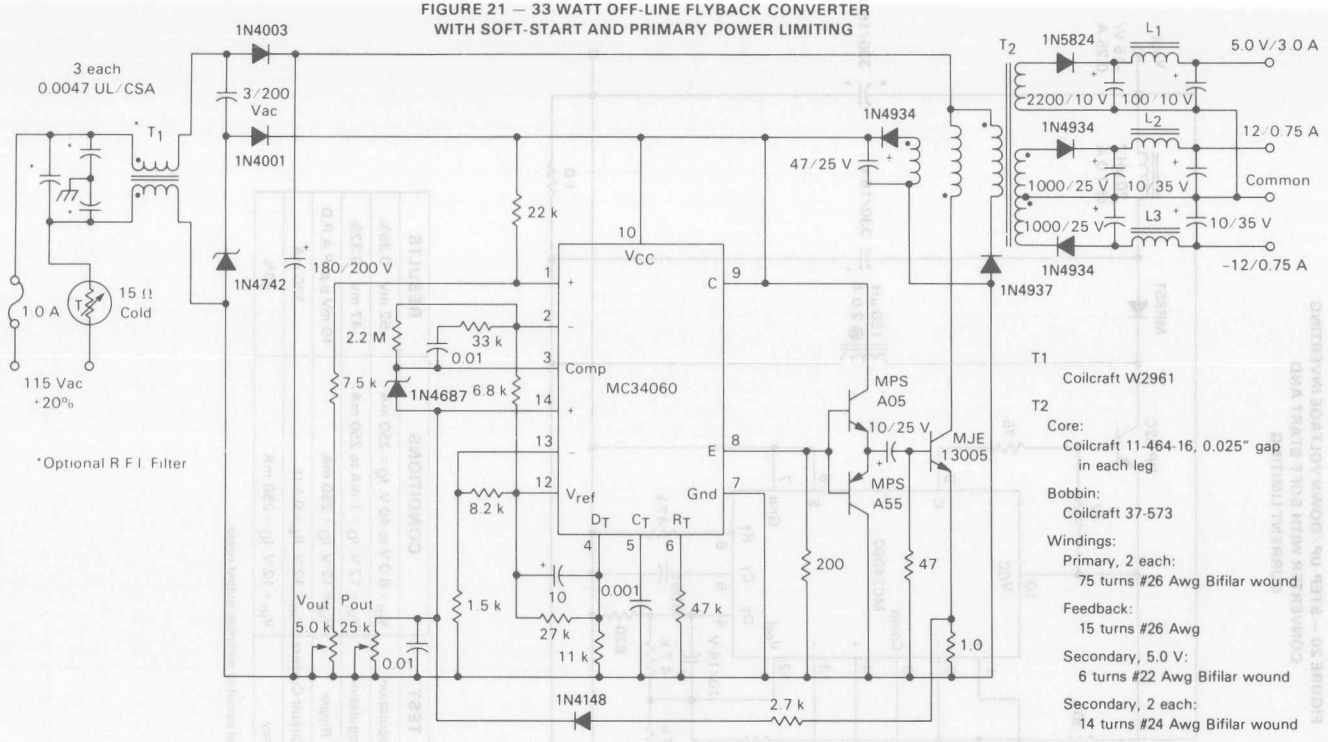
FIGURE 20 — STEP-UP/DOWN VOLTAGE INVERTING CONVERTER WITH SOFT-START AND CURRENT LIMITING



TEST	CONDITIONS	RESULTS
Line Regulation	V_{in} = 8.0 V to 40 V, I_O = 250 mA	52 mV 0.35%
Load Regulation	V_{in} = 12 V, I_O = 1 mA to 250 mA	47 mV 0.32%
Output Ripple	V_{in} = 12 V, I_O = 250 mA	10 mV p.p. P.A.R.D.
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	330 mA
Efficiency	V_{in} = 12 V, I_O = 250 mA	86%

* Optional circuit to minimize output ripple.

FIGURE 21 — 33 WATT OFF-LINE FLYBACK CONVERTER WITH SOFT-START AND PRIMARY POWER LIMITING



T1
Coilcraft W2961

T2
Core:
Coilcraft 11-464-16, 0.025" gap in each leg

Bobbin:
Coilcraft 37-573

Windings:
Primary, 2 each:
75 turns #26 Awg Bifilar wound

Feedback:
15 turns #26 Awg

Secondary, 5.0 V:
6 turns #22 Awg Bifilar wound

Secondary, 2 each:
14 turns #24 Awg Bifilar wound

L1
Coilcraft Z7156, 15 μH @ 5.0 A

L2, L3
Coilcraft Z7157, 25 μH @ 1.0 A

TEST	CONDITIONS	RESULTS
Line Regulation 5.0 V	V_{in} = 95 to 135 Vac, I_O = 3.0 A	20 mV 0.40%
Line Regulation ±12 V	V_{in} = 95 to 135 Vac, I_O = ±0.75 A	52 mV 0.26%
Load Regulation 5.0 V	V_{in} = 115 Vac, I_O = 1.0 to 4.0 A	476 mV 9.5%
Load Regulation ±12 V	V_{in} = 115 Vac, I_O = ±0.4 to ±0.9 A	300 mV 2.5%
Output Ripple 5.0 V	V_{in} = 115 Vac, I_O = 3.0 A	45 mV p-p P.A.R.D.
Output Ripple ±12 V	V_{in} = 115 Vac, I_O = ±0.75 A	75 mV p-p P.A.R.D.
Efficiency	V_{in} = 115 Vac, I_O 5.0 V = 3.0 A I_O ±12 = ±0.75 A	74%

MOTOROLA

MC34060A
MC35060A
MC33060A

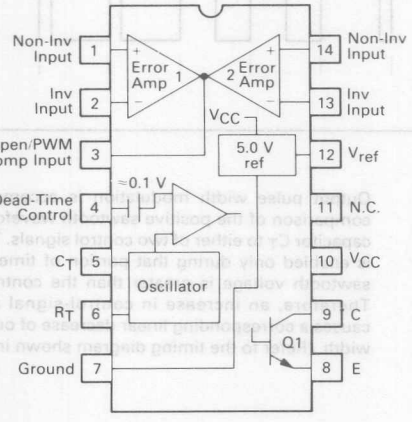
PRECISION SWITCHMODE PULSE WIDTH MODULATION CONTROL CIRCUITS

The MC35060A/MC34060A/MC33060A are low cost fixed frequency, pulse width modulation control circuits designed primarily for single ended SWITCHMODE power supply control. These devices feature:

The MC34060A is specified over the commercial operating range of 0° to +70°C. The MC35060A is specified over the full military range of −55° to +125°C. The MC33060A is specified over the vehicular temperature range of −40° to +85°C.

- Complete Pulse Width Modulation Control Circuitry
- On-Chip Oscillator With Master or Slave Operation
- On-Chip Error Amplifiers
- On-Chip 5.0 Volt Reference, 1.5% Accuracy
- Adjustable Dead Time Control
- Uncommitted Output Transistor Rated to 500 mA Source or Sink
- Undervoltage Lockout
- Available in Surface Mount Package

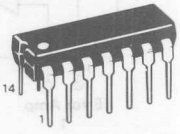
PIN CONNECTIONS



(top view)

PRECISION SWITCHMODE PULSE WIDTH MODULATION CONTROL CIRCUITS

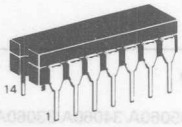
SILICON MONOLITHIC INTEGRATED CIRCUITS



P SUFFIX
PLASTIC PACKAGE
CASE 646-06



D SUFFIX
PLASTIC PACKAGE
CASE 751A-02
SO-14



L SUFFIX
CERAMIC PACKAGE
CASE 632-08

ORDERING INFORMATION

Device	Temperature Range	Package
MC35060AL	−55° to +125°C	Ceramic DIP
MC34060AD	0° to +70°C	SO-14 Plastic DIP
MC34060AP		Plastic DIP
MC33060AD	−40° to +85°C	SO-14 Plastic DIP
MC33060AP		Plastic DIP

FIGURE 1 — BLOCK DIAGRAM

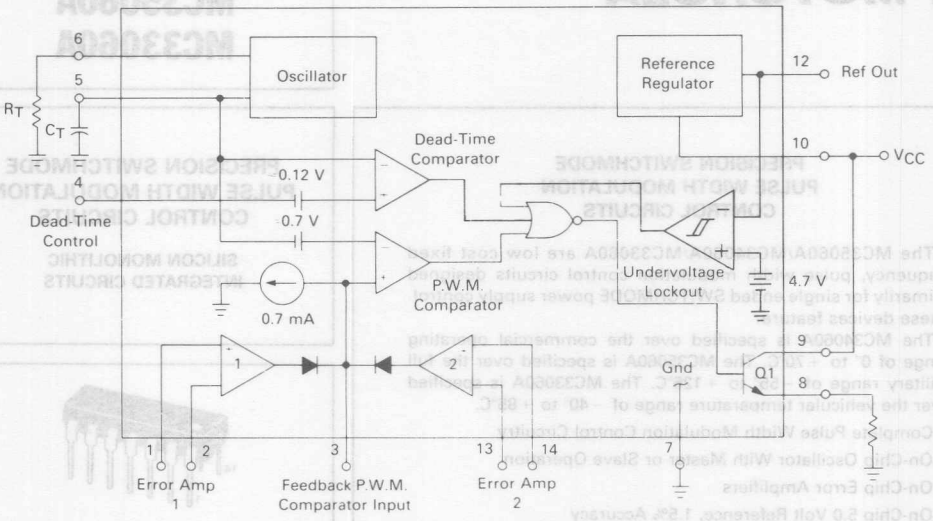
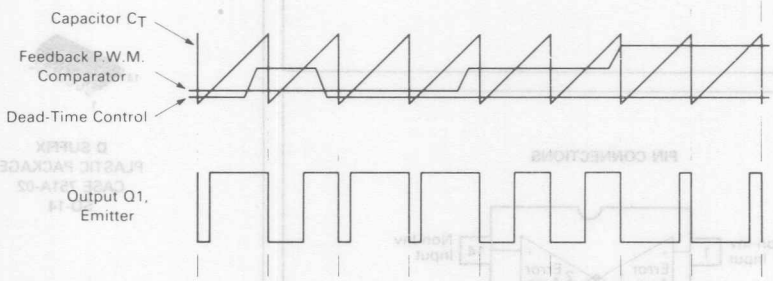


FIGURE 2 — TIMING DIAGRAM



Description

The MC35060A/34060A/33060A is a fixed-frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply. (See Figure 1.) An internal-linear sawtooth oscillator is frequency-programmable by two external components, R_T and C_T. The approximate oscillator frequency is determined by:

$$f_{osc} \cong \frac{1.2}{R_T \bullet C_T}$$

For more information refer to Figure 3.

Output pulse width modulation is accomplished by comparison of the positive sawtooth waveform across capacitor C_T to either of two control signals. The output is enabled only during that portion of time when the sawtooth voltage is greater than the control signals. Therefore, an increase in control-signal amplitude causes a corresponding linear decrease of output pulse width. (Refer to the timing diagram shown in Figure 2.)

The control signals are external inputs that can be fed into the dead-time control, the error amplifier inputs, or the feedback input. The dead-time control comparator has an effective 120 mV input offset which limits the minimum output dead time to approximately the first 4% of the sawtooth-cycle time. This would result in a maximum duty cycle of 96%. Additional dead time may be imposed on the output by setting the dead time-control input to a fixed voltage, ranging between 0 to 3.3 V.

The pulse width modulator comparator provides a means for the error amplifiers to adjust the output pulse width from the maximum percent on-time, established by the dead time control input, down to zero, as the voltage at the feedback pin varies from 0.5 to 3.5 V. Both error amplifiers have a common-mode input range from −0.3 V to (V_{CC} − 2.0 V), and may be used to sense power supply output voltage and current. The error-amplifer outputs are active high and are ORed together at the non-inverting input of the pulse-width modulator comparator. With this configuration, the amplifier that demands minimum output on time, dominates control of the loop.

The MC35060A/34060A/33060A has an internal 5.0 V reference capable of sourcing up to 10 mA of load currents for external bias circuits. The reference has an internal accuracy of ±1.5% with a typical thermal drift of less than 50 mV over an operating temperature range of 0° to +70°C.

MAXIMUM RATINGS (Full operating ambient temperature range applies unless otherwise noted)

Rating	Symbol	MC35060A	MC34060A	MC33060A	Unit
Power Supply Voltage	V_{CC}	42	42	42	V
Collector Output Voltage	V_C	42	42	42	V
Collector Output Current (Note 1)	I_C	500	500	500	mA
Amplifier Input Voltage Range	V_{IR}	−0.3 to +42	−0.3 to +42	−0.3 to +42	V
Power Dissipation @ $T_A \leq 45°C$	P_D	1000	1000	1000	mW
Operating Junction Temperature Plastic Package Ceramic Package	T_J	 — 150	 125 —	 125 —	°C
Operating Ambient Temperature Range	T_A	−55 to +125	0 to 70	−40 to +85	°C
Storage Temperature Range Plastic Package Ceramic Package	T_{stg}	 — −65 to +150	 −55 to +125 —	 −55 to +125 —	°C

Note 1: Maximum thermal limits must be observed.

THERMAL CHARACTERISTICS

Characteristic	Symbol	L Suffix Ceramic Package	P Suffix Plastic Package	D Suffix Plastic Package	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	100	80	120	°C/W
Derating Ambient Temperature	T_A	50	45	45	°C

RECOMMENDED OPERATING CONDITIONS

Condition/Value	Symbol	MC35060A/MC34060A/MC33060A			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	7.0	15	40	V
Collector Output Voltage	V_C	—	30	40	V
Collector Output Current	I_C	—	—	200	mA
Amplifier Input Voltage	V_{in}	−0.3	—	V_{CC} − 2	V
Current Into Feedback Terminal	I_{fb}	—	—	0.3	mA
Reference Output Current	I_{ref}	—	—	10	mA
Timing Resistor	R_T	1.8	47	500	kΩ
Timing Capacitor	C_T	0.0047	0.001	10	μF
Oscillator Frequency	f_{osc}	1.0	25	200	kHz
PWM Input Voltage (Pins 3 and 4)	—	−0.3	—	5.3	V

Characteristic	Symbol	MC35060A/MC34060A/MC33060A Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Voltage (I_O = 1.0 mA, T_A = 25°C)	V_{ref}	4.925	5.0	5.075	V
(I_O = 1.0 mA)		4.9	—	5.1	
Line Regulation (V_{CC} = 7.0 V to 40 V, I_O = 1.0 mA)	Reg_{line}	—	2.0	25	mV
Load Regulation (I_O = 1.0 mA to 10 mA)	Reg_{load}	—	2.0	15	mV
Short-Circuit Output Current (V_{ref} = 0 V)	I_{SC}	15	35	75	mA
OUTPUT SECTION					
Collector Off-State Current (V_{CC} = 40 V, V_{CE} = 40 V)	$I_{C(off)}$	—	2.0	100	μA
Emitter Off-State Current (V_{CC} = 40 V, V_C = 40 V, V_E = 0 V)	$I_{E(off)}$	—	—	100	μA
Collector-Emitter Saturation Voltage (Note 2)					V
Common-Emitter (V_E = 0 V, I_C = 200 mA)	$V_{sat(C)}$	—	1.1	1.5	
Emitter-Follower (V_C = 15 V, I_E = 200 mA)	$V_{sat(E)}$	—	1.5	2.5	
Output Voltage Rise Time (T_A = 25°C)	t_r				ns
Common-Emitter (See Figure 12)		—	100	200	
Emitter-Follower (See Figure 13)		—	100	200	
Output Voltage Fall Time (T_A = 25°C)	t_f				ns
Common-Emitter (See Figure 12)		—	40	100	
Emitter-Follower (See Figure 13)		—	40	100	

Characteristic	Symbol	MC35060A/MC34060A/MC33060A Min	Typ	Max	Unit
ERROR AMPLIFIER SECTIONS					
Input Offset Voltage ($V_{O[Pin\ 3]}$ = 2.5 V)	V_{IO}	—	2.0	10	mV
Input Offset Current ($V_{O[Pin\ 3]}$ = 2.5 V)	I_{IO}	—	5.0	250	nA
Input Bias Current ($V_{O[Pin\ 3]}$ = 2.5 V)	I_{IB}	—	0.1	2.0	μA
Input Common-Mode Voltage Range (V_{CC} = 40 V)	V_{ICR}	0 to V_{CC} − 2.0	—	—	V
Inverting Input Voltage Range	$V_{IR(INV)}$	0.3 to V_{CC} − 2.0	—	—	V
Open Loop Voltage Gain (ΔV_O = 3.0 V, V_O = 0.5 to 3.5 V, R_L = 2.0 kΩ)	A_{VOL}	70	95	—	dB

Note 2: Low duty cycle techniques are used during test to maintain junction temperature as close to ambient temperatures as possible.

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, C_T = 0.01 μF, R_T = 12 kΩ unless otherwise noted. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies unless otherwise noted.)

Characteristic	Symbol	MC35060A/MC34060A/MC33060A Min	Typ	Max	Unit
ERROR AMPLIFIER SECTIONS (Continued)					
Unity-Gain Crossover Frequency (V_O = 0.5 to 3.5 V, R_L = 2.0 kΩ)	f_c	—	600	—	kHz
Phase Margin at Unity-Gain (V_O = 0.5 to 3.5 V, R_L = 2.0 kΩ)	ϕ_m	—	65	—	deg.
Common-Mode Rejection Ratio (V_{CC} = 40 V, V_{in} = 0 V to 38 V)	CMRR	65	90	—	dB
Power Supply Rejection Ratio (ΔV_{CC} = 33 V, V_O = 2.5 V, R_L = 2.0 kΩ)	PSRR	—	100	—	dB
Output Sink Current ($V_{O[Pin\ 3]}$ = 0.7 V)	I_O-	0.3	0.7	—	mA
Output Source Current ($V_{O[Pin\ 3]}$ = 3.5 V)	I_O+	−2.0	−4.0	—	mA
PWM COMPARATOR SECTION (Test circuit Figure 11)					
Input Threshold Voltage (Zero Duty Cycle)	V_{TH}	—	3.5	4.5	V
Input Sink Current ($V_{[Pin\ 3]}$ = 0.7 V)	I_I	0.3	0.7	—	mA
DEAD-TIME CONTROL SECTION (Test Circuit Figure 11)					
Input Bias Current (Pin 4) (V_{in} = 0 to 5.25 V)	$I_{IB(DT)}$	—	−1.0	−10	μA
Maximum Output Duty Cycle	DC_{max}				%
(V_{in} = 0 V, C_T = 0.01 μF, R_T = 12 kΩ)		90	96	100	
(V_{in} = 0 V, C_T = 0.001 μF, R_T = 47 kΩ)		—	92	—	
Input Threshold Voltage (Pin 4)	V_{TH}				V
(Zero Duty Cycle)		—	2.8	3.3	
(Maximum Duty Cycle)		0	—	—	
OSCILLATOR SECTION					
Frequency (C_T = 0.01 μF, R_T = 12 kΩ)	f_{osc}				kHz
T_A = 25°C		9.7	10.5	11.3	
T_A = T_{low} to T_{high}		9.5	—	12.5	
(C_T = 0.001 μF, R_T = 47 kΩ)		—	25	—	
Standard Deviation of Frequency* (C_T = 0.001 μF, R_T = 47 kΩ)	σf_{osc}	—	1.5	—	%
Frequency Change with Voltage (V_{CC} = 7.0 V to 40 V)	$\Delta f_{osc}(\Delta V)$	—	0.5	2.0	%
Frequency Change with Temperature	$\Delta f_{osc}(\Delta T)$				%
(ΔT_A = T_{low} to T_{high})		—	4.0	—	
(C_T = 0.01 μF, R_T = 12 kΩ)		—	—	—	
UNDERVOLTAGE LOCKOUT SECTION					
Turn-On Threshold (V_{CC} increasing, I_{ref} = 1.0 mA)	V_{th}	4.0	4.7	5.5	V
Hysteresis	V_H	50	150	300	mV
TOTAL DEVICE					
Standby Supply Current (Pin 6 at V_{ref}, all other inputs and outputs open)	I_{CC}				mA
(V_{CC} = 15 V)		—	5.5	10	
(V_{CC} = 40 V)		—	7.0	15	
Average Supply Current ($V_{[Pin\ 4]}$ = 2.0 V, C_T = 0.001 μF, R_T = 47 kΩ). See Figure 11.	I_S	—	7.0	—	mA

*Standard deviation is a measure of the statistical distribution about the mean as derived from the formula: $\sigma = \sqrt{\frac{\sum_{n=1}^{N} (X_n - x)^2}{N-1}}$

3

FIGURE 3 — OSCILLATOR FREQUENCY versus TIMING RESISTANCE

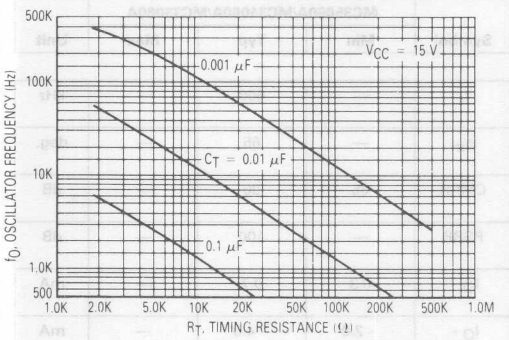


FIGURE 4 — OPEN-LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY

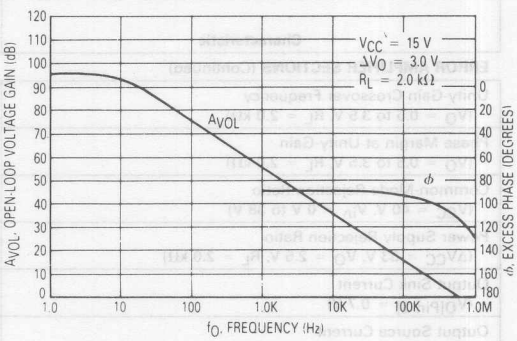


FIGURE 5 — PERCENT DEAD-TIME versus OSCILLATOR FREQUENCY

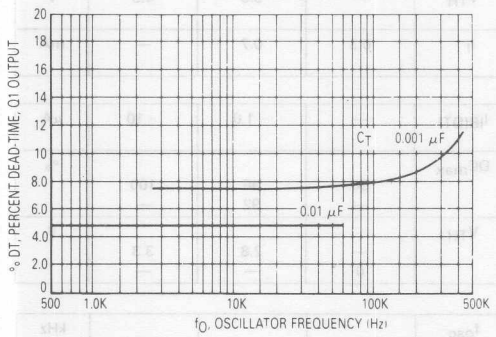


FIGURE 6 — PERCENT DUTY CYCLE versus DEAD-TIME CONTROL VOLTAGE

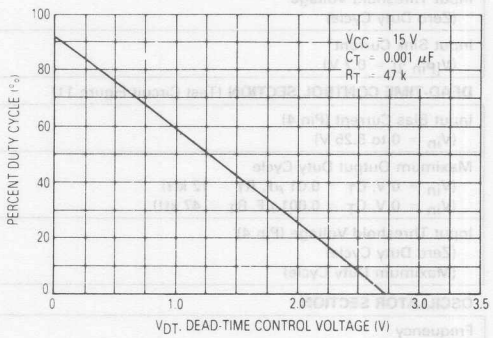


FIGURE 7 — EMITTER FOLLOWER CONFIGURATION OUTPUT SATURATION VOLTAGE versus EMITTER CURRENT

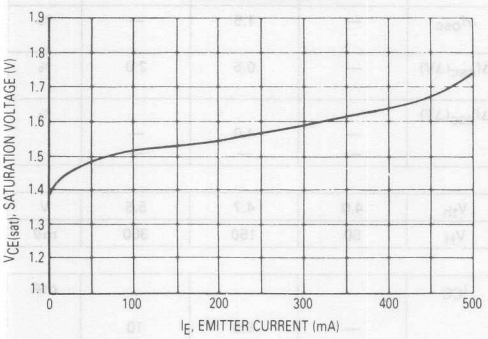


FIGURE 8 — COMMON EMITTER CONFIGURATION OUTPUT SATURATION VOLTAGE versus COLLECTOR CURRENT

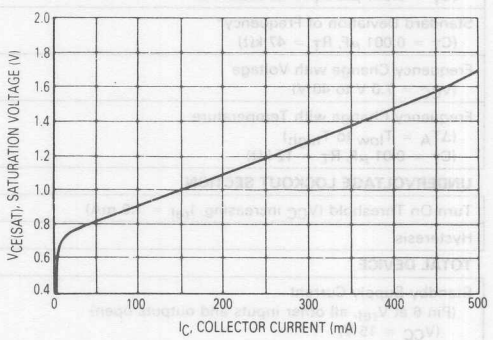


FIGURE 9 — STANDBY SUPPLY CURRENT versus SUPPLY VOLTAGE

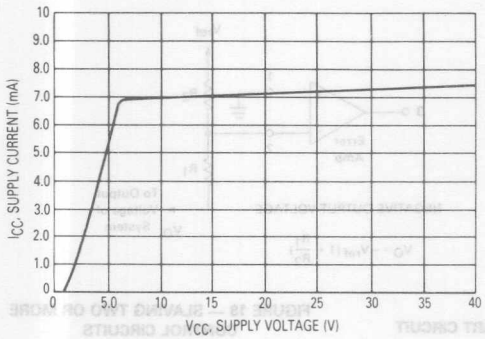


FIGURE 10 — UNDERVOLTAGE LOCKOUT THRESHOLDS versus REFERENCE LOAD CURRENT

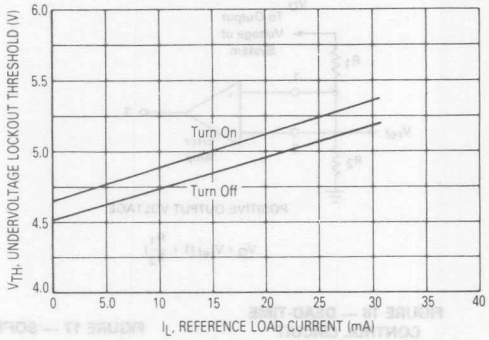


FIGURE 11 — ERROR AMPLIFIER CHARACTERISTICS

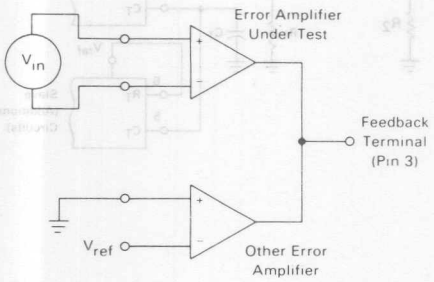


FIGURE 12 — DEAD-TIME AND FEEDBACK CONTROL TEST CIRCUIT

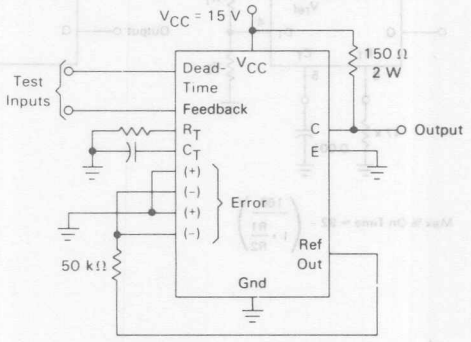


FIGURE 13 — COMMON-EMITTER CONFIGURATION TEST CIRCUIT AND WAVEFORM

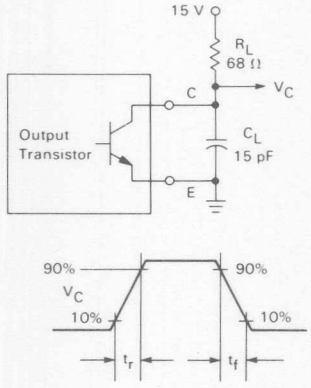
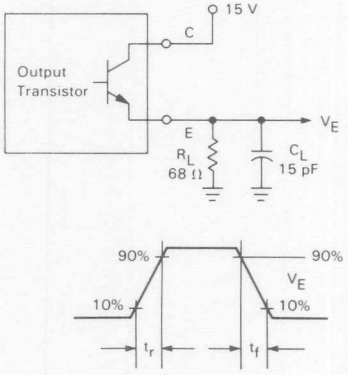


FIGURE 14 — EMITTER-FOLLOWER CONFIGURATION TEST CIRCUIT AND WAVEFORM



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FIGURE 15 — ERROR AMPLIFIER SENSING TECHNIQUES

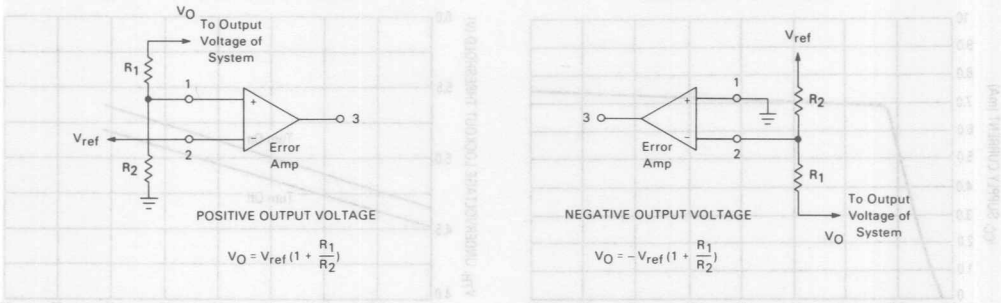
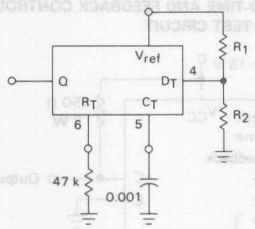


FIGURE 16 — DEAD-TIME CONTROL CIRCUIT



Max % On Time ≈ 92 − $\left(\frac{160}{1 + \frac{R1}{R2}}\right)$

FIGURE 17 — SOFT-START CIRCUIT

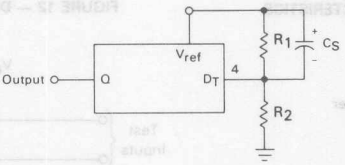
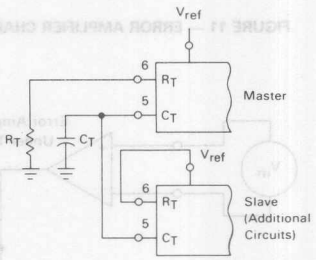
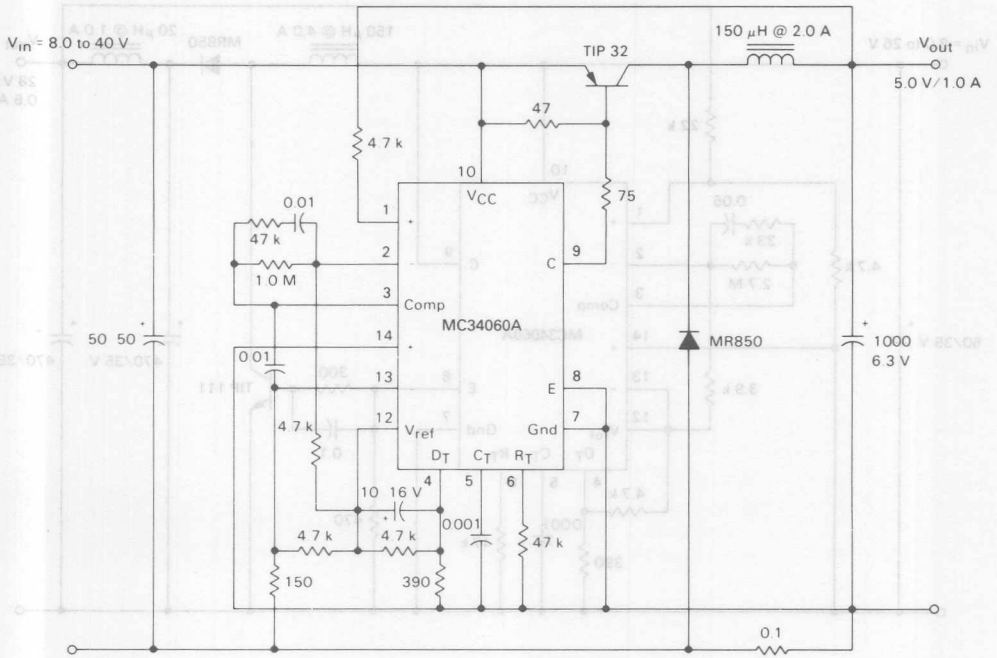


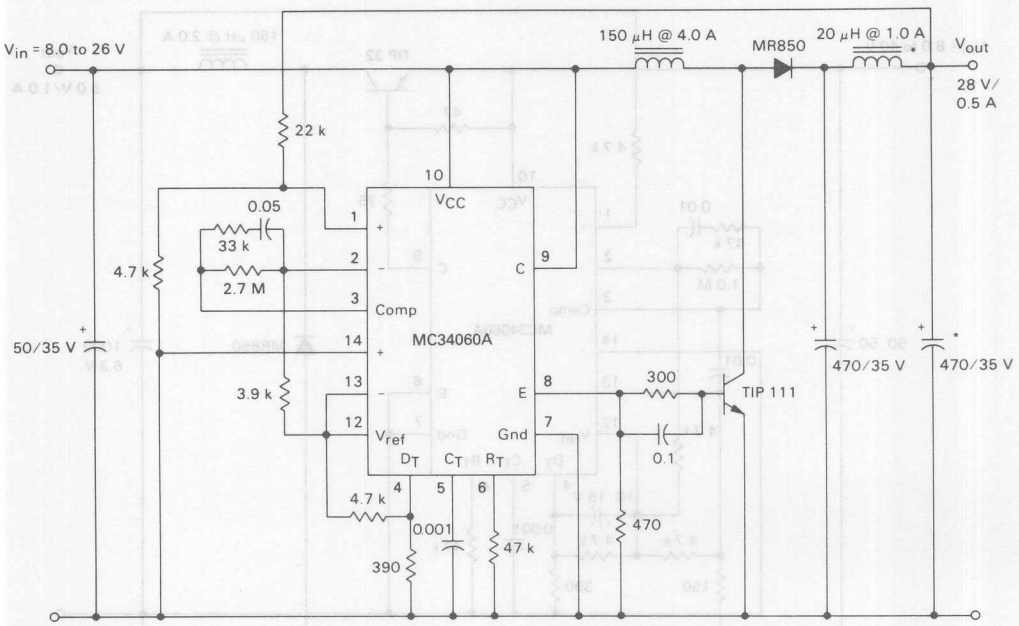
FIGURE 18 — SLAVING TWO OR MORE CONTROL CIRCUITS





TEST	CONDITIONS	RESULTS
Line Regulation	V_{in} = 8.0 V to 40 V, I_O = 1.0 A	25 mV 0.5%
Load Regulation	V_{in} = 12 V, I_O = 1.0 mA to 1.0 A	3.0 mV 0.06%
Output Ripple	V_{in} = 12 V, I_O = 1.0 A	75 mV p-p P.A.R.D.
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	1.6 A
Efficiency	V_{in} = 12 V, I_O = 1.0 A	73%

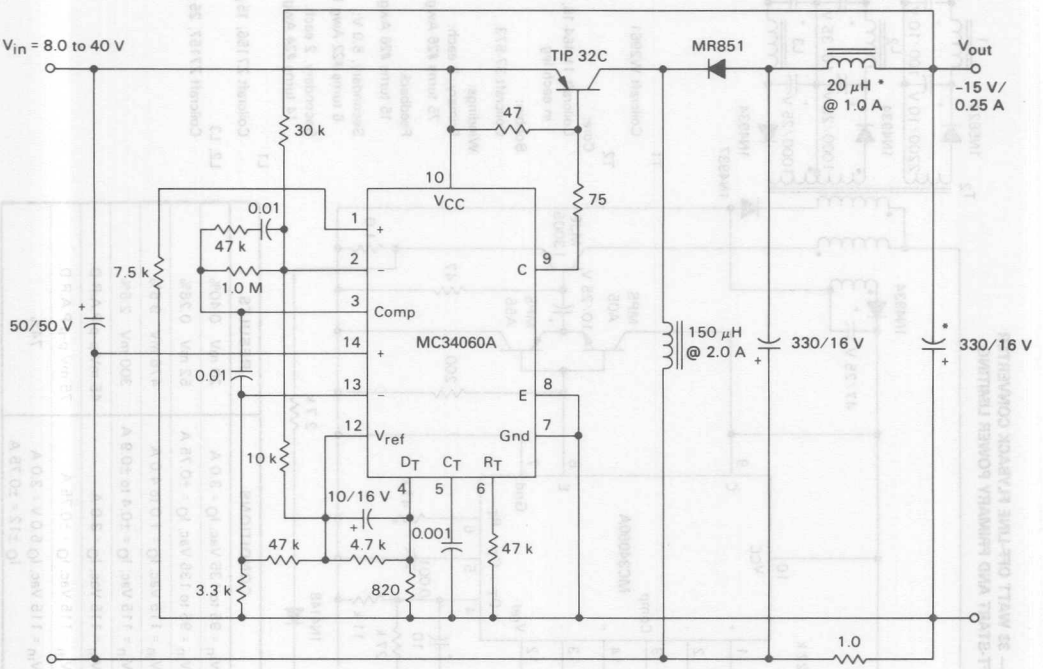
FIGURE 20 — STEP-UP CONVERTER



TEST	CONDITIONS	RESULTS
Line Regulation	V_{in} = 8.0 V to 26 V, I_O = 0.5 A	40 mV 0.14%
Load Regulation	V_{in} = 12 V, I_O = 1.0 mA to 0.5 A	5.0 mV 0.18%
Output Ripple	V_{in} = 12 V, I_O = 0.5 A	24 mV p-p P.A.R.D.
Efficiency	V_{in} = 12 V, I_O = 0.5 A	75%

*Optional circuit to minimize output ripple.

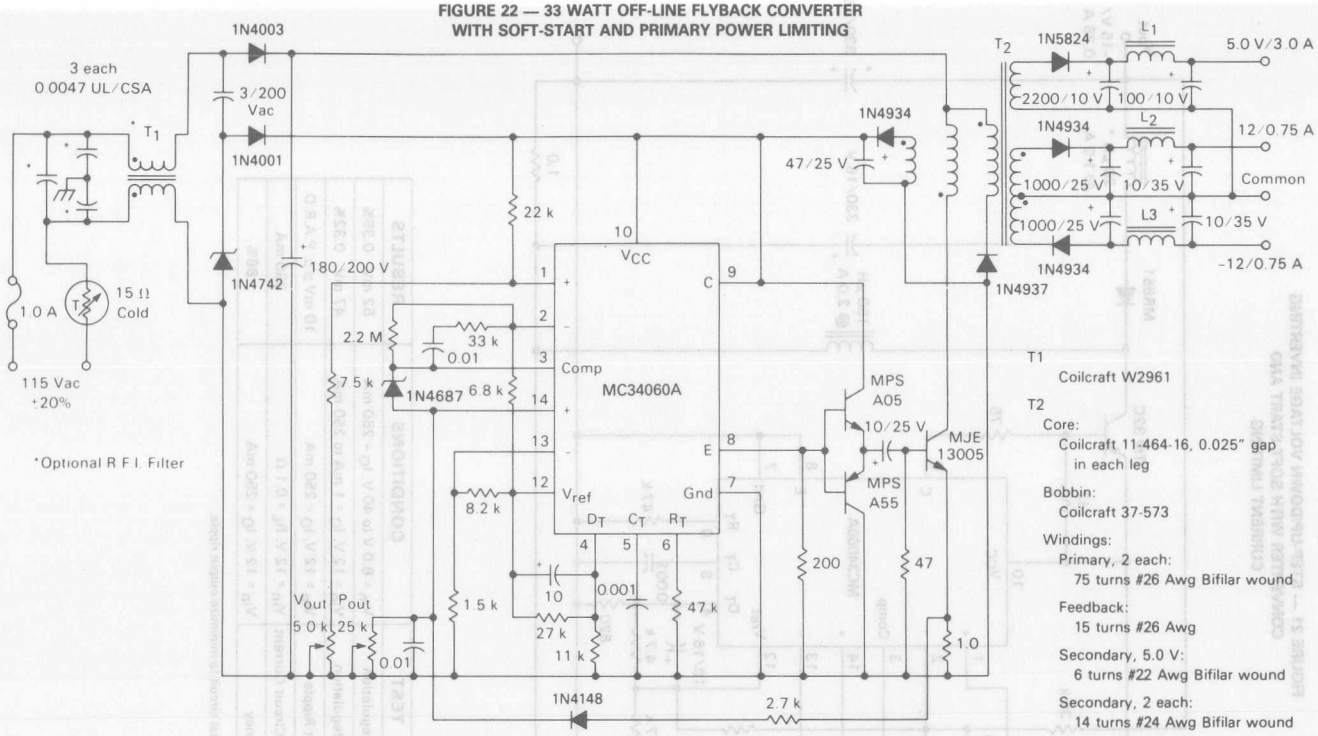
FIGURE 21 — STEP-UP/DOWN VOLTAGE INVERTING CONVERTER WITH SOFT-START AND CURRENT LIMITING



TEST	CONDITIONS	RESULTS
Line Regulation	V_{in} = 8.0 V to 40 V, I_O = 250 mA	52 mV 0.35%
Load Regulation	V_{in} = 12 V, I_O = 1 mA to 250 mA	47 mV 0.32%
Output Ripple	V_{in} = 12 V, I_O = 250 mA	10 mV p.p. P.A.R.D.
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	330 mA
Efficiency	V_{in} = 12 V, I_O = 250 mA	86%

*Optional circuit to minimize output ripple.

FIGURE 22 — 33 WATT OFF-LINE FLYBACK CONVERTER WITH SOFT-START AND PRIMARY POWER LIMITING



T1
Coilcraft W2961

T2
Core:
Coilcraft 11-464-16, 0.025" gap in each leg

Bobbin:
Coilcraft 37-573

Windings:
Primary, 2 each:
75 turns #26 Awg Bifilar wound

Feedback:
15 turns #26 Awg

Secondary, 5.0 V:
6 turns #22 Awg Bifilar wound

Secondary, 2 each:
14 turns #24 Awg Bifilar wound

L1
Coilcraft Z7156, 15 μH @ 5.0 A

L2, L3
Coilcraft Z7157, 25 μH @ 1.0 A

TEST	CONDITIONS	RESULTS
Line Regulation 5.0 V	V_{in} = 95 to 135 Vac, I_O = 3.0 A	20 mV 0.40%
Line Regulation ±12 V	V_{in} = 95 to 135 Vac, I_O = ±0.75 A	52 mV 0.26%
Load Regulation 5.0 V	V_{in} = 115 Vac, I_O = 1.0 to 4.0 A	476 mV 9.5%
Load Regulation ±12 V	V_{in} = 115 Vac, I_O = ±0.4 to ±0.9 A	300 mV 2.5%
Output Ripple 5.0 V	V_{in} = 115 Vac, I_O = 3.0 A	45 mV p-p P.A.R.D.
Output Ripple ±12 V	V_{in} = 115 Vac, I_O = ±0.75 A	75 mV p-p P.A.R.D.
Efficiency	V_{in} = 115 Vac, I_O 5.0 V = 3.0 A I_O ±12 = ±0.75 A	74%

MOTOROLA

MC34061
MC34061A

Advance Information

THREE-TERMINAL OVERVOLTAGE "CROWBAR" SENSING CIRCUIT

The MC34061,A overvoltage protection (OVP) circuit, in combination with two external programming resistors and a "crowbar" SCR, protects sensitive electronic circuitry from overvoltage damage. It senses an overvoltage condition and quickly "crowbars," or short circuits, the supply. An external capacitor may be used to program a minimum overvoltage duration before tripping, thus providing noise immunity.

This three-terminal circuit provides a cost-effective means of protecting either positive or negative power supplies. The unique design of the MC34061,A eliminates trip voltage and temperature drift errors due to SCR gate variations.

The basic MC34061,A device offers a ±2% tolerance on the sense trip voltage. The A-suffix device has a ±1% sense trip voltage specification and other key parameters have tightened limits. The device is available in a low-cost plastic package and features:

age and features:

- Unique Three-Terminal Design
- SCR Gate Drive Output of 200 mA
- Sense Voltage of 2.5 V ±1% or ±2%
- Hysteresis of 250 mV
- Wide Supply Range: 4.0 V ≤ V_{CC} ≤ 41 V

THREE-TERMINAL PROGRAMMABLE OVERVOLTAGE SENSING CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT

3

P SUFFIX
PLASTIC PACKAGE
CASE 29-04



Pin 1. V_{CC}
2. Drive Output
3. Sense

"NOT FOR NEW DESIGN-INS"

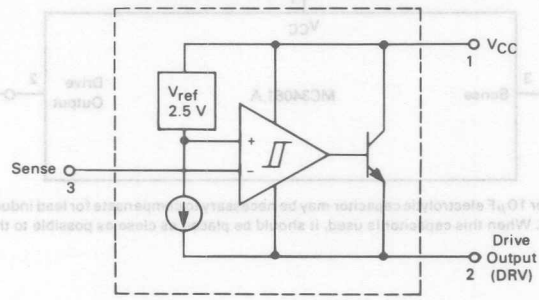
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Operating Voltage	$V_{CC} - V_{DRV}$	40	Vdc
Sense Voltage	V_{Sense}	40	Vdc
Drive Output Current	I_{DRV}	Internally Limited	mA
Operating Ambient Temperature Range	T_A	0 to +70	°C
Operating Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ORDERING INFORMATION

Device	Temperature Range	Package
MC34061P,AP	0 to +70° C	Plastic TO-92

FUNCTIONAL BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

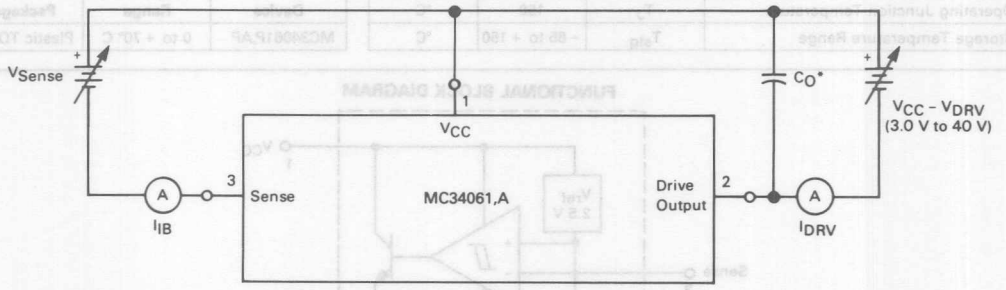
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ELECTRICAL CHARACTERISTICS ($V_{CC} - V_{DRV}$ = 5.0 V; T_A = T_{low} to T_{high} [see Note 1] unless otherwise specified)

Characteristic	Symbol	MC34061A			MC34061			Unit
		Min	Typ	Max	Min	Typ	Max	
Operating Voltage Range	$V_{CC} - V_{DRV}$	3.0	—	40	3.0	—	40	Vdc
Sense Trip Voltage T_A = 25°C T_{low} to T_{high} (Note 1)	V_{Sense}	 2.475 2.45	 2.5 2.5	 2.525 2.55	 2.45 2.4	 2.5 2.5	 2.55 2.6	Vdc
Line Regulation, V_{Sense} (3.0 ≤ $V_{CC} - V_{DRV}$ ≤ 40 V) T_A = 25°C T_{low} to T_{high} (Note 1)	Reg_{line}	 — —	 0.001 0.001	 0.005 0.01	 — —	 0.001 0.001	 0.01 0.02	%/V
Input Bias Current, Sense Pin At Trip Point (Note 2) After Trip (V_{Sense} = 3.0 V)	I_{IB}	 — —	 0.3 0.9	 1.0 3.0	 — —	 0.3 0.9	 2.0 6.0	μA
Hysteresis Voltage, Sense Pin	V_H	—	250	—	—	250	—	mV
Drive Output Current, ON State T_J = 25°C T_{low} to T_{high} (Note 1)	$I_{DRV(on)}$	 130 90	 200 —	 300 350	 130 90	 200 —	 300 350	mA
Drive Output Current, OFF State $V_{CC} - V_{DRV}$ = 5.0 V 3.0 V ≤ $V_{CC} - V_{DRV}$ ≤ 40 V	$I_{DRV(off)}$	 0.2 0.2	 0.6 0.6	 1.0 1.5	 0.2 0.2	 0.6 0.6	 1.0 1.5	mA
Drive Output Current Slew Rate T_A = 25°C	di/dt	—	2.0	—	—	2.0	—	A/μs
Drive Output V_{CC} Transient Rejection $V_{CC} - V_{DRV}$ = 0 V to 15 V at dV/dt = 200 V/μs; V_{Sense} = 0 V; T_A = 25°C	$\Delta I_{DRV(trans)}$	—	1.0	—	—	1.0	—	mA (Peak)
Propagation Delay Time (T_A = 25°C) 500 mV Overdrive	t_{PLH}	—	500	—	—	500	—	ns

NOTES:
(1) T_{low} to T_{high} = 0°C to 70°C
(2) This specification is an engineering estimate based on design parameters, and is not tested.

FIGURE 1 — STANDARD TEST CIRCUIT



*A 1.0 μF tantalum or 10 μF electrolytic capacitor may be necessary to compensate for lead inductance when measuring Hysteresis Voltage. When this capacitor is used, it should be placed as close as possible to the device package.

TYPICAL CHARACTERISTICS

FIGURE 2 — DRIVE CURRENT versus SENSE VOLTAGE

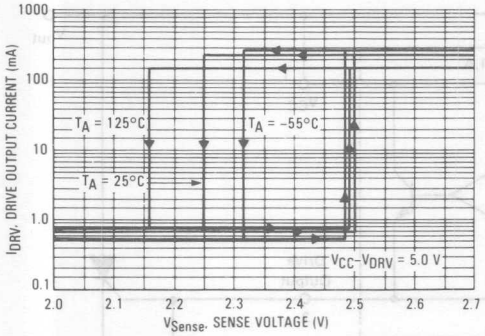


FIGURE 3 — SENSE TRIP VOLTAGE versus TEMPERATURE

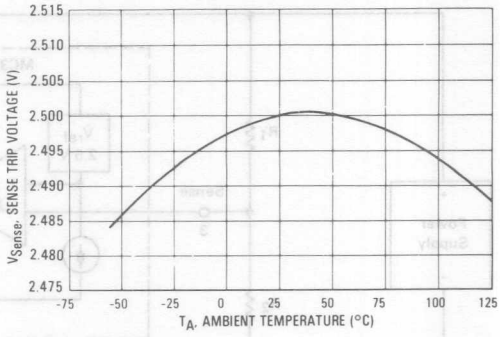


FIGURE 4 — OFF STATE DRIVE CURRENT versus SUPPLY VOLTAGE

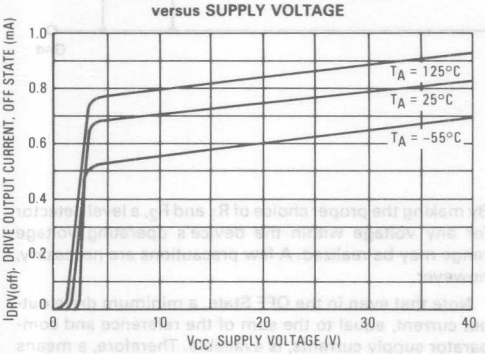


FIGURE 5 — INPUT BIAS CURRENT versus SENSE VOLTAGE

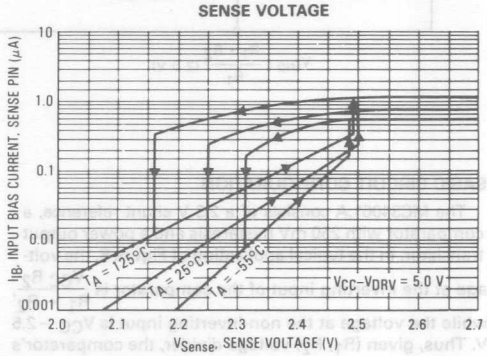


FIGURE 6 — DELAY CAPACITANCE versus DELAY TIME

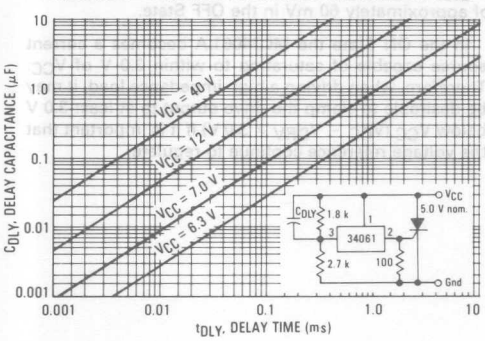
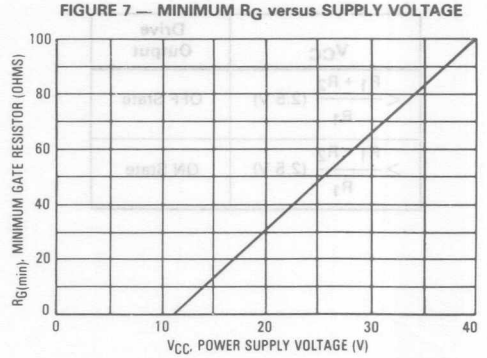
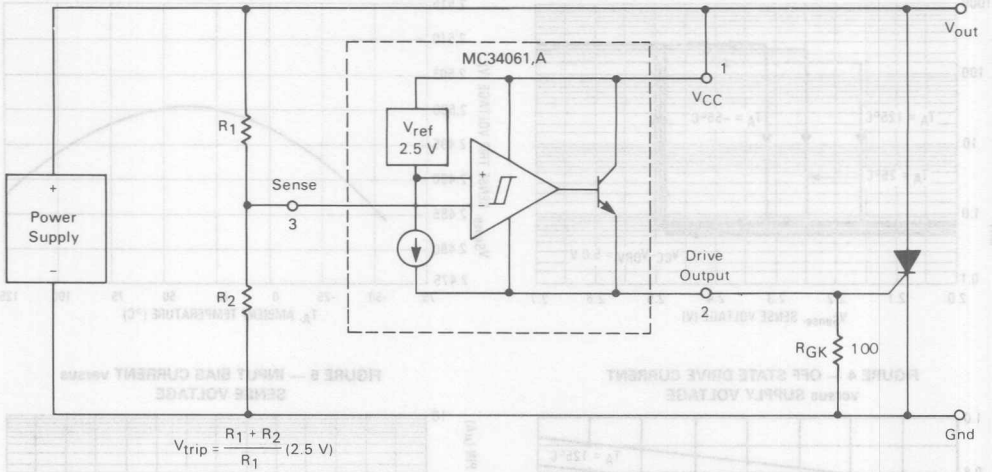


FIGURE 7 — MINIMUM R_G versus SUPPLY VOLTAGE



APPLICATIONS INFORMATION

FIGURE 8 — BLOCK DIAGRAM AND TYPICAL APPLICATION



BASIC CIRCUIT CONFIGURATION

The MC34061,A consists of a 2.5 V shunt reference, a comparator with 250 mV hysteresis and a power output transistor. In the typical application of Figure 8, the voltage at the inverting input of the comparator is $\frac{V_{CC}\ R_2}{R_1 + R_2}$, while the voltage at the non-inverting input is $V_{CC} - 2.5$ V. Thus, given (R_1, R_2) voltage divider, the comparator's output state is a function of V_{CC}. The following table applies:

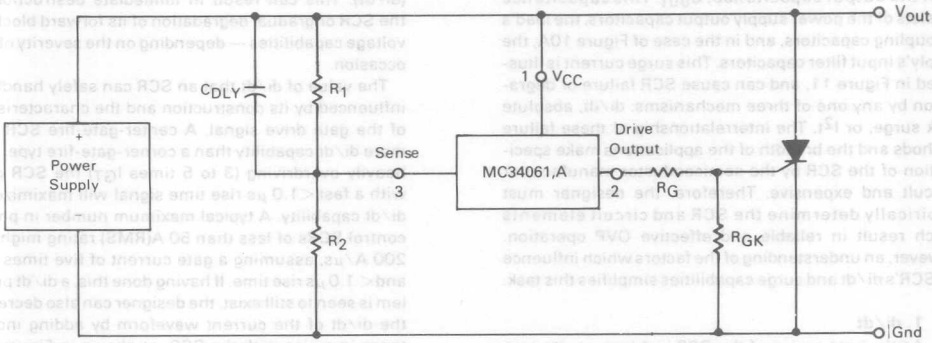
V_{CC}	Drive Output
$< \frac{R_1 + R_2}{R_1}$ (2.5 V)	OFF State
$> \frac{R_1 + R_2}{R_1}$ (2.5 V)	ON State

By making the proper choice of R_1 and R_2, a level detector for any voltage within the device's operating voltage range may be realized. A few precautions are necessary, however.

Note that even in the OFF State, a minimum drive output current, equal to the sum of the reference and comparator supply currents, is available. Therefore, a means of shunting this current away from the driven circuit is necessary. In the example of Figure 8, a 100 Ω resistor (R_{GK}) is used, producing a voltage at the Drive Output of approximately 60 mV in the OFF State.

In the ON State the MC34061,A becomes a current source capable of saturating to within 2.0 V of V_{CC}. Therefore, when driving a high impedance load, it may be desirable to clamp the drive output to at least 3.0 V below V_{CC} ($V_{CC} - V_{DRV} \geq 3.0$ V) if it is important that the voltage reference continue to regulate.

FIGURE 9 — OVERVOLTAGE PROTECTION WITH TIME DELAY



PROGRAMMING A MINIMUM OVERVOLTAGE DURATION BEFORE TRIPPING

A time delay may be programmed into the operation of the MC34061,A to provide noise immunity. This time delay is implemented by adding a capacitor (C_{DLY}) between the V_{CC} and Sense leads as shown in Figure 9. The time delay obtained by this technique is a function of R_1, R_2 and C_{DLY} as well as the nominal supply voltage, $V_{CC(nom)}$, and the overvoltage supply voltage, V_{CC}. The nominal supply voltage determines the initial charge on C_{DLY}, while the magnitude of the overvoltage condition determines the rate at which C_{DLY} charges to the reference voltage, V_{ref} = 2.5 V. Thus, for a given R_1, R_2 and C_{DLY}, the time delay is reduced as the overvoltage is increased. The expression for the time delay, T_{DLY}, is:

$$t_{DLY} = \frac{R_1 R_2 C_{DLY}}{R_1 + R_2} \ln \left[\frac{V_{CC} - V_{CC(nom)}}{V_{CC} - V_{trip}} \right]$$

where:

$$V_{trip} = \frac{R_1 + R_2}{R_1} (2.5\ V)$$

Figure 6 shows the C_{DLY} values versus delay time (t_{DLY}) for a typical 5.0 V power supply protection circuit. The figure also shows the change in t_{DLY} with variations in the overvoltage supply, V_{CC}. In this example R_1 = 1.8 k, R_2 = 2.7 k, $V_{CC(nom)}$ = 5.0 V, and V_{trip} = 6.25 V.

THE NEED FOR A GATE RESISTOR

For power supplies above 11 V, a gate resistor, R_G, in series with the SCR gate is recommended to limit the power dissipated by the IC to approximately 2.0 W. This resistor will protect the MC34061,A in the event of a defective or missing SCR, while allowing the maximum drive output current to the gate of the SCR. Figure 7 shows the minimum recommended gate resistor, $R_{G(min)}$, versus the power supply voltage, V_{CC}. A larger value of R_G may be used if less drive current is needed.

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CROWBAR SCR CONSIDERATIONS

Referring to Figure 10, it can be seen that the crowbar SCR, when activated, is subject to a large current surge from the output capacitance, C_{out}. This capacitance consists of the power supply output capacitors, the load's decoupling capacitors, and in the case of Figure 10A, the supply's input filter capacitors. This surge current is illustrated in Figure 11, and can cause SCR failure or degradation by any one of three mechanisms: di/dt, absolute peak surge, or I^2t. The interrelationship of these failure methods and the breadth of the applications make specification of the SCR by the semiconductor manufacturer difficult and expensive. Therefore, the designer must empirically determine the SCR and circuit elements which result in reliable and effective OVP operation. However, an understanding of the factors which influence the SCR's di/dt and surge capabilities simplifies this task.

1. di/dt

As the gate region of the SCR is driven on, its area of conduction takes a finite amount of time to grow, starting as a very small region and gradually spreading. Since the anode current flows through this turned-on gate region, very high current densities can occur in the gate region if high anode currents appear quickly (di/dt). This can result in immediate destruction of the SCR or gradual degradation of its forward blocking voltage capabilities — depending on the severity of the occasion.

The value of di/dt that an SCR can safely handle is influenced by its construction and the characteristics of the gate drive signal. A center-gate-fire SCR has more di/dt capability than a corner-gate-fire type, and heavily overdriving (3 to 5 times I_{GT}) the SCR gate with a fast $<1.0\ \mu s$ rise time signal will maximize its di/dt capability. A typical maximum number in phase control SCRs of less than 50 A(RMS) rating might be 200 A/μs, assuming a gate current of five times I_{GT} and $< 1.0\ \mu s$ rise time. If having done this, a di/dt problem is seen to still exist, the designer can also decrease the di/dt of the current waveform by adding inductance in series with the SCR, as shown in Figure 12. Of course, this reduces the circuit's ability to rapidly reduce the dc bus voltage and a tradeoff must be made between speedy voltage reduction and di/dt.

FIGURE 10 — TYPICAL CROWBAR CIRCUIT CONFIGURATIONS

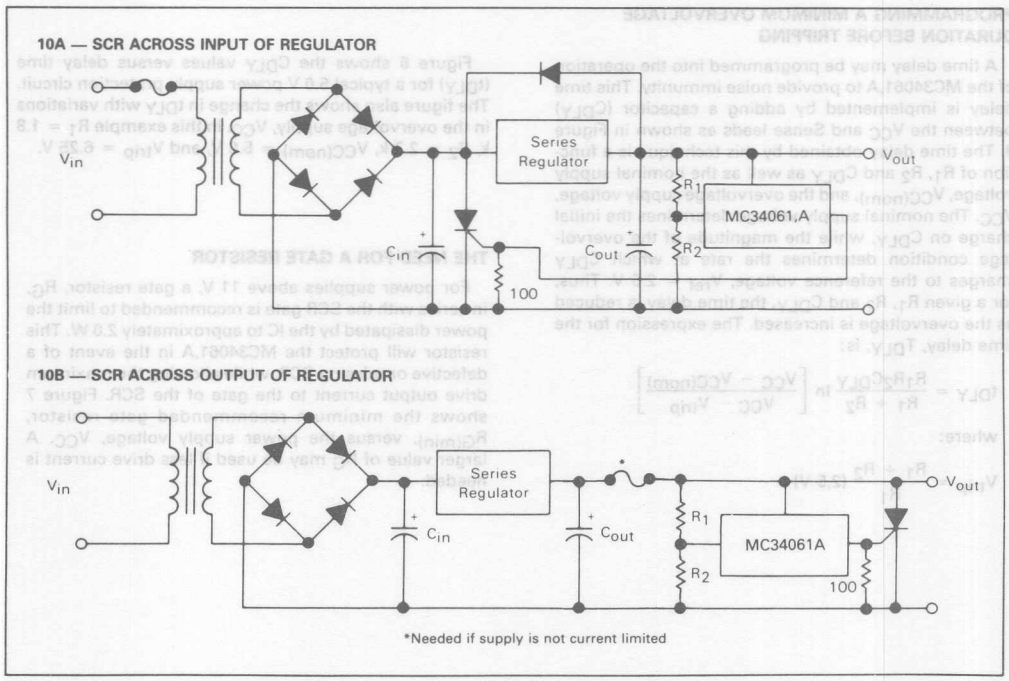
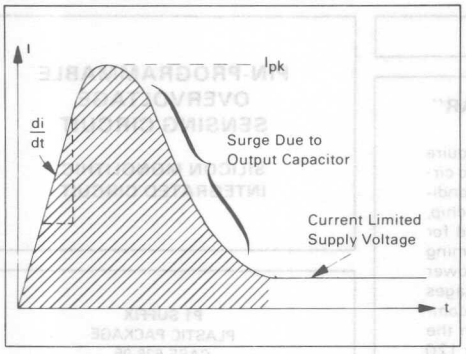


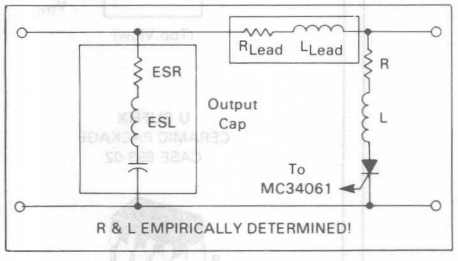
FIGURE 11 — CROWBAR SCR SURGE CURRENT WAVEFORM



2. Surge Current

If the peak current and/or the duration of the surge is excessive, immediate destruction due to device overheating will result. The surge capability of the SCR is directly proportional to its die area. If the surge current cannot be reduced (by adding series resistance — see Figure 12) to a safe level which is consistent with the system's requirements for speedy bus voltage reduction, the designer must use a higher current SCR. This may result in the average current capability of the SCR exceeding the steady state current requirements imposed by the dc power supply.

FIGURE 12 — CIRCUIT ELEMENTS AFFECTING SCR SURGE AND di/dt



A WORD ABOUT FUSING

Before leaving the subject of the crowbar SCR, a few words about fuse protection are in order. Referring back to Figure 10A, it will be seen that a fuse is necessary if the power supply to be protected is not output current limited. This fuse is not meant to prevent SCR failure but rather to prevent a fire!

In order to protect the SCR, the fuse would have to possess an I^2t rating less than that of the SCR and yet have a high enough continuous current rating to survive normal supply output currents. In addition, it must be capable of successfully clearing the high short circuit currents from the supply. Such a fuse as this is quite expensive, and may not even be available.

The usual design compromise then is to use a garden variety fuse (3AG or 3AB style) which cannot be relied on to blow before the thyristor does, and trust that if the SCR does fail, it will fail short circuit. In the majority of the designs, this will be the case, though this is difficult to guarantee. Of course, a sufficiently high surge will cause an open. These comments also apply to the fuse in Figure 10B.

CROWBAR SCR SELECTION GUIDE

As an aid in selecting an SCR for crowbar use, the following selection guide is presented.

DEVICE	I_{RMS}	I_{FSM}	PACKAGE
MCR67 Series	12 A	100 A	Metal Stud
MCR68 Series	12 A	100 A	TO-220 Plastic
2N1842 Series	16 A	125 A	Metal Stud
2N6400 Series	16 A	160 A	TO-220 Plastic
2N6504 Series	25 A	160 A	TO-220 Plastic
2N681 Series	25 A	200 A	Metal Stud
2N2573 Series	25 A	260 A	TO-3 Metal Can
MCR69 Series	25 A	300 A	TO-220 Plastic
MCR70 Series	35 A	350 A	Metal Stud
MCR71 Series	55 A	550 A	Metal Stud

For a complete and detailed treatment of SCR and fuse selection refer to Motorola Application Note AN-789.

MC35062

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Advance Information

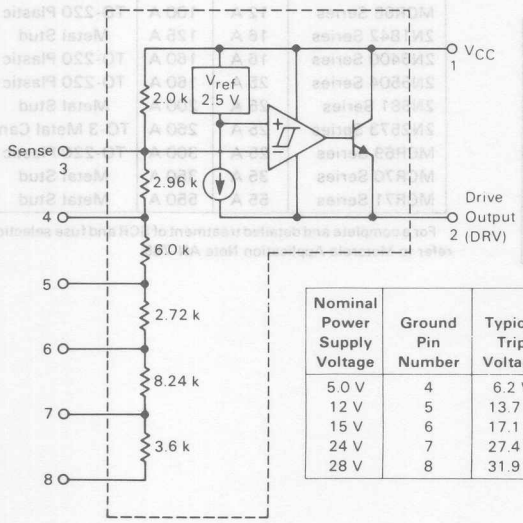
PIN-PROGRAMMABLE OVERVOLTAGE "CROWBAR" SENSING CIRCUIT

The MC34062/35062 overvoltage protection (OVP) circuits require only an external "crowbar" SCR to protect sensitive electronic circuitry from overvoltage damage. They sense an overvoltage condition and quickly "crowbar", or short circuit, the supply. An on-chip, tapped resistor network allows the device to be programmed for trip voltages ranging from 3.5 to 40 V. Each of the five programming pins provides one standard overvoltage trip point for nominal power supply voltages of 5.0, 12, 15, 24 or 28 V. Many other trip voltages may be programmed by interconnecting and grounding various combinations of these programming pins. Tables are provided in the Applications Information which show connection schemes for 120 trip voltages.

These circuits provide a cost-effective means of protecting either positive or negative power supplies. In addition, an external capacitor may be used to program a minimum overvoltage duration before tripping, thus providing noise immunity. The unique design of the MC34062/35062 eliminates voltage and temperature drift errors due to SCR gate variations.

- Unique Pin-Programmable Trip Voltage from 3.5 to 40 V
- One-Pin Programming for 5.0, 12, 15, 24 and 28 V Power Supplies
- SCR Gate Drive Output of 200 mA
- Built-In Hysteresis Voltage
- Wide Supply Range: $4.0\ V \leq V_{CC} \leq 40\ V$

FUNCTIONAL BLOCK DIAGRAM



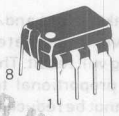
Nominal Power Supply Voltage	Ground Pin Number	Typical Trip Voltage
5.0 V	4	6.2 V
12 V	5	13.7 V
15 V	6	17.1 V
24 V	7	27.4 V
28 V	8	31.9 V

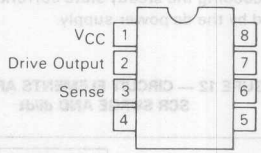
Pins 4 through 8 are used to program the Trip Voltage, V_{trip}

PIN-PROGRAMMABLE OVERVOLTAGE SENSING CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT

P1 SUFFIX
PLASTIC PACKAGE
CASE 626-05
(MC34062 only)

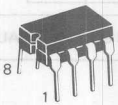




Note: Pins 4 thru 8 are used to program the Trip Voltage, V_{trip}

(Top View)

U SUFFIX
CERAMIC PACKAGE
CASE 693-02



ORDERING INFORMATION

Device	Temperature Range	Package
MC35062U	-55 to +125°C	Ceramic DIP
MC34062P1	0 to +70°C	Plastic DIP
MC34062U		Ceramic DIP

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Operating Voltage	V_{CC} - V_{DRV}	40	Vdc
Voltage Across Any Internal Resistor In Network	V_{RN}	40	Vdc
Current Through Any Resistor In Network	I_{RN}	10	mA
Sense Voltage	V_{Sense}	40	Vdc
Drive Output Current	I_{DRV}	Internally Limited	mA
Operating Ambient Temperature MC34062 MC35062	T_A	 0 to +70 -55 to +125	°C
Operating Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	-65 to +150°C	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V; V_{DRV} = 0 V; T_A = T_{low} to T_{high} unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit
Operating Voltage Range	V_{CC} - V_{DRV}	3.0	—	40	Vdc
Sense Trip Voltage	V_{Sense}				Vdc
T_A = 25°C		2.425	2.5	2.575	
T_{low} to T_{high}		2.375	2.5	2.625	
Line Regulation, V_{Sense} (3.0 V ≤ V_{CC} - V_{DRV} ≤ 40 V)	Reg_{line}				%/V
T_A = 25°C		—	0.001	0.01	
T_{low} to T_{high}		—	0.001	0.02	
Trip Voltage (Pin 4 = Gnd; V_{DRV} = 0 V)	$V_{trip(4)}$				V
T_A = 25°C		6.01	6.2	6.39	
T_{low} to T_{high}		5.89	6.2	6.51	
Hysteresis Voltage (Pin 4 = Gnd; V_{DRV} = 0 V)	$V_{H(4)}$	—	0.62	—	V
Trip Voltage (Pin 5 = Gnd; V_{DRV} = 0 V)	$V_{trip(5)}$				V
T_A = 25°C		13.3	13.7	14.1	
T_{low} to T_{high}		13.0	13.7	14.4	
Hysteresis Voltage (Pin 5 = Gnd; V_{DRV} = 0 V)	$V_{H(5)}$	—	1.37	—	V
Trip Voltage (Pin 6 = Gnd; V_{DRV} = 0 V)	$V_{trip(6)}$				V
T_A = 25°C		16.6	17.1	17.6	
T_{low} to T_{high}		16.2	17.1	18.0	
Hysteresis Voltage (Pin 6 = Gnd; V_{DRV} = 0 V)	$V_{H(6)}$	—	1.71	—	V
Trip Voltage (Pin 7 = Gnd; V_{DRV} = 0 V)	$V_{trip(7)}$				V
T_A = 25°C		26.6	27.4	28.2	
T_{low} to T_{high}		26.0	27.4	28.8	
Hysteresis Voltage (Pin 7 = Gnd; V_{DRV} = 0 V)	$V_{H(7)}$	—	2.74	—	V
Trip Voltage (Pin 8 = Gnd; V_{DRV} = 0 V)	$V_{trip(8)}$				V
T_A = 25°C		30.9	31.9	32.9	
T_{low} to T_{high}		30.3	31.9	33.5	
Hysteresis Voltage (Pin 8 = Gnd; V_{DRV} = 0 V)	$V_{H(8)}$	—	3.19	—	V
Resistor Network Current at Nominal Power Supply Voltage V_{CC} = 28 V; V_{DRV} = 0 V; Pin 8 = Gnd	I_{RN}	0.5	1.1	2.0	mA
Drive Output Current, ON State	$I_{DRV(on)}$				mA
T_J = 25°C		130	200	300	
T_{low} to T_{high}		90	—	350	
Drive Output Current, OFF State	$I_{DRV(off)}$				mA
V_{CC} = 5.0 V; V_{DRV} = 0 V		0.2	0.6	1.0	
3.0 V ≤ V_{CC} - V_{DRV} ≤ 40 V		0.2	0.6	1.5	
Drive Output Current Slew Rate (T_A = 25°C)	di/dt	—	2.0	—	A/μs
Drive Output V_{CC} Transient Rejection V_{CC} = 0 V to 15 V at dV/dt = 200 V/μs; V_{DRV} = 0 V; V_{Sense} = 0 V; T_A = 25°C	$\Delta I_{DRV(trans)}$	—	1.0	—	mA (Peak)
Propagation Delay Time (T_A = 25°C; 500 mV Overdrive)	t_{PLH}	—	500	—	ns

T_{low} = -55°C for MC35062 = 0°C for MC34062 T_{high} = +125°C for MC35062 = + 70°C for MC34062

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FIGURE 1 — STANDARD TEST CIRCUIT

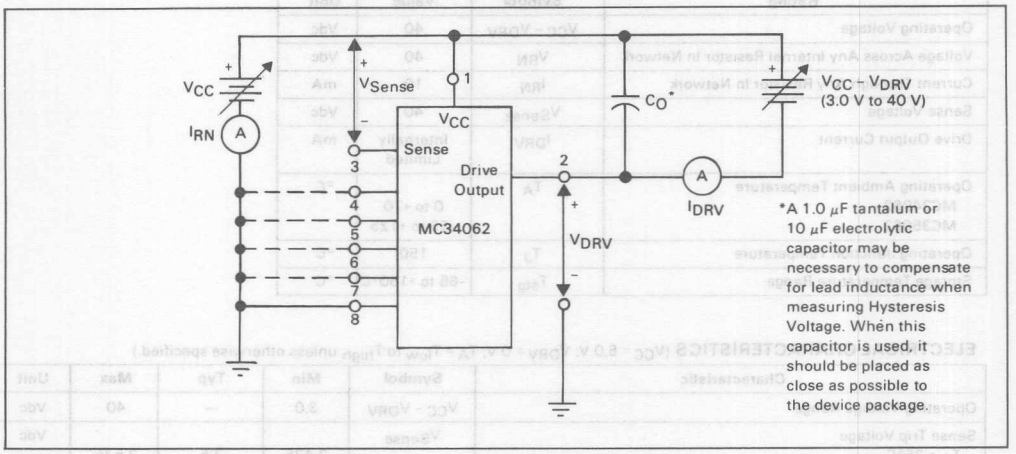


FIGURE 2 — DRIVE CURRENT versus NORMALIZED RESISTOR DIVIDER VOLTAGE
(Normalized to V_{trip} at T_A = 25°C)

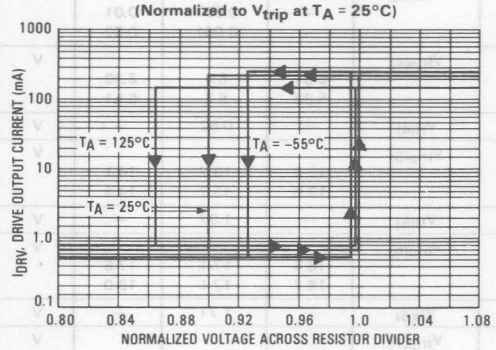


FIGURE 3 — NORMALIZED TRIP VOLTAGE versus TEMPERATURE
(Normalized to T_A = 25°C)

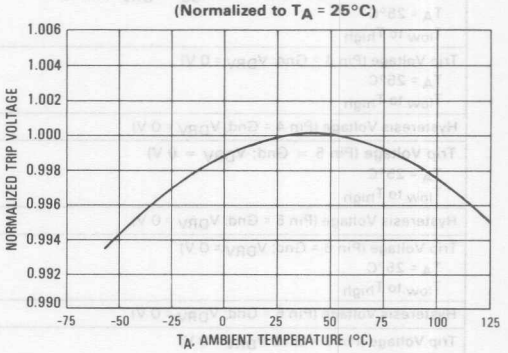


FIGURE 4 — OFF STATE DRIVE CURRENT versus SUPPLY VOLTAGE

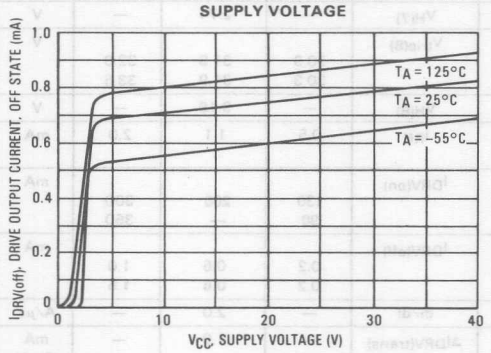


FIGURE 5 — MINIMUM R_G versus SUPPLY VOLTAGE

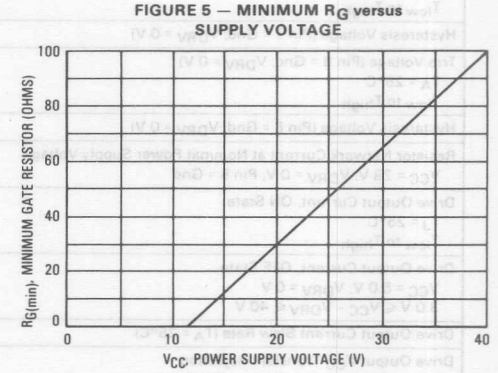


FIGURE 6 — DELAY CAPACITANCE versus DELAY TIME FOR NOMINAL 5.0 V POWER SUPPLY

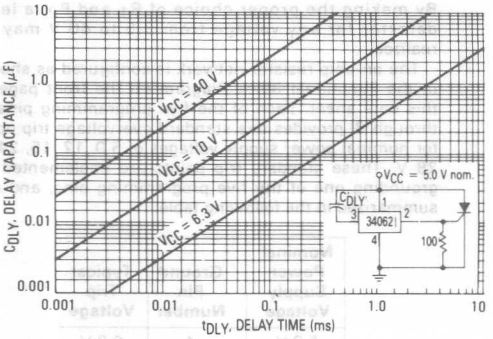


FIGURE 7 — DELAY CAPACITANCE versus DELAY TIME FOR NOMINAL 12 V POWER SUPPLY

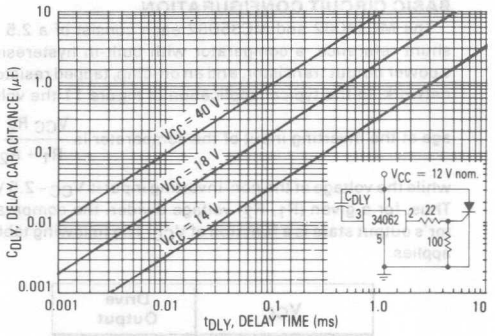


FIGURE 8 — DELAY CAPACITANCE versus DELAY TIME FOR NOMINAL 15 V POWER SUPPLY

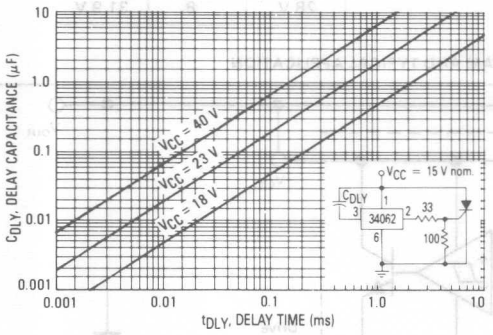


FIGURE 9 — DELAY CAPACITANCE versus DELAY TIME FOR NOMINAL 24 V POWER SUPPLY

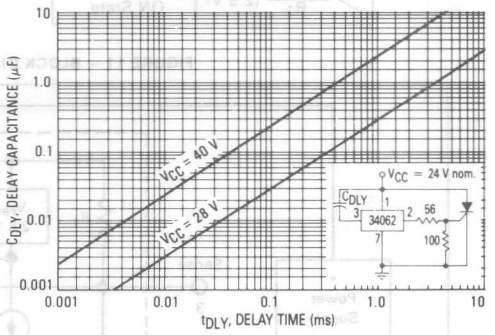
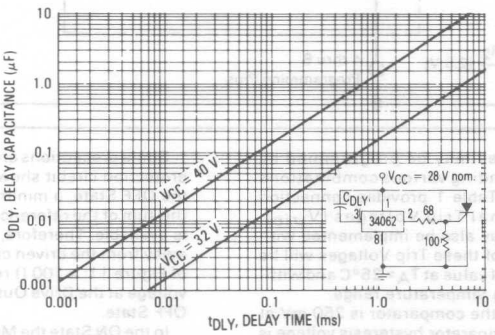


FIGURE 10 — DELAY CAPACITANCE versus DELAY TIME FOR NOMINAL 28 V POWER SUPPLY



APPLICATIONS INFORMATION

BASIC CIRCUIT CONFIGURATION

The MC34062 and MC35062 each consist of a 2.5 V shunt reference, a comparator with built-in hysteresis, a power output transistor, and an on-chip, tapped resistor network. In the typical application of Figure 11 the voltage at the inverting input of the comparator is $\frac{V_{CC}\ R_2}{R_1 + R_2}$, while the voltage at the non-inverting input is V_{CC} - 2.5 V. Thus, for a given (R_1, R_2) voltage divider, the comparator's output state is a function of V_{CC}. The following table applies:

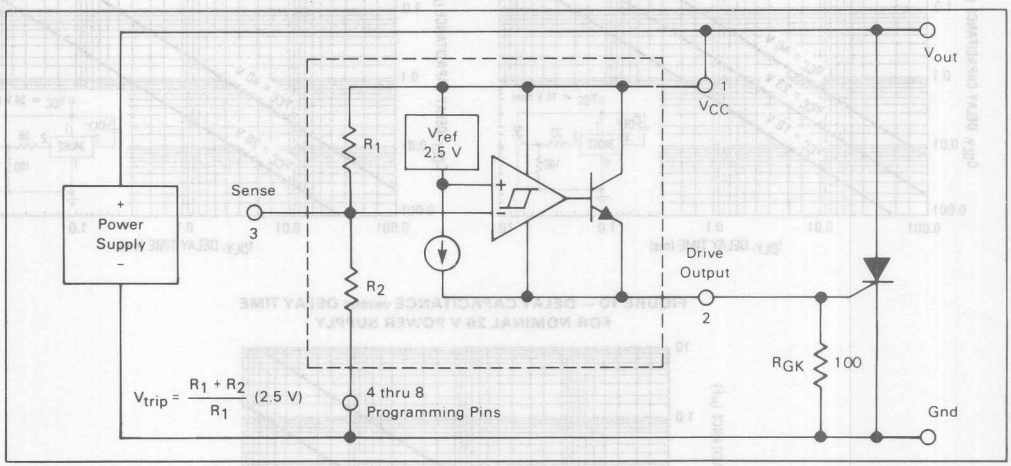
V_{CC}	Drive Output
$< \frac{R_1 + R_2}{R_1}$ (2.5 V)	OFF State
$> \frac{R_1 + R_2}{R_1}$ (2.5 V)	ON State

By making the proper choice of R_1 and R_2, a level detector for any voltage from 3.5 to 40 V may be realized.

The on-chip resistor network is configured as shown in the Functional Block Diagram on the front page of this data sheet. Each of the five programming pins (4 through 8) provides one standard overvoltage trip point for nominal power supply voltages of 5.0, 12, 15, 24 or 28 V. These standard trip points are implemented by grounding one of the five programming pins, and are summarized in the following table.

Nominal Power Supply Voltage	Ground Pin Number	Typical Trip Voltage
5.0 V	4	6.2 V
12 V	5	13.7 V
15 V	6	17.1 V
24 V	7	27.4 V
28 V	8	31.9 V

FIGURE 11 — BLOCK DIAGRAM AND TYPICAL APPLICATION



Many other trip voltages may be programmed by interconnecting and grounding various combinations of the programming pins. Table 1 provides connection schemes for 120 nominal Trip Voltages (V_{trip}). Additional Trip Voltages may also be implemented with other pin connections. All of these Trip Voltages will be within ±3.0% of the nominal value at T_A = 25°C and within ±5.0% over the operating temperature range.

The hysteresis built into the comparator is 250 mV at the inverting input. This comparator hysteresis voltage is multiplied by the ratio $\frac{R_1 + R_2}{R_1}$, just as the 2.5 V Sense Trip Voltage (V_{Sense}) is multiplied by the same ratio to define the Trip Voltage (V_{trip}). Thus, the Hysteresis Voltage (V_H) is approximately 10% of the Trip Voltage for any Trip Voltage.

Some precautions are necessary in the operation of the protection circuit shown in Figure 11. Note that even in the OFF State, a minimum drive output current, equal to the sum of the reference and comparator supply currents, is available. Therefore, a means of shunting this current away from the driven circuit is necessary. In the example of Figure 11, a 100 Ω resistor (R_{GK}) is used, producing a voltage at the Drive Output of approximately 60 mV in the OFF State.

In the ON State the MC34062 becomes a current source capable of saturating to within 2.0 V of V_{CC}. Therefore, when driving a high impedance load, it may be desirable to clamp the drive output to at least 3.0 V below V_{CC} ($V_{CC} - V_{DRV} \geq 3.0$ V) if it is important that the reference continue to regulate.

PROGRAMMING A MINIMUM OVERVOLTAGE DURATION BEFORE TRIPPING

A time delay may be programmed into the operation of the MC34062/35062 to provide noise immunity. This time delay is implemented by adding a capacitor (C_{DLY}) between the V_{CC} and Sense leads as shown in Figure 12. The time delay obtained by this technique is a function of the internal resistors (R_1, R_2) and C_{DLY}, as well as the nominal supply voltage, $V_{CC(nom)}$, and the overvoltaged supply voltage V_{CC}. The nominal supply voltage determines the initial charge on C_{DLY}, while the magnitude of the overvoltage condition determines the rate at which C_{DLY} charges to the reference voltage, V_{ref} = 2.5 V. Thus, for a given R_1, R_2 and C_{DLY}, the time delay is reduced as the overvoltage is increased. The expression for the time delay, t_{DLY} is:

$$t_{DLY} = \frac{R_1 R_2 C_{DLY}}{R_1 + R_2} \ln \left[\frac{V_{CC} - V_{CC(nom)}}{V_{CC} - V_{trip}} \right]$$

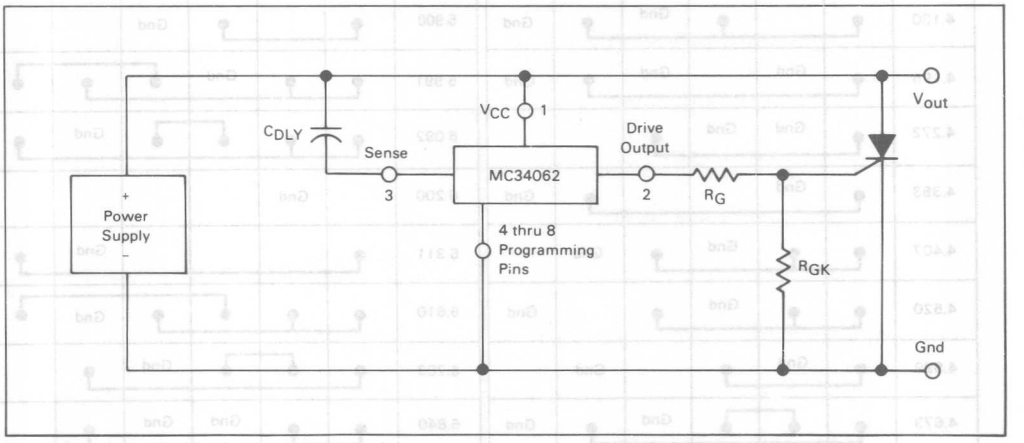
where: $V_{trip} = \frac{R_1 + R_2}{R_1}(2.5\ V)$

Figures 6 through 10 show the C_{DLY} values versus delay time (t_{DLY}) for nominal 5.0, 12, 15, 24 and 28 V power supply protection circuits, each using a one-pin MC34062/35062 programming scheme. These figures also show the change in t_{DLY} with variations in the overvoltaged supply, V_{CC}.

THE NEED FOR A GATE RESISTOR

For power supplies above 11 V, a gate resistor, R_G, in series with the SCR gate is recommended to limit the power dissipated by the IC to approximately 2.0 W. This resistor will protect the MC34062/35062 in the event of a defective or missing SCR, while allowing the maximum drive output current to the gate of the SCR. Figure 5 shows the minimum recommended gate resistor, $R_{G(min)}$, versus the power supply voltage, V_{CC}. A larger value of R_G may be used if less drive current is needed.

FIGURE 12 — OVERVOLTAGE PROTECTION WITH TIME DELAY



3

TABLE 1 — PIN-PROGRAMMING OF RESISTOR NETWORK FOR NOMINAL TRIP VOLTAGES

V_{trip}	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8
3.483		Gnd		Gnd		Gnd
3.632		Gnd	Gnd		Gnd	
3.758		Gnd		Gnd		
3.807		Gnd		Gnd		
3.883		Gnd			Gnd	
3.923			Gnd		Gnd	
4.012		Gnd	Gnd		Gnd	
4.098		Gnd				Gnd
4.130				Gnd		Gnd
4.196		Gnd		Gnd		Gnd
4.272		Gnd	Gnd			
4.353		Gnd				Gnd
4.407			Gnd		Gnd	
4.520			Gnd			Gnd
4.598		Gnd			Gnd	
4.673				Gnd		Gnd
4.709			Gnd	Gnd		Gnd
4.845		Gnd		Gnd		
4.947			Gnd	Gnd		Gnd
4.996			Gnd		Gnd	

V_{trip}	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8
5.101			Gnd			Gnd
5.222		Gnd		Gnd		
5.328		Gnd				
5.413		Gnd	Gnd			
5.563		Gnd				
5.673		Gnd				
5.734		Gnd				
5.887					Gnd	
5.900				Gnd		
5.991			Gnd			
6.092					Gnd	
6.200		Gnd				
6.311					Gnd	
6.610					Gnd	
6.703				Gnd		
6.840			Gnd	Gnd		
7.000						Gnd
7.132			Gnd			
7.298				Gnd		
7.347			Gnd			

TABLE 1 — (Continued)

V_{trip}	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8
7.478			Gnd	Gnd		
7.799			Gnd			
8.106			Gnd		Gnd	
8.220			Gnd			Gnd
8.409			Gnd	Gnd		Gnd
8.539			Gnd			
8.633				Gnd		Gnd
8.756				Gnd		
8.870			Gnd	Gnd		
8.906						Gnd
9.013			Gnd		Gnd	
9.178						Gnd
9.331		V_{CC}		Gnd		
9.377			Gnd			
9.385				Gnd	Gnd	
9.433			Gnd			
9.600				Gnd		
9.826				Gnd		
9.912					Gnd	
10.000			Gnd			

V_{trip}	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8
10.400						Gnd
10.540			Gnd	Gnd		
10.700						Gnd
11.047			Gnd			
11.178			Gnd	Gnd		
11.496				Gnd		
11.630				Gnd		Gnd
11.895				Gnd		V_{CC}
11.937				Gnd	Gnd	
12.086			Gnd			V_{CC}
12.477				Gnd		
12.556				Gnd		
12.732					Gnd	
12.800					Gnd	
13.387					Gnd	
13.400				Gnd		
13.700			Gnd			
14.233					Gnd	
14.500						Gnd
15.330				Gnd		Gnd

TABLE 1 — (Continued)

V_{trip}	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8
15.637				Gnd	Gnd	
16.200					Gnd	
16.256				Gnd		
16.465				Gnd		
16.500					Gnd	
16.532					Gnd	
16.832					Gnd	
17.087					Gnd	
17.100				Gnd		
17.300						Gnd
17.900						Gnd
18.200						Gnd
18.733						Gnd
19.900					Gnd	
20.232					Gnd	
20.300					Gnd	
20.700						Gnd
21.000						Gnd
21.600						Gnd
22.122		V_{CC}			Gnd	

V_{trip}	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8
22.673			V_{CC}		Gnd	
23.700					Gnd	
23.807			V_{CC}		Gnd	
24.000					Gnd	
24.283			V_{CC}			Gnd
24.400						Gnd
24.800						Gnd
25.211				Gnd	V_{CC}	
27.333		V_{CC}	V_{CC}		Gnd	
27.400					Gnd	
28.200						Gnd
28.500						Gnd
30.023		V_{CC}			Gnd	
30.694		V_{CC}				Gnd
31.486			V_{CC}			Gnd
31.900						Gnd
32.233		V_{CC}				Gnd
33.116			V_{CC}			Gnd
38.182		V_{CC}	V_{CC}			Gnd
39.064		V_{CC}				Gnd

CROWBAR SCR CONSIDERATIONS

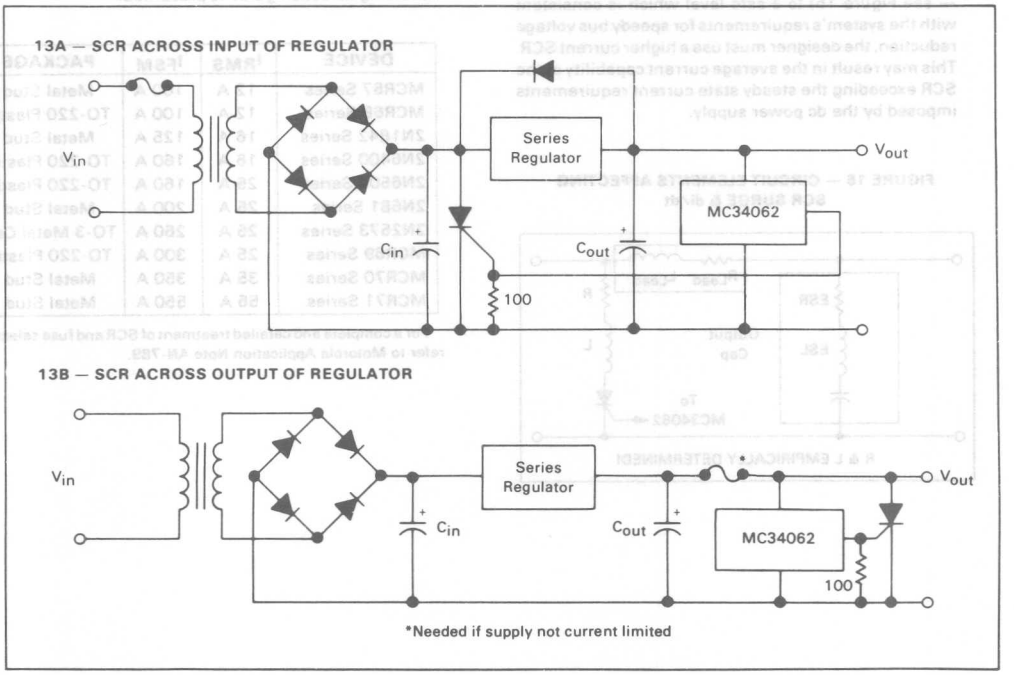
Referring to Figure 13, it can be seen that the crowbar SCR, when activated, is subject to a large current surge from the output capacitance, C_{out}. This capacitance consists of the power supply output capacitors, the load's decoupling capacitors, and in the case of Figure 13A, the supply's input filter capacitors. This surge current is illustrated in Figure 14, and can cause SCR failure or degradation by any one of three mechanisms: di/dt, absolute peak surge, or I^2t. The interrelationship of these failure methods and the breadth of the applications make specification of the SCR by the semiconductor manufacturer difficult and expensive. Therefore, the designer must empirically determine the SCR and circuit elements which result in reliable and effective OVP operation. However, an understanding of the factors which influence the SCR's di/dt and surge capabilities simplifies this task.

1. di/dt

As the gate region of the SCR is driven on, its area of conduction takes a finite amount of time to grow, starting as a very small region and gradually spreading. Since the anode current flows through this turned-on gate region, very high current densities can occur in the gate region if high anode currents appear quickly (di/dt). This can result in immediate destruction of the SCR or gradual degradation of its forward blocking voltage capabilities — depending on the severity of the occasion.

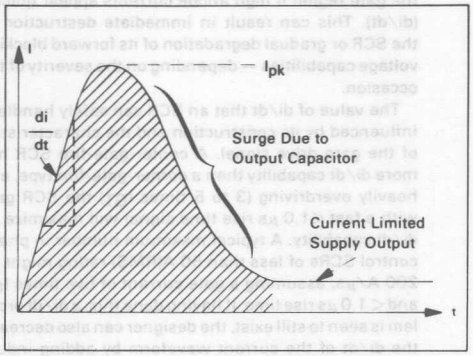
The value of di/dt that an SCR can safely handle is influenced by its construction and the characteristics of the gate drive signal. A center-gate-fire SCR has more di/dt capability than a corner-gate-fire type, and heavily overdriving (3 to 5 times I_{GT}) the SCR gate with a fast $<1.0\ \mu s$ rise time signal will maximize its di/dt capability. A typical maximum number in phase control SCRs of less than 50 A(RMS) rating might be 200 $A/\mu s$, assuming a gate current of five times I_{GT} and $< 1.0\ \mu s$ rise time. If having done this, a di/dt problem is seen to still exist, the designer can also decrease the di/dt of the current waveform by adding inductance in series with the SCR, as shown in Figure 15. Of course, this reduces the circuit's ability to rapidly reduce the dc bus voltage and a tradeoff must be made between speedy voltage reduction and di/dt.

FIGURE 13 — TYPICAL CROWBAR CIRCUIT CONFIGURATIONS



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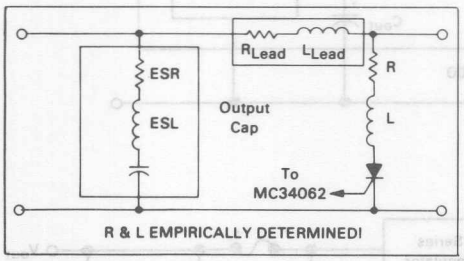
FIGURE 14 — CROWBAR SCR SURGE CURRENT WAVEFORM



2. Surge Current

If the peak current and/or the duration of the surge is excessive, immediate destruction due to device overheating will result. The surge capability of the SCR is directly proportional to its die area. If the surge current cannot be reduced (by adding series resistance — see Figure 15) to a safe level which is consistent with the system's requirements for speedy bus voltage reduction, the designer must use a higher current SCR. This may result in the average current capability of the SCR exceeding the steady state current requirements imposed by the dc power supply.

FIGURE 15 — CIRCUIT ELEMENTS AFFECTING SCR SURGE & di/dt



A WORD ABOUT FUSING

Before leaving the subject of the crowbar SCR, a few words about fuse protection are in order. Referring back to Figure 13A, it will be seen that a fuse is necessary if the power supply to be protected is not output current limited. This fuse is not meant to prevent SCR failure but rather to prevent a fire!

In order to protect the SCR, the fuse would have to possess an I^2t rating less than that of the SCR and yet have a high enough continuous current rating to survive normal supply output currents. In addition, it must be capable of successfully clearing the high short circuit currents from the supply. Such a fuse as this is quite expensive, and may not even be available.

The usual design compromise then is to use a garden variety fuse (3AG or 3AB style) which cannot be relied on to blow before the thyristor does, and trust that if the SCR does fail, it will fail short circuit. In the majority of the designs, this will be the case, though this is difficult to guarantee. Of course, a sufficiently high surge will cause an open. These comments also apply to the fuse in Figure 13B.

CROWBAR SCR SELECTION GUIDE

As an aid in selecting an SCR for crowbar use, the following selection guide is presented.

DEVICE	I_{RMS}	I_{FSM}	PACKAGE
MCR67 Series	12 A	100 A	Metal Stud
MCR68 Series	12 A	100 A	TO-220 Plastic
2N1842 Series	16 A	125 A	Metal Stud
2N6400 Series	16 A	160 A	TO-220 Plastic
2N6504 Series	25 A	160 A	TO-220 Plastic
2N681 Series	25 A	200 A	Metal Stud
2N2573 Series	25 A	260 A	TO-3 Metal Can
MCR69 Series	25 A	300 A	TO-220 Plastic
MCR70 Series	35 A	350 A	Metal Stud
MCR71 Series	55 A	550 A	Metal Stud

For a complete and detailed treatment of SCR and fuse selection refer to Motorola Application Note AN-789.

MOTOROLA

MC34063
MC35063
MC33063

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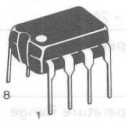
DC TO DC CONVERTER CONTROL CIRCUITS

The MC34063 Series is a monolithic control circuit containing the primary functions required for dc-to-dc converters. The device consists of an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active current limit circuit, driver and high current output switch. This series was specifically designed to be incorporated in Step-Down and Step-Up and Voltage-Inverting applications with a minimum number of external components.

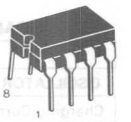
- Operation from 2.5 V to 40 V Input
- Low Standby Current
- Current Limiting
- Output Switch Current of 1.5 A
- Output Voltage Adjustable from 1.25 to 40 V
- Frequency of Operation to 100 kHz

DC TO DC CONVERTER CONTROL CIRCUITS

SILICON MONOLITHIC INTEGRATED CIRCUITS

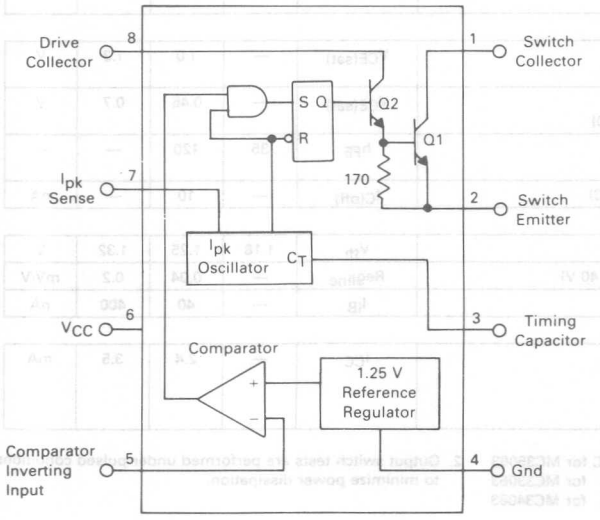


P1 SUFFIX
PLASTIC PACKAGE
CASE 626-05

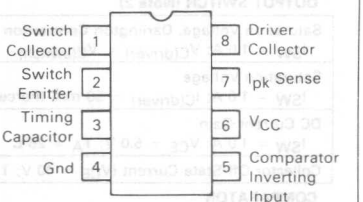


U SUFFIX
CERAMIC PACKAGE
CASE 693-02

FUNCTIONAL BLOCK DIAGRAM



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC35063U	−55 to +125°C	Ceramic DIP
MC33063U	−40 to +85°C	Ceramic DIP
MC33063P1		Plastic DIP
MC34063U	0 to +70°C	Ceramic DIP
MC34063P1		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	Vdc
Comparator Input Voltage Range	V_{IR}	−0.3 to +40	Vdc
Switch Collector Voltage	$V_{C(switch)}$	40	Vdc
Switch Emitter Voltage	$V_{E(switch)}$	40	Vdc
Switch Collector to Emitter Voltage	$V_{CE(switch)}$	40	Vdc
Driver Collector Voltage	$V_{C(driver)}$	40	Vdc
Switch Current	I_{SW}	1.5	Amps
Power Dissipation and Thermal Characteristics Ceramic Package T_A = +25°C Derate above T_A = +25°C Plastic Package T_A = +25°C Derate above T_A = +25°C	 P_D $1/\theta JA$ P_D $1/\theta JA$	 1.25 10 1.0 10	 W mW/°C W mW/°C
Operating Junction Temperature Ceramic Package Plastic Package	T_J	 +150 +125	°C
Operating Ambient Temperature Range MC35063 MC33063 MC34063	T_A	 −55 to +125 −40 to +85 0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V; T_A = T_{low} to T_{high} [Note 1] unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Charging Current (5.0 V ≤ V_{CC} ≤ 40 V, T_A = 25°C)	I_{chg}	20	35	50	μA
Discharge current (5.0 V ≤ V_{CC} ≤ 40 V; T_A = 25°C)	I_{dischg}	150	200	250	μA
Voltage Swing (T_A = 25°C)	V_{osc}	—	0.5	—	V_{p-p}
Discharge to Charge Current Ratio ($I_{pk(sense)}$ = V_{CC}, T_A = 25°C)	I_{dischg}/I_{chg}	—	6.0	—	—
Current Limit Sense Voltage I_{chg} = I_{dischg}, T_A = 25°C	$V_{Ipk(sense)}$	250	300	350	mV
OUTPUT SWITCH (Note 2)					
Saturation Voltage, Darlington Connection I_{SW} = 1.0 A; $V_{C(driver)}$ = $V_{C(switch)}$	$V_{CE(sat)}$	—	1.0	1.3	V
Saturation Voltage I_{SW} = 1.0 A; $I_{C(driver)}$ = 50 mA, (Forced B ≈ 20)	$V_{CE(sat)}$	—	0.45	0.7	V
DC Current Gain I_{SW} = 1.0 A; V_{CE} = 5.0 V; T_A = 25°C	h_{FE}	35	120	—	—
Collector Off-State Current (V_{CE} = 40 V; T_A = 25°C)	$I_{C(off)}$	—	10	—	nA
COMPARATOR					
Threshold Voltage	V_{th}	1.18	1.25	1.32	V
Threshold Voltage Line Regulation (3.0 V ≤ V_{CC} ≤ 40 V)	Reg_{line}	—	0.04	0.2	mV/V
Input Bias Current (V_{in} = 0 V)	I_{IB}	—	40	400	nA
TOTAL DEVICE					
Supply Current 5.0 V ≤ V_{CC} ≤ 40 V, C_T = 0.001 μF $I_{pk(sense)}$ = V_{CC}, V pin 5 > V_{th}, Pin 2 = Gnd, Remaining pins open	I_{CC}	—	2.4	3.5	mA

NOTES:

1. T_{low} = −55°C for MC35063, −40°C for MC33063, 0°C for MC34063; T_{high} = +125°C for MC35063, +85°C for MC33063, +70°C for MC34063
2. Output switch tests are performed under pulsed conditions to minimize power dissipation.

FIGURE 1 — OUTPUT SWITCH ON-OFF TIME versus OSCILLATOR TIMING CAPACITOR

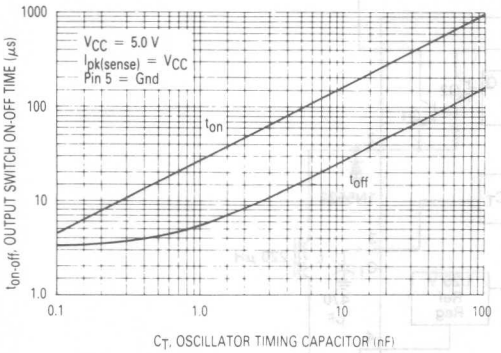


FIGURE 2 — STANDBY SUPPLY CURRENT versus SUPPLY VOLTAGE

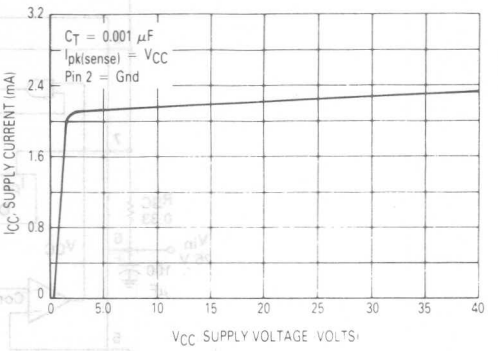


FIGURE 3 — EMITTER-FOLLOWER CONFIGURATION OUTPUT SWITCH SATURATION VOLTAGE versus EMITTER CURRENT

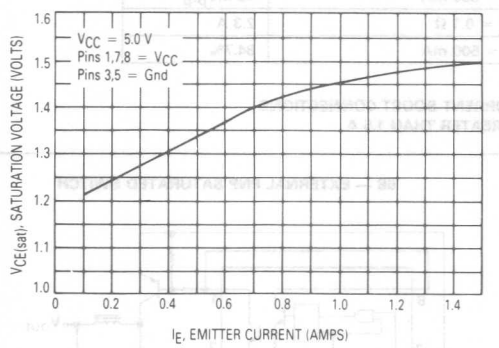
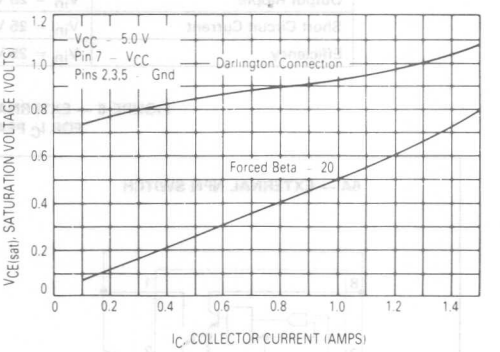
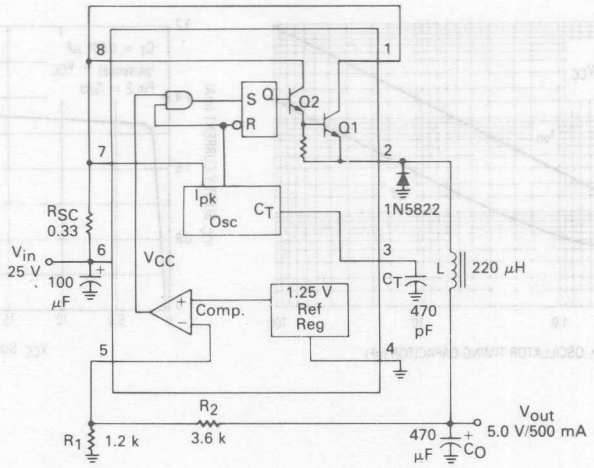


FIGURE 4 — COMMON-EMITTER CONFIGURATION OUTPUT SWITCH SATURATION VOLTAGE versus COLLECTOR CURRENT



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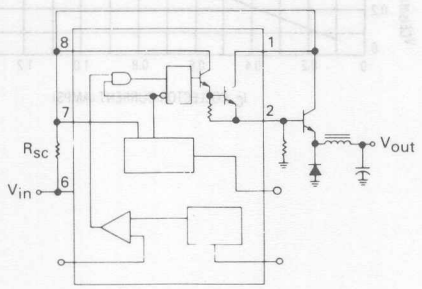
FIGURE 5 — STEP-DOWN CONVERTER



Test	Conditions	Results
Line Regulation	V_{in} = 15 to 25 V, I_o = 500 mA	15 mV
Load Regulation	V_{in} = 25 V, I_o = 50 to 500 mA	5.0 mV
Output Ripple	V_{in} = 25 V, I_o = 500 mA	40 mV_{p-p}
Short Circuit Current	V_{in} = 25 V, R_L = 0.1 Ω	2.3 A
Efficiency	V_{in} = 25 V, I_o = 500 mA	84.7%

FIGURE 6 — EXTERNAL CURRENT BOOST CONNECTIONS FOR I_C PEAK GREATER THAN 1.5 A

6A — EXTERNAL NPN SWITCH



6B — EXTERNAL PNP SATURATED SWITCH

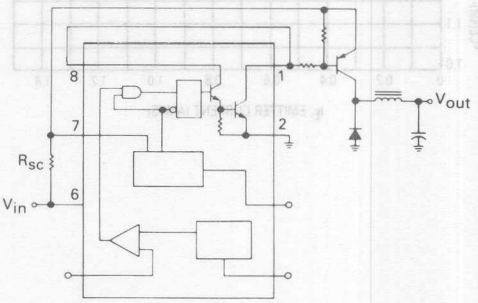
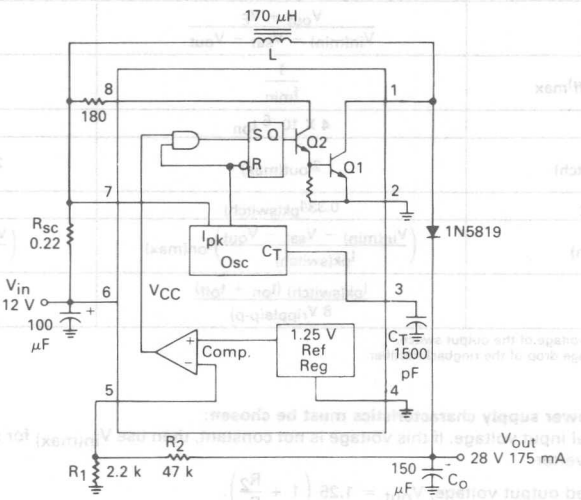


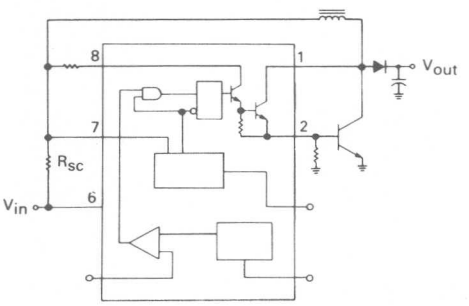
FIGURE 7 — STEP-UP CONVERTER



Test	Conditions	Results
Line Regulation	V_{in} = 8.0 to 16 V, I_O = 175 mA	12 mV
Load Regulation	V_{in} = 12 V, I_O = 75 to 175 mA	45 mV
Output Ripple	V_{in} = 12 V, I_O = 175 mA	150 mV_{p-p}
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	2.0 A
Efficiency	V_{in} = 12 V, I_O = 175 mA	93%

FIGURE 8 — EXTERNAL CURRENT BOOST CONNECTIONS FOR I_C PEAK GREATER THAN 1.5 A

8A — EXTERNAL NPN SWITCH



8B — EXTERNAL NPN SATURATED SWITCH

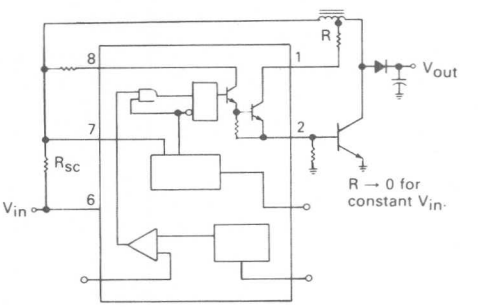


FIGURE 9 — DESIGN FORMULA TABLE

Calculation	Step-Down	Step-Up
$\frac{t_{on}}{t_{off}}$	$\frac{V_{out} + V_F}{V_{in(min)} - V_{sat} - V_{out}}$	$\frac{V_{out} + V_F - V_{in(min)}}{V_{in(min)} - V_{sat}}$
$(t_{on} + t_{off})_{max}$	$\frac{1}{f_{min}}$	$\frac{1}{f_{min}}$
C_T	$4 \times 10^{-5}\, t_{on}$	$4 \times 10^{-5}\, t_{on}$
$I_{pk(switch)}$	$2I_{out(max)}$	$2I_{out(max)} \left(\frac{t_{on} + t_{off}}{t_{off}}\right)$
R_{SC}	$0.33/I_{pk(switch)}$	$0.33/I_{pk(switch)}$
$L_{(min)}$	$\left(\frac{V_{in(min)} - V_{sat} - V_{out}}{I_{pk(switch)}}\right) t_{on(max)}$	$\left(\frac{V_{in(min)} - V_{sat}}{I_{pk(switch)}}\right) t_{on(max)}$
C_o	$\frac{I_{pk(switch)}\,(t_{on} + t_{off})}{8\,V_{ripple(p\text{-}p)}}$	$\approx \frac{I_{out}\, t_{on}}{V_{ripple}}$

V_{sat} = Saturation voltage of the output switch.
V_F = Forward voltage drop of the ringback rectifier

The following power supply characteristics must be chosen:

V_{in} — Nominal input voltage. If this voltage is not constant, then use $V_{in(max)}$ for step-down and $V_{in(min)}$ for step-up converter.

V_{out} — Desired output voltage, $V_{out} = 1.25 \left(1 + \frac{R_2}{R_1}\right)$.

I_{out} — Desired output current.

f_{min} — Minimum desired output switching frequency at the selected values for V_{in} and I_o.

$V_{ripple(p\text{-}p)}$ — Desired peak-to-peak output ripple voltage. In practice, the calculated value will need to be increased due to the capacitor's equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly effect the line and load regulation.

Note:
For further information refer to application note AN920A.

MOTOROLA

MC34063A
MC35063A
MC33063A

3

Advance Information

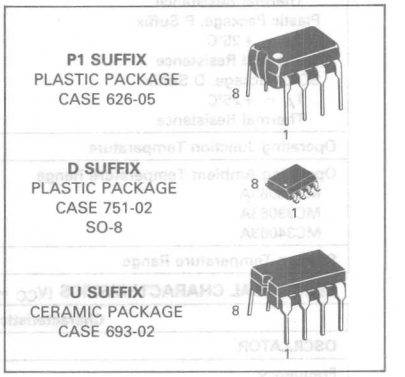
DC-TO-DC CONVERTER CONTROL CIRCUITS

The MC34063A Series is a monolithic control circuit containing the primary functions required for DC-to-DC converters. These devices consist of an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active current limit circuit, driver and high current output switch. This series was specifically designed to be incorporated in Step-Down and Step-Up and Voltage-Inverting applications with a minimum number of external components. Refer to Application Notes AN920A and AN954 for additional design information.

- Operation from 3.0 V to 40 V Input
- Low Standby Current
- Current Limiting
- Output Switch Current to 1.5 A
- Output Voltage Adjustable
- Frequency Operation to 100 kHz
- Precision 2% Reference

DC-TO-DC CONVERTER CONTROL CIRCUITS

SILICON MONOLITHIC INTEGRATED CIRCUITS

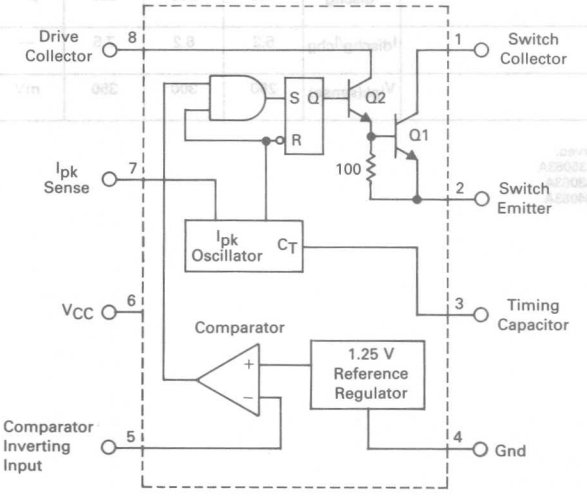


P1 SUFFIX
PLASTIC PACKAGE
CASE 626-05

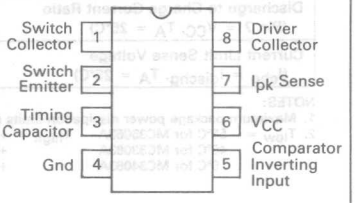
D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SO-8

U SUFFIX
CERAMIC PACKAGE
CASE 693-02

FUNCTIONAL BLOCK DIAGRAM



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC35063AU	−55 to +125°C	Ceramic DIP
MC33063AD	−40 to +85°C	Plastic SOIC
MC33063AP1		Plastic DIP
MC34063AD	0 to +70°C	Plastic SOIC
MC34063AP1		Plastic DIP

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	Vdc
Comparator Input Voltage Range	V_{IR}	−0.3 to +40	Vdc
Switch Collector Voltage	$V_{C(switch)}$	40	Vdc
Switch Emitter Voltage ($V_{Pin\ 1}$ = 40 V)	$V_{E(switch)}$	40	Vdc
Switch Collector to Emitter Voltage	$V_{CE(switch)}$	40	Vdc
Driver Collector Voltage	$V_{C(driver)}$	40	Vdc
Driver Collector Current (Note 1)	$I_{C(driver)}$	100	mA
Switch Current	I_{SW}	1.5	Amps
Power Dissipation and Thermal Characteristics			
Ceramic Package, U Suffix			
T_A = +25°C	P_D	1.25	W
Thermal Resistance	$R_{\theta JA}$	100	°C/W
Plastic Package, P Suffix			
T_A = +25°C	P_D	1.25	W
Thermal Resistance	$R_{\theta JA}$	100	°C/W
SOIC Package, D Suffix			
T_A = +25°C	P_D	625	mW
Thermal Resistance	$R_{\theta JA}$	160	°C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature Range	T_A		°C
MC35063A		−55 to +125	
MC33063A		−40 to +85	
MC34063A		0 to +70	
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V; T_A = T_{low} to T_{high} [Note 2] unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Units
OSCILLATOR					
Frequency ($V_{Pin\ 5}$ = 0 V, C_T = 1.0 nF, T_A = 25°C)	f_{OSC}	24	33	42	kHz
Charge Current (V_{CC} = 5.0 V to 40 V, T_A = 25°C)	I_{chg}	24	33	42	μA
Discharge Current (V_{CC} = 5.0 V to 40 V, T_A = 25°C)	I_{dischg}	140	200	260	μA
Discharge to Charge Current Ratio (Pin 7 = V_{CC}, T_A = 25°C)	I_{dischg}/I_{chg}	5.2	6.2	7.5	—
Current Limit Sense Voltage (I_{chg} = I_{dischg}, T_A = 25°C)	$V_{ipk(sense)}$	250	300	350	mV

NOTES:
1. Maximum package power dissipation limits must be observed.
2. T_{low} = −55°C for MC35063A, −40°C for MC33063A, 0°C for MC34063A; T_{high} = +125°C for MC35063A, +85°C for MC33063A, +70°C for MC34063A

ELECTRICAL CHARACTERISTICS — continued (V_{CC} = 5.0 V; T_A = T_{low} to T_{high} unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Units
OUTPUT SWITCH (Note 3)					
Saturation Voltage, Darlington Connection (I_{SW} = 1.0 A, Pins 1, 8 connected)	$V_{CE(sat)}$	—	1.0	1.3	V
Saturation Voltage (I_{SW} = 1.0 A, $R_{Pin\ 8}$ = 82 Ω to V_{CC}, Forced β ≈ 20)	$V_{CE(sat)}$	—	0.45	0.7	V
DC Current Gain (I_{SW} = 1.0 A, V_{CE} = 5.0 V, T_A = 25°C)	h_{FE}	50	120	—	—
Collector Off-State Current (V_{CE} = 40 V)	$I_{C(off)}$	—	0.01	100	μA
COMPARATOR					
Threshold Voltage (T_A = 25°C) (T_A = T_{low} to T_{high})	V_{th}	 1.225 1.21	 1.25 —	 1.275 1.29	V
Threshold Voltage Line Regulation (V_{CC} = 3.0 V to 40 V)	Reg_{line}	—	1.4	5.0	mV
Input Bias Current (V_{in} = 0 V)	I_{IB}	—	−40	−400	nA
TOTAL DEVICE					
Supply Current (V_{CC} = 5.0 V to 40 V, C_T = 1.0 nF, Pin 7 = V_{CC}, $V_{Pin\ 5}$ > V_{th}, Pin 2 = Gnd, Remaining pins open)	I_{CC}	—	2.5	4.0	mA
TOTAL DEVICE					
Supply Current (V_{CC} = 5.0 V to 40 V, C_T = 1.0 nF, Pin 7 = V_{CC}, $V_{Pin\ 5}$ > V_{th}, Pin 2 = Gnd, Remaining pins open)	I_{CC}	—	2.5	4.0	mA

NOTES:
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.
4. If the output switch is driven into hard saturation (non-Darlington configuration) at low switch currents (≤300 mA) and high driver currents (≥30 mA), it may take up to (2.0 μs) to come out of saturation. This condition will shorten the "off" time at frequencies ≥ 30 kHz, and is magnified at high temperatures. This condition does not occur with a Darlington configuration, since the output switch cannot saturate. If a non-Darlington configuration is used, the following output drive condition is recommended:

Forced β of output switch = I_C, output/(I_C, driver − 7.0 mA*) ≥ 10

*The 100 Ω resistor in the emitter of the driver device requires about 7.0 mA before the output switch conducts.

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FIGURE 1 — OUTPUT SWITCH ON-OFF TIME versus OSCILLATOR TIMING CAPACITOR

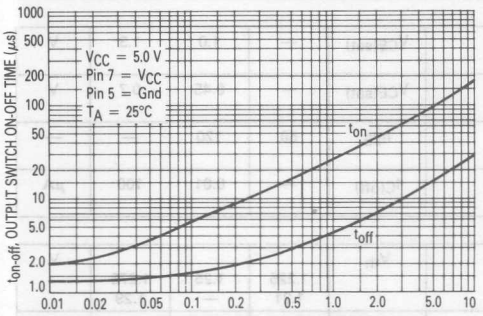


FIGURE 2 — TIMING CAPACITOR WAVEFORM

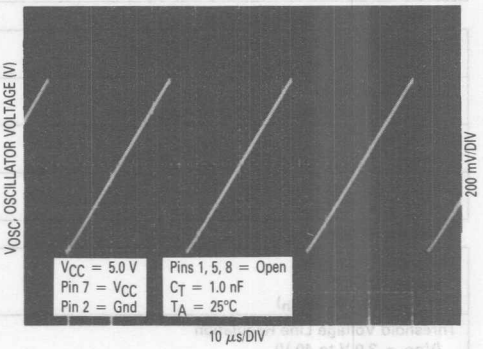


FIGURE 3 — EMITTER FOLLOWER CONFIGURATION OUTPUT SATURATION VOLTAGE versus EMITTER CURRENT

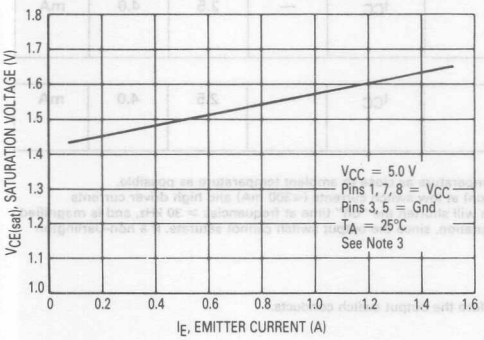


FIGURE 4 — COMMON EMITTER CONFIGURATION OUTPUT SWITCH SATURATION VOLTAGE versus COLLECTOR CURRENT

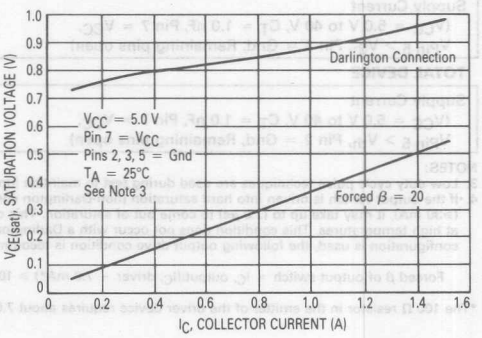


FIGURE 5 — CURRENT LIMIT SENSE VOLTAGE versus TEMPERATURE

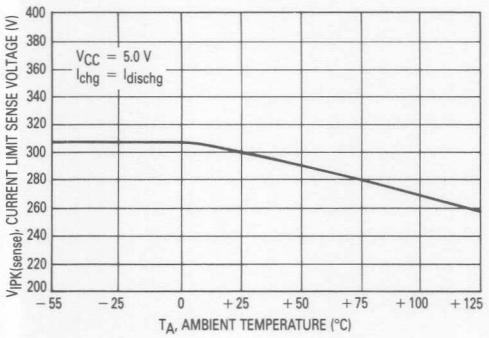


FIGURE 6 — STANDBY SUPPLY CURRENT versus SUPPLY VOLTAGE

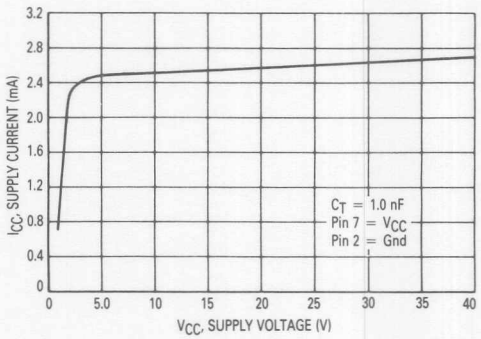
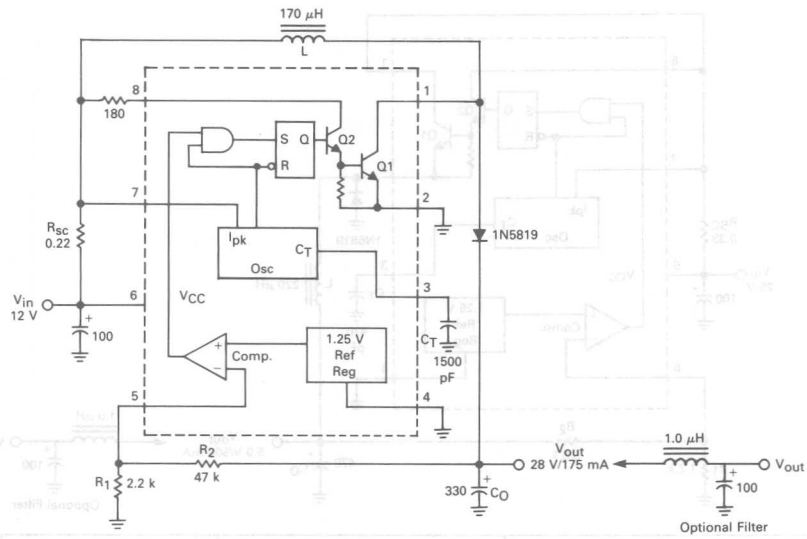


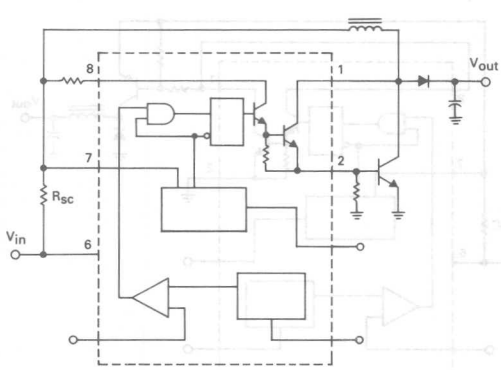
FIGURE 7 — STEP-UP CONVERTER



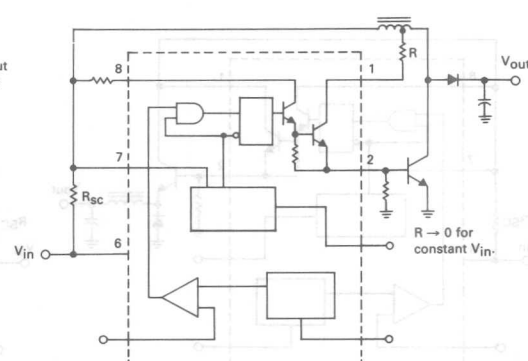
Test	Conditions	Results
Line Regulation	V_{in} = 8.0 V to 16 V, I_O = 175 mA	30 mV = ±0.05%
Load Regulation	V_{in} = 12 V, I_O = 75 to 175 mA	10 mV = ±0.017%
Output Ripple	V_{in} = 12 V, I_O = 175 mA	400 mVp-p
Efficiency	V_{in} = 12 V, I_O = 175 mA	89.2%
Output Ripple With Optional Filter	V_{in} = 12 V, I_O = 175 mA	40 mVp-p

FIGURE 8 — EXTERNAL CURRENT BOOST CONNECTIONS FOR I_C PEAK GREATER THAN 1.5 A

8A — EXTERNAL NPN SWITCH

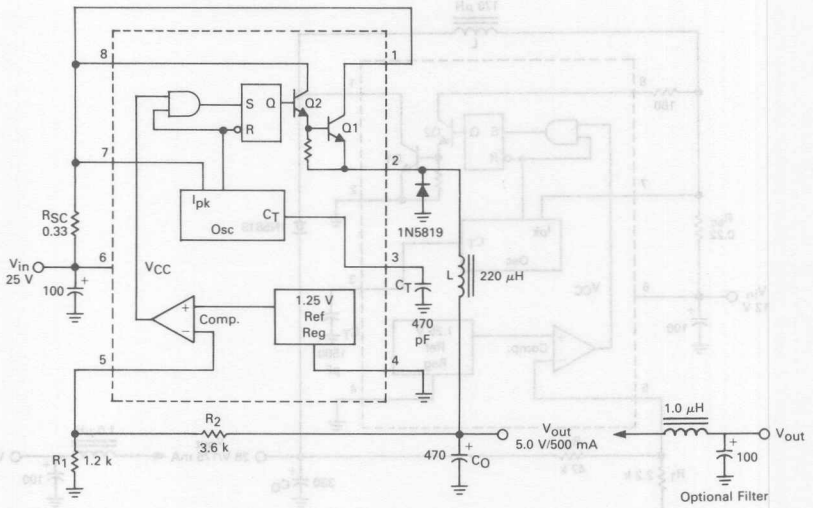


8B — EXTERNAL NPN SATURATED SWITCH (REFER TO NOTE 4)



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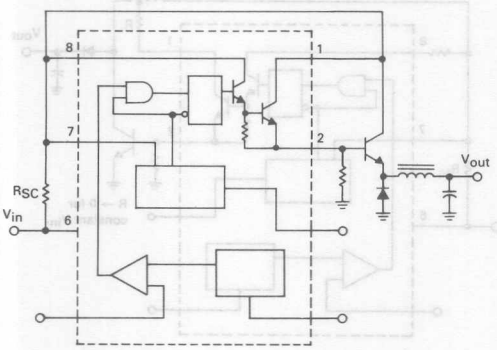
FIGURE 9 — STEP-DOWN CONVERTER



Test	Conditions	Results
Line Regulation	V_{in} = 15 V to 25 V, I_O = 500 mA	12 mV = ±0.12%
Load Regulation	V_{in} = 25 V, I_O = 50 to 500 mA	3.0 mV = ±0.03%
Output Ripple	V_{in} = 25 V, I_O = 500 mA	120 mVp-p
Short Circuit Current	V_{in} = 25 V, R_L = 0.1 Ω	1.1 A
Efficiency	V_{in} = 25 V, I_O = 500 mA	82.5%
Output Ripple With Optional Filter	V_{in} = 25 V, I_O = 500 mA	40 mVp-p

FIGURE 10 — EXTERNAL CURRENT BOOST CONNECTIONS FOR I_C PEAK GREATER THAN 1.5 A

10A — EXTERNAL NPN SWITCH



10B — EXTERNAL PNP SATURATED SWITCH

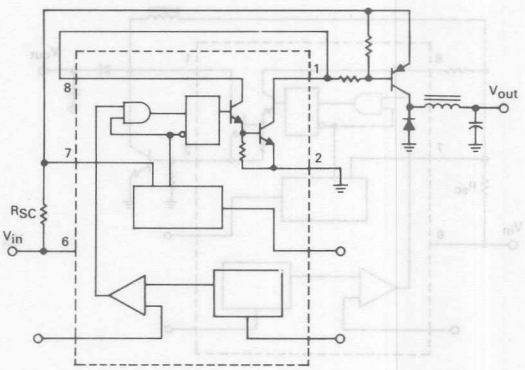
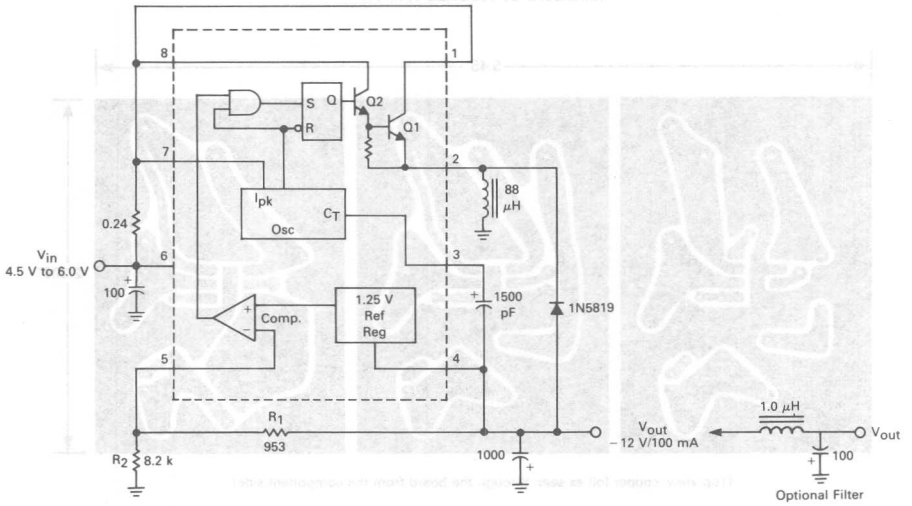


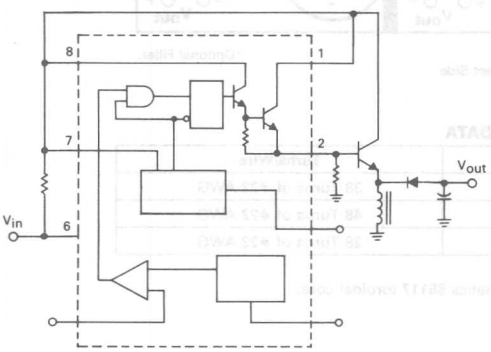
FIGURE 11 — VOLTAGE INVERTING CONVERTER



Test	Conditions	Results
Line Regulation	V_{in} = 4.5 V to 6.0 V, I_O = 100 mA	3.0 mV = ±0.012%
Load Regulation	V_{in} = 5.0 V, I_O = 10 to 100 mA	0.022 V = ±0.09%
Output Ripple	V_{in} = 5.0 V, I_O = 100 mA	50 mVp-p
Short Circuit Current	V_{in} = 5.0 V, R_L = 0.1 Ω	910 mA
Efficiency	V_{in} = 5.0 V, I_O = 100 mA	64.5%
Output Ripple With Optional Filter	V_{in} = 5.0 V, I_O = 100 mA	70 mVp-p

FIGURE 12 — EXTERNAL CURRENT BOOST CONNECTIONS FOR I_C PEAK GREATER THAN 1.5 A

12A — EXTERNAL NPN SWITCH



12B — EXTERNAL PNP SATURATED SWITCH

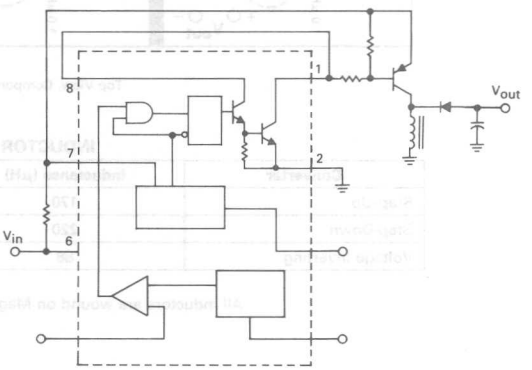
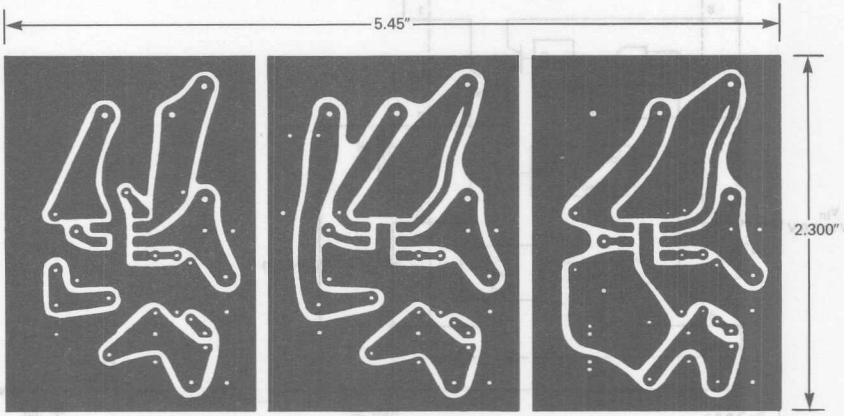
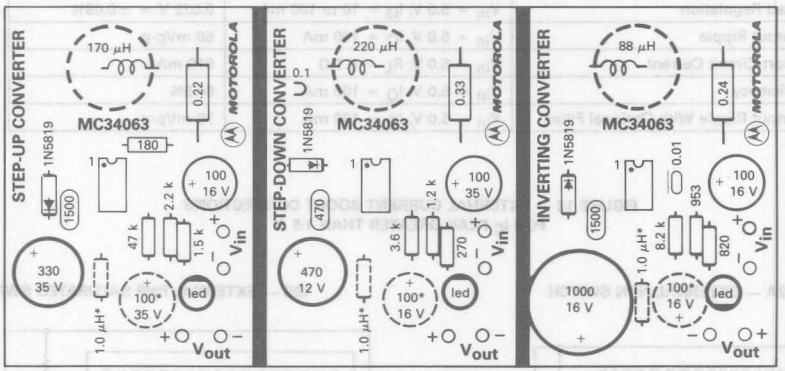


FIGURE 13 — PRINTED CIRCUIT BOARD AND COMPONENT LAYOUT
(CIRCUITS OF FIGURES 7, 9, 11)



(Top view, copper foil as seen through the board from the component side)



Top View, Component Side

*Optional Filter.

INDUCTOR DATA

Converter	Inductance (μH)	Turns/Wire
Step-Up	170	38 Turns of #22 AWG
Step-Down	220	48 Turns of #22 AWG
Voltage-Inverting	88	28 Turns of #22 AWG

All inductors are wound on Magnetics 55117 toroidal core.

FIGURE 14 — DESIGN FORMULA TABLE

Calculation	Step-Up	Step-Down	Voltage-Inverting
t_{on}/t_{off}	$\frac{V_{out}+V_F-V_{in(min)}}{V_{in(min)}-V_{sat}}$	$\frac{V_{out}+V_F}{V_{in(min)}-V_{sat}-V_{out}}$	$\frac{\lvert V_{out}\rvert+V_F}{V_{in}-V_{sat}}$
$(t_{on}+t_{off})$ max	$1/f_{min}$	$1/f_{min}$	$1/f_{min}$
C_T	$4 \times 10^{-5}\ t_{on}$	$4 \times 10^{-5}\ t_{on}$	$4 \times 10^{-5}\ t_{on}$
$I_{pk(switch)}$	$2I_{out(max)}(t_{on}/t_{off}+1)$	$2I_{out(max)}$	$2I_{out(max)}(t_{on}/t_{off}+1)$
R_{SC}	$0.3/1_{pk(switch)}$	$0.3/I_{pk(switch)}$	$0.3/I_{pk(switch)}$
$L_{(min)}$	$\frac{(V_{in(min)}-V_{sat})t_{on(max)}}{I_{pk(switch)}}$	$\frac{(V_{in(min)}-V_{sat}-V_{out})t_{on(max)}}{I_{pk(switch)}}$	$\frac{(V_{in(min)}-V_{sat})t_{on(max)}}{I_{pk(switch)}}$
C_O	$\approx \frac{I_{out}t_{on}}{V_{ripple(p-p)}}$	$\frac{I_{pk(switch)}(t_{on}+t_{off})}{8\ V_{ripple(p-p)}}$	$\approx \frac{I_{out}t_{on}}{V_{ripple(p-p)}}$

V_{sat} = Saturation voltage of the output switch.
V_F = Forward voltage drop of the output rectifier.

The following power supply characteristics must be chosen:

V_{in} — Nominal input voltage.

V_{out} -- Desired output voltage, $|V_{out}| = 1.25\ (1 + R2/R1)$

I_{out} — Desired output current.

f_{min} — Minimum desired output switching frequency at the selected values of V_{in} and I_O.

$V_{ripple(p-p)}$ — Desired peak-to-peak output ripple voltage. In practice, the calculated capacitor value will need to be increased due to its equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly affect the line and load regulation.

MOTOROLA

MC34064
MC33064

3

Product Preview

UNDERVOLTAGE SENSING CIRCUIT

UNDERVOLTAGE SENSING CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT

The MC34064 is an undervoltage sensing circuit specifically designed for use as a reset controller in microprocessor-based systems. It offers the designer an economical solution for low voltage detection with a single external resistor. The MC34064 features a trimmed-in-package bandgap reference, and a comparator with precise thresholds and built-in hysteresis to prevent erratic reset operation. The open collector reset output is capable of sinking in excess of 10 mA, and operation is guaranteed down to 1.0 volt input with low standby current. These devices are packaged in 3-pin TO-226AA and 8-pin surface mount packages.

Applications include direct monitoring of the 5.0 volt MPU/logic power supply used in appliance, automotive, consumer and industrial equipment.

- Trimmed-In-Package Temperature Compensated Reference
- Precise Comparator Thresholds Guaranteed Over Temperature
- Comparator Hysteresis Prevents Erratic Reset
- Reset Output Capable of Sinking in Excess of 10 mA
- Internal Clamp Diode for Discharging Delay Capacitor
- Guaranteed Reset Operation with 1.0 Volt Input
- Low Standby Current
- Economical TO-226AA and Surface Mount Packages

P SUFFIX
PLASTIC PACKAGE
CASE 29-04



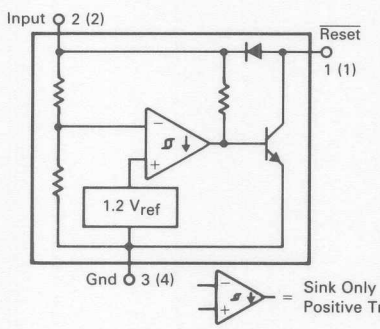
PIN 1. $\overline{\text{RESET}}$
2. INPUT
3. GROUND

D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SO-8



PIN 1. $\overline{\text{RESET}}$
2. INPUT
3. N.C.
4. GROUND
5. N.C.
6. N.C.
7. N.C.
8. N.C.

REPRESENTATIVE BLOCK DIAGRAM



Pin numbers adjacent to terminals are for the 3-pin TO-226AA package.
Pin numbers in parenthesis are for the D suffix SO-8 package.

ORDERING INFORMATION

Device	Temperature Range	Package
MC34064D-5	0°C to +70°C	Plastic SO-8
MC34064P-5		Plastic TO-226AA
MC33064D-5	−40°C to +85°C	Plastic SO-8
MC33064P-5		Plastic TO-226AA

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Input Supply Voltage	V_{in}	−1.0 to 10	V
$\overline{\text{Reset}}$ Output Voltage	V_O	10	V
$\overline{\text{Reset}}$ Output Sink Current	I_{Sink}	Internally Limited	mA
Clamp Diode Forward Current, Pin 1 to 2 (Note 1)	I_F	100	mA
Power Dissipation and Thermal Characteristics			
P Suffix, Plastic Package			
Maximum Power Dissipation @ T_A = 25°C	P_D	625	mW
Thermal Resistance, Junction to Air	$R_{\theta JA}$	200	°C/W
D Suffix, Plastic Package			
Maximum Power Dissipation @ T_A = 25°C	P_D	625	mW
Thermal Resistance Junction to Air	$R_{\theta JA}$	200	°C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_A		°C
MC34064		0 to +70	
MC33064		−40 to +85	
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Notes 2 and 3].

Characteristic	Symbol	Min	Typ	Max	Unit
COMPARATOR					
Threshold Voltage					V
High State Output (V_{in} Increasing)	V_{IH}	4.5	4.61	4.7	
Low State Output (V_{in} Decreasing)	V_{IL}	4.5	4.59	4.7	
Hysteresis	V_H	0.01	0.02	0.05	
$\overline{\text{RESET}}$ OUTPUT					
Output Sink Saturation	V_{OL}				V
(V_{in} = 4.0 V, I_{Sink} = 8.0 mA)		—	0.46	1.0	
(V_{in} = 4.0 V, I_{Sink} = 2.0 mA)		—	0.15	0.4	
(V_{in} = 1.0 V, I_{Sink} = 0.1 mA)		—	—	0.1	
Output Sink Current (V_{in}, $\overline{\text{Reset}}$ = 4.0 V)	I_{Sink}	10	27	60	mA
Output Off-State Leakage (V_{in}, $\overline{\text{Reset}}$ = 5.0 V)	I_{OH}	—	0.02	0.5	μA
Clamp Diode Forward Voltage, Pin 1 to 2 (I_F = 10 mA)	V_F	0.6	0.9	1.2	V
TOTAL DEVICE					
Operating Input Voltage Range	V_{in}	1.0 to 6.5	—	—	V
Quiescent Input Current (V_{in} = 5.0 V)	I_{in}	—	390	500	μA

NOTES:
1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
3. T_{low} = 0°C for MC34064 = −40°C for MC33064 T_{high} = +70°C for MC34064 = +85°C for MC33064

FIGURE 1 — $\overline{\text{RESET}}$ OUTPUT VOLTAGE versus INPUT VOLTAGE

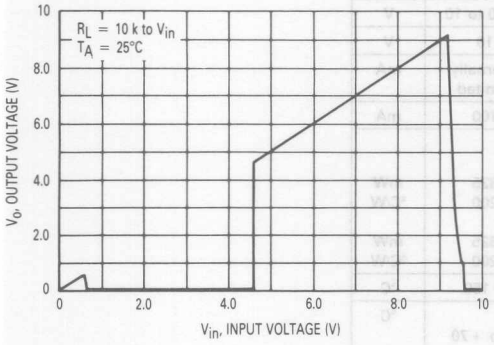


FIGURE 2 — $\overline{\text{RESET}}$ OUTPUT VOLTAGE versus INPUT VOLTAGE

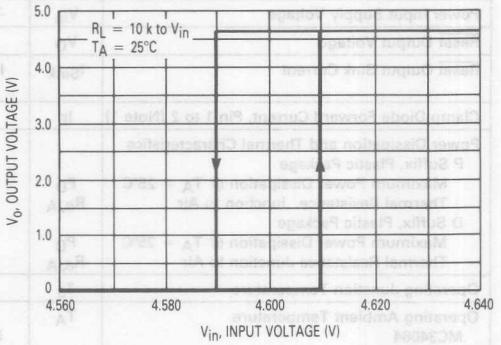


FIGURE 3 — COMPARATOR THRESHOLD VOLTAGE versus TEMPERATURE

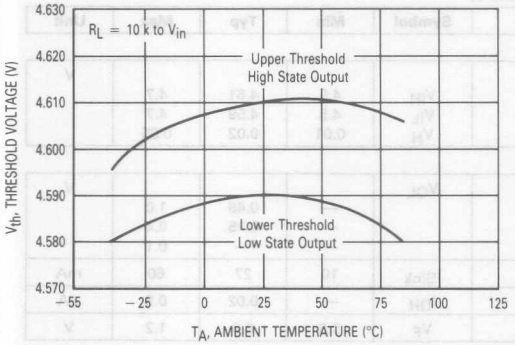


FIGURE 4 — INPUT CURRENT versus INPUT VOLTAGE

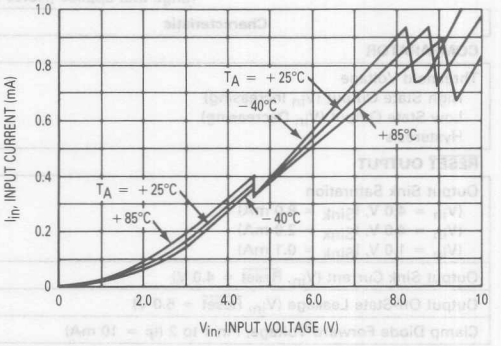


FIGURE 5 — $\overline{\text{RESET}}$ OUTPUT SATURATION versus SINK CURRENT

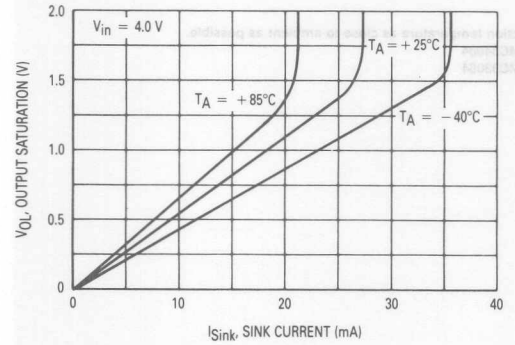


FIGURE 6 — CLAMP DIODE FORWARD CURRENT versus VOLTAGE

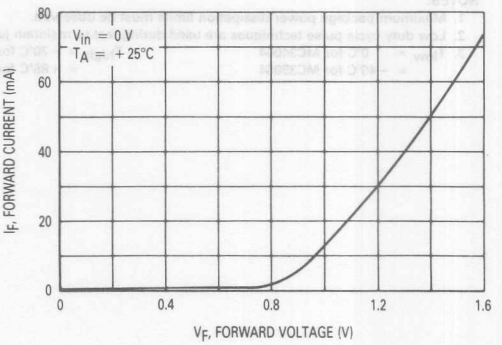
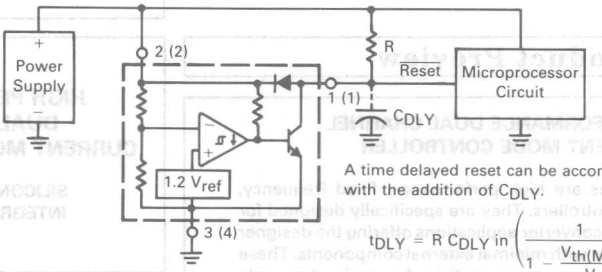


FIGURE 7 — LOW VOLTAGE MICROPROCESSOR RESET



A time delayed reset can be accomplished with the addition of C_{DLY}.

$$t_{DLY} = R\,C_{DLY}\,\ln\left(\frac{1}{1 - \frac{V_{th(MPU)}}{V_{in}}}\right)$$

FIGURE 8 — VOLTAGE MONITOR

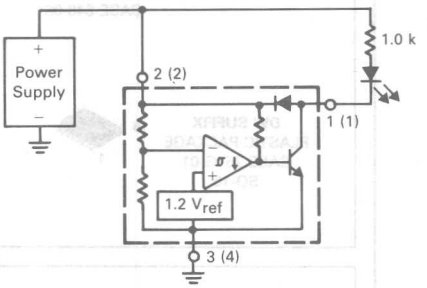


FIGURE 9 — SOLAR POWERED BATTERY CHARGER

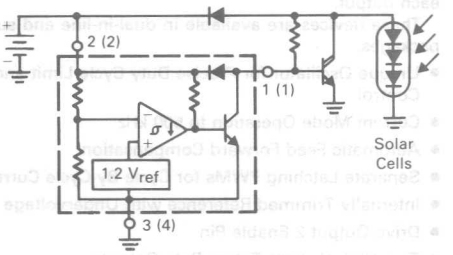
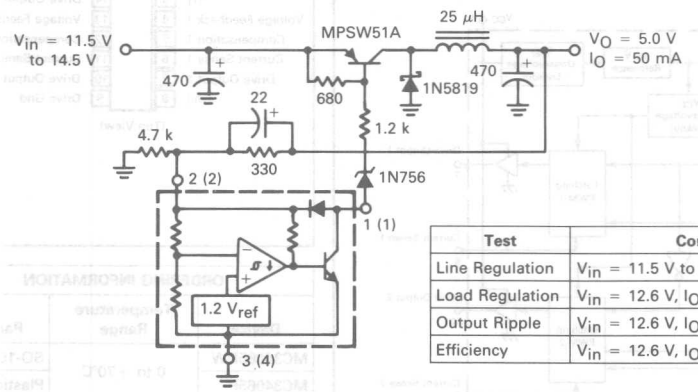


FIGURE 10 — LOW POWER SWITCHING REGULATOR



Test	Conditions	Results
Line Regulation	V_{in} = 11.5 V to 14.5 V, I_O = 50 mA	35 mV
Load Regulation	V_{in} = 12.6 V, I_O = 0 mA to 50 mA	12 mV
Output Ripple	V_{in} = 12.6 V, I_O = 50 mA	60 mV_{p-p}
Efficiency	V_{in} = 12.6 V, I_O = 50 mA	77%

MOTOROLA

MC34065
MC33065

Product Preview

HIGH PERFORMANCE DUAL CHANNEL CURRENT MODE CONTROLLER

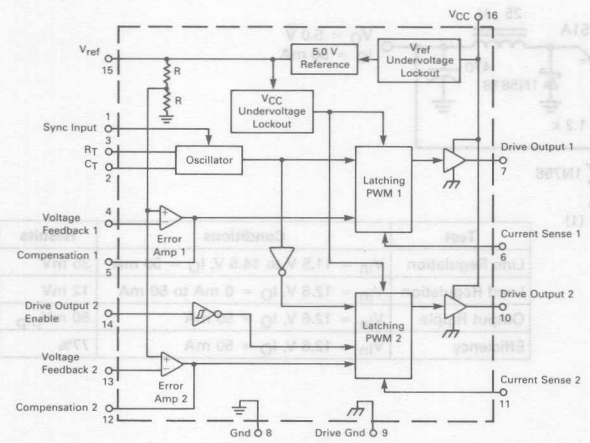
The MC34065 series are high performance, fixed frequency, dual current mode controllers. They are specifically designed for Off-Line and DC to DC converter applications offering the designer a cost effective solution with minimal external components. These integrated circuits feature a unique oscillator for precise duty cycle limit and frequency control, a temperature compensated reference, two high gain error amplifiers, two current sensing comparators, drive output 2 enable pin, and two high current totem pole outputs ideally suited for driving power MOSFETs.

Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle-by-cycle current limiting, and a latch for single pulse metering of each output.

These devices are available in dual-in-line and surface mount packages.

- Unique Oscillator for Precise Duty Cycle Limit and Frequency Control
- Current Mode Operation to 500 kHz
- Automatic Feed Forward Compensation
- Separate Latching PWMs for Cycle-By-Cycle Current Limiting
- Internally Trimmed Reference with Undervoltage Lockout
- Drive Output 2 Enable Pin
- Two High Current Totem Pole Outputs
- Input Undervoltage Lockout with Hysteresis
- Low Start-Up and Operating Current
- Direct Interface with Motorola SENSEFET Products

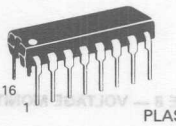
SIMPLIFIED BLOCK DIAGRAM



This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

HIGH PERFORMANCE DUAL CHANNEL CURRENT MODE CONTROLLER

SILICON MONOLITHIC INTEGRATED CIRCUIT

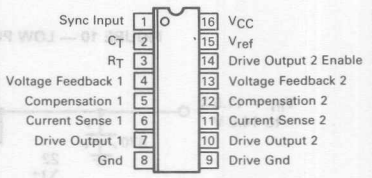


P SUFFIX
PLASTIC PACKAGE
CASE 648-06



DW SUFFIX
PLASTIC PACKAGE
CASE 751G-01
SO-16

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC34065DW	0 to +70°C	SO-16
MC34065P		Plastic DIP
MC33065DW	−40 to +85°C	SO-16
MC33065P		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Total Power Supply and Zener Current	$(I_{CC}+I_Z)$	50	mA
Output Current, Source or Sink (Note 1)	I_O	1.0	A
Output Energy (Capacitive Load per Cycle)	W	5.0	μJ
Current Sense, Enable, and Voltage Feedback Inputs	V_{in}	−0.3 to +5.5	V
Sync Input			
High State (Voltage)	V_{IH}	5.5	V
Low State (Reverse Current)	I_{IL}	−5.0	mA
Error Amp Output Sink Current	I_O	10	mA
Power Dissipation and Thermal Characteristics			
DW Suffix Package SO-16 Case 751G-01			
Maximum Power Dissipation @ T_A = 25°C	P_D	862	mW
Thermal Resistance Junction to Air	$R_{\theta JA}$	145	°C/W
P Suffix Package Case 648-06			
Maximum Power Dissipation @ T_A = 25°C	P_D	1.25	W
Thermal Resistance Junction to Air	$R_{\theta JA}$	100	°C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_A		°C
MC34065		0 to +70	
MC33065		−40 to +85	
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 2], R_T = 8.2 kΩ, C_T = 3.3 nF, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3].)

Characteristic	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Output Voltage (I_O = 1.0 mA, T_J = 25°C)	V_{ref}	4.9	5.0	5.1	V
Line Regulation (V_{CC} = 11 V to 15 V)	Reg_{line}	—	2.0	20	mV
Load Regulation (I_O = 1.0 mA to 10 mA)	Reg_{load}	—	3.0	25	mV
Total Output Variation over Line, Load, and Temperature	V_{ref}	4.85	—	5.15	V
Output Short Circuit Current	I_{SC}	30	100	—	mA
OSCILLATOR and PWM SECTIONS					
Total Frequency Variation over Line and Temperature (V_{CC} = 11 V to 15 V, T_A = T_{low} to T_{high})	f_{OSC}				kHz
MC34065		46.5	49	51.5	
MC33065		45	49	53	
Frequency Change with Voltage (V_{CC} = 11 V to 15 V)	$\Delta f_{OSC}/\Delta V$	—	0.2	1.0	%
Duty Cycle at each Output					%
Maximum	DC_{max}	46	49.5	52	
Minimum	DC_{min}	—	—	0	
Sync Input Current					μA
High State (V_{in} = 2.4 V)	I_{IH}	—	170	250	
Low State (V_{in} = 0.8 V)	I_{IL}	—	80	160	
ERROR AMPLIFIERS					
Voltage Feedback Input (V_O = 2.5 V)	V_{FB}	2.42	2.5	2.58	V
Input Bias Current (V_{FB} = 5.0 V)	I_{IB}	—	−0.1	−1.0	μA
Open-Loop Voltage Gain (V_O = 2.0 to 4.0 V)	A_{VOL}	65	100	—	dB
Unity Gain Bandwidth (T_J = 25°C)	BW	0.7	1.0	—	MHz
Power Supply Rejection Ratio (V_{CC} = 11 V to 15 V)	PSRR	60	90	—	dB
Output Current					mA
Source (V_O = 3.0 V, V_{FB} = 2.3 V)	I_{Source}	−0.45	−1.0	—	
Sink (V_O = 1.2 V, V_{FB} = 2.7 V)	I_{Sink}	2.0	12	—	
Output Voltage Swing					V
High State (R_L = 15 k to ground, V_{FB} = 2.3 V)	V_{OH}	5.0	6.2	—	
Low State (R_L = 15 k to V_{ref}, V_{FB} = 2.7 V)	V_{OL}	—	0.8	1.1	

Notes: 1. Maximum package power dissipation limits must be observed.
2. Adjust V_{CC} above the Start-Up threshold before setting to 15 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
T_{low} = 0°C for the MC34065 = −40°C for MC33065
T_{high} = +70°C for MC34065 = +85°C for MC33065

3

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 2], R_T = 8.2 kΩ, C_T = 3.3 nF, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3].)

Characteristic	Symbol	Min	Typ	Max	Unit
CURRENT SENSE SECTION					
Current Sense Input Voltage Gain (Notes 4 and 5)	A_V	2.75	3.0	3.25	V/V
Maximum Current Sense Input Threshold (Note 4)	V_{th}	430	480	530	mV
Input Bias Current	I_{IB}	—	−2.0	−10	μA
Propagation Delay (Current Sense Input to Output)	$t_{PLN(IN/OUT)}$	—	150	300	ns
DRIVE OUTPUT 2 ENABLE PIN					
Enable Pin Voltage					V
High State (Output 2 Enabled)	V_{IH}	3.5	—	V_{ref}	
Low State (Output 2 Disabled)	V_{IL}	0	—	1.5	
Low State Input Current (V_{IL} = 0 V)	I_{IB}	100	250	400	μA
DRIVE OUTPUTS					
Output Voltage					V
Low State (I_{Sink} = 20 mA)	V_{OL}	—	0.1	0.4	
(I_{Sink} = 200 mA)		—	1.6	2.5	
High State (I_{Source} = 20 mA)	V_{OH}	13	13.5	—	
(I_{Source} = 200 mA)		12	13.4	—	
Output Voltage with UVLO Activated (V_{CC} = 6.0 V, I_{Sink} = 1.0 mA)	$V_{OL(UVLO)}$	—	0.1	1.1	V
Output Voltage Rise Time (C_L = 1.0 nF)	t_r	—	28	150	ns
Output Voltage Fall Time (C_L = 1.0 nF)	t_f	—	25	150	ns
UNDERVOLTAGE LOCKOUT SECTION					
Start-Up Threshold	V_{th}	13	14	15	V
Minimum Operating Voltage After Turn-On	$V_{CC(min)}$	9.0	10	11	V
TOTAL DEVICE					
Power Supply Current	I_{CC}				mA
Start-Up (V_{CC} = 12 V)		—	0.6	1.0	
Operating (Note 2)		—	20	25	
Power Supply Zener Voltage (I_{CC} = 30 mA)	V_Z	15.5	17	19	V

Notes: 1. Maximum package power dissipation limits must be observed.
2. Adjust V_{CC} above the Start-Up threshold before setting to 15 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
T_{low} = 0°C for the MC34065 T_{high} = +70°C for MC34065
= −40°C for MC33065 = +85°C for MC33065
4. This parameter is measured at the latch trip point with V_{fb} = 0 V.
5. Comparator gain is defined as $A_V = \frac{\Delta V \text{ Compensation}}{\Delta V \text{ Current Sense}}$

FIGURE 1 — TIMING RESISTOR versus OSCILLATOR FREQUENCY

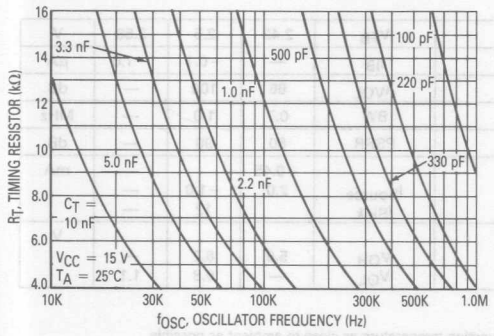


FIGURE 2 — MAXIMUM OUTPUT DUTY CYCLE versus OSCILLATOR FREQUENCY

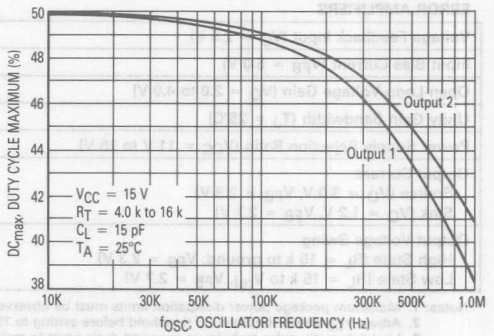


FIGURE 3 — ERROR AMP SMALL-SIGNAL TRANSIENT RESPONSE

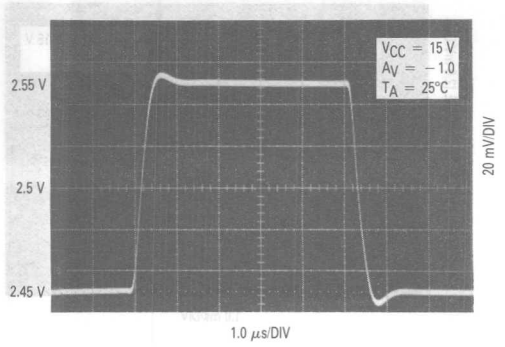


FIGURE 4 — ERROR AMP LARGE-SIGNAL TRANSIENT RESPONSE

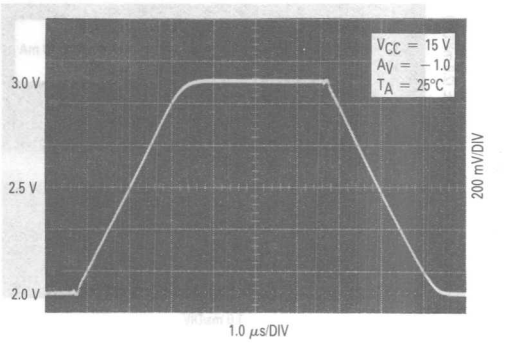


FIGURE 5 — ERROR AMP OPEN-LOOP GAIN AND PHASE versus FREQUENCY

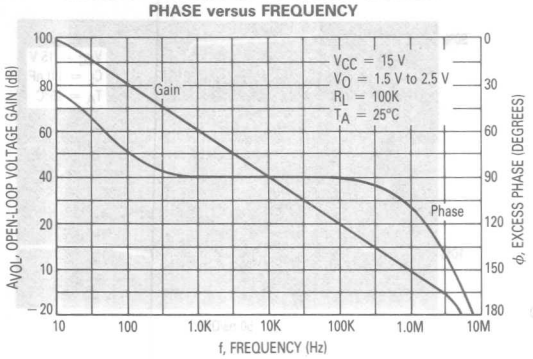


FIGURE 6 — CURRENT SENSE INPUT THRESHOLD versus ERROR AMP OUTPUT VOLTAGE

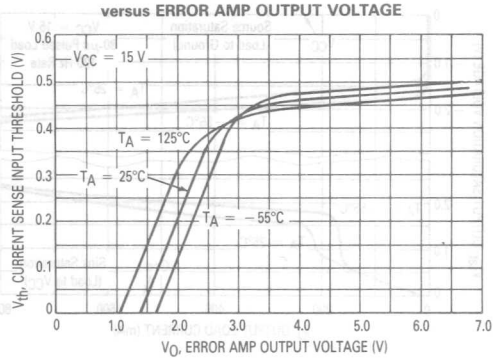


FIGURE 7 — REFERENCE VOLTAGE CHANGE versus SOURCE CURRENT

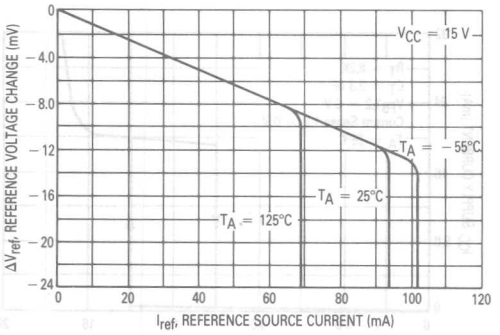
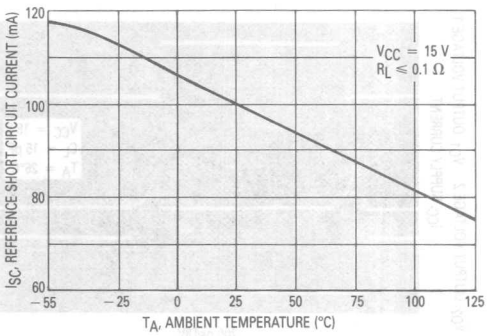


FIGURE 8 — REFERENCE SHORT CIRCUIT CURRENT versus TEMPERATURE



3

FIGURE 9 — REFERENCE LOAD REGULATION

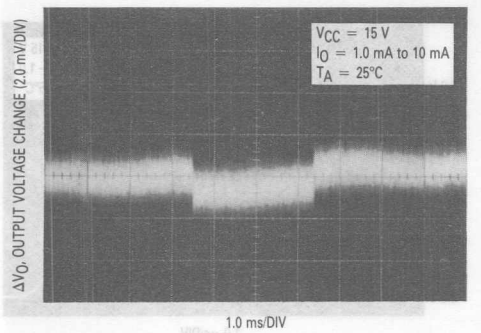


FIGURE 10 — REFERENCE LINE REGULATION

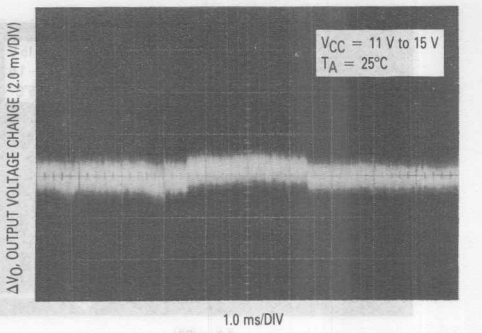


FIGURE 11 — OUTPUT SATURATION VOLTAGE versus LOAD CURRENT

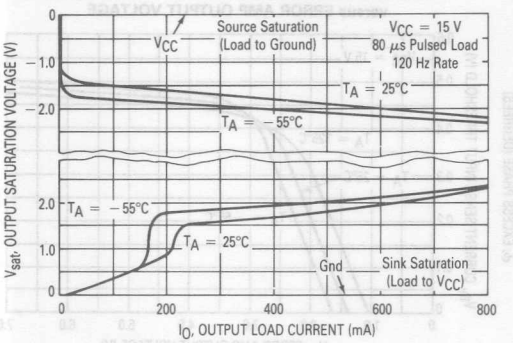


FIGURE 12 — OUTPUT WAVEFORM

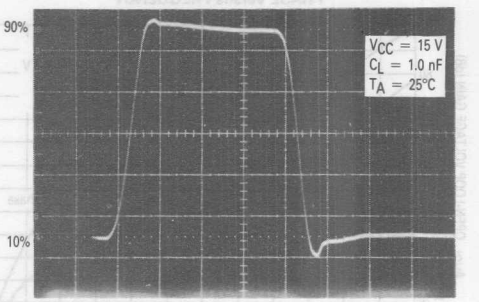


FIGURE 13 — OUTPUT CROSS-CONDUCTION

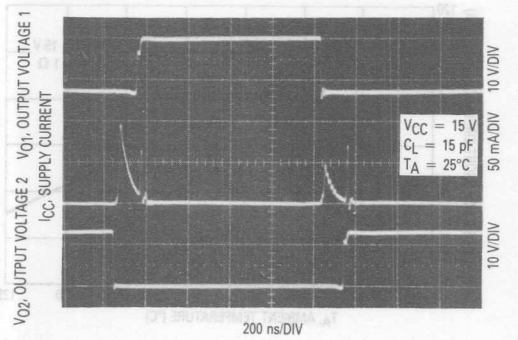
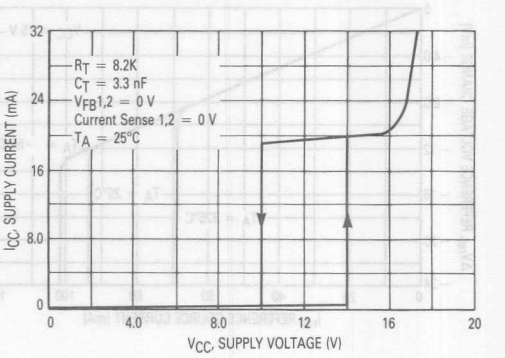


FIGURE 14 — SUPPLY CURRENT versus SUPPLY VOLTAGE



OPERATING DESCRIPTION

The MC34065 series are high performance, fixed frequency, dual channel current mode controllers specifically designed for Off-Line and DC to DC converter applications. These devices offer the designer a cost effective solution with minimal external components where independent regulation of two power converters is required. The Representative Block Diagram is shown in Figure 15. Each channel contains a high gain error amplifier, current sensing comparator, pulse width modulator latch, and totem pole output driver. The oscillator, reference regulator, and undervoltage lockout circuits are common to both channels.

Oscillator

The unique oscillator configuration employed features precise frequency and duty cycle control. The frequency is programmed by the values selected for the timing components R_T and C_T. Capacitor C_T is charged and discharged by an equal magnitude internal current source and sink, generating a symmetrical 50 percent duty cycle waveform at Pin 2. The oscillator peak and valley thresholds are 3.5 V and 1.6 V respectively. The source/sink current magnitude is controlled by resistor R_T. For proper operation over temperature it must be in the range of 4.0 kΩ to 16 kΩ as shown in Figure 1.

As C_T charges and discharges, an internal blanking pulse is generated that alternately drives the center inputs of the upper and lower NOR gates high. This, in conjunction with a precise amount of delay time introduced into each channel, produces well defined non-overlapping output duty cycles. Output 2 is enabled while C_T is charging, and Output 1 is enabled during the discharge. Figure 2 shows the Maximum Output Duty Cycle versus Oscillator Frequency. Note that even at 500 kHz, each output is capable of approximately 44% on-time, making this controller suitable for high frequency power conversion applications.

In many noise sensitive applications it may be desirable to frequency-lock the converter to an external system clock. This can be accomplished by applying a clock signal as shown in Figure 17. For reliable locking, the free-running oscillator frequency should be set about 10% less than the clock frequency. Referring to the timing diagram shown in Figure 16, the rising edge of the clock signal applied to the Sync input, terminates charging of C_T and Drive Output 2 conduction. By tailoring the clock waveform symmetry, accurate duty cycle clamping of either output can be achieved. A circuit method for this, and multi unit synchronization, is shown in Figure 18.

Error Amplifier

Each channel contains a fully-compensated Error Amplifier with access to the inverting input and output. The amplifier features a typical dc voltage gain of 100 dB, and a unity gain bandwidth of 1.0 MHz with 71 degrees of phase margin (Figure 5). The non-inverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input through a resistor divider. The maximum input bias current is −1.0 μA which will cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amp output (Pin 5, 12) is provided for external loop compensation. The output voltage is offset by two diode drops (≈1.4 V) and divided by three before it connects to the inverting input of the Current Sense Comparator. This guarantees that no pulses appear at the Drive Output (Pin 7, 10) when the error amplifier output is at its lowest state (V_{OL}). This occurs when the power supply is operating and the load is removed, or at the beginning of a soft-start interval (Figures 20, 21).

The minimum allowable Error Amp feedback resistance is limited by the amplifier's source current (0.5 mA) and the output voltage (V_{OH}) required to reach the comparator's 0.5 V clamp level with the inverting input at ground. This condition happens during initial system startup or when the sensed output is shorted:

$$R_{f(MIN)} \approx \frac{3.0\ (0.5\ V) + 1.4\ V}{0.5\ mA} = 5800\ \Omega$$

Current Sense Comparator and PWM Latch

The MC34065 operates as a current mode controller, whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier output. Thus the error signal controls the peak inductor current on a cycle-by-cycle basis. The Current Sense Comparator-PWM Latch configuration used ensures that only a single pulse appears at the Drive Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting a ground-referenced sense resistor R_S in series with the source of output switch Q1. This voltage is monitored by the Current Sense Input (Pin 6, 11) and compared to a level derived from the Error Amp output. The peak inductor current under normal operating conditions is controlled by the voltage at Pin 5, 12 where:

$$I_{pk} = \frac{V_{(Pin\ 5,\ 12)} - 1.4\ V}{3\ R_S}$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the Current Sense Comparator threshold will be internally clamped to 0.5 V. Therefore the maximum peak switch current is:

$$I_{pk(max)} = \frac{0.5\ V}{R_S}$$

When designing a high power switching regulator it may be desirable to reduce the internal clamp voltage in order to keep the power dissipation of R_S to a reasonable level. A simple method to adjust this voltage is shown in Figure 19. The two external diodes are used to compensate the internal diodes, yielding a constant clamp voltage over temperature. Erratic operation due to noise pickup can result if there is an excessive reduction of the $I_{pk(max)}$ clamp voltage.

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Current Sense input with a time constant that approximates the spike duration will usually eliminate the instability; refer to Figure 24.

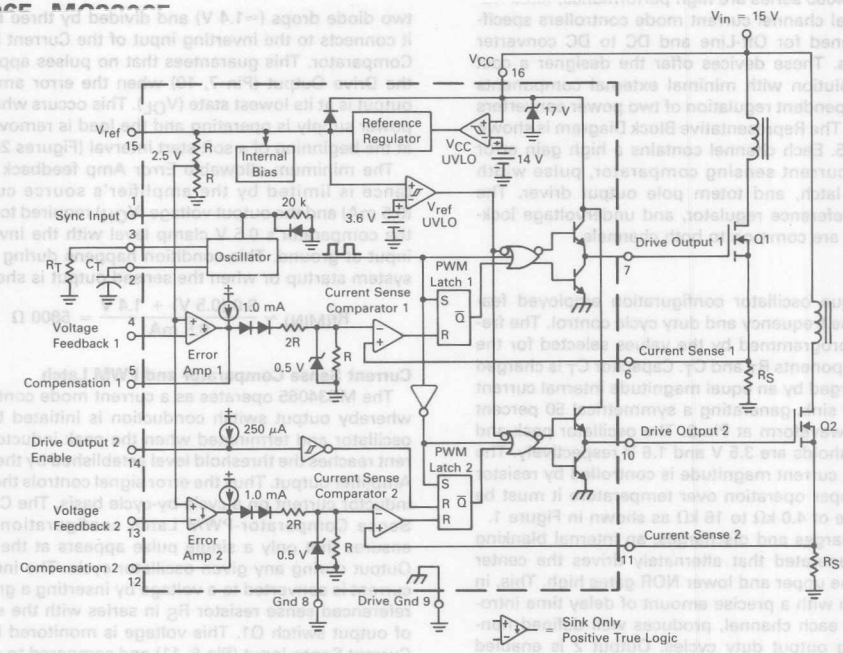
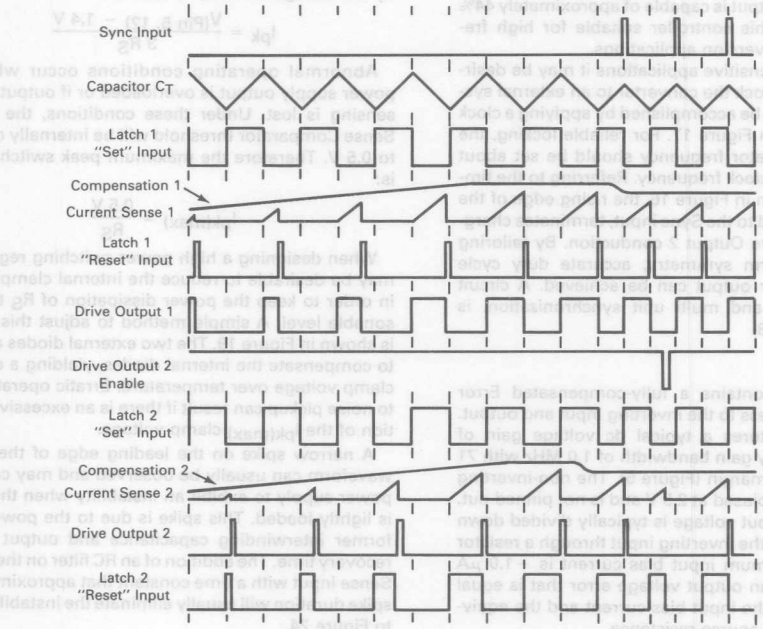


FIGURE 16 — TIMING DIAGRAM



Undervoltage Lockout

Two Undervoltage Lockout comparators have been incorporated to guarantee that the IC is fully functional before the output stages are enabled. The positive power supply terminal (V_{CC}) and the reference output (V_{ref}) are each monitored by separate comparators. Each has built-in hysteresis to prevent erratic output behavior as their respective thresholds are crossed. The V_{CC} comparator upper and lower thresholds are 14 V and 10 V respectively. The hysteresis and low start-up current makes these devices ideally suited to off-line converter applications where efficient bootstrap start-up techniques are required (Figure 28). The V_{ref} comparator disables the Drive Outputs until the internal circuitry is functional. This comparator has upper and lower thresholds of 3.6 V and 3.4 V. A 17 V zener is connected as a shunt regulator from V_{CC} to ground. Its purpose is to protect the IC and power MOSFET gate from excessive voltage that can occur during system start-up. The guaranteed minimum operating voltage after turn-on is 11 V.

Drive Outputs and Drive Ground

Each channel contains a single totem-pole output stage that is specifically designed for direct drive of power MOSFET's. The Drive Outputs are capable of up to ±10 A peak current and have a typical rise and fall times of 28 ns with a 1.0 nF load. Internal circuitry has been added to keep the outputs in a sinking mode whenever an Undervoltage Lockout is active. This characteristic eliminates the need for an external pull-down resistor. Cross-conduction current in the totem-pole output stage has been minimized for high speed operation, as shown in Figure 13. The average added power due to cross-conduction with V_{CC} = 15 V is only 60 mW at 500 kHz.

Although the Drive Outputs were optimized for MOSFETs, they can easily supply the negative base current required by bipolar NPN transistors for enhanced turn-off (Figure 25). The outputs do not contain internal current limiting, therefore an external series resistor may be required to prevent the peak output current from exceeding the ±1.0 A maximum rating. The sink saturation (V_{OL}) is less than 0.4 V at 100 mA.

A separate Drive Ground pin is provided and, with proper implementation, will significantly reduce the level of switching transient noise imposed on the control circuitry. This becomes particularly useful when reducing the $I_{pk(max)}$ clamp level. Figure 23 shows the proper ground connections required for current sensing power MOSFET applications.

Drive Output 2 Enable Pin

This input is used to enable Drive Output 2. Drive Output 1 can be used to control circuitry that must run continuously such as volatile memory and the system clock, or a remote controlled receiver, while Drive Output 2 controls the high power circuitry that is occasionally turned off.

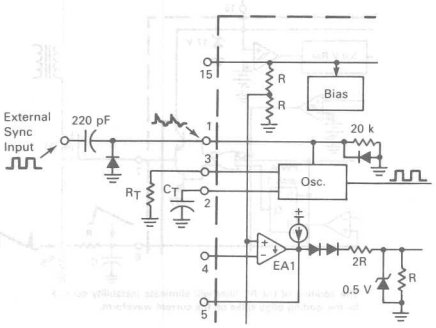
Reference

The 5.0 V bandgap reference is trimmed to ±2.0% tolerance at T_J = 25°C. The reference has short circuit protection and is capable of providing in excess of 30 mA for powering any additional control system circuitry.

Design Considerations

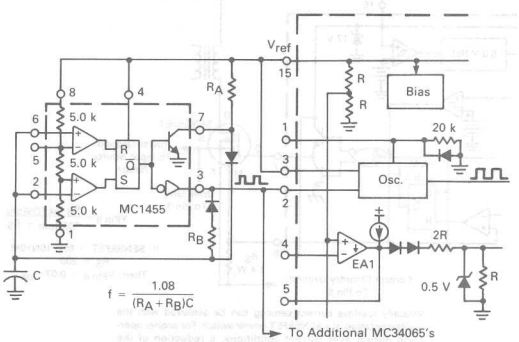
Do not attempt to construct the converter on wire-wrap or plug-in prototype boards. High frequency circuit layout techniques are imperative to prevent pulse-width jitter. This is usually caused by excessive noise pick-up imposed on the Current Sense or Voltage Feedback inputs. Noise immunity can be improved by lowering circuit impedances at these points. The printed circuit layout should contain a ground plane with low current signal and high current switch and output grounds returning on separate paths back to the input filter capacitor. Ceramic bypass capacitors (0.1 μF) connected directly to V_{CC} and V_{ref} may be required depending upon circuit layout. This provides a low impedance path for filtering the high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI. The Error Amp compensation circuitry and the converter output voltage-divider should be located close to the IC and as far as possible from the power switch and other noise generating components.

FIGURE 17 — EXTERNAL CLOCK SYNCHRONIZATION



The external diode clamp is required if the negative Sync current is greater than −5.0 mA.

FIGURE 18 — EXTERNAL DUTY CYCLE CLAMP AND MULTI UNIT SYNCHRONIZATION



D_{max} Drive Output 1 = $\frac{R_B}{R_A + R_B}$ D_{max} Drive Output 2 = $\frac{R_A}{R_A + R_B}$

3

FIGURE 19 — ADJUSTABLE REDUCTION OF CLAMP LEVEL

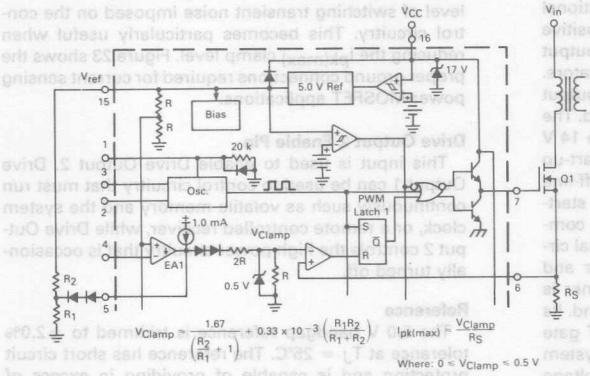


FIGURE 20 — SOFT-START CIRCUIT

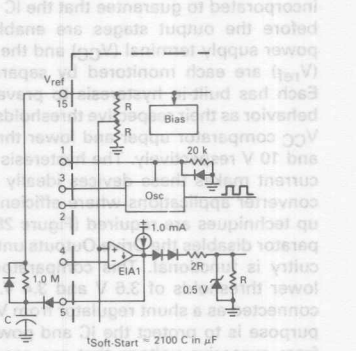


FIGURE 21 — ADJUSTABLE REDUCTION OF CLAMP LEVEL WITH SOFT-START

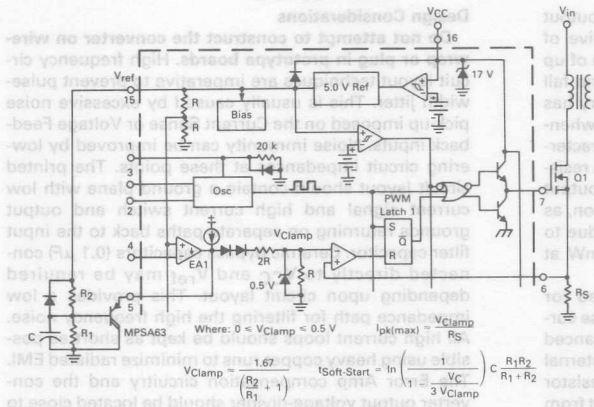
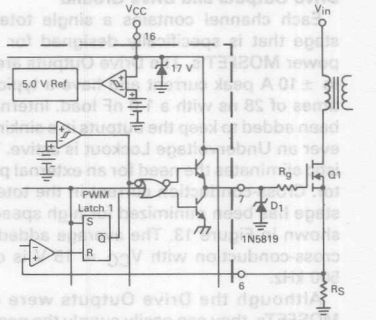
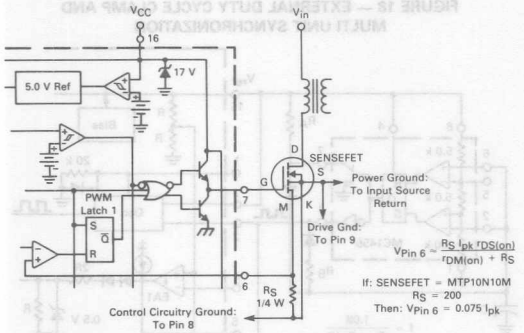


FIGURE 22 — MOSFET PARASITIC OSCILLATIONS



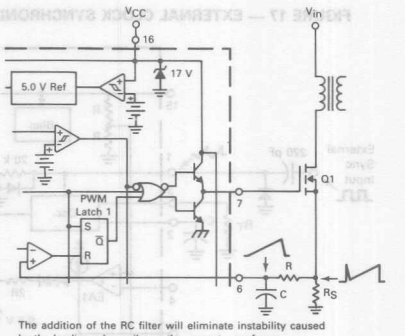
Series gate resistor R_g may be needed to damp high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate-source circuit. R_g will decrease the MOSFET switching speed. Schottky diode D_1 is required if circuit ringing drives the output pin below ground.

FIGURE 23 — CURRENT SENSING POWER MOSFET



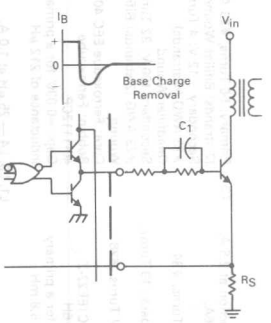
Virtually lossless current sensing can be achieved with the implementation of a SENSEFET power switch. For proper operation during over current conditions, a reduction of the $I_{pk(max)}$ clamp level must be implemented. Refer to Figures 19 and 21.

FIGURE 24 — CURRENT WAVEFORM SPIKE SUPPRESSION



The addition of the RC filter will eliminate instability caused by the leading edge spike on the current waveform.

FIGURE 25 — BIPOLAR TRANSISTOR DRIVE



The totem-pole outputs can furnish negative base current for enhanced transistor turn-off, with the addition of capacitor C_1.

FIGURE 26 — ISOLATED MOSFET DRIVE

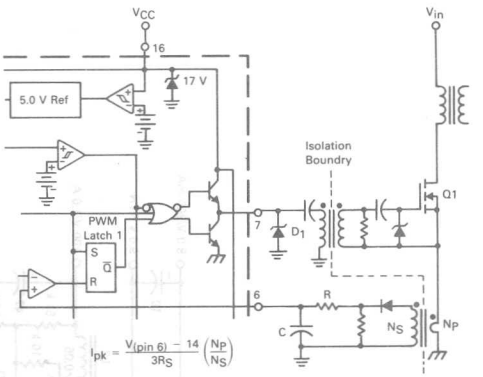
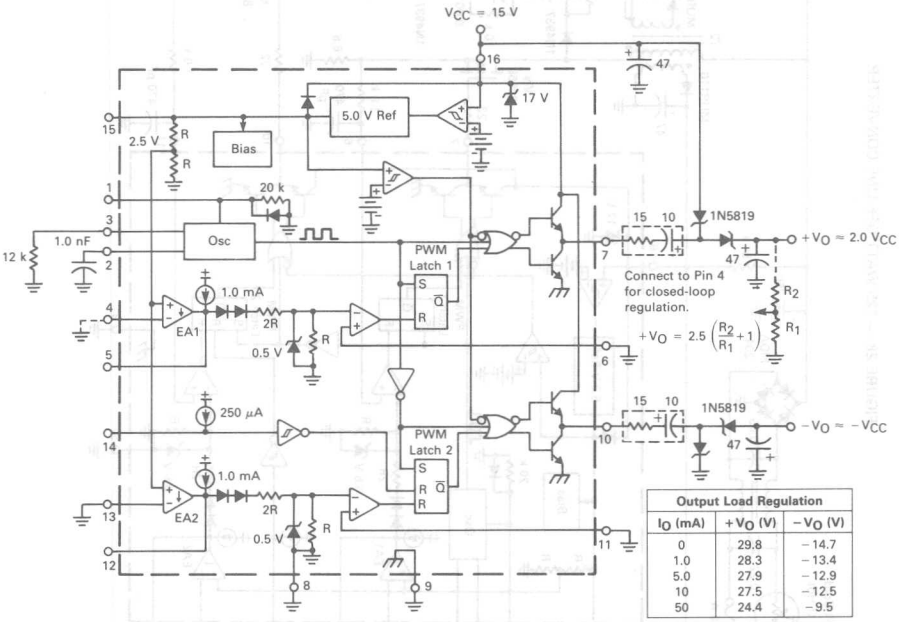


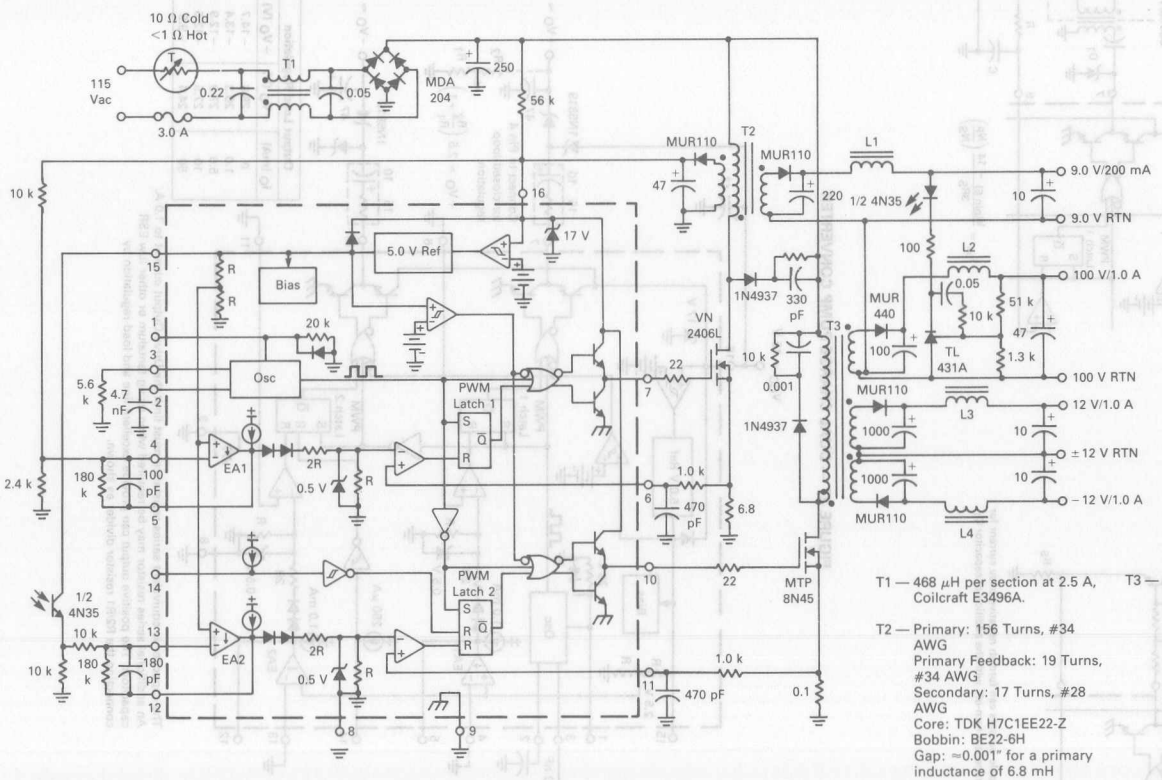
FIGURE 27 — DUAL CHARGE PUMP CONVERTER



Output Load Regulation		
I_O (mA)	$+V_O$ (V)	$-V_O$ (V)
0	29.8	−14.7
1.0	28.3	−13.4
5.0	27.9	−12.9
10	27.5	−12.5
50	24.4	−9.5

The capacitor is equivalent series resistance must limit the Drive Output current to 1.0 A. An additional series resistor may be required when using tantalum or other low ESR capacitors. The positive output can provide excellent line and load regulation by connecting the R2/R1 resistor divider as shown.

FIGURE 28 — 125 WATT OFF-LINE CONVERTER



T1 — 468 μH per section at 2.5 A, Coilcraft E3496A.

T2 — Primary: 156 Turns, #34 AWG
Primary Feedback: 19 Turns, #34 AWG
Secondary: 17 Turns, #28 AWG
Core: TDK H7C1EE22-Z
Bobbin: BE22-6H
Gap: ≈0.001" for a primary inductance of 6.8 mH

T3 — Primary: 56 Turns, #23 AWG (2 strands) Bifiliar Wound
Secondary ±12 V: 4 Turns, #23 AWG (4 strands) Quadfiliar Wound
Secondary 100 V: 32 Turns, #23 AWG (2 strands) Bifiliar Wound
Core: Ferroxcube EEC 40-3C8
Bobbin: Ferroxcube 40-1112CP
Gap: ≈0.030" for a primary inductance of 212 μH

L1, L3, L4 — 25 μH at 1.0 A, Coilcraft Z7157.

L2 — 10 μH at 3.0 A, Coilcraft PCV-0-010-03.

PIN FUNCTION DESCRIPTION

Pin #	Function	Description
1	Sync Input	A narrow rectangular waveform applied to this input will synchronize the Oscillator. A dc voltage within the range of 2.4 V to 5.5 V will inhibit the Oscillator.
2	C_T	Timing capacitor C_T connects from this pin to ground setting the free-running Oscillator frequency range.
3	R_T	Resistor R_T connects from this pin to ground precisely setting the charge current for C_T. R_T must be between 4.0 k and 16 k.
4	Voltage Feedback 1	This pin is the inverting input of Error Amplifier 1. It is normally connected to the switching power supply output through a resistor divider.
5	Compensation 1	This pin is the output of Error Amplifier 1 and is made available for loop compensation.
6	Current Sense 1	A voltage proportional to the inductor current is connected to this input. PWM 1 uses this information to terminate conduction of output switch Q1.
7	Drive Output 1	This pin directly drives the gate of a power MOSFET Q1. Peak currents up to 1.0 A are sourced and sinked by this pin.
8	Gnd	This pin is the control circuitry ground return and is connected back to the source ground.
9	Drive Gnd	This pin is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
10	Drive Output 2	This pin directly drives the gate of a power MOSFET Q2. Peak currents up to 1.0 A are sourced and sinked by this pin.
11	Current Sense 2	A voltage proportional to inductor current is connected to this input. PWM 2 uses this information to terminate conduction of output switch Q2.
12	Compensation 2	This pin is the output of Error Amplifier 2 and is made available for loop compensation.
13	Voltage Feedback 2	This pin in the inverting input of Error Amplifier 2. It is normally connected to the switching power supply output through a resistor divider.
14	Drive Output 2 Enable	A logic low at this input disables Drive Output 2.
15	V_{ref}	This is the 5.0 V reference output. It can provide bias for any additional system circuitry.
16	V_{CC}	This pin is the positive supply of the control IC. The minimum operating voltage range after start-up is 11 V to 15.5 V.

MOTOROLA

MC34129
MC33129

Advance Information

HIGH PERFORMANCE CURRENT MODE CONTROLLER

SILICON MONOLITHIC INTEGRATED CIRCUIT

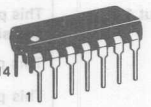
HIGH PERFORMANCE CURRENT MODE CONTROLLER

The MC34129 series are high performance current mode switching regulators specifically designed for use in low power digital telephone applications. These integrated circuits feature a unique internal fault timer that provides automatic restart for overload recovery. For enhanced system efficiency, a start/run comparator is included to implement bootstrapped operation of V_{CC}. Other functions contained are a temperature compensated reference, reference amplifier, fully accessible error amplifier, sawtooth oscillator with sync input, pulse width modulator comparator, and a high current totem pole driver ideally suited for driving a power MOSFET.

Also included are protective features consisting of soft-start, undervoltage lockout, cycle-by-cycle current limiting, adjustable dead time, and a latch for single pulse metering.

Although these devices are primarily intended for use in digital telephone systems, they can be used cost effectively in many other applications.

- Current Mode Operation to 300 kHz
- Automatic Feed Forward Compensation
- Latching PWM for Cycle-By-Cycle Current Limiting
- Continuous Retry after Fault Timeout
- Soft-Start with Maximum Peak Switch Current Clamp
- Internally Trimmed 2% Bandgap Reference
- High Current Totem Pole Driver
- Input Undervoltage Lockout
- Low Start-Up and Operating Current
- Direct Interface with Motorola SENSEFET Products

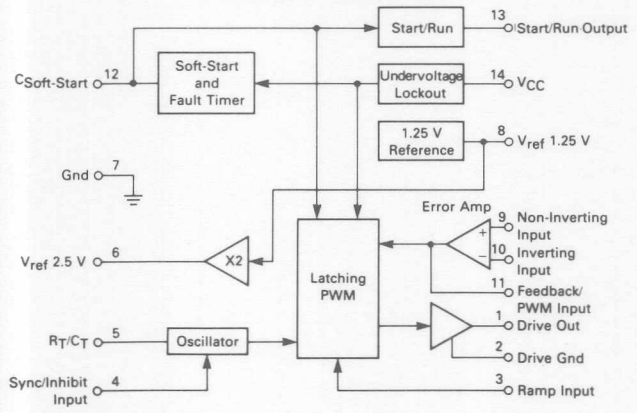


P SUFFIX
PLASTIC PACKAGE
CASE 646-06

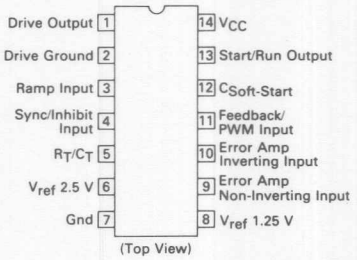


D SUFFIX
PLASTIC PACKAGE
CASE 751A-02
SO-14

SIMPLIFIED BLOCK DIAGRAM



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC34129D	0 to +70°C	SO-14 Plastic DIP
MC34129P	0 to +70°C	Plastic DIP
MC33129D	−40 to +85°C	SO-14 Plastic DIP
MC33129P	−40 to +85°C	Plastic DIP

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATING

Rating	Symbol	Value	Unit
V_{CC} Zener Current	$I_{Z(V_{CC})}$	50	mA
Start/Run Output Zener Current	$I_{Z(Start/Run)}$	50	mA
Analog Inputs (Pins 3, 5, 9, 10, 11, 12)	—	−0.3 to 5.5	V
Sync Input Voltage	V_{sync}	−0.3 to V_{CC}	V
Drive Output Current, Source or Sink	I_{DRV}	1.0	A
Current, Reference Outputs (Pins 6, 8)	I_{ref}	20	mA
Power Dissipation and Thermal Characteristics			
D Suffix Package SO-14 Case 751A-02			
Maximum Power Dissipation @ T_A = 70°C	P_D	552	mW
Thermal Resistance Junction to Air	$R_{\theta JA}$	145	°C/W
P Suffix Package Case 646-06			
Maximum Power Dissipation @ T_A = 70°C	P_D	800	mW
Thermal Resistance Junction to Air	$R_{\theta JA}$	100	°C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_A		°C
MC34129		0 to +70	
MC33129		−40 to +85	
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 10 V, T_A = 25°C [Note 1] unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
REFERENCE SECTIONS					
Reference Output Voltage, T_A = 25°C	V_{ref}				V
1.25 V Ref., I_L = 0 mA		1.225	1.250	1.275	
2.50 V Ref., I_L = 1.0 mA		2.375	2.500	2.625	
Reference Output Voltage, T_A = T_{low} to T_{high}	V_{ref}				V
1.25 V Ref., I_L = 0 mA		1.200	—	1.300	
2.50 V Ref., I_L = 1.0 mA		2.250	—	2.750	
Line Regulation (V_{CC} = 4.0 V to 12 V)	Reg_{line}				mV
1.25 V Ref., I_L = 0 mA		—	2.0	12	
2.50 V Ref., I_L = 1.0 mA		—	10	50	
Load Regulation	Reg_{load}				mV
1.25 V Ref., I_L = −10 to +500 μA		—	1.0	12	
2.50 V Ref., I_L = −0.1 to +1.0 mA		—	3.0	25	
ERROR AMPLIFIER					
Input Offset Voltage (V_{in} = 1.25 V)	V_{IO}				mV
T_A = 25°C		—	1.5	—	
T_A = T_{low} to T_{high}		—	—	10	
Input Offset Current (V_{in} = 1.25 V)	I_{IO}	—	10	—	nA
Input Bias Current (V_{in} = 1.25 V)	I_{IB}				nA
T_A = 25°C		—	25	—	
T_A = T_{low} to T_{high}		—	—	200	
Input Common-Mode Voltage Range	V_{ICR}	—	0.5 to 5.5	—	V
Open-Loop Voltage Gain (V_O = 1.25 V)	A_{VOL}	65	87	—	dB
Gain Bandwidth Product (V_O = 1.25 V, f = 100 kHz)	GBW	500	750	—	kHz
Power Supply Rejection Ratio (V_{CC} = 5.0 to 10 V)	PSRR	65	85	—	dB
Output Source Current (V_O = 1.5 V)	I_{Source}	40	80	—	μA
Output Voltage Swing					V
High State (I_{Source} = 0 μA)	V_{OH}	1.75	1.96	2.25	
Low State (I_{Sink} = 500 μA)	V_{OL}	—	0.1	0.15	

Note 1. T_{low} = 0°C for MC34129 = −40°C for MC33129 T_{high} = +70°C for MC34129 = +85°C for MC33129

ELECTRICAL CHARACTERISTICS (V_{CC} = 10 V, T_A = 25°C [Note 1] unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
PWM COMPARATOR					
Input Offset Voltage (V_{in} = 1.25 V)	V_{IO}	150	275	400	mV
Input Bias Current	I_{IB}	—	−120	−250	μA
Propagation Delay, Ramp Input to Drive Output	$t_{PLH(IN/DRV)}$	—	250	—	ns
SOFT-START					
Capacitor Charge Current (Pin 12 = 0 V)	I_{chg}	0.75	1.2	1.50	μA
Buffer Input Offset Voltage (V_{in} = 1.25 V)	V_{IO}	—	15	40	mV
Buffer Output Voltage (I_{Sink} = 100 μA)	V_{OL}	—	0.15	0.225	V
FAULT TIMER					
Restart Delay Time	t_{DLY}	200	400	600	μs
START/RUN COMPARATOR					
Threshold Voltage (Pin 12)	V_{th}	—	2.0	—	V
Threshold Hysteresis Voltage (Pin 12)	V_H	—	350	—	mV
Output Voltage (I_{Sink} = 500 μA)	V_{OL}	9.0	10	10.3	V
Output Off-State Leakage Current (V_{OH} = 15 V)	$I_{S/R(leak)}$	—	0.4	2.0	μA
Output Zener Voltage (I_Z = 10 mA)	V_Z	—	(V_{CC} + 7.6)	—	V
OSCILLATOR					
Frequency (R_T = 25.5 kΩ, C_T = 390 pF)	f_{OSC}	80	100	120	kHz
Capacitor C_T Discharge Current (Pin 5 = 1.2 V)	I_{dischg}	240	350	460	μA
Sync Input Current					μA
High State (V_{in} = 2.0 V)	I_{IH}	—	40	125	
Low State (V_{in} = 0.8 V)	I_{IL}	—	15	35	
Sync Input Resistance	R_{in}	12.5	32	50	kΩ
DRIVE OUTPUT					
Output Voltage					V
High State (I_{Source} = 200 mA)	V_{OH}	8.3	8.9	—	
Low State (I_{Sink} = 200 mA)	V_{OL}	—	1.4	1.8	
Low State Holding Current	I_H	—	225	—	μA
Output Voltage Rise Time (C_L = 500 pF)	t_r	—	100	—	ns
Output Voltage Fall Time (C_L = 500 pF)	t_f	—	30	—	ns
Output Pull-Down Resistance	R_{PD}	100	225	350	kΩ
UNDERVOLTAGE LOCKOUT					
Start-Up Threshold	V_{th}	3.0	3.6	4.2	V
Hysteresis	V_H	5.0	10	15	%
TOTAL DEVICE					
Power Supply Current R_T = 25.5 kΩ, C_T = 390 pF, C_L = 500 pF	I_{CC}	1.0	2.5	4.0	mA
Power Supply Zener Voltage (I_Z = 10 mA)	V_Z	12	14.3	—	V

Note 1. T_{low} = 0°C for MC34129 = −40°C for MC33129 T_{high} = +70°C for MC34129 = +85°C for MC33129

FIGURE 1 — TIMING RESISTOR versus OSCILLATOR FREQUENCY

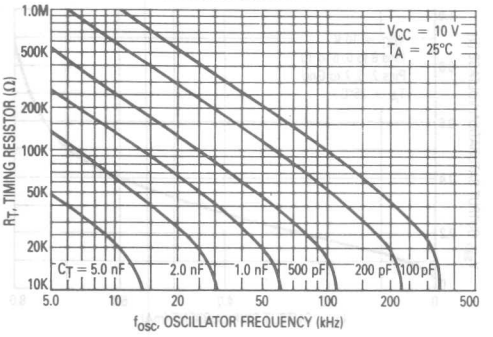


FIGURE 2 — OUTPUT DEAD-TIME versus OSCILLATOR FREQUENCY

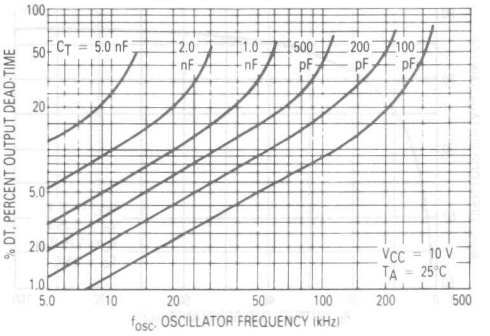


FIGURE 3 — OSCILLATOR FREQUENCY CHANGE versus TEMPERATURE

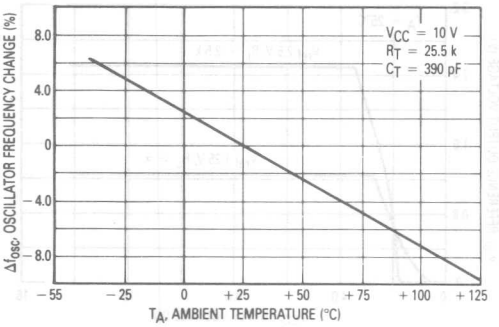


FIGURE 4 — ERROR AMP OPEN-LOOP GAIN AND PHASE versus FREQUENCY

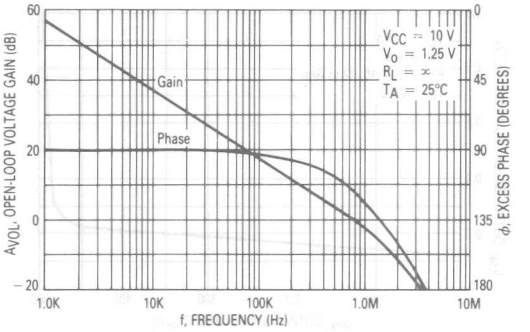


FIGURE 5 — ERROR AMP SMALL-SIGNAL TRANSIENT RESPONSE

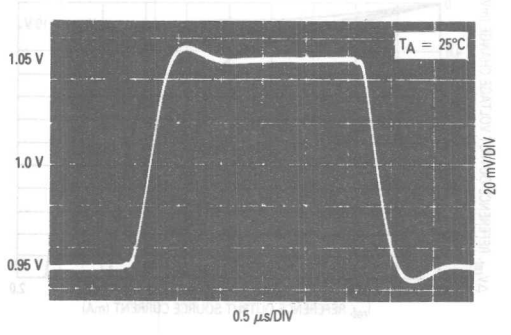
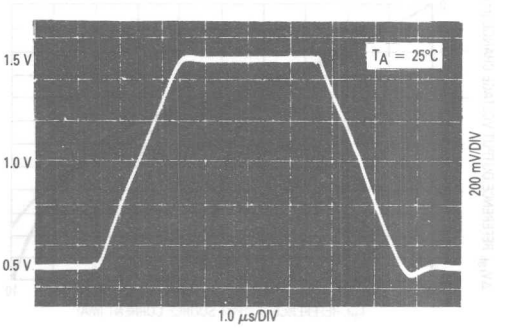


FIGURE 6 — ERROR AMP LARGE-SIGNAL TRANSIENT RESPONSE



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FIGURE 7 — ERROR AMP OPEN-LOOP DC GAIN versus LOAD RESISTANCE

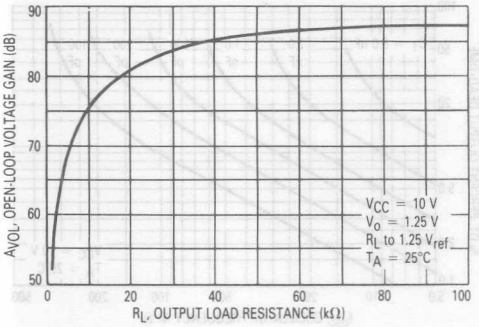


FIGURE 8 — ERROR AMP OUTPUT SATURATION versus SINK CURRENT

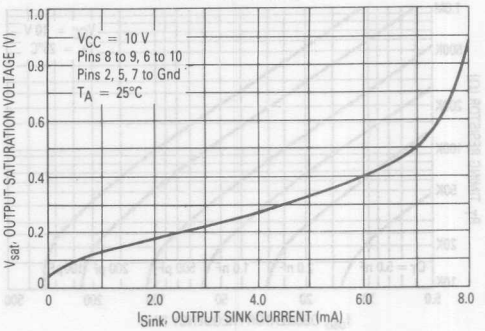


FIGURE 9 — SOFT-START BUFFER OUTPUT SATURATION versus SINK CURRENT

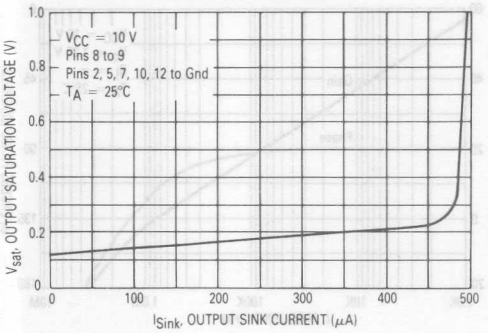


FIGURE 10 — REFERENCE OUTPUT VOLTAGE versus SUPPLY VOLTAGE

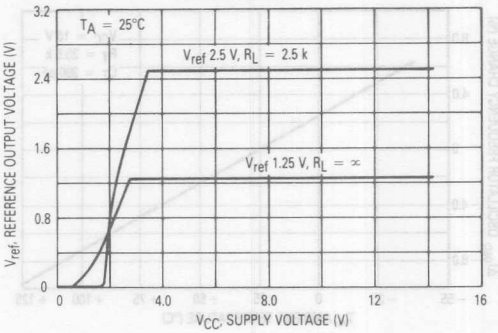


FIGURE 11 — 1.25 V REFERENCE OUTPUT VOLTAGE CHANGE versus SOURCE CURRENT

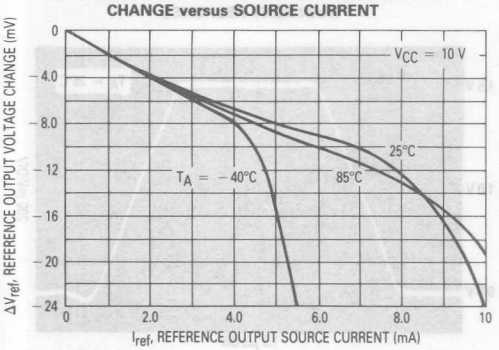


FIGURE 12 — 2.5 V REFERENCE OUTPUT VOLTAGE CHANGE versus SOURCE CURRENT

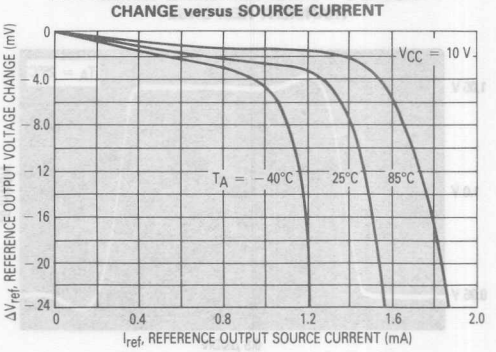


FIGURE 13 — 1.25 V REFERENCE OUTPUT VOLTAGE versus TEMPERATURE

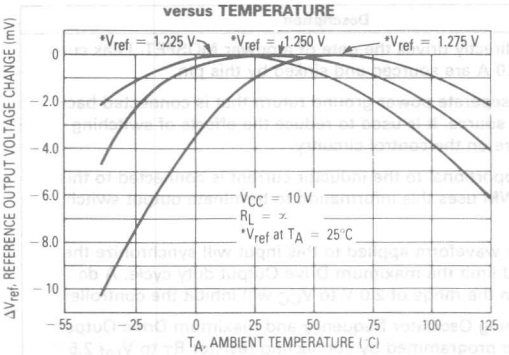


FIGURE 14 — 2.5 V REFERENCE OUTPUT VOLTAGE versus TEMPERATURE

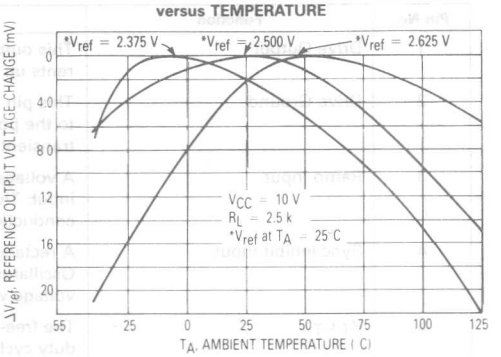


FIGURE 15 — DRIVE OUTPUT SATURATION versus LOAD CURRENT

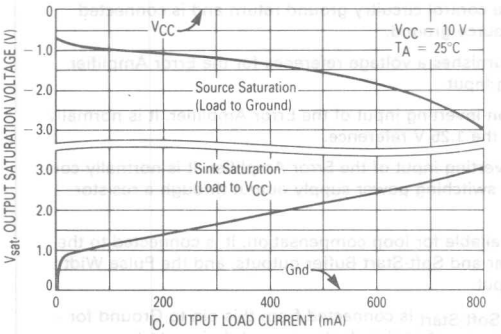


FIGURE 16 — DRIVE OUTPUT WAVEFORM

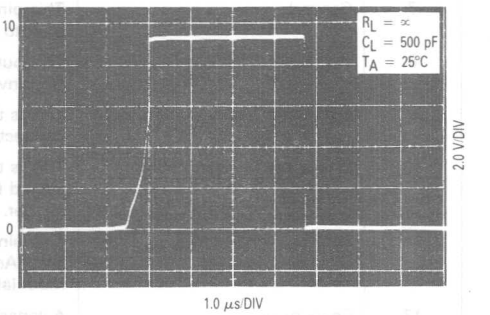
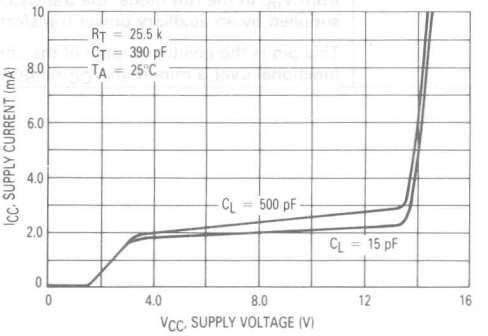


FIGURE 17 — SUPPLY CURRENT versus SUPPLY VOLTAGE



PIN FUNCTION DESCRIPTION

Pin No.	Function	Description
1	Drive Output	This output directly drives the gate of a power MOSFET. Peak currents up to 1.0 A are sourced and sinked by this pin.
2	Drive Ground	This pin is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
3	Ramp Input	A voltage proportional to the inductor current is connected to this input. The PWM uses this information to terminate output switch conduction.
4	Sync/Inhibit Input	A rectangular waveform applied to this input will synchronize the Oscillator and limit the maximum Drive Output duty cycle. A dc voltage within the range of 2.0 V to V_{CC} will inhibit the controller.
5	R_T/C_T	The free-running Oscillator frequency and maximum Drive Output duty cycle are programmed by connecting resistor R_T to V_{ref} 2.5 V and capacitor C_T to Ground. Operation to 300 kHz is possible.
6	V_{ref} 2.50 V	This output is derived from V_{ref} 1.25 V. It provides charging current for capacitor C_T through resistor R_T.
7	Ground	This pin is the control circuitry ground return and is connected back to the source ground.
8	V_{ref} 1.25 V	This output furnishes a voltage reference for the Error Amplifier Non-Inverting Input.
9	Error Amp Non-Inverting Input	This is the non-inverting input of the Error Amplifier. It is normally connected to the 1.25 V reference.
10	Error Amp Inverting Input	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
11	Feedback/PWM Input	This pin is available for loop compensation. It is connected to the Error Amplifier and Soft-Start Buffer outputs, and the Pulse Width Modulator input.
12	$C_{Soft\text{-}Start}$	A capacitor $C_{Soft\text{-}Start}$ is connected from this pin to Ground for a controlled ramp-up of peak inductor current during start-up.
13	Start/Run Output	This output controls the state of an external bootstrap transistor. During the start mode, operating bias is supplied by the transistor from V_{in}. In the run mode, the transistor is switched off and bias is supplied by an auxiliary power transformer winding.
14	V_{CC}	This pin is the positive supply of the control IC. The controller is functional over a minimum V_{CC} range of 4.2 V to 12 V.

OPERATING DESCRIPTION

The MC34129 series are high performance current mode switching regulator controllers specifically designed for use in low power telecommunication applications. Implementation will allow remote digital telephones and terminals to shed their power cords and derive operating power directly from the twisted pair used for data transmission. Although these devices are primarily intended for use in digital telephone systems, they can be used cost effectively in a wide range of converter applications. A representative block diagram is shown in Figure 18.

OSCILLATOR

The oscillator frequency is programmed by the values selected for the timing components R_T and C_T. Capacitor C_T is charged from the 2.5 V reference through resistor R_T to approximately 1.25 V and discharged by an internal current sink to ground. During the discharge of C_T, the oscillator generates an internal blanking pulse that holds the lower input of the NOR gate high. This causes the Drive Output to be in a low state, thus producing a controlled amount of output deadtime. Figure 1 shows Oscillator Frequency versus R_T and Figure 2, Output Deadtime versus Frequency, both for given values of C_T. Note that many values of R_T and C_T will give the same oscillator frequency but only one combination will yield a specific output deadtime at a given frequency. In many noise sensitive applications it may be desirable to frequency-lock one or more switching regulators to an external system clock. This can be accomplished by applying the clock signal to the Sync/Inhibit Input. For reliable locking, the free-running oscillator frequency should be about 10% less than the clock frequency. Referring to the timing diagram shown in Figure 19, the rising edge of the clock signal applied to the Sync/Inhibit Input, terminates charging of C_T and Drive Output conduction. By tailoring the clock waveform, accurate duty cycle clamping of the Drive Output can be achieved. A circuit method is shown in Figure 20. The Sync/Inhibit Input may also be used as a means for system shutdown by applying a dc voltage that is within the range of 2.0 V to V_{CC}.

PWM COMPARATOR AND LATCH

The MC34129 operates as a current mode controller whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches a threshold level established by the output of the Error Amp or Soft-Start Buffer (Pin 11). Thus the error signal controls the peak inductor current on a cycle-by-cycle basis. The PWM Comparator-Latch configuration used, ensures that only a single pulse appears at the Drive Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting the ground-referenced resistor R_S in series with the source of output switch Q_1. The Ramp Input adds an offset of 275 mV to this voltage to guarantee that no pulses appear at the Drive Output when Pin 11 is at its lowest state. This occurs at the beginning of the soft-start interval or when the power supply is operating and the load is removed. The peak inductor current under normal operating conditions is controlled by the voltage at Pin 11 where:

$$I_{pk} = \frac{V_{(Pin\ 11)} - 0.275\ V}{R_S}$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the voltage at Pin 11 will be internally clamped to 1.95 V by the output of the Soft-Start Buffer. Therefore the maximum peak switch current is:

$$I_{pk(max)} = \frac{1.95\ V - 0.275}{R_S} = \frac{1.675\ V}{R_S}$$

When designing a high power switching regulator it becomes desirable to reduce the internal clamp voltage in order to keep the power dissipation of R_S to a reasonable level. A simple method which adjusts this voltage in discrete increments is shown in Figure 22. This method is possible because the Ramp Input bias current is always negative (typically $-120\ \mu A$). A positive temperature coefficient equal to that of the diode string will be exhibited by $I_{pk(max)}$. An adjustable method that is more precise and temperature stable is shown in Figure 23. Erratic operation due to noise pickup can result if there is an excessive reduction of the clamp voltage. In this situation, high frequency circuit layout techniques are imperative.

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Ramp Input with a time constant that approximates the spike duration will usually eliminate the instability; refer to Figure 25.

ERROR AMP AND SOFT-START BUFFER

A fully-compensated Error Amplifier with access to both inputs and output is provided for maximum design flexibility. The Error Amplifier output is common with that of the Soft-Start Buffer. These outputs are open-collector (sink only) and are ORed together at the inverting input of the PWM Comparator. With this configuration, the amplifier that demands lower peak inductor current dominates control of the loop. Soft-start is mandatory for stable start-up when power is provided through a high source impedance such as the long twisted pair used in telecommunications. It effectively removes the load from the output of the switching power supply upon initial start-up. The Soft-Start Buffer is configured as a unity gain follower with the non-inverting input connected to Pin 12. An internal 1.0 μA

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FIGURE 18 — REPRESENTATIVE BLOCK DIAGRAM

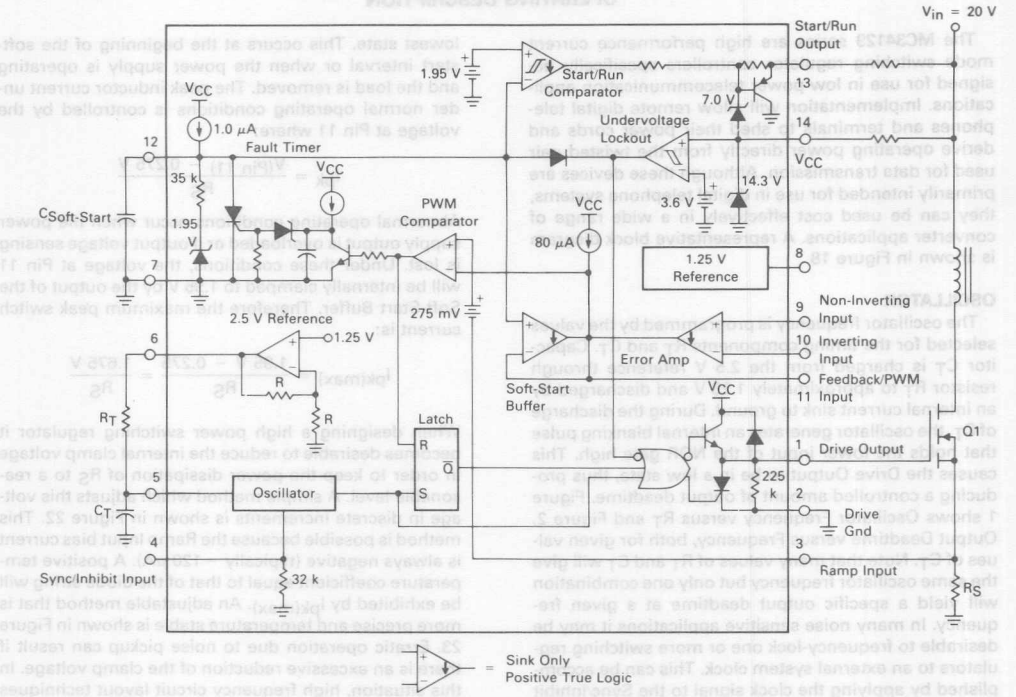
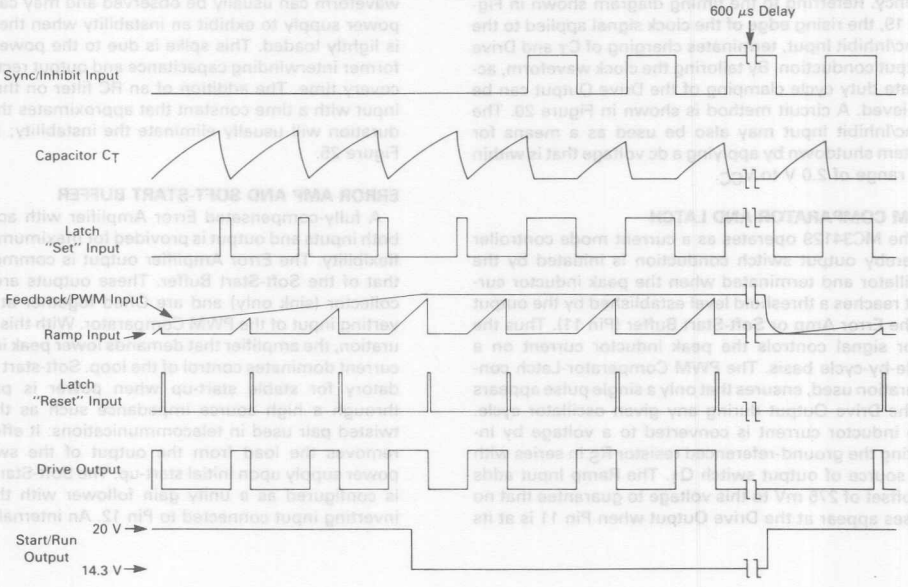


FIGURE 19 — TIMING DIAGRAM



OPERATING DESCRIPTION (continued)

current source charges the soft-start capacitor ($C_{Soft-Start}$) to an internally clamped level of 1.95 V. The rate of change of peak inductor current, during start-up, is programmed by the capacitor value selected. Either the Fault Timer or the Undervoltage Lockout can discharge the soft-start capacitor.

FAULT TIMER

This unique circuit prevents sustained operation in a lockout condition. This can occur with conventional switching control IC's when operating from a power source with a high series impedance. If the power required by the load is greater than that available from the source, the input voltage will collapse, causing the lockout condition. The Fault Timer provides automatic recovery when this condition is detected. Under normal operating conditions, the output of the PWM Comparator will reset the Latch and discharge the internal Fault Timer capacitor on a cycle-by-cycle basis. Under operating conditions where the required power into the load is greater than that available from the source (V_{in}), the Ramp Input voltage (plus offset) will not reach the comparator threshold level (Pin 11), and the output of the PWM Comparator will remain low. If this condition persists for more than 600 μs, the Fault Timer will activate, discharging $C_{Soft-Start}$ and initiating a soft-start cycle. The power supply will operate in a skip cycle or hiccup mode until either the load power or source impedance is reduced. The minimum fault timeout is 200 μs, which limits the useful switching frequency to a minimum of 5.0 kHz.

START/RUN COMPARATOR

A bootstrap start-up circuit is included to improve system efficiency when operating from a high input voltage. The output of the Start/Run Comparator controls the state of an external transistor. A typical application is shown in Figure 21. While $C_{Soft-Start}$ is charging, start-up bias is supplied to V_{CC} (Pin 14) from V_{in} through transistor Q2. When $C_{Soft-Start}$ reaches the 1.95 V clamp level, the Start-Run output switches low (V_{CC} – 50 mV), turning off Q2. Operating bias is now derived from the auxiliary bootstrap winding of the transformer, and all drive power is efficiently converted down from V_{in}. The start time must be long enough for the power supply output to reach regulation. This will ensure that there is sufficient bias voltage at the auxiliary bootstrap winding for sustained operation.

$$t_{Start} = \frac{1.95\ V\ C_{Soft-Start}}{1.0\ \mu A} = 1.95\ C_{Soft-Start\ in\ \mu F}$$

The Start/Run Comparator has 350 mV of hysteresis. The output off-state is clamped to V_{CC} + 7.6 V by the internal zener and PNP transistor base-emitter junction.

DRIVE OUTPUT AND DRIVE GROUND

The MC34129 contains a single totem-pole output stage that was specifically designed for direct drive of power MOSFETs. It is capable of up to ±1.0 A peak drive current and has a typical fall time of 30 ns with a 500 pF load. The totem-pole stage consists of an NPN transistor for turn-on drive and a high speed SCR for turn-off. The SCR design requires less average supply current (I_{CC}) when compared to conventional switching control IC's that use an all NPN totem-pole. The SCR accomplishes this during turn-off of the MOSFET, by utilizing the gate charge as regenerative on-bias, whereas the conventional all transistor design requires continuous base current. Conversion efficiency in low power applications is greatly enhanced with this reduction of I_{CC}. The SCR's low-state holding current (I_H) is typically 225 μA. An internal 225 kΩ pull-down resistor is included to shunt the Drive Output off-state leakage to ground when the Undervoltage Lockout is active. A separate Drive Ground is provided to reduce the effects of switching transient noise imposed on the Ramp Input. This feature becomes particularly useful when the $I_{pk(max)}$ clamp level is reduced. Figure 24 shows the proper implementation of the MC34129 with a current sensing power MOSFET.

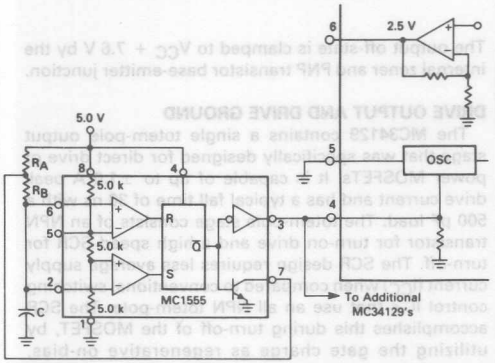
UNDERVOLTAGE LOCKOUT

The Undervoltage Lockout comparator holds the Drive Output and $C_{Soft-Start}$ pins in the low state when V_{CC} is less than 3.6 V. This ensures that the MC34129 is fully functional before the output stage is enabled and a soft-start cycle begins. A built-in hysteresis of 350 mV prevents erratic output behavior as V_{CC} crosses the comparator threshold voltage. A 14.3 V zener is connected as a shunt regulator from V_{CC} to ground. Its purpose is to protect the MOSFET gate from excessive drive voltage during system start-up. An external 9.1 V zener is required when driving low threshold MOSFETs. Refer to Figure 21. The minimum operating voltage range of the IC is 4.2 V to 12 V.

REFERENCES

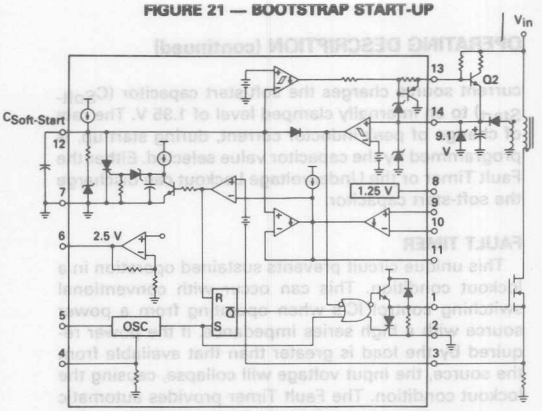
The 1.25 V bandgap reference is trimmed to ±2.0% tolerance at T_A = 25°C. It is intended to be used in conjunction with the Error Amp. The 2.50 V reference is derived from the 1.25 V reference by an internal op amp with a fixed gain of 2.0. It has an output tolerance of ±5.0% at T_A = 25°C and its primary purpose is to supply charging current to the oscillator timing capacitor.

FIGURE 20 — EXTERNAL DUTY CYCLE CLAMP AND MULTI UNIT SYNCHRONIZATION



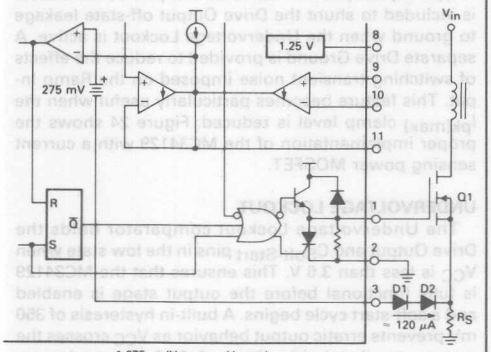
$$f = \frac{1.44}{(R_A + 2R_B)C} \qquad D_{max} = \frac{R_B}{R_A + 2R_B}$$

FIGURE 21 — BOOTSTRAP START-UP



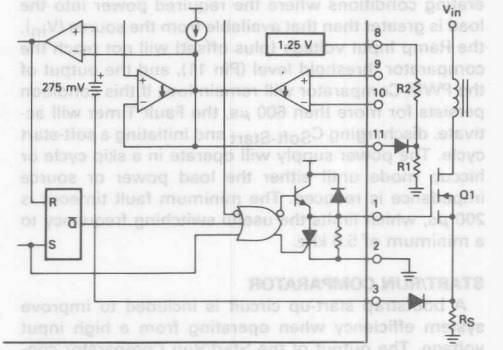
The external 9.1 V zener is required when driving low threshold MOSFETs.

FIGURE 22 — DISCRETE STEP REDUCTION OF CLAMP LEVEL



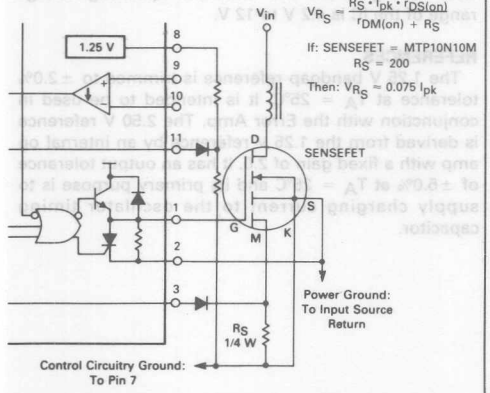
$$I_{pk(max)} = \frac{1.675 - (V_{F(D1)} + V_{F(D2)})}{R_S}$$

FIGURE 23 — ADJUSTABLE REDUCTION OF CLAMP LEVEL



If: $\frac{1.25\ V}{R1 + R2} \geq 1.0\ mA$ Then: $I_{pk(max)} \approx \frac{1.25}{\left(\frac{R2}{R1} + 1\right)} - 0.275$ / R_S

FIGURE 24 — CURRENT SENSING POWER MOSFET

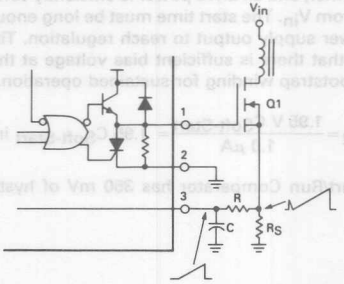


$$V_{R_S} \approx \frac{R_S \cdot I_{pk} \cdot r_{DS(on)}}{r_{DM(on)} + R_S}$$

If: SENSEFET = MTP10N10M
R_S = 200
Then: $V_{R_S} \approx 0.075\ I_{pk}$

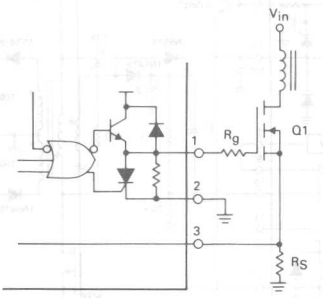
Virtually lossless current sensing can be achieved with the implementation of a SENSEFET power switch.

FIGURE 25 — CURRENT WAVEFORM SPIKE SUPPRESSION



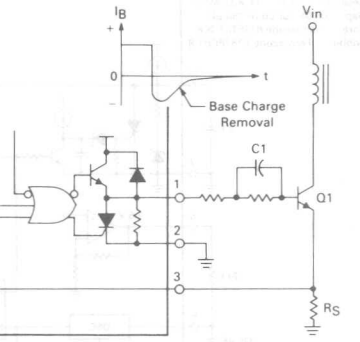
The addition of the RC filter will eliminate instability caused by the leading edge spike on the current waveform.

FIGURE 26 — MOSFET PARASITIC OSCILLATIONS



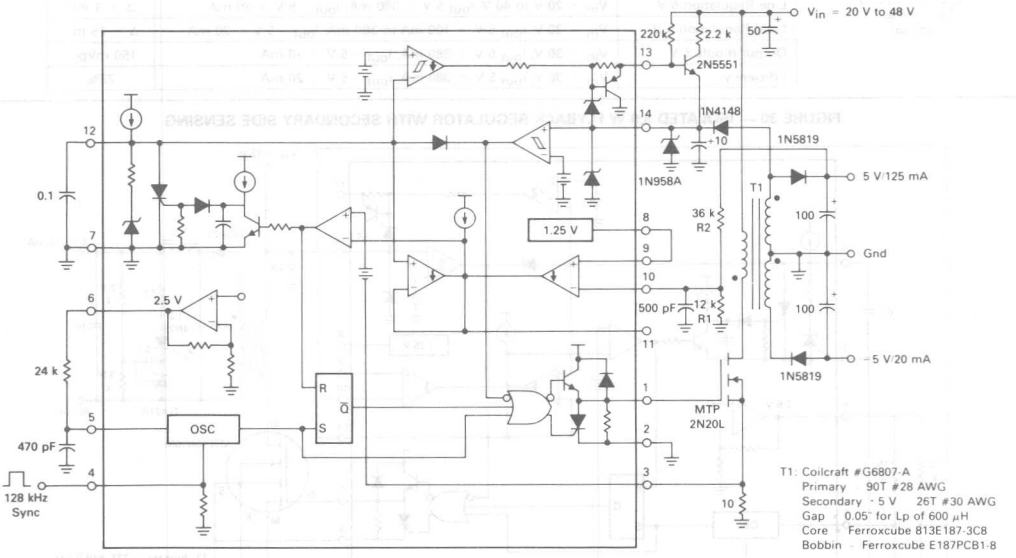
Series gate resistor R_g will damp any high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate-source circuit.

FIGURE 27 — BIPOLAR TRANSISTOR DRIVE



The totem-pole output can furnish negative base current for enhanced transistor turn-off, with the addition of capacitor C1.

FIGURE 28 — NON-ISOLATED 725 mW FLYBACK REGULATOR



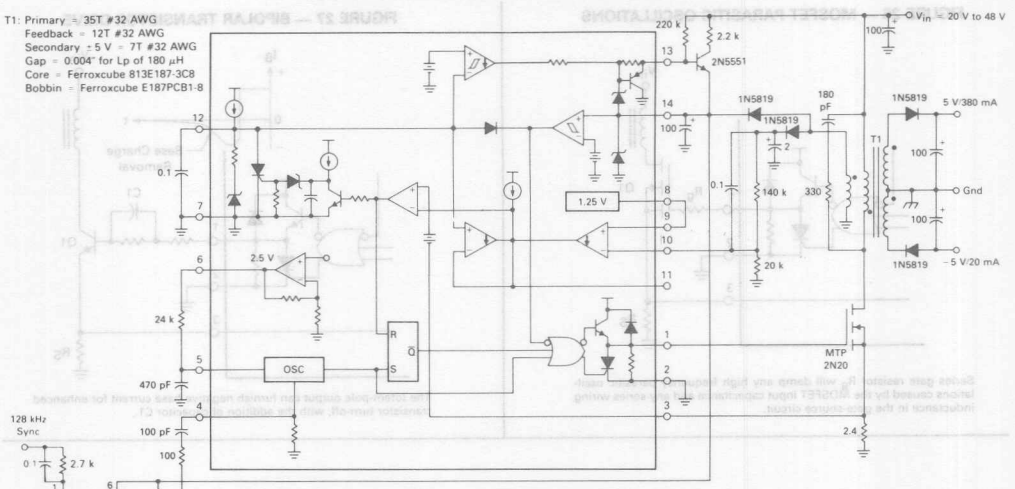
T1: Coilcraft #G6807-A
Primary 90T #28 AWG
Secondary - 5 V 26T #30 AWG
Gap 0.05" for Lp of 600 μH
Core Ferroxcube 813E187-3C8
Bobbin Ferroxcube E187PCB1-8

Test	Conditions	Results
Line Regulation 5 V	V_{in} = 20 V to 40 V, I_{out} 5 V = 125 mA, I_{out} −5 V = 20 mA	Δ = 1.0 mV
Load Regulation 5 V	V_{in} = 30 V, I_{out} 5 V = 0 mA to 150 mA, I_{out} −5 V = 20 mA	Δ = 2.0 mV
Output Ripple 5 V	V_{in} = 30 V, I_{out} 5 V = 125 mA, I_{out} −5 V = 20 mA	150 mVp-p
Efficiency	V_{in} = 30 V, I_{out} 5 V = 125 mA, I_{out} −5 V = 20 mA	77%

$$V_{out} = 1.25\left(\frac{R2}{R1} + 1\right)$$

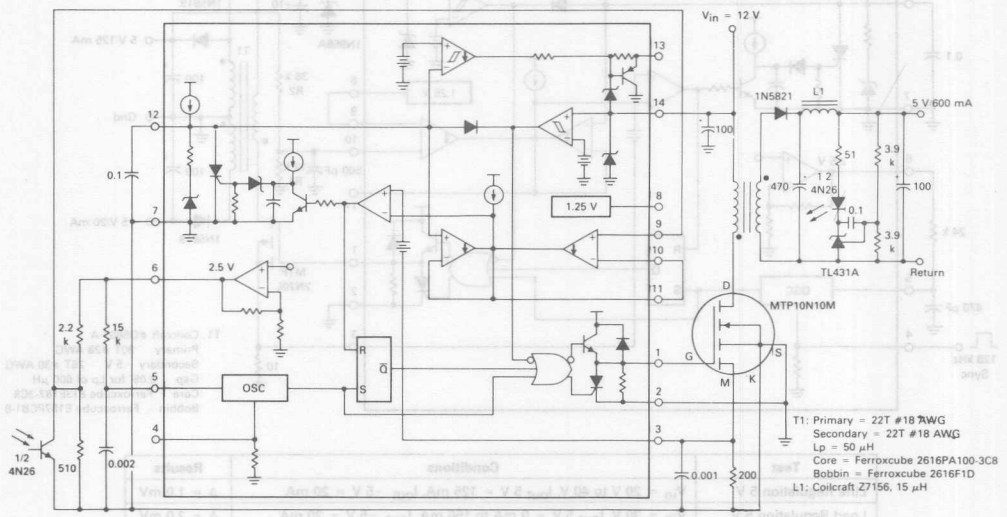
3

FIGURE 29 — ISOLATED 2.0 W FLYBACK REGULATOR



Test	Conditions	Results
Line Regulation 5 V	V_{in} = 20 V to 40 V, I_{out} 5 V = 380 mA, I_{out} −5 V = 20 mA	Δ = 1 mV
Load Regulation 5 V	V_{in} = 30 V, I_{out} 5 V = 100 mA to 380 mA, I_{out} −5 V = 20 mA	Δ = 15 mV
Output Ripple 5 V	V_{in} = 30 V, I_{out} 5 V = 380 mA, I_{out} −5 V = 20 mA	150 mVp-p
Efficiency	V_{in} = 30 V, I_{out} 5 V = 380 mA, I_{out} −5 V = 20 mA	73%

FIGURE 30 — ISOLATED 3.0 W FLYBACK REGULATOR WITH SECONDARY SIDE SENSING



Test	Conditions	Results
Line Regulation	V_{in} = 8 V to 12 V, I_{out} 600 mA	Δ = 1 mV
Load Regulation	V_{in} = 12 V, I_{out} = 100 mA to 600 mA	Δ = 8 mV
Output Ripple	V_{in} = 12 V, I_{out} = 600 mA	20 mVp-p
Efficiency	V_{in} = 12 V, I_{out} = 600 mA	81%

An economical method of achieving secondary sensing is to combine the TL431A with a 4N26 optocoupler.

MOTOROLA

MC34160
MC33160

Product Preview

MICROPROCESSOR VOLTAGE REGULATOR AND SUPERVISORY CIRCUIT

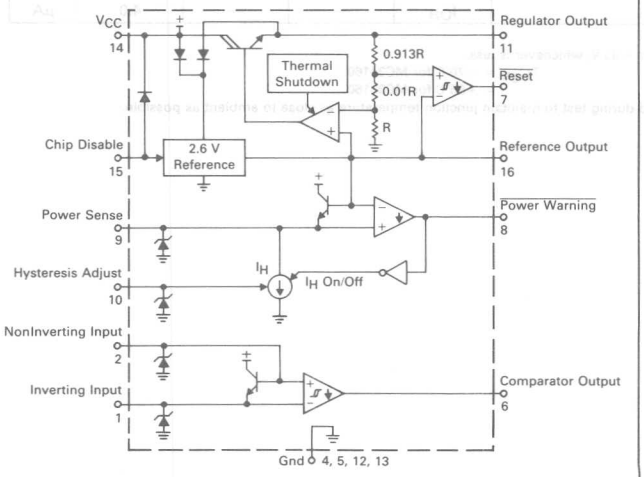
The MC34160 Series is a voltage regulator and supervisory circuit containing many of the necessary monitoring functions required in microprocessor based systems. It is specifically designed for appliance and industrial applications, offering the designer a cost effective solution with minimal external components. These integrated circuits feature a 5.0 V/100 mA regulator with short circuit current limiting, pinned out 2.6 V bandgap reference, low voltage reset comparator, power warning comparator with programmable hysteresis, and an uncommitted comparator ideally suited for microprocessor line synchronization.

Additional features include a chip disable input for low standby current, and internal thermal shutdown for over temperature protection.

These devices are contained in a 16 pin dual-in-line heat tab plastic package for improved thermal conduction.

- 5.0 Volt Regulator Output Current in Excess of 100 mA
- Internal Short Circuit Current Limiting
- Pinned Out 2.6 V Reference
- Low Voltage Reset Comparator
- Power Warning Comparator with Programmable Hysteresis
- Uncommitted Comparator
- Low Standby Current
- Internal Thermal Shutdown Protection
- Heat Tab Power Package

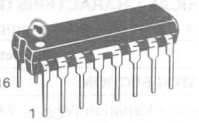
REPRESENTATIVE BLOCK DIAGRAM



This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

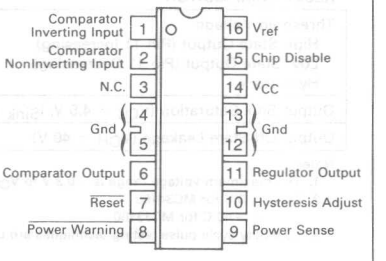
MICROPROCESSOR VOLTAGE REGULATOR/ SUPERVISORY CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 648C-02

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC34160P	0°C to +70°C	Plastic DIP
MC33160P	−40°C to +85°C	Plastic DIP

MAXIMUM RATING

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	V
Chip Disable Input Voltage (Pin 15, Note 1)	V_{CD}	−0.3 to V_{CC}	V
Comparator Input Current (Pin 1, 2, 9)	I_{in}	−2.0 to +2.0	mA
Comparator Output Voltage (Pin 6, 7, 8)	V_O	40	V
Comparator Output Sink Current (Pin 6, 7, 8)	I_{Sink}	10	mA
Power Dissipation and Thermal Characteristics Maximum Power Dissipation @ T_A = 70°C Thermal Resistance Junction to Air Thermal Resistance Junction to Case (Pin 4, 5, 12, 13)	 P_D $R_{\theta JA}$ $R_{\theta JC}$	 1000 80 15	 mW °C/W °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature MC34160 MC33160	T_A	 0 to +70 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 30 V, I_O = 10 mA, I_{ref} = 100 μA) For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Notes 2 and 3] unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
REGULATOR SECTION					
Total Output Variation (V_{CC} = 7.0 V to 40 V, I_O = 1.0 mA to 100 mA, T_A = T_{low} to T_{high})	V_O	4.75	5.0	5.25	V
Line Regulation (V_{CC} = 7.0 V to 40 V, T_A = 25°C)	Reg_{line}	—	5.0	40	mV
Load Regulation (I_O = 1.0 mA to 100 mA, T_A = 25°C)	Reg_{load}	—	20	50	mV
Ripple Rejection (V_{CC} = 25 V to 35 V, I_O = 40 mA, f = 120 Hz, T_A = 25°C)	RR	50	65	—	dB
REFERENCE SECTION					
Total Output Variation (V_{CC} = 7.0 V to 40 V, I_O = 0.1 mA to 2.0 mA, T_A = T_{low} to T_{high})	V_{ref}	2.47	2.6	2.73	V
Line Regulation (V_{CC} = 5.0 V to 40 V, T_A = 25°C)	Reg_{line}	—	2.0	20	mV
Load Regulation (I_O = 0.1 mA to 2.0 mA, T_A = 25°C)	Reg_{load}	—	4.0	30	mV
RESET COMPARATOR					
Threshold Voltage High State Output (Pin 11 Increasing) Low State Output (Pin 11 Decreasing) Hysteresis	 V_{IH} V_{IL} V_H	 — 4.55 0.02	 (V_O − 0.11) (V_O − 0.18) 0.07	 (V_O − 0.05) — —	V
Output Sink Saturation (V_{CC} = 4.5 V, I_{Sink} = 2.0 mA)	V_{OL}	—	—	0.4	V
Output Off-State Leakage (V_{OH} = 40 V)	I_{OH}	—	—	4.0	μA

Notes:
1. The maximum voltage range is −0.3 V to V_{CC} or +35 V, whichever is less.
2. T_{low} = 0°C for MC34160 = −40°C for MC33160 T_{high} = +70°C for MC34160 = +85°C for MC33160
3. Low duty cycle pulse testing techniques are used during test to maintain junction temperature as close to ambient as possible.

ELECTRICAL CHARACTERISTICS — Continued (V_{CC} = 30 V, I_O = 10 mA, I_{ref} = 100 μA) For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Notes 2 and 3] unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER WARNING COMPARATOR					
Input Offset Voltage	V_{IO}	—	1.2	10	mV
Input Bias Current ($V_{Pin\ 9}$ = 3.0 V)	I_{IB}	—	—	0.5	μA
Input Hysteresis Current ($V_{Pin\ 9}$ = V_{ref} − 100 mV) $R_{Pin\ 10}$ = 24 k $R_{Pin\ 10}$ = ∞	I_H	 40 4.5	 50 7.5	 60 11	 μA
Output Sink Saturation (I_{Sink} = 2.0 mA)	V_{OL}	—	0.13	0.4	V
Output Off-State Leakage (V_{OH} = 40 V)	I_{OH}	—	—	4.0	μA
UNCOMMITTED COMPARATOR					
Input Offset Voltage (Output Transition Low to High)	V_{IO}	—	—	20	mV
Input Hysteresis Voltage (Output Transition High to Low)	I_H	140	200	260	mV
Input Bias Current ($V_{Pin\ 1, 2}$ = 2.6 V)	I_{IB}	—	—	−1.0	μA
Input Common-Mode Voltage Range	V_{ICR}	0.6 to 5.0	—	—	V
Output Sink Saturation (I_{Sink} = 2.0 mA)	V_{OL}	—	0.13	0.4	V
Output Off-State Leakage (V_{OH} = 40 V)	I_{OH}	—	—	4.0	μA
TOTAL DEVICE					
Chip Disable Threshold Voltage (Pin 15) High State (Chip Disabled) Low State (Chip Enabled)	 V_{IH} V_{IL}	 2.5 —	 — —	 — 0.8	V
Chip Disable Input Current (Pin 15) High State (V_{in} = 2.5 V) Low State (V_{in} = 0.8 V)	 I_{IH} I_{IL}	 — —	 — —	 100 30	μA
Chip Disable Input Resistance (Pin 15)	R_{in}	50	100	—	kΩ
Operating Voltage Range V_O (Pin 11) Regulated V_{ref} (Pin 16) Regulated	V_{CC}	 7.0 to 40 5.0 to 40	 — —	 — —	V
Power Supply Current Standby (Chip Disable High State) Operating (Chip Disable Low State)	I_{CC}	 — —	 0.18 1.5	 0.35 3.0	mA

FIGURE 1 — REGULATOR OUTPUT VOLTAGE CHANGE versus SOURCE CURRENT

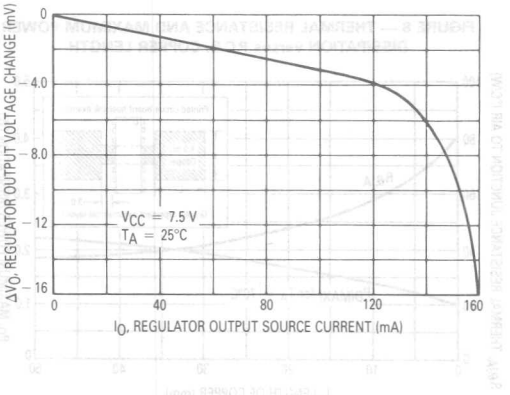
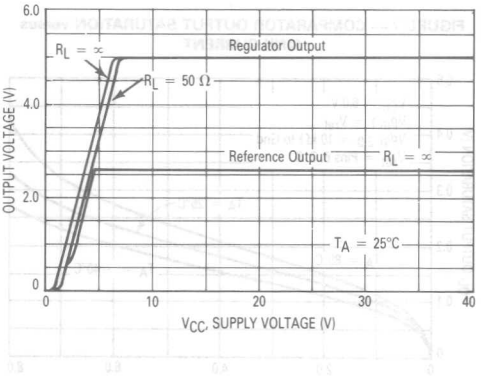


FIGURE 2 — REFERENCE AND REGULATOR OUTPUT versus SUPPLY VOLTAGE



3

FIGURE 3 — REFERENCE OUTPUT VOLTAGE CHANGE versus SOURCE CURRENT

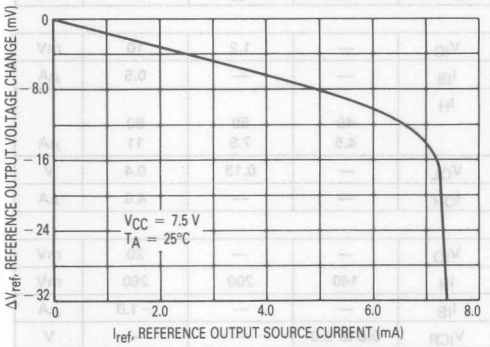


FIGURE 4 — POWER WARNING HYSTERESIS CURRENT versus PROGRAMMING RESISTOR

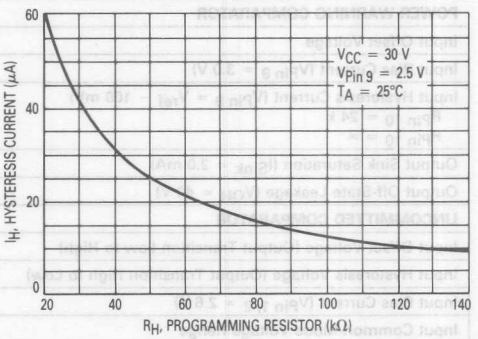


FIGURE 5 — POWER WARNING COMPARATOR DELAY versus TEMPERATURE

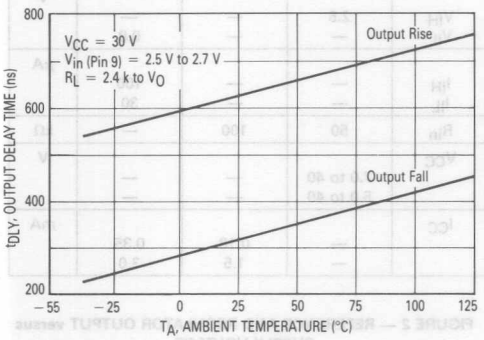


FIGURE 6 — UNCOMMITTED COMPARATOR DELAY versus TEMPERATURE

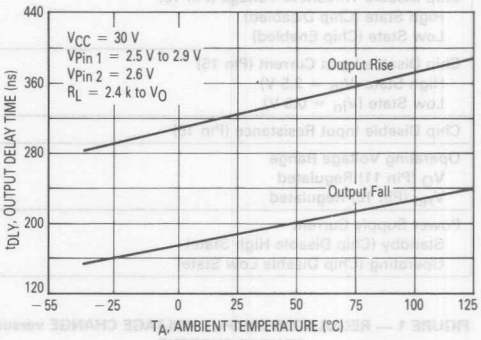


FIGURE 7 — COMPARATOR OUTPUT SATURATION versus SINK CURRENT

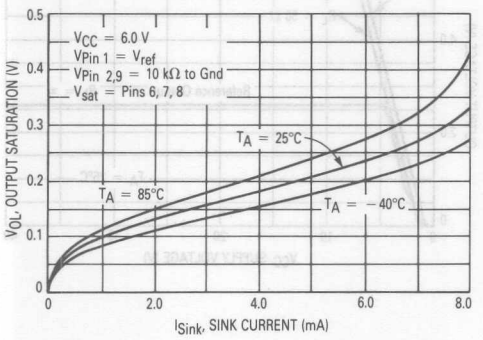
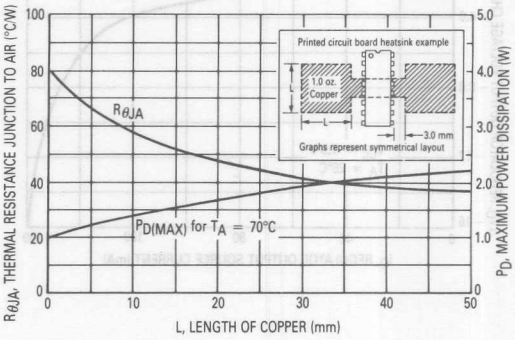


FIGURE 8 — THERMAL RESISTANCE AND MAXIMUM POWER DISSIPATION versus P.C.B. COPPER LENGTH



PIN FUNCTION DESCRIPTION

Pin No.	Function	Description
1	Comparator Inverting Input	This is the Uncommitted Comparator inverting input. It is typically connected to a resistor divider to monitor a voltage.
2	Comparator Noninverting Input	This is the Uncommitted Comparator noninverting input. It is typically connected to a reference voltage.
3	N.C.	No connection. This pin is not internally connected.
4,5,12,13	Gnd	These pins are the control circuit grounds and are connected to the source and load ground returns. They are part of the IC lead frame and can be used for heatsinking.
6	Comparator Output	This is the Uncommitted Comparator output. It is an open collector sink-only output requiring a pull-up resistor.
7	Reset	This is the Reset Comparator output. It is an open collector sink-only output requiring a pull-up resistor.
8	Power Warning	This is the Power Warning Comparator output. It is an open collector sink-only output requiring a pull-up resistor.
9	Power Sense	This is the Power Warning Comparator noninverting input. It is typically connected to a resistor divider to monitor the input power source voltage.
10	Hysteresis Adjust	The Power Warning Comparator hysteresis is programmed by a resistor connected from this pin to ground.
11	Regulator Output	This is the 5.0 V Regulator output.
14	V_{CC}	This pin is the positive supply input of the control IC.
15	Chip Disable	This input is used to switch the IC into a standby mode turning off all outputs.
16	V_{ref}	This is the 2.6 V Reference output. It is intended to be used in conjunction with the Power Warning and Uncommitted comparators.

OPERATING DESCRIPTION

The MC34160 Series is a monolithic voltage regulator and supervisory circuit containing many of the necessary monitoring functions required in microprocessor based systems. It is specifically designed for appliance and industrial applications, offering the designer a cost effective solution with minimal external components. These devices are specified for operation over an input voltage of 7.0 V to 40 V, and with a junction temperature of −40°C to +150°C. A typical microprocessor application is shown in Figure 9.

Regulator

The 5.0 V regulator is designed to source in excess of 100 mA output current and is short circuit protected. The output has a guaranteed tolerance of ±5.0% over line, load, and temperature. Internal thermal shutdown circuitry is included to limit the maximum junction temperature to a safe level. When activated, typically at 170°C, the regulator output turns off.

In specific situations a combination of input and output bypass capacitors may be required for regulator

itor (C_{in}) of 0.33 μF or greater is suggested. Output capacitance values of less than 5.0 nF may cause regulator instability at light load (≤1.0 mA) and cold temperature. An output bypass capacitor of 0.1 μF or greater is recommended to ensure stability under all load conditions. The capacitors selected must provide good high frequency characteristics.

Good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator does not have external sense inputs.

Reference

The 2.6 V bandgap reference is short circuit protected and has a guaranteed output tolerance of ±5.0% over line, load, and temperature. It is intended to be used in conjunction with the Power Warning and Uncommitted Comparator. The reference can source in excess of 2.0 mA and sink a maximum of 10 μA. For additional current sinking capability, an external load resistor to ground must be used.

Reference biasing is internally derived from either V_{CC} or V_O, allowing proper operation if either drops below nominal.

Chip Disable

This input is used to switch the IC into a standby mode. When activated, internal biasing for the entire die is removed causing all outputs to turn off. This reduces the power supply current (I_{CC}) to less than 0.3 mA.

Comparators

Three separate comparators are incorporated for voltage monitoring. Their outputs can provide diagnostic information to the microprocessor, preventing system malfunctions.

The Reset comparator inverting input is internally connected to the 2.6 V reference while the noninverting input monitors V_O. The Reset output is active low when V_O falls approximately 180 mV below its regulated voltage. To prevent erratic operation when crossing the comparator threshold, 70 mV of hysteresis is provided.

The Power Warning comparator is typically used to detect an impending loss of system power. The inverting input is internally connected to the reference, fixing the threshold at 2.6 V. The input power source V_{in} is monitored by the noninverting input through the R_1/R_2 divider (Figure 9). This input features an adjustable 10 μA to 50 μA current sink I_H that is programmed by the value selected for resistor R_H. A default current of 6.5 μA is provided if R_H is omitted. When the comparator input falls below 2.6 V, the current sink is activated. This follows:

$$V_{th(lower)} = V_{ref}\left(1 + \frac{R_1}{R_2}\right) - I_{IB}\,R_1$$

$$V_{th(upper)} = V_{ref}\left(1 + \frac{R_1}{R_2}\right) + I_H\,R_1$$

The nominal hysteresis current I_H equals 1.2 V/R_H (Figure 4).

The Uncommitted Comparator can be used to synchronize the microprocessor with the ac line signal for timing functions, or for synchronous load switching. It can also be connected as a line loss detector as shown in Figure 10. The comparator contains 200 mV of hysteresis preventing erractic output behavior when crossing the input threshold.

The Power Warning and Uncommitted comparators each have a transistor base-emitter connected across their inputs. The base input normally connects to a voltage reference while the emitter input connects to the voltage to be monitored. The transistor limits the negative excursion on the emitter input to −0.7 V below the base input by supplying current from V_{CC}. This clamp current will prevent forward biasing the IC substrate. Zener diodes are connected to the comparator inputs to enhance the IC's electrostatic discharge capability. Resistors R_1 and R_{in} must limit the input current to a maximum of ±2.0 mA.

Each comparator output consists of an open collector NPN transistor capable of sinking 2.0 mA with a saturation voltage less than 0.4 V, and standing off 40 V with minimal leakage. Internal bias for the Reset and Power Warning comparators is derived from either V_{CC} or the regulator output to ensure functionality when either is below nominal.

Heat Tab Package

The MC34160 is contained in a 16 lead plastic dual-in-line package in which the die is mounted on a special Heat Tab copper alloy lead frame. This tab consists of the four center ground pins that are specifically designed to improve thermal conduction from the die to the surrounding air. The pictorial in Figure 8 shows a simple but effective method of utilizing the printed circuit board medium as a heat dissipator by soldering these tabs to an adequate area of copper foil. This permits the use of standard board layout and mounting practices while having the ability to more than halve the junction to air thermal resistance. The example and graph are for a symmetrical layout on a single sided board with one ounce per square foot copper.

FIGURE 9 — TYPICAL MICROPROCESSOR APPLICATION

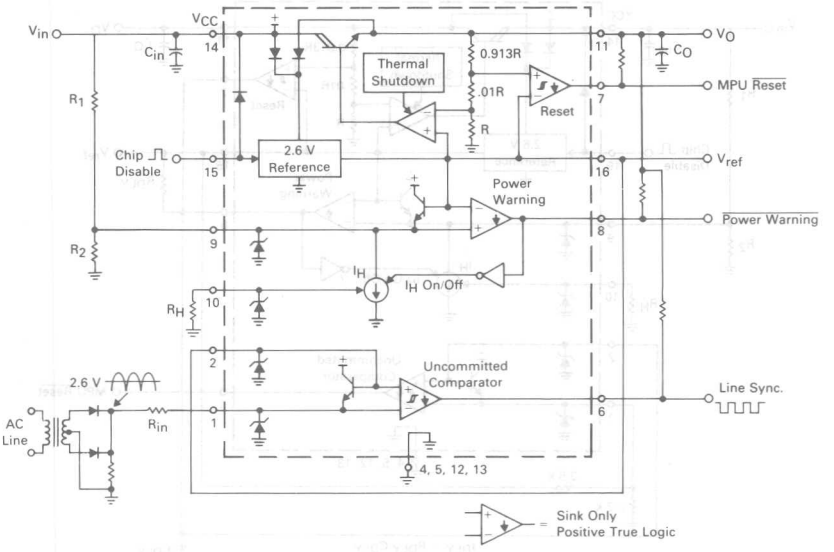
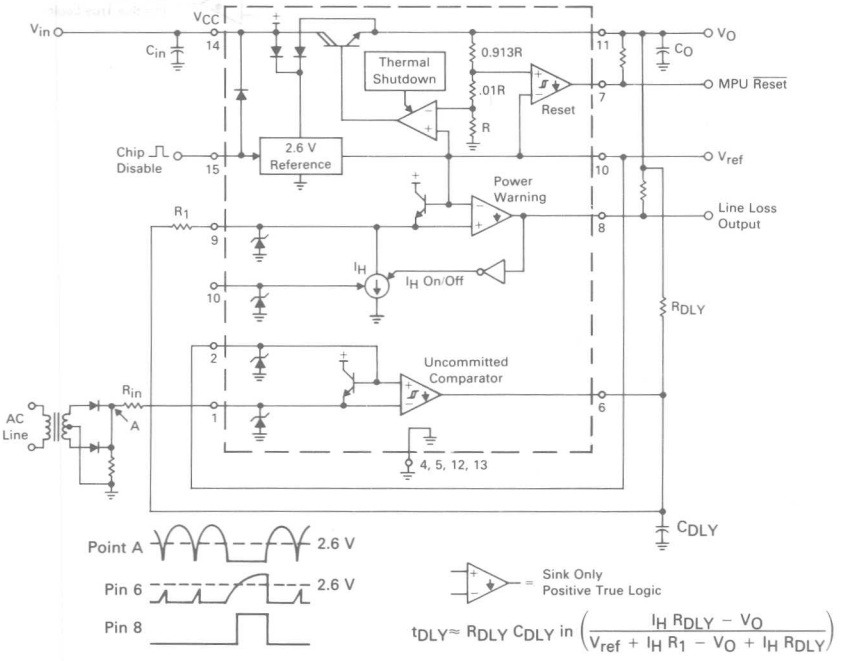


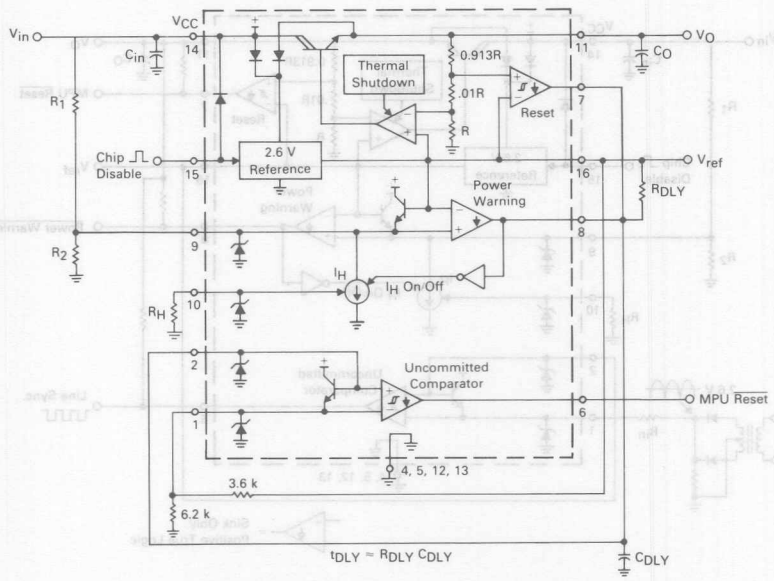
FIGURE 10 — LINE LOSS DETECTOR APPLICATION



$$t_{DLY} \approx R_{DLY}\, C_{DLY}\, \text{in}\left(\frac{I_H R_{DLY} - V_O}{V_{ref} + I_H R_1 - V_O + I_H R_{DLY}}\right)$$

3

FIGURE 11 — TIME DELAYED MICROPROCESSOR RESET



MOTOROLA

SG1525A/SG1527A
SG2525A/SG2527A
SG3525A/SG3527A

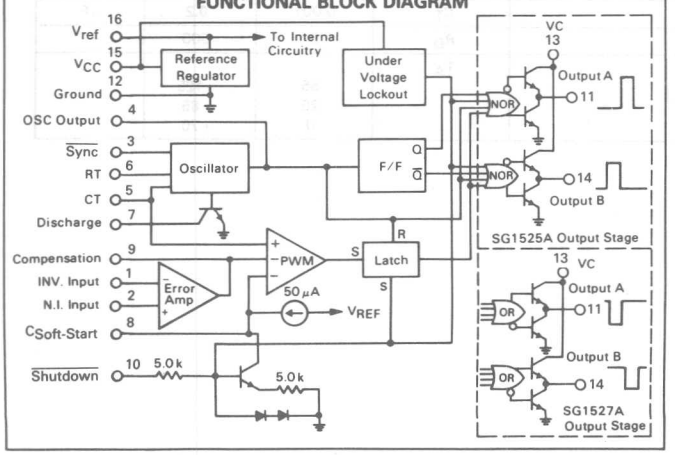
3

PULSE WIDTH MODULATOR CONTROL CIRCUITS

The SG1525A/1527A series of pulse width modulator control-circuits offer improved performance and lower external parts count when implemented for controlling all types of switching power supplies. The on-chip +5.1 volt reference is trimmed to ±1% and the error amplifier has an input common-mode voltage range that includes the reference voltage, thus eliminating the need for external divider resistors. A sync input to the oscillator enables multiple units to be slaved or a single unit to be synchronized to an external system clock. A wide range of dead time can be programmed by a single resistor connected between the C_T and Discharge pins. These devices also feature built-in soft-start circuitry, requiring only an external timing capacitor. A shutdown pin controls both the soft-start circuitry and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft-start recycle with longer shutdown commands. The under voltage lockout inhibits the outputs and the changing of the soft-start capacitor when V_{CC} is below nominal. The output stages are totem-pole design capable of sinking and sourcing in excess of 200 mA. The output stage of the SG1525A series features NOR Logic resulting in a low output for an off state while the SG1527A series utilizes OR Logic which gives a high output when off. The devices are available in Military, Industrial and Commercial temperature ranges.

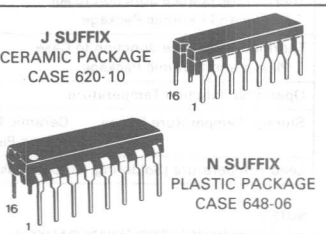
- 8.0 to 35 Volt Operation
- 5.1 Volt ± 1.0% Trimmed Reference
- 100 Hz to 400 kHz Oscillator Range
- Separate Oscillator Sync Pin
- Adjustable Dead Time Control
- Input Undervoltage Lockout
- Latching PWM to Prevent Multiple Pulses
- Pulse-by-Pulse Shutdown
- Dual Source/Sink Outputs: ± 400 mA Peak

FUNCTIONAL BLOCK DIAGRAM

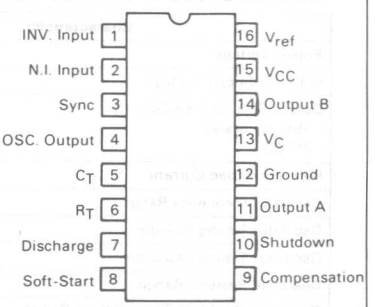


PULSE WIDTH MODULATOR CONTROL CIRCUITS

SILICON MONOLITHIC INTEGRATED CIRCUITS



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
SG1525AJ	−55 to +125°C	Ceramic DIP
SG1527AJ	−55 to +125°C	Ceramic DIP
SG2525AJ	−25 to +85°C	Ceramic DIP
SG2525AN	−25 to +85°C	Plastic DIP
SG2527AJ	−25 to +85°C	Ceramic DIP
SG2527AN	−25 to +85°C	Plastic DIP
SG3525AJ	0 to +70°C	Ceramic DIP
SG3525AN	0 to +70°C	Plastic DIP
SG3527AJ	0 to +70°C	Ceramic DIP
SG3527AN	0 to +70°C	Plastic DIP

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	+40	Vdc
Collector Supply Voltage	V_C	+40	Vdc
Logic Inputs	—	-0.3 to +5.5	V
Analog Inputs	—	-0.3 to V_{CC}	V
Output Current, Source or Sink	I_O	±500	mA
Reference Output Current	I_{ref}	50	mA
Oscillator Charging Current	—	5.0	mA
Power Dissipation (Plastic & Ceramic Package) T_A = +25°C (Note 2) T_C = +25°C (Note 3)	P_D	 1000 2000	mW
Thermal Resistance Junction to Air Plastic and Ceramic Package	$R_{\theta JA}$	100	°C/W
Thermal Resistance Junction to Case Plastic and Ceramic Package	$R_{\theta JC}$	60	°C/W
Operating Junction Temperature	T_J	+150	°C
Storage Temperature Range Ceramic Package Plastic Package	T_{stg}	-65 to +150 -55 to +125	°C
Lead Temperature (Soldering, 10 Seconds)	T_{Solder}	+300	°C

NOTES:
1. Values beyond which damage may occur.
2. Derate at 10 mW/°C for ambient temperatures above +50°C.
3. Derate at 16 mW/°C for case temperatures above +25°C.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min.	Max.	Unit
Supply Voltage	V_{CC}	+8.0	+35	Vdc
Collector Supply Voltage	V_C	+4.5	+35	Vdc
Output Sink/Source Current (Steady State) (Peak)	I_O	 0 0	 ±100 ±400	mA
Reference Load Current	I_{ref}	0	20	mA
Oscillator Frequency Range	f_{osc}	0.1	400	kHz
Oscillator Timing Resistor	R_T	2.0	150	kΩ
Oscillator Timing Capacitor	C_T	0.001	0.2	μF
Deadtime Resistor Range	R_D	0	500	Ω
Operating Ambient Temperature Range SG1525A, SG1527A SG2525A, SG2527A SG3525A, SG3527A	T_A	 -55 -25 0	 +125 +85 +70	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +20 Vdc, T_A = T_{low} to T_{high} [Note 4], unless otherwise specified)

Characteristic	Symbol	SG1525A/2525A SG1527A/2527A Min	Typ	Max	SG3525A SG3527A Min	Typ	Max	Unit
REFERENCE SECTION								
Reference Output Voltage (T_J = +25°C)	V_{ref}	5.05	5.10	5.15	5.00	5.10	5.20	Vdc
Line Regulation (+8.0 V ≤ V_{CC} ≤ +35 V)	Reg_{line}	—	10	20	—	10	20	mV
Load Regulation (0 mA ≤ I_L ≤ 20 mA)	Reg_{load}	—	20	50	—	20	50	mV
Temperature Stability	$\Delta V_{ref}/\Delta T$	—	20	—	—	20	—	mV
Total Output Variation Includes Line and Load Regulation over Temperature	ΔV_{ref}	5.00	—	5.20	4.95	—	5.25	Vdc
Short Circuit Current (V_{ref} = 0 V, T_J = +25°C)	I_{SC}	—	80	100	—	80	100	mA
Output Noise Voltage (10 Hz ≤ f ≤ 10 kHz, T_J = +25°C)	V_n	—	40	200	—	40	200	μV_{rms}
Long Term Stability (T_J = +125°C) (Note 5)	S	—	20	50	—	20	50	mV/khr
OSCILLATOR SECTION (Note 6, unless otherwise specified)								
Initial Accuracy (T_J = +25°C)	—	—	±2.0	±6.0	—	±2.0	±6.0	%
Frequency Stability with Voltage (+8.0 V ≤ V_{CC} ≤ +35 V)	$\frac{\Delta f_{osc}}{\Delta V_{CC}}$	—	±0.3	±1.0	—	±1.0	±2.0	%
Frequency Stability with Temperature	$\frac{\Delta f_{osc}}{\Delta T}$	—	±3.0	—	—	±3.0	—	%
Minimum Frequency (R_T = 150 kΩ, C_T = 0.2 μF)	f_{min}	—	50	—	—	50	—	Hz
Maximum Frequency (R_T = 2.0 kΩ, C_T = 1.0 nF)	f_{max}	400	—	—	400	—	—	kHz
Current Mirror (I_{R_T} = 2.0 mA)	—	1.7	2.0	2.2	1.7	2.0	2.2	mA
Clock Amplitude	—	3.0	3.5	—	3.0	3.5	—	V
Clock Width (T_J = +25°C)	—	0.3	0.5	1.0	0.3	0.5	1.0	μs
Sync Threshold	—	1.2	2.0	2.8	1.2	2.0	2.8	V
Sync Input Current (Sync Voltage = +3.5 V)	—	—	1.0	2.5	—	1.0	2.5	mA
ERROR AMPLIFIER SECTION (V_{CM} = +5.1 V)								
Input Offset Voltage	V_{IO}	—	0.5	5.0	—	2.0	10	mV
Input Bias Current	I_{IB}	—	1.0	10	—	1.0	10	μA
Input Offset Current	I_{IO}	—	—	1.0	—	—	1.0	μA
DC Open Loop Gain (R_L ≥ 10 MΩ)	A_{VOL}	60	75	—	60	75	—	dB
Low Level Output Voltage	V_{OL}	—	0.2	0.5	—	0.2	0.5	V
High Level Output Voltage	V_{OH}	3.8	5.6	—	3.8	5.6	—	V
Common Mode Rejection Ratio (+1.5 V ≤ V_{CM} ≤ +5.2 V)	CMRR	60	75	—	60	75	—	dB
Power Supply Rejection Ratio (+8.0 V ≤ V_{CC} ≤ +35 V)	PSRR	50	60	—	50	60	—	dB
PWM COMPARATOR SECTION								
Minimum Duty Cycle	DC_{min}	—	—	0	—	—	0	%
Maximum Duty Cycle	DC_{max}	45	49	—	45	49	—	%
Input Threshold, Zero Duty Cycle (Note 6)	V_{TH}	0.6	0.9	—	0.6	0.9	—	V
Input Threshold, Maximum Duty Cycle (Note 6)	V_{TH}	—	3.3	3.6	—	3.3	3.6	V
Input Bias Current	I_{IB}	—	0.05	1.0	—	0.05	1.0	μA

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	SG1525A/2525A SG1527A/2527A			SG3525A SG3527A			Unit
		Min	Typ	Max	Min	Typ	Max	
SOFT-START SECTION								
Soft-Start Current ($V_{shutdown}$ = 0 V)	—	25	50	80	25	50	80	μA
Soft-Start Voltage ($V_{shutdown}$ = 2.0 V)	—	—	0.4	0.6	—	0.4	0.6	V
Shutdown Input Current ($V_{shutdown}$ = 2.5 V)	—	—	0.4	1.0	—	0.4	1.0	mA
OUTPUT DRIVERS (Each Output, V_{CC} = +20 V)								
Output Low Level	V_{OL}							V
(I_{sink} = 20 mA)		—	0.2	0.4	—	0.2	0.4	
(I_{sink} = 100 mA)		—	1.0	2.0	—	1.0	2.0	
Output High Level	V_{OH}							V
(I_{source} = 20 mA)		18	19	—	18	19	—	
(I_{source} = 100 mA)		17	18	—	17	18	—	
Under Voltage Lockout (V8 and V9 = High)	V_{UL}	6.0	7.0	8.0	6.0	7.0	8.0	V
Collector Leakage, V_C = +35 V (Note 7)	$I_{C(leak)}$	—	—	200	—	—	200	μA
Rise Time (C_L = 1.0 nF, T_J = 25°C)	t_r	—	100	600	—	100	600	ns
Fall Time (C_L = 1.0 nF, T_J = 25°C)	t_f	—	50	300	—	50	300	ns
Shutdown Delay (V_{SD} = +3.0 V, C_S = 0, T_J = +25°C)	t_{ds}	—	0.2	0.5	—	0.2	0.5	μs
Supply Current, (V_{CC} = +35 V)	I_{CC}	—	14	20	—	14	20	mA

NOTES:

4. T_{low} = −55°C for SG1525A/1527A
   −25°C for SG2525A/2527A
   0°C for SG3525A/3527A
   T_{high} = +125°C for SG1525A/1527A
   +85°C for SG2525A/2527A
   +70°C for SG3525A/3527A
5. Since long term stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.
6. Tested at f_{osc} = 40 kHz (R_T = 3.6 kΩ, C_T = 0.01 μF, R_D = 0 Ω).
7. Applies to SG1525A/2525A/3525A only, due to polarity of output pulses.

APPLICATION INFORMATION

SHUTDOWN OPTIONS
(See Block Diagram, front page)

Since both the compensation and soft-start terminals (Pins 9 and 8) have current source pull-ups, either can readily accept a pull-down signal which only has to sink a maximum of 100 μA to turn off the outputs. This is subject to the added requirement of discharging whatever external capacitance may be attached to these pins.

An alternate approach is the use of the shutdown circuitry of Pin 10 which has been improved to enhance the available shutdown options. Activating this circuit by applying a positive signal on Pin 10 performs two functions: the PWM latch is immediately set providing the fastest turn-off signal to the outputs; and a 150 μA current sink begins to discharge the external soft-start capacitor. If the shutdown command is short, the PWM signal is terminated without significant discharge of the soft-start capacitor, thus, allowing, for example, a convenient implementation of pulse-by-pulse current limiting. Holding Pin 10 high for a longer duration, however, will ultimately discharge this external capacitor, recycling slow turn-on upon release.

Pin 10 should not be left floating as noise pickup could conceivably interrupt normal operation.

TYPICAL CHARACTERISTICS

FIGURE 1 — SG1525A OSCILLATOR SCHEMATIC

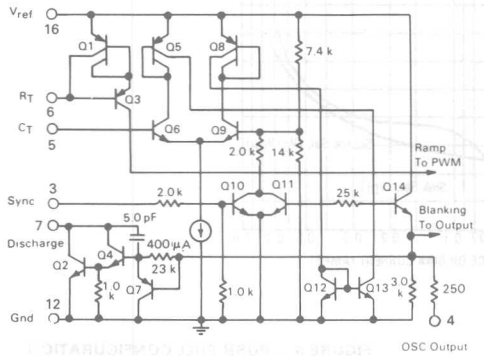


FIGURE 2 — OSCILLATOR CHARGE TIME versus R_T

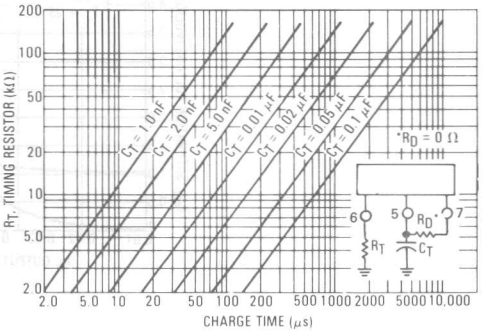


FIGURE 3 — OSCILLATOR DISCHARGE TIME versus R_D

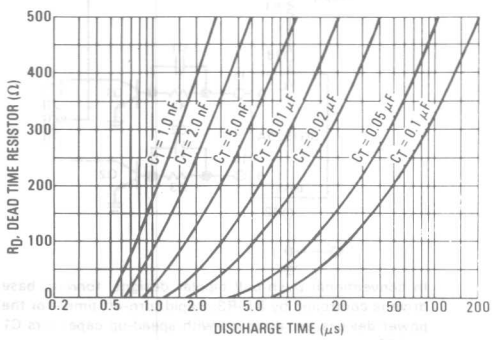


FIGURE 4 — SG1525A ERROR AMPLIFIER SCHEMATIC

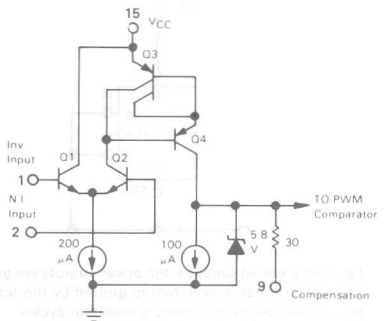


FIGURE 5 — ERROR AMPLIFIER OPEN-LOOP FREQUENCY RESPONSE

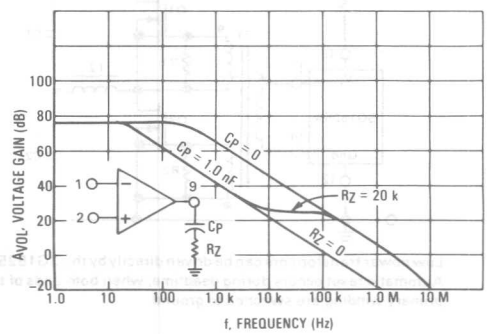


FIGURE 6 — SG1525A OUTPUT CIRCUIT (1/2 CIRCUIT SHOWN)

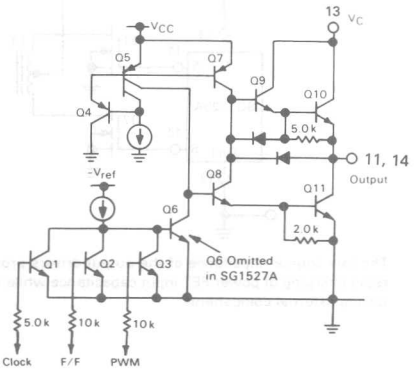


FIGURE 7 — SG1525A/2525A/3525A OUTPUT SATURATION CHARACTERISTICS

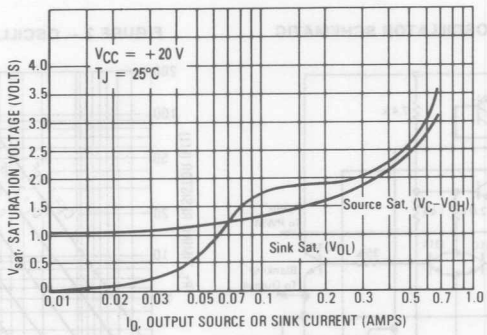
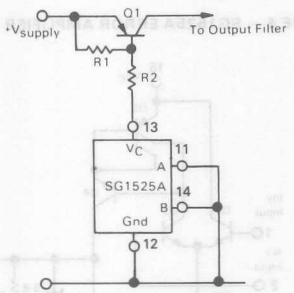
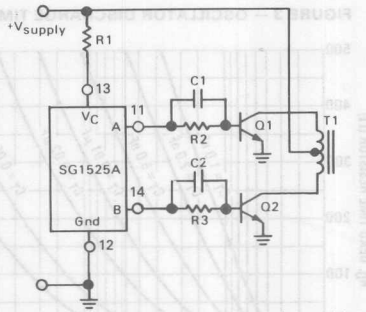


FIGURE 8 — SINGLE ENDED SUPPLY



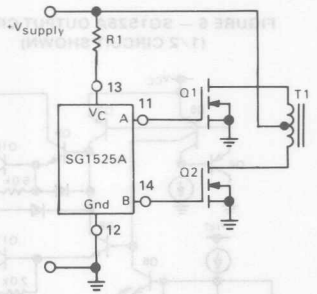
For single-ended supplies, the driver outputs are grounded. The V_C terminal is switched to ground by the totem-pole source transistors on alternate oscillator cycles.

FIGURE 9 — PUSH-PULL CONFIGURATION



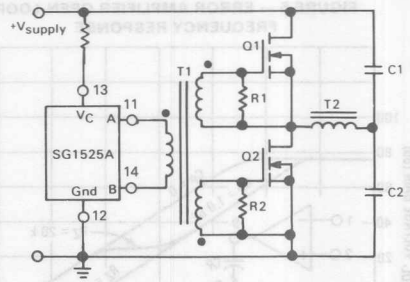
In conventional push-pull bipolar designs, forward base drive is controlled by R1–R3. Rapid turn-off times for the power devices are achieved with speed-up capacitors C1 and C2.

FIGURE 10 — DRIVING POWER FETS



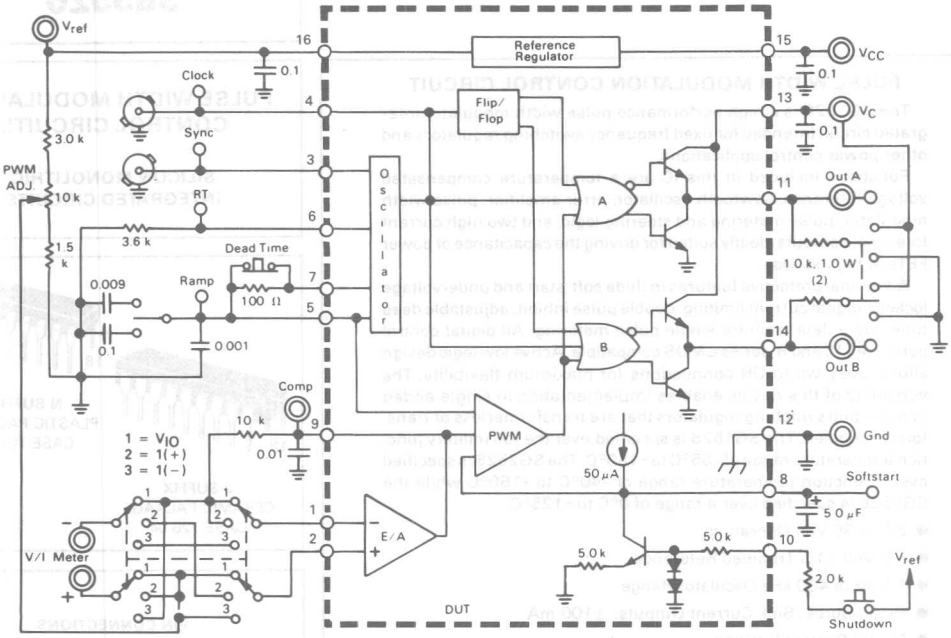
The low source impedance of the output drivers provides rapid charging of power FET input capacitance while minimizing external components.

FIGURE 11 — DRIVING TRANSFORMERS IN A HALF-BRIDGE CONFIGURATION



Low power transformers can be driven directly by the SG1525A. Automatic reset occurs during deadtime, when both ends of the primary winding are switched to ground.

FIGURE 12 — LAB TEST FIXTURE



MOTOROLA

SG1526
SG2526
SG3526

3

PULSE WIDTH MODULATION CONTROL CIRCUIT

The SG1526 is a high performance pulse width modulator integrated circuit intended for fixed frequency switching regulators and other power control applications.

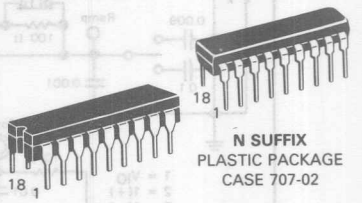
Functions included in this IC are a temperature compensated voltage reference, sawtooth oscillator, error amplifier, pulse width modulator, pulse metering and steering logic, and two high current totem pole outputs ideally suited for driving the capacitance of power FETs at high speeds.

Additional protective features include soft start and undervoltage lockout, digital current limiting, double pulse inhibit, adjustable dead time and a data latch for single pulse metering. All digital control ports are TTL and B-series CMOS compatible. Active low logic design allows easy wired-OR connections for maximum flexibility. The versatility of this device enables implementation in single-ended or push-pull switching regulators that are transformerless or transformer coupled. The SG1526 is specified over the full military junction temperature range of −55°C to +150°C. The SG2526 is specified over a junction temperature range of −40°C to +150°C while the SG3526 is specified over a range of 0°C to +125°C.

- 8.0 to 35 Volt Operation
- 5.0 Volt ±1% Trimmed Reference
- 1.0 Hz to 400 kHz Oscillator Range
- Dual Source/Sink Current Outputs: ±100 mA
- Digital Current Limiting
- Programmable Dead Time
- Undervoltage Lockout
- Single Pulse Metering
- Programmable Soft Start
- Wide Current Limit Common Mode Range
- Guaranteed 6 Unit Synchronization

PULSE WIDTH MODULATION CONTROL CIRCUITS

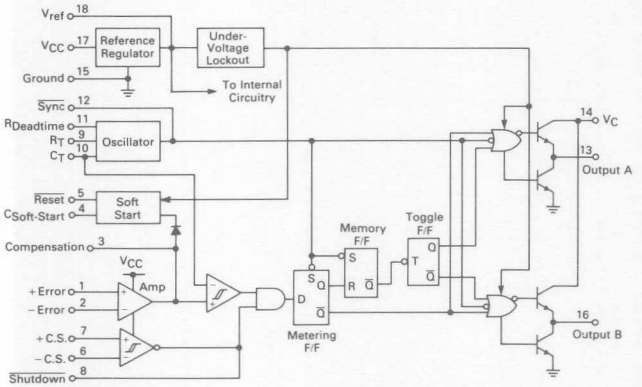
SILICON MONOLITHIC INTEGRATED CIRCUITS



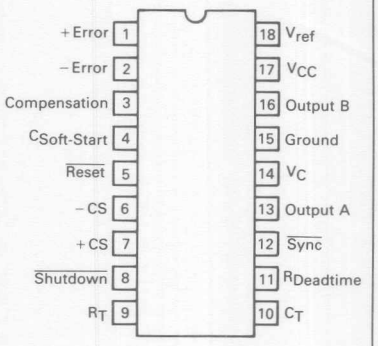
N SUFFIX
PLASTIC PACKAGE
CASE 707-02

J SUFFIX
CERAMIC PACKAGE
CASE 726-04

BLOCK DIAGRAM



PIN CONNECTIONS



Top View

ORDERING INFORMATION

Device	Junction Temperature Range	Package
SG1526J	−55 to +150°C	Ceramic DIP
SG2526J SG2526N	−40 to +150°C	Ceramic DIP Plastic DIP
SG3526J SG3526N	0 to +125°C	Ceramic DIP Plastic DIP

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	+40	Vdc
Collector Supply Voltage	V_C	+40	Vdc
Logic Inputs	—	-0.3 to +5.5	V
Analog Inputs	—	-0.3 to V_{CC}	V
Output Current, Source or Sink	I_O	±200	mA
Reference Load Current (V_{CC} = 40 V, Note 2)	I_{ref}	50	mA
Logic Sink Current	—	15	mA
Power Dissipation (Plastic and Ceramic Package) (Note 3) T_A = +25°C (Note 4) T_C = +25°C	P_D	 1000 3000	mW
Thermal Resistance Junction to Air (Plastic and Ceramic Package)	$R_{\theta JA}$	100	°C/W
Thermal Resistance Junction to Case (Plastic and Ceramic Package)	$R_{\theta JC}$	42	°C/W
Operating Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Lead Temperature (Soldering, 10 Seconds)	T_{Solder}	±300	°C

Notes:
1. Values beyond which damage may occur
2. Maximum junction temperature must be observed.
3. Derate at 10 mW/°C for ambient temperatures above +50°C
4. Derate at 24 mW/°C for case temperatures above +25°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	+8.0	+35	Vdc
Collector Supply Voltage	V_C	+4.5	+35	Vdc
Output Sink/Source Current (Each Output)	I_O	0	±100	mA
Reference Load Current	I_{ref}	0	20	mA
Oscillator Frequency Range	f_{osc}	0.001	400	kHz
Oscillator Timing Resistor	R_T	2.0	150	kΩ
Oscillator Timing Capacitor	C_T	0.001	20	μF
Available Deadtime Range (40 kHz)		3.0	50	%
Operating Junction Temperature Range SG1526 SG2526 SG3526	T_J	 -55 -40 0	 +150 +150 +125	°C

Characteristic	Symbol	SG1526/2526			SG3526			Unit
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION (Note 6)								
Reference Output Voltage (T_J = +25°C)	V_{ref}	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation (+8.0 V ≤ V_{CC} ≤ +35 V)	Reg_{line}	—	10	20	—	10	30	mV
Load Regulation, 0 mA ≤ I_L ≤ 20 mA	Reg_{load}	—	10	30	—	10	50	mV
Temperature Stability	$\Delta V_{ref}/\Delta T_J$	—	15	—	—	10	—	mV
Total Reference Output Voltage Variation (+8.0 V ≤ V_{CC} ≤ +35 V, 0 mA ≤ I_L ≤ 20 mA)	ΔV_{ref}	4.90	5.00	5.10	4.85	5.00	5.15	V
Short Circuit Current (V_{ref} = 0 V, Note 2)	I_{SC}	25	80	125	25	80	125	mA
UNDERVOLTAGE LOCKOUT								
$\overline{\text{Reset}}$ Output Voltage (V_{ref} = +3.8 V)	—	—	0.2	0.4	—	0.2	0.4	V
$\overline{\text{Reset}}$ Output Voltage (V_{ref} = +4.8 V)	—	2.4	4.8	—	2.4	4.8	—	V
OSCILLATOR SECTION (Note 7)								
Initial Accuracy (T_J = +25°C)	—	—	—	±3.0	±8.0	—	±3.0	±8.0	%
Frequency Stability over Power Supply Range (+8.0 V ≤ V_{CC} ≤ +35 V)	$\frac{\Delta f_{osc}}{\Delta V_{CC}}$	—	0.5	1.0	—	0.5	1.0	%
Frequency Stability over Temperature ($\Delta T_J = T_{low}$ to T_{high})	$\frac{\Delta f_{osc}}{\Delta T_J}$	—	4.0	—	—	2.0	—	%
Minimum Frequency (R_T = 150 kΩ, C_T = 20 μF)	f_{min}	—	0.5	—	—	0.5	—	Hz
Maximum Frequency (R_T = 2.0 kΩ, C_T = 0.001 μF)	f_{max}	400	—	—	400	—	—	kHz
Sawtooth Peak Voltage (V_{CC} = +35 V)	$V_{osc(P)}$	—	3.0	3.5	—	3.0	3.5	V
Sawtooth Valley Voltage (V_{CC} = +8.0 V)	$V_{osc(V)}$	0.45	0.8	—	0.45	0.8	—	V
ERROR AMPLIFIER SECTION (Note 8)								
Input Offset Voltage (R_S ≤ 2.0 kΩ)	V_{IO}	—	2.0	5.0	—	2.0	10	mV
Input Bias Current	I_{IB}	—	−350	−1000	—	−350	−2000	nA
Input Offset Current	I_{IO}	—	35	100	—	35	200	nA
DC Open Loop Gain (R_L ≥ 10 MΩ)	A_{Vol}	64	72	—	60	72	—	dB
High Output Voltage ($V_{Pin\ 1}$−$V_{Pin\ 2}$ ≥ +150 mV, I_{source} = 100 μA)	V_{OH}	3.6	4.2	—	3.6	4.2	—	V
Low Output Voltage ($V_{Pin\ 2}$−$V_{Pin\ 1}$ ≥ +150 mV, I_{sink} = 100 μA)	V_{OL}	—	0.2	0.4	—	0.2	0.4	V
Common Mode Rejection Ratio (R_S ≤ 2.0 kΩ)	CMRR	70	94	—	70	94	—	dB
Power Supply Rejection Ratio (+12 V ≤ V_{CC} ≤ +18 V)	PSRR	66	80	—	66	80	—	dB

Notes:
5. T_{low} = −55°C for SG1526
   −40°C for SG2526
   0°C for SG3526
   T_{high} = +150°C for SG1526/2526
   +125°C for SG3526
6. I_L = 0 mA unless otherwise noted.
7. f_{osc} = 40 kHz (R_T = 4.12 kΩ ±1%, C_T = 0.01 μF ±1%, R_D = 0 Ω)
8. 0 V ≤ V_{CM} ≤ +5.2 V

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	SG1526/2526			SG3526			Unit
		Min	Typ	Max	Min	Typ	Max	
PWM COMPARATOR SECTION (Note 7)								
Minimum Duty Cycle ($V_{compensation}$ = +0.4 V)	DC_{min}	—	—	0	—	—	0	%
Maximum Duty Cycle ($V_{compensation}$ = +3.6 V)	DC_{max}	45	49	—	45	49	—	%
DIGITAL PORTS (SYNC, SHUTDOWN, RESET)								
Output Voltage — High Logic Level (I_{source} = 40 μA)	V_{OH}	2.4	4.0	—	2.4	4.0	—	V
Output Voltage — Low Logic Level (I_{sink} = 3.6 mA)	V_{OL}	—	0.2	0.4	—	0.2	0.4	V
Input Current — High Logic Level (V_{IH} = +2.4 V)	I_{IH}	—	-125	-200	—	-125	-200	μA
Input Current — Low Logic Level (V_{IL} = +0.4 V)	I_{IL}	—	-225	-360	—	-225	-360	μA
CURRENT LIMIT COMPARATOR SECTION (Note 9)								
Sense Voltage ($R_S \leq 50\ \Omega$)	V_{sense}	90	100	110	80	100	120	mV
Input Bias Current	I_{IB}	—	-3.0	-10	—	-3.0	-10	μA
SOFT-START SECTION								
Error Clamp Voltage ($\overline{Reset}$ = +0.4 V)	—	—	0.1	0.4	—	0.1	0.4	V
$C_{Soft\text{-}Start}$ Charging Current ($\overline{Reset}$ = +2.4 V)	I_{CS}	50	100	150	50	100	150	μA
OUTPUT DRIVERS (Each Output, V_C = +15 Vdc unless otherwise specified)								
Output High Level I_{source} = 20 mA I_{source} = 100 mA	V_{OH}	 12.5 12	 13.5 13	 — —	 12.5 12	 13.5 13	 — —	V
Output Low Level I_{sink} = 20 mA I_{sink} = 100 mA	V_{OL}	 — —	 0.2 1.2	 0.3 2.0	 — —	 0.2 1.2	 0.3 2.0	V
Collector Leakage, V_C = +40 V	$I_{C(leak)}$	—	50	150	—	50	150	μA
Rise Time (C_L = 1000 pF)	t_r	—	0.3	0.6	—	0.3	0.6	μs
Fall Time (C_L = 1000 pF)	t_f	—	0.1	0.2	—	0.1	0.2	μs
Supply Current (Shutdown = +0.4 V, V_{CC} = +35 V, R_T = 4.12 kΩ)	I_{CC}	—	18	30	—	18	30	mA

7. f_{osc} = 40 kHz (R_T = 4.12 kΩ ±1%, C_T = 0.01 μF ±1%, R_D = 0 Ω)
8. 0 V ≤ V_{CM} ≤ +5.2 V
9. 0 V ≤ V_{CM} ≤ +12 V

3

TYPICAL CHARACTERISTICS

FIGURE 1 — SG1526 REFERENCE STABILITY OVER TEMPERATURE

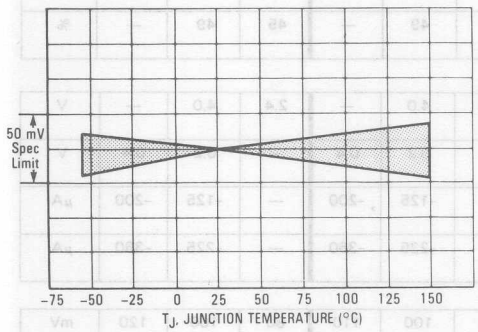


FIGURE 2 — REFERENCE VOLTAGE AS A FUNCTION SUPPLY VOLTAGE

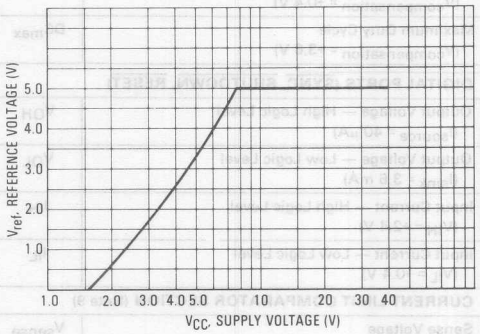


FIGURE 3 — ERROR AMPLIFIER OPEN LOOP FREQUENCY RESPONSE

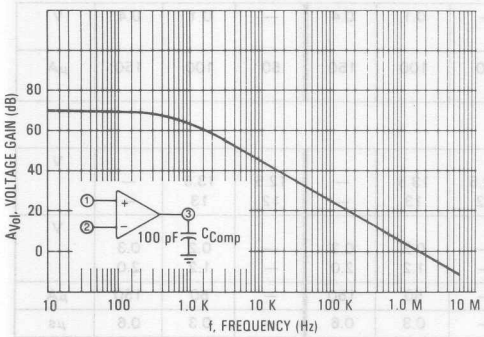


FIGURE 4 — CURRENT LIMIT COMPARATOR THRESHOLD

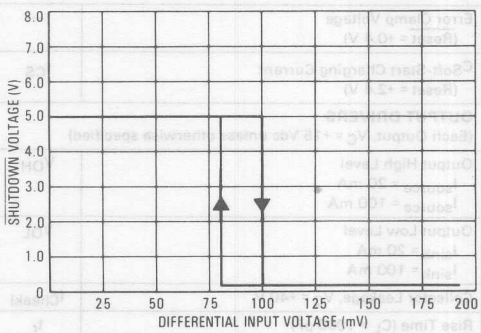


FIGURE 5 — UNDERVOLTAGE LOCKOUT CHARACTERISTIC

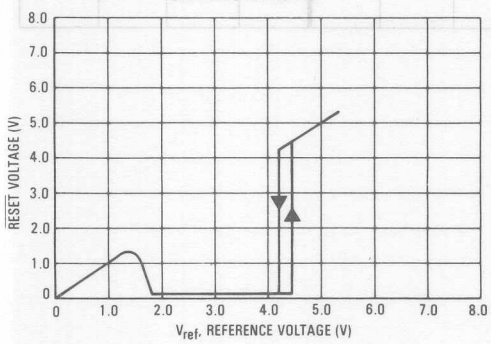


FIGURE 6 — OUTPUT DRIVER SATURATION VOLTAGE AS A FUNCTION OF SINK CURRENT

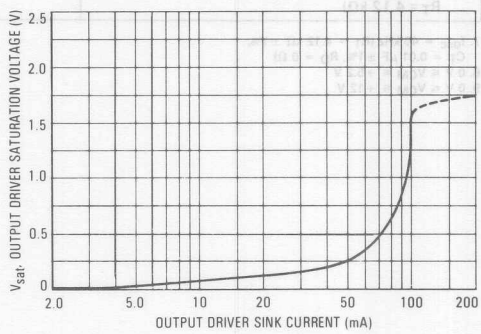


FIGURE 7 — V_C SATURATION VOLTAGE AS A FUNCTION OF SINK CURRENT

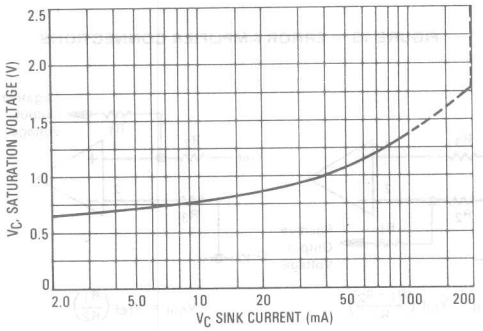


FIGURE 8 — SG1526 OSCILLATOR PERIOD

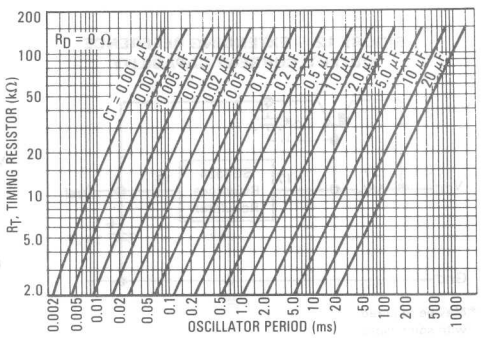


FIGURE 9 — SG1526 ERROR AMPLIFIER

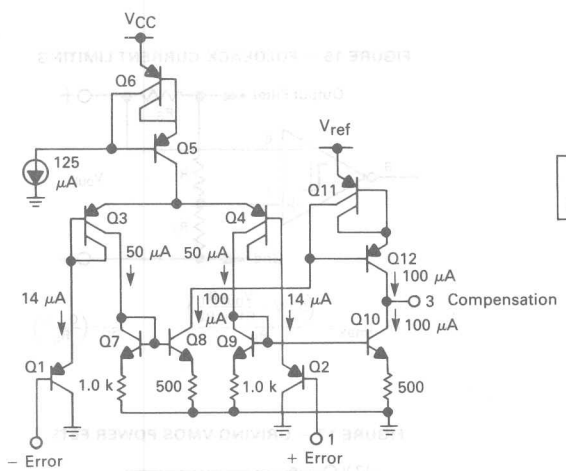


FIGURE 10 — SG1526 UNDERVOLTAGE LOCKOUT

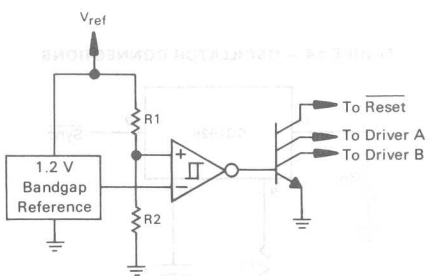
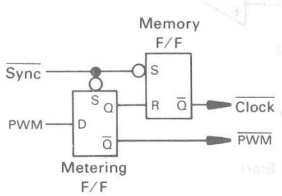


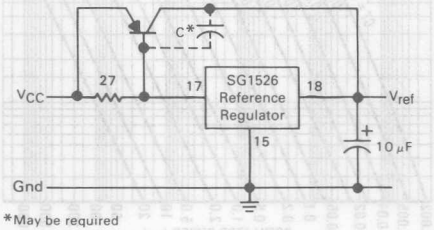
FIGURE 11 — SG1526 PULSE PROCESSING LOGIC



The metering FLIP-FLOP is an asynchronous data latch which suppresses high frequency oscillations by allowing only one PWM pulse per oscillator cycle.

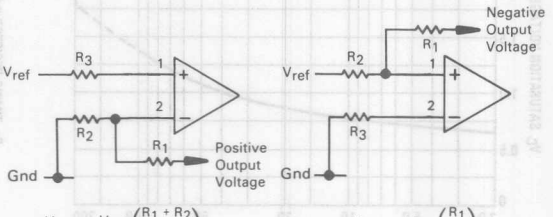
The memory FLIP-FLOP prevents double pulsing in a push-pull configuration by remembering which output produced the last pulse.

FIGURE 12 — EXTENDING REFERENCE OUTPUT CURRENT CAPABILITY



*May be required with some types of transistors

FIGURE 13 — ERROR AMPLIFIER CONNECTIONS



$V_{out} = V_{ref}\left(\frac{R_1 + R_2}{R2}\right)$ $V_{out} = V_{ref}\left(\frac{R_1}{R2}\right)$

$R_3 = \left(\frac{R_1 R_2}{R_1 + R_2}\right)$

FIGURE 14 — OSCILLATOR CONNECTIONS

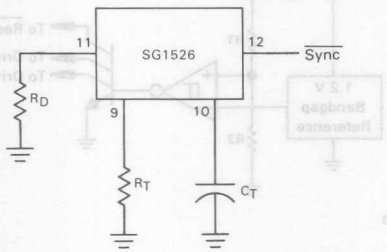
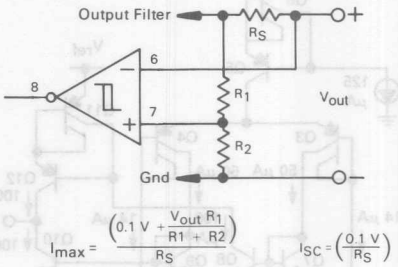


FIGURE 15 — FOLDBACK CURRENT LIMITING



$I_{max} = \frac{\left(0.1\ V + \frac{V_{out} R_1}{R1 + R2}\right)}{R_S}$ $I_{SC} = \left(\frac{0.1\ V}{R_S}\right)$

FIGURE 16 — SG1526 SOFT-START CIRCUITRY

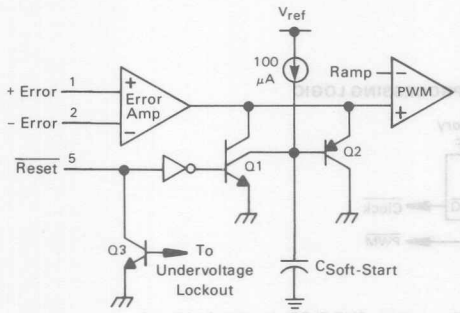
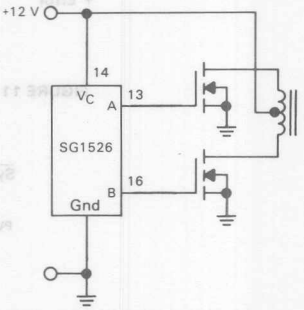


FIGURE 17 — DRIVING VMOS POWER FETS



The totem pole output drivers of the SG1526 are ideally suited for driving the input capacitance of power FETs at high speeds.

FIGURE 18 — HALF-BRIDGE CONFIGURATION

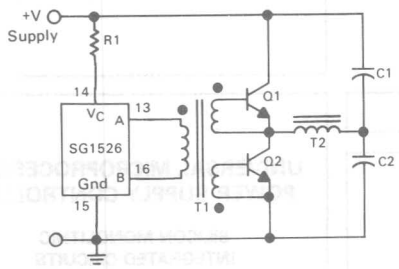
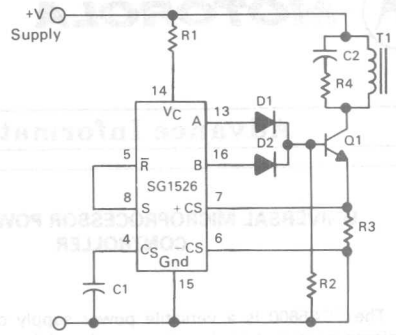


FIGURE 19 — FLYBACK CONVERTER WITH CURRENT LIMITING



In the above circuit, current limiting is accomplished by using the current limit comparator output to reset the soft-start capacitor.

FIGURE 20 — SINGLE-ENDED CONFIGURATION

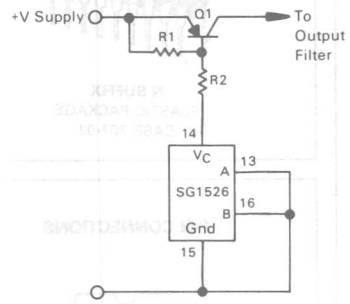
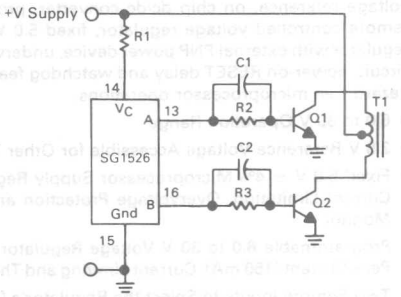


FIGURE 21 — PUSH-PULL CONFIGURATION



MOTOROLA

TCA5600

Advance Information

3

UNIVERSAL MICROPROCESSOR POWER SUPPLY CONTROLLER

The TCA5600 is a versatile power supply control circuit for microprocessor based systems and mainly intended for automotive applications and battery powered instruments. To cover a wide range of applications, the device offers high circuit flexibility with minimum of external components.

Functions included in this IC are a temperature compensated voltage reference, on chip dc/dc converter, programmable and remote controlled voltage regulator, fixed 5.0 V supply voltage regulator with external PNP power device, undervoltage detection circuit, power-on RESET delay and watchdog feature for safe and hazard free microprocessor operations.

- 6.0 to 30 V Operation Range
- 2.5 V Reference Voltage Accessible for Other Tasks
- Fixed 5.0 V ± 4% Microprocessor Supply Regulator Including Current Limitation, Overvoltage Protection and Undervoltage Monitor
- Programmable 6.0 to 30 V Voltage Regulator Exhibiting High Peak Current (150 mA), Current Limiting and Thermal Protection
- Two Remote Inputs to Select the Regulator's Operation Mode: OFF, 5.0 V, 5.0 V Standby and Programmable Output Voltage
- Self Contained dc/dc Converter Fully Controlled By the Programmable Regulator to Guarantee Safe Operation Under All Working Conditions
- Programmable Power-On RESET Delay
- Watchdog Select Input
- Negative Edge Triggered Watchdog Input
- Low Current Consumption in the V_{CC1} Standby Mode
- All Digital Control Ports are TTL- and MOS-Compatible

APPLICATIONS INCLUDE:

- Microprocessor Systems with E^2PROMs
- High Voltage Crystal and Plasma Displays
- Decentralized Power Supplies in Computer and Telecommunication Systems

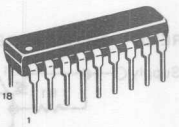
RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Max	Unit
Power Supply Voltage	V_{CC1} V_{CC2}	5.0 5.5	30 30	V
Collector Current	I_C	—	800	mA
Output Voltage	V_{out2}	6.0	30	V
Reference Source Current	I_{ref}	0	2.0	mA

This document contains information on a new product. Specifications and information herein are subject to change without notice.

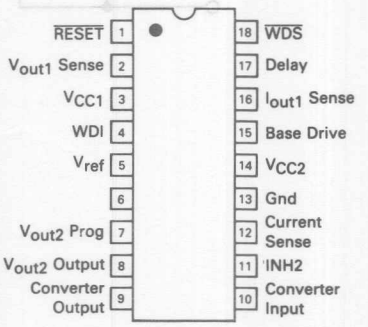
UNIVERSAL MICROPROCESSOR POWER SUPPLY CONTROLLER

SILICON MONOLITHIC INTEGRATED CIRCUITS



N SUFFIX
PLASTIC PACKAGE
CASE 707-02

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

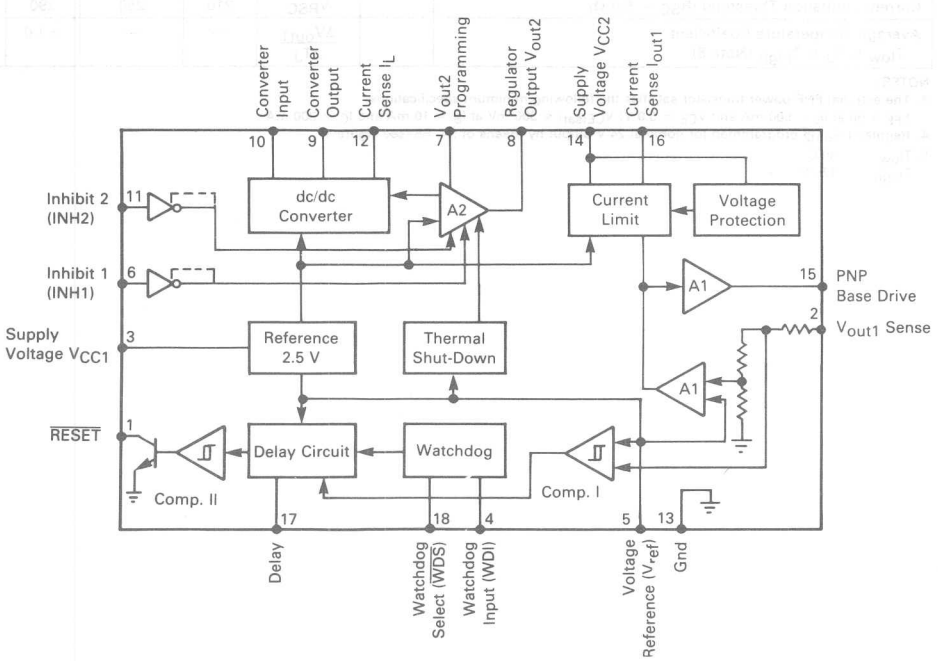
Device	Operating Junction Temperature Range	Package
TCA5600	−40° to +125°C	Plastic DIP

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted, Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 3, 14)	V_{CC1}, V_{CC2}	35	Vdc
Base Drive Current (Pin 15)	I_B	20	mA
Collector Current (Pin 10)	I_C	1.0	A
Forward Rectifier Current (Pin 10–Pin 9)	I_F	1.0	A
Logic Inputs INH1, INH2, $\overline{WDS}$ (Pin 6, 11, 18)	V_{INP}	−0.3 V to V_{CC1}	Vdc
Logic Input Current WDI (Pin 4)	I_{WDI}	±0.5	mA
Output Sink Current $\overline{RESET}$ (Pin 1)	$I_{\overline{RES}}$	10	mA
Analog Inputs (Pin 2) (Pin 7)	— —	−0.3 to 10 −0.3 to 5.0	V
Reference Source Current (Pin 5)	I_{ref}	5.0	mA
Power Dissipation (Note 2) T_A = +85°C	P_D	500	mW
Thermal Resistance (Junction to Air)	$R_{\theta JA}$	100	°C/W
Operating Temperature Range	T_A	−40 to +85°C	°C
Operating Junction Temperature	T_J	+125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

NOTES:
1. Values beyond which damage may occur.
2. Derate at 10 mW/°C for ambient temperature above +85°C.

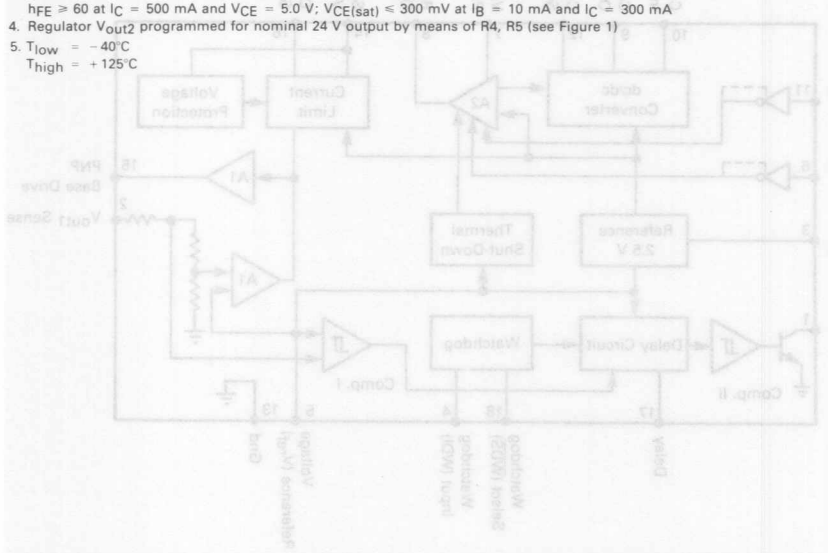
FIGURE 1 — FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (V_{CC1} = V_{CC2} = 12 V; T_J = 25°C; I_{ref} = 0; I_{out1} = 0 (Note 3); R_{SC} = 0.5 Ω; INH1 = "High"; INH2 = "High"; $\overline{WDS}$ = "High"; I_{out2} = 0 (Note 4); if not otherwise specified)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION						
Nominal Reference Voltage	1	$V_{ref\ nom}$	2.42	2.5	2.58	V
Reference Voltage I_{ref} = 0.5 mA, $T_{low} \le T_J \le T_{high}$ (Note 5), 6.0 V ≤ V_{CC1} ≤ 18 V		V_{ref}	2.4	—	2.6	V
Line Regulation (6.0 V ≤ V_{CC2} ≤ 18 V)		Reg_{line}	—	2.0	15	mV
Average Temperature Coefficient $T_{low} \le T_J \le T_{high}$ (Note 5)	2	$\frac{\Delta V_{ref}}{\Delta T_J}$	—	—	+/−0.5	mV/°C
Ripple Rejection Ratio f = 1.0 kHz, V_{sin} = 1.0 V_{pp}	3	RR	60	70	—	dB
Output Impedance 0 ≤ I_{ref} ≤ 2.0 mA		Z_O	—	1.0	—	Ohm
Standby Current Consumption V_{CC2} = Open	4	I_{CC1}	—	3.0	—	mA
5.0 V MICROPROCESSOR VOLTAGE REGULATOR SECTION						
Nominal Output Voltage		$V_{out1(nom)}$	4.8	5.0	5.2	V
Output Voltage 5.0 mA ≤ I_{out1} ≤ 300 mA, $T_{low} \le T_J \le T_{high}$ (Note 5) 6.0 V ≤ V_{CC2} ≤ 18 V	5 6	V_{out1}	4.75	—	5.25	V
Line Regulation (6.0 V ≤ V_{CC2} ≤ 18 V)		Reg_{line}	—	10	50	mV
Load Regulation (5.0 mA ≤ I_{out1} ≤ 300 mA)		Reg_{load}	—	20	100	mV
Base Current Drive (V_{CC2} = 6.0 V, V_{15} = 4.0 V)		I_B	10	15	—	mA
Ripple Rejection Ratio f = 1.0 kHz, V_{sin} = 1.0 V_{pp}	3	RR	50	65	—	dB
Undervoltage Detection Level (R_{SC} = 5.0 Ω)	7	V_{low}	4.5	0.93 x V_{out1}	—	V
Current Limitation Threshold (R_{SC} = 5.0 Ω)		V_{RSC}	210	250	290	mV
Average Temperature Coefficient $T_{low} \le T_J \le T_{high}$ (Note 5)		$\frac{\Delta V_{out1}}{\Delta T_J}$	—	—	±1.0	mV/°C

NOTES:
3. The external PNP power transistor satisfies the following minimum specifications:
   $h_{FE} \ge 60$ at I_C = 500 mA and V_{CE} = 5.0 V; $V_{CE(sat)} \le 300$ mV at I_B = 10 mA and I_C = 300 mA
4. Regulator V_{out2} programmed for nominal 24 V output by means of R4, R5 (see Figure 1)
5. T_{low} = −40°C
   T_{high} = +125°C



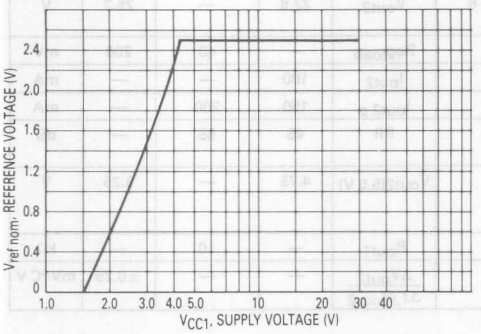
Characteristic	Figure	Symbol	Min	Typ	Max	Unit
PROGRAMMABLE VOLTAGE REGULATOR SECTION (Note 6)						
Nominal Output Voltage		$V_{out2(nom)}$	23	24	25	V
Output Voltage 1.0 mA ≤ I_{out2} ≤ 100 mA, T_{low} ≤ T_J ≤ T_{high} (Notes 5, 7)	8	V_{out2}	22.8	—	25.2	V
Load Regulation 1.0 mA ≤ I_{out2} ≤ 100 mA (Note 7)		Reg_{load}	—	40	200	mV
DC Output Current		I_{out2}	100	—	—	mA
Peak Output Current (Internally Limited)		$I_{out2\,p}$	150	200	—	mA
Ripple Rejection Ratio f = 20 kHz, V = 0.4 V_{pp}		RR	45	55	—	dB
Output Voltage (Fixed 5.0 V) 1.0 mA ≤ I_{out2} ≤ 20 mA, T_{low} ≤ T_J ≤ T_{high}, INH1 = "High" (Note 5)		$V_{out2(5.0\ V)}$	4.75	—	5.25	V
OFF State Output Impedance (INH2 = "Low")		R_{out1}	—	10	—	kΩ
Average Temperature Coefficient T_{low} ≤ T_J ≤ T_{high} (Note 5)		$\frac{\Delta V_{out2}}{\Delta T_J V_{out2}}$	—	—	±0.25	mV/°C V
DC/DC CONVERTER SECTION						
Collector Current Detection Level "High" R_C = 10 k "Low"	9	$V_{12(H)}$ $V_{12(L)}$	350 —	400 50	450 —	mV
Collector Saturation Voltage I_C = 600 mA (Note 7)	10	$V_{CE(sat)}$	—	—	1.6	V
Rectifier Forward Voltage Drop I_F = 600 mA (Note 7)	11	V_F	—	—	1.4	V
WATCHDOG AND $\overline{\text{RESET}}$ CIRCUIT SECTION						
Threshold Voltage "High" (static) "Low"		$V_{C5(H)}$ $V_{C5(L)}$	— —	2.5 1.0	— —	V
Current Source T_{low} ≤ T_J ≤ T_{high} (Note 5) Power-Up $\overline{\text{RESET}}$ Watchdog Time Out Watchdog $\overline{\text{RESET}}$		I_{C5}	 −1.8 — —	 −2.5 5xI_{C5} −50xI_{C5}	 −3.2 — —	μA
Watchdog Input Voltage Swing		V_{WDI}	—	—	±5.5	V
Watchdog Input Impedance		r_i	12	15	—	kΩ
Watchdog Reset Pulse Width (C8 = 1.0 nF) (Note 9)		t_p	—	—	10	μs
DIGITAL PORTS: $\overline{\text{WDS}}$, INH 1, INH 2, $\overline{\text{RESET}}$ (Note 8)						
Input Voltage Range		V_{INP}	—	—	−0.3 to V_{CC1}	V
Input HIGH Current 2.0 V ≤ V_{IH} ≤ 5.5 V 5.5 V ≤ V_{IH} ≤ V_{CC1}		I_{IH}	 — —	 — —	 100 150	μA
Input LOW Current −0.3 V ≤ V_{IL} ≤ 0.8 V for INH1, INH2, −0.3 V ≤ V_{IL} ≤ 0.4 V for $\overline{\text{WDS}}$		I_{IL}	—	—	−100	μA
Leakage Current Immunity (INH2, High "Z" State)	12	I_Z	±20	—	—	μA
Output LOW Voltage $\overline{\text{RESET}}$ (I_{OL} = 6.0 mA)		V_{OL}	—	—	0.4	V
Output HIGH Current $\overline{\text{RESET}}$ (V_{OH} = 5.5 V)		V_{OH}	—	—	20	μA

NOTES:
5. T_{low} = −40°C
   T_{high} = +125°C
6. V_S = 28 V, INH1 = "Low" for this Electrical Characteristic section unless otherwise specified.
7. Pulse tested t_p ≤ 300 μs
8. Temperature range T_{low} ≤ T_J ≤ T_{high} applies to this Electrical Characteristics section.
9. For test purposes, a negative pulse is applied to Pin 4 (−2.5 V ≥ V_4 ≥ −5.5 V).

3

TYPICAL CHARACTERISTICS

FIGURE 1 — REFERENCE VOLTAGE versus SUPPLY VOLTAGE



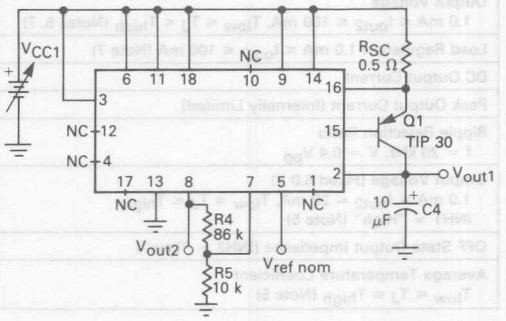
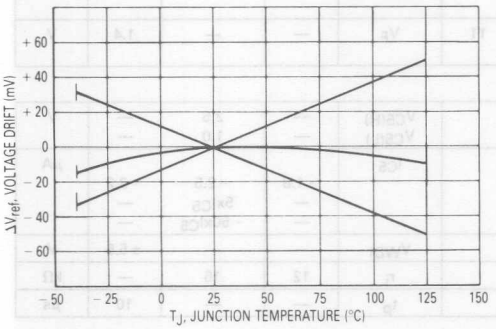


FIGURE 2 — REFERENCE STABILITY versus TEMPERATURE



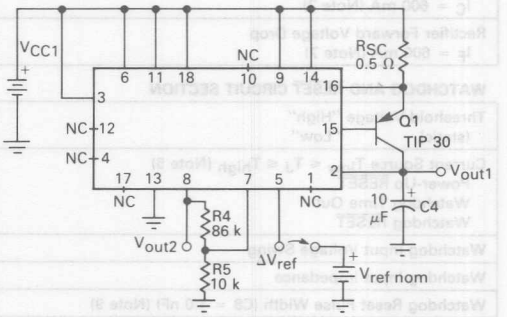
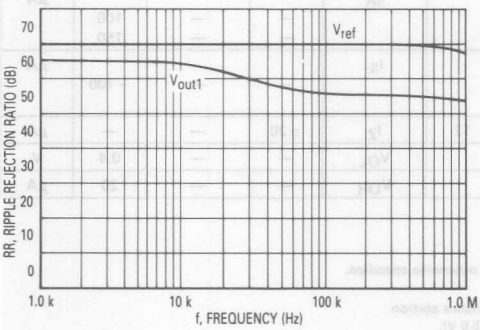


FIGURE 3 — RIPPLE REJECTION versus FREQUENCY



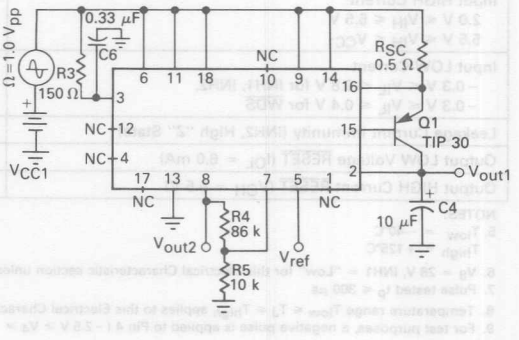
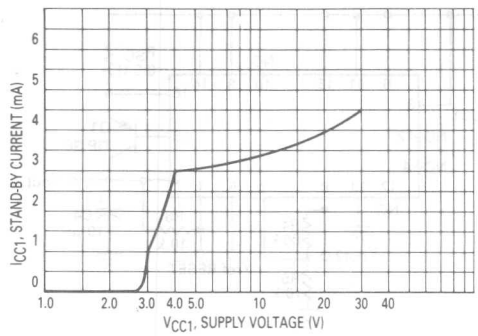


FIGURE 4 — STAND-BY CURRENT versus SUPPLY VOLTAGE



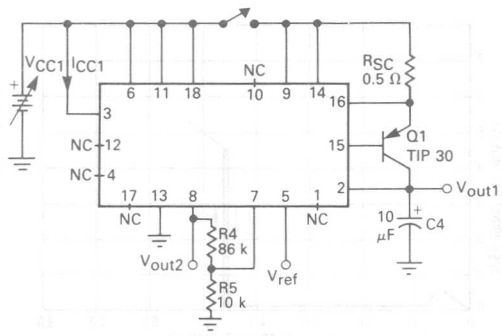
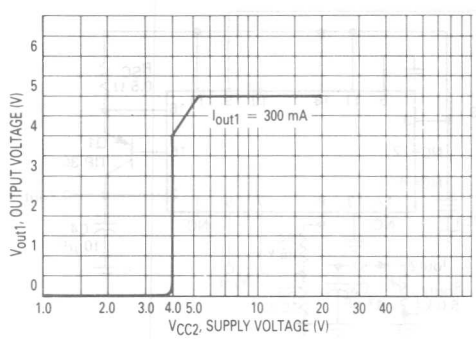


FIGURE 5 — POWER-UP BEHAVIOR OF THE 5.0 V REGULATOR



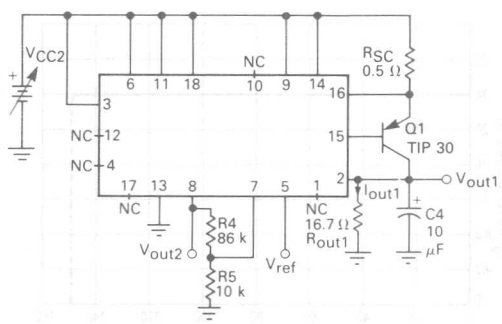
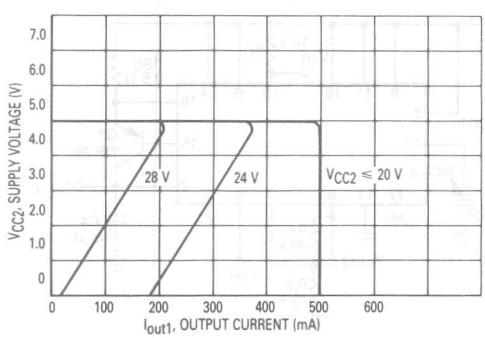


FIGURE 6 — FOLDBACK CHARACTERISTICS OF THE 5.0 V REGULATOR



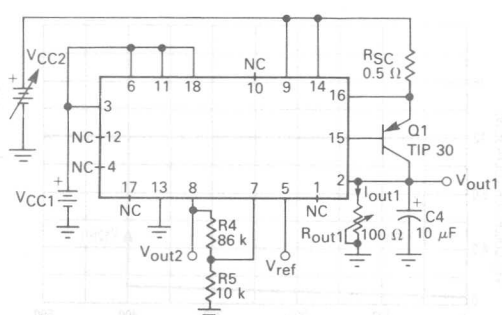


FIGURE 7 — UNDERVOLTAGE LOCKOUT CHARACTERISTICS

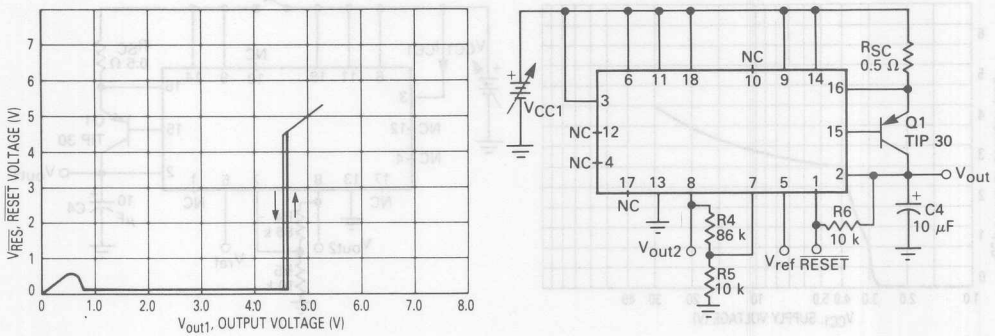


FIGURE 8 — OUTPUT CURRENT CAPABILITY OF THE PROGRAMMING REGULATOR

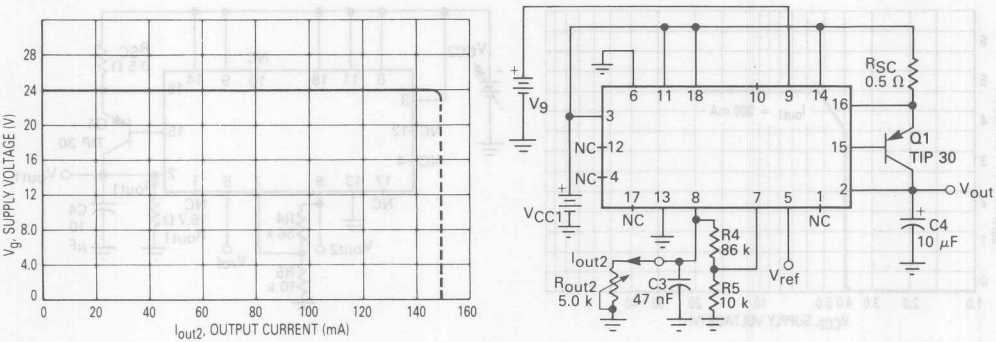


FIGURE 9 — COLLECTOR CURRENT DETECTION LEVEL

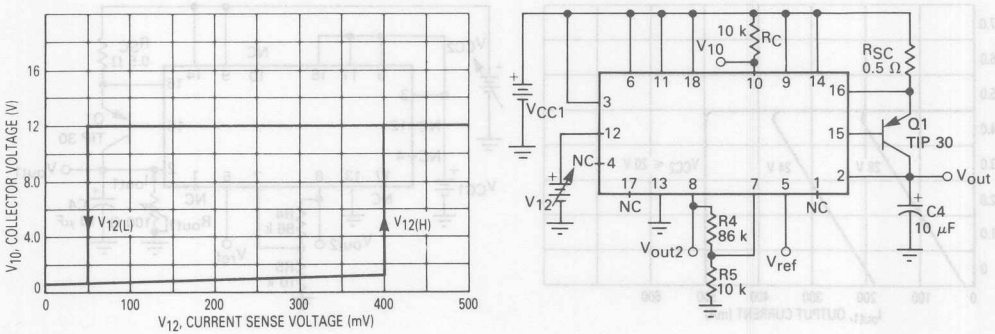


FIGURE 10 — POWER SWITCH CHARACTERISTICS

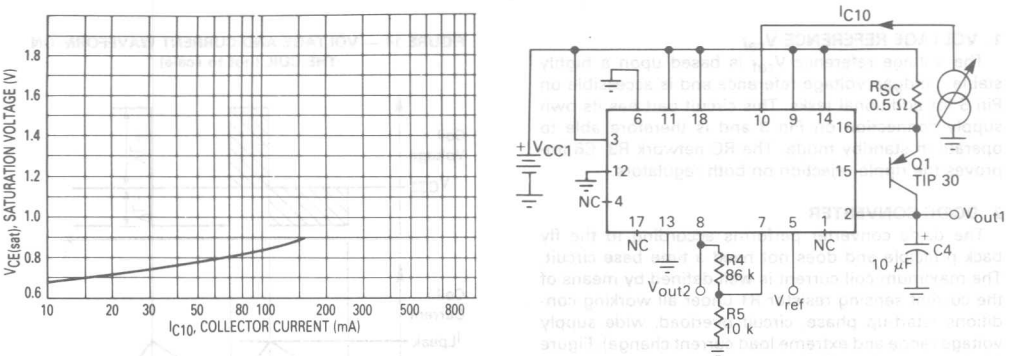


FIGURE 11 — RECTIFIER CHARACTERISTICS

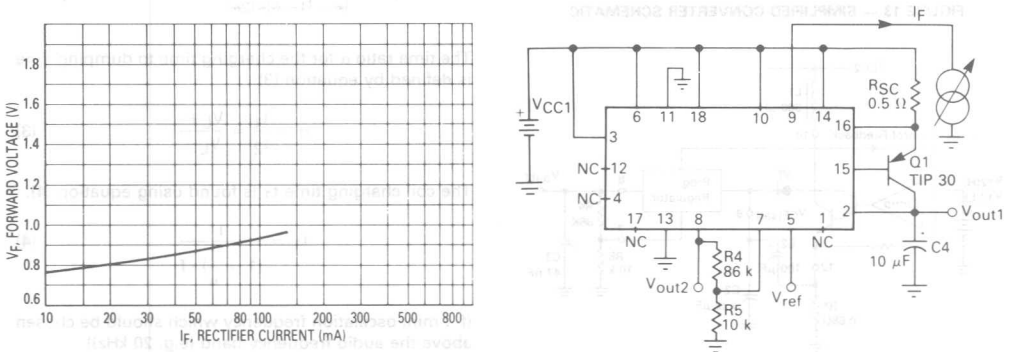
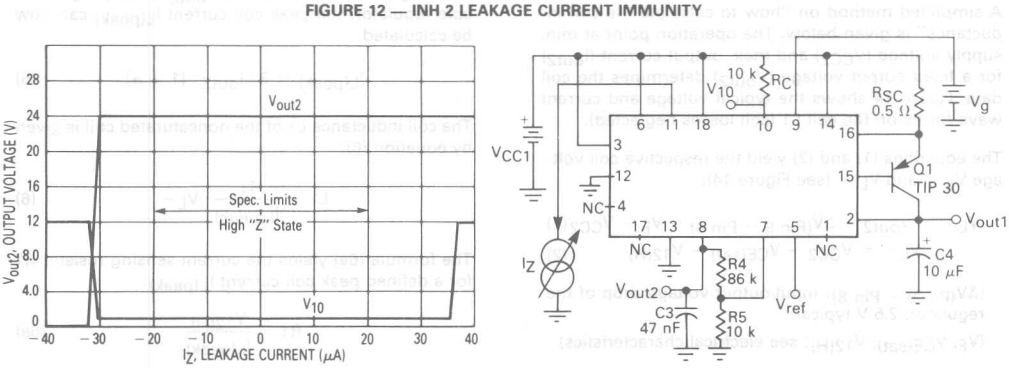


FIGURE 12 — INH 2 LEAKAGE CURRENT IMMUNITY



3

APPLICATIONS INFORMATION
(See Figure 18)

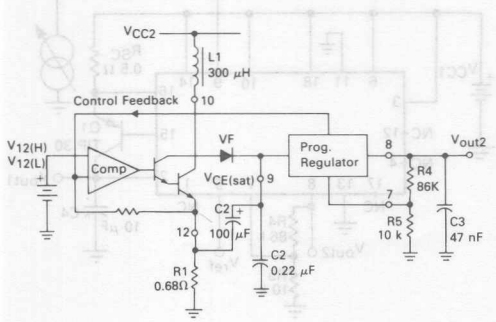
1. VOLTAGE REFERENCE V_{ref}

The voltage reference V_{ref} is based upon a highly stable bandgap voltage reference and is accessible on Pin 5 for additional tasks. This circuit part has its own supply connection on Pin 3 and is therefore able to operate in standby mode. The RC network R3, C6 improves the ripple rejection on both regulators.

2. DC/DC CONVERTER

The dc/dc converter performs according to the fly back principle and does not need a time base circuit. The maximum coil current is well defined by means of the current sensing resistor R1 under all working conditions (start-up phase, circuit overload, wide supply voltage range and extreme load current change). Figure 13 shows the simplified converter schematic:

FIGURE 13 — SIMPLIFIED CONVERTER SCHEMATIC



A simplified method on "how to calculate the coil inductance" is given below. The operation point at min. supply voltage (V_{CC2}) and max. output current (I_{out2}) for a fixed output voltage (V_{out2}) determines the coil data. Figure 14 shows the typical voltage and current wave forms on the coil L1 (coil losses neglected).

The equations (1) and (2) yield the respective coil voltage V_L- and V_L+ (see Figure 14):

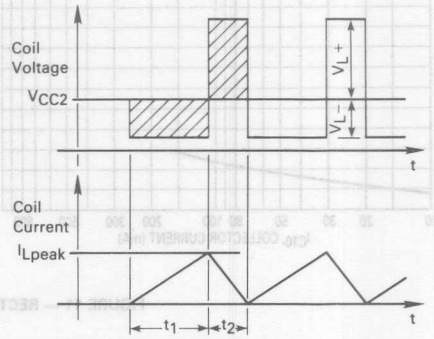
$$V_L+ = V_{out2} + \Delta V_{(Pin\ 9\ -\ Pin\ 8)} + V_F - V_{CC2} \quad (1)$$

$$V_L- = V_{CC2} - V_{CE(sat)} - V_{12(H)} \quad (2)$$

($\Delta V_{(Pin\ 9\ -\ Pin\ 8)}$: input/output voltage drop of the regulator, 2.5 V typical)

(V_F, $V_{CE(sat)}$, $V_{12(H)}$: see electrical characteristics)

FIGURE 14 — VOLTAGE AND CURRENT WAVEFORM ON THE COIL (not to scale)



The time ratio α for the charging time to dumping time is defined by equation (3):

$$\alpha = \frac{t_1}{t_2} = \frac{V_L+}{V_L-} \quad (3)$$

The coil charging time t_1 is found using equation (4):

$$t_1 = \frac{1}{(1 + \frac{1}{\alpha}) \cdot f} \quad (4)$$

(f : min. oscillation frequency which should be chosen above the audio frequency band (e.g. 20 kHz))

Knowing the dc output current I_{out2} of the programmable regulator, the peak coil current $I_{L(peak)}$ can now be calculated:

$$I_{L(peak)} = 2 \cdot I_{out2} \cdot (1 + \alpha) \quad (5)$$

The coil inductance L1 of the nonsaturated coil is given by equation (6):

$$L1 = \frac{t_1}{I_{L(peak)}} \cdot V_L- \quad (6)$$

The formula (6a) yields the current sensing resister R1 for a defined peak coil current $I_{L(peak)}$:

$$R1 = \frac{V_{12(H)}}{I_{L(peak)}} \quad (6a)$$

In order to limit the by-pass current through capacitor C7 during the energy dumping phase the value C2>>C7 should be implemented.

For all other operation conditions, the feedback signal from the programmable voltage regulator controls the activity of the converter.

3. PROGRAMMABLE VOLTAGE REGULATOR

This series voltage regulator is programmable by the voltage divider R4, R5 for a nominal output voltage $6.0\ V \leq V_{out2} \leq 30\ V$.

$$R4 = \frac{(V_{out2} - V_{ref\ nom}) \cdot R5}{V_{ref\ nom}} \quad (7)$$

($R5 = 10\ k$, $V_{ref\ nom} = 2.5\ V$)

Current limitation and thermal shutdown capability are standard features of this regulator. The voltage drop $\Delta V_{(Pin\ 9\ -\ Pin\ 8)}$ across the series pass transistor generates the feedback signal to control the dc/dc converter (see Figure 13).

4. CONTROL INPUTS INH1, INH2

The dc/dc converter and/or the regulator V_{out2} are remote controllable through the TTL, MOS compatible inhibit inputs INH1 and INH2 where the latter is a 3-level detector (Logic "0", high impedance "Z", Logic "1"). Both inputs are setup to provide the following truth table:

FIGURE 15 — INH1, INH2 TRUTH TABLE

Mode	INH1	INH2	V_{out2}	dc/dc
1	0	0	OFF	INT
2	0	High "Z"	V_{out2}	ON
3	0	1	V_{out2}	INT
4	1	0	OFF	INT
5	1	High "Z"	5.0 V	ON
6	1	1	5.0 V	INT

INT: Intermittent operation of the converter means that the converter operates only if $V_{CC2} < V_{out2}$.

ON: The converter loads the storage capacitor C2 to its full charge (V_9 = 33 V), allowing fast response time of the regulator V_{out2} when addressed by the control software.

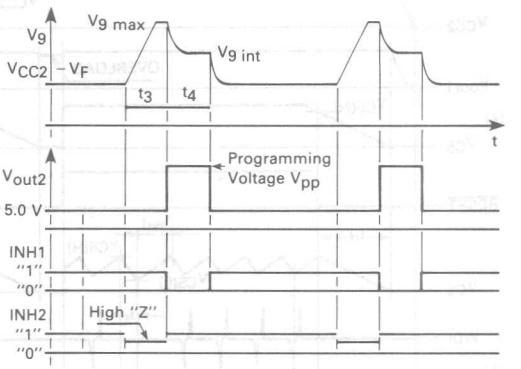
OFF: High impedance (internal resistor 10 k to ground)

Figure 16 represents a typical timing diagram for an E²PROM programming sequence in a microprocessor based system. The high "Z" state enables the dc/dc converter to ramp during t_3 to the voltage V_9 at Pin 9 to a high level before the write cycle takes place in the memory.

5. MICROPROCESSOR SUPPLY REGULATOR

Together with an external PNP power transistor (Q1), a 5.0 V supply exhibiting low voltage drop is obtained to power microprocessor systems and auxilliary circuits. Using a power Darlington with adequate heat sink in the output stage boosts the output current I_{out1} above 1 amp.

FIGURE 16 — TYPICAL E²PROM PROGRAMMING SEQUENCE (not to scale)



The current limitation circuit measures the emitter current of Q1 by means of the sensing resistor R_{SC}.

$$R_{SC} = \frac{V_{RSC}}{I_E} \quad (8)$$

(I_E: emitter current of Q1)

(V_{RSC}: threshold voltage (see electrical characteristics))

The voltage protection circuit performs a fold-back characteristic above a nominal operating voltage $V_{CC2} \geq 18\ V$.

6. DELAY AND WATCHDOG CIRCUIT

The under voltage monitor supervises the power supply V_{out1} and releases the delay circuit $\overline{RESET}$ as soon as the regulator output reaches the microprocessor operating range (e.g. $V_{LOW} \geq 0.93 \cdot V_{out1(nom)}$). The $\overline{RESET}$ output has an open-collector and may be connected in a "wired-OR" configuration.

The watchdog circuit consists of a retriggerable monostable with a negative edge sensitive control input WDI. The watchdog feature may be disabled by means of the watchdog select input $\overline{WDS}$ driven to a "1". Figure 17 displays the typical $\overline{RESET}$ timing diagram.

The commuted current source I_{C5} on Pin 17, threshold voltage $V_{C5(L)}$, $V_{C5(H)}$ and an external capacitor C5 define the $\overline{RESET}$ delay and the watchdog timing. The relationship of the timing signals are indicated by the equations (9) to (11).

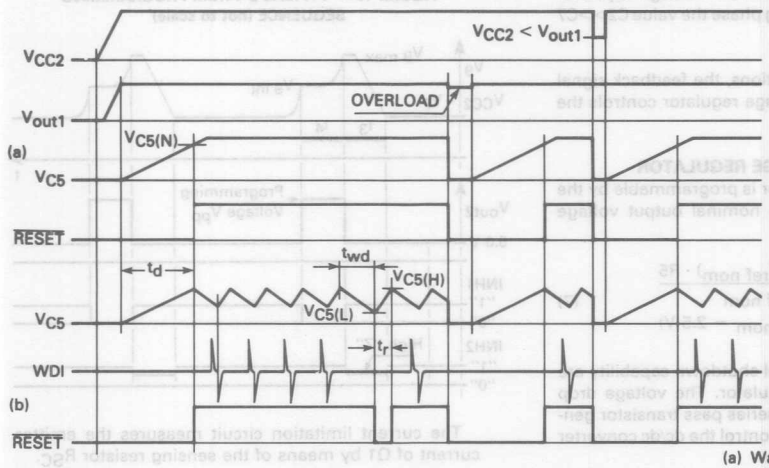
$\overline{RESET}$ delay: $$t_d = \frac{C5 \cdot V_{C5(H)}}{|I_{C5}|} \quad (9)$$

Watchdog time-out: $$t_{wd} = \frac{C5 \cdot (V_{C5(H)} - V_{C5(L)})}{5 \cdot I_{C5}} \quad (10)$$

Watchdog $\overline{RESET}$: $$t_r = \frac{C5 \cdot (V_{C5(H)} - V_{C5(L)})}{50 \cdot |I_{C5}|} \quad (11)$$

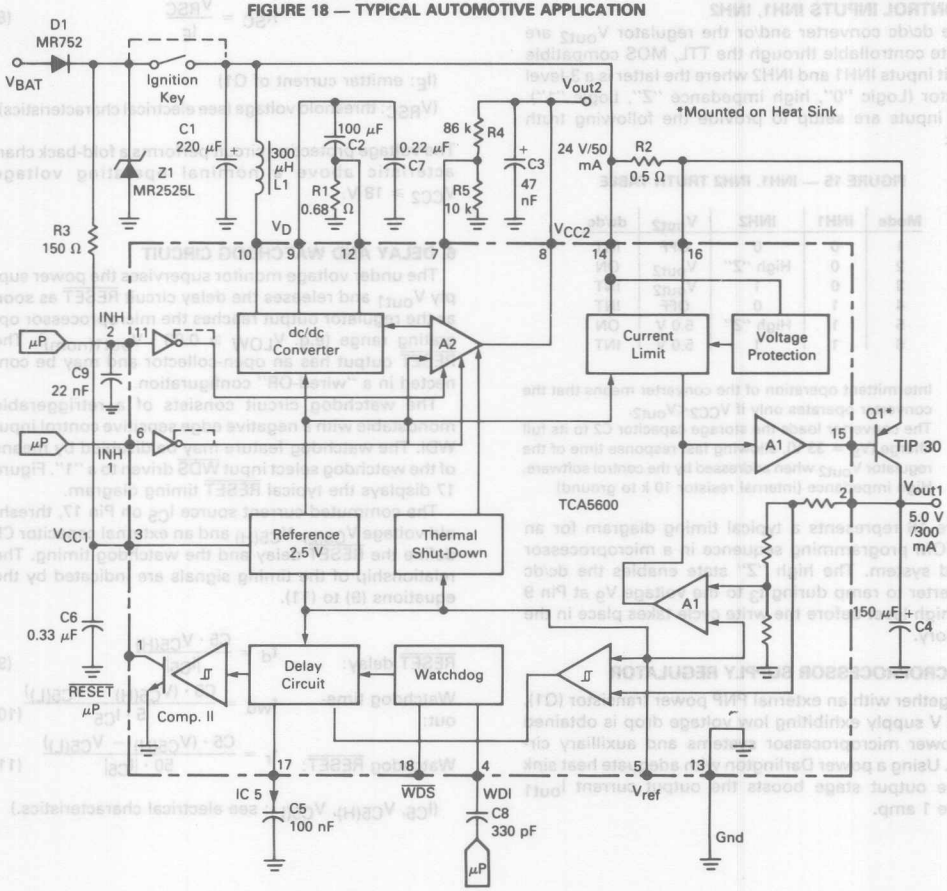
(I_{C5}, $V_{C5(H)}$, $V_{C5(L)}$: see electrical characteristics.)

(not to scale)



(a) Watchdog inhibited, $\overline{WDS}$ = "1"
(b) Watchdog operational, $\overline{WDS}$ = "0"

FIGURE 18 — TYPICAL AUTOMOTIVE APPLICATION



MOTOROLA

TDA4601
TDA4601B

3

Data Sheet

CONTROL IC FOR LINE ISOLATED RINGING CHOKE FLYBACK CONVERTER

The bipolar integrated circuit TDA4601 drives, regulates and monitors the switching transistor in a power supply based on ringing choke flyback principle.

Due to the wide regulating range and the high voltage stability during large load changes, SMPS for Hi-Fi equipment and active loudspeakers can be realised as well as applications in TV receivers and video recorders.

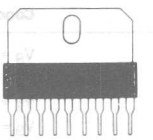
The TDA4601 is available in SIP9 and DIL18 plastic medium-power package. The temperature operating range is -15°C to +85°C.

- Wide operational range.
- High voltage stability even at high load changes.
- Direct control of switching transistor.
- Low start-up current.
- Linear foldback of the overload characteristic.
- Base drive proportional to the current through the power switching transistor.
- Stand-by mode 3.5W into the external load.
- Inhibition capability (TTL compatible).
- Under voltage lockout.

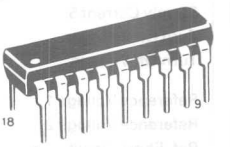
For application details see ANE002

FLYBACK CONVERTER REGULATION CONTROL CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT

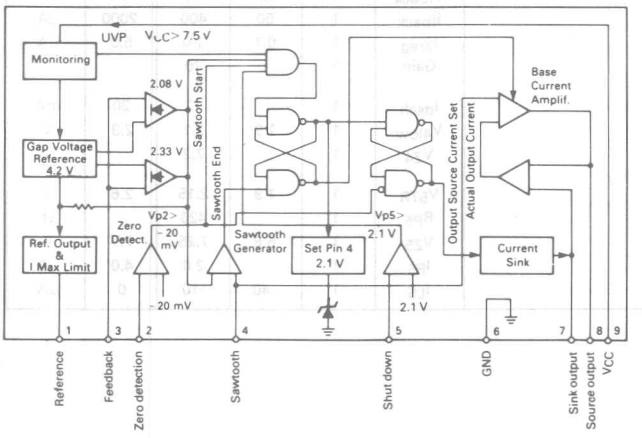


SIP 9
PLASTIC MEDIUM POWER PACKAGE
CASE 762



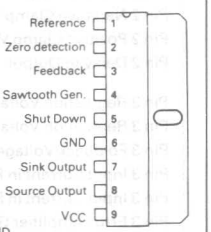
DIL 18
B SUFFIX
PLASTIC PACKAGE
CASE 707

Simplified Block Diagram



PIN ASSIGNMENTS

SIP 9



DIL 18



The flag is mechanically connected to pin 10 thru pin 18

ORDERING INFORMATION

Device	Temperature Range	Package
TDA4601	-15°C to +85°C	Plastic SIP
TDA4601B	-15°C to +85°C	Plastic DIP

3

MAXIMUM RATINGS

Rating		Value	Unit	Rating			Value	Unit
Supply voltage	V_9	20	V	Sink output		I_7	- 1.5	A
Sink output voltage	V_7	0 to V_9	V					
	$V_7 - V_8$	±6	V	Junction temperature		T_j	+150	°C
Reference output	I_1	-10 to +1	mA	Storage temperature		T_{stg}	-40 to +125	°C
Zero crossing	I_2	-3 to +3	mA	Thermal resistance (junction to air)	SIP9	R_{thJA}	70	°C/W
Control amplifier	I_3	-3 to 0	mA	Thermal resistance (junction to case)	DIL	R_{thJA}	85	°C/W
Collector current	I_4	-2 to +5	mA		SIP9	R_{thJC}	15	°C/W
Trigger input	I_5	-2 to +3	mA					

ELECTRICAL CHARACTERISTICS (T_A = 25°C. Test configurations Fig. 1 / Fig. 2)
V_9 = 15 V, V_5 = 3 V, unless otherwise specified.

Test Name	Condition Values	Symbol	Fig. No.	Min	Typ	Max	Unit
Supply Current 1	V_9 = 3 V	I_{CC1}	1			1.6	mA
Supply Current 2	V_9 = 5 V	I_{CC2}	1		1.5	2.0	mA
Supply Current 3	V_9 = 10 V	I_{CC3}	1		2.2	3.2	mA
Supply Current 4	V_9 = 12.3 V	I_{CC4}	1	10.0	20.0		mA
Supply Current 5	V_9 = 20 V	I_{CC5}	1	10.0	21.0		mA
Turn On Voltage	V_2 = 0 V	V_{CCon}	1	11.3	11.8	12.3	V
Turn Off Voltage	V_2 = 0 V	V_{CCoff}	1	6.5	7.0	7.5	V
Reference Voltage 1	V_9 = 20 V	V_{ref1}	1	4.0	4.35	4.5	V
Reference Voltage 2	V_9 = 15 V, I_1 = -5mA	V_{ref2}	1	4.0	4.3	4.5	V
Ref. Short Circuit	V_9 = 20 V	I_{SC}	1	5.0	7.0	20.0	mA
Reference Voltage 3	V_9 = 20 V, I_1 = -5 mA	V_{ref3}	1	4.0	4.3	4.5	V
Reference Voltage 4	V_9 = 10 V, I_9 = -5 mA	V_{ref4}	1	4.0	4.25	4.5	V
Line Regulation	$V_{ref3} - V_{ref4}$	RGLN	1		50.0	100.0	mV
Average Temperature Coefficient		TCV_{ref}	1		0.5		mV/°C
Pin 2 Offset Voltage		V_{IO2}	1	-60	-20	-5.0	mV
Pin 2 Negative Clamp Voltage		V_{2-}	1		-0.3		V
Pin 2 Positive Clamp Voltage		V_{2+}	1		0.8		V
Pin 2 Delay to Output		t_{DO}	1		700		nS
Pin 3 Regulation Voltage for V_{pin4} = 4 V		V_{reg1}	1	2.08	2.15	2.23	V
Pin 3 Regulation Voltage for V_{pin4} = 2.6 V		V_{reg2}	1	2.06	2.13	2.21	V
Pin 3 Foldback Voltage		V_{fback}	1	2.4	2.5	2.7	V
Pin 3 Input Current in Foldback Mode		I_{fback}	1	50	400	2000	µA
Pin 3 Input Current in Regulation Mode		I_{3reg}	1	0.1	1.0	5.0	µA
Pin 3 Error Amplifier Gain		Gain	1		70		
Pin 4 Discharge Current		I_{dsch}	1		12	20	mA
Pin 4 Voltage Low		V_{4low}	1	1.9	2.1	2.3	V
Pin 4 Clamp Voltage I_4 = 1 mA		V_{Z4}	1		7.2		V
Pin 5 Trigger Voltage		V_{5TR}	1	1.9	2.15	2.6	V
Pin 5 Internal Resistance V_5 = 1.8 V		R_{P5}	1		420		Ω
Pin 5 Clamp Voltage I_5 = 80 mA		V_{Z5}	1	6.8	7.25	7.7	V
Pin 5 Input Current		I_{P5}	1		2.0	4.0	µA
Pin 5 Leakage Current V_5 = 0 V		I_{L5}	1	-40	-10	0	µA

ELECTRICAL CHARACTERISTICS (T_A = 25°C. Test configurations Fig. 1 / Fig. 2)
V_9 = 15 V, V_2 = 0 V, V_5 = 3 V, unless otherwise specified.

Test Name — Condition Values	Symbol	Fig. No.	Min	Typ	Max	Unit
Output Voltage High V_{P8} at I_{out} = 0.2 A	V_{OH1}	1	13	13.4		V
Output Voltage High V_{P8} at I_{out} = 1 A	V_{OH2}	1	12	12.6		V
Output Voltage Low V_{P7} at I_{out} = -0.2 A	V_{OL1}	1		1.6	2.0	V
Output Voltage Low V_{P7} at I_{out} = -1 A	V_{OL2}	1		2.3	3.0	V
Output Current Limit for V_{P4} = 3.3 V	I_L	2	0.3	0.45	0.55	A

ELECTRICAL CHARACTERISTICS USING APPLICATION SIMULATION CIRCUIT (Fig. 3)
Normal Operation (V_9 = 10 V; V_{reg} = -10 V; V_{pulse} = ±0.5 V; f = 20 kHz; duty cycle ½) after the turn-on process completed.

Range of Operation		Symbol	Fig. No.	Typ	Unit
Current Consumption	V_{reg} = -10 V	I_9	3	105	mA
	V_{reg} = 0 V	I_9	3	50	mA
Collector Current Balancing Voltage	V_{reg} = 0 V	V_4	3	2.6	V
	V_{reg} = 0 V/-10 V	ΔV_4	3	0.4	V
Output Voltages	V_{reg} = 0 V	V_7	3	4.3	V
	V_{reg} = 0 V	V_8	3	4.4	V
	V_{reg} = 0 V/-10 V	ΔV_8	3	1.7	V

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise stated) (Fig. 18)

Characteristics	Symbol	Fig. No.	Min	Typ	Max	Unit
Turn-on time (secondary voltages)				350	450	ms
Voltage Change						
When S_3 = closed ($\triangle P_3$ = 19 W)	ΔV_2	18		100	500	mV
When S_2 = closed ($\triangle P_2$ = 15 W)	ΔV_2			500	1000	mV
Standby operation (minimum secondary power: 3 Watts)						
When S_1 = open	ΔV_2			20	30	V
Switching frequency during standby mode	f		70	75		kHz
Primary power consumption during standby mode	P_{prim}			10	15	VA
The heat sink must be optimized, taking the maximum data (T_j, R_{thJC}, T_{amb}) into consideration.						

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Figure 1

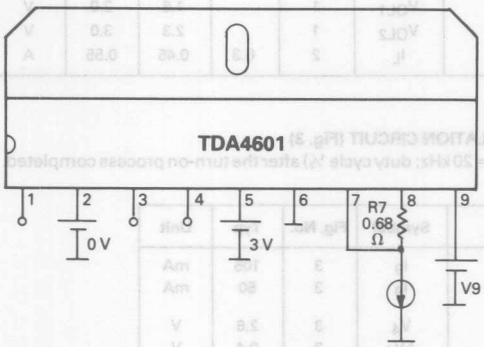


Figure 2

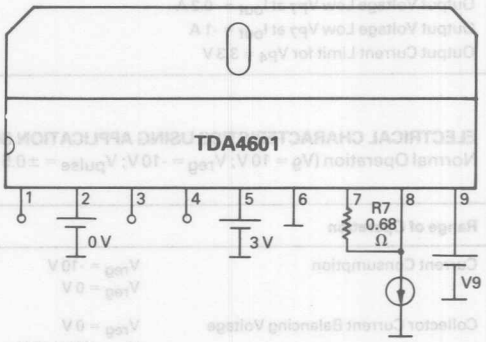


Figure 3 Application Simulation Circuit

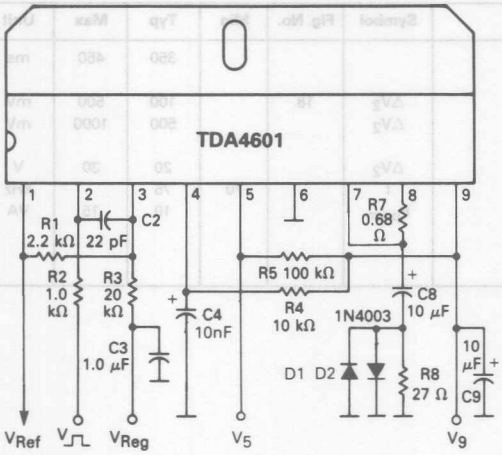


Figure 4 Test Diagram: Normal Operation

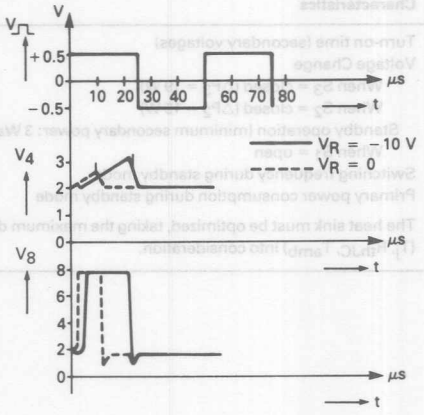
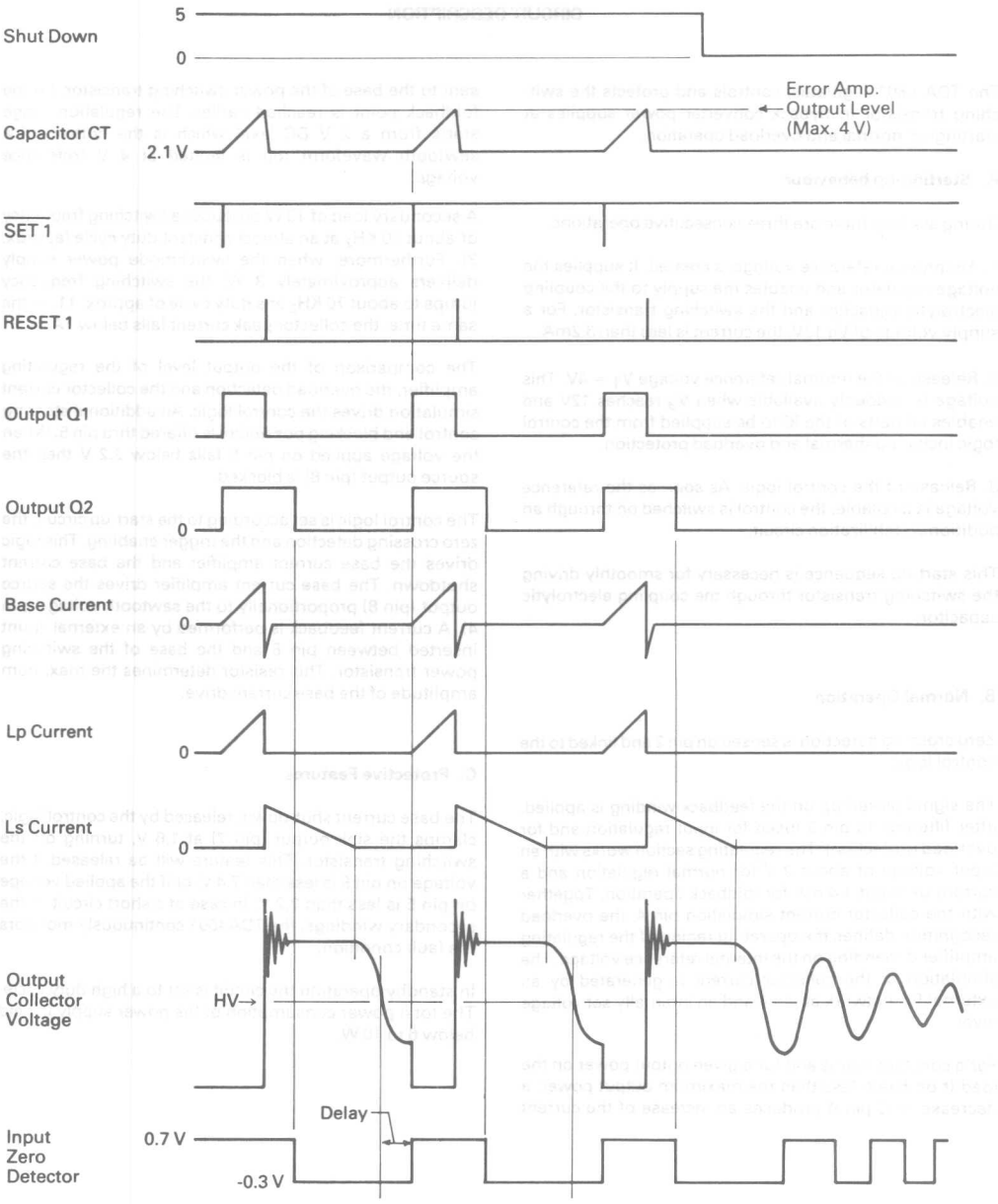


Figure 5 - TDA4601 Timing Diagram - Normal Operation

(see in conjunction with Fig. 20 - Representative Block Diagram and Typical Application)



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CIRCUIT DESCRIPTION

The TDA 4601 regulates, controls and protects the switching transistor in flyback converter power supplies at starting-up normal and overload operation.

A. Starting-up behaviour

During start-up there are three consecutive operations:

1. An internal reference voltage is created. It supplies the voltage regulator and enables the supply to the coupling electrolytic capacitor and the switching transistor. For a supply voltage of V_9 12V, the current is less than 3.2mA.

2. Release of the internal reference voltage V_1 = 4V. This voltage is suddenly available when V_9 reaches 12V and enables all parts of the IC to be supplied from the control logic including thermal and overload protection.

3. Release of the control logic. As soon as the reference voltage is available, the control is switched on through an additional stabilization circuit.

This start-up sequence is necessary for smoothly driving the switching transistor through the coupling electrolytic capacitor.

B. Normal Operation

Zero crossing detection is sensed on pin 2 and linked to the control logic.

The signal picked up on the feedback winding is applied, after filtering, to pin 3 (used for input regulation and for overload protection). The regulating section works with an input voltage of about 2 V for normal regulation and a current of about 1.4 mA for foldback operation. Together with the collector current simulation pin 4, the overload recognition defines the operating region of the regulating amplifier depending on the internal reference voltage. The simulation of the collector current is generated by an external RC network at pin 4 and an internally set voltage level.

For a constant mains and for a given output power on the load (t on fixed) less than the maximum output power, a decrease of C pin 4 produces an increase of the current sent to the base of the power switching transistor. So the foldback point is reached earlier. The regulation range starts from a 2 V DC level which is the bottom of a sawtooth waveform top is limited at 4 V (reference voltage).

A secondary load of 19 W produces a switching frequency of about 50 KH_z at an almost constant duty cycle (approx. 3). Furthermore, when the switchmode power supply delivers approximately 3 W, the switching frequency jumps to about 70 KH_z at a duty cycle of approx. 11. At the same time, the collector peak current falls below 1A.

The comparison of the output level of the regulating amplifier, the overload detection and the collector current simulation drives the control logic. An additional steering control and blocking possibility is offered thru pin 5. When the voltage applied on pin 5 falls below 2.2 V then the source output (pin 8) is blocked.

The control logic is set according to the start-up circuit, the zero crossing detection and the trigger enabling. This logic drives the base current amplifier and the base current shutdown. The base current amplifier drives the source output (pin 8) proportionally to the sawtooth voltage (pin 4). A current feedback is performed by an external shunt inserted between pin 8 and the base of the switching power transistor. This resistor determines the maximum amplitude of the base current drive.

C. Protective Features

The base current shut-down, released by the control logic, clamps the sink output (pin 7) at 1.6 V, turning off the switching transistor. This feature will be released if the voltage on pin 9 is less than 7.4 V, or if the applied voltage on pin 5 is less than 2.2 V. In case of s short circuit of the secondary windings, the TDA4601 continuously monitors the fault condition.

In standby operation the circuit is set to a high duty cycle. The total power consumption of the power supply is held below 6 to 10 W.

PINS FUNCTION - DESCRIPTION

Pin 1 Reference V_{ref}: 4.21 V.
This output furnishes a voltage reference for the Error Amplifier Non-inverting input. The same voltage is used for the internal reference.

Pin 2 Zero detector.
This is the Inverting Input of the Zero Detector Comparator. It is normally connected to the feedback through an RC network. During a normal operation each positive edge starts a sawtooth. Gives the information: "demagnetisation complete" to the logic.

Pin 3 Feedback.
This is the non-inverting input of the Error Amplifier. It is normally connected to the 2.1 V reference through a bridge resistor and an RC network.

Pin 4 Sawtooth.
Sawtooth signal is programmed by connecting resistor RT to HV and capacitor CT to ground. The voltage at Pin 4 is related to the inductor current.

Pin 5 Shut Down.
As soon as $V_{P5} < 2.1$ V the operation stops. The input is then held low via 300 Ω (typical) resistor. To restart V_{P5} must be pulled to a voltage > 2.1 V, $V_{ref}/2$ (typical). Therefore it depends if an ideal source is available to set the voltage (in which case there are no problems) or a source with a non zero internal resistance. If the voltage source has an internal resistor R_i, the voltage source has to reach:

$$V = [(R_i + 300) / 300] \times 2.1$$

to restart (hysteresis).

Pin 6 Ground.
This is the circuit ground.

Pin 7 Sink current.
This is the sink current output. It allows the output transistor to be turned off through the 100 µF capacitor.

Pin 8 Source current.
A resistor connected between Pin 7 and Pin 8 allows transformation of the ramp voltage (Pin 4) into a ramp current. This output is a current source (during t_{on}).

Pin 9 V_{CC}.
This pin is the positive supply of the control IC. The controller is functional over a minimum V_{CC} range of 7.5 V to 11.3 V. This pin is normally connected to main line through a diode and a 10 kΩ resistor (3 W) and a 100 µF tank capacitor.

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Figure 6 - Frequency vs Output Power

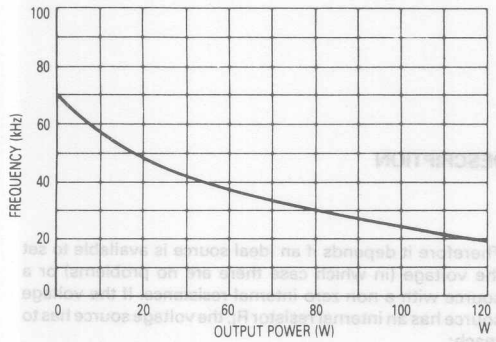


Figure 7 - Efficiency vs Output Power

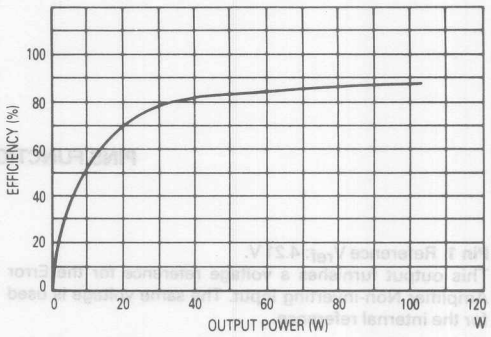


Figure 8 - Load Characteristics $V_2 = f(I_{V2})$

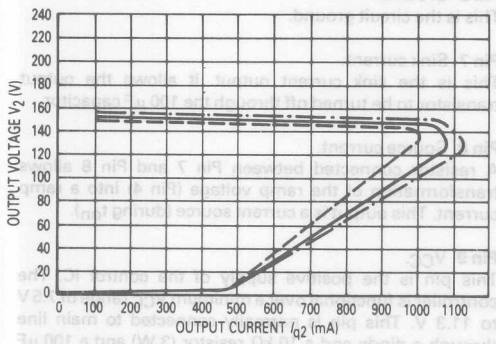


Figure 9 - Output Voltage V_2 (mains change)

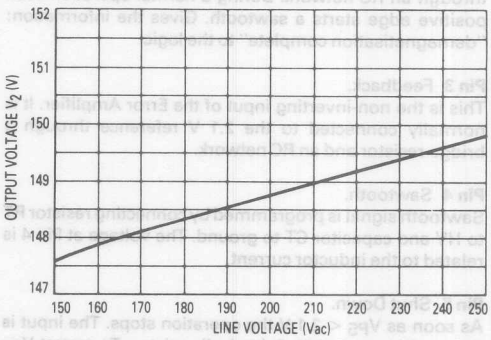


Figure 10 - Voltage Reference vs Temperature

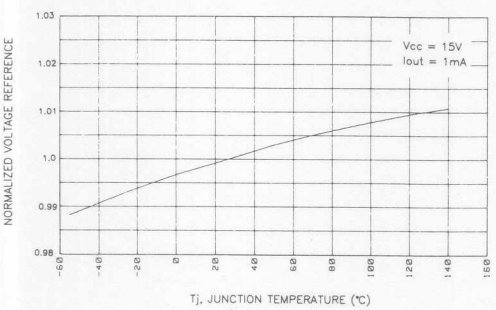


Figure 11 - Impedance Pin 3

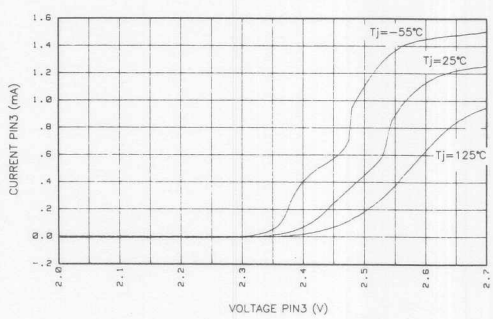


Figure 12 - Line Regulation

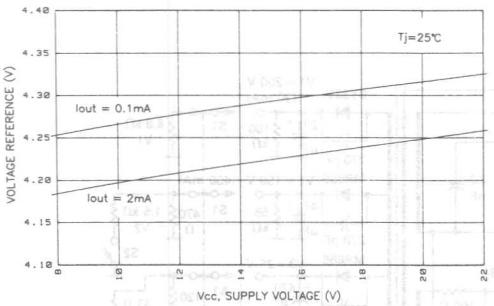


Figure 13 - Error Amplifier Gain

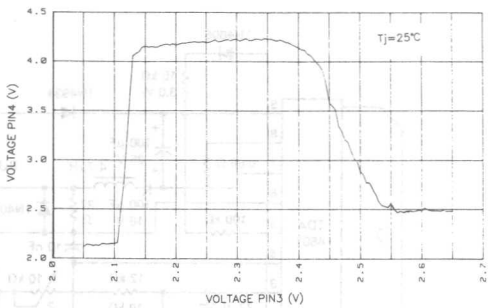


Figure 14 - Load Regulation

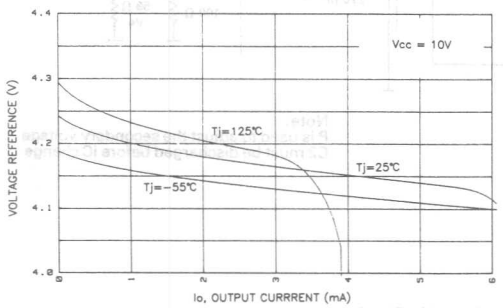


Figure 15 - Regulation Gain

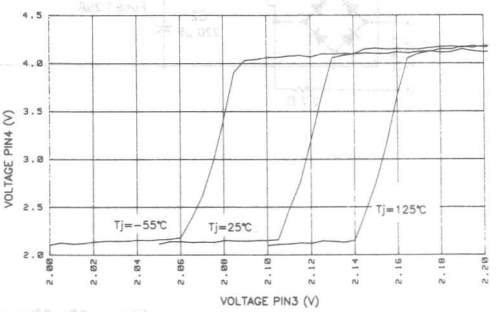


Figure 16 - Supply Current vs Supply Voltage

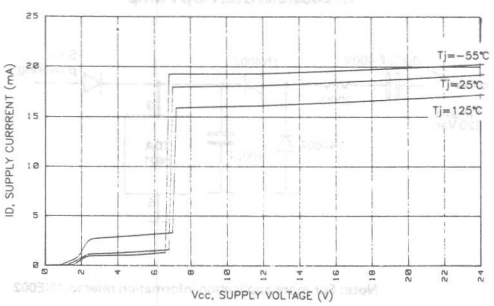
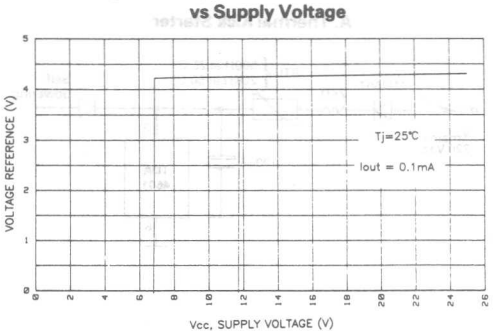
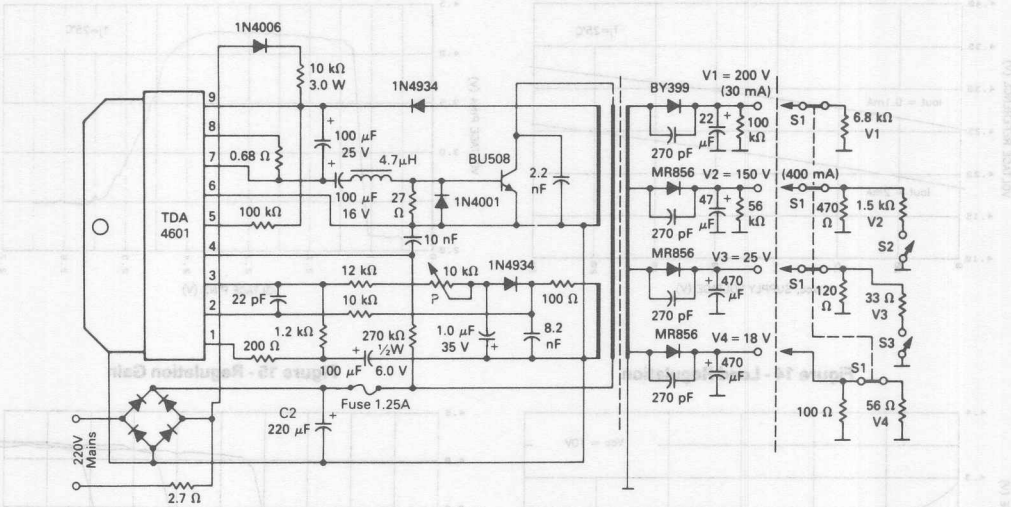


Figure 17 - V_{ref} Under Voltage Lockout vs Supply Voltage



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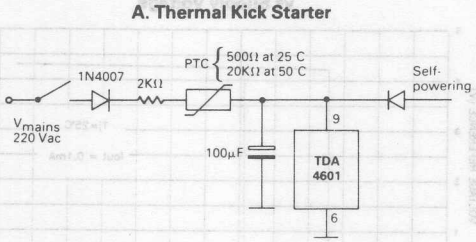
Figure 18 - Typical Application



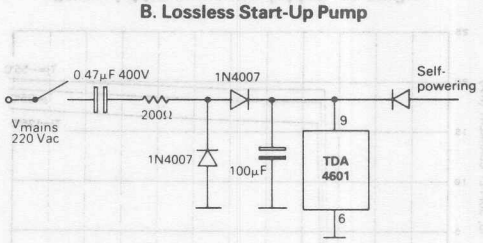
Note:
P is used to adjust the secondary voltage
C2 must be discharged before IC change

Figure 19 - Alternative Start-Up Circuit

A. Thermal Kick Starter



B. Lossless Start-Up Pump



Note: For more application information refer to ANE002

TEST CIRCUIT AND TYPICAL APPLICATION (see Fig. 18)

This application circuit shown in figure 18 represents a blocking converter for color TV sets with 30 W to 120 W of output power and mains voltages from 160 to 270 V.

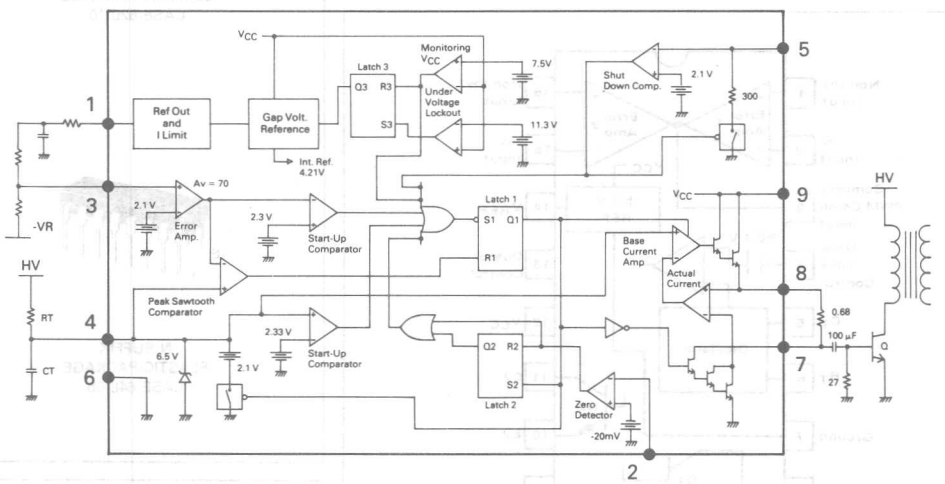
In spite of regulation on the primary side, good voltage stability of the various secondary voltages is achieved even with large load changes.

For mains isolation and transformation to the desired secondary voltages, a transformer with ferrite core is used.

SPECIAL FEATURES OF THE FLYBACK CONVERTER POWER, SUPPLY USING THE TDA4601

- Direct driving of the power switching transistor
- Low starting current, defined starting behaviour also at slowly rising mains voltage
- Short-circuit proof and open-loop resistant circuit. In both cases a power of only 6 to 10 W is consumed. Linear foldback characteristic at overload.
- Automatic restart after elimination of the overload.
- Efficiency of more than 80% at an output power of 40 to 100 W.
- Frequency of oscillation between 20kHz (100W) and 70kHz (without load).
- Simple RF 1 suppression.
- Good regulation of load current and mains voltage variations. At a mains voltage variation between 170 and 240 V the output voltage of 150V will change only by about 2V.

Figure 20 - Representative Block Diagram and Typical Application



3

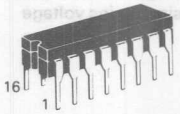
SWITCHMODE PULSE WIDTH MODULATION CONTROL CIRCUITS

The TL494 is a fixed frequency, pulse width modulation control circuit designed primarily for Switchmode power supply control. This device features:

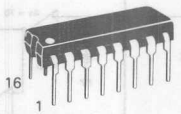
- Complete Pulse Width Modulation Control Circuitry
- On-Chip Oscillator With Master Or Slave Operation
- On-Chip Error Amplifiers
- On-Chip 5 Volt Reference
- Adjustable Dead-Time Control
- Uncommitted Output Transistors Rated to 500 mA Source Or Sink
- Output Control For Push-Pull Or Single-Ended Operation
- Undervoltage Lockout

SWITCHMODE PULSE WIDTH MODULATION CONTROL CIRCUITS

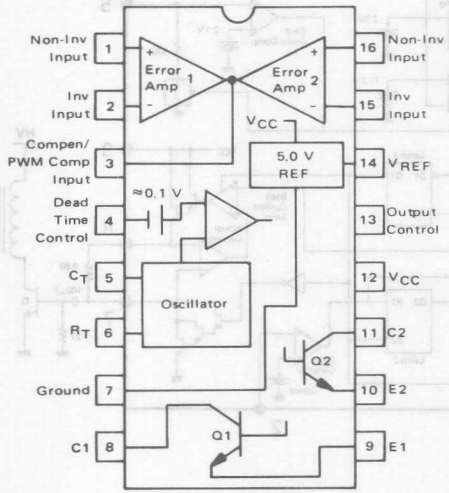
SILICON MONOLITHIC INTEGRATED CIRCUITS



J SUFFIX
CERAMIC PACKAGE
CASE 620-10



N SUFFIX
PLASTIC PACKAGE
CASE 648-06



(top view)

The TL494C is specified over the commercial operating range of 0°C to 70°C. The TL494I is specified over the industrial range of −25°C to 85°C. The TL494M is specified over the full military range of −55°C to 125°C.

ORDERING INFORMATION

Device	Temperature Range	Package
TL494CN	0° to +70°C	Plastic DIP
TL494CJ	0° to +70°C	Ceramic DIP
TL494IN	−25° to +85°C	Plastic DIP
TL494IJ	−25° to +85°C	Ceramic DIP
TL494MJ	−55° to +125°C	Ceramic DIP

FIGURE 1 — BLOCK DIAGRAM

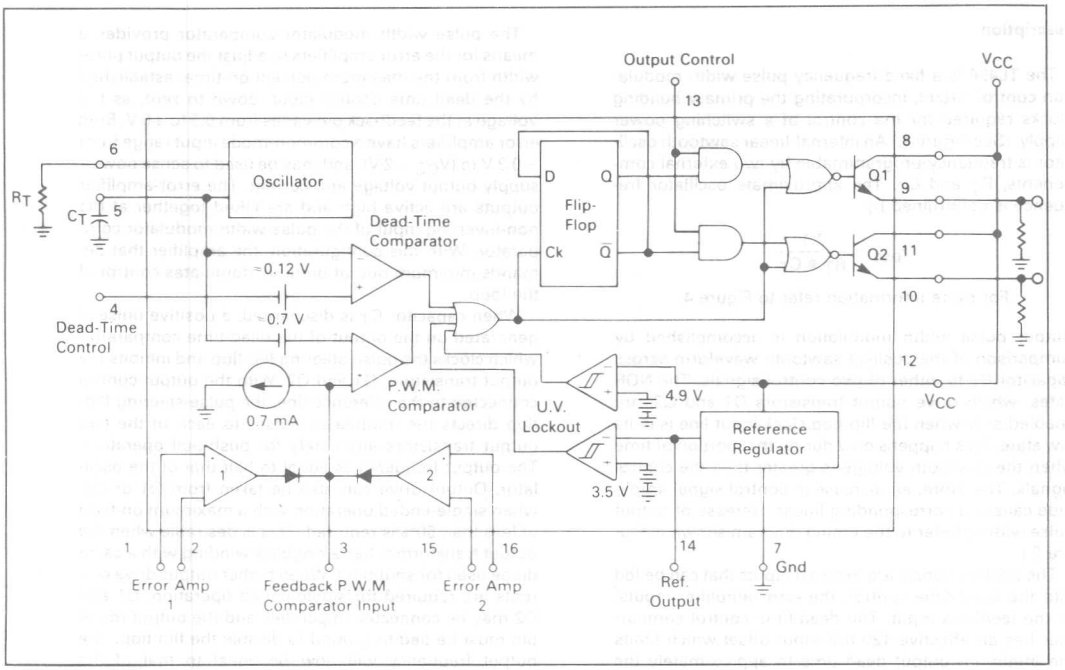
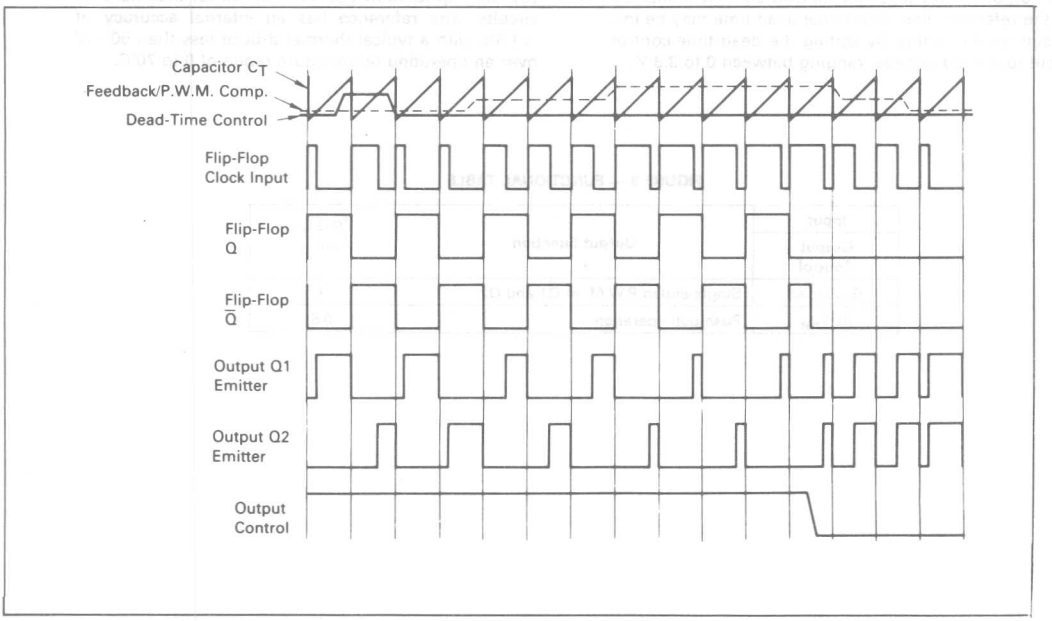


FIGURE 2 — TIMING DIAGRAM



Description

The TL494 is a fixed-frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply. (See Figure 1.) An internal-linear sawtooth oscillator is frequency-programmable by two external components, R_T and C_T. The approximate oscillator frequency is determined by:

$$f_{osc} \approx \frac{1.1}{R_T \bullet C_T}$$

For more information refer to Figure 4.

Output pulse width modulation is accomplished by comparison of the positive sawtooth waveform across capacitor C_T to either of two control signals. The NOR gates, which drive output transistors Q1 and Q2, are enabled only when the flip-flop clock-input line is in its low state. This happens only during that portion of time when the sawtooth voltage is greater than the control signals. Therefore, an increase in control-signal amplitude causes a corresponding linear decrease of output pulse width. (Refer to the timing diagram shown in Figure 2.)

The control signals are external inputs that can be fed into the dead-time control, the error amplifier inputs, or the feedback input. The dead-time control comparator has an effective 120 mV input offset which limits the minimum output dead time to approximately the first 4% of the sawtooth-cycle time. This would result in a maximum duty cycle on a given output of 96% with the output control grounded, and 48% with it connected to the reference line. Additional dead time may be imposed on the output by setting the dead time-control input to a fixed voltage, ranging between 0 to 3.3 V.

The pulse width modulator comparator provides a means for the error amplifiers to adjust the output pulse width from the maximum percent on-time, established by the dead time control input, down to zero, as the voltage at the feedback pin varies from 0.5 to 3.5 V. Both error amplifiers have a common-mode input range from −0.3 V to (V_{CC} − 2 V), and may be used to sense power-supply output voltage and current. The error-amplifier outputs are active high and are ORed together at the non-inverting input of the pulse-width modulator comparator. With this configuration, the amplifier that demands minimum output on time, dominates control of the loop.

When capacitor C_T is discharged, a positive pulse is generated on the output of the dead-time comparator, which clocks the pulse-steering flip-flop and inhibits the output transistors, Q1 and Q2. With the output-control connected to the reference line, the pulse-steering flip-flop directs the modulated pulses to each of the two output transistors alternately for push-pull operation. The output frequency is equal to half that of the oscillator. Output drive can also be taken from Q1 or Q2, when single-ended operation with a maximum on-time of less than 50% is required. This is desirable when the output transformer has a ringback winding with a catch diode used for snubbing. When higher output-drive currents are required for single-ended operation, Q1 and Q2 may be connected in parallel, and the output-mode pin must be tied to ground to disable the flip-flop. The output frequency will now be equal to that of the oscillator.

The TL494 has an internal 5 V reference capable of sourcing up to 10 mA of load current for external bias circuits. The reference has an internal accuracy of ±1.5% with a typical thermal drift of less than 50 mV over an operating temperature range of 0 to 70°C.

FIGURE 3 — FUNCTIONAL TABLE

Input Output Control	Output Function	$\frac{f_{out}}{f_{osc}}$ =
Grounded	Single-ended P.W.M. at Q1 and Q2	1
At V_{ref}	Push-pull operation	0.5

MAXIMUM RATINGS (Full operating ambient temperature range applies unless otherwise noted)

Rating	Symbol	TL494C	TL494I	TL494M	Unit
Power Supply Voltage	V_{CC}	42	42	42	V
Collector Output Voltage	V_{C1}, V_{C2}	42	42	42	V
Collector Output Current (each transistor) (1)	I_{C1}, I_{C2}	500	500	500	mA
Amplifier Input Voltage Range	V_{IR}	−0.3 to 42	−0.3 to 42	−0.3 to 42	V
Power Dissipation @ $T_A \leq 45°C$	P_D	1000	1000	1000	mW
Operating Junction Temperature Plastic Package Ceramic Package	T_J	 125 150	 125 150	 — 150	°C °C
Operating Ambient Temperature Range	T_A	0 to 70	−25 to 85	−55 to 125	°C
Storage Temperature Range Plastic Package Ceramic Package	T_{stg}	 −55 to 125 −65 to 150	 −55 to 125 −65 to 150	 — −65 to 150	°C

NOTE 1: Maximum thermal limits must be observed.

THERMAL CHARACTERISTICS

Characteristics	Symbol	N Suffix Plastic Package	J Suffix Ceramic Package	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	80	100	°C/W
Derating Ambient Temperature	T_A	45	50	°C

RECOMMENDED OPERATING CONDITIONS

Condition/Value	Symbol	TL494			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	7.0	15	40	V
Collector Output Voltage	V_{C1}, V_{C2}	—	30	40	V
Collector Output Current (each transistor)	I_{C1}, I_{C2}	—	—	200	mA
Amplifier Input Voltage	V_{in}	−0.3	—	V_{CC} − 2.0	V
Current Into Feedback Terminal	I_{fb}	—	—	0.3	mA
Reference Output Current	I_{ref}	—	—	10	mA
Timing Resistor	R_T	1.8	30	500	kΩ
Timing Capacitor	C_T	0.0047	0.001	10	μF
Oscillator Frequency	f_{osc}	1.0	40	200	kHz

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, C_T = 0.01 μF, R_T = 12 kΩ unless otherwise noted.)
For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies unless otherwise noted.

Characteristic	Symbol	TL494C,I			TL494M			Unit
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION								
Reference Voltage (I_O = 1.0 mA)	V_{ref}	4.75	5.0	5.25	4.75	5.0	5.25	V
Line Regulation (V_{CC} = 7.0 V to 40 V)	Reg_{line}	—	2.0	25	—	2.0	25	mV
Load Regulation (I_O = 1.0 mA to 10 mA)	Reg_{load}	—	3.0	15	—	3.0	15	mV
Short-Circuit Output Current (V_{ref} = 0 V)	I_{SC}	15	35	75	15	35	75	mA

For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies unless otherwise noted.

Characteristic	Symbol	TL494C,I			TL494M			Unit
		Min	Typ	Max	Min	Typ	Max	
OUTPUT SECTION								
Collector Off-State Current (V_{CC} = 40 V, V_{CE} = 40 V)	$I_{C(off)}$	—	2.0	100	—	2.0	100	μA
Emitter Off-State Current (V_{CC} = 40 V, V_C = 40 V, V_E = 0 V)	$I_{E(off)}$	—	—	−100	—	—	−150	μA
Collector-Emitter Saturation Voltage (2) Common-Emitter (V_E = 0 V, I_C = 200 mA)	$V_{SAT(C)}$	—	1.1	1.3	—	1.1	1.5	V
Emitter-Follower (V_C = 15 V, I_E = −200 mA)	$V_{SAT(E)}$	—	1.5	2.5	—	1.5	2.5	V
Output Control Pin Current Low State ($V_{OC} \leq$ 0.4 V)	I_{OCL}	—	10	—	—	10	—	μA
High State (V_{OC} = V_{ref})	I_{OCH}	—	0.2	3.5	—	0.2	3.5	mA
Output Voltage Rise Time Common-Emitter (See Figure 13)	t_r	—	100	200	—	100	200	ns
Emitter-Follower (See Figure 14)		—	100	200	—	100	200	ns
Output Voltage Fall Time Common-Emitter (See Figure 13)	t_f	—	25	100	—	25	100	ns
Emitter-Follower (See Figure 14)		—	40	100	—	40	100	ns

Characteristic	Symbol	TL494			Unit
		Min	Typ	Max	
ERROR AMPLIFIER SECTIONS					
Input Offset Voltage (V_O (Pin 3) = 2.5 V)	V_{IO}	—	2.0	10	mV
Input Offset Current (V_O (Pin 3) = 2.5 V)	I_{IO}	—	5.0	250	nA
Input Bias Current (V_O (Pin 3) = 2.5 V)	I_{IB}	—	−0.1	−1.0	μA
Input Common-Mode Voltage Range (V_{CC} = 40 V, T_A = 25°C)	V_{ICR}	−0.3 to V_{CC} − 2.0	—	—	V
Open-Loop Voltage Gain (ΔV_O = 3.0 V, V_O = 0.5 to 3.5 V, R_L = 2.0 kΩ)	A_{VOL}	70	95	—	dB
Unity-Gain Crossover Frequency (V_O = 0.5 to 3.5 V, R_L = 2.0 kΩ)	f_C	—	350	—	kHz
Phase Margin at Unity-Gain (V_O = 0.5 to 3.5 V, R_L = 2.0 kΩ)	Øm	—	65	—	deg.
Common-Mode Rejection Ratio (V_{CC} = 40 V)	CMRR	65	90		dB
Power Supply Rejection Ratio (ΔV_{CC} = 33 V, V_O = 2.5 V, R_L = 2.0 kΩ)	PSRR	—	100	—	dB
Output Sink Current (V_O (Pin 3) = 0.7 V)	I_O-	0.3	0.7	—	mA
Output Source Current (V_O (Pin 3) = 3.5 V)	I_O+	−2.0	−4.0	—	mA

NOTE 2: Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperatures as possible.

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, C_T = 0.01 μF, R_T = 12 kΩ unless otherwise noted.)
For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies unless otherwise noted.

Characteristic	Symbol	TL494			Unit
		Min	Typ	Max	
PWM COMPARATOR SECTION (Test Circuit Figure 12)					
Input Threshold Voltage (Zero duty cycle)	V_{TH}	—	3.5	4.5	V
Input Sink Current ($V_{(Pin\ 3)}$ = 0.7 V)	I_I-	0.3	0.7	—	mA
DEAD-TIME CONTROL SECTION (Test Circuit Figure 12)					
Input Bias Current (Pin 4) ($V_{Pin\ 4}$ = 0 to 5.25 V)	I_{IB} (DT)	—	−2.0	−10	μA
Maximum Duty Cycle, Each Output, Push-Pull Mode ($V_{Pin\ 4}$ = 0 V, C_T = 0.01 μF, R_T = 12 kΩ) ($V_{Pin\ 4}$ = 0 V, C_T = 0.001 μF, R_T = 30 kΩ)	DC_{max}	 45 —	 48 45	 50 50	%
Input Threshold Voltage (Pin 4) (Zero Duty Cycle) (Maximum Duty Cycle)	V_{TH}	 — 0	 2.8 —	 3.3 —	V
OSCILLATOR SECTION					
Frequency (C_T = 0.001 μF, R_T = 30 kΩ)	f_{osc}	—	40	—	kHz
Standard Deviation of Frequency* (C_T = 0.001 μF, R_T = 30 kΩ)	σf_{osc}	—	3.0	—	%
Frequency Change with Voltage (V_{CC} = 7.0 V to 40 V, T_A = 25°C)	Δf_{osc} (ΔV)	—	0.1	—	%
Frequency Change with Temperature ($\Delta T_A = T_{low}$ to T_{high}) (C_T = 0.01 μF, R_T = 12 kΩ)	Δf_{osc} (ΔT)	—	—	12	%
UNDERVOLTAGE LOCKOUT SECTION					
Turn-On Threshold (V_{CC} Increasing, I_{ref} = 1.0 mA)	V_{th}	5.5	6.43	7.0	V
TOTAL DEVICE					
Standby Supply Current (Pin 6 at V_{ref}, All Other Inputs and Outputs Open) (V_{CC} = 15 V) (V_{CC} = 40 V)	I_{CC}	 — —	 5.5 7.0	 10 15	mA
Average Supply Current ($V_{(Pin\ 4)}$ = 2.0 V) (See Figure 12) (C_T = 0.01 μF, R_T = 12 kΩ, V_{CC} = 15 V)	—	—	7.0	—	mA

* Standard deviation is a measure of the statistical distribution about the mean as derived from the formula, $\sigma = \sqrt{\frac{\sum_{n=1}^{N} (x_n - \bar{x})^2}{N-1}}$

3

FIGURE 4 — OSCILLATOR FREQUENCY versus TIMING RESISTANCE

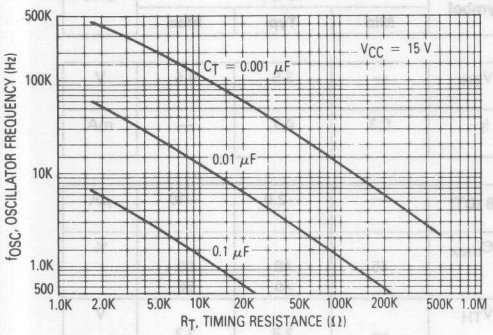


FIGURE 5 — OPEN-LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY

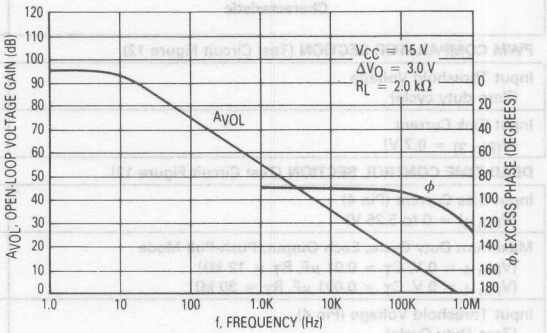


FIGURE 6 — PERCENT DEAD-TIME versus OSCILLATOR FREQUENCY

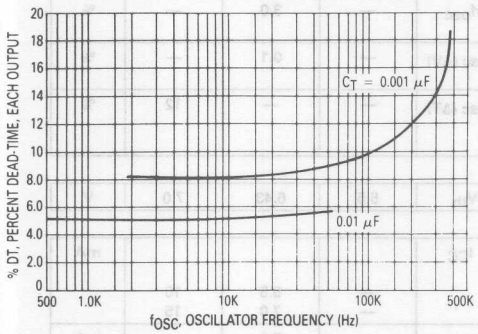


FIGURE 7 — PERCENT DUTY CYCLE versus DEAD-TIME CONTROL VOLTAGE

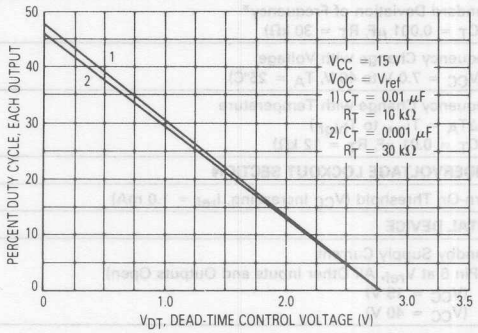


FIGURE 8 — EMITTER FOLLOWER CONFIGURATION OUTPUT SATURATION VOLTAGE versus EMITTER CURRENT

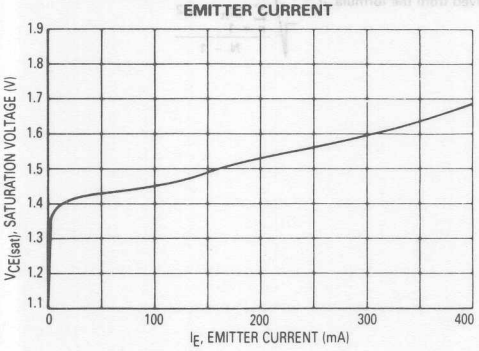


FIGURE 9 — COMMON EMITTER CONFIGURATION OUTPUT SATURATION VOLTAGE versus COLLECTOR CURRENT

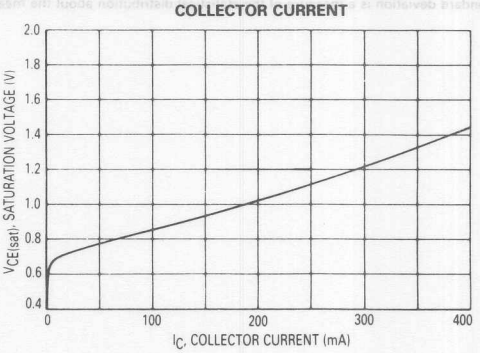


FIGURE 10 — STANDBY SUPPLY CURRENT versus SUPPLY VOLTAGE

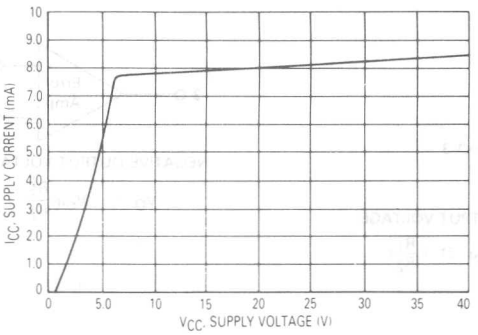


FIGURE 11 — ERROR AMPLIFIER CHARACTERISTICS

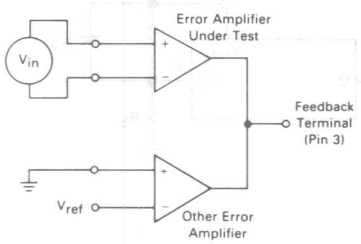


FIGURE 12 — DEAD-TIME AND FEEDBACK CONTROL TEST CIRCUIT

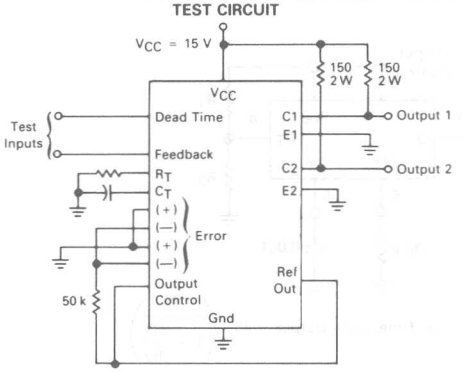


FIGURE 13 — COMMON-EMITTER CONFIGURATION TEST CIRCUIT AND WAVEFORM

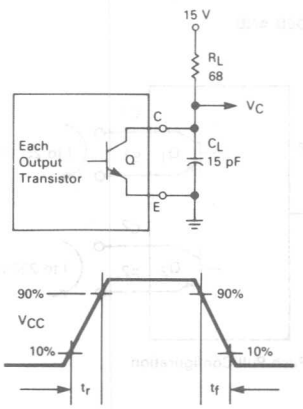


FIGURE 14 — EMITTER-FOLLOWER CONFIGURATION TEST CIRCUIT AND WAVEFORM

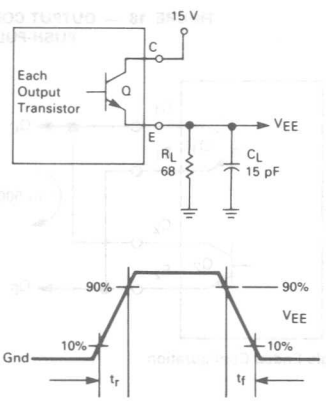


FIGURE 15 — ERROR-AMPLIFIER SENSING TECHNIQUES

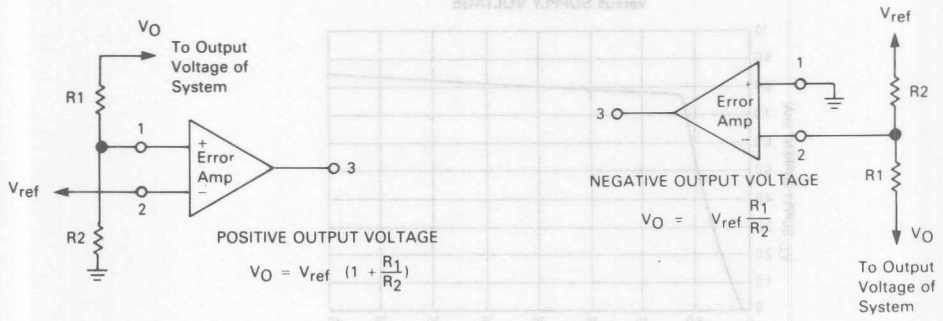


FIGURE 16 — DEAD-TIME CONTROL CIRCUIT

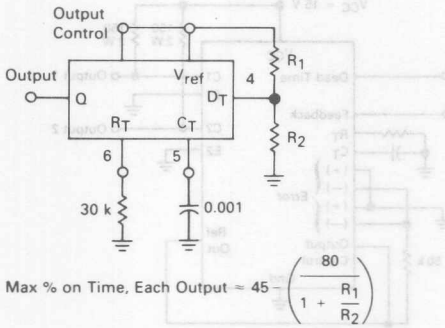


FIGURE 17 — SOFT-START CIRCUIT

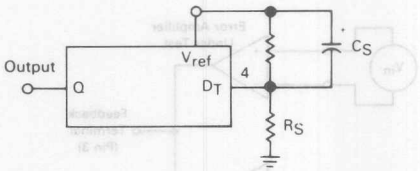


FIGURE 18 — OUTPUT CONNECTIONS FOR SINGLE-ENDED AND PUSH-PULL CONFIGURATIONS

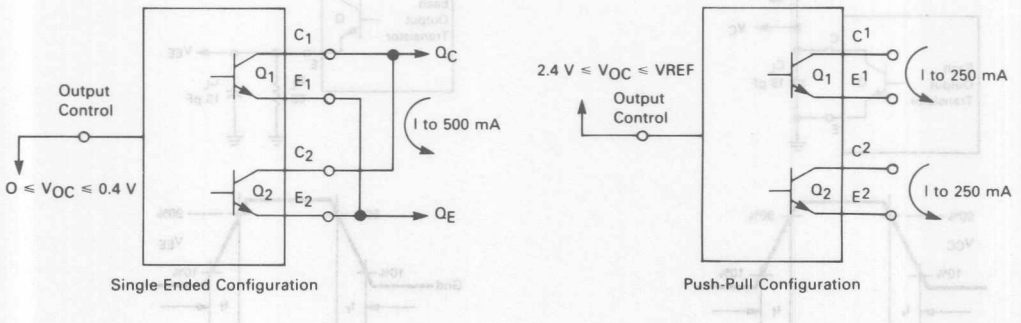


FIGURE 19 — SLAVING TWO OR MORE CONTROL CIRCUITS

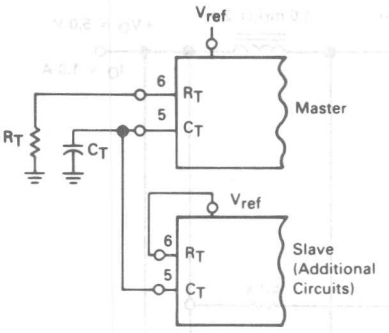


FIGURE 20 — OPERATION WITH V_{IN} > 40 V USING EXTERNAL ZENER

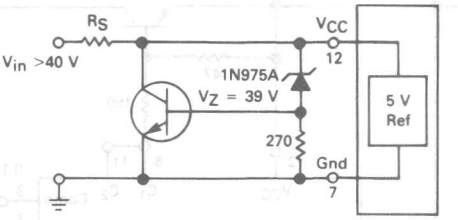
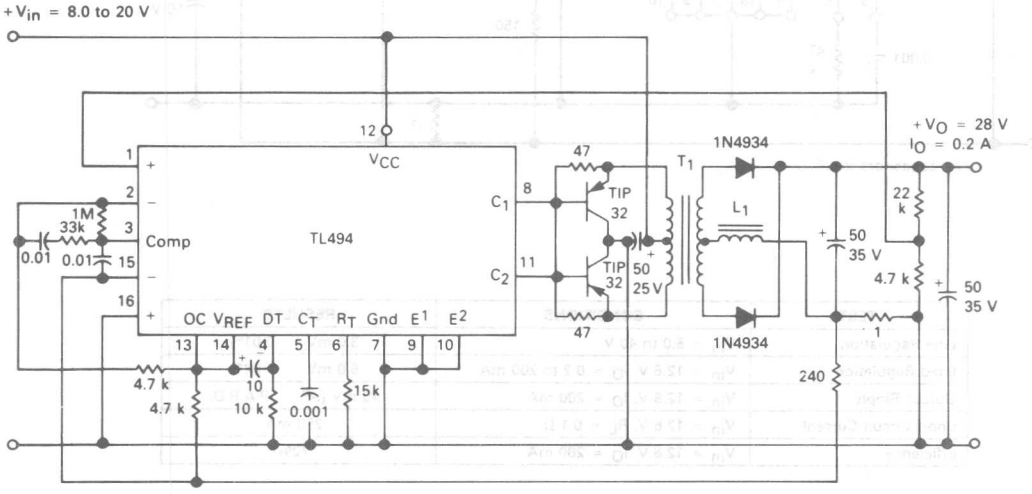


FIGURE 21 — PULSE-WIDTH MODULATED PUSH-PULL CONVERTER

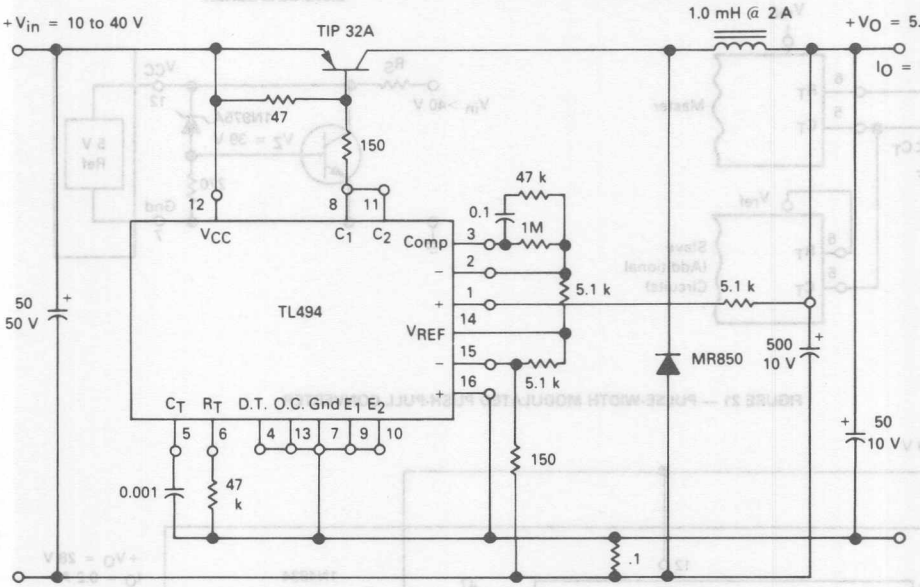


All capacitors in μF

L1 — 3.5 mH @ 0.3 A
T1 — Primary: 20T C.T. #28 AWG
Secondary: 120T C.T. #36 AWG
Core: Ferroxcube 1408P-L00-3C8

TEST	CONDITIONS	RESULTS
Line Regulation	V_{in} = 10 V to 40 V	14 mV 0.28%
Load Regulation	V_{in} = 28 V, I_O = 1 mA to 1 A	3.0 mV 0.06%
Output Ripple	V_{in} = 28 V, I_O = 1.0 A	65 mV P-P P.A.R.D.
Short Circuit Current	V_{in} = 28 V, R_L = 0.1 Ω	1.6 amps
Efficiency	V_{in} = 28 V, I_O = 1 A	71%

FIGURE 22 — PULSE-WIDTH MODULATED STEP-DOWN CONVERTER



TEST	CONDITIONS	RESULTS
Line Regulation	V_{in} = 8.0 to 40 V	3.0 mV 0.01%
Load Regulation	V_{in} = 12.6 V, I_O = 0.2 to 200 mA	5.0 mV 0.02%
Output Ripple	V_{in} = 12.6 V, I_O = 200 mA	40 mV p-P P.A.R.D.
Short Circuit Current	V_{in} = 12.6 V, R_L = 0.1 Ω	250 mA
Efficiency	V_{in} = 12.6 V, I_O = 200 mA	72%

MOTOROLA

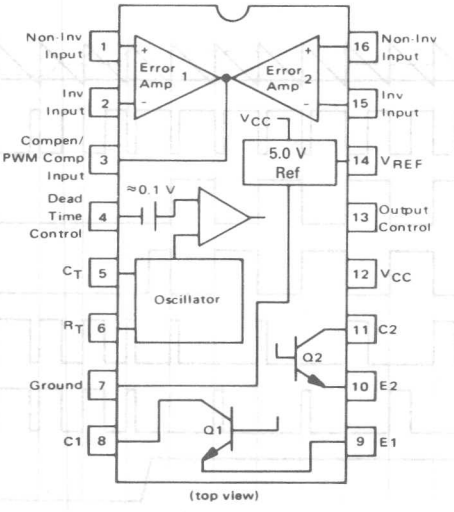
TL594

Advance Information

PRECISION SWITCHMODE PULSE WIDTH MODULATION CONTROL CIRCUIT

The TL594 is a fixed frequency, pulse width modulation control circuit designed primarily for Switchmode power supply control. This device features:

- Complete Pulse Width Modulation Control Circuitry
- On-Chip Oscillator With Master Or Slave Operation
- On-Chip Error Amplifiers
- On-Chip 5 Volt Reference, 1.5% Accuracy
- Adjustable Dead-Time Control
- Uncommitted Output Transistors Rated to 500 mA Source Or Sink
- Output Control For Push-Pull Or Single-Ended Operation
- Undervoltage Lockout

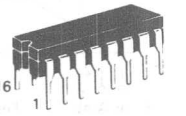


(top view)

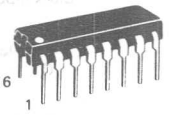
The TL594C is specified over the commercial operating range of 0°C to 70°C. The TL594I is specified over the industrial range of −25°C to 85°C. The TL594M is specified over the full military range of −55°C to 125°C.

PRECISION SWITCHMODE PULSE WIDTH MODULATION CONTROL CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUITS



J SUFFIX
CERAMIC PACKAGE
CASE 620-10



N SUFFIX
PLASTIC PACKAGE
CASE 648-06

ORDERING INFORMATION

Device	Temperature Range	Package
TL594CN	0° to +70°C	Plastic DIP
TL594IN	−25° to +85°C	Plastic DIP
TL594MJ	−55° to +125°C	Ceramic DIP

This document contains information on a new product. Specifications and information herein are subject to change without notice.

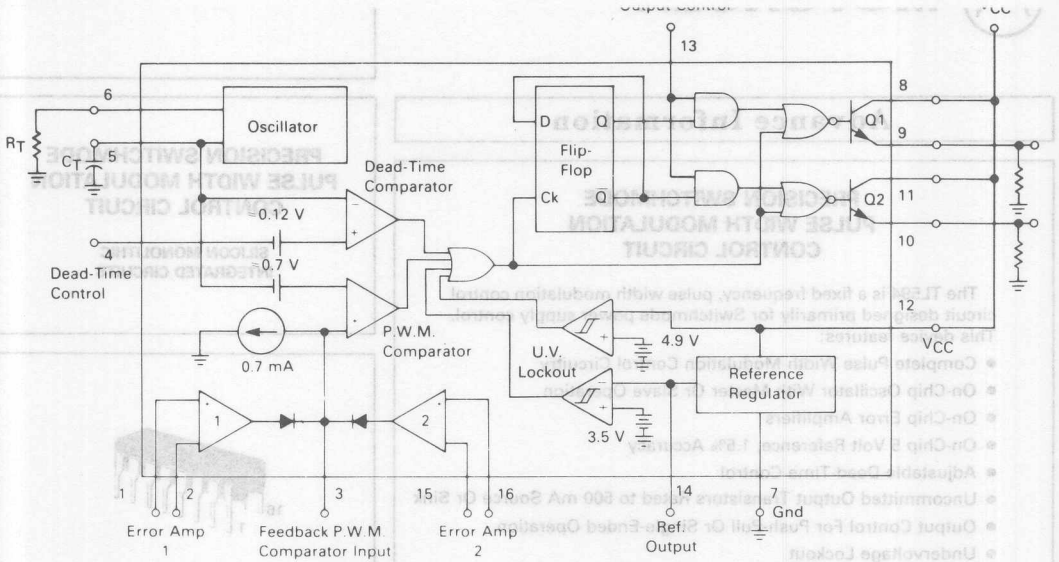
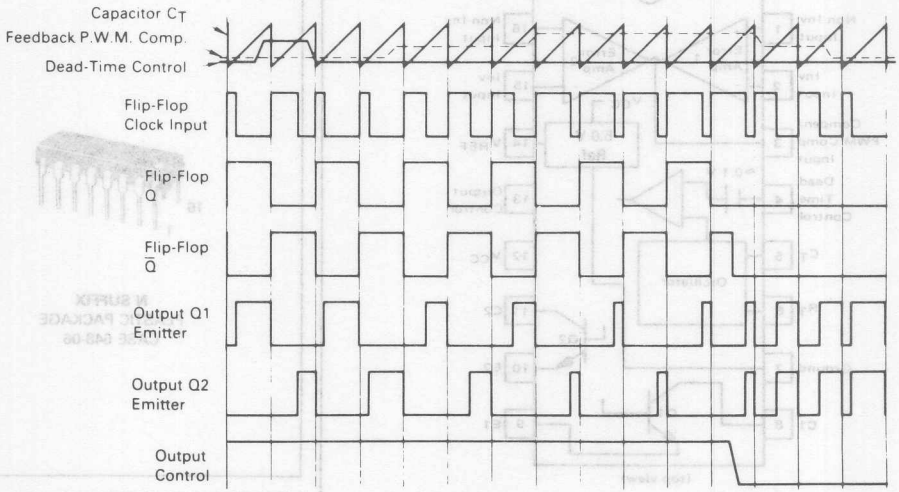


FIGURE 2 — TIMING DIAGRAM



Description

The TL594 is a fixed-frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply. (See Figure 1.) An internal-linear sawtooth oscillator is frequency-programmable by two external components, R_T and C_T. The approximate oscillator frequency is determined by:

$$f_{osc} \approx \frac{1.2}{R_T \bullet C_T}$$

For more information refer to Figure 4.

Output pulse width modulation is accomplished by comparison of the positive sawtooth waveform across capacitor C_T to either of two control signals. The NOR gates, which drive output transistors Q1 and Q2, are enabled only when the flip-flop clock-input line is in its low state. This happens only during that portion of time when the sawtooth voltage is greater than the control signals. Therefore, an increase in control-signal amplitude causes a corresponding linear decrease of output pulse width. (Refer to the timing diagram shown in Figure 2.)

The control signals are external inputs that can be fed into the dead-time control, the error amplifier inputs, or the feedback input. The dead-time control comparator has an effective 120 mV input offset which limits the minimum output dead time to approximately the first 4% of the sawtooth-cycle time. This would result in a maximum duty cycle on a given output of 96% with the output control grounded, and 48% with it connected to the reference line. Additional dead time may be imposed on the output by setting the dead time-control input to a fixed voltage, ranging between 0 to 3.3 V.

The pulse width modulator comparator provides a means for the error amplifiers to adjust the output pulse width from the maximum percent on-time, established by the dead time control input, down to zero, as the voltage at the feedback pin varies from 0.5 to 3.5 V. Both error amplifiers have a common-mode input range from −0.3 V to (V_{CC} − 2 V), and may be used to sense power-supply output voltage and current. The error-amplifier outputs are active high and are ORed together at the non-inverting input of the pulse-width modulator comparator. With this configuration, the amplifier that demands minimum output on time, dominates control of the loop.

When capacitor C_T is discharged, a positive pulse is generated on the output of the dead-time comparator, which clocks the pulse-steering flip-flop and inhibits the output transistors, Q1 and Q2. With the output-control connected to the reference line, the pulse-steering flip-flop directs the modulated pulses to each of the two output transistors alternately for push-pull operation. The output frequency is equal to half that of the oscillator. Output drive can also be taken from Q1 or Q2, when single-ended operation with a maximum on-time of less than 50% is required. This is desirable when the output transformer has a ringback winding with a catch diode used for snubbing. When higher output-drive currents are required for single-ended operation, Q1 and Q2 may be connected in parallel, and the output-mode pin must be tied to ground to disable the flip-flop. The output frequency will now be equal to that of the oscillator.

The TL594 has an internal 5.0 V reference capable of sourcing up to 10 mA of load current for external bias circuits. The reference has an internal accuracy of ±1.5% with a typical thermal drift of less than 50 mV over an operating temperature range of 0 to 70°C.

FIGURE 3 — FUNCTIONAL TABLE

Input Output Control	Output Function	$\frac{f_{out}}{f_{osc}}$ =
Grounded	Single-ended P.W.M. at Q1 and Q2	1
At V_{ref}	Push-pull operation	0.5

MAXIMUM RATINGS (Full operating ambient temperature range applies unless otherwise noted)

Rating	Symbol	TL594C	TL594I	TL594M	Unit
Power Supply Voltage	V_{CC}	42	42	42	V
Collector Output Voltage	V_{C1}, V_{C2}	42	42	42	V
Collector Output Current (each transistor) (Note 1)	I_{C1}, I_{C2}	500	500	500	mA
Amplifier Input Voltage Range	V_{IR}	−0.3 to 42	−0.3 to 42	−0.3 to 42	V
Power Dissipation @ $T_A \leq 45°C$	P_D	1000	1000	1000	mW
Operating Junction Temperature Plastic Package Ceramic Package	T_J	 125 —	 125 —	 — 150	°C
Operating Ambient Temperature Range	T_A	0 to 70	−25 to 85	−55 to 125	°C
Storage Temperature Range Plastic Package Ceramic Package	T_{stg}	 −55 to 125 —	 −55 to 125 —	 — −65 to 150	°C

NOTE 1: Maximum thermal limits must be observed.

THERMAL CHARACTERISTICS

Characteristics	Symbol	N Suffix Plastic Package	J Suffix Ceramic Package	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	80	100	°C/W
Derating Ambient Temperature	T_A	45	50	°C

RECOMMENDED OPERATING CONDITIONS

Condition/Value	Symbol	TL594			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	7.0	15	40	V
Collector Output Voltage	V_{C1}, V_{C2}	—	30	40	V
Collector Output Current (each transistor)	I_{C1}, I_{C2}	—	—	200	mA
Amplifier Input Voltage	V_{in}	0.3	—	V_{CC} − 2.0	V
Current Into Feedback Terminal	I_{fb}	—	—	0.3	mA
Reference Output Current	I_{ref}	—	—	10	mA
Timing Resistor	R_T	1.8	30	500	kΩ
Timing Capacitor	C_T	0.0047	0.001	10	μF
Oscillator Frequency	f_{osc}	1.0	40	200	kHz
PWM Input Voltage (Pins 3, 4 & 13)	—	0.3	—	5.3	V

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, C_T = 0.01 μF, R_T = 12 kΩ unless otherwise noted.)
For typical values T_A = 25°C, for min max values T_A is the operating ambient temperature range that applies unless otherwise noted.

Characteristic	Symbol	TL594C,I			TL594M			Unit
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION								
Reference Voltage (I_O = 1.0 mA, T_A = 25°C) (I_O = 1.0 mA)	V_{ref}	 4.925 4.9	 5.0 —	 5.075 5.1	 4.925 4.9	 5.0 —	 5.075 5.1	V
Line Regulation (V_{CC} = 7.0 V to 40 V)	Reg_{line}	—	2.0	25	—	2.0	25	mV
Load Regulation (I_O = 1.0 mA to 10 mA)	Reg_{load}	—	2.0	15	—	2.0	15	mV
Short-Circuit Output Current (V_{ref} = 0 V)	I_{SC}	15	40	75	15	40	75	mA

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, C_T = 0.01 μF, R_T = 12 kΩ unless otherwise noted.)
For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies unless otherwise noted.

Characteristic	Symbol	TL594C,I			TL594M			Unit
		Min	Typ	Max	Min	Typ	Max	
OUTPUT SECTION								
Collector Off-State Current (V_{CC} = 40 V, V_{CE} = 40 V)	$I_{C(off)}$	—	2.0	100	—	2.0	100	μA
Emitter Off-State Current (V_{CC} = 40 V, V_C = 40 V, V_E = 0 V)	$I_{E(off)}$	—	—	−100	—	—	−100	μA
Collector-Emitter Saturation Voltage (Note 2) Common-Emitter (V_E = 0 V, I_C = 200 mA)	$V_{SAT(C)}$	—	1.1	1.3	—	1.1	1.5	V
Emitter-Follower (V_C = 15 V, I_E = −200 mA)	$V_{SAT(E)}$	—	1.5	2.5	—	1.5	2.5	V
Output Control Pin Current Low State ($V_{OC} \leq$ 0.4 V)	I_{OCL}	—	0.1	—	—	0.1	—	μA
High State (V_{OC} = V_{ref})	I_{OCH}	—	2.0	20	—	2.0	20	μA
Output Voltage Rise Time Common-Emitter (See Figure 13)	t_r	—	100	200	—	100	200	ns
Emitter-Follower (See Figure 14)		—	100	200	—	100	200	ns
Output Voltage Fall Time Common-Emitter (See Figure 13)	t_f	—	40	100	—	40	100	ns
Emitter-Follower (See Figure 14)		—	40	100	—	40	100	ns

Characteristic	Symbol	TL594			Unit
		Min	Typ	Max	
ERROR AMPLIFIER SECTIONS					
Input Offset Voltage ($V_{O\ (Pin\ 3)}$ = 2.5 V)	V_{IO}	—	2.0	10	mV
Input Offset Current ($V_{O\ (Pin\ 3)}$ = 2.5 V)	I_{IO}	—	5.0	250	nA
Input Bias Current ($V_{O\ (Pin\ 3)}$ = 2.5 V)	I_{IB}	—	−0.1	−1.0	μA
Input Common-Mode Voltage Range (V_{CC} = 40 V, T_A = 25°C)	V_{ICR}	0 to V_{CC} − 2.0	—	—	V
Inverting Input Voltage Range	$V_{IR(INV)}$	−0.3 to V_{CC} − 2.0	—	—	V
Open-Loop Voltage Gain (ΔV_O = 3.0 V, V_O = 0.5 to 3.5 V, R_L = 2.0 kΩ)	A_{VOL}	70	95	—	dB
Unity-Gain Crossover Frequency (V_O = 0.5 to 3.5 V, R_L = 2.0 kΩ)	f_C	—	700	—	kHz
Phase Margin at Unity-Gain (V_O = 0.5 to 3.5 V, R_L = 2.0 kΩ)	Øm	—	65	—	deg.
Common-Mode Rejection Ratio (V_{CC} = 40 V)	CMRR	65	90	—	dB
Power Supply Rejection Ratio (ΔV_{CC} = 33 V, V_O = 2.5 V, R_L = 2.0 kΩ)	PSRR	—	100	—	dB
Output Sink Current ($V_{O\ (Pin\ 3)}$ = 0.7 V)	I_O-	0.3	0.7	—	mA
Output Source Current ($V_{O\ (Pin\ 3)}$ = 3.5 V)	I_O+	−2.0	−4.0	—	mA

NOTE 2: Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, C_T = 0.01 μF, R_T = 12 kΩ unless otherwise noted.)
For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies unless otherwise noted.

Characteristic	Symbol	TL594			Unit
		Min	Typ	Max	
PWM COMPARATOR SECTION (Test Circuit Figure 12)					
Input Threshold Voltage (Zero Duty Cycle)	V_{TH}	—	3.6	4.5	V
Input Sink Current ($V_{Pin\ 3}$ = 0.7 V)	I_I –	0.3	0.7	—	mA
DEAD-TIME CONTROL SECTION (Test Circuit Figure 12)					
Input Bias Current (Pin 4) ($V_{Pin\ 4}$ = 0 to 5.25 V)	$I_{IB\ (DT)}$	—	– 2.0	– 10	μA
Maximum Duty Cycle, Each Output, Push-Pull Mode	DC_{max}				%
($V_{Pin\ 4}$ = 0 V, C_T = 0.01 μF, R_T = 12 kΩ)		45	48	50	
($V_{Pin\ 4}$ = 0 V, C_T = 0.001 μF, R_T = 30 kΩ)		—	45	—	
Input Threshold Voltage (Pin 4)	V_{TH}				V
(Zero Duty Cycle)		—	2.8	3.3	
(Maximum Duty Cycle)		0	—	—	
OSCILLATOR SECTION					
Frequency	f_{osc}				kHz
(C_T = 0.001 μF, R_T = 30 kΩ)		—	40	—	
(C_T = 0.01 μF, R_T = 12 kΩ, T_A = 25°C)		9.2	10	10.8	
(C_T = 0.01 μF, R_T = 12 kΩ, T_A = T_{low} to T_{high})		9.0	—	12	
Standard Deviation of Frequency* (C_T = 0.001 μF, R_T = 30 kΩ)	σf_{osc}	—	1.5	—	%
Frequency Change with Voltage (V_{CC} = 7.0 V to 40 V, T_A = 25°C)	$\Delta f_{osc}\ (\Delta V)$	—	0.2	1.0	%
Frequency Change with Temperature (ΔT_A = T_{low} to T_{high}, C_T = 0.01 μF, R_T = 12 kΩ)	$\Delta f_{osc}\ (\Delta T)$	—	4.0	—	%
UNDERVOLTAGE LOCKOUT SECTION					
Turn-On Threshold (V_{CC} Increasing, I_{ref} = 1.0 mA)	V_{th}				V
T_A = 25°C		4.0	5.2	6.0	
T_A = T_{low} to T_{high}		3.5	—	6.5	
Hysteresis	V_H				mV
TL594C,I		100	150	300	
TL594M		50	150	300	
TOTAL DEVICE					
Standard Supply Current (Pin 6 at V_{ref}, All Other Inputs and Outputs Open)	I_{CC}				mA
(V_{CC} = 15 V)		—	8.0	15	
(V_{CC} = 40 V)		—	8.5	18	
Average Supply Current ($V_{Pin\ 4}$ = 2.0 V, C_T = 0.01 μF, R_T = 12 kΩ, V_{CC} = 15 V, See Figure 12)	—	—	11	—	mA

*Standard deviation is a measure of the statistical distribution about the mean as derived from the formula, $\sigma = \sqrt{\frac{\sum_{n=1}^{N} (X_n - \bar{X})^2}{N-1}}$

FIGURE 4 — OSCILLATOR FREQUENCY versus TIMING RESISTANCE

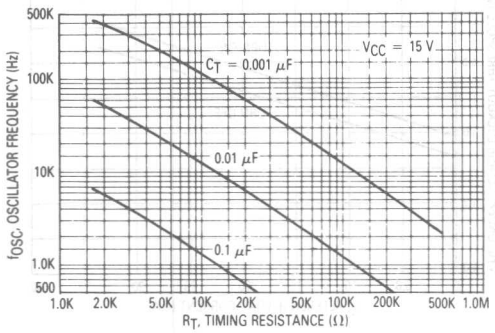


FIGURE 5 — OPEN-LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY

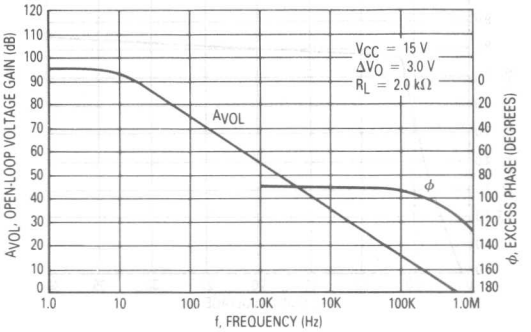


FIGURE 6 — PERCENT DEAD-TIME versus OSCILLATOR FREQUENCY

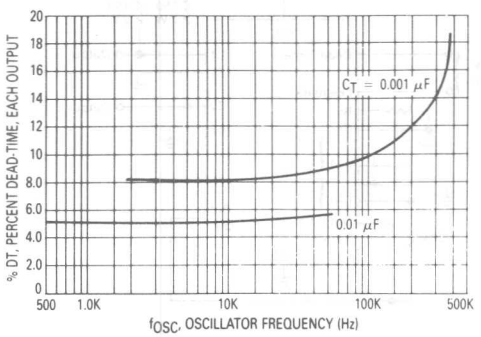


FIGURE 7 — PERCENT DUTY CYCLE versus DEAD-TIME CONTROL VOLTAGE

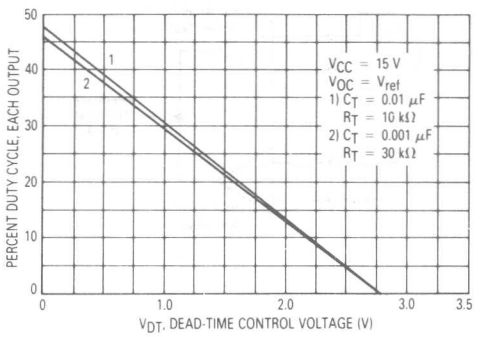


FIGURE 8 — EMITTER FOLLOWER CONFIGURATION OUTPUT SATURATION VOLTAGE versus EMITTER CURRENT

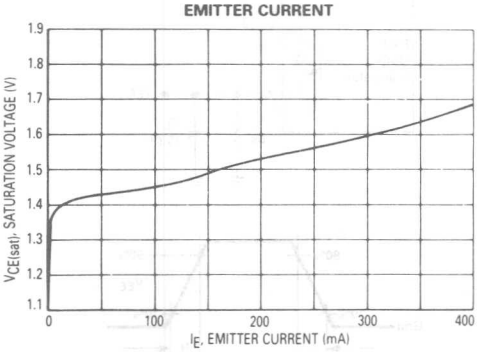
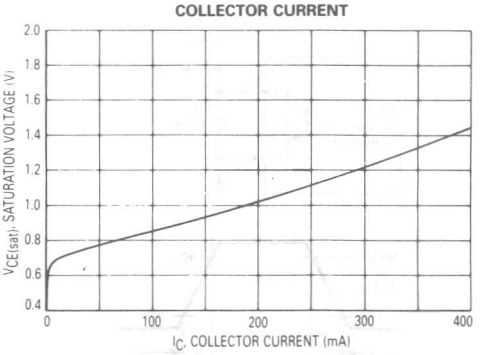


FIGURE 9 — COMMON EMITTER CONFIGURATION OUTPUT SATURATION VOLTAGE versus COLLECTOR CURRENT



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FIGURE 10 — STANDBY SUPPLY CURRENT versus SUPPLY VOLTAGE

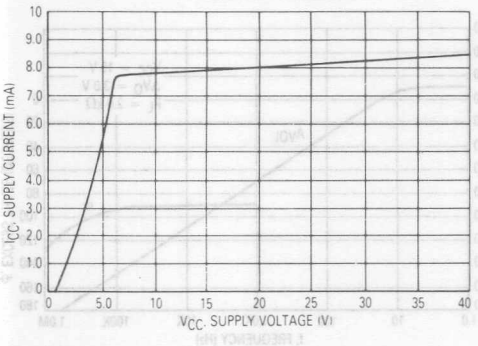


FIGURE 11 — UNDERVOLTAGE LOCKOUT THRESHOLDS versus REFERENCE LOAD CURRENT

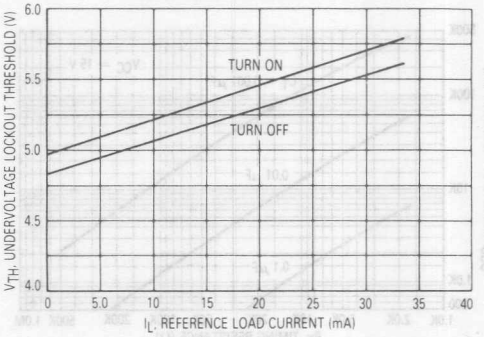


FIGURE 12 — ERROR AMPLIFIER CHARACTERISTICS

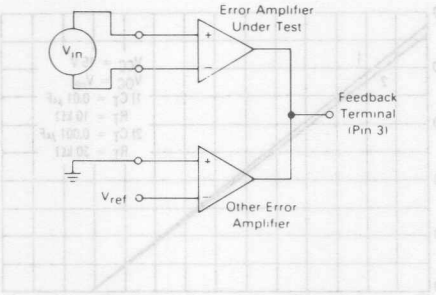


FIGURE 13 — DEAD-TIME AND FEEDBACK CONTROL TEST CIRCUIT

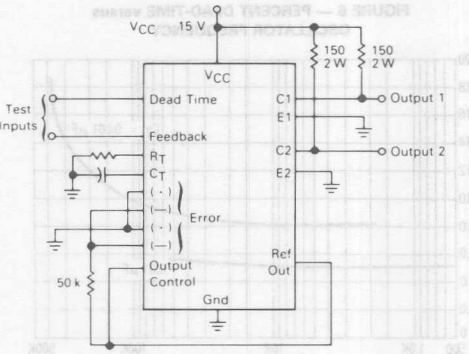


FIGURE 14 — COMMON-EMITTER CONFIGURATION TEST CIRCUIT AND WAVEFORM

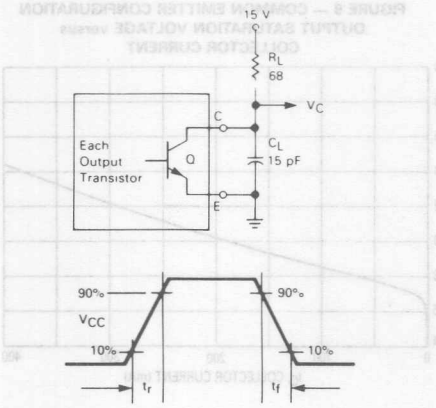


FIGURE 15 — EMITTER-FOLLOWER CONFIGURATION TEST CIRCUIT AND WAVEFORM

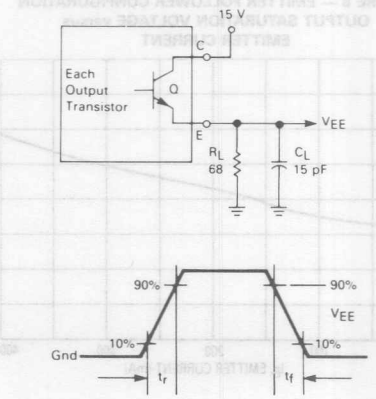


FIGURE 16 — ERROR-AMPLIFIER SENSING TECHNIQUES

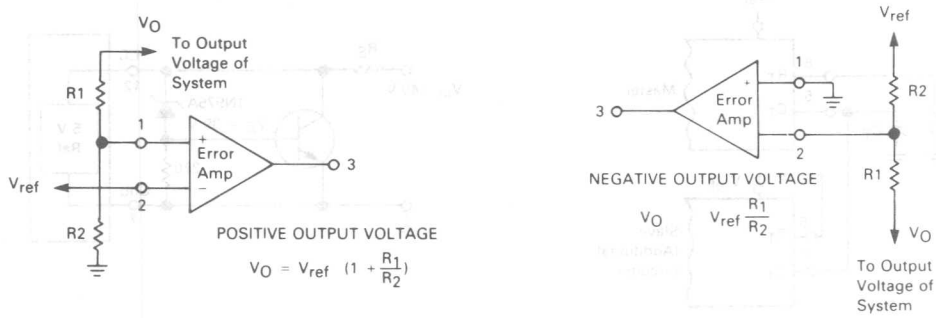


FIGURE 17 — DEAD-TIME CONTROL CIRCUIT

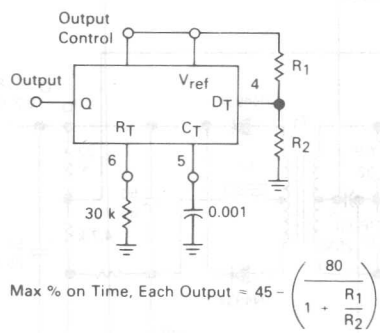


FIGURE 18 — SOFT-START CIRCUIT

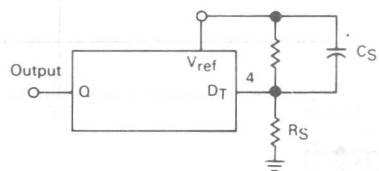


FIGURE 19 — OUTPUT CONNECTIONS FOR SINGLE-ENDED AND PUSH-PULL CONFIGURATIONS

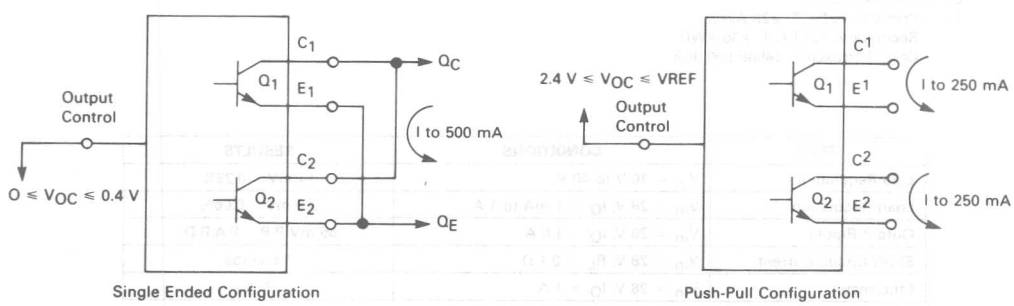


FIGURE 20 — SLAVING TWO OR MORE CONTROL CIRCUITS

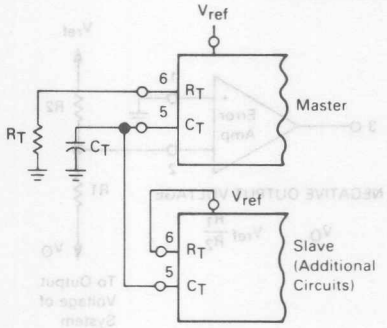


FIGURE 21 — OPERATION WITH V_{IN} > 40 V USING EXTERNAL ZENER

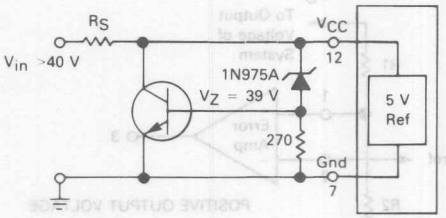
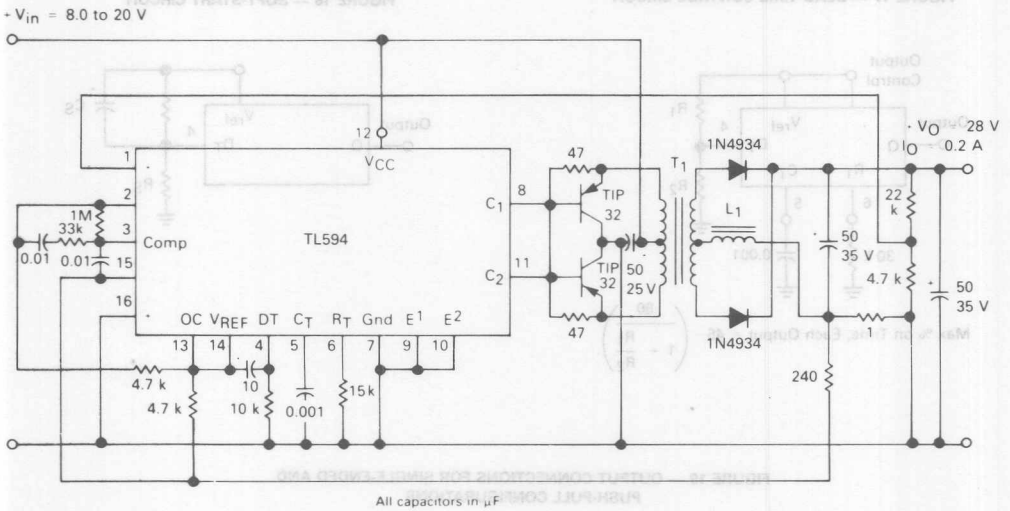


FIGURE 22 — PULSE-WIDTH MODULATED PUSH-PULL CONVERTER

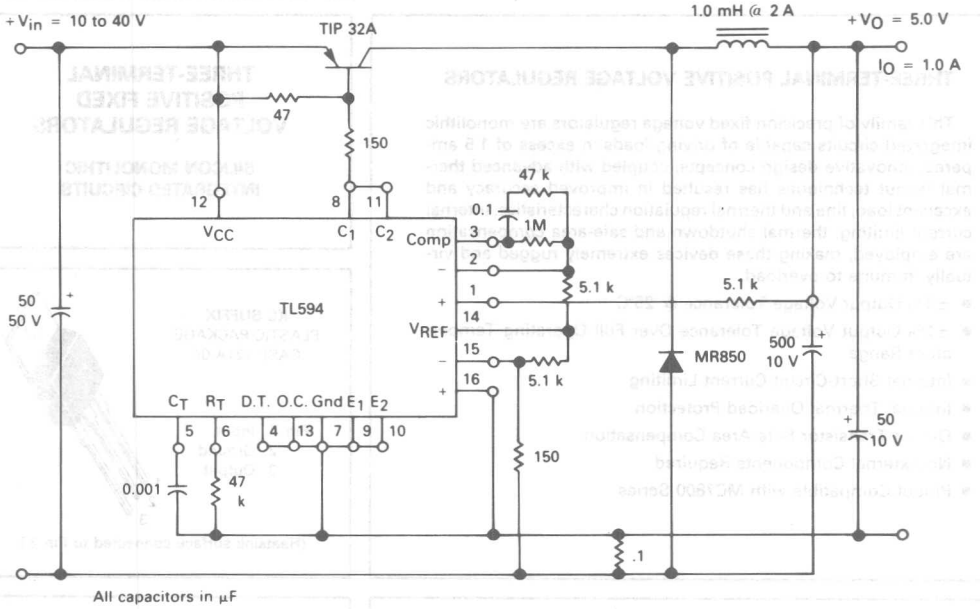


All capacitors in μF

L1 — 3.5 mH @ 0.3 A
T1 — Primary: 20T C.T. #28 AWG
Secondary: 120T C.T. #36 AWG
Core: Ferroxcube 1408P-L00-3C8

TEST	CONDITIONS	RESULTS
Line Regulation	V_{in} = 10 V to 40 V	14 mV 0.28%
Load Regulation	V_{in} = 28 V, I_O = 1 mA to 1 A	3.0 mV 0.06%
Output Ripple	V_{in} = 28 V, I_O = 1.0 A	65 mV P-P P.A.R.D.
Short Circuit Current	V_{in} = 28 V, R_L = 0.1 Ω	1.6 amps
Efficiency	V_{in} = 28 V, I_O = 1 A	71%

FIGURE 23 — PULSE-WIDTH MODULATED STEP-DOWN CONVERTER



TEST	CONDITIONS	RESULTS
Line Regulation	V_{in} = 8.0 to 40 V	3.0 mV 0.01%
Load Regulation	V_{in} = 12.6 V, I_O = 0.2 to 200 mA	5.0 mV 0.02%
Output Ripple	V_{in} = 12.6 V, I_O = 200 mA	40 mV p-P P.A.R.D.
Short Circuit Current	V_{in} = 12.6 V, R_L = 0.1 Ω	250 mA
Efficiency	V_{in} = 12.6 V, I_O = 200 mA	72%

MOTOROLA

TL780 Series

3

THREE-TERMINAL POSITIVE VOLTAGE REGULATORS

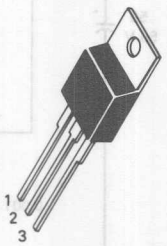
This family of precision fixed voltage regulators are monolithic integrated circuits capable of driving loads in excess of 1.5 amperes. Innovative design concepts, coupled with advanced thermal layout techniques has resulted in improved accuracy and excellent load, line and thermal regulation characteristics. Internal current limiting, thermal shutdown and safe-area compensation are employed, making these devices extremely rugged and virtually immune to overload.

- ±1% Output Voltage Tolerance @ 25°C
- ±2% Output Voltage Tolerance Over Full Operating Temperature Range
- Internal Short-Circuit Current Limiting
- Internal Thermal Overload Protection
- Output Transistor Safe-Area Compensation
- No External Components Required
- Pinout Compatible with MC7800 Series

THREE-TERMINAL POSITIVE FIXED VOLTAGE REGULATORS

SILICON MONOLITHIC INTEGRATED CIRCUITS

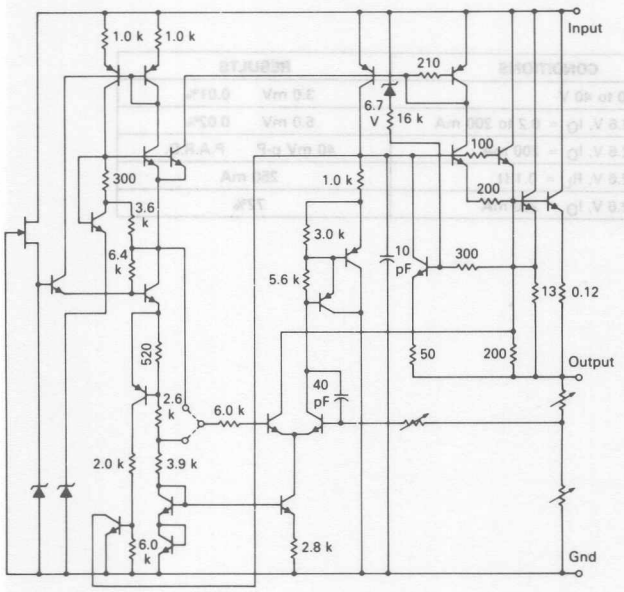
KC SUFFIX
PLASTIC PACKAGE
CASE 221A-04



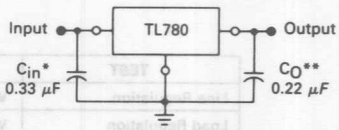
Pin 1. Input
2. Ground
3. Output

(Heatsink surface connected to Pin 2.)

EQUIVALENT SCHEMATIC DIAGRAM



STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O is not needed for stability; however, it does improve transient response.

ORDERING INFORMATION

Nominal Output Voltage	Device
5.0 V	TL780-05CKC
12 V	TL780-12CKC
15 V	TL780-15CKC

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	V_{in}	35	Vdc
Power Dissipation and Thermal Characteristics			
T_A = +25°C	P_D	2.0	Watts
Derate above T_A = +25°C	$1/\theta_{JA}$	16	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	62.5	°C/W
T_C = +25°C	P_D	15	Watts
Derate above T_C = +75°C (See Figure 1)	$1/\theta_{JC}$	200	mW/°C
Thermal Resistance, Junction to Case	θ_{JC}	5.0	°C/W
Operating Junction Temperature Range	T_J	0 to +150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

TL780-05C

ELECTRICAL CHARACTERISTICS (V_{in} = 10 V, I_O = 500 mA, 0°C ≤ T_J ≤ +125°C unless otherwise noted [Note 1])

Characteristic	Symbol	TL780-05C Min	TL780-05C Typ	TL780-05C Max	Unit
Output Voltage 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W 7.0 V ≤ V_{in} ≤ 20 V	V_O				V
T_J = +25°C		4.95	5.0	5.05	
0°C ≤ T_J ≤ +125°C		4.90	—	5.10	
Line Regulation (T_J = +25°C)	Reg_{line}				mV
7.0 V ≤ V_{in} ≤ 25 V		—	0.5	5.0	
8.0 V ≤ V_{in} ≤ 12 V		—	0.5	5.0	
Load Regulation (T_J = +25°C)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.5 A		—	4.0	25	
250 mA ≤ I_O ≤ 750 mA		—	1.5	15	
Ripple Rejection 8.0 V ≤ V_{in} ≤ 18 V, f = 120 Hz	RR	70	80	—	dB
Output Resistance (f = 1.0 kHz)	r_O	—	0.0035	—	Ω
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	—	0.06	—	mV/°C
Output Noise Voltage (T_J = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	75	—	μV
Dropout Voltage (T_J = +25°C) I_O = 1.0 A	V_{in}-V_O	—	2.0	—	V
Bias Current (T_J = +25°C)	I_B	—	3.5	8.0	mA
Bias Current Change	ΔI_B				mA
7.0 V ≤ V_{in} ≤ 25 V, I_O = 500 mA		—	0.7	1.3	
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 10 V		—	0.03	0.5	
Short-Circuit Output Current (T_J = +25°C) V_{in} = 35 V	I_{sc}	—	200	—	mA
Peak Output Current (T_J = +25°C)	I_P	—	2.2	—	A

Note 1: Line and load regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

TL780-12C

ELECTRICAL CHARACTERISTICS (V_{in} = 19 V, I_O = 500 mA, 0°C ≤ T_J ≤ +125°C unless otherwise noted [Note 1])

Characteristic	Symbol	TL780-12C Min	TL780-12C Typ	TL780-12C Max	Unit
Output Voltage 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W 14.5 V ≤ V_{in} ≤ 27 V	V_O				V
T_J = +25°C		11.88	12	12.12	
0°C ≤ T_J ≤ +125°C		11.76	—	12.24	
Line Regulation (T_J = +25°C)	Reg_{line}				mV
14.5 V ≤ V_{in} ≤ 30		—	1.2	12	
16 V ≤ V_{in} ≤ 22		—	1.2	12	

TL780-12C (continued)

ELECTRICAL CHARACTERISTICS (V_{in} = 19 V, I_O = 500 mA, 0°C ≤ T_J ≤ +125°C unless otherwise noted [Note 1])

Characteristic	Symbol	TL780-12C Min	TL780-12C Typ	TL780-12C Max	Unit
Load Regulation (T_J = +25°C) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 — —	 6.5 2.5	 60 36	mV
Ripple Rejection 15 V ≤ V_{in} ≤ 25 V, f = 120 Hz	RR	65	77	—	dB
Output Resistance (f = 1.0 kHz)	r_O	—	0.0035	—	Ω
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	—	0.15	—	mV/°C
Output Noise Voltage (T_J = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	180	—	μV
Dropout Voltage (T_J = +25°C) I_O = 1.0 A	V_{in}-V_O	—	2.0	—	V
Bias Current (T_J = +25°C)	I_B	—	3.5	8.0	mA
Bias Current Change 14.5 V ≤ V_{in} ≤ 30 V, I_O = 500 mA 5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 19 V	ΔI_B	 — —	 0.4 0.03	 1.3 0.5	mA
Short-Circuit Output Current (T_J = +25°C) V_{in} = 35 V	I_{sc}	—	200	—	mA
Peak Output Current (T_J = +25°C)	I_P	—	2.2	—	A

Note 1: Line and load regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

TL780-15C

ELECTRICAL CHARACTERISTICS (V_{in} = 23 V, I_O = 500 mA, 0°C ≤ T_J ≤ +125°C unless otherwise noted [Note 1])

Characteristic	Symbol	TL780-15C Min	TL780-15C Typ	TL780-15C Max	Unit
Output Voltage 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W 17.5 V ≤ V_{in} ≤ 30 V T_J = +25°C 0°C ≤ T_J ≤ +125°C	V_O	 14.85 14.70	 15 —	 15.15 15.30	V
Line Regulation (T_J = +25°C) 17.5 V ≤ V_{in} ≤ 30 V 20 V ≤ V_{in} ≤ 26 V	Reg_{line}	 — —	 1.5 1.5	 15 15	mV
Load Regulation (T_J = +25°C) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 — —	 7.0 2.5	 75 45	mV
Ripple Rejection 18.5 V ≤ V_{in} ≤ 28.5 V, f = 120 Hz	RR	60	75	—	dB
Output Resistance (f = 1.0 kHz)	r_O	—	0.0035	—	Ω
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	—	0.18	—	mV/°C
Output Noise Voltage (T_J = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	225	—	μV
Dropout Voltage (T_J = +25°C) I_O = 1.0 A	V_{in}-V_O	—	2.0	—	V
Bias Current (T_J = +25°C)	I_B	—	3.6	8.0	mA
Bias Current Change 17.5 V ≤ V_{in} ≤ 30 V, I_O = 500 mA 5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 23 V	ΔI_B	 — —	 0.4 0.02	 1.3 0.5	mA
Short-Circuit Output Current (T_J = +25°C) V_{in} = 35 V	I_{sc}	—	200	—	mA
Peak Output Current (T_J = +25°C)	I_P	—	2.2	—	A

Note 1: Line and load regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

TYPICAL PERFORMANCE CHARACTERISTICS

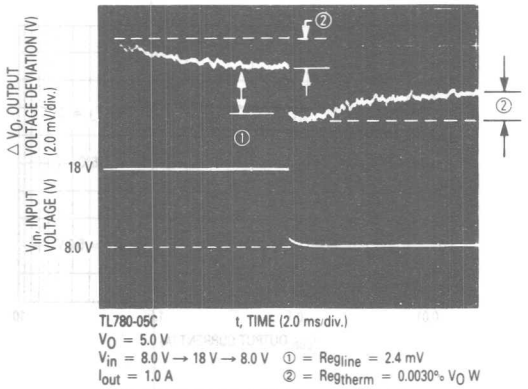
VOLTAGE REGULATOR PERFORMANCE

The performance of a voltage regulator is specified by its immunity to changes in load, input voltage, power dissipation, and temperature. Line and load regulation are tested with a pulse of short duration (< 100 μs) and are strictly a function of electrical gain. However, pulse widths of longer duration (> 1.0 ms) are sufficient to affect temperature gradients across the die. These temperature gradients can cause a change in the output voltage, in addition to changes caused by line and load regulation. Longer pulse widths and thermal gradients make it desirable to specify thermal regulation.

Thermal regulation is defined as the change in output voltage caused by a change in dissipated power for a specified time, and is expressed as a percentage output voltage change per watt. The change in dissipated power can be caused by a change in either the input voltage or the load current. Thermal regulation is a function of I.C. layout and die attach techniques, and usually occurs within 10 ms of a change in power dissipation. After 10 ms, additional changes in the output voltage are due to the temperature coefficient of the device.

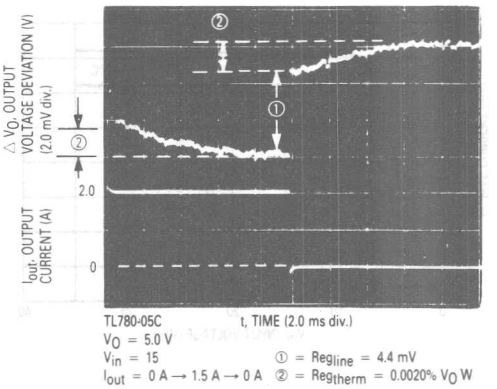
Figure 1 shows the line and thermal regulation response of a typical TL780-05C to a 10 watt input pulse. The variation of the output voltage due to line regulation is labeled ① and the thermal regulation component is labeled ②. Figure 2 shows the load and thermal regulation response of a typical TL780-05C to a 15 watt load pulse. The output voltage variation due to load regulation is labeled ① and the thermal regulation component is labeled ②.

FIGURE 1 — LINE AND THERMAL REGULATION



TL780-05C t, TIME (2.0 ms/div.)
V_O = 5.0 V
V_{in} = 8.0 V → 18 V → 8.0 V ① = Reg_{line} = 2.4 mV
I_{out} = 1.0 A ② = Reg_{therm} = 0.0030%/W V_O

FIGURE 2 — LOAD AND THERMAL REGULATION



TL780-05C t, TIME (2.0 ms div.)
V_O = 5.0 V
V_{in} = 15 ① = Reg_{line} = 4.4 mV
I_{out} = 0 A → 1.5 A → 0 A ② = Reg_{therm} = 0.0020%/W V_O

FIGURE 3 — TEMPERATURE STABILITY

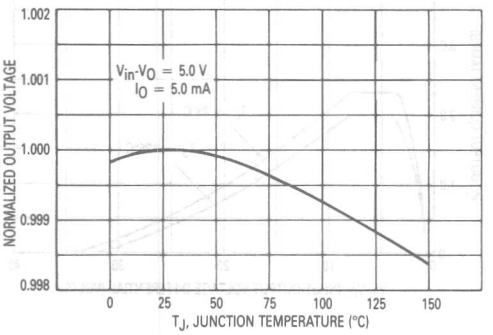
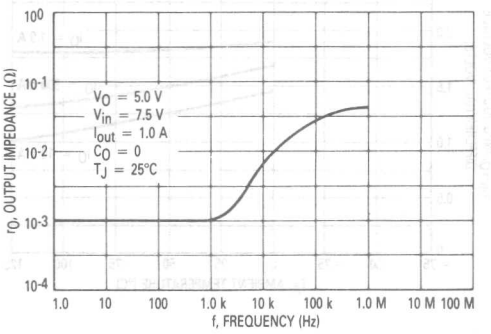


FIGURE 4 — OUTPUT IMPEDANCE



3

FIGURE 5 — RIPPLE REJECTION versus FREQUENCY

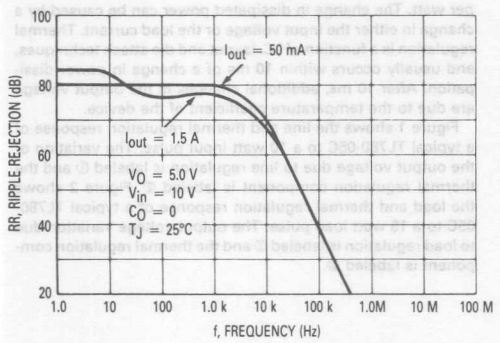


FIGURE 6 — RIPPLE REJECTION versus OUTPUT CURRENT

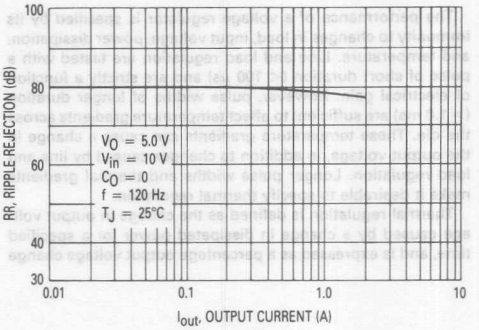


FIGURE 7 — BIAS CURRENT versus INPUT VOLTAGE

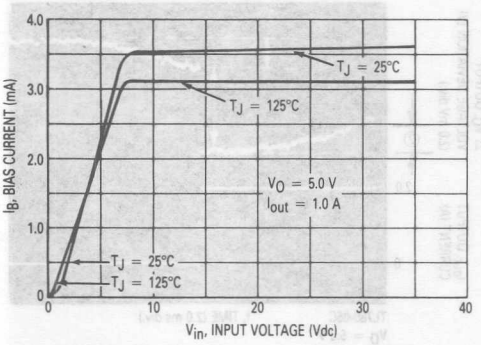


FIGURE 8 — BIAS CURRENT versus OUTPUT CURRENT

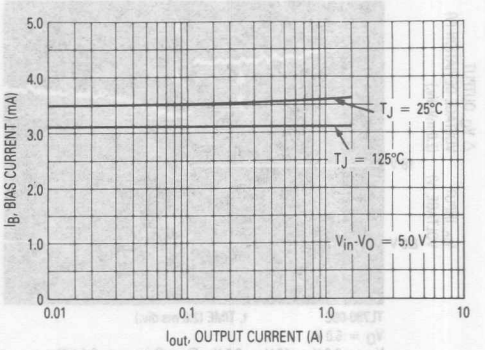


FIGURE 9 — DROPOUT VOLTAGE

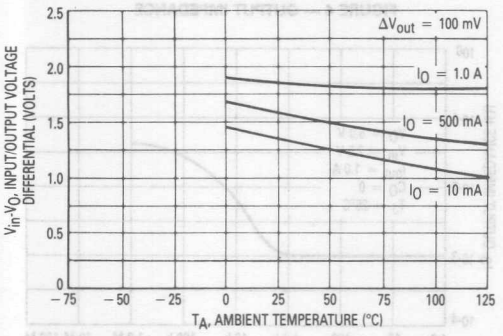


FIGURE 10 — PEAK OUTPUT CURRENT

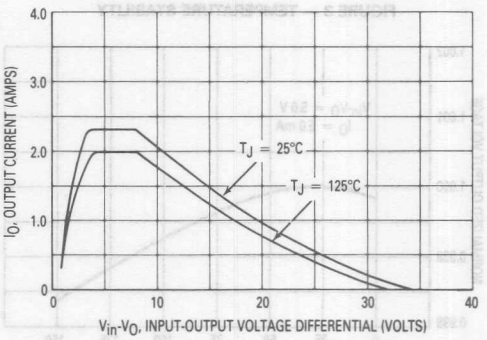


FIGURE 11 — LINE TRANSIENT RESPONSE

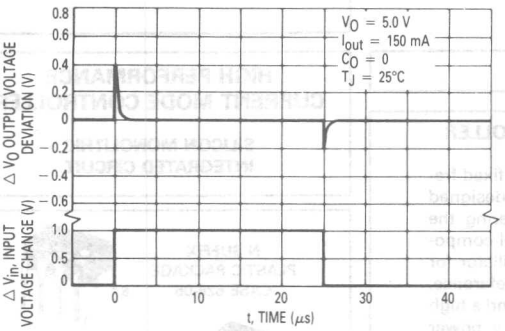


FIGURE 12 — LOAD TRANSIENT RESPONSE

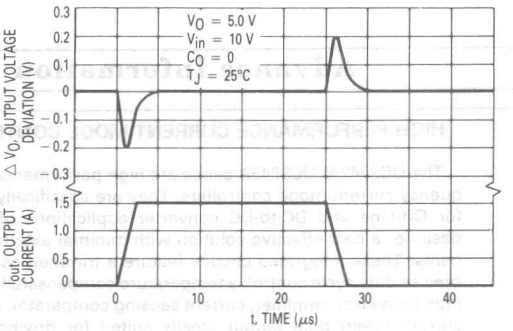
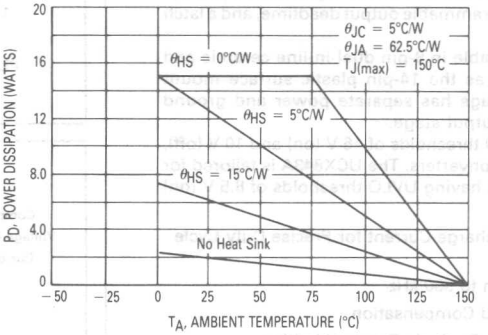


FIGURE 13 — WORST CASE POWER DISSIPATION versus AMBIENT TEMPERATURE



Advance Information

HIGH PERFORMANCE CURRENT MODE CONTROLLER

The UC3842A, UC3843A series are high performance fixed frequency current mode controllers. They are specifically designed for Off-Line and DC-to-DC converter applications offering the designer a cost effective solution with minimal external components. These integrated circuits feature a trimmed oscillator for precise duty cycle control, a temperature compensated reference, high gain error amplifier, current sensing comparator, and a high current totem pole output ideally suited for driving a power MOSFET.

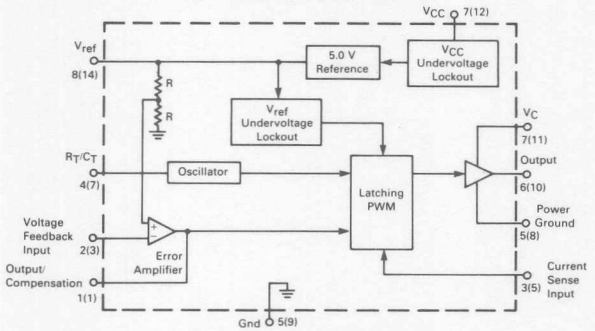
Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle-by-cycle current limiting, programmable output deadtime, and a latch for single pulse metering.

These devices are available in 8-pin dual-in-line ceramic and plastic packages as well as the 14-pin plastic surface mount (SO-14). The SO-14 package has separate power and ground pins for the totem pole output stage.

The UCX842A has UVLO thresholds of 16 V (on) and 10 V (off), ideally suited for off-line converters. The UCX843A is tailored for lower voltage applications having UVLO thresholds of 8.5 V (on) and 7.6 V (off).

- Trimmed Oscillator Discharge Current for Precise Duty Cycle Control
- Current Mode Operation to 500 kHz
- Automatic Feed Forward Compensation
- Latching PWM for Cycle-By-Cycle Current Limiting
- Internally Trimmed Reference with Undervoltage Lockout
- High Current Totem Pole Output
- Undervoltage Lockout with Hysteresis
- Low Start-Up and Operating Current
- Direct Interface with Motorola SENSEFET Products

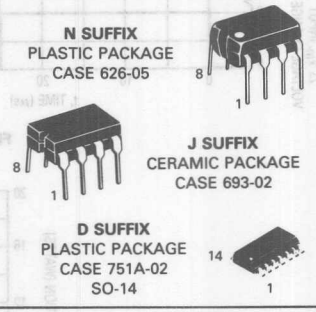
SIMPLIFIED BLOCK DIAGRAM



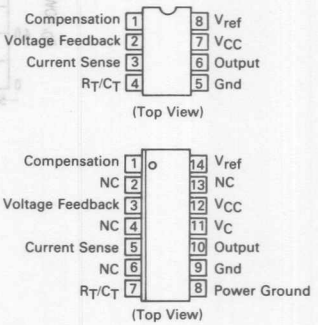
Pin numbers adjacent to terminals are for the 8-pin dual-in-line package.
Pin numbers in parenthesis are for the D suffix SO-14 package.

HIGH PERFORMANCE CURRENT MODE CONTROLLER

SILICON MONOLITHIC INTEGRATED CIRCUIT



PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
UC3842AD	0 to +70°C	SO-14 Plastic DIP
UC3843AD		SO-14 Plastic DIP
UC3842AN		Plastic DIP
UC3843AN		Plastic DIP
UC2842AD	−25 to +85°C	SO-14 Plastic DIP
UC2843AD		SO-14 Plastic DIP
UC2842AJ		Ceramic DIP
UC2843AJ		Ceramic DIP
UC2842AN		Plastic DIP
UC2843AN		Plastic DIP

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATING

Rating	Symbol	Value	Unit
Total Power Supply and Zener Current	$(I_{CC}+I_Z)$	30	mA
Output Current, Source or Sink (Note 1)	I_O	1.0	A
Output Energy (Capacitive Load per Cycle)	W	5.0	μJ
Current Sense and Voltage Feedback Inputs	V_{in}	−0.3 to +5.5	V
Error Amp Output Sink Current	I_O	10	mA
Power Dissipation and Thermal Characteristics			
D Suffix, Plastic Package			
Maximum Power Dissipation @ T_A = 25°C	P_D	862	mW
Thermal Resistance Junction to Air	$R_{\theta JA}$	145	°C/W
N Suffix, Plastic Package and			
J Suffix, Ceramic Package			
Maximum Power Dissipation @ T_A = 25°C	P_D	1.25	W
Thermal Resistance Junction to Air	$R_{\theta JA}$	100	°C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_A		°C
UC3842A, UC3843A		0 to +70	
UC2842A, UC2843A		−25 to +85	
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 2], R_T = 10 k, C_T = 3.3 nF, T_A = T_{low} to T_{high} [Note 3] unless otherwise noted)

Characteristic	Symbol	UC284XA			UC384XA			Unit
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION								
Reference Output Voltage (I_O = 1.0 mA, T_J = 25°C)	V_{ref}	4.95	5.0	5.05	4.9	5.0	5.1	V
Line Regulation (V_{CC} = 12 V to 25 V)	Reg_{line}	—	2.0	20	—	2.0	20	mV
Load Regulation (I_O = 1.0 mA to 20 mA)	Reg_{load}	—	3.0	25	—	3.0	25	mV
Temperature Stability	T_S	—	0.2	—	—	0.2	—	mV/°C
Total Output Variation over Line, Load, and Temperature	V_{ref}	4.9	—	5.1	4.82	—	5.18	V
Output Noise Voltage (f = 10 Hz to 10 kHz, T_J = 25°C)	V_n	—	50	—	—	50	—	μV
Long Term Stability (T_A = 125°C for 1000 Hours)	S	—	5.0	—	—	5.0	—	mV
Output Short Circuit Current	I_{SC}	−30	−85	−180	−30	−85	−180	mA
OSCILLATOR SECTION								
Frequency	f_{OSC}							kHz
T_J = 25°C		47	52	57	47	52	57	
T_A = T_{low} to T_{high}		46	—	60	46	—	60	
Frequency Change with Voltage (V_{CC} = 12 V to 25 V)	$\Delta f_{OSC}/\Delta V$	—	0.2	1.0	—	0.2	1.0	%
Frequency Change with Temperature T_A = T_{low} to T_{high}	$\Delta f_{OSC}/\Delta T$	—	5.0	—	—	5.0	—	%
Oscillator Voltage Swing (Peak-to-Peak)	V_{OSC}	—	1.6	—	—	1.6	—	V
Discharge Current (V_{OSC} = 2.0 V)	I_{dischg}							mA
T_J = 25°C		7.5	8.4	9.3	7.5	8.4	9.3	
T_A = T_{low} to T_{high}		7.2	—	9.5	7.2	—	9.5	

Notes: 1. Maximum Package power dissipation limits must be observed.
2. Adjust V_{CC} above the Start-Up threshold before setting to 15 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
T_{low} = 0°C for UC3842A, UC3843A; −25°C for UC2842A, UC2843A
T_{high} = +70°C for UC3842A, UC3843A; +85°C for UC2842A, UC2843A
4. This parameter is measured at the latch trip point with V_{FB} = 0 V.
5. Comparator gain is defined as: $A_V = \frac{\Delta V \text{ Output/Compensation}}{\Delta V \text{ Current Sense Input}}$

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 2], R_T = 10 k, C_T = 3.3 nF, T_A = T_{low} to T_{high} [Note 3] unless otherwise noted)

Characteristic	Symbol	UC284XA Min	UC284XA Typ	UC284XA Max	UC384XA Min	UC384XA Typ	UC384XA Max	Unit
ERROR AMPLIFIER SECTION								
Voltage Feedback Input (V_O = 2.5 V)	V_{FB}	2.45	2.5	2.55	2.42	2.5	2.58	V
Input Bias Current (V_{FB} = 5.0 V)	I_{IB}	—	−0.1	−1.0	—	−0.1	−2.0	μA
Open-Loop Voltage Gain (V_O = 2.0 V to 4.0 V)	A_{VOL}	65	90	—	65	90	—	dB
Unity Gain Bandwidth (T_J = 25°C)	BW	0.7	1.0	—	0.7	1.0	—	MHz
Power Supply Rejection Ratio (V_{CC} = 12 V to 25 V)	PSRR	60	70	—	60	70	—	dB
Output Current								mA
Sink (V_O = 1.1 V, V_{FB} = 2.7 V)	I_{Sink}	2.0	12	—	2.0	12	—	
Source (V_O = 5.0 V, V_{FB} = 2.3 V)	I_{Source}	−0.5	−1.0	—	−0.5	−1.0	—	
Output Voltage Swing								V
High State (R_L = 15 k to ground, V_{FB} = 2.3 V)	V_{OH}	5.0	6.2	—	5.0	6.2	—	
Low State (R_L = 15 k to V_{ref}, V_{FB} = 2.7 V)	V_{OL}	—	0.8	1.1	—	0.8	1.1	
CURRENT SENSE SECTION								
Current Sense Input Voltage Gain (Notes 4 & 5)	A_V	2.85	3.0	3.15	2.85	3.0	3.15	V/V
Maximum Current Sense Input Threshold (Note 4)	V_{th}	0.9	1.0	1.1	0.9	1.0	1.1	V
Power Supply Rejection Ratio V_{CC} = 12 V to 25 V, Note 4	PSRR	—	70	—	—	70	—	dB
Input Bias Current	I_{IB}	—	−2.0	−10	—	−2.0	−10	μA
Propagation Delay (Current Sense Input to Output)	$t_{PLH(IN/OUT)}$	—	150	300	—	150	300	ns
OUTPUT SECTION								
Output Voltage								V
Low State (I_{Sink} = 20 mA)	V_{OL}	—	0.1	0.4	—	0.1	0.4	
(I_{Sink} = 200 mA)		—	1.6	2.2	—	1.6	2.2	
High State (I_{Source} = 20 mA)	V_{OH}	13	13.5	—	13	13.5	—	
(I_{Source} = 200 mA)		12	13.4	—	12	13.4	—	
Output Voltage with UVLO Activated V_{CC} = 6.0 V, I_{Sink} = 1.0 mA	$V_{OL(UVLO)}$	—	0.1	1.1	—	0.1	1.1	V
Output Voltage Rise Time (C_L = 1.0 nF, T_J = 25°C)	t_r	—	50	150	—	50	150	ns
Output Voltage Fall Time (C_L = 1.0 nF, T_J = 25°C)	t_f	—	50	150	—	50	150	ns
UNDERVOLTAGE LOCKOUT SECTION								
Start-Up Threshold	V_{th}							V
UCX842A		15	16	17	14.5	16	17.5	
UCX843A		7.8	8.4	9.0	7.8	8.4	9.0	
Minimum Operating Voltage After Turn-On	$V_{CC(min)}$							V
UCX842A		9.0	10	11	8.5	10	11.5	
UCX843A		7.0	7.6	8.2	7.0	7.6	8.2	
PWM SECTION								
Duty Cycle								%
Maximum	DC_{max}	94	96	—	94	96	—	
Minimum	DC_{min}	—	—	0	—	—	0	
TOTAL DEVICE								
Power Supply Current	I_{CC}							mA
Start-Up (V_{CC} = 6.5 V for UCX843A, 14 V for UCX842A)		—	0.5	1.0	—	0.5	1.0	
Operating (Note 2)		—	12	17	—	12	17	
Power Supply Zener Voltage (I_{CC} = 25 mA)	V_Z	30	36	—	30	36	—	V

FIGURE 1 — TIMING RESISTOR versus OSCILLATOR FREQUENCY

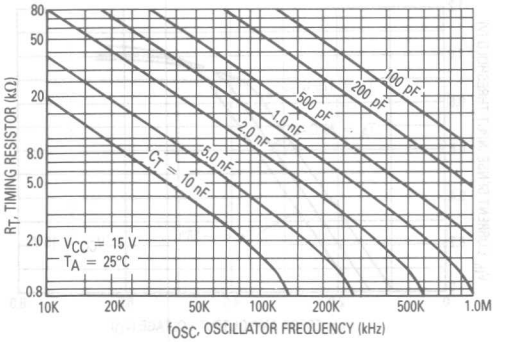


FIGURE 2 — OUTPUT DEAD TIME versus OSCILLATOR FREQUENCY

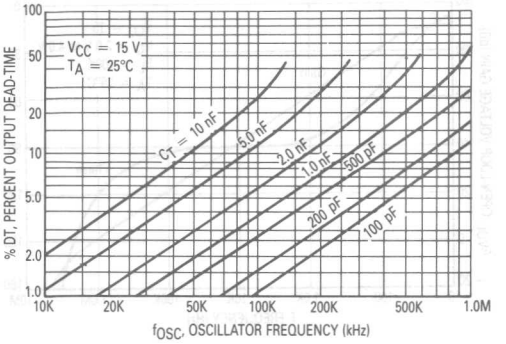


FIGURE 3 — OSCILLATOR DISCHARGE CURRENT versus TEMPERATURE

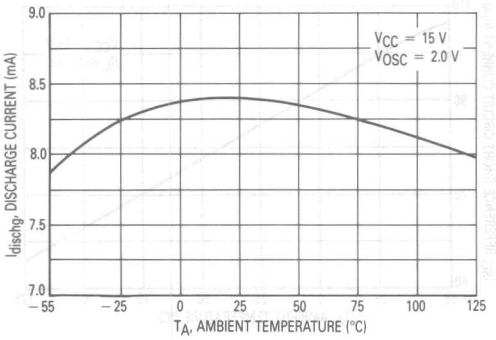


FIGURE 4 — MAXIMUM OUTPUT DUTY CYCLE versus TIMING RESISTOR

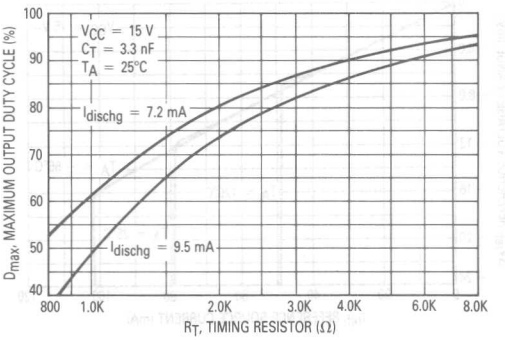


FIGURE 5 — ERROR AMP SMALL SIGNAL TRANSIENT RESPONSE

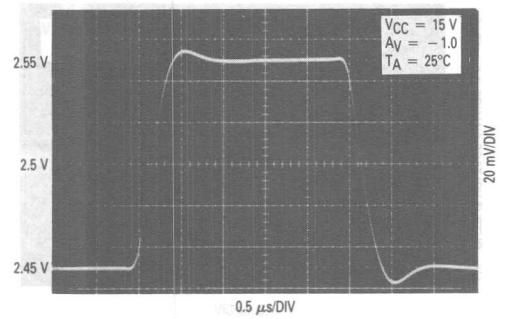


FIGURE 6 — ERROR AMP LARGE SIGNAL TRANSIENT RESPONSE

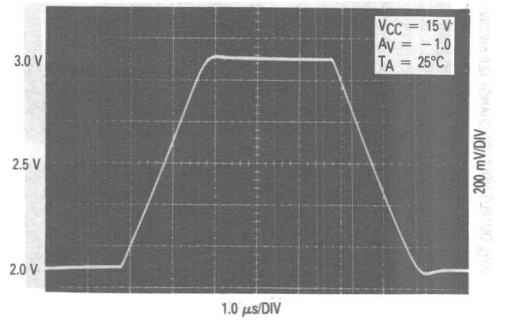


FIGURE 7 — ERROR AMP OPEN-LOOP GAIN AND PHASE versus FREQUENCY

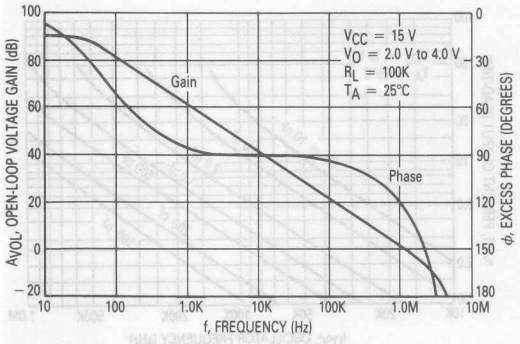


FIGURE 8 — CURRENT SENSE INPUT THRESHOLD versus ERROR AMP OUTPUT VOLTAGE

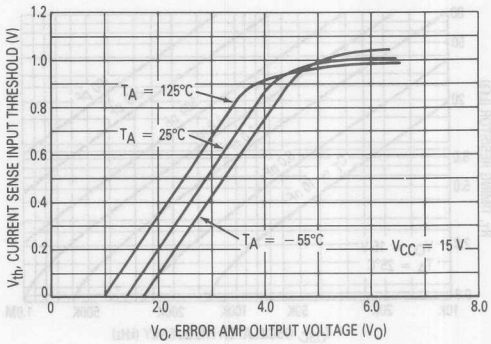


FIGURE 9 — REFERENCE VOLTAGE CHANGE versus SOURCE CURRENT

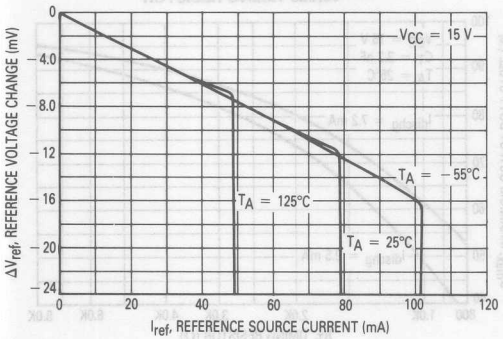


FIGURE 10 — REFERENCE SHORT CIRCUIT CURRENT versus TEMPERATURE

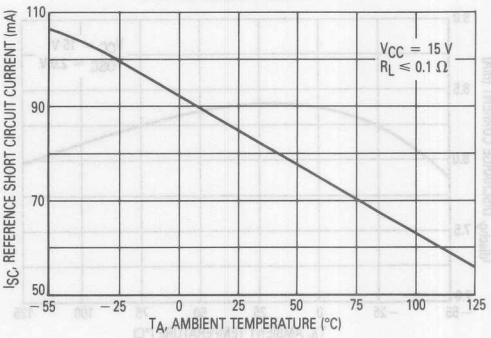


FIGURE 11 — REFERENCE LOAD REGULATION

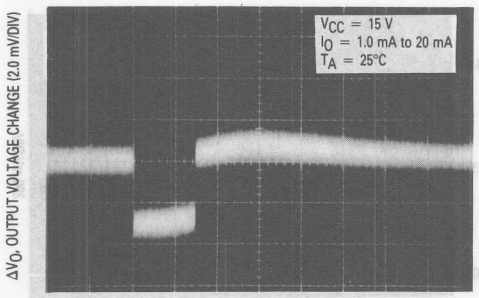


FIGURE 12 — REFERENCE LINE REGULATION

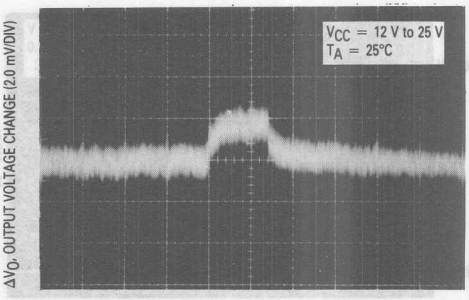


FIGURE 13 — OUTPUT SATURATION VOLTAGE versus LOAD CURRENT

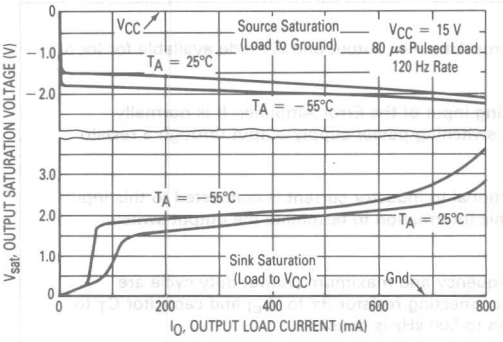


FIGURE 14 — OUTPUT WAVEFORM

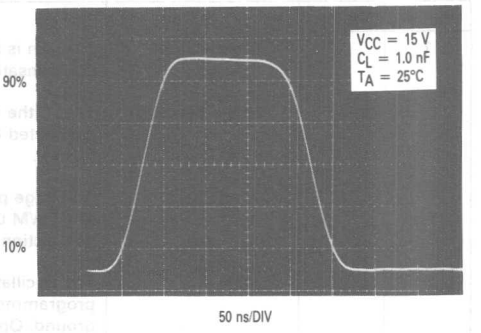


FIGURE 15 — OUTPUT CROSS CONDUCTION

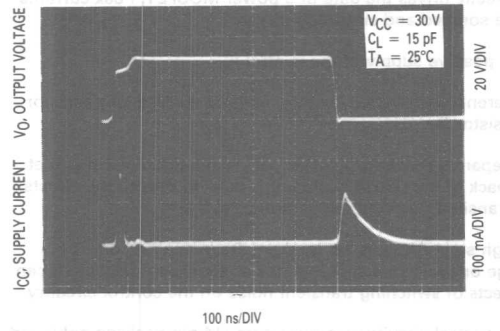
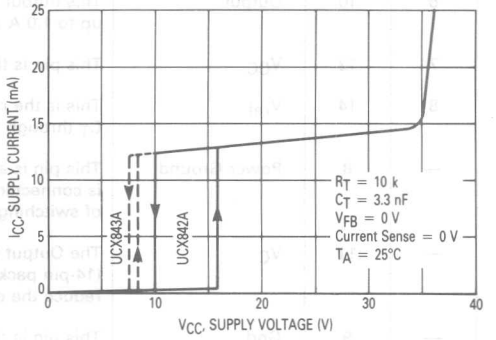


FIGURE 16 — SUPPLY CURRENT versus SUPPLY VOLTAGE



PIN FUNCTION DESCRIPTION

Pin No.		Function	Description
8-Pin	14-Pin		
1	1	Compensation	This pin is the Error Amplifier output and is made available for loop compensation.
2	3	Voltage Feedback	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	5	Current Sense	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	7	R_T/C_T	The Oscillator frequency and maximum Output duty cycle are programmed by connecting resistor R_T to V_{ref} and capacitor C_T to ground. Operation to 500 kHz is possible.
5	—	Gnd	This pin is the combined control circuitry and power ground (8-pin package only).
6	10	Output	This output directly drives the gate of a power MOSFET. Peak currents up to 1.0 A are sourced and sinked by this pin.
7	12	V_{CC}	This pin is the positive supply of the control IC.
8	14	V_{ref}	This is the reference output. It provides charging current for capacitor C_T through resistor R_T.
—	8	Power Ground	This pin is a separate power ground return (14-pin package only) that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
—	11	V_C	The Output high state (V_{OH}) is set by the voltage applied to this pin (14-pin package only). With a separate power source connection, it can reduce the effects of switching transient noise on the control circuitry.
—	9	Gnd	This pin is the control circuitry ground return (14-pin package only) and is connected back to the power source ground.
—	2,4,6,13	NC	No connection (14-pin package only). These pins are not internally connected.

OPERATING DESCRIPTION

The UC3842A, UC3843A series are high performance, fixed frequency, current mode controllers. They are specifically designed for Off-Line and DC-to-DC converter applications offering the designer a cost effective solution with minimal external components. A representative block diagram is shown in Figure 17.

Oscillator

The oscillator frequency is programmed by the values selected for the timing components R_T and C_T. Capacitor C_T is charged from the 5.0 V reference through resistor R_T to approximately 2.8 V and discharged to 1.2 V by an internal current sink. During the discharge of C_T, the oscillator generates an internal blanking pulse that holds the center input of the NOR gate high. This causes the Output to be in a low state, thus producing a controlled amount of output deadtime. Figure 1 shows R_T versus Oscillator Frequency and Figure 2, Output Deadtime versus Frequency, both for given values of C_T. Note that many values of R_T and C_T will give the same oscillator frequency but only one combination will yield a specific output deadtime at a given frequency. The oscillator thresholds are temperature compensated, and the discharge current is trimmed and guaranteed to within ±10% at T_J = 25°C. These internal circuit refinements minimize variations of oscillator frequency and maximum output duty cycle. The results are shown in Figures 3 and 4.

In many noise sensitive applications it may be desirable to frequency-lock the converter to an external system clock. This can be accomplished by applying a clock signal to the circuit shown in Figure 20. For reliable locking, the free-running oscillator frequency should be set about 10% less than the clock frequency. A method for multi unit synchronization is shown in Figure 21. By tailoring the clock waveform, accurate Output duty cycle clamping can be achieved.

Error Amplifier

A fully compensated Error Amplifier with access to the inverting input and output is provided. It features a typical DC voltage gain of 90 dB, and a unity gain bandwidth of 1.0 MHz with 57 degrees of phase margin (Figure 7). The non-inverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input. The maximum input bias current is −2.0 μA which can cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amp Output (Pin 1) is provided for external loop compensation (Figure 31). The output voltage is offset by two diode drops (≈1.4 V) and divided by three before it connects to the inverting input of the Current Sense Comparator. This guarantees that no drive pulses appear at the Output (Pin 6) when pin 1 is at its lowest state (V_{OL}). This occurs when the power supply is operating and the load is removed, or at the beginning of a soft-start interval (Figures 23, 24). The Error Amp minimum feedback resistance is limited by the amplifier's source current (0.5 mA) and the required output voltage (V_{OH}) to reach the comparator's 1.0 V clamp level:

$$R_{f(MIN)} \approx \frac{3.0\ (1.0\ V) + 1.4\ V}{0.5\ mA} = 8800\ \Omega$$

Current Sense Comparator and PWM Latch

The UC3842A, UC3843A operate as a current mode controller, whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier Output/Compensation (Pin 1). Thus the error signal controls the peak inductor current on a cycle-by-cycle basis. The Current Sense Comparator PWM Latch configuration used ensures that only a single pulse appears at the Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting the ground referenced sense resistor R_S in series with the source of output switch Q1. This voltage is monitored by the Current Sense Input (Pin 3) and compared a level derived from the Error Amp Output. The peak inductor current under normal operating conditions is controlled by the voltage at pin 1 where:

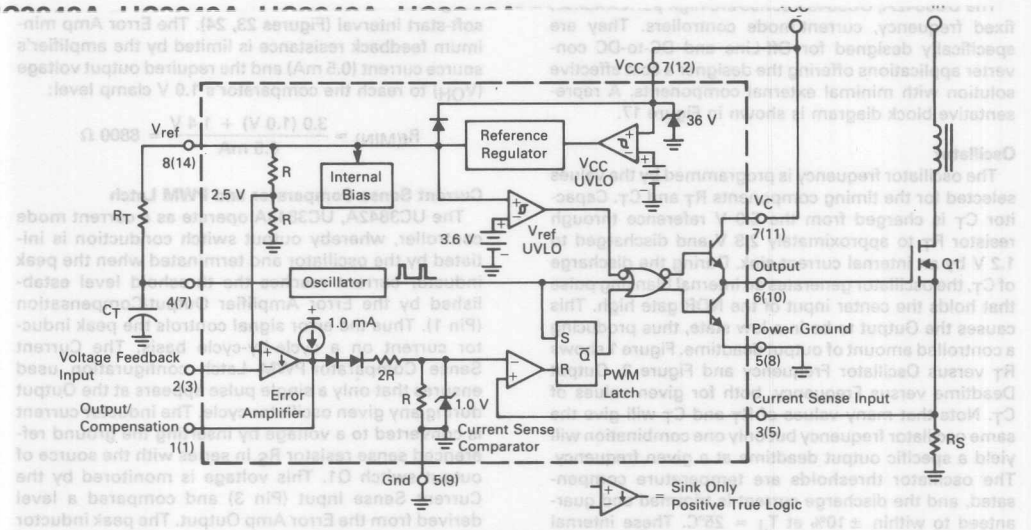
$$I_{pk} = \frac{V_{(Pin\ 1)} - 1.4\ V}{3\ R_S}$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the Current Sense Comparator threshold will be internally clamped to 1.0 V. Therefore the maximum peak switch current is:

$$I_{pk(max)} = \frac{1.0\ V}{R_S}$$

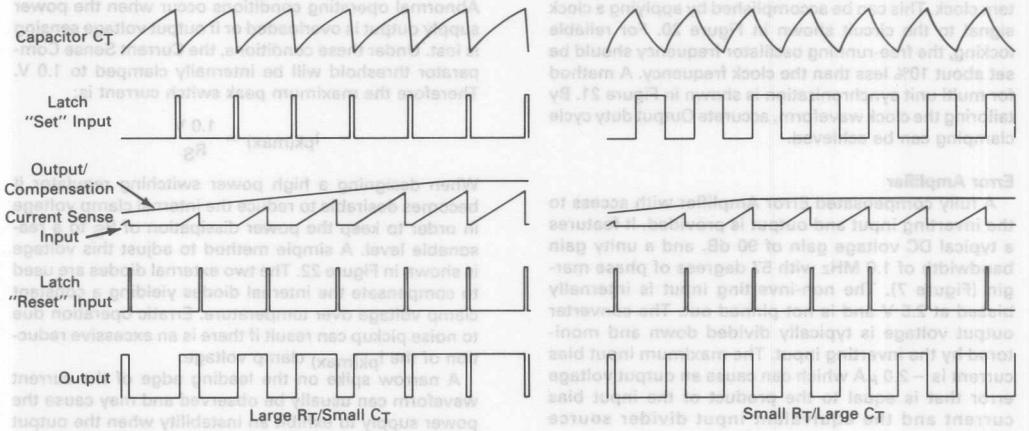
When designing a high power switching regulator it becomes desirable to reduce the internal clamp voltage in order to keep the power dissipation of R_S to a reasonable level. A simple method to adjust this voltage is shown in Figure 22. The two external diodes are used to compensate the internal diodes yielding a constant clamp voltage over temperature. Erratic operation due to noise pickup can result if there is an excessive reduction of the $I_{pk(max)}$ clamp voltage.

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Current Sense Input with a time constant that approximates the spike duration will usually eliminate the instability; refer to Figure 26.



Pin numbers adjacent to terminals are for the 8 pin dual-in-line package.
Pin numbers in parenthesis are for the D suffix SO-14 package.

FIGURE 18 — TIMING DIAGRAM



Undervoltage Lockout

Two undervoltage lockout comparators have been incorporated to guarantee that the IC is fully functional before the output stage is enabled. The positive power supply terminal (V_{CC}) and the reference output (V_{ref}) are each monitored by separate comparators. Each has built-in hysteresis to prevent erratic output behavior as their respective thresholds are crossed. The V_{CC} comparator upper and lower thresholds are 16 V/10 V for the UCX842A, and 8.4 V/7.6 V for the UCX843A. The V_{ref} comparator upper and lower thresholds are 3.6 V/3.4 V. The large hysteresis and low start-up current of the UCX842A makes it ideally suited in off-line converter applications where efficient bootstrap start-up tech-

niques are required (Figure 33). The UCX843A is intended for lower voltage DC to DC converter applications. A 36 V zener is connected as a shunt regulator from V_{CC} to ground. Its purpose is to protect the IC from excessive voltage that can occur during system start-up. The minimum operating voltage for the UCX842A is 11 V and 8.2 V for the UCX843A.

Output

These devices contain a single totem pole output stage that was specifically designed for direct drive of power MOSFET's. It is capable of up to ±1.0 A peak drive current and has a typical rise and fall time of 50 ns with a 1.0 nF load. Additional internal circuitry has been added to keep the Output in a sinking mode whenever an undervoltage lockout is active. This characteristic eliminates the need for an external pull-down resistor.

The SO-14 surface mount package provides separate pins for V_C (output supply) and Power Ground. Proper implementation will significantly reduce the level of switching transient noise imposed on the control circuitry. This becomes particularly useful when reducing the $I_{pk(max)}$ clamp level. The separate V_C supply input allows the designer added flexibility in tailoring the drive voltage independent of V_{CC}. A zener clamp is typically connected to this input when driving power MOSFETs in systems where V_{CC} is greater than 20 V. Figure 25 shows proper power and control ground connections in a current sensing power MOSFET application.

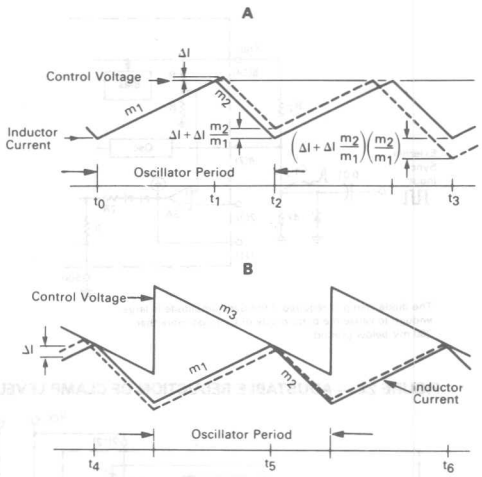
Reference

The 5.0 V bandgap reference is trimmed to ±1.0% tolerance at T_J = 25°C on the UC284XA, and ±2.0% on the UC384XA. Its primary purpose is to supply charging current to the oscillator timing capacitor. The reference has short circuit protection and is capable of providing in excess of 20 mA for powering additional control system circuitry.

Design Considerations

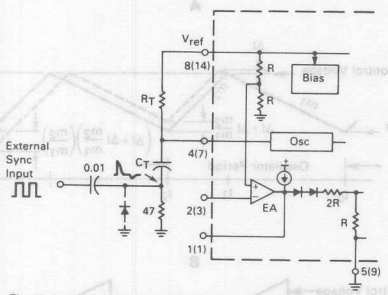
Do not attempt to construct the converter on wire-wrap or plug-in prototype boards. High frequency circuit layout techniques are imperative to prevent pulse-width jitter. This is usually caused by excessive noise pick-up imposed on the Current Sense or Voltage Feedback inputs. Noise immunity can be improved by lowering circuit impedances at these points. The printed circuit layout should contain a ground plane with low-current signal and high-current switch and output grounds returning on separate paths back to the input filter capacitor. Ceramic bypass capacitors (0.1 μF) connected directly to V_{CC}, V_C, and V_{ref} may be required depending upon circuit layout. This provides a low impedance path for filtering the high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI. The Error Amp compensation circuitry and the converter output voltage divider should be located close to the IC and as far as possible from the power switch and other noise generating components.

FIGURE 19 — CONTINUOUS CURRENT WAVEFORMS



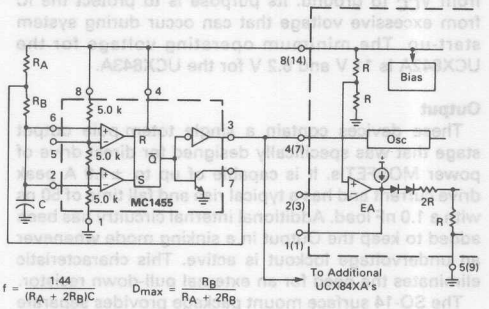
Current mode converters can exhibit subharmonic oscillations when operating at a duty cycle greater than 50% with continuous inductor current. This instability is independent of the regulators closed loop characteristics and is caused by the simultaneous operating conditions of fixed frequency and peak current detecting. Figure 19A shows the phenomenon graphically. At t_0, switch conduction begins, causing the inductor current to rise at a slope of m_1. This slope is a function of the input voltage divided by the inductance. At t_1, the Current Sense Input reaches the threshold established by the control voltage. This causes the switch to turn off and the current to decay at a slope of m_2, until the next oscillator cycle. The unstable condition can be shown if a pertubation is added to the control voltage, resulting in a small ΔI (dashed line). With a fixed oscillator period, the current decay time is reduced, and the minimum current at switch turn-on (t_2) is increased by $\Delta I + \Delta I\, m_2/m_1$. The minimum current at the next cycle (t_3) decreases to $(\Delta I + \Delta I\, m_2/m_1)(m_2/m_1)$. This pertubation is multiplied by m_2/m_1 on each succeeding cycle, alternately increasing and decreasing the inductor current at switch turn-on. Several oscillator cycles may be required before the inductor current reaches zero causing the process to commence again. If m_2/m_1 is greather than 1, the converter will be unstable. Figure 19B shows that by adding an artificial ramp that is synchronized with the PWM clock to the control voltage, the ΔI pertubation will decrease to zero on succeeding cycles. This compensating ramp (m_3) must have a slope equal to or slightly greater than $m_2/2$ for stability. With $m_2/2$ slope compensation, the average inductor current follows the control voltage yielding true current mode operation. The compensating ramp can be derived from the oscillator and added to either the Voltage Feedback or Current Sense inputs (Figure 32).

FIGURE 20 — EXTERNAL CLOCK SYNCHRONIZATION



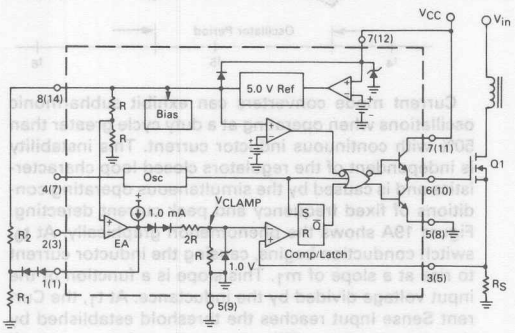
The diode clamp is required if the Sync amplitude is large enough to cause the bottom side of C_T to go more than 300 mV below ground.

FIGURE 21 — EXTERNAL DUTY CYCLE CLAMP AND MULTI UNIT SYNCHRONIZATION



$$f = \frac{1.44}{(R_A + 2R_B)C} \qquad D_{max} = \frac{R_B}{R_A + 2R_B}$$

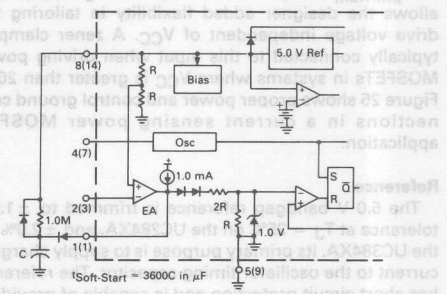
FIGURE 22 — ADUSTABLE REDUCTION OF CLAMP LEVEL



$$V_{Clamp} \approx \frac{1.67}{\left(\frac{R_2}{R_1} + 1\right)} + 0.33 \times 10^{-3}\left(\frac{R_1 R_2}{R_1 + R_2}\right) \qquad I_{pk(max)} \approx \frac{V_{Clamp}}{R_S}$$

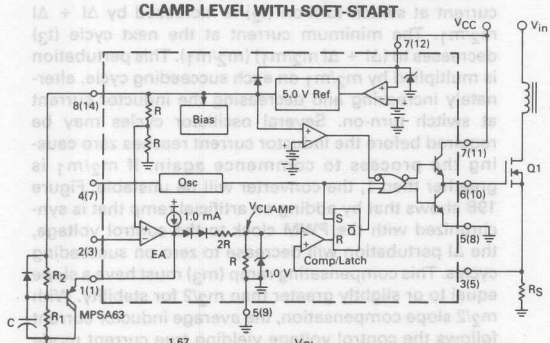
Where: $0 \leq V_{Clamp} \leq 1.0$ V

FIGURE 23 — SOFT-START CIRCUIT



$t_{Soft\text{-}Start} \approx 3600C$ in μF

FIGURE 24 — ADJUSTABLE BUFFERED REDUCTION OF CLAMP LEVEL WITH SOFT-START

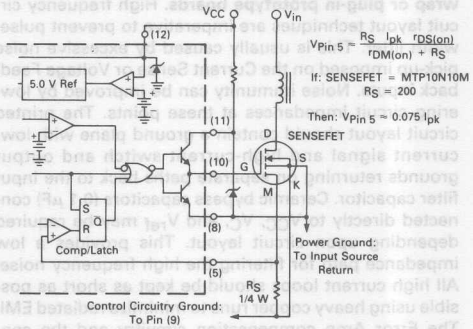


$$V_{Clamp} \approx \frac{1.67}{\left(\frac{R_2}{R_1} + 1\right)} \qquad I_{pk(max)} \approx \frac{V_{Clamp}}{R_S}$$

Where: $0 \leq V_{Clamp} \leq 1.0$ V

$$t_{SOFTSTART} = -\ln\left[1 - \frac{V_C}{3\,V_{CLAMP}}\right] C\,\frac{R_1 R_2}{R_1 + R_2}$$

FIGURE 25 — CURRENT SENSING POWER MOSFET



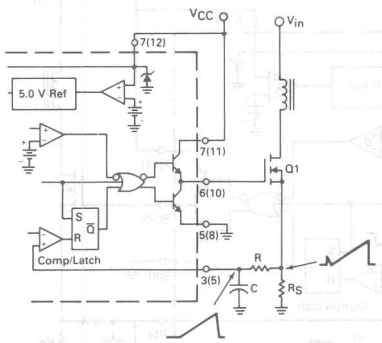
$$V_{Pin\,5} \approx \frac{R_S\ I_{pk}\ r_{DS(on)}}{r_{DM(on)} + R_S}$$

If: SENSEFET = MTP10N10M
$R_S = 200$

Then: $V_{Pin\,5} \approx 0.075\ I_{pk}$

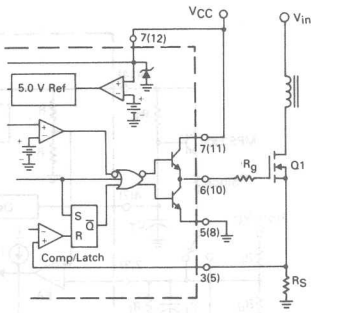
Virtually lossless current sensing can be achieved with the implementation of a SENSEFET power switch. For proper operation during over current conditions, a reduction of the $I_{pk(max)}$ clamp level must be implemented. Refer to Figures 22 and 24.

FIGURE 26 — CURRENT WAVEFORM SPIKE SUPPRESSION



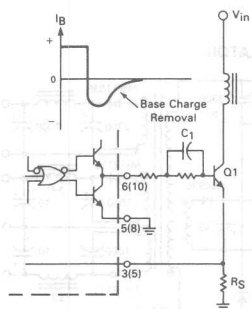
The addition of the RC filter will eliminate instability caused by the leading edge spike on the current waveform.

FIGURE 27 — MOSFET PARASITIC OSCILLATIONS



Series gate resistor R_G will damp any high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate-source circuit.

FIGURE 28 — BIPOLAR TRANSISTOR DRIVE



The totem-pole output can furnish negative base current for enhanced transistor turn-off, with the addition of capacitor C_1.

FIGURE 29 — ISOLATED MOSFET DRIVE

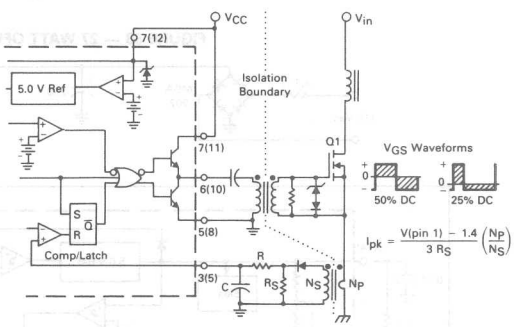
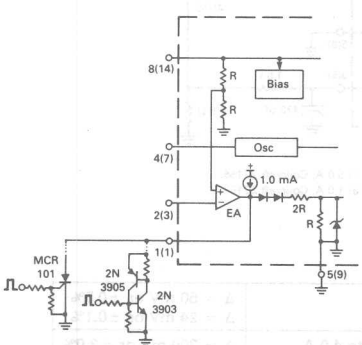
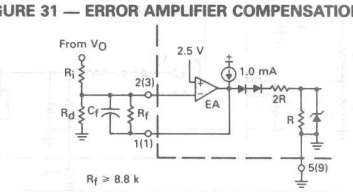


FIGURE 30 — LATCHED SHUTDOWN

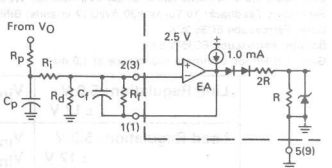


The MCR101 SCR must be selected for a holding of less than 0.5 mA at $T_{A(min)}$. The simple two transistor circuit can be used in place of the SCR as shown. All resistors are 10 k.

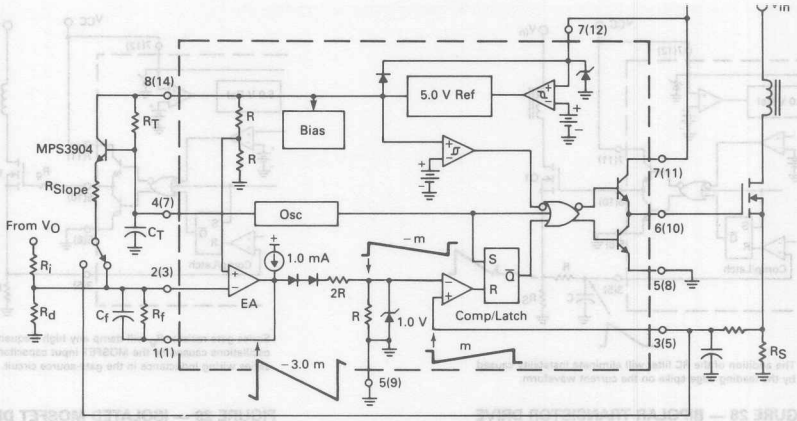
FIGURE 31 — ERROR AMPLIFIER COMPENSATION



Error Amp compensation circuit for stabilizing any current-mode topology except for boost and flyback converters operating with continuous inductor current.

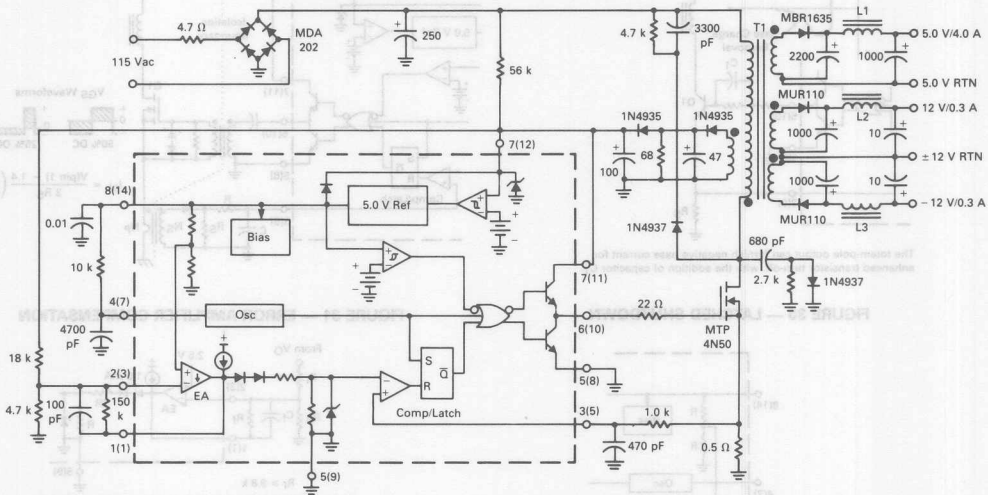


Error Amp compensation circuit for stabilizing current-mode boost and flyback topologies operating with continuous inductor current.



The buffered oscillator ramp can be resistively summed with either the voltage feedback or current sense inputs to provide slope compensation.

FIGURE 33 — 27 WATT OFF-LINE FLYBACK REGULATOR



T1 — Primary: 45 Turns #26 AWG
Secondary ± 12 V: 9 Turns #30 AWG (2 strands) Bifiliar Wound
Secondary 5.0 V: 4 Turns (six strands) #26 Hexfiliar Wound
Secondary Feedback: 10 Turns #30 AWG (2 strands) Bifiliar Wound
Core: Ferroxcube EC35-3C8
Bobbin: Ferroxcube EC35PCB1
Gap: ≈ 0.10" for a primary inductance of 1.0 mH

L1 — 15 μH at 5.0 A, Coilcraft Z7156.
L2, L3 — 25 μH at 1.0 A, Coilcraft Z7157.

Line Regulation: 5.0 V ±12 V	V_{in} = 95 to 130 Vac	Δ = 50 mV or ±0.5% Δ = 24 mV or ±0.1%
Load Regulation: 5.0 V ±12 V	V_{in} = 115 Vac, I_{out} = 1.0 A to 4.0 A V_{in} = 115 Vac, I_{out} = 100 mA to 300 mA	Δ = 300 mV or ±3.0% Δ = 60 mV or ±0.25%
Output Ripple: 5.0 V ±12 V	V_{in} = 115 Vac	40 mV_{p-p} 80 mV_{p-p}
Efficiency	V_{in} = 115 Vac	70%

All outputs are at nominal load currents unless otherwise noted.

MOTOROLA

μA78S40

Specifications and Applications Information

UNIVERSAL SWITCHING REGULATOR SUBSYSTEM

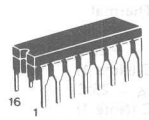
SILICON MONOLITHIC INTEGRATED CIRCUIT

3

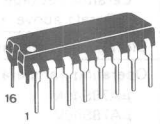
The μA78S40 is a monolithic-switching regulator subsystem, providing all active functions necessary for a switching regulator system. The device consists of a temperature compensated voltage reference, controlled-duty cycle oscillator with an active current limit circuit, comparator, high-current and high-voltage output switch, capable of 1.5 A and 40 V, pinned-out power diode and an uncommitted operational amplifier, which can be powered up or down independent of the IC supply. The switching output can drive external NPN or PNP transistors when voltages greater than 40 V, or currents in excess of 1.5 A, are required. Some of the features are wide-supply voltage range, low standby current, high efficiency and low drift. The μA78S40 is available in commercial (0°C to +70°C), automotive (−40°C to +85°C), and military (−55°C to +125°C) temperature ranges.

Some of the applications include use in step-up, step-down, and inverting regulators, with extremely good results obtained in battery-operated systems.

- Output Adjustable from 1.25 V to 40 V
- Peak Output Current of 1.5 A Without External Transistor
- 80 dB Line and Load Regulation
- Operation from 2.5 V to 40 V Supply
- Low Standby Current Drain
- High Gain, High Output Current, Uncommitted Op Amp

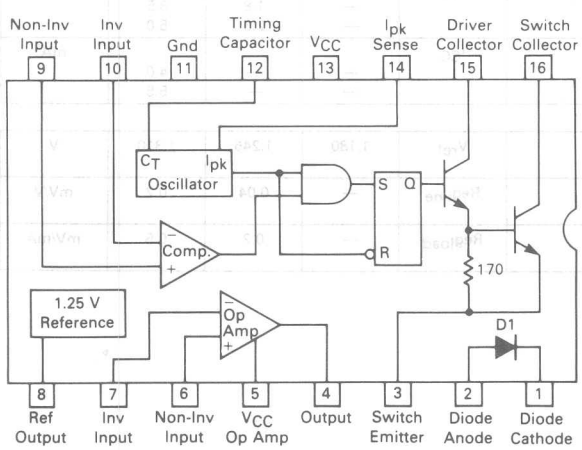


D SUFFIX
CERAMIC PACKAGE
CASE 620-10



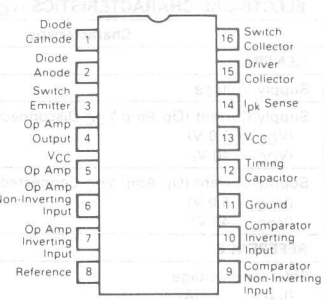
P SUFFIX
PLASTIC PACKAGE
CASE 648-06

BLOCK DIAGRAM



(Bottom View)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
μA78S40PC	0°C to +70°C	Plastic DIP
μA78S40PV	−40°C to +85°C	Plastic DIP
μA78S40DC	0°C to +70°C	Ceramic DIP
μA78S40DM	−55°C to +125°C	Ceramic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	V
Op Amp Power Supply Voltage	V_{CC} (Op Amp)	40	V
Common Mode Input Range (Comparator and Op Amp)	V_{ICR}	−0.3 to V_{CC}	V
Differential Input Voltage (Note 2)	V_{ID}	±30	V
Output Short-Circuit Duration (Op Amp)	—	Continuous	—
Reference Output Current	I_{ref}	10	mA
Voltage from Switch Collectors to Gnd	—	40	V
Voltage from Switch Emitters to Gnd	—	40	V
Voltage from Switch Collectors to Emitter	—	40	V
Voltage from Power Diode to Gnd	—	40	V
Reverse-Power Diode Voltage	V_{DR}	40	V
Current through Power Switch	I_{SW}	1.5	A
Current through Power Diode	I_D	1.5	A
Power Dissipation and Thermal Characteristics Plastic Package — T_A = +25°C Derate above +25°C (Note 1) Ceramic Package — T_A = 25°C Derate above +25°C (Note 1)	 P_D $1/R_{\theta JA}$ P_D $1/R_{\theta JA}$	 1500 14 1000 8.0	 mW mW/°C mW mW/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Operating Temperature Range μA78S40M μA78S40V μA78S40C	T_A	 −55 to +125 −40 to +85 0 to +70	°C

Notes:
1. T_{low} = −55°C for μA78S40DM = −40°C for μA78S40PV = 0°C for μA78S40DC and μA78S40PC; T_{high} = +125°C for μA78S40DM = +85°C for μA78S40PV = +70°C for μA78S40DC and μA78S40PC
2. For supply voltages less than 30 V the maximum differential input voltage (Error Amp and Op Amp) is equal to the supply voltage.

ELECTRICAL CHARACTERISTICS (V_{CC} = V_{CC} (Op Amp) = 5.0 V, T_A = T_{low} to T_{high} unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
GENERAL					
Supply Voltage	V_{CC}	2.5	—	40	V
Supply Current (Op Amp V_{CC} Disconnected) (V_{CC} = 5.0 V) (V_{CC} = 40 V)	I_{CC}	 — —	 1.8 2.3	 3.5 5.0	mA
Supply Current (Op Amp V_{CC} Connected) (V_{CC} = 5.0 V) (V_{CC} = 40 V)	I_{CC}	 — —	 — —	 4.0 5.5	mA
REFERENCE					
Reference Voltage (I_{ref} = 1.0 mA)	V_{ref}	1.180	1.245	1.310	V
Reference Voltage Line Regulation (3.0 V ≤ V_{CC} ≤ 40 V, I_{ref} = 1.0 mA, T_A = 25°C)	Reg_{line}	—	0.04	0.2	mV/V
Reference Voltage Load Regulation (1.0 mA ≤ I_{ref} ≤ 10 mA, T_A = 25°C)	Reg_{load}	—	0.2	0.5	mV/mA

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Charging Current (T_A = 25°C) (V_{CC} = 5.0 V) (V_{CC} = 40 V)	I_{chg}	 20 20	 — —	 50 70	μA
Discharge Current (T_A = 25°C) (V_{CC} = 5.0 V) (V_{CC} = 40 V)	I_{dis}	 150 150	 — —	 250 350	μA
Oscillator Voltage Swing (T_A = 25°C) (V_{CC} = 5.0 V)	V_{osc}	—	0.5	—	V
Ratio of Charge/Discharge Time	t_{chg}/t_{dis}	—	6.0	—	—
CURRENT LIMIT					
Current-Limit Sense Voltage (T_A = 25°C) (V_{CC} – V_{Ipk} Sense)	V_{CLS}	250	—	350	mV
OUTPUT SWITCH					
Output Saturation Voltage 1 (I_{SW} = 1.0 A, Pin 15 tied to Pin 16)	V_{sat1}	—	0.93	1.3	V
Output Saturation Voltage 2 (I_{SW} = 1.0 A, I_{15} = 50 mA)	V_{sat2}	—	0.5	0.7	V
Output Transistor Current Gain (T_A = 25°C) (I_C = 1.0 A, V_{CE} = 5.0 V)	h_{FE}	—	70	—	—
Output Leakage Current (T_A = 25°C) (V_{CE} = 40 V)	$I_{C(off)}$	—	10	—	nA
POWER DIODE					
Forward Voltage Drop (I_D = 1.0 A)	V_D	—	1.25	1.5	V
Diode Leakage Current (T_A = 25°C) (V_{DR} = 40 V)	I_{DR}	—	10	—	nA
COMPARATOR					
Input Offset Voltage (V_{CM} = V_{Ref})	V_{IO}	—	1.5	15	mV
Input Bias Current (V_{CM} = V_{Ref})	I_{IB}	—	35	200	nA
Input Offset Current (V_{CM} = V_{Ref})	I_{IO}	—	5.0	75	nA
Common-Mode Voltage Range (T_A = 25°C)	V_{ICR}	0	—	V_{CC} – 2.0	V
Power-Supply Rejection Ratio (T_A = 25°C) (3.0 ≤ V_{CC} ≤ 40 V)	PSRR	70	96	—	dB
OUTPUT OPERATIONAL AMPLIFIER					
Input Offset Voltage (V_{CM} = 2.5 V)	V_{IO}	—	4.0	15	mV
Input Bias Current (V_{CM} = 2.5 V)	I_{IB}	—	30	200	nA
Input Offset Current (V_{CM} = 2.5 V)	I_{IO}	—	5.0	75	nA
Voltage Gain + (T_A = 25°C) (R_L = 2.0 kΩ to Gnd, 1.0 V ≤ V_O ≤ 2.5 V)	A_{VOL+}	25	250	—	V/mV
Voltage Gain – (T_A = 25°C) (R_L = 2.0 kΩ to V_{CC} (Op Amp), 1.0 V ≤ V_O ≤ 2.5 V)	A_{VOL-}	25	250	—	V/mV
Common-Mode Voltage Range (T_A = 25°C)	V_{ICR}	0	—	V_{CC} – 2.0	V
Common-Mode Rejection Ratio (T_A = 25°C) (V_{CM} = 0 to 3.0 V)	CMRR	76	100	—	dB
Power-Supply Rejection Ratio (T_A = 25°C) (3.0 V ≤ V_{CC} (Op Amp) ≤ 40 V)	PSRR	76	100	—	dB
Output Source Current (T_A = 25°C)	I_{Source}	75	150	—	mA
Output Sink Current (T_A = 25°C)	I_{Sink}	10	35	—	mA
Slew Rate (T_A = 25°C)	SR	—	0.6	—	V/μs
Output Low Voltage (T_A = 25°C, I_L = –5.0 mA)	V_{OL}	—	—	1.0	V
Output High Voltage (T_A = 25°C, I_L = 50 mA)	V_{OH}	V_{CC} (Op Amp) – 3.0	—	—	V

3

versus OSCILLATOR TIMING CAPACITOR

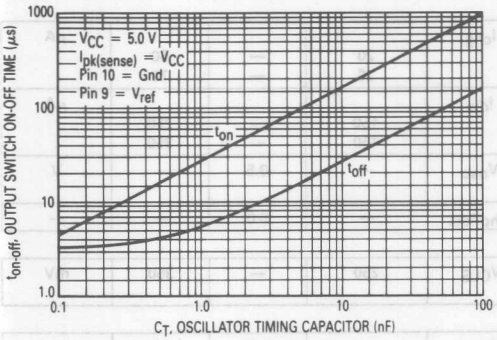
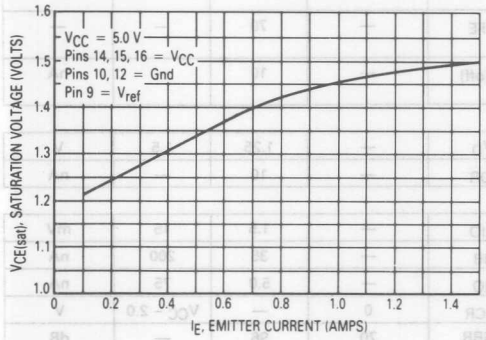


FIGURE 3 — EMITTER-FOLLOWER CONFIGURATION OUTPUT SWITCH SATURATION VOLTAGE versus EMITTER CURRENT



versus SUPPLY VOLTAGE

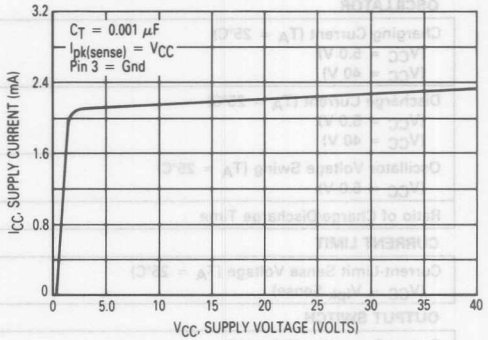
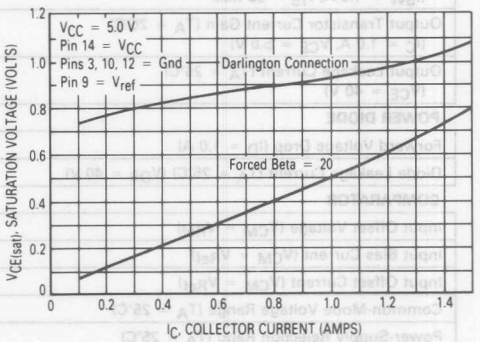


FIGURE 4 — COMMON-EMITTER CONFIGURATION OUTPUT SWITCH SATURATION VOLTAGE versus COLLECTOR CURRENT



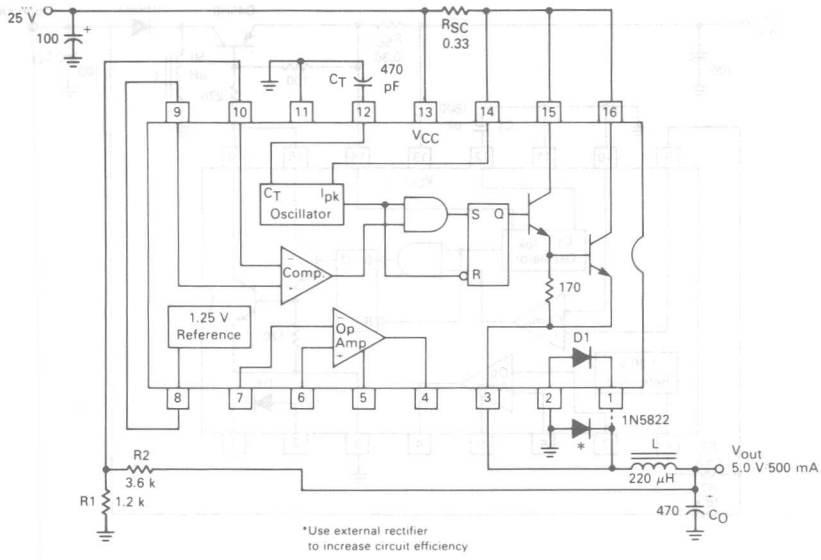
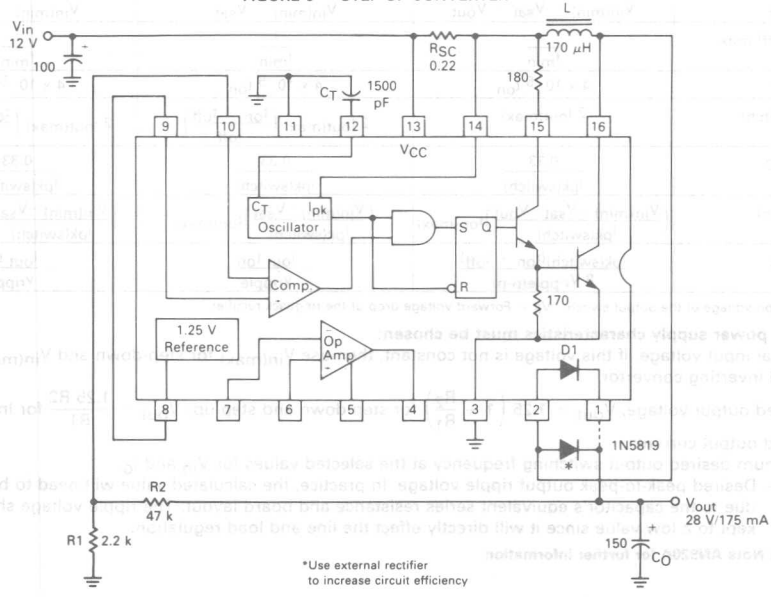


FIGURE 6 — STEP-UP CONVERTER



3°

FIGURE 7 — INVERTING CONVERTER

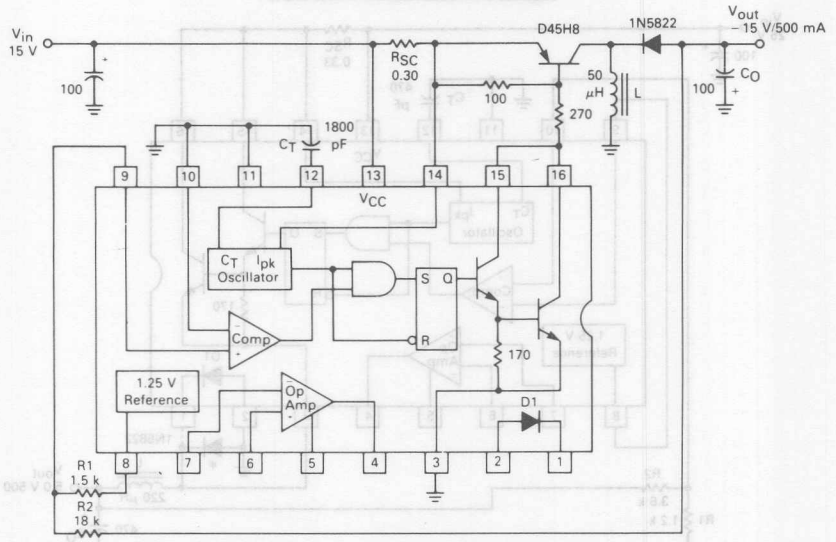


FIGURE 8 — DESIGN FORMULA TABLE

Calculation	Step-Down	Step-Up	Inverting
$\frac{t_{on}}{t_{off}}$	$\frac{V_{out} + V_F}{V_{in(min)} - V_{sat} - V_{out}}$	$\frac{V_{out} + V_F}{V_{in(min)} - V_{sat}}\left(\frac{V_{in(min)}}{}\right)$	$\frac{V_{out} + V_F}{V_{in(min)} - V_{sat}}$
$(t_{on} + t_{off})$ max	$\frac{1}{f_{min}}$	$\frac{1}{f_{min}}$	$\frac{1}{f_{min}}$
C_T	$4 \times 10^{5} t_{on}$	$4 \times 10^{5} t_{on}$	$4 \times 10^{5} t_{on}$
$I_{pk(switch)}$	$2 I_{out(max)}$	$2 I_{out(max)} \left(\frac{t_{on} + t_{off}}{t_{off}}\right)$	$2 I_{out(max)} \left(\frac{t_{on} + t_{off}}{t_{off}}\right)$
R_{SC}	$\frac{0.33}{I_{pk(switch)}}$	$\frac{0.33}{I_{pk(switch)}}$	$\frac{0.33}{I_{pk(switch)}}$
$L_{(min)}$	$\left(\frac{V_{in(min)} - V_{sat} - V_{out}}{I_{pk(switch)}}\right) t_{on(max)}$	$\left(\frac{V_{in(min)} - V_{sat}}{I_{pk(switch)}}\right) t_{on(max)}$	$\left(\frac{V_{in(min)} - V_{sat}}{I_{pk(switch)}}\right) t_{on(max)}$
C_O	$\frac{I_{pk(switch)}(t_{on} + t_{off})}{8 V_{ripple(p-p)}}$	$\approx \frac{I_{out}\, t_{on}}{V_{ripple}}$	$\approx \frac{I_{out}\, t_{on}}{V_{ripple}}$

V_{sat} = Saturation voltage of the output switch. V_F = Forward voltage drop of the ringback rectifier.

The following power supply characteristics must be chosen:

V_{in} — Nominal input voltage. If this voltage is not constant, then use $V_{in(max)}$ for step-down and $V_{in(min)}$ for step-up and inverting convertor.

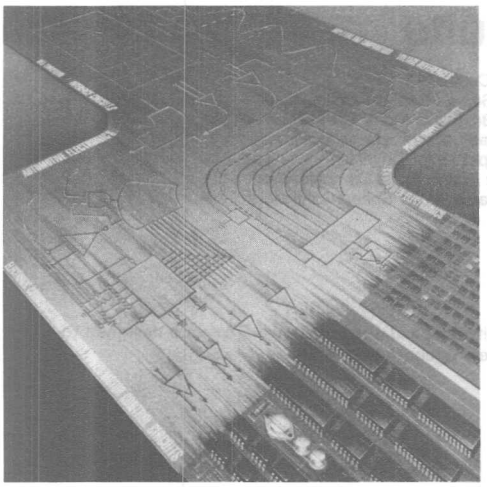
V_{out} — Desired output voltage, $V_{out} = 1.25\left(1 + \frac{R_2}{R_1}\right)$ for step-down and step-up; $V_{out} = \frac{1.25\ R2}{R1}$ for Inverting.

I_{out} — Desired output current.

f_{min} — Minimum desired output switching frequency at the selected values for V_{in} and I_o.

$V_{ripple(p-p)}$ — Desired peak-to-peak output ripple voltage. In practice, the calculated value will need to be increased due to the capacitor's equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly effect the line and load regulation.

See Application Note AN920A for further information.



Power/Motor Control Circuits

4

In Brief . . .

With the expansion of electronics into more and more mechanical systems there comes an ever increasing demand for simple but intelligent circuits that can blend these two technologies together. In past years, the task of power/motor control was once the domain of discrete devices. But today, increasingly, this task is being performed by bipolar IC technology because of cost, size, and reliability constraints. Motorola offers integrated circuits designed to anticipate the requirements for both simple and sophisticated control systems, while providing cost effective solutions to meet the application.

Selector Guide
- **Power Controllers** 4-2
- **Motor Controllers** 4-4

Alphanumeric Listing 4-7

Data Sheets 4-8

Zero Voltage Controller 4-3
Integrated Solenoid Driver 4-3
High-Side Driver Switch. 4-3
DC Brushless Motor Controller 4-4
Closed-Loop Brushless Motor Adapter 4-5
Stepper Motor Drivers 4-5
Triac Phase Angle Controller 4-5
Universal Motor Speed Controllers 4-6

Power Controllers

4

An assortment of battery and ac line-operated control ICs for specific applications are shown. They are designed to enhance system performance and reduce complexity in a wide variety of control applications.

Zero Voltage Switches

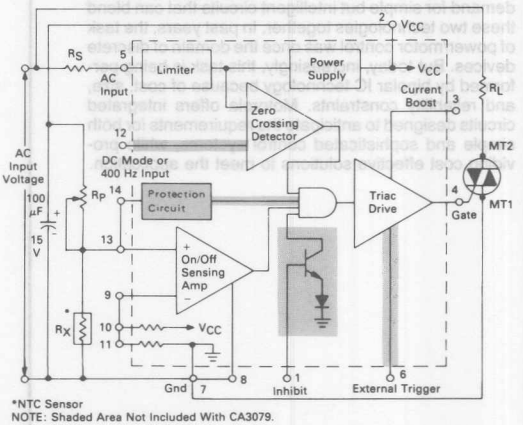
CA3079P/CA3059P

T_A = −40° to +85°C, Case 646

. . . designed for thyristor control in a variety of ac power switching applications for ac input voltages of 24 V, 120 V, 208/230 V, and 227 V @ 50/60 Hz. Features include:

- Limiter-Power Supply — Allows operation directly from an ac line.
- Differential On/Off Sensing Amplifier — Tests for condition of external sensors or input command signals. Proportional control capability or hysteresis may be implemented.
- Zero-Crossing Detector — Synchronizes the output pulses to the zero voltage point of the ac cycle. Eliminates RFI when used with resistive loads.
- Triac Drive — Supplies high-current pulses to the external power controlling thyristor.
- Protection Circuit (CA3059 only) — A built-in circuit may be actuated, if the sensor opens or shorts, to remove the drive circuit from the external triac.
- Inhibit Capability (CA3059 only) — Thyristor firing may be inhibited by the action of an internal diode gate.
- High Power DC Comparator Operation (CA3059 only) — Operation in this mode is accomplished by connecting Pin 7 to Pin 12 (thus overriding the action of the zero-crossing detector).

CA3079



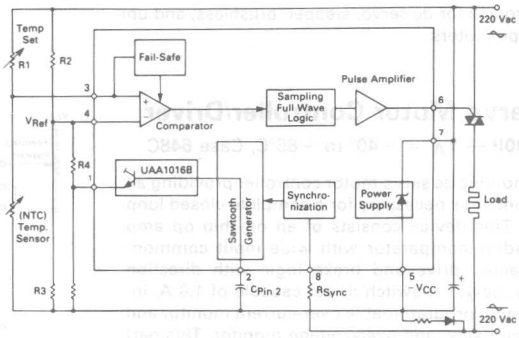
*NTC Sensor
NOTE: Shaded Area Not Included With CA3079.

UAA1016B — T_A = −20° to +100°C, Case 626

. . . designed to drive triacs with the Zero Voltage technique which allows RFI free power regulation of resistive loads. They provide the following features:

- Proportional Temperature Control Over an Adjustable Band
- Adjustable Burst Frequency (to Comply with Standards)
- Sensor Fail-Safe
- No dc Current Component Through the Main Line (to Comply with Standards)
- Negative Output Current Pulses (Triacs Quadrants 2 and 3)
- Direct ac Line Operation
- Low External Components Count

UAA1016B

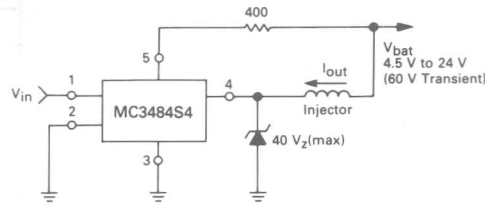


Integrated Solenoid Driver

MC3484S2,S4 — T_J = −40° to +125°C, Case 314D

The MC3484 is an integrated monolithic solenoid driver. Its typical function is to apply full battery voltage to fuel injector(s) for rapid current rise, in order to produce positive injector opening. When load current reaches a preset level (4.0 A in MC3484S4 or 2.4 A in MC3484S2) the injector driver reduces the load current by a 4-to-1 ratio and operates as a constant current supply. This condition holds the injector open and reduces system dissipation.

MC3484



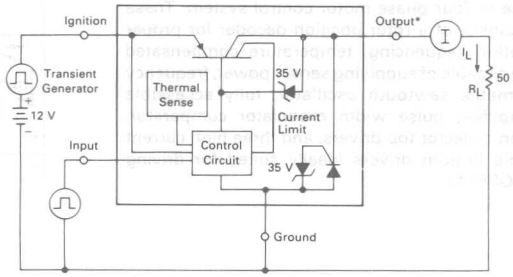
High-Side Driver Switch

MC3399T — T_J = −40° to +150°C, Case 314D

The MC3399T is a High-Side Driver Switch that is designed to drive loads from the positive side of the power supply. The output is controlled by a TTL compatible Enable pin. In the ON state, the device exhibits very low saturation voltages for load currents in excess of 750 mA. The device also protects the load from positive- or negative-going high voltage transients by becoming an open circuit and isolating the transient for its duration from the load.

The MC3399T is fabricated on a power BIMOS process which combines the best features of Bipolar and MOS technologies. The mixed technology provides higher gain PNP output devices and results in Power Integrated Circuits with reduced quiescent current.

MC3399T



NOTE:
*Depending on Load Current and Transient Duration, an Output Capacitor (C_O) of sufficient value may be used to hold up Output Voltage during the Transient, and absorb Turn-off Delay Voltage Overshoot.

Motor Controllers

This section contains integrated circuits designed for cost effective control of specific motor-families. Included are controllers for dc servo, stepper, brushless, and universal type motors.

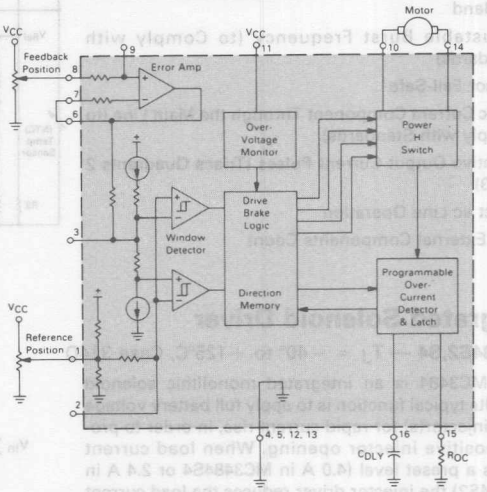
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DC Servo Motor Controller/Driver

MC33030P — T_A = −40° to +85°C, Case 648C

A monolithic dc servo motor controller providing all active functions necessary for a complete closed loop system. This device consists of an on-chip op amp and window comparator with wide input common-mode range, drive and brake logic with direction memory, power H switch driver capable of 1.0 A, independently programmable over-current monitor and shutdown delay, and over-voltage monitor. This part is ideally suited for almost any servo positioning application that requires sensing of temperature, pressure, light, magnetic flux, or any other means that can be converted to a voltage.

MC33030P

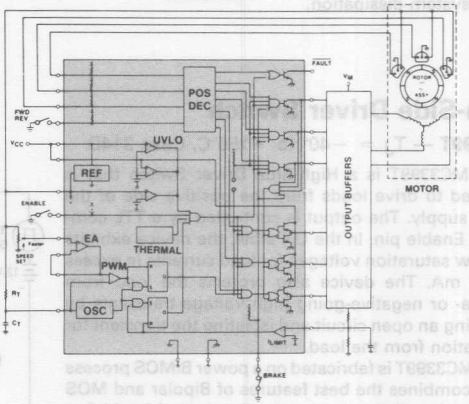


DC Brushless Motor Controller

MC33034P60,P120 — T_A = −40° to +85°C, Case 724

The MC33034 Series is a high performance monolithic brushless motor controller containing all of the active functions required to implement a full featured open-loop three or four phase motor control system. These devices consist of a rotor position decoder for proper commutation sequencing, temperature compensated reference capable of supplying sensor power, frequency programmable sawtooth oscillator, fully accessible error amplifier, pulse width modulator comparator, three open collector top drivers, and three high current totem pole bottom drivers ideally suited for driving power MOSFETs.

MC33034

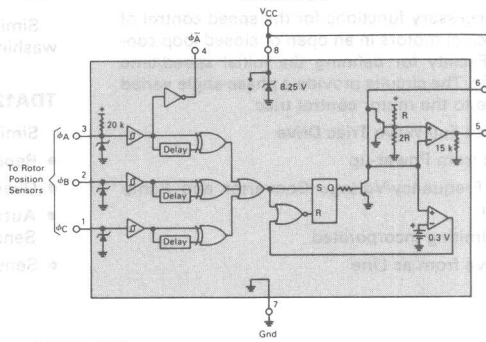


Closed-Loop Brushless Motor Adapter

MC33039P — T_A = −40° to +85°C, Case 626

The MC33039P is a high performance closed-loop speed control adapter specifically designed for use in dc brushless motor control systems. Implementation will allow precise speed regulation without the need for a magnetic or optical tachometer. This device contains three input buffers each with hysteresis for noise immunity, three digital edge detectors, a programmable monostable, and an internal shunt regulator. Also included is an inverter output for use in systems that require conversion of sensor phasing. Although this device is primarily intended for use with the MC33034 brushless motor controller, it can be used cost effectively in many other closed-loop speed control applications.

MC33039



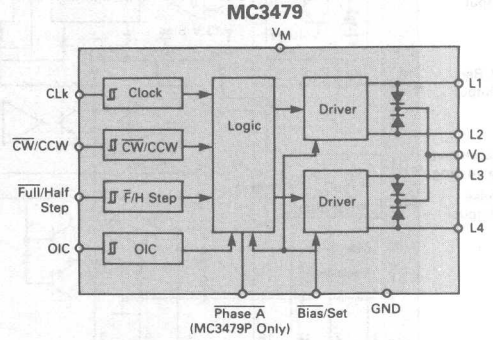
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Stepper Motor Drivers

MC3479P — T_A = 0° to +70°C, Case 648C
SAA1042,A — T_A = 0° to +70°C, Case 721

Stepper Motor Drivers provide up to 500 mA of drive per coil for two phase 6.0 V to 24 V stepper motors. Control logic is provided to accept commands for clockwise, counter clockwise and half or full step operation. MC3479P has added Output Impedance Control (OIC) and Phase A drive state indicator (not available on SAA1042 devices).

MC3479



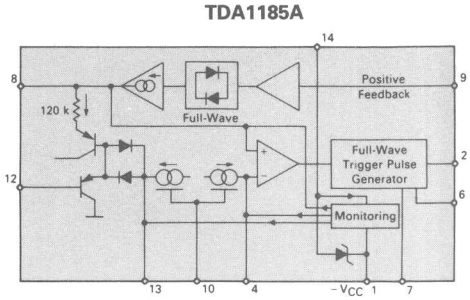
Triac Phase Angle Controller

TDA1185A T_A = 0° to +70°C, Case 646

. . . generates controlled triac triggering pulses and allows tacholess speed stabilization of universal motors by an integrated positive feedback function.

- Low Cost External Components Count
- Optimum Triac Firing (2nd and 3rd Quadrants)
- Repetitive Trigger Pulses When Triac Current is Interrupted by Motor Brush Bounce
- Triac Current Sensed to Allow Inductive Loads
- Soft Start
- Power Failure Detection and General Circuit Reset
- Low Power Consumption: 1.0 mA

TDA1185A



. . . all the necessary functions for the speed control of universal (ac/dc) motors in an open or closed loop configuration. Facility for defining the initial speed/time characteristic. The circuits provide a phase angle varied trigger pulse to the motor control triac

- Guaranteed Full Wave Triac Drive
- Soft Start from Power-up
- On-Chip Frequency/Voltage Converter and Ramp Generator
- Current Limiting Incorporated
- Direct Drive from ac Line

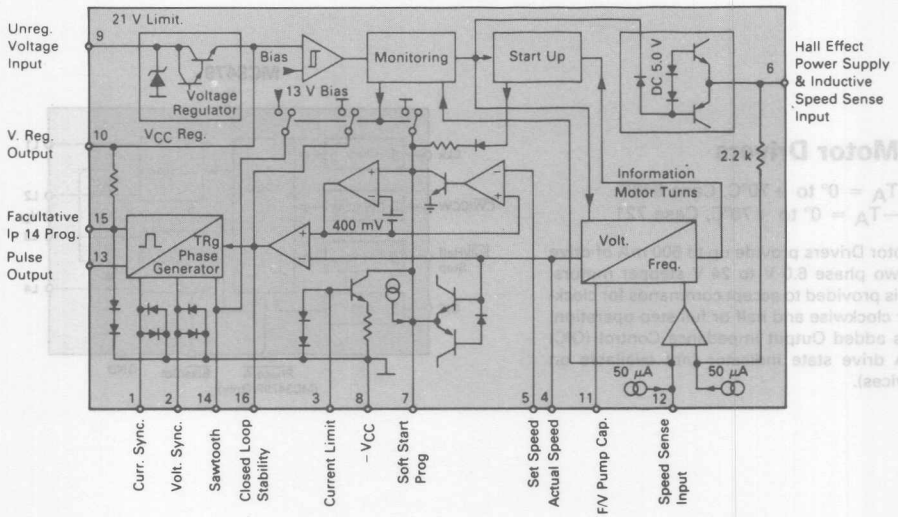
Similar to TDA1085A, but designed for commercial washing machine service.

TDA1285A T_A = 0° to +70°C, Case 648

Similar to TDA1085A, plus:

- Repeated Trigger Pulse if Triac Fails to Latch
- Over 65 mA Output Pulse Current
- Automatic Adaptation to Inductive or Hall Effect Sensors
- Sensor Circuit Continuity Detection

TDA1285A



POWER CONTROLLERS

Device	Function	Page
CA3059	Zero Voltage Switch	4-8
CA3079	Zero Voltage Switch	4-8
MC3399T	High Side Driver Switch	See Chapter 10
MC3484S2,S4	Integrated Solenoid Driver	See Chapter 10
UAA1016B	Zero Voltage Controller	4-95

MOTOR CONTROLLERS

Device	Function	Page
MC33030	DC Servo Motor Controller/Driver	4-21
MC33034	DC Brushless Motor Controller	4-34
MC33039	Closed Loop Brushless Motor Adapter	4-54
MC3479P	Stepper Motor Driver	4-13
SAA1042,A	Stepper Motor Driver	4-59
TDA1085A	Universal Motor Speed Controller	4-64
TDA1085C	Universal Motor Speed Controller	4-71
TDA1185A	TRIAC Phase Angle Controller	4-81
TDA1285A	Universal Motor Speed Controller	4-88

MOTOROLA

CA3059
CA3079

ZERO VOLTAGE SWITCHES

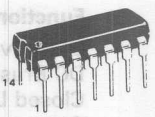
. . . designed for thyristor control in a variety of ac power switching applications for ac input voltages of 24 V, 120 V, 208/230 V, and 277 V @ 50/60 Hz.

Applications:

- Relay Control
- Heater Control
- Valve Control
- Lamp Control
- Synchronous Switching of Flashing Lights
- On-Off Motor Switching
- Differential Comparator With Self-Contained Power Supply for Industrial Applications
- Photosensitive Control
- Power One-Shot Control

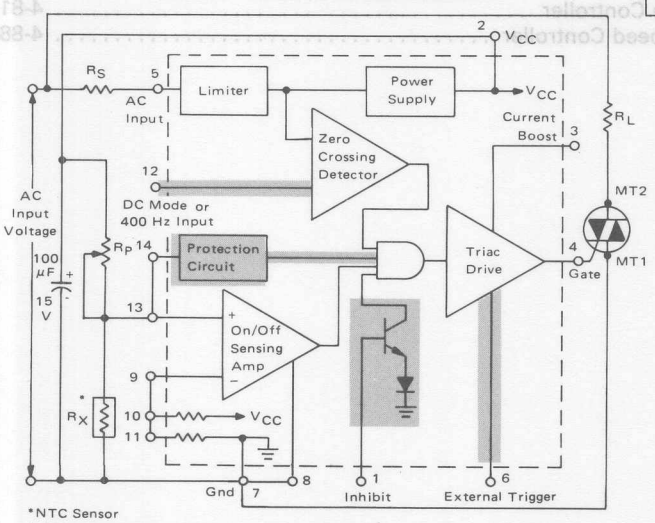
ZERO VOLTAGE SWITCHES

SILICON MONOLITHIC INTEGRATED CIRCUITS



PLASTIC PACKAGE
CASE 646-06

FIGURE 1 – FUNCTIONAL BLOCK DIAGRAM



*NTC Sensor
NOTE: Shaded Area Not Included With CA3079.

TABLE A

AC Input Voltage (50/60 Hz) vac	Input Series Resistor (R_S) kΩ	Dissipation Rating for R_S W
24	2.0	0.5
120	10	2.0
208/230	20	4.0
277	25	5.0

FUNCTIONAL BLOCK DESCRIPTION

1. **Limiter-Power Supply** – Allows operation of the CA3059/79 directly from an ac line. Suggested dropping resistor (R_S) values are given in Table A.
2. **Differential On/Off Sensing Amplifier** – Tests for condition of external sensors or input command signals. Proportional control capability or hysteresis may be implemented using this block.
3. **Zero-Crossing Detector** – Synchronizes the output pulses to the zero voltage point of the ac cycle. This synchronization eliminates RFI when used with resistive loads.
4. **Triac Drive** – Supplies high-current pulses to the external power controlling thyristor.
5. **Protection Circuit (CA3059 only)** – A built-in circuit may be actuated, if the sensor opens or shorts, to remove the drive current from the external triac.
6. **Inhibit Capability (CA3059 only)** – Thyristor firing may be inhibited by the action of an internal diode gate at Pin 1.
7. **High Power DC Comparator Operation (CA3059 only)** – Operation in this mode is accomplished by connecting Pin 7 to Pin 12 (thus overriding the action of the zero-crossing detector). When Pin 13 is positive with respect to Pin 9, current to the thyristor is continuous.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating		Symbol	Value	Unit
DC Supply Voltage (Between Pins 2 and 7)	CA3059	V_{CC}	12	Vdc
	CA3079		10	
DC Supply Voltage (Between Pins 2 and 8)	CA3059	V_{CC}	12	Vdc
	CA3079		10	
Peak Supply Current (Pins 5 and 7)		$I_{5,7}$	±50	mA
Fail-Safe Input Current (Pin 14)		I_{14}	2.0	mA
Output Pulse Current (Pin 4)		I_{out}	150	mA
Junction Temperature		T_J	150	°C
Operating Temperature Range		T_A	-40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (Operation @ 120 Vrms, 50-60 Hz, T_A = 25°C)**

Characteristic	Test Circuits	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	Fig. 2	V_S				Vdc
Inhibit Mode						
R_S = 10 k, I_L = 0			6.1	6.5	7.0	
R_S = 5.0 k, I_L = 2.0 mA			–	6.1	–	
Pulse Mode						
R_S = 10 k, I_L = 0			6.0	6.4	7.0	
R_S = 5.0 k, R_L = 2.0 mA			–	6.2	–	
Gate Trigger Current (V_{GT} = 1.0 V, Pins 3 and 2 connected)	Fig. 3	I_{GT}	–	160	–	mA
Peak Output Current, Pulsed	Fig. 3	I_{OM}				mA
With Internal Power Supply, V_{GT} = 0						
Pin 3 Open			50	125	–	
Pins 3 and 2 Connected			90	190	–	
With External Power Supply, V_{CC} = 12 V, V_{GT} = 0	Fig. 4					
Pin 3 Open			–	230	–	
Pins 3 and 2 Connected			–	300	–	
Inhibit Input Ratio (Ratio of Voltage @ Pin 9 to Pin 2)	Fig. 5	V_9/V_2	0.465	0.485	0.520	–
Total Gate Pulse Duration (C_{Ext} = 0)	Fig. 6					μs
Positive dv/dt		tp	70	100	140	
Negative dv/dt		tn	70	100	140	
Pulse Duration After Zero Crossing (C_{Ext} = 0, R_{Ext} = ∞)	Fig. 6					μs
Positive dv/dt		tp_1	–	50	–	
Negative dv/dt		tn_1	–	60	–	
Output Leakage Current Inhibit Mode***	Fig. 3	I_4	–	0.001	10	μA
Input Bias Current CA3059	Fig. 7	I_{IB}	–	0.15	1.0	μA
Input Bias Current CA3079			–	0.15	2.0	
Common Mode Input Voltage Range (Pins 9 and 13 Connected)	–	V_{CMR}	–	1.4 to 5.0	–	Vdc
Inhibit Input Voltage CA3059 only	Fig. 8	V_1	–	1.4	1.6	Vdc
External Trigger Voltage CA3059 only	–	V_6-V_4	–	1.4	–	Vdc

*Care must be taken, especially when using an external power supply, that total package dissipation is not exceeded.

**The values given in the Electrical Characteristics Chart at 120 V also apply for operation at input voltages of 24 V, 208/230 V, and 277 V, except for Pulse Duration test. However, the series resistor (R_S) must have the indicated value, shown in Table A for the specified input voltage.

***I_4 out of Pin 4
2 V on Pin 1
S1 position 2

TEST CIRCUITS

(All resistor values are in ohms)

FIGURE 2 – DC SUPPLY VOLTAGE

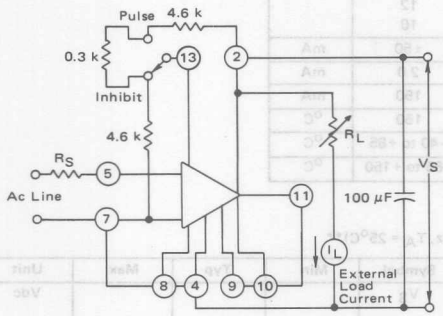


FIGURE 3 – PEAK OUTPUT (PULSED) AND GATE TRIGGER CURRENT WITH INTERNAL POWER SUPPLY

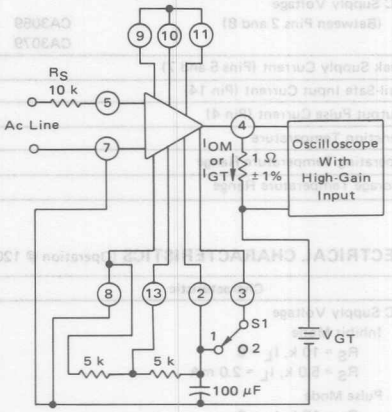


FIGURE 4 – PEAK OUTPUT CURRENT (PULSED) WITH EXTERNAL POWER SUPPLY

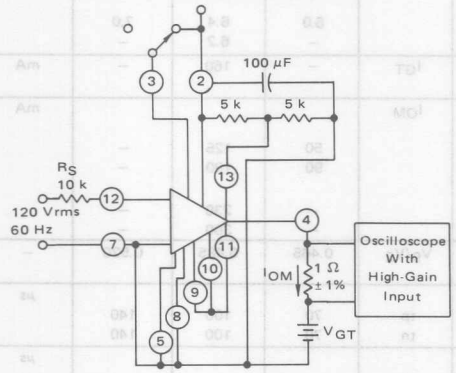


FIGURE 5 – INPUT INHIBIT RATIO

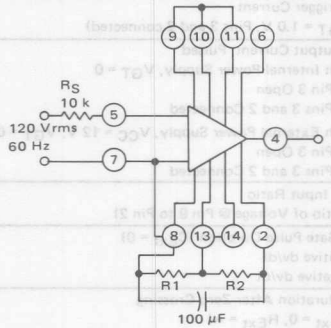


FIGURE 6 – GATE PULSE DURATION TEST CIRCUIT WITH ASSOCIATED WAVEFORM

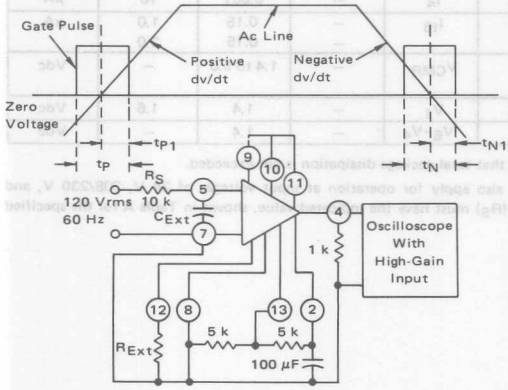
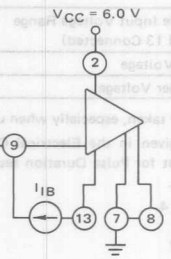


FIGURE 7 – INPUT BIAS CURRENT TEST CIRCUIT



TYPICAL CHARACTERISTICS

FIGURE 8 – INHIBIT INPUT VOLTAGE TEST

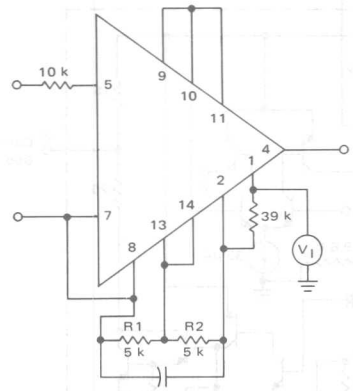


FIGURE 9 – PEAK OUTPUT CURRENT (PULSED) versus EXTERNAL POWER SUPPLY VOLTAGE

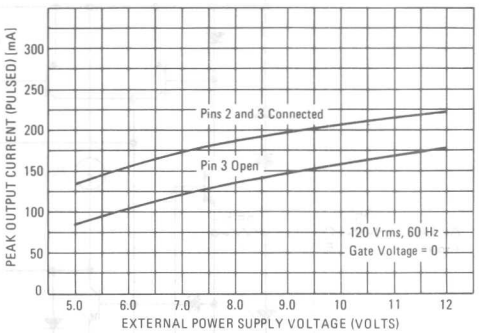


FIGURE 10 – PEAK OUTPUT CURRENT (PULSED) versus AMBIENT TEMPERATURE

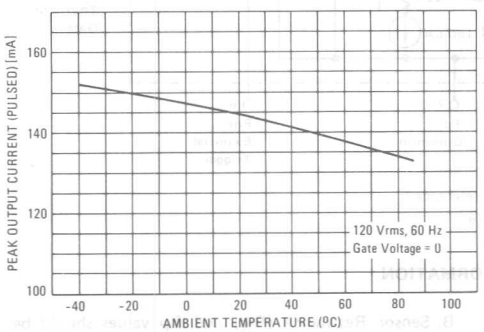


FIGURE 11 – TOTAL PULSE WIDTH versus AMBIENT TEMPERATURE

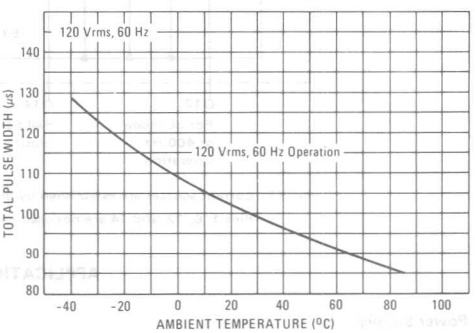


FIGURE 12 – INTERNAL SUPPLY versus AMBIENT TEMPERATURE

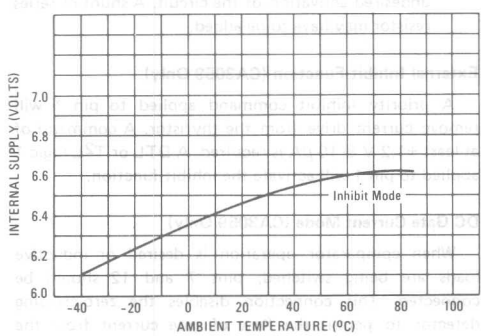


FIGURE 13 – INHIBIT VOLTAGE RATIO versus AMBIENT TEMPERATURE

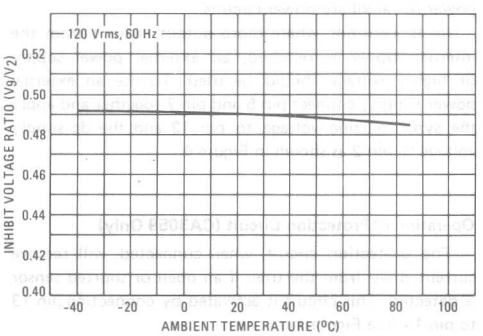
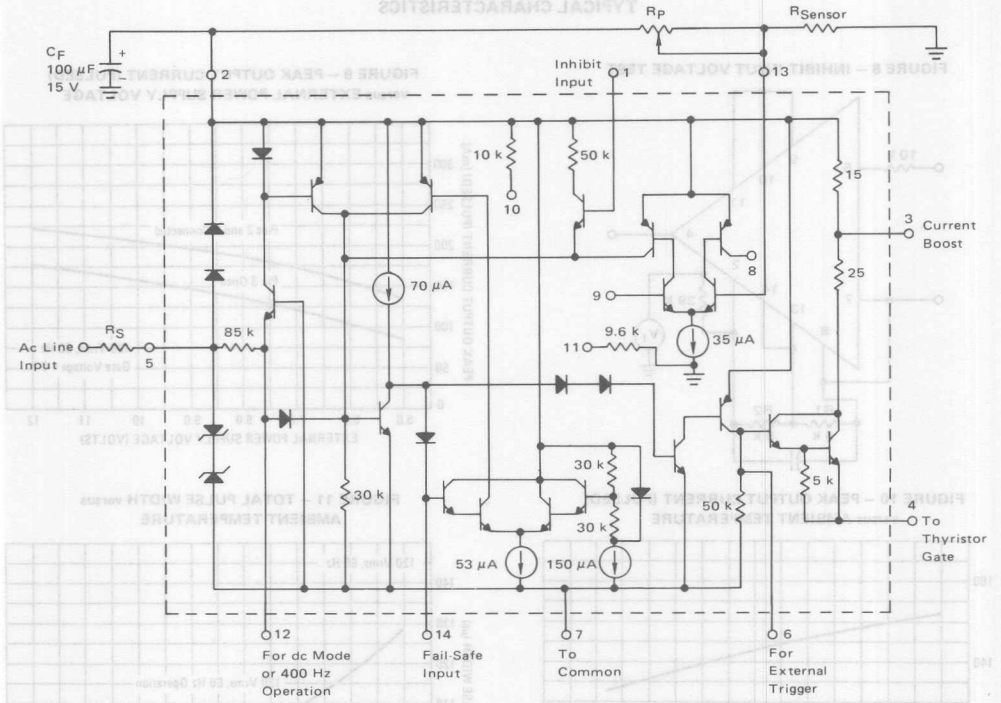


FIGURE 14 – CIRCUIT SCHEMATIC



NOTE: Current sources are established by an internal reference.
Pins 1, 6, 12, and 14 are not used with CA3079.

APPLICATION INFORMATION

Power Supply

The CA3059 and CA3079 are self-powered circuits, powered from the ac line through an appropriate dropping resistor (see Table A). The internal supply is designed to power the auxiliary power circuits.

In applications where more output current from the internal supply is required, an external power supply of higher voltage should be used. To use an external power supply, connect pin 5 and pin 7 together and apply the synchronizing voltage to pin 12 and the dc supply voltage to pin 2 as shown in Figure 4.

Operation of Protection Circuit (CA3059 Only)

The protection circuit, when connected, will remove current drive from the triac if an open or shorted sensor is detected. This circuit is activated by connecting pin 13 to pin 14 (see Figure 1).

The following conditions should be observed when the protection circuit is utilized:

A. The internal supply should be used and the external load current must be limited to 2 mA with a 5 kΩ dropping resistor.

B. Sensor Resistance (R_X) and R_P values should be between 2 kΩ and 100 kΩ.

C. The relationship $0.33 < R_X/R_P < 3$ must be met over the anticipated temperature range to prevent undesired activation of the circuit. A shunt or series resistor may have to be added.

External Inhibit Function (CA3059 Only)

A priority inihibit command applied to pin 1 will remove current drive from the thyristor. A command of at least +1.2 V @ 10 μA is required. A DTL or T^2L logic 1 applied to pin 1 will activate the inhibit function.

DC Gate Current Mode (CA3059 Only)

When comparator operation is desired or inductive loads are being switched, pins 7 and 12 should be connected. This connection disables the zero-crossing detector to permit the flow of gate current from the differential sensing amplifier on demand. Care should be exercised to avoid possible overloading of the internal power supply when operating the device in this mode. A resistor should be inserted between pin 4 and the thyristor gate in order to limit the current.

MOTOROLA

MC3479P

Advance Information

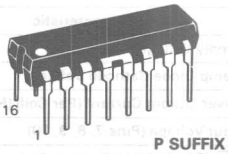
STEPPER MOTOR DRIVER

The MC3479P is designed to drive a two-phase stepper motor in the bipolar mode. The circuit consists of four input sections, a logic decoding/sequencing section, two driver-stages for the motor coils, and an output to indicate the Phase A drive state.

- Single Supply Operation — +7.2 to +16.5 Volts
- 350 mA/Coil Drive Capability
- Clamp Diodes Provided for Back-EMF Suppression
- Selectable $\overline{CW}$/CCW and $\overline{Full}$/Half Step Operation
- Selectable High/Low Output Impedance (Half Step Mode)
- TTL/CMOS Compatible Inputs
- Input Hysteresis — 400 mV Minimum
- Phase Logic Can Be Initialized to $\overline{Phase\ A}$
- $\overline{Phase\ A}$ Output Drive State Indication (Open-Collector)

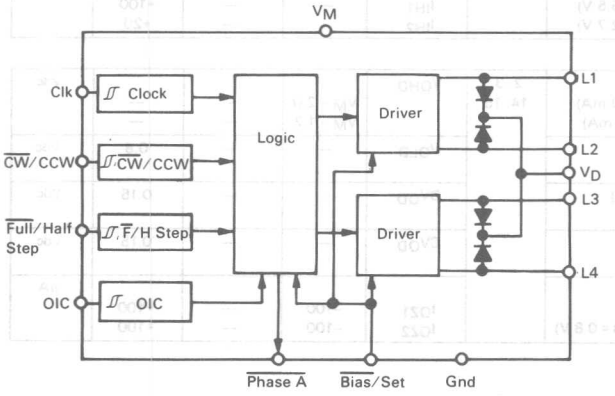
STEPPER MOTOR DRIVER

SILICON MONOLITHIC
INTEGRATED CIRCUIT

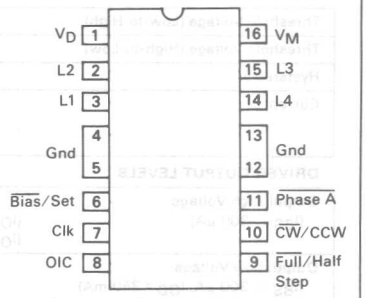


P SUFFIX
PLASTIC PACKAGE
CASE 648C-02

FIGURE 1 — BLOCK DIAGRAM



PIN ASSIGNMENT



INPUT TRUTH TABLE

	Input Low	Input High
$\overline{CW}$/CCW	CW	CCW
$\overline{Full}$/Half Step	Full Step	Half Step
OIC	Hi Z	Low Z
Clk	Positive Edge Triggered	

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Supply Voltage	V_M	+18	Vdc
Clamp Diode Cathode Voltage (Pin 1)	V_D	V_M + 5.0	Vdc
Driver Output Voltage (Pins 2, 3, 14, 15)	V_{OD}	V_M + 6.0	Vdc
Driver Output Current/Coil	I_{OD}	±500	mA
Input Voltage (Pins 7, 8, 9, 10)	V_{in}	−0.5 to +7.0	Vdc
$\overline{\text{Bias}}$/Set Current (Pin 6)	I_{BS}	−10	mA
$\overline{\text{Phase A}}$ Output Voltage (Pin 11)	V_{OA}	+18	Vdc
$\overline{\text{Phase A}}$ Sink Current (Pin 11)	I_{OA}	20	mA
Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Max	Unit
Supply Voltage	V_M	+7.2	+16.5	Vdc
Clamp Diode Cathode Voltage	V_D	V_M	V_M + 4.5	Vdc
Driver Output Current (Per Coil) (Note 5)	I_{OD}	—	350	mA
Input Voltage (Pins 7, 8, 9, 10)	V_{in}	0	+5.5	Vdc
$\overline{\text{Bias}}$/Set Current (Outputs Active)	I_{BS}	−300	−75	μA
$\overline{\text{Phase A}}$ Output Voltage	V_{OA}	—	V_M	Vdc
$\overline{\text{Phase A}}$ Sink Current	I_{OA}	0	8.0	mA
Operating Ambient Temperature	T_A	0	+70	°C

DC ELECTRICAL CHARACTERISTICS

(Specifications apply over the recommended supply voltage and temperature ranges unless otherwise noted.) (See Notes 1, 2)

Characteristic	Pins	Symbol	Min	Typ	Max	Unit
INPUT LOGIC LEVELS						
Threshold Voltage (Low-to-High)	7, 8, 9, 10	V_{TLH}	—	—	2.0	Vdc
Threshold Voltage (High-to-Low)		V_{THL}	0.8	—	—	Vdc
Hysteresis		V_{HYS}	0.4	—	—	Vdc
Current (V_I = 0.4 V)		I_{IL}	−100	—	—	μA
(V_I = 5.5 V)		I_{IH1}	—	—	+100	
(V_I = 2.7 V)		I_{IH2}	—	—	+20	
DRIVER OUTPUT LEVELS						
Output High Voltage (I_{BS} = −300 μA) (I_{OD} = −350 mA)	2, 3, 14, 15	V_{OHD}	V_M − 2.0	—	—	Vdc
(I_{OD} = −0.1 mA)			V_M − 1.2	—	—	
Output Low Voltage (I_{BS} = −300 μA, I_{OD} = 350 mA)		V_{OLD}	—	—	0.8	Vdc
Differential Mode Output Voltage Difference (Note 3) (I_{BS} = −300 μA, I_{OD} = 350 mA)		DV_{OD}	—	—	0.15	Vdc
Common Mode Output Voltage Difference (Note 4) (I_{BS} = −300 μA, I_{OD} = −0.1 mA)		CV_{OD}	—	—	0.15	Vdc
Output Leakage — Hi Z State						μA
($0 \leq V_{OD} \leq V_M$, I_{BS} = −5.0 μA)		I_{OZ1}	−100	—	+100	
($0 \leq V_{OD} \leq V_M$, I_{BS} = −300 μA, Pin 9 = 2.0 V, Pin 8 = 0.8 V)		I_{OZ2}	−100	—	+100	

DC ELECTRICAL CHARACTERISTICS (continued)

(Specifications apply over the recommended supply voltage and temperature ranges unless otherwise noted.) (See Notes 1, 2)

Characteristic	Pins	Symbol	Min	Typ	Max	Unit
CLAMP DIODES						
Forward Voltage (I_D = 350 mA)	1, 2, 3, 14, 15	V_{DF}	—	2.5	3.0	Vdc
Leakage Current (Per Diode) (Pin 1 = 21 V; Pins 2, 3, 14, 15 = 0 V; I_{BS} = 0 μA)		I_{DR}	—	—	100	μA
PHASE A OUTPUT						
Output Low Voltage (I_{OA} = 8.0 mA)	11	V_{OLA}	—	—	0.4	Vdc
Off State Leakage Current (V_{OHA} = 16.5 V)		I_{OHA}	—	—	100	μA
POWER SUPPLY						
Power Supply Current (I_{OD} = 0 μA, I_{BS} = −300 μA)	16					mA
(L1 = V_{OHD}, L2 = V_{OLD}, L3 = V_{OHD}, L4 = V_{OLD})		I_{MW}	—	—	70	
(L1 = V_{OHD}, L2 = V_{OLD}, L3 = Hi Z, L4 = Hi Z)		I_{MZ}	—	—	40	
(L1 = V_{OHD}, L2 = V_{OLD}, L3 = V_{OHD}, L4 = V_{OHD})		I_{MN}	—	—	75	
$\overline{\text{BIAS}}$/SET CURRENT						
To Set $\overline{\text{Phase A}}$	6	I_{BS}	−5.0	—	—	μA

NOTES:
1. Algebraic convention rather than absolute values is used to designate limit values.
2. Current into a pin is designated as positive. Current out of a pin is designated as negative.
3. $DV_{OD} = |V_{OD1,2} - V_{OD3,4}|$ where
   $V_{OD1,2} = (V_{OHD1} - V_{OLD2})$ or $(V_{OHD2} - V_{OLD1})$, and
   $V_{OD3,4} = (V_{OHD3} - V_{OLD4})$ or $(V_{OHD4} - V_{OLD3})$.
4. $CV_{OD} = |V_{OHD1} - V_{OHD2}|$ or $|V_{OHD3} - V_{OHD4}|$.
5. See section on Power Dissipation in Application Information.

PACKAGE THERMAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Thermal Resistance, Junction to Ambient — No Heat Sink	$R_{\theta JA}$	—	45	—	°C/W

AC SWITCHING CHARACTERISTICS (T_A = +25°C, V_M = 12 V) (See Figures 2, 3, 4)

Characteristic	Pins	Symbol	Min	Typ	Max	Unit
Clock Frequency	7	f_{CK}	0	—	50	kHz
Clock Pulse Width — High	7	PW_{CKH}	10	—	—	μs
Clock Pulse Width — Low	7	PW_{CKL}	10	—	—	μs
$\overline{\text{Bias}}$/Set Pulse Width	6	PW_{BS}	10	—	—	μs
Setup Time — $\overline{\text{CW}}$/CCW and $\overline{\text{F}}$/HS	10–7 9–7	t_{su}	5.0	—	—	μs
Hold Time — $\overline{\text{CW}}$/CCW and $\overline{\text{F}}$/HS	10–7 9–7	t_h	10	—	—	μs
Propagation Delay — Clk-to-Driver Output		t_{PCD}	—	8.0	—	μs
Propagation Delay — $\overline{\text{Bias}}$/Set-to-Driver Output		t_{PBSD}	—	1.0	—	μs
Propagation Delay — Clk-to-$\overline{\text{Phase A}}$ Low	7–11	t_{PHLA}	—	12	—	μs
Propagation Delay — Clk-to-$\overline{\text{Phase A}}$ High	7–11	t_{PLHA}	—	5.0	—	μs

FIGURE 2 — AC TEST CIRCUIT

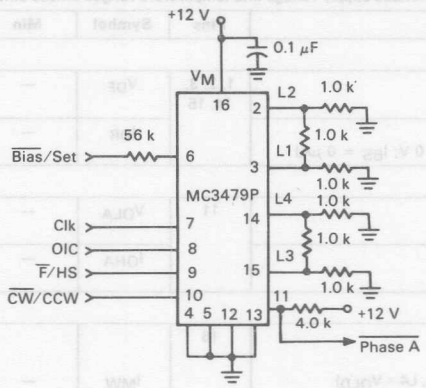
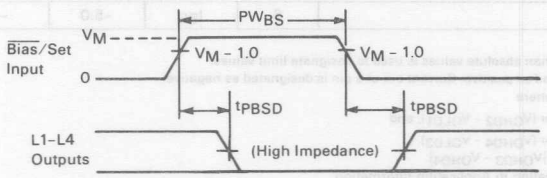


FIGURE 3 — BIAS/SET TIMING (Refer to Figure 2)



Note: t_r, t_f (10%–90%) for input signals are ⩽ 25 ns.

PIN DESCRIPTION

Name	Symbol	Pin #	Description
Power Supply	V_M	16	Power supply pin for both the logic circuit and the motor coil current. Voltage range is +7.2 to +16.5 volts.
Ground	Gnd	4, 5 12, 13	Ground pins for the logic circuit and the motor coil current. The physical configuration of the pins aids in dissipating heat from within the IC package.
Clamp Diode Voltage	V_D	1	This pin is used to protect the outputs where large voltage spikes may occur as the motor coils are switched. Typically a diode is connected between this pin and Pin 16. See Figure 11.
Driver Outputs	L1, L2 L3, L4	2, 3 14, 15	High current outputs for the motor coils. L1 and L2 are connected to one coil, and L3 and L4 to the other coil.
Bias/Set	B/S	6	This pin is typically 0.7 volts below V_M. The current out of this pin (through a resistor to ground) determines the maximum output sink current. If the pin is opened ($I_{BS} < 5.0\ \mu A$) the outputs assume a high impedance condition, while the internal logic presets to a Phase A condition.
Clock	Clk	7	The positive edge of the clock input switches the outputs to the next position. This input has no effect if Pin 6 is open.
Full/Half Step	F/HS	9	When low (Logic "0"), each clock pulse will cause the motor to rotate one full step. When high, each clock pulse will cause the motor to rotate one-half step. See Figure 7 for sequence.
Clockwise/ Counterclockwise	CW/CCW	10	This input allows reversing the rotation of the motor. See Figure 7 for sequence.
Output Impedance Control	OIC	8	This input is relevant only in the half step mode (Pin 9 > 2.0 V). When low (Logic "0") the two driver outputs of the non-energized coil will be in a high impedance condition. When high the same driver outputs will be at a low impedance referenced to V_M. See Figure 7.
Phase A	Ph A	11	This open-collector output indicates (when low) that the driver outputs are in the Phase A condition (L1 = L3 = V_{OHD}, L2 = L4 = V_{OLD}).

FIGURE 4 — CLOCK TIMING (Refer to Figure 2)

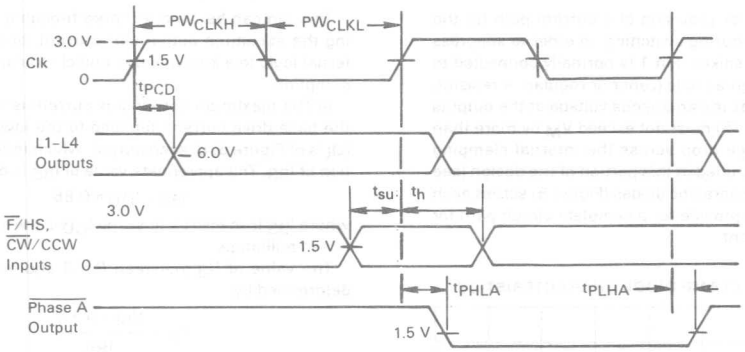
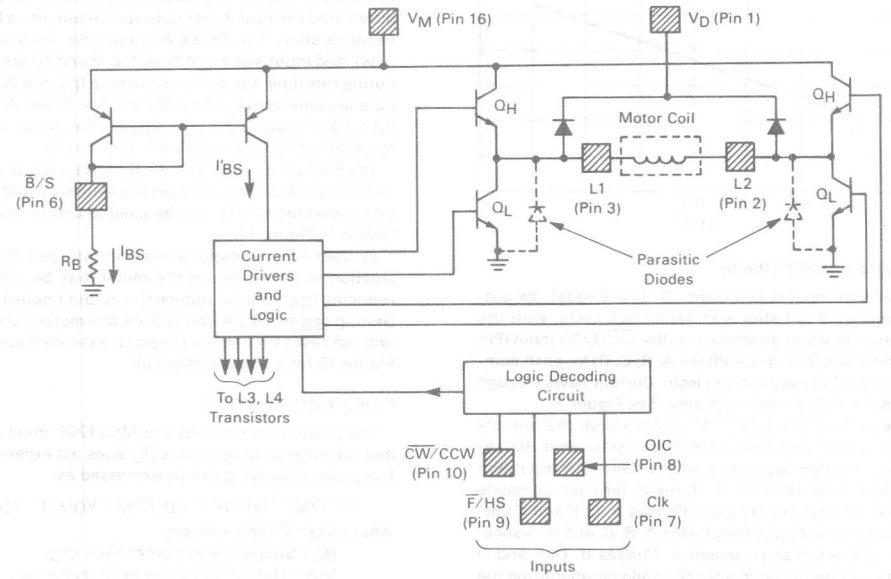


FIGURE 5 — OUTPUT STAGES



APPLICATION INFORMATION

GENERAL

The MC3479P integrated circuit is designed to drive a stepper positioning motor in applications such as disk drives and robotics. The outputs can provide up to 350 mA to each of two coils of a two-phase motor. The outputs change state with each low-to-high transition of the clock input, with the new output state depending on the previous state, as well as the input conditions on Pins 8, 9, and 10.

OUTPUTS (Pins 2, 3, 14, 15)

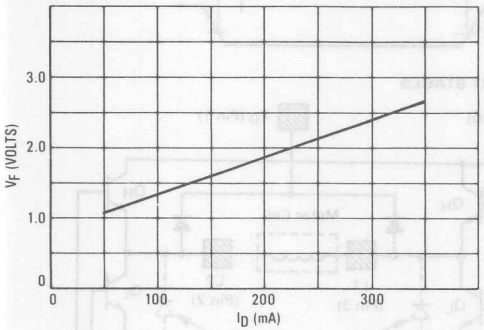
The outputs (L1–L4) are high current outputs (see Figure 5), which when connected to a two-phase motor, provide two full-bridge configurations (L3 and L4 are not shown in Figure 5). The polarities applied to the motor coils depend on which transistor (Q_H or Q_L) of each output is on, which in turn depends on the inputs and the decoding circuitry.

The maximum sink current available at the outputs is a function of the resistor connected between Pin 6 and ground (see section on Bias/Set operation). Whenever the outputs are to be in a high impedance state, both transistors (Q_H and Q_L of Figure 5) of each output are off.

motor coil current during switching, in order to suppress back-EMF voltage spikes. Pin 1 is normally connected to V_M (Pin 16) through a diode (zener or regular), a resistor, or directly. The peak instantaneous voltage at the outputs (Pins 2, 3, 14, and 15) must not exceed V_M by more than 6 volts. The voltage drop across the internal clamping diodes must be included in this portion of the design (see Figure 6). Note the parasitic diodes (Figure 5) across each Q_L of each output provide for a complete circuit path for the switched current.

4

FIGURE 6 — CLAMP DIODE CHARACTERISTICS



$\overline{\text{FULL}}$/HALF STEP (Pin 9)

When this input is at a Logic "0" (<0.8 volts), the outputs change a full step with each clock cycle, with the sequence direction depending on the $\overline{\text{CW}}$/CCW input (Pin 10). There are four steps (Phase A, B, C, D) for each complete cycle of the sequencing logic. Current flows through both motor coils during each step. See Figure 7.

When taken to a Logic "1" (>2.0 volts), the outputs change a half step with each clock cycle, with the sequence direction depending on the $\overline{\text{CW}}$/CCW input (Pin 10). Eight steps (Phases A–H) result for each complete cycle of the sequencing logic. Phases A, C, E and G correspond (in polarity) to the phases A, B, C, and D, respectively, of the full step sequence. Phases B, D, F and H provide current to one motor coil, while de-energizing the other coil. The condition of the outputs of the de-energized coil depends on the OIC input (Pin 8). See Figure 7 for timing diagram.

OIC (Pin 8)

The output impedance control input determines the output impedance to the de-energized coil when operating in the half-step mode. When the outputs are in Phase B, D, F or H (Figure 7) and this input is at a Logic "0" (<0.8 V), the two outputs to the de-energized coil are in a high-impedance condition — Q_L and Q_H of both outputs (Figure 5) are off. When this input is at a Logic "1" (>2.0 V), a low impedance output is provided to the de-energized coil as both outputs have Q_H on (Q_L off). To complete the low impedance path requires connecting Pin 1 (V_D) to Pin 16 (V_M) as described elsewhere in this data sheet.

ing the maximum output sink current; b) setting the internal logic to a known state; and c) reducing power consumption.

a) The maximum output sink current is determined by the base drive current supplied to the lower transistors (Q_L's of Figure 5) of each output, which in turn, is a function of I_{BS}. The appropriate value of I_{BS} is determined by:

$$I_{BS} = I_{OD} \times 0.86$$

where I_{BS} is in microamps, and I_{OD} is the motor current/coil in milliamps.

The value of R_B (between Pin 6 and ground) is then determined by:

$$R_B = \frac{V_M - 0.7\ V}{I_{BS}}$$

b) When Pin 6 is opened (raised to V_M) such that I_{BS} is <5.0 μA, the internal logic is set to the Phase A condition, and the four driver outputs are put into a high impedance state. The $\overline{\text{Phase A}}$ output (Pin 11) goes active (low), and input signals at Pins 7, 8, 9 and 10 are ignored during this time. Upon re-establishing I_{BS}, the driver outputs become active, and will be in the Phase A position (L1 = L3 = V_{OHD}, L2 = L4 = V_{OLD}). The circuit will then respond to the inputs at Pins 7, 8, 9 and 10.

The Set function (opening Pin 6) can be used as a power-up reset while supply voltages are settling. A CMOS logic gate (powered by V_M) can be used to control this pin as shown in Figure 11.

c) Whenever the motor is not being stepped, power dissipation in the IC and in the motor may be lowered by reducing I_{BS}, so as to reduce the output (motor) current. Setting I_{BS} to 75 μA will reduce the motor current, but will not reset the internal logic as described above. See Figure 12 for a suggested circuit.

POWER DISSIPATION

The power dissipated by the MC3479P must be such that the junction temperature (T_J) does not exceed 150°C. The power dissipated can be expressed as:

$$P = (V_M \times I_M) + (2 \times I_{OD})[(V_M - V_{OHD}) + V_{OLD}]$$

where V_M = Supply voltage;
I_M = Supply current other than I_{OD};
I_{OD} = Output current to each motor coil;
V_{OHD} = Driver output high voltage;
V_{OLD} = Driver output low voltage.

The power supply current (I_M) is obtained from Figure 8. After the power dissipation is calculated, the junction temperature can be calculated using:

$$T_J = (P \times R_{\theta JA}) + T_A$$

where $R_{\theta JA}$ = Junction to ambient thermal resistance;
T_A = Ambient temperature.

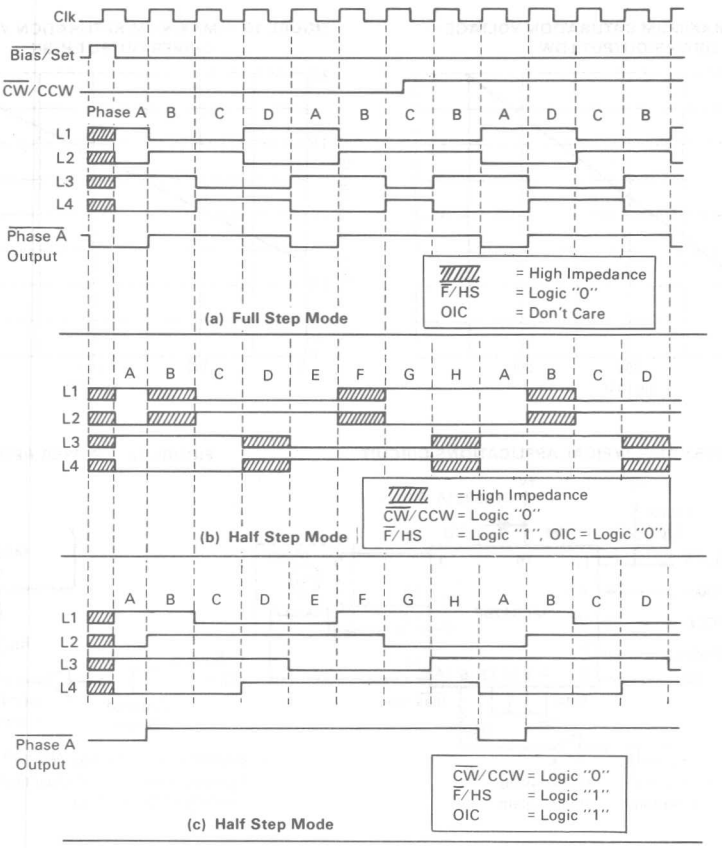
For example, assume an application where V_M = 12 V, the motor requires 200 mA/coil, operating at room temperature with no heat sink on the IC. I_{BS} is calculated:

$$I_{BS} = 200 \times 0.86$$
$$I_{BS} = 172\ \mu A$$

R_B is calculated:

$$R_B = (12 - 0.7)\ V/172\ \mu A$$
$$R_B = 65.7\ k\Omega$$

FIGURE 7 — OUTPUT SEQUENCE



From Figure 8, I_M (max) is determined to be 40 mA. From Figure 9, V_{OLD} is 0.46 volts, and from Figure 10, (V_M - V_{OHD}) is 1.4 volts.

$$P = (12 \times 0.040) + (2 \times 0.2)(1.4 + 0.46)$$
$$P = 1.22\ W$$

$$T_J = (1.22\ W \times 45°C/W) + 25°C$$
$$T_J = 80°C$$

This temperature is well below the maximum limit. If the calculated T_J had been higher than 150°C, a heat sink such as the Staver Co. V-7 series, Aavid #5802, or Thermalloy #6012 could be used to reduce $R_{\theta JA}$. In extreme cases forced air cooling should be considered.

The above calculation, and $R_{\theta JA}$, assumes that a ground plane is provided under the MC3479P (either or both sides of the PC board) to aid in the heat dissipation. Single nominal width traces leading from the four ground pins should be avoided as this will increase T_J, as well as provide potentially disruptive ground noise and I_R drops when switching the motor current.

FIGURE 8 — POWER SUPPLY CURRENT

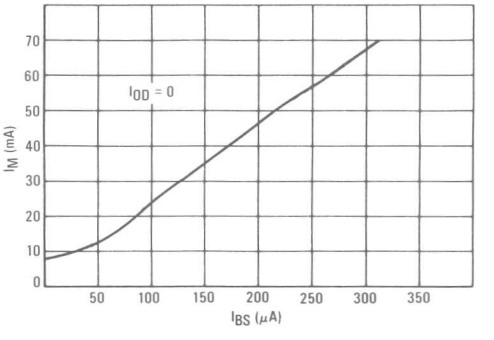


FIGURE 9 — MAXIMUM SATURATION VOLTAGE — DRIVER OUTPUT LOW

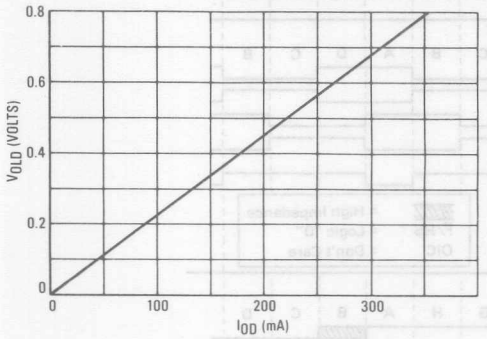


FIGURE 10 — MAXIMUM SATURATION VOLTAGE — DRIVER OUTPUT HIGH

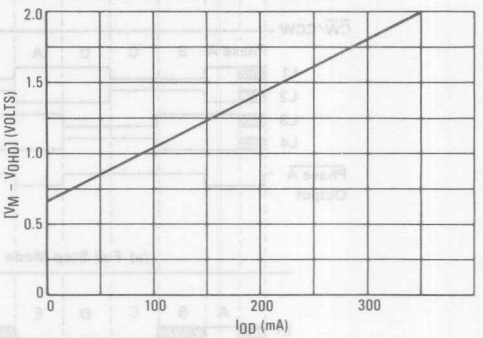


FIGURE 11 — TYPICAL APPLICATIONS CIRCUIT

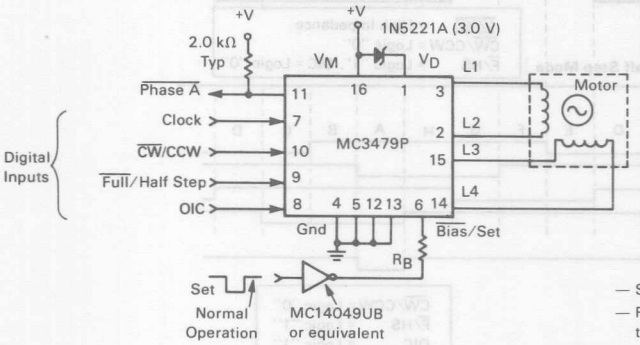
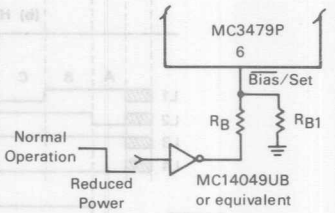


FIGURE 12 — POWER REDUCTION



— Suggested value for R_{B1} (V_M = 12 V) is 150 kΩ.

— R_B calculation (see text) must take into account the current through R_{B1}.

MOTOROLA

MC33030

Advance Information

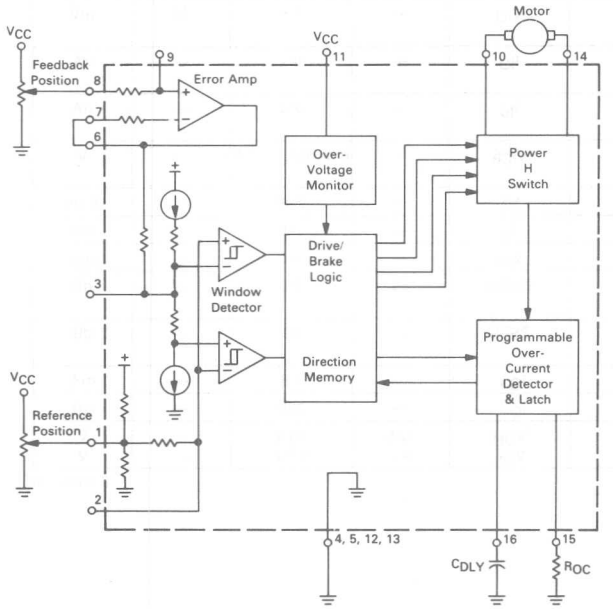
DC SERVO MOTOR CONTROLLER/DRIVER

The MC33030 is a monolithic dc servo motor controller providing all active functions necessary for a complete closed loop system. This device consists of an on-chip op amp and window comparator with wide input common-mode range, drive and brake logic with direction memory, power H switch driver capable of 1.0 A, independently programmable over-current monitor and shutdown delay, and over-voltage monitor. This part is ideally suited for almost any servo positioning application that requires sensing of temperature, pressure, light, magnetic flux, or any other means that can be converted to a voltage.

Although this device is primarily intended for servo applications, it can be used as a switchmode motor controller.

- On-Chip Error Amp for Feedback Monitoring
- Window Detector with Deadband and Self Centering Reference Input
- Drive/Brake Logic with Direction Memory
- 1.0 A Power H Switch
- Programmable Over-Current Detector
- Programmable Over-Current Shutdown Delay
- Over-Voltage Shutdown

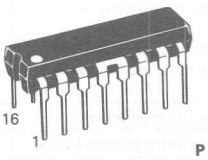
SIMPLIFIED BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

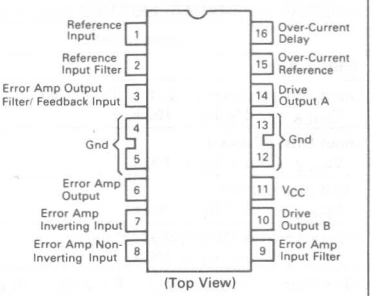
DC SERVO MOTOR CONTROLLER/DRIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 648C-02

PIN CONNECTIONS



(Top View)

Pins 4, 5, 12 and 13 are electrical ground and heat sink pins for IC

ORDERING INFORMATION

Device	Temperature Range	Package
MC33030P	−40°C to +85°C	Plastic DIP

4

Power Supply Voltage	V_{CC}	36	V
Input Voltage Range Op Amp, Comparator, Current Limit. Pins 1, 2, 3, 6, 7, 8, 9, 15.	V_{IR}	−0.3 to V_{CC}	V
Input Differential Voltage Range Op Amp, Comparator. Pins 1, 2, 3, 6, 7, 8, 9.	V_{IDR}	−0.3 to V_{CC}	V
Delay Pin Sink Current (Pin 16)	$I_{DLY(sink)}$	20	mA
Output Source Current (Op Amp)	I_{source}	10	mA
Drive Output Voltage Range (Note 1)	V_{DRV}	−0.3 to (V_{CC} + V_F)	V
Drive Output Source Current (Note 2)	$I_{DRV(source)}$	1.0	A
Drive Output Sink Current (Note 2)	$I_{DRV(sink)}$	1.0	A
Brake Diode Forward Current (Note 2)	I_F	1.0	A
Power Dissipation and Thermal Characteristics Maximum Power Dissipation @ T_A = 70°C Thermal Resistance Junction to Air Thermal Resistance Junction to Case. Pins 4, 5, 12, 13.	 P_D $R_{\theta JA}$ $R_{\theta JC}$	 1000 80 15	 mW °C/W °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

Notes:
1. The upper voltage level is clamped by the forward drop, V_F, of the brake diode.
2. These values are for continuous dc current. Maximum package power dissipation limits must be observed.

ELECTRICAL CHARACTERISTICS (V_{CC} = 14 V, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ERROR AMP					
Input Offset Voltage (−40°C ≤ T_A ≤ +85°C) $V_{Pin\ 6}$ = 7.0 V, R_L = 100 k	V_{IO}	—	1.5	10	mV
Input Offset Current $V_{Pin\ 6}$ = 1.0 V, R_L = 100 k	I_{IO}	—	0.7	—	nA
Input Bias Current $V_{Pin\ 6}$ = 7.0 V, R_L = 100 k	I_{IB}	—	7.0	—	nA
Input Common-Mode Voltage Range ΔV_{IO} = 20 mV, R_L = 100 k	V_{ICR}	—	0 to (V_{CC} − 1.2)	—	V
Slew Rate, Open Loop (V_{ID} = 0.5 V, C_L = 15 pF)	SR	—	0.40	—	V/μs
Unity-Gain Crossover Frequency	f_c	—	550	—	kHz
Unity-Gain Phase Margin	ϕ_m	—	63	—	deg.
Common-Mode Rejection Ratio $V_{Pin\ 6}$ = 7.0 V, R_L = 100 k	CMRR	50	82	—	dB
Power Supply Rejection Ratio V_{CC} = 9.0 to 16 V, $V_{Pin\ 6}$ = 7.0 V, R_L = 100 k	PSRR	—	89	—	dB
Output Source Current ($V_{Pin\ 6}$ = 12 V)	I_{O+}	—	1.8	—	mA
Output Sink Current ($V_{Pin\ 6}$ = 1.0 V)	I_{O-}	—	250	—	μA
Output Voltage Swing (R_L = 17 k to Ground)	V_{OH} V_{OL}	12.5 —	13.1 0.02	— —	V V

(Continued)

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Min	Typ	Max	Unit
WINDOW DETECTOR					
Input Hysteresis Voltage ($V_1 - V_4$, $V_2 - V_3$, Figure 17)	V_H	25	35	45	mV
Input Dead Zone Range ($V_2 - V_4$, Figure 17)	V_{IDZ}	166	210	254	mV
Input Offset Voltage ($\|[V_2 - V_{Pin\ 2}] - [V_{Pin\ 2} - V_4]\|$, Figure 17)	V_{IO}	—	25	—	mV
Input Functional Common-Mode Range (Note 3) Upper Threshold Lower Threshold	 V_{IH} V_{IL}	 — —	 $(V_{CC} - 1.05)$ 0.24	 — —	V
Reference Input Self Centering Voltage Pins 1 and 2 Open	V_{RSC}	—	$(1/2\ V_{CC})$	—	V
Window Detector Propagation Delay Comparator Input, Pin 3, to Drive Outputs V_{ID} = 0.5 V, $R_{L(DRV)}$ = 390 Ω	$t_{p(IN/DRV)}$	—	2.0	—	μs
OVER-CURRENT MONITOR					
Over-Current Reference Resistor Voltage (Pin 15)	R_{OC}	3.9	4.3	4.7	V
Delay Pin Source Current V_{DLY} = 0 V, R_{OC} = 27 k, I_{DRV} = 0 mA	$I_{DLY(source)}$	—	5.5	6.9	μA
Delay Pin Sink Current (R_{OC} = 27 k, I_{DRV} = 0 mA) V_{DLY} = 5.0 V V_{DLY} = 8.3 V V_{DLY} = 14 V	$I_{DLY(sink)}$	 — — —	 0.1 0.7 16.5	 — — —	mA
Delay Pin Voltage, Low State (I_{DLY} = 0 mA)	$V_{OL(DLY)}$	—	0.3	0.4	V
Over-Current Shutdown Threshold V_{CC} = 14 V V_{CC} = 8.0 V	$V_{th(OC)}$	 6.8 5.5	 7.5 6.0	 8.2 6.5	V
Over-Current Shutdown Propagation Delay Delay Capacitor Input, Pin 16, to Drive Outputs V_{ID} = 0.5 V	$t_{p(DLY/DRV)}$	—	1.8	—	μs
POWER H-SWITCH					
Drive-Output Saturation ($-40°C \le T_A \le +85°C$, Note 4) High State (I_{source} = 100 mA) Low State (I_{sink} = 100 mA)	 $V_{OH(DRV)}$ $V_{OL(DRV)}$	 $(V_{CC} - 2)$ —	 $(V_{CC} - 0.85)$ 0.12	 — 1.0	V
Drive-Output Voltage Switching Time (C_L = 15 pF) Rise Time Fall Time	 t_r t_f	 — —	 200 200	 — —	ns
Brake Diode Forward Voltage Drop (I_F = 200 mA, Note 4)	V_F	—	1.04	2.5	V
TOTAL DEVICE					
Standby Supply Current	I_{CC}	—	14	25	mA
Over-Voltage Shutdown Threshold ($-40°C \le T_A \le +85°C$)	$V_{th(OV)}$	16.5	18	20.5	V
Over-Voltage Shutdown Hysteresis (Device off to on)	$V_{H(OV)}$	0.3	0.6	1.0	V
Operating Voltage Lower Threshold ($-40°C \le T_A \le +85°C$)	V_{CC}	—	7.5	8.0	V

NOTES:

3. The upper or lower hysteresis will be lost when operating the Input, Pin 3, close to the respective rail. Refer to Figure 4.
4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperatures as possible.

4

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FIGURE 1 — ERROR AMP INPUT COMMON-MODE VOLTAGE RANGE versus TEMPERATURE

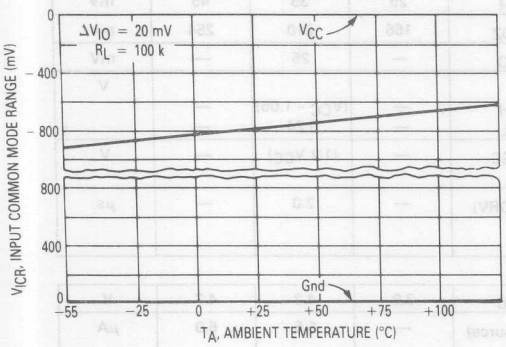


FIGURE 2 — ERROR AMP OUTPUT SATURATION versus LOAD CURRENT

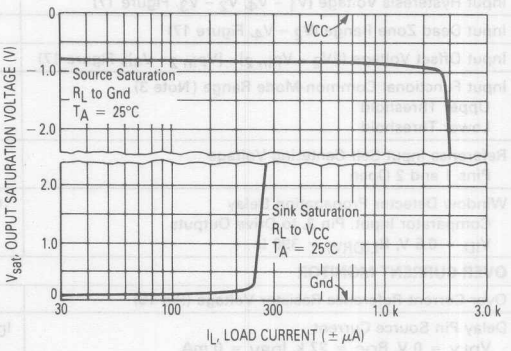


FIGURE 3 — OPEN-LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY

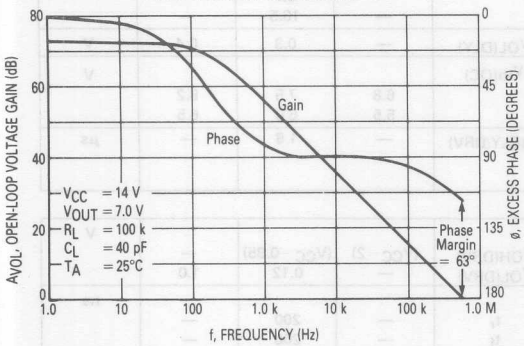


FIGURE 4 — WINDOW DETECTOR REFERENCE-INPUT COMMON-MODE VOLTAGE RANGE versus TEMPERATURE

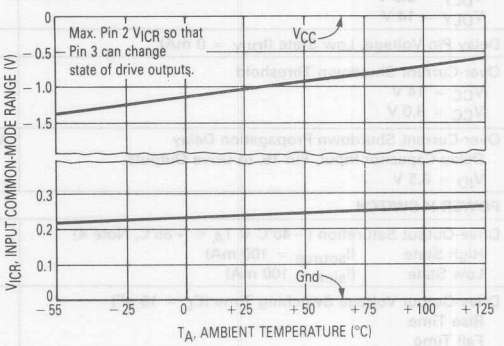


FIGURE 5 — WINDOW DETECTOR FEEDBACK-INPUT THRESHOLDS versus TEMPERATURE

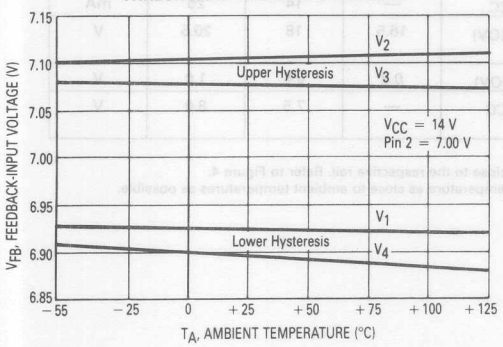


FIGURE 6 — OUTPUT DRIVE SATURATION versus LOAD CURRENT

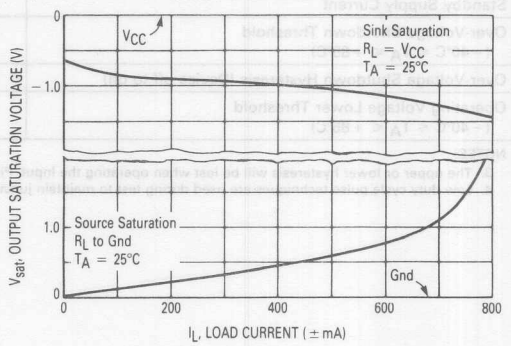


FIGURE 7 — BRAKE DIODE FORWARD CURRENT versus FORWARD VOLTAGE

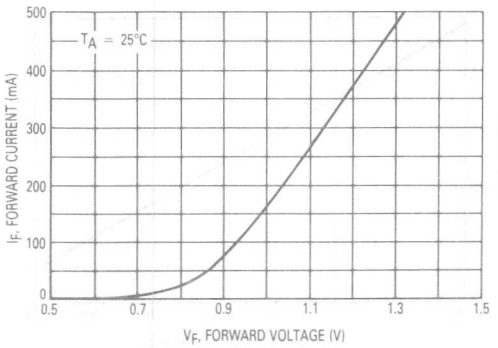


FIGURE 8 — OUTPUT SOURCE CURRENT-LIMIT versus OVER-CURRENT REFERENCE RESISTANCE

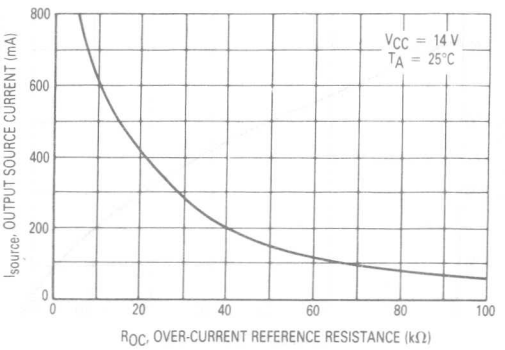


FIGURE 9 — OUTPUT SOURCE CURRENT-LIMIT versus TEMPERATURE

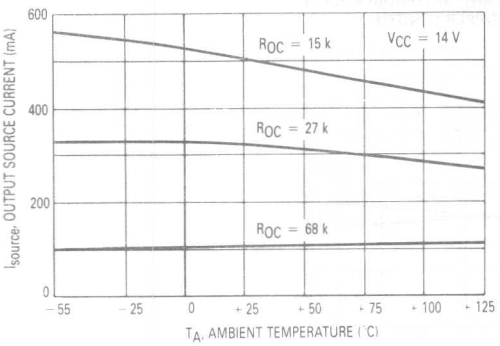


FIGURE 10 — NORMALIZED DELAY PIN SOURCE CURRENT versus TEMPERATURE

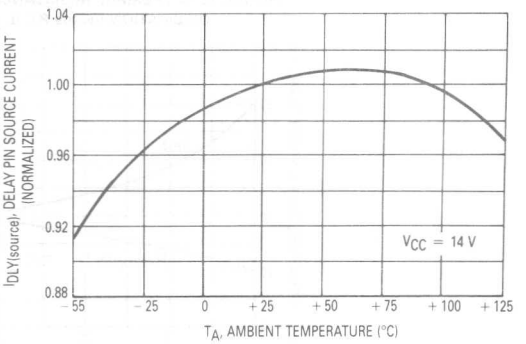


FIGURE 11 — NORMALIZED OVER-CURRENT DELAY THRESHOLD VOLTAGE versus TEMPERATURE

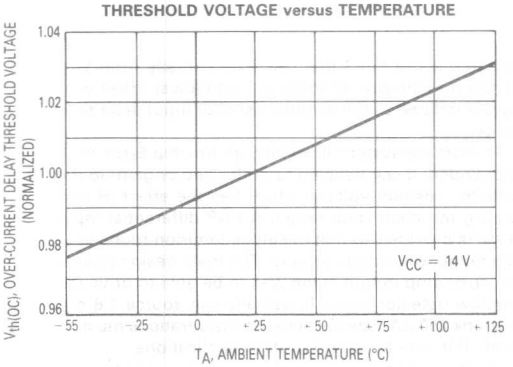
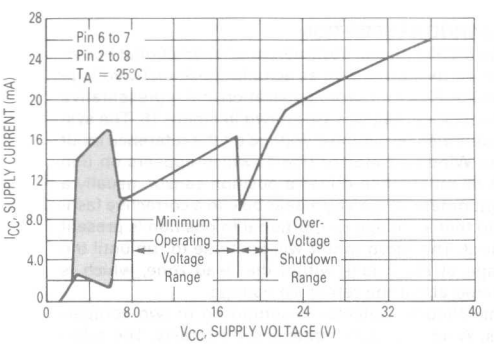


FIGURE 12 — SUPPLY CURRENT versus SUPPLY VOLTAGE



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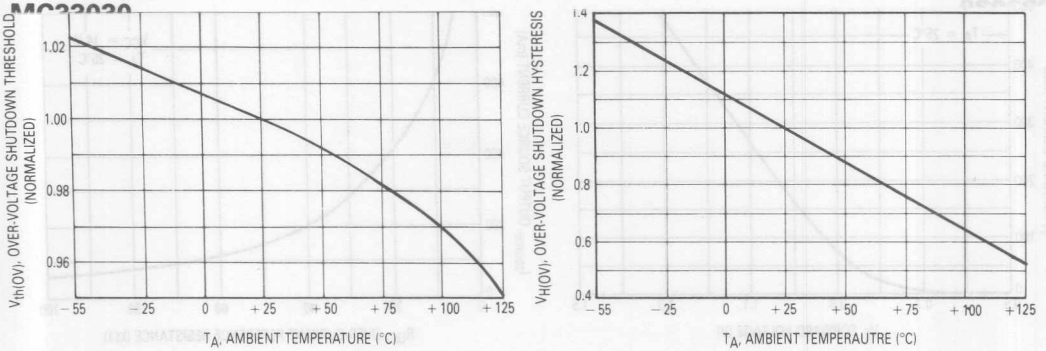
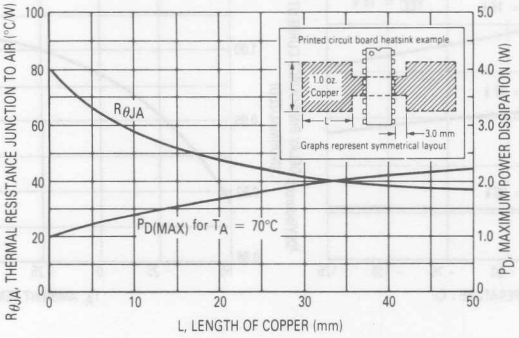


FIGURE 15 — THERMAL RESISTANCE AND MAXIMUM POWER DISSIPATION versus P.C.B. COPPER LENGTH



OPERATING DESCRIPTION

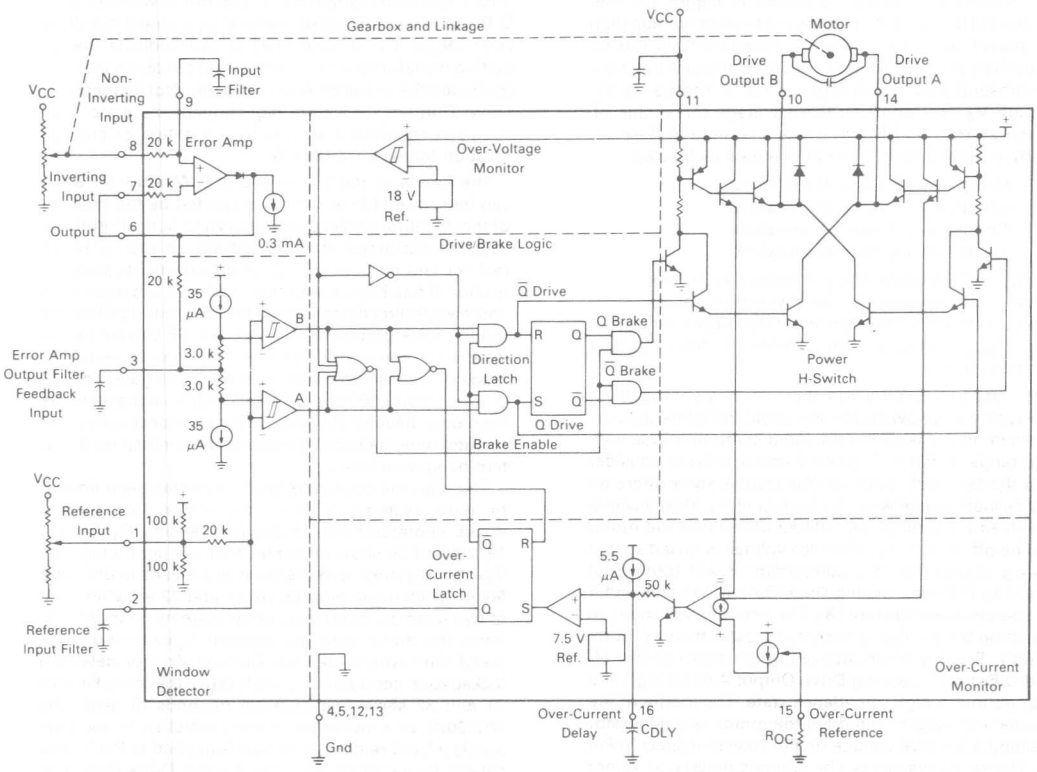
The MC33030 was designed to drive fractional horsepower dc motors and sense actuator position by voltage feedback. A typical servo application and representative internal block diagram are shown in Figure 16. The system operates by setting a voltage on the reference input of the Window Detector (Pin 1) which appears on (Pin 2). A dc motor then drives a position sensor, usually a potentiometer driven by a gear box, in a corrective fashion so that a voltage proportional to position is present at Pin 3. The servo motor will continue to run until the voltage at Pin 3 falls within the dead zone, which is centered about the reference voltage.

The Window Detector is composed of two comparators, A and B, each containing hysteresis. The reference input, common to both comparators, is pre-biased at 1/2 V_{CC} for simple two position servo systems and can easily be overriden by an external voltage divider. The feedback voltage present at Pin 3 is connected to the center of two resistors that are driven by an equal magnitude current source and sink. This generates an offset voltage at the input of each comparator which is centered about Pin 3 that can float virtually from V_{CC} to ground. The sum of the upper and lower offset voltages is defined as the window detector input dead zone range.

To increase system flexibility, an on-chip Error Amp is provided. It can be used to buffer and/or gain-up the actuator position voltage which has the effect of narrowing the dead zone range. A PNP differential input stage is provided so that the input common-mode voltage range will include ground. The main design goal of the error amp output stage was to be able to drive the window detector input. It typically can source 1.8 mA and sink 250 μA. Special design considerations must be made if it is to be used for other applications.

The Power H-Switch provides a direct means for motor drive and braking with a maximum source, sink, and brake current of 1.0 A continuous. Maximum package power dissipation limits must be observed. Refer to Figure 15 for thermal information. For greater drive current requirements, a method for buffering that maintains all the system features is shown in Figure 29.

FIGURE 16 — REPRESENTATIVE BLOCK DIAGRAM AND TYPICAL SERVO APPLICATION



The Over-Current Monitor is designed to distinguish between motor start-up or locked rotor conditions that can occur when the actuator has reached its travel limit. A fraction of the Power H-Switch source current is internally fed into one of the two inverting inputs of the current comparator, while the non-inverting input is driven by a programmable current reference. This reference level is controlled by the resistance value selected for R_{OC}, and must be greater than the required motor run-current with its mechanical load over temperature; refer to Figure 8. During an over-current condition, the comparator will turn off and allow the current source to charge the delay capacitor, C_{DLY}. When C_{DLY} charges to a level of 7.5 V, the set input of the over-current latch will go high, disabling the drive and brake functions of the Power H-Switch. The programmable time delay is determined by the capacitance value-selected for C_{DLY}.

$$t_{DLY} = \frac{V_{ref}\, C_{DLY}}{I_{DLY(source)}} = \frac{7.5\, C_{DLY}}{5.5\ \mu A} = 1.36\, C_{DLY} \text{ in } \mu F$$

This system allows the Power H-Switch to supply motor start-up current for a predetermined amount of time. If the rotor is locked, the system will time-out and shutdown. This feature eliminates the need for servo end-of-travel or limit switches. Care must be taken so as not to select too large of a capacitance value for C_{DLY}. An over-current condition for an excessively long time-out period can cause the integrated circuit to overheat and eventually fail. Again, the maximum package power dissipation limits must be observed. The over-current latch is reset upon power-up or by readjusting $V_{pin\ 2}$ as to cause $V_{pin\ 3}$ to enter or pass through the dead zone. This can be achieved by requesting the motor to reverse direction.

An Over-Voltage Monitor circuit provides protection for the integrated circuit and motor by disabling the Power H-Switch functions if V_{CC} should exceed 18 V. Resumption of normal operation will commence when V_{CC} falls below 17.4 V.

4

A timing diagram that depicts the operation of the Drive/Brake Logic section is shown in Figure 17. The waveforms grouped in [1] show a reference voltage that was preset, appearing on Pin 2, which corresponds to the desired actuator position. The true actuator position is represented by the voltage on Pin 3. The points V_1 through V_4 represent the input voltage thresholds of comparators A and B that cause a change in their respective output state. They are defined as follows:

V_1 = Comparator B turn-off threshold
V_2 = Comparator A turn-on threshold
V_3 = Comparator A turn-off threshold
V_4 = Comparator B turn-on threshold

V_1–V_4 = Comparator B input hysteresis voltage
V_2–V_3 = Comparator A input hysteresis voltage
V_2–V_4 = Window detector input dead zone range
$|(V_2 - V_{pin2}) - (V_{pin2} - V_4)|$ = Window detector input offset voltage

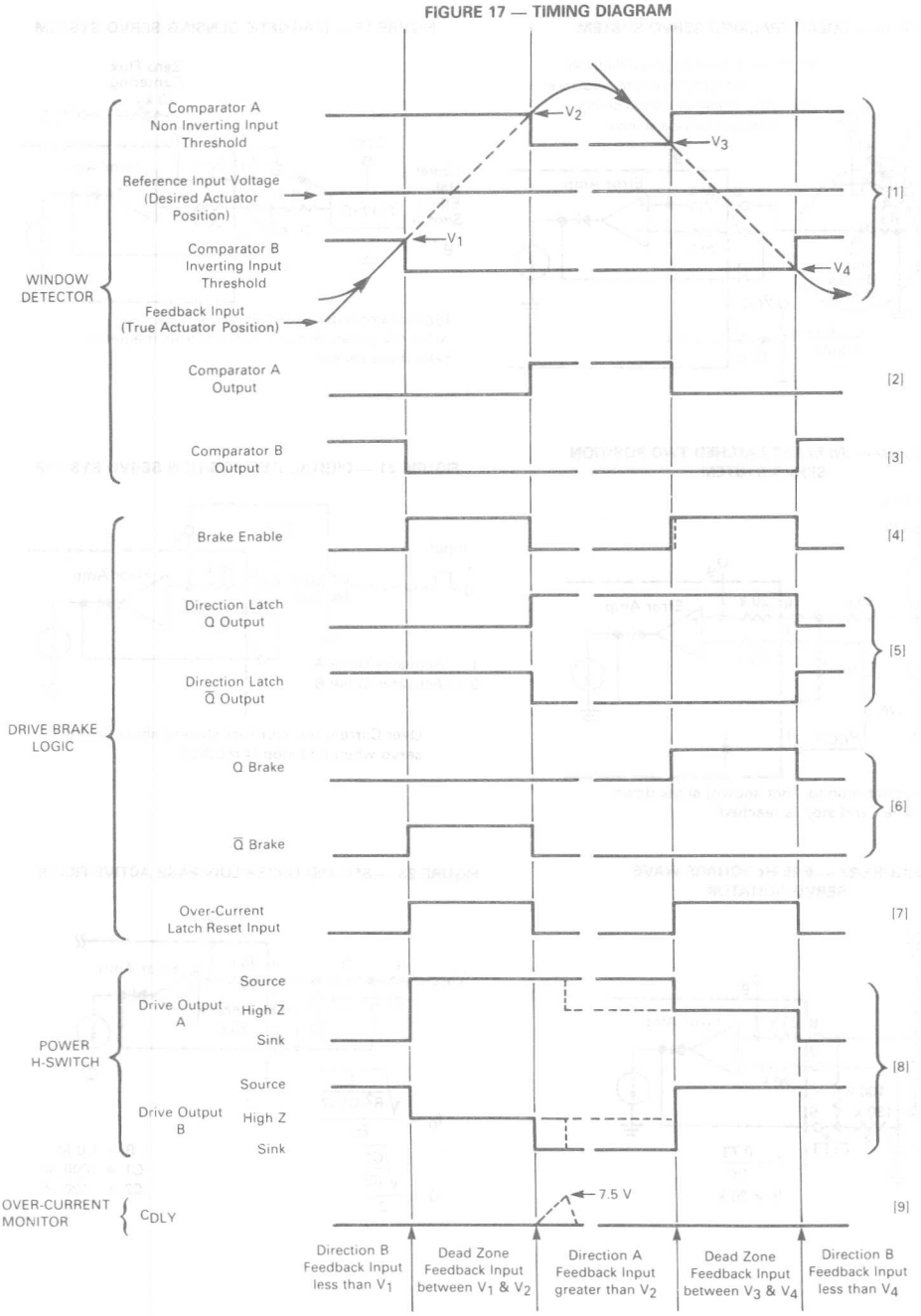
It must be remembered that points V_1 through V_4 always try to follow and center about the reference voltage setting if it is within the input common-mode voltage range of Pin 3; Figures 4 and 5. Initially consider that the feedback input voltage level is somewhere on the dashed line between V_2 and V_4 in [1]. This is within the dead zone range as defined above and the motor will be off. Now if the reference voltage is raised so that $V_{pin\ 3}$ is less than V_4, comparator B will turn-on [3] enabling $\overline{Q}$ Drive, causing Drive Output A to sink and B to source motor current [8]. The actuator will move in Direction B until $V_{pin\ 3}$ becomes greater than V_1. Comparator B will turn-off, activating the brake enable [4] and $\overline{Q}$ Brake [6] causing Drive Output A to go high and B to go into a high impedance state. The inertia of the mechanical system will drive the motor as a generator creating a positive voltage on Pin 10 with respect to Pin 14. The servo system can be stopped quickly, so as not to over-shoot through the dead zone range, by braking. This is accomplished by shorting the motor/generator terminals together. Brake current will flow into the diode at Drive Output B, through the internal V_{CC} rail, and out the emitter of the sourcing transistor at Drive Output A. The end of the solid line and beginning of the dashed for $V_{pin\ 3}$ [1] indicates the possible resting position of the actuator after braking.

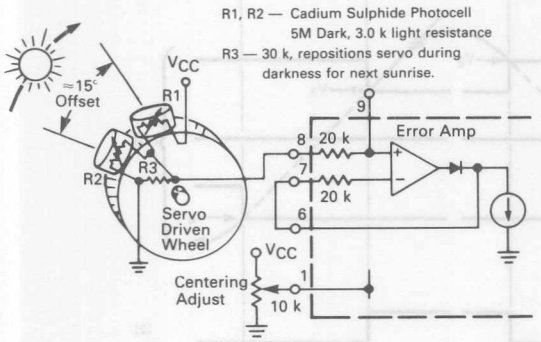
If $V_{pin\ 3}$ should continue to rise and become greater than V_2, the actuator will have over shot the dead zone range and cause the motor to run in Direction A until $V_{pin\ 3}$ is equal to V_3. The Drive/Brake behavior for Direction A is identical to that of B. Overshooting the dead zone range in both directions can cause the servo system to continuously hunt or oscillate. Notice that the last motor run-direction is stored in the direction latch. This information is needed to determine whether Q or $\overline{Q}$ Brake is to be enabled when $V_{pin\ 3}$ enters the dead zone range. The dashed lines in [8,9] indicate the resulting waveforms of an over-current condition that has exceeded the programmed time delay. Notice that both Drive Outputs go into a high impedance state until $V_{pin\ 2}$ is readjusted so that $V_{pin\ 3}$ enters or crosses through the dead zone [7,4].

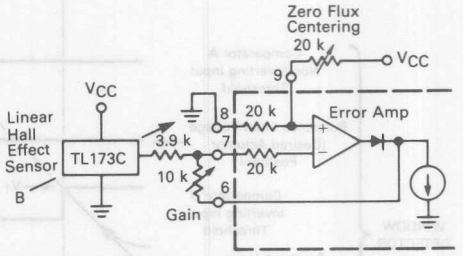
The inputs of the Error Amp and Window Detector can be susceptible to the noise created by the brushes of the dc motor and cause the servo to hunt. Therefore, each of these inputs are provided with an internal series resistor and are pinned out for an external bypass capacitor. It has been found that placing a capacitor with *short leads* directly across the brushes will significantly reduce noise problems. Good quality RF bypass capacitors in the range of 0.001 to 0.1 μF may be required. Many of the more economical motors will generate significant levels of RF energy over a spectrum that extends from dc to beyond 200 MHz. The capacitance value and method of noise filtering must be determined on a system by system basis.

Thus far, the operating description has been limited to servo systems in which the motor mechanically drives a potentiometer for position sensing. Figures 18, 19, 26, and 30 show examples that use light, magnetic flux, temperature, and pressure as a means to drive the feedback element. Figures 20, 21 and 22 are examples of two position, open-loop servo systems. In these systems, the motor runs the actuator to each end of its travel limit where the Over-Current Monitor detects a locked rotor condition and shuts down the drive. Figures 31 and 32 show two possible methods of using the MC33030 as a switching motor controller. In each example a fixed reference voltage is applied to Pin 2. This causes $V_{pin\ 3}$ to be less than V_4 and Drive Output A, Pin 14, to be in a low state saturating the TIP42 transistor. In Figure 31, the motor drives a tachometer that generates an ac voltage proportional to RPM. This voltage is rectified, filtered, divided down by the speed set potentiometer, and applied to Pin 8. The motor will accelerate until $V_{pin\ 3}$ is equal to V_1 at which time Pin 14 will go to a high state and terminate the motor drive. The motor will now coast until $V_{pin\ 3}$ is less than V_4 where upon drive is then reapplied. The system operation of Figure 32 identical to that of 31 except the signal at Pin 3 is an amplified average of the motors drive and back EMF voltages. Both systems exhibit excellent control of RPM with variations of V_{CC}; however, Figure 31 has somewhat better torque characteristics at low RPM.

FIGURE 17 — TIMING DIAGRAM

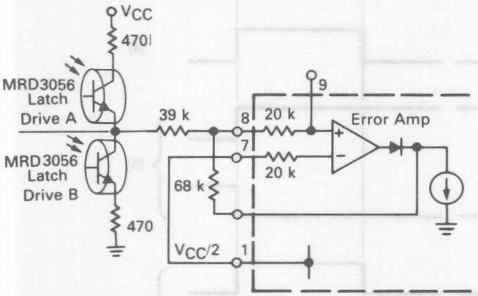






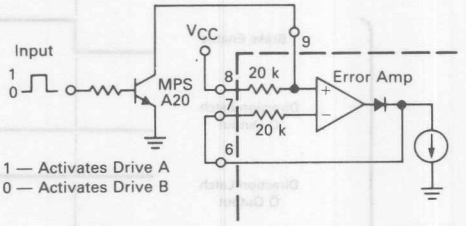
Typical sensitivity with gain set at 3.9 k is 1.5 mV/gauss. Servo motor controls magnetic field about sensor.

FIGURE 20 — INFRARED LATCHED TWO POSITION SERVO SYSTEM



Over-current monitor (not shown) shuts down servo when end stop is reached.

FIGURE 21 — DIGITAL TWO POSITION SERVO SYSTEM



Over-Current monitor (not shown) shuts down servo when end stop is reached.

FIGURE 22 — 0.25 Hz SQUARE-WAVE SERVO AGITATOR

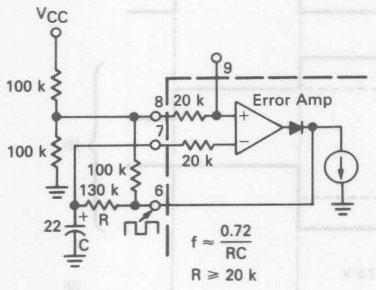


FIGURE 23 — SECOND ORDER LOW-PASS ACTIVE FILTER

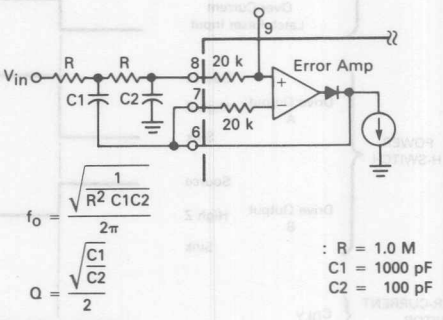
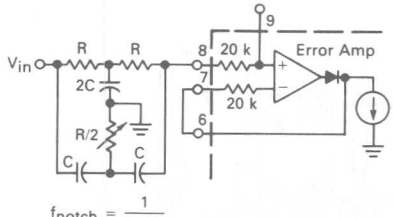


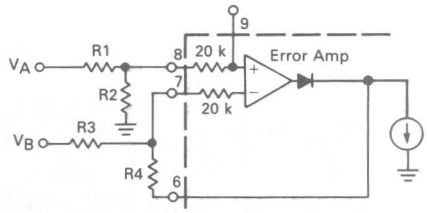
FIGURE 24 — NOTCH FILTER



$$f_{notch} = \frac{1}{2\pi RC}$$

For 60 Hz R = 53.6 k, C = 0.05

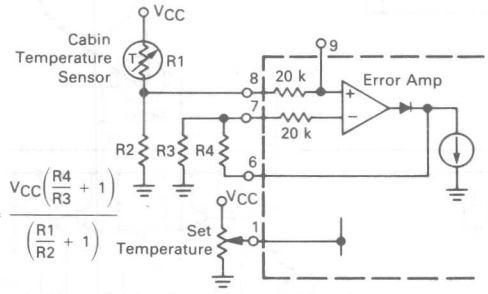
FIGURE 25 — DIFFERENTIAL INPUT AMPLIFIER



$$V_{pin6} = V_A\left(\frac{R3+R4}{R1+R2}\right)\frac{R2}{R3} - \left(\frac{R4}{R3}V_B\right)$$

4

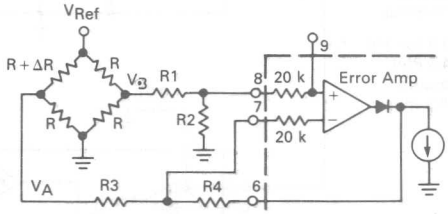
FIGURE 26 — TEMPERATURE SENSING SERVO SYSTEM



$$V_{pin\ 6} = \frac{V_{CC}\left(\frac{R4}{R3}+1\right)}{\left(\frac{R1}{R2}+1\right)}$$

In this application the servo motor drives the heat/air conditioner modulator door in a duct system.

FIGURE 27 — BRIDGE AMPLIFIER

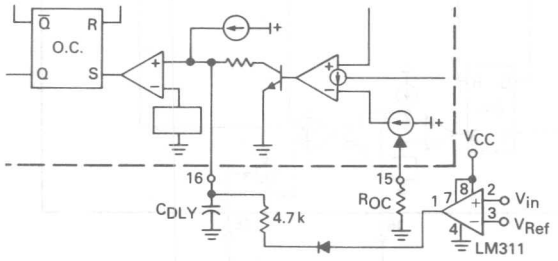


$$V_A - V_B = V_{Ref}\left(\frac{\Delta R}{4R+2\Delta R}\right)$$

R1 = R3, R2 = R4, R1 >>R

$$V_{pin6} = \frac{R4}{R3}(V_A - V_B)$$

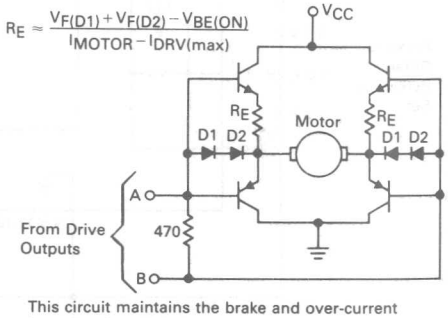
FIGURE 28 — REMOTE LATCHED SHUTDOWN



A direction change signal is required at Pins 2 or 3 to reset the over-current latch.

FIGURE 29 — POWER H-SWITCH BUFFER

$$R_E \approx \frac{V_{F(D1)} + V_{F(D2)} - V_{BE(ON)}}{I_{MOTOR} - I_{DRV(max)}}$$



This circuit maintains the brake and over-current features of the MC33030. Set R_{OC} to 15 k for $I_{DRV(max)} \approx 0.5$ A.

FIGURE 30 — ADJUSTABLE PRESSURE DIFFERENTIAL REGULATOR

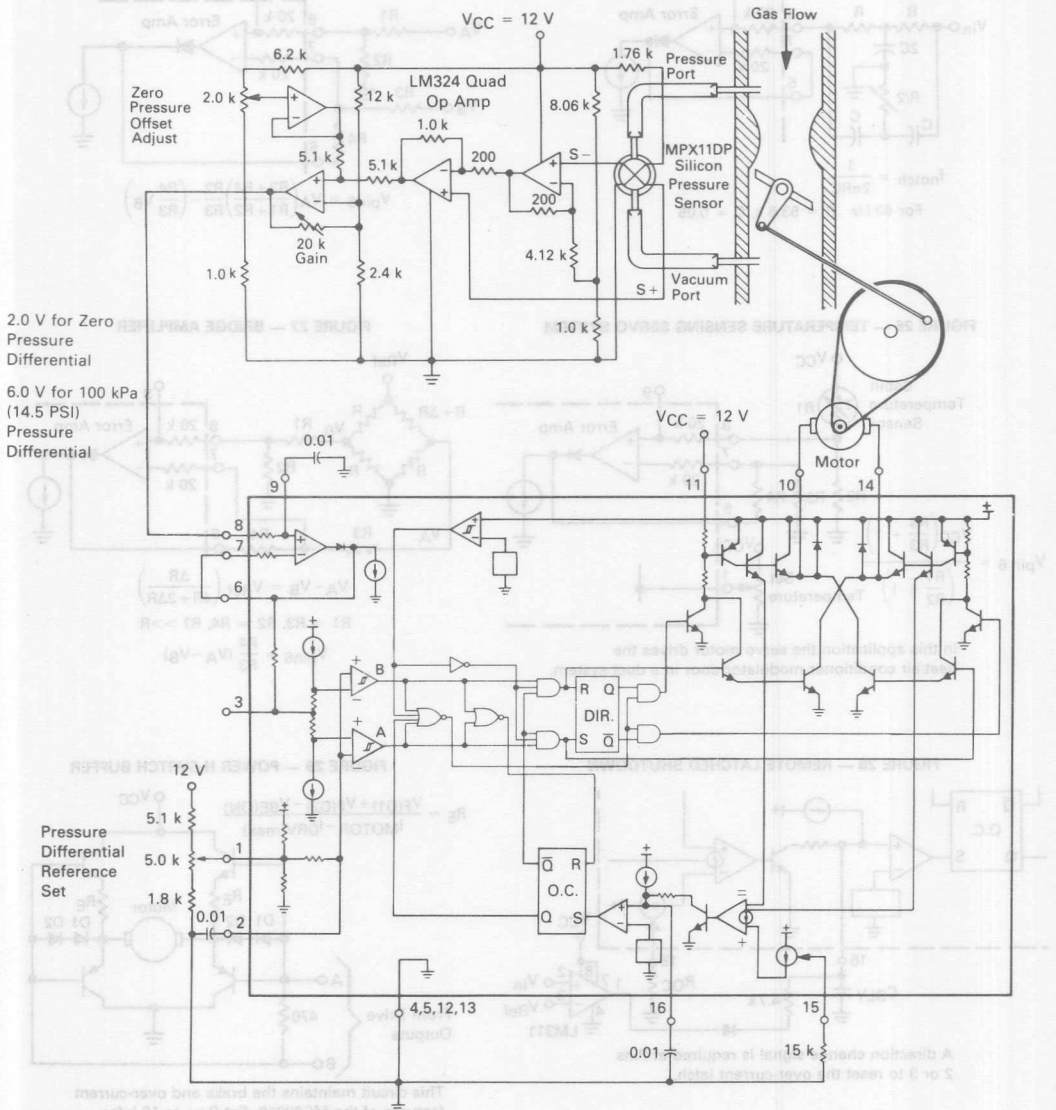


FIGURE 31 — SWITCHING MOTOR CONTROLLER WITH BUFFERED OUTPUT AND TACH FEEDBACK

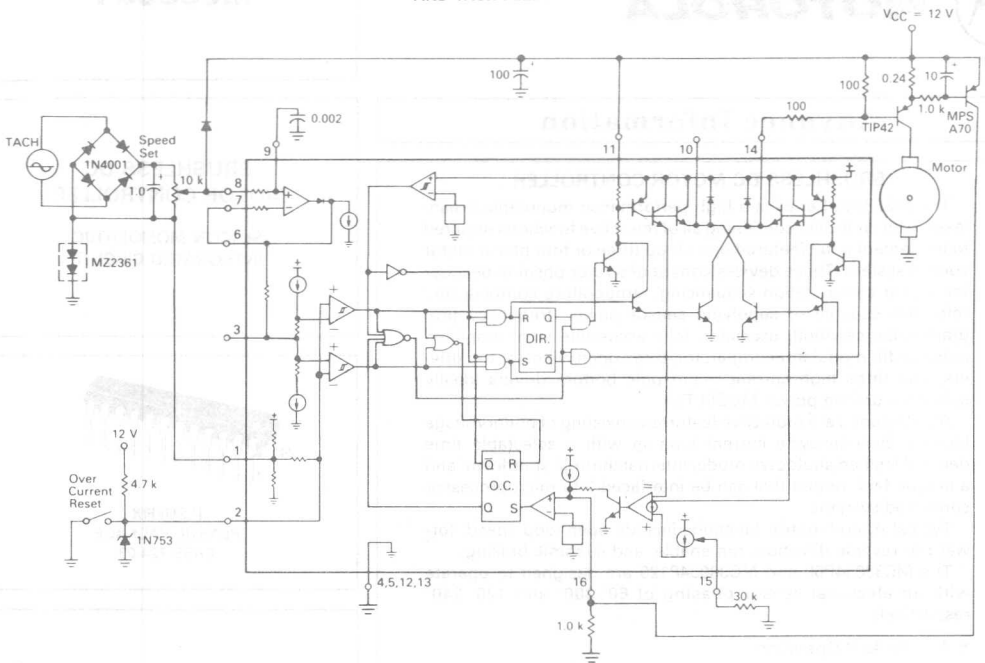
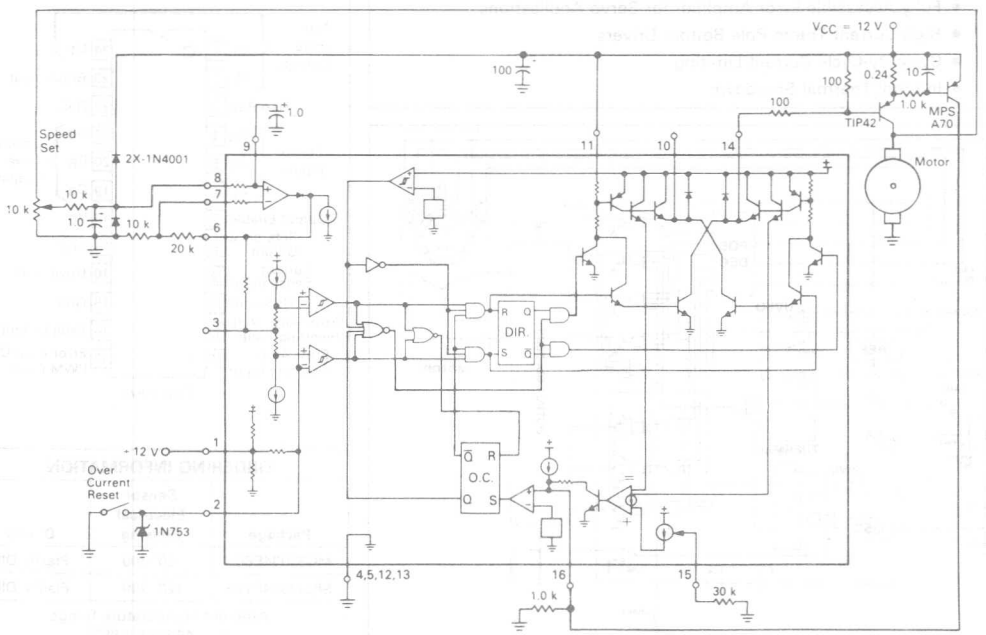


FIGURE 32 — SWITCHING MOTOR CONTROLLER WITH BUFFERED OUTPUT AND BACK EMF SENSING



4

Advance Information

BRUSHLESS DC MOTOR CONTROLLER

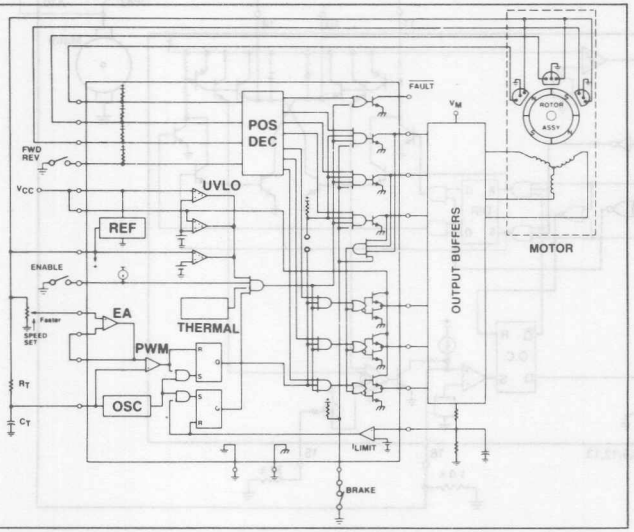
The MC33034 Series is a high performance monolithic brushless motor controller containing all of the active functions required to implement a full featured open-loop three or four phase motor control system. These devices consist of a rotor position decoder for proper commutation sequencing, temperature compensated reference capable of supplying sensor power, frequency programmable sawtooth oscillator, fully accessible error amplifier, pulse width modulator comparator, three open collector top drivers, and three high current totem pole bottom drivers ideally suited for driving power MOSFETs.

Also included are protective features consisting of undervoltage lockout, cycle-by-cycle current limiting with a selectable time delayed latched shutdown mode, internal thermal shutdown, and a unique fault output that can be interfaced into microprocessor controlled systems.

Typical motor control functions include open-loop speed, forward or reverse direction, run enable, and dynamic braking.

The MC33034P60 and MC33034P120 are designed to operate with an electrical sensor phasing of 60°/300° and 120°/240° respectively.

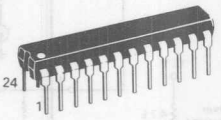
- 10 V to 40 V Operation
- Undervoltage Lockout
- 6.25 V Reference Capable of Supplying Sensor Power
- Fully Accessible Error Amplifier for Servo Applications
- High Current Totem Pole Bottom Drivers
- Cycle-By-Cycle Current Limiting
- Internal Thermal Shutdown



This document contains information on a new product. Specifications and information herein are subject to change without notice.

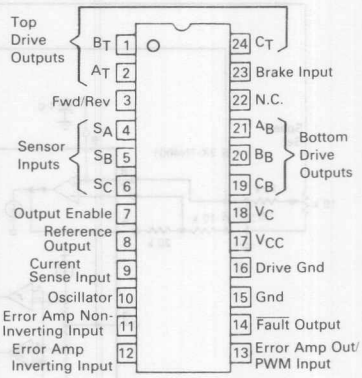
BRUSHLESS DC MOTOR CONTROLLER

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 724-03

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Package	Sensor Electrical Phasing	Device
MC33034P60	60°/300°	Plastic DIP
MC33034P120	120°/240°	Plastic DIP
Ambient Temperature Range = −40°C to +85°C		

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	V
Digital Inputs (Pins 3, 4, 5, 6, 7, 23)	—	V_{ref}	V
Oscillator Input Current (Source or Sink)	I_{OSC}	30	mA
Error Amp Input Voltage Range (Pins 11, 12, Note 1)	V_{IR}	−0.3 to 40	V
Error Amp Output Current, Source or Sink (Note 2)	I_{Out}	10	mA
Current Sense Input Voltage	V_{Sense}	5.0	V
$\overline{\text{Fault}}$ Output Voltage	$V_{CE(\overline{Fault})}$	20	V
$\overline{\text{Fault}}$ Output Sink Current	$I_{Sink(\overline{Fault})}$	20	mA
Top Drive Voltage (Pins 1, 2, 24)	$V_{CE(top)}$	45	V
Top Drive Sink Current (Pins 1, 2, 24)	$I_{Sink(top)}$	50	mA
Bottom Drive Supply Voltage (Pin 18)	V_C	40	V
Bottom Drive Output Current, Source or Sink (Pins 19, 20, 21)	I_{DRV}	100	mA
Power Dissipation and Thermal Characteristics Maximum Power Dissipation @ T_A = 85°C Thermal Resistance Junction to Air	 P_D $R_{\theta JA}$	 867 75	 mW °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} and V_C = 20 V, R_T = 4.7 k, C_T = 10 nF, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Output Voltage (I_{Ref} = 1.0 mA) T_A = 25°C T_A = −40°C to +85°C	V_{ref}	 5.9 5.82	 6.25 —	 6.5 6.57	V
Line Regulation (V_{CC} = 10 V to 40 V, I_{ref} = 1.0 mA)	Reg_{line}	—	12	30	mV
Load Regulation (I_{ref} = 1.0 mA to 20 mA)	Reg_{load}	—	5.0	30	mV
Output Short-Circuit Current (Note 3)	I_{SC}	40	60	—	mA
Reference Under Voltage Lockout Threshold	V_{th}	4.0	4.5	5.0	V
ERROR AMPLIFIER					
Input Offset Voltage (T_A = −40°C to +85°C)	V_{IO}	—	2.0	10	mV
Input Offset Current (T_A = −40 to +85°C)	I_{IO}	—	10	500	nA
Input Bias Current (T_A = −40°C to +85°C)	I_{IB}	—	−25	−1000	nA
Input Common-Mode Voltage Range	V_{ICR}	(0 V to V_{CC} −2.0 V)			V
Open-Loop Voltage Gain (V_O = 3.0 V, R_L = 15 k)	A_{VOL}	75	95	—	dB
Input Common-Mode Rejection Ratio	CMRR	55	80	—	dB
Power Supply Rejection Ratio (V_{CC} and V_C = 10 V to 40 V)	PSRR	65	95	—	dB
Output Voltage Swing High State (R_L = 15 k to Gnd) Low State (R_L = 15 k to V_{ref})	 V_{OH} V_{OL}	 4.6 —	 5.4 0.7	 — 1.0	V

Notes:
1. The input common mode voltage or input signal voltage should not be allowed to go negative by more than 0.3 V. The upper functional limit of the common mode voltage range is typically V_{CC} − 2.0 V, but either or both inputs can go to 40 V, independent of V_{CC} without device destruction.
2. The compliance voltage must not exceed the range of −0.3 V to V_{ref}.
3. Maximum package power dissipation limits must be observed.

ELECTRICAL CHARACTERISTICS (V_{CC} and V_C = 20 V, R_T = 4.7 k, C_T = 10 nF, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR SECTION					
Oscillator Frequency	f_{OSC}	21	23.5	26	kHz
Frequency Change with Voltage (V_{CC} = 10 V to 40 V)	$\Delta f_{OSC}/\Delta V$	—	0.1	5.0	%
Sawtooth Peak Voltage	$V_{OSC(P)}$	—	4.0	4.2	V
Sawtooth Valley Voltage	$V_{OSC(V)}$	1.2	1.5	—	V
LOGIC INPUTS					
Input Threshold Voltage (Pins 3, 4, 5, 6, 7, 23)					V
High State	V_{IH}	2.0	1.4	—	
Low State	V_{IL}	—	1.4	0.8	
Sensor Inputs (Pins 4, 5, 6)					μA
High State Input Current (V_{IH} = 5.0 V)	I_{IH}	−250	−150	−40	
Low State Input Current (V_{IL} = 0 V)	I_{IL}	−900	−600	−300	
Forward/Reverse and Brake Inputs (Pins 3, 23)					μA
High State Input Current (V_{IH} = 5.0 V)	I_{IH}	−150	−88	−25	
Low State Input Current (V_{IL} = 0 V)	I_{IL}	−600	−325	−150	
Output Enable					μA
High State Input Current (V_{IH} = 5.0 V)	I_{IH}	−70	−40	−10	
Low State Input Current (V_{IL} = 0 V)	I_{IL}	−80	−40	−20	
CURRENT-LIMIT COMPARATOR					
Threshold Voltage	V_{th}	75	100	125	mV
Input Bias Current (V_{in} = 0 V to 5.0 V)	I_{IB}	—	−1.0	−2.0	μA
OUTPUTS AND POWER SECTIONS					
Top Drive Output Sink Saturation (I_{sink} = 25 mA)	$V_{CE(sat)}$	—	0.95	1.5	V
Top Drive Output Off-State Leakage (V_{CE} = 40 V)	$I_{DRV(leak)}$	—	2.0	100	μA
Top Drive Output Switching Time (C_L = 47 pF, R_L = 1.0 k)					ns
Rise Time	t_r	—	100	300	
Fall Time	t_f	—	35	300	
Bottom Drive Output Voltage					V
High State (I_{source} = 50 mA)	V_{OH}	(V_C − 3.0)	(V_C − 2.4)	—	
Low State (I_{sink} = 50 mA)	V_{OL}	—	1.5	2.0	
Bottom Drive Output Switching Time (C_L = 1000 pF)					ns
Rise Time	t_r	—	75	200	
Fall Time	t_f	—	65	200	
$\overline{\text{Fault}}$ Output Sink Saturation (I_{sink} = 16 mA)	$V_{CE(sat)}$	—	225	500	mV
$\overline{\text{Fault}}$ Output Off-State Leakage (V_{CE} = 20 V)	$I_{FLT(leak)}$	—	1.0	100	μA
Under Voltage Lockout					V
Drive Outputs Enabled (V_{CC} or V_C Increasing)	$V_{th(on)}$	8.2	9.1	10	
Hysteresis	V_H	0.1	0.2	0.3	
Power Supply Current					mA
V_{CC} and V_C = 20 V					
V_{CC} Current (Pin 17)	I_{CC}	—	16	22	
V_C Current (Pin 18)	I_C	—	3.0	7.0	

FIGURE 1 — OSCILLATOR FREQUENCY versus TIMING RESISTOR

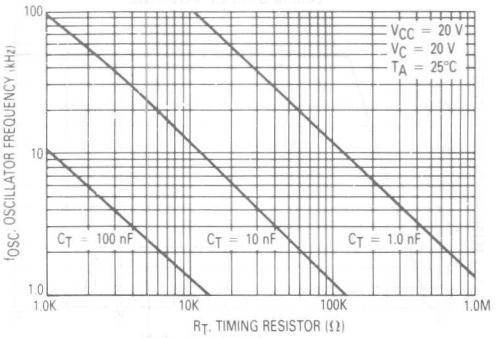
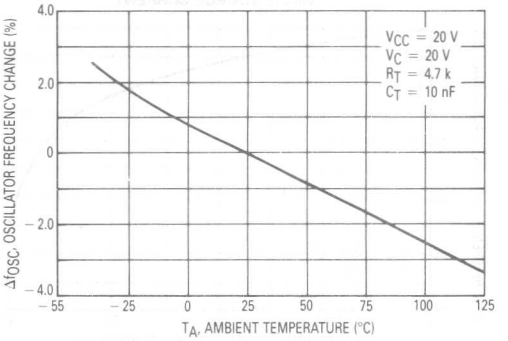


FIGURE 2 — OSCILLATOR FREQUENCY CHANGE versus TEMPERATURE



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FIGURE 3 — ERROR AMP OPEN-LOOP GAIN AND PHASE versus FREQUENCY

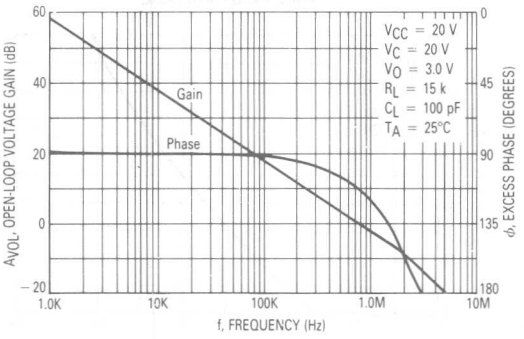


FIGURE 4 — ERROR AMP OUTPUT SATURATION versus LOAD CURRENT

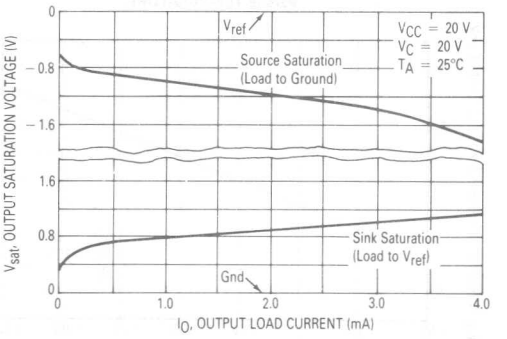


FIGURE 5 — ERROR AMP SMALL-SIGNAL TRANSIENT RESPONSE

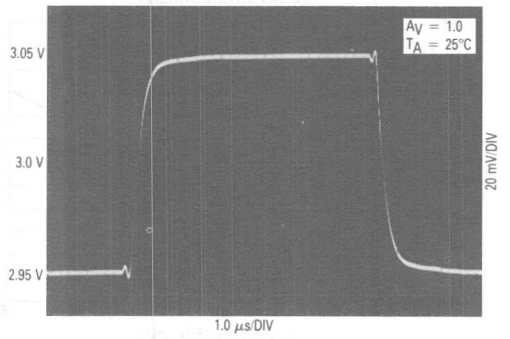
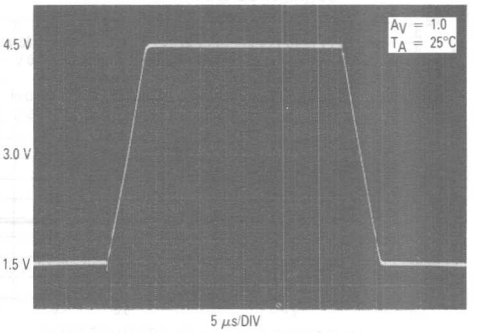


FIGURE 6 — ERROR AMP LARGE-SIGNAL TRANSIENT RESPONSE



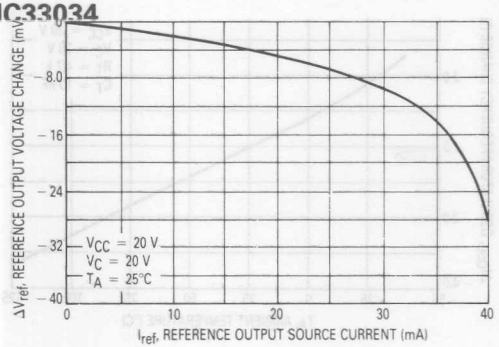


FIGURE 9 — REFERENCE OUTPUT VOLTAGE versus TEMPERATURE

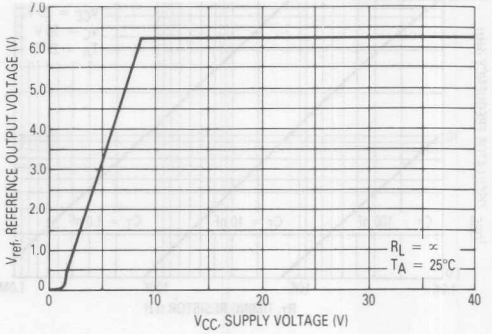


FIGURE 10 — OUTPUT DUTY CYCLE versus PWM INPUT VOLTAGE

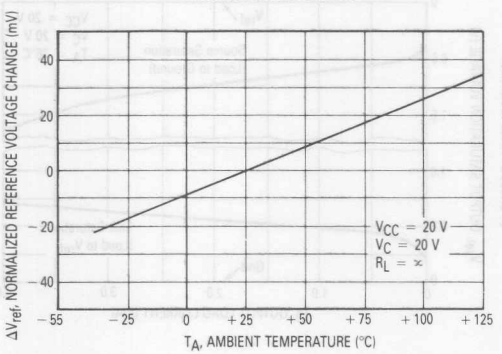


FIGURE 11 — BOTTOM DRIVE RESPONSE TIME versus CURRENT SENSE INPUT VOLTAGE

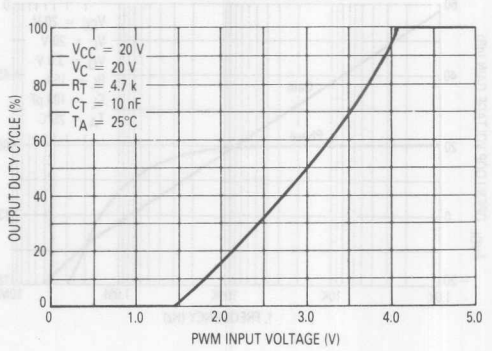
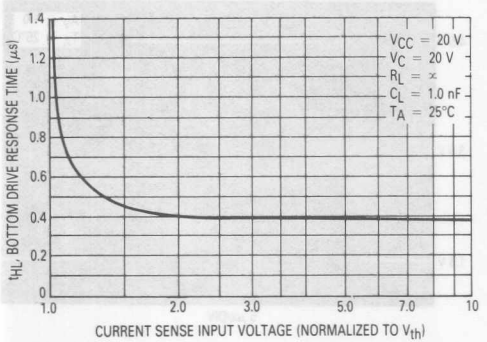


FIGURE 12 — $\overline{\text{FAULT}}$ OUTPUT SATURATION versus SINK CURRENT



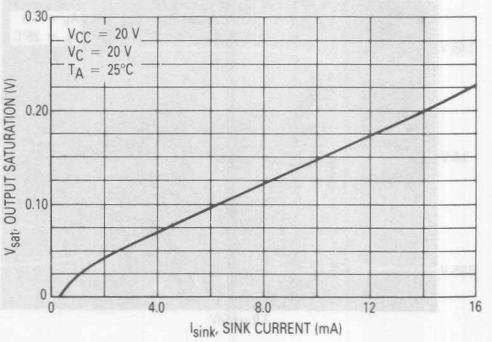


FIGURE 13 — TOP DRIVE OUTPUT SATURATION versus SINK CURRENT

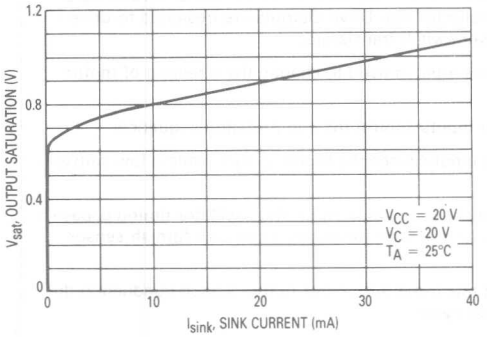


FIGURE 14 — TOP DRIVE OUTPUT WAVEFORM

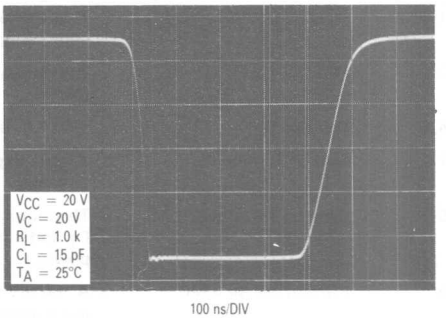


FIGURE 15 — BOTTOM DRIVE OUTPUT WAVEFORM

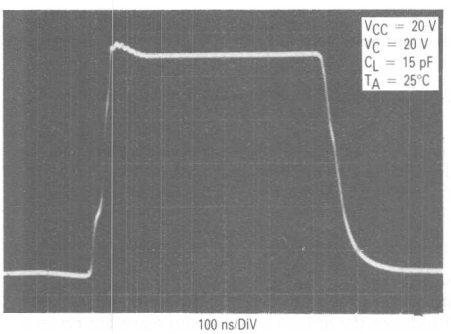


FIGURE 16 — BOTTOM DRIVE OUTPUT WAVEFORM

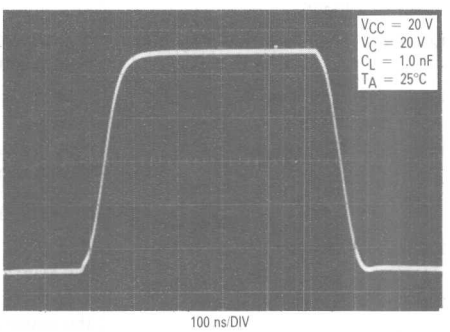


FIGURE 17 — BOTTOM DRIVE OUTPUT SATURATION versus LOAD CURRENT

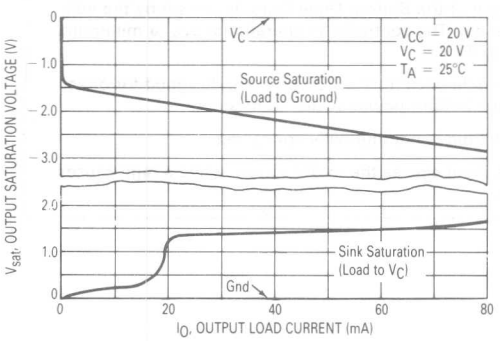
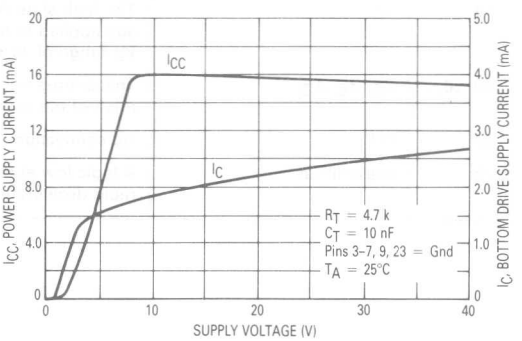


FIGURE 18 — POWER AND BOTTOM DRIVE SUPPLY CURRENT versus SUPPLY VOLTAGE



4

PIN FUNCTION DESCRIPTION

Pin No.	Function	Description
1, 2, 24	B_T, A_T, C_T	These three open collector Top Drive Outputs are designed to drive the external upper power switch transistors.
3	FWD/REV	The Forward/Reverse input is used to change the direction of motor rotation.
4, 5, 6	S_A, S_B, S_C	These three Sensor Inputs control the commutation sequence.
7	Output Enable	A logic high at this input causes the motor to run, while a low causes it to coast.
8	Reference Output	This output provides charging current for the oscillator timing capacitor C_T and a reference for the error amplifier. It can also furnish sensor power.
9	Current Sense Input	A 100 mV signal at this input terminates output switch conduction during a given oscillator cycle.
10	Oscillator	The Oscillator frequency is programmed by the values selected for timing components R_T and C_T.
11	Error Amp Non-Inverting Input	This input is normally connected to the speed set potentiometer.
12	Error Amp Inverting Input	This input is normally connected to the Error Amp Output in open-loop applications.
13	Error Amp Output/PWM Input	This pin is available for compensation in closed-loop applications.
14	$\overline{\text{Fault}}$ Output	This open collector output is active low during one or more of the following conditions: Invalid Sensor Input code, Enable Input at logic 0, Current Sense Input > 100 mV, Undervoltage Lockout activation, and Thermal Shutdown.
15	Ground	This pin is the control circuitry ground return and is connected back to the source ground.
16	Drive Ground	This pin is a separate power ground return that is connected back to the power source. It reduces the effects of switching transient noise on the control circuitry.
17	V_{CC}	This pin is the positive supply of the control IC. The controller is functional over a minimum V_{CC} range of 10 V to 40 V.
18	V_C	The high state (V_{OH}) of the Bottom Drive Outputs are set by the voltage applied to this pin. The controller is operational over a minimum V_C range of 10 V to 40 V.
19, 20, 21	C_B, B_B, A_B	These three totem pole Bottom Drive Outputs are designed for direct drive of the external bottom power switch transistors.
22	N.C.	No connection. This pin is not internally connected.
23	Brake Input	A logic low at this input causes the motor to run, while a high causes rapid deceleration.

INTRODUCTION

The Motorola MC33034 is a high performance monolithic brushless motor controller containing all of the active functions required to implement a full featured, open-loop, three or four phase motor control system. These integrated circuits are constructed with Bipolar Analog technology which offers a high degree of performance and ruggedness in hostile industrial environments. The MC33034 consists of a rotor position decoder for proper commutation sequencing, temperature compensated reference capable of supplying sensor power, frequency programmable sawtooth oscillator, fully accessible error amplifier, pulse width modulator comparator, three open collector top drivers, and three high current totem pole bottom drivers ideally suited for driving power MOSFETs.

Also included are protective features consisting of undervoltage lockout, cycle by cycle current limiting with a selectable time delayed latched shutdown mode, internal thermal shutdown, and a unique $\overline{\text{fault}}$ output that can be interfaced into microprocessor controlled systems.

Typical motor control functions include open-loop speed control, forward or reverse direction, run enable, and dynamic braking.

FUNCTIONAL DESCRIPTION

A representative internal block diagram and a typical system application are shown in Figures 19 and 36. A discussion of the features and function of each of the internal blocks is given below.

Rotor Position Decoder

An internal rotor position decoder monitors the three sensor inputs (Pins 4, 5, 6) to provide the proper sequencing of the top and bottom drive outputs. The sensor inputs are designed to interface directly with open collector type Hall effect switches or opto slotted couplers. Internal pull-up resistors are included to minimize the required number of external components. The inputs are TTL compatible, with the thresholds typically at 1.4 volts. The MC33034 Series consists of two device types, each is designed to control three phase motors and operate with two of the four most common conventions of sensor phasing. The MC33034P60 is intended to operate with an electrical sensor phasing of 60° or 300° and the MC33034P120 with 120° or 240°. With three sensor inputs there are eight possible input code combinations, six of these are valid rotor positions. The remaining two codes are invalid and are usually caused by an open or shorted sensor line. When an invalid input condition exists, the $\overline{\text{fault}}$ output is activated and the drive outputs are disabled. With six valid input codes, the decoder can resolve the rotor position to within a window of 60 electrical degrees.

The forward/reverse input (Pin 3) is used to change the direction of motor rotation by reversing the voltage across the stator winding. When this input changes state, from high to low with a given sensor input code (for example 100), the enabled top and bottom drive outputs with the same alpha designation are exchanged (A_T to A_B, C_B to C_T). In effect the commutation sequence is reversed.

Motor on/off control is accomplished by the output enable (Pin 7). When left disconnected, an internal 40 μA current source enables sequencing of the top and bottom drive outputs. When grounded, the top drive outputs turn off and the bottom drives are forced low, causing the motor to coast and activating the $\overline{\text{fault}}$ output.

Dynamic motor braking allows an additional margin of safety to be designed into the final product. Braking is accomplished by placing the brake input (Pin 23) in a high state. This causes the top drive outputs to turn off and the bottom drives to turn on, shorting the motor-generated back EMF. The brake input has unconditional priority over all other inputs. The internal 20 kΩ pull-up resistor simplifies interfacing with the system safety-switch by ensuring brake activation if opened or disconnected. The commutation truth table is shown in Figure 20. A four input AND gate is used to monitor the brake input and the three top drive outputs. Its purpose is to disable braking until the top drive outputs attain a high state. This helps to avoid simultaneous conduction of the top and bottom power switches. In half wave motor drive applications, the top drive outputs are not required and are typically left disconnected. Under these conditions braking will be disabled by the AND gate. If required, it can be enabled by connecting a single pull-up resistor from V_{CC} to the three open collector outputs. Figure 38 shows a pull-up method utilizing the enable input current source.

Error Amplifier

A high performance, fully compensated error amplifier with access to both inputs and output (Pins 11, 12, 13) is provided to facilitate the implementation of closed-loop motor speed control. The amplifier features a typical DC voltage gain of 95 dB, 800 kHz gain bandwidth, and a wide input common mode voltage range that extends from ground to V_{CC} – 2.0 V. In most open-loop speed control applications, the amplifier is configured as a unity gain voltage follower with the non-inverting input connected to the speed set voltage source. Additional configurations are shown in Figures 31 through 35.

Oscillator

The frequency of the internal ramp oscillator is programmed by the values selected for timing components R_T and C_T. Capacitor C_T is charged from the reference output (Pin 8) through resistor R_T and discharged by an internal transistor. The ramp peak and valley voltages are typically 4.0 V and 1.5 V respectively. To provide a good compromise between audible noise and output switching efficiency, an oscillator frequency in the range of 20 kHz to 30 kHz is recommended. Refer to Figure 1 for component selection.

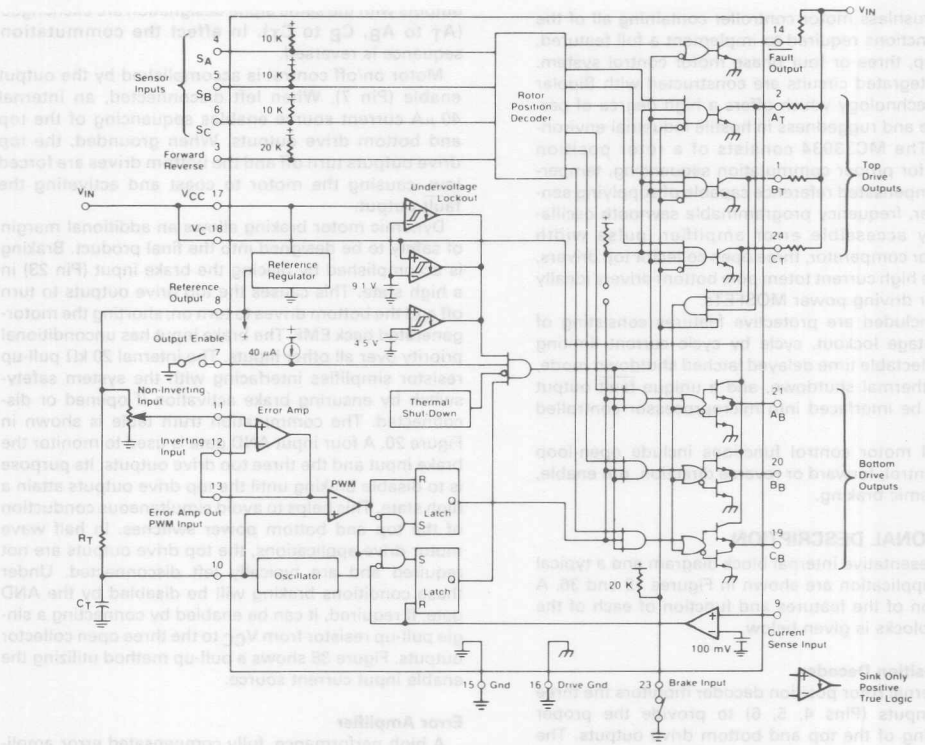


FIGURE 20 — THREE PHASE, SIX STEP COMMUTATION TRUTH TABLE

Inputs (Note 1)										Outputs (Note 2)						
Sensor Electrical Phasing										Top Drives			Bottom Drives			
MC33034P60 60°			MC33034P120 120°													
S_A	S_B	S_C	S_A	S_B	S_C	F/R	Enable	Brake	Current Sense	A_T	B_T	C_T	A_B	B_B	C_B	$\overline{\text{Fault}}$
1	0	0	1	0	0	1	1	0	0	0	1	1	0	0	1	1
1	1	0	1	1	0	1	1	0	0	1	0	1	0	0	1	1
1	1	1	0	1	0	1	1	0	0	1	0	1	1	0	0	1
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0	0	0	1	0	1	0	1	0	0	1	0	1	1	0	0	1
1	0	1	0	0	0	X	X	0	X	1	1	1	0	0	0	0
0	1	0	1	1	1	X	X	0	X	1	1	1	0	0	0	0
X	X	X	X	X	X	X	0	0	X	1	1	1	0	0	0	0
V	V	V	V	V	V	X	1	1	0	1	1	1	1	1	1	1
X	X	X	X	X	X	X	X	1	1	1	1	1	1	1	1	0
X	X	X	X	X	X	X	X	0	1	1	1	1	0	0	0	0

Notes:

1. The digital inputs (Pins 3, 4, 5, 6, 7, 23) are all TTL compatible. The current sense input (Pin 9) has a 100 mV threshold. A logic 0 for this input is defined as < 80 mV, and a logic 1 is > 120 mV.
2. The $\overline{\text{fault}}$ and top drive outputs are open collectors and are active in the low (0) state.
3. V = any one of the six valid sensor combinations.
   X = Don't care.

Pulse Width Modulator

The use of pulse width modulation provides an energy efficient method of controlling the motor speed by varying the average voltage applied to each stator winding during the commutation sequence. As C_T discharges, the oscillator sets both latches, allowing conduction of the top and bottom drive outputs. The PWM comparator resets the upper latch, terminating bottom drive output conduction when the positive-going ramp on C_T becomes greater than the error amplifier output. The pulse width modulator timing diagram is shown in Figure 21. Pulse width modulation for speed control appears only at the bottom drive outputs.

Current Limit

Continuous operation of a motor that is severely overloaded results in overheating and eventual failure. This destructive condition can best be prevented with the use of cycle-by-cycle current limiting. That is, each on-cycle is treated as a separate problem. This is implemented by monitoring the stator current build-up each time the output switch conducts, and upon sensing an over current condition, immediately turns off the switch and holds it off for the duration of the oscillator ramp-up period. The stator current is converted to a voltage by inserting a ground-referenced sense resistor R_S (Figure 36) in series with the three bottom switch transistors (Q4, Q5, Q6). This voltage is monitored by the current sense input (Pin 9), and compared to an internal 100 mV reference. If exceeded, the comparator resets the lower latch and terminates output switch conduction. The value for the sense resistor is:

$$R_S = \frac{0.1}{I_{stator(max)}}$$

The $\overline{\text{fault}}$ output is activated during the over current condition. The dual-latch PWM configuration ensures that only a single output conduction pulse will occur during any given oscillator cycle, whether terminated by the output of the error amp or current limit comparator.

Reference

The on chip 6.25 V regulator (Pin 8) provides charging current for the oscillator timing capacitor, a reference for the error amplifier, and has a current capability of 40 mA for direct power of the sensors in low voltage applications. In higher voltage applications it may become necessary to transfer the power dissipated by the regulator off the I.C. This is easily accomplished with the addition of an external pass transistor as shown in Figure 22. A 6.25 V reference level was chosen to allow implementation of the simpler NPN circuit, where $V_{ref} - V_{BE}$ exceeds the minimum voltage required by Hall effect sensors over temperature. With proper transistor selection, and adequate heatsinking, up to 1.0 amp of load current can be obtained.

FIGURE 22 — REFERENCE OUTPUT BUFFERS

The NPN circuit is recommended for powering Hall or opto sensors, where the output voltage temperature coefficient is not critical. The PNP circuit is slightly more complex, but is also more accurate over temperature. Neither circuit has current limiting.

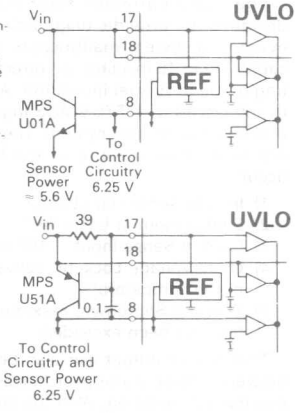
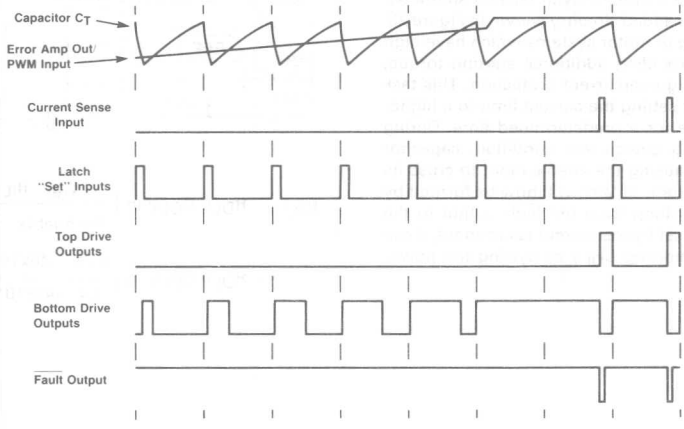


FIGURE 21 — PULSE WIDTH MODULATOR TIMING DIAGRAM



4

Undervoltage Lockout

A triple Undervoltage Lockout has been incorporated to prevent damage to the control IC and the external power switch transistors. Under low power supply conditions, it guarantees that the IC and sensors are fully functional, and that there is sufficient bottom drive output voltage. The positive power supplies to the IC (V_{CC}) and the bottom drives (V_C) are each monitored by separate comparators that have their thresholds at 8.9 V. This level ensures sufficient gate drive for low $r_{DS(on)}$ when interfacing with standard power MOSFETs. When directly powering the Hall sensors from the reference, improper sensor operation can result if the output voltage should fall below 4.5 V. A third comparator is used to detect this condition. If one or more of the comparators detects an undervoltage condition, the $\overline{\text{fault}}$ output is activated, the top drives are turned off and the bottom drive outputs are held in a low state. Each of the comparators contain hysteresis to prevent oscillations when crossing their respective thresholds.

$\overline{\text{Fault}}$ Output

The open collector $\overline{\text{fault}}$ output (Pin 14) was designed to provide diagnostic information in the event of a system malfunction. It has a sink current capability of 16 mA and can directly drive a light emitting diode for visual indication. Additionally, it is easily interfaced with TTL/CMOS logic for use in a microprocessor controlled system. The $\overline{\text{fault}}$ output is active low when one or more of the following conditions occur:

1) Invalid Sensor Input code.
2) Enable Input at Logic "0."
3) Current Sense Input > 100 mV.
4) Undervoltage Lockout, activation of one or more of the comparators.
5) Thermal Shutdown, maximum junction temperature has been exceeded.

This unique output can also be used to distinguish between motor start-up or sustained operation in an overloaded condition. With the addition of an R/C network between the $\overline{\text{fault}}$ output and the enable input, it is possible to create a time-delayed latched shutdown for overcurrent. The added circuitry shown in Figure 23, makes easy starting of motor systems which have high inertial loads by providing additional starting torque, while still preserving overcurrent protection. This task is accomplished by setting the current limit to a higher than nominal value for a predetermined time. During an excessively long overcurrent condition, capacitor C_{DLY} will charge causing the enable input to cross its threshold to a low state. A latch will now be formed by a positive feedback loop from the $\overline{\text{fault}}$ output to the enable input. Once set by the current sense input, it can only be reset by shorting C_{DLY} or cycling the power supply.

Drive Outputs

The three top drive outputs (Pins 1, 2, 24) are open collector NPN transistors capable of sinking 50 milliamps with a minimum breakdown of 45 volts. Interfacing into higher voltage applications is easily accomplished with the circuits shown in Figures 24 and 25.

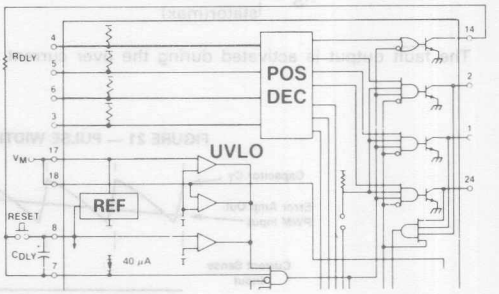
The three totem pole bottom drive outputs (Pins 19, 20, 21) are particularly suited for direct drive of 'N'channel MOSFETs or NPN bipolar transistors (Figures 26, 27 and 28). Each output is capable of sourcing and sinking up to 100 mA. Power for the bottom drives is supplied from V_C (Pin 18). This separate supply input allows the designer added flexibility in tailoring the drive voltage, independent of V_{CC}. A zener clamp is typically connected to this input when driving power MOSFETs in systems where V_{CC} is greater than 20 V.

A separate drive ground (Pin 16) is included to reduce the effects of switching transient noise imposed on the current sense input. This feature becomes particularly useful when driving current sensing power MOSFETs (Figure 29).

Thermal Shutdown

Internal thermal shutdown circuitry is provided to protect the IC in the event that the maximum junction temperature is exceeded. When activated, typically at 170°C, the I.C. acts as though the enable input was grounded.

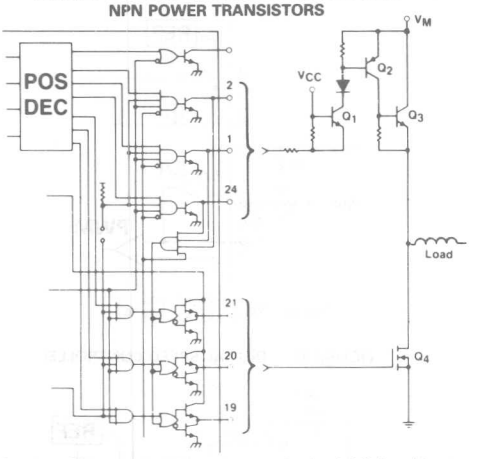
FIGURE 23 — TIMED DELAYED LATCHED OVER-CURRENT SHUTDOWN



$$t_{DLY} \approx R_{DLY}\, C_{DLY}\, \ln\left(\frac{V_{ref} - (I_{IL\ enable}\, R_{DLY})}{V_{th\ enable} - (I_{IL\ enable}\, R_{DLY})}\right)$$

$$\approx R_{DLY}\, C_{DLY}\, \ln\left(\frac{6.25 - (40x10^{-6}\, R_{DLY})}{1.4 - (40x10^{-6}\, R_{DLY})}\right)$$

FIGURE 24 — HIGH VOLTAGE INTERFACE WITH NPN POWER TRANSISTORS



Transistor Q1 is a common base stage used to level shift from V_{CC} to the high motor voltage V_M. The collector diode is required if V_{CC} is present while V_M is low.

FIGURE 25 — HIGH VOLTAGE INTERFACE WITH 'N' CHANNEL POWER MOSFETs

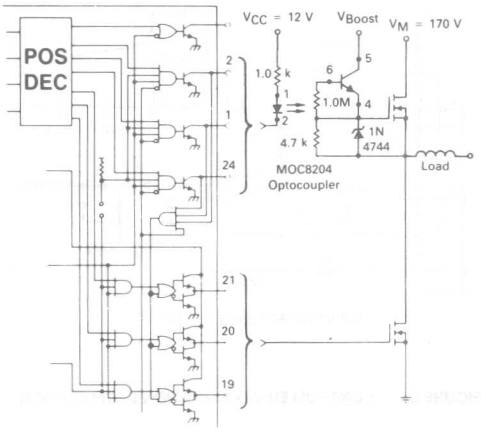
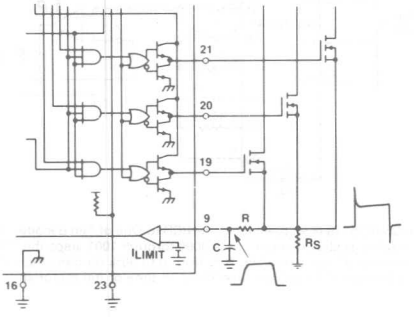
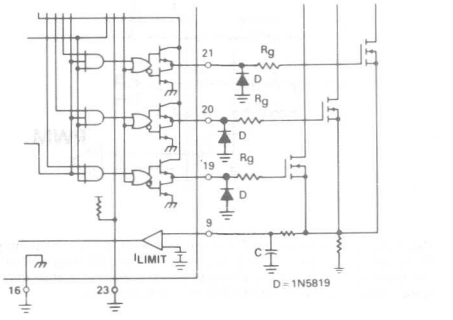


FIGURE 26 — CURRENT WAVEFORM SPIKE SUPPRESSION



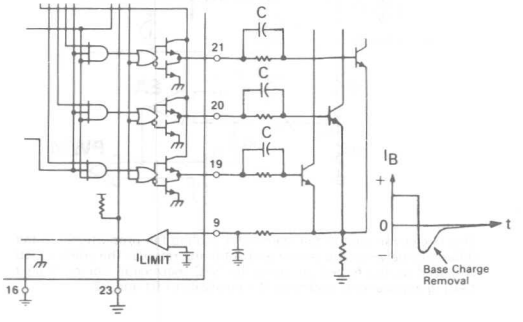
The addition of the RC filter will eliminate current-limit instability caused by the leading edge spike on the current waveform. Resistor R_S should be a low inductance type.

FIGURE 27 — MOSFET DRIVE PRECAUTIONS



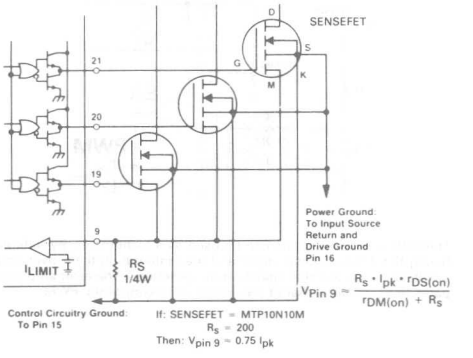
Series gate resistor R_g will damp any high frequency oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate-source circuit. Diode D is required if the negative current into the Bottom Drive Outputs exceeds 5.0 mA peak.

FIGURE 28 — BIPOLAR TRANSISTOR DRIVE



The totem-pole output can furnish negative base current for enhanced transistor turn-off, with the addition of capacitor C.

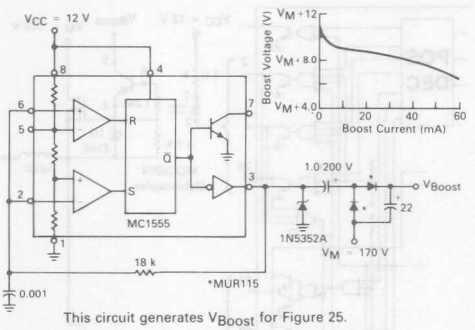
FIGURE 29 — CURRENT SENSING POWER MOSFETs



Virtually lossless current sensing can be achieved with the implementation of SENSEFET power switches.

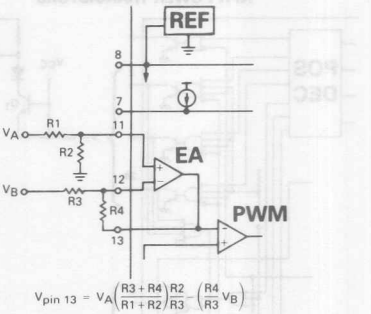
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FIGURE 30 — HIGH VOLTAGE BOOST SUPPLY



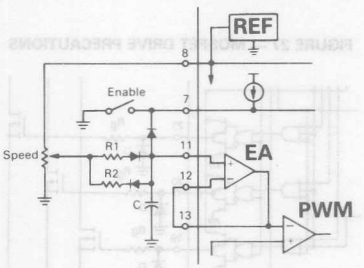
This circuit generates V_{Boost} for Figure 25.

FIGURE 31 — DIFFERENTIAL INPUT SPEED CONTROLLER



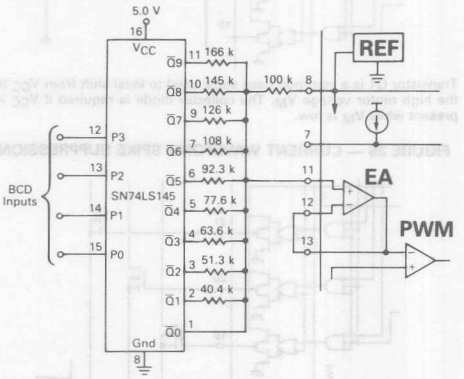
$$V_{pin\ 13} = V_A\left(\frac{R3+R4}{R1+R2}\right)\frac{R2}{R3} - \left(\frac{R4}{R3}V_B\right)$$

FIGURE 32 — CONTROLLED ACCELERATION/DECELERATION



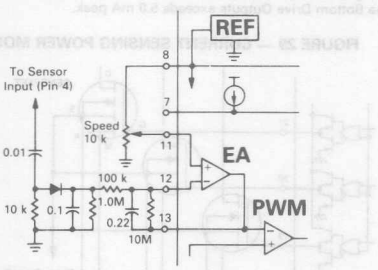
Resistors R1 with capacitor C sets the acceleration time constant while R2 controls the deceleration. The values of R1 and R2 should be at least ten times greater than that of the speed set potentiometer to minimize time constant variations with different speed settings.

FIGURE 33 — DIGITAL SPEED CONTROLLER



The SN74LS175 is an open collector BCD to One of Ten decoder. When connected as shown, input codes 0000 through 1001 steps the PWM in increments of approximately 10% from 0 to 90% on-time. Input codes 1010 through 1111 will produce 100% on-time or full motor speed.

FIGURE 34 — CLOSED-LOOP SPEED CONTROL



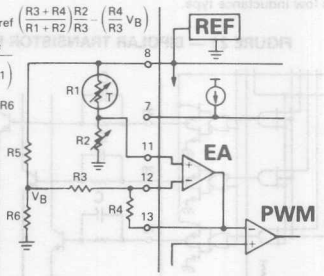
The rotor position sensors can be used as a tachometer. By differentiating the positive-going edges and then integrating them over time, a voltage proportional to speed can be generated. The error amp compares this voltage to that of the speed set to control the PWM.

FIGURE 35 — CLOSED-LOOP TEMPERATURE CONTROL

$$V_{pin\ 13} = V_{ref}\left(\frac{R3+R4}{R1+R2}\right)\frac{R2}{R3} - \left(\frac{R4}{R3}V_B\right)$$

$$V_B = \frac{V_{ref}}{\left(\frac{R5}{R6}+1\right)}$$

$R3 >> R5 \parallel R6$



This circuit can control the speed of a cooling fan proportional to the difference between the sensor and set temperatures. The control loop is closed as the forced air cools the NTC thermistor. For controlled heating applications, exchange the positions of R1 and R2.

SYSTEM APPLICATIONS

Three Phase Motor Commutation

The three phase application shown in Figure 36 is a full-featured open-loop motor controller with full wave, six step drive. The upper power switch transistors are Darlingtons while the lower devices are power MOSFETs. Each of these devices contains an internal parasitic catch diode that is used to return the stator inductive energy back to the power supply. The outputs are capable of driving a delta or wye connected stator, and a grounded neutral wye if split supplies are used. At any given rotor position, only one top and one bottom power switch (of different totem poles) is enabled. This configuration switches both ends of the stator winding from supply to ground which causes the current flow to be bidirectional or full wave. A leading edge spike is usually present on the current waveform and can cause a current-limit instability. The spike can be eliminated by adding an RC filter in series with the current sense input. Using a low inductance type resistor for R_S will also aid in spike reduction. Care must be taken in the selection of the bottom power switch transistors so that the current during braking does not exceed the device rating. During braking, the peak current generated is limited only by the series resistance of the conducting bottom switch and winding.

$$I_{peak} = \frac{V_M + EMF}{R_{switch} + R_{winding}}$$

If the motor is running at maximum speed with no load, the generated back EMF can be as high as the supply voltage, and at the onset of braking the peak current may approach twice the motor stall current. Figure 37 shows the commutation waveforms over two electrical cycles. The first cycle (0° to 360°) depicts motor operation at full speed while the second cycle (360° to 720°) shows a reduced speed with about 50 percent pulse width modulation. The current waveforms reflect a constant torque load and are shown synchronous to the commutation frequency for clarity.

4

FIGURE 36 — THREE PHASE, SIX STEP, FULL WAVE MOTOR CONTROLLER

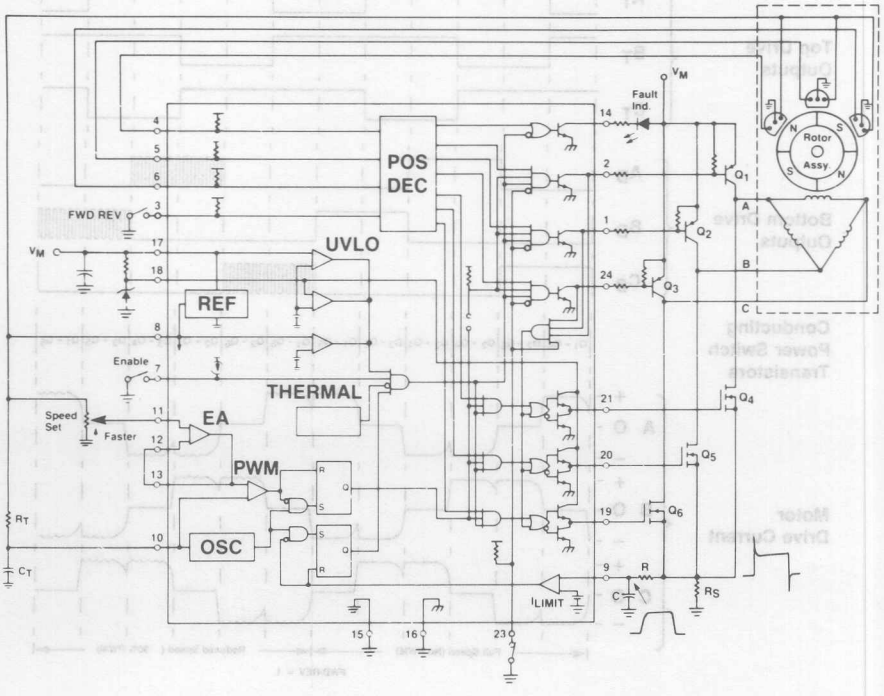


FIGURE 37 — THREE PHASE, SIX STEP, FULL WAVE COMMUTATION WAVEFORMS

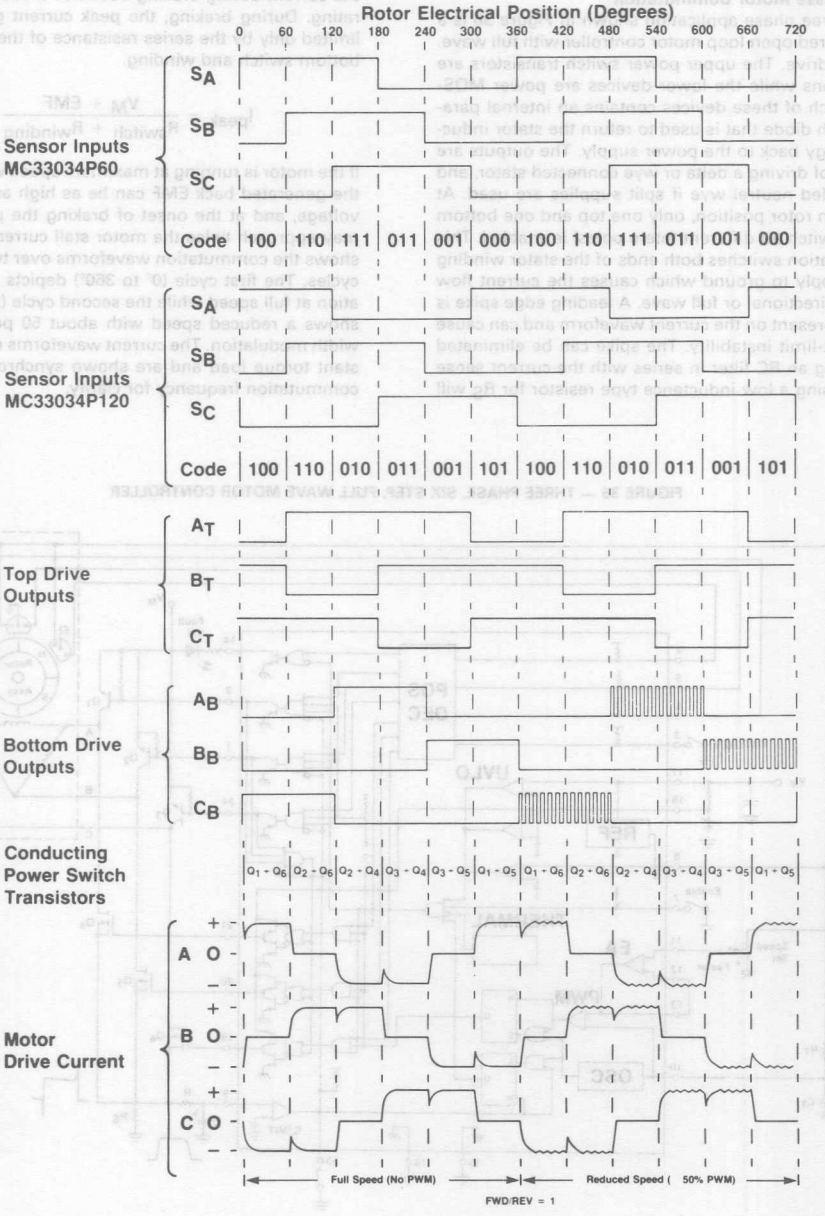


FIGURE 38 — THREE PHASE, THREE STEP, HALF WAVE MOTOR CONTROLLER

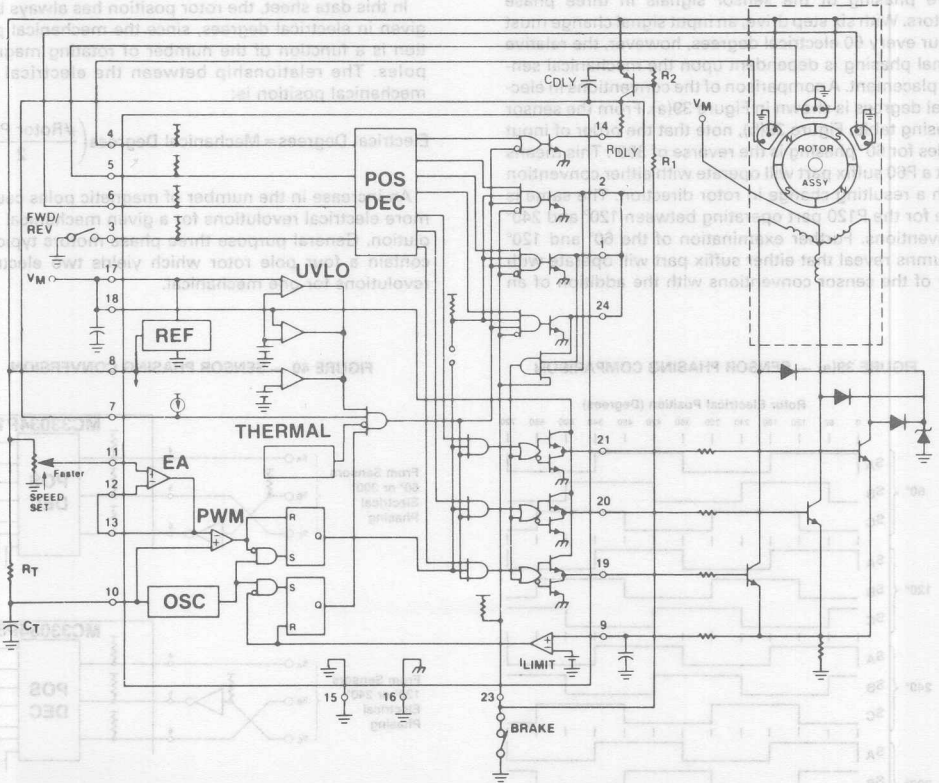


Figure 38 shows a three phase, three step, half wave motor controller. This configuration is ideally suited for automotive and other low voltage applications since there is only one power switch voltage drop in series with a given stator winding. Current flow is unidirectional or half wave because only one end of each winding is switched. Continuous braking with the typical half wave arrangement presents a motor overheating problem since stator current is limited only by the winding resistance. This is due to the lack of upper power switch transistors, as in the full wave circuit, used to disconnect the windings from the supply voltage V_M. A unique solution is to provide braking until the motor stops and then turn off the bottom drives. This can be accomplished by using the fault output in conjunction with the enable input as an over current timer. Components R_{DLY} and C_{DLY} are selected to give the motor sufficient time to stop before latching the enable input and the top drive AND gate low. To enabling the motor, the PNP transistor along with resistors R1 and R3 are used to reset the latch by discharging C_{DLY} upon brake switch closure. The stator flyback voltage is clamped by a single zener and three diodes.

There are four conventions used to establish the relative phasing of the sensor signals in three phase motors. With six step drive, an input signal change must occur every 60 electrical degrees, however, the relative signal phasing is dependent upon the mechanical sensor placement. A comparison of the conventions in electrical degrees is shown in Figure 39(a). From the sensor phasing table, Figure 39(b), note that the order of input codes for 60° phasing is the reverse of 300°. This means that a P60 suffix part will operate with either convention with a resulting change in rotor direction. The same is true for the P120 part operating between 120° and 240° conventions. Further examination of the 60° and 120° columns reveal that either suffix part will operate with any of the sensor conventions with the addition of an

shown in Figure 40.

In this data sheet, the rotor position has always been given in electrical degrees, since the mechanical position is a function of the number of rotating magnetic poles. The relationship between the electrical and mechanical position is:

$$\text{Electrical Degrees} = \text{Mechanical Degrees}\left(\frac{\#\text{Rotor Poles}}{2}\right)$$

An increase in the number of magnetic poles causes more electrical revolutions for a given mechanical revolution. General purpose three phase motors typically contain a four pole rotor which yields two electrical revolutions for one mechanical.

FIGURE 39(a) — SENSOR PHASING COMPARISON

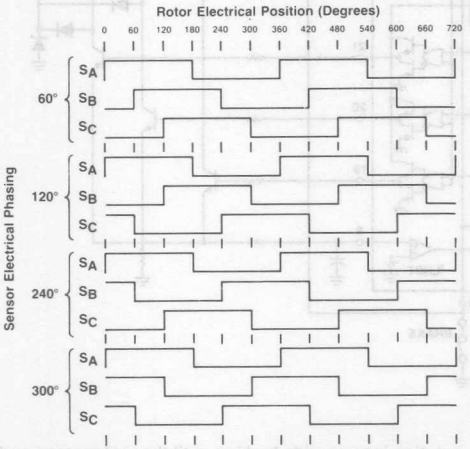
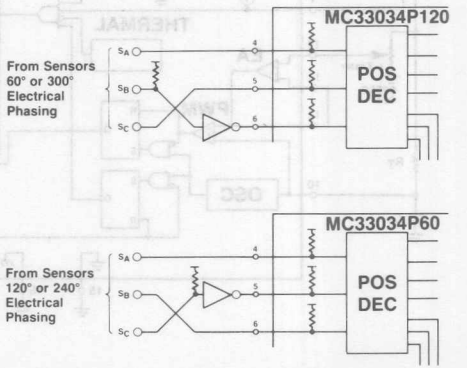


FIGURE 39(b) — SENSOR PHASING TABLE

Sensor Electrical Phasing (Degrees)												
60°			120°			240°			300°		
S_A	S_B	S_C	S_A	S_B	S_C	S_A	S_B	S_C	S_A	S_B	S_C
1	0	0	1	0	1	1	1	0	1	1	1
1	1	0	1	0	0	1	0	0	1	1	0
1	1	1	1	1	0	1	0	1	1	0	0
0	1	1	0	1	0	0	0	1	0	0	0
0	0	1	0	1	1	0	1	1	0	0	1
0	0	0	0	0	1	0	1	0	0	1	1

FIGURE 40 — SENSOR PHASING CONVERSION



Two and Four Phase Motor Commutation

The MC33034P60 is also capable of providing a four step output that can be used to drive two or four phase motors. The truth table in Figure 41 shows that by connecting sensor inputs S_B and S_C together, it is possible to truncate the number of drive output states from six to four. The output power switches are connected to B_T, C_T, B_B, and C_B. Figure 42 shows a four phase, four step, full wave motor control application. Power switch transistors Q1 through Q8 are Darlington type, each with an internal parasitic catch diode. With four step drive, only two rotor position sensors spaced at 90 electrical degrees are required. The commutation waveforms are shown in Figure 43.

Figure 44 shows a four phase, four step, half wave motor controller. It has the same features as the circuit in Figure 38, except for the deletion of braking.

FIGURE 41 — TWO AND FOUR PHASE, FOUR STEP, COMMUTATION TRUTH TABLE

MC33034P60						
Inputs			Outputs			
Sensor Electrical Spacing = 90°			Top Drives		Bottom Drives	
S_A	S_B	F/R	B_T	C_T	B_B	C_B
1	0	1	1	1	0	1
1	1	1	0	1	0	0
0	1	1	1	0	0	0
0	0	1	1	1	1	0
1	0	0	1	0	0	0
1	1	0	1	1	1	0
0	1	0	1	1	0	1
0	0	0	0	1	0	0

S_B connected to S_C

FIGURE 42 — FOUR PHASE, FOUR STEP, FULL WAVE MOTOR CONTROLLER

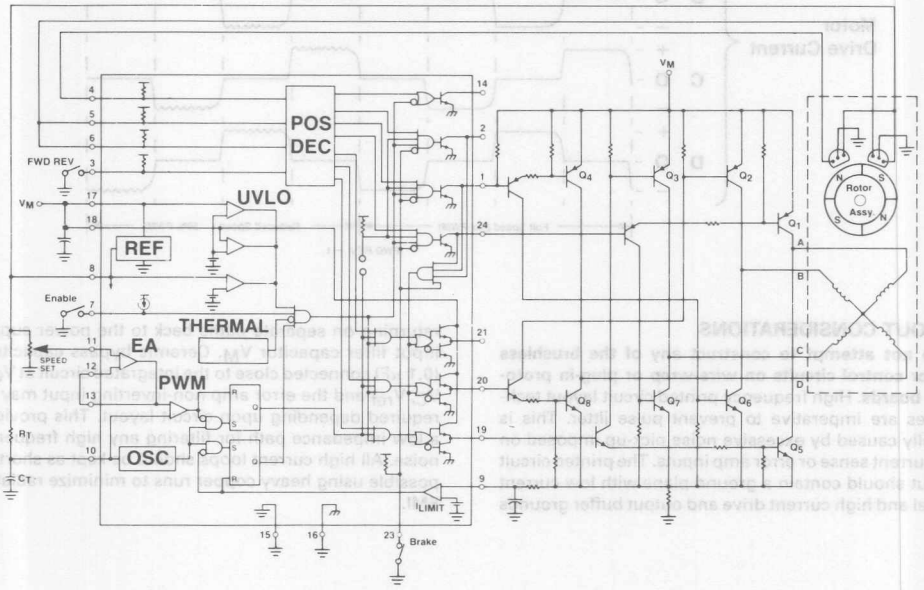
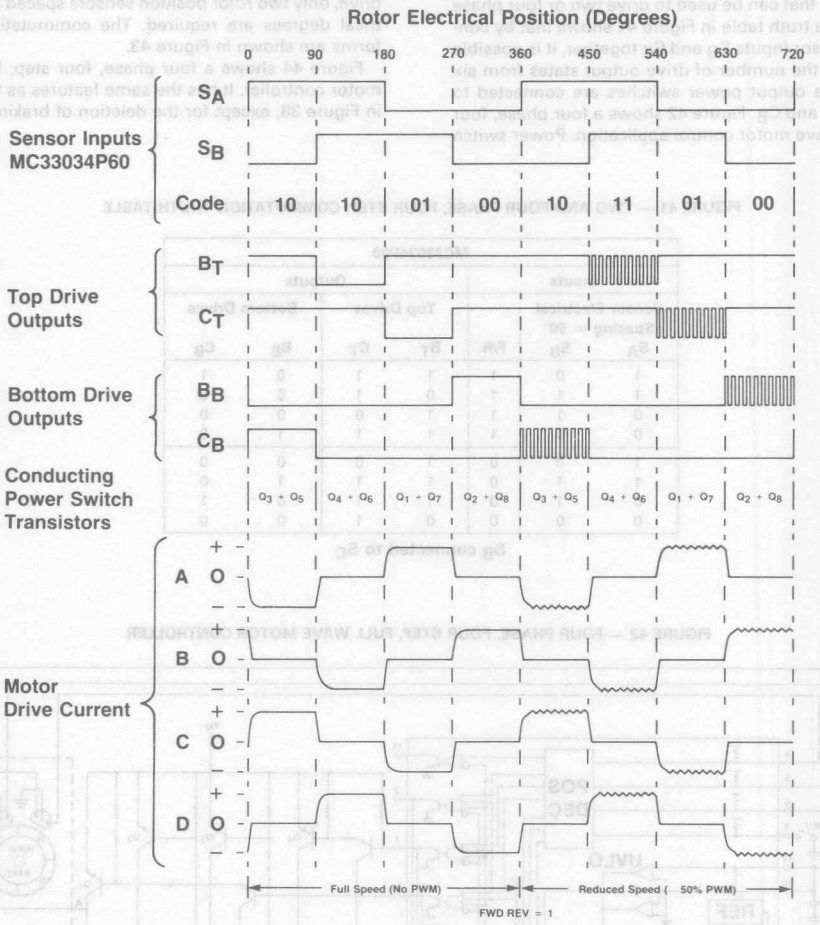


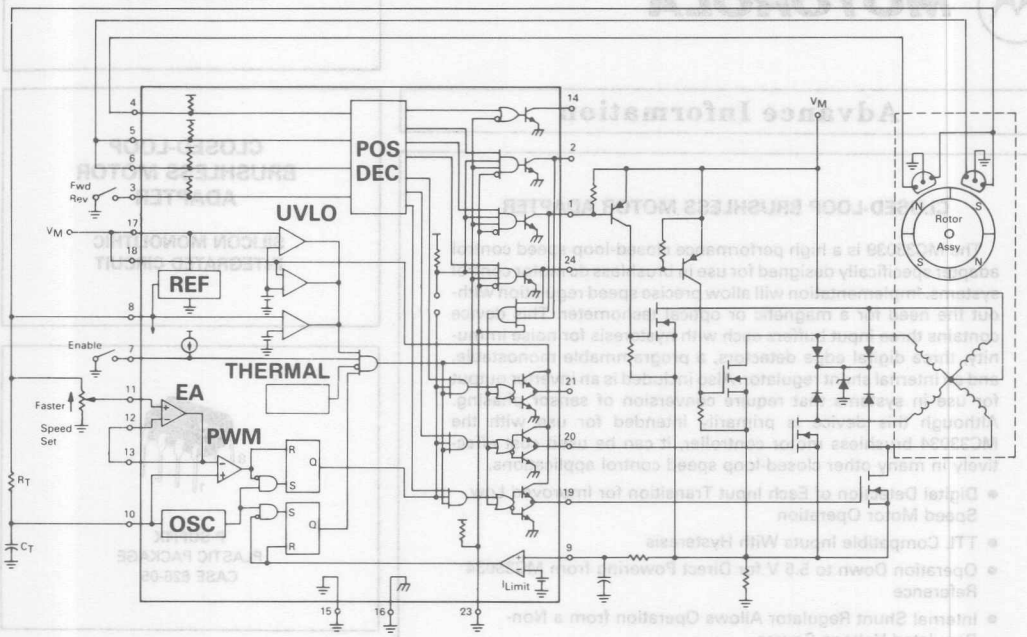
FIGURE 43 — FOUR PHASE, FOUR STEP, FULL WAVE COMMUTATION WAVEFORMS



LAYOUT CONSIDERATIONS

Do not attempt to construct any of the brushless motor control circuits on wire-wrap or plug-in prototype boards. High frequency printed circuit layout techniques are imperative to prevent pulse jitter. This is usually caused by excessive noise pick-up imposed on the current sense or error amp inputs. The printed circuit layout should contain a ground plane with low current signal and high current drive and output buffer grounds returning on separate paths back to the power supply input filter capacitor V_M. Ceramic bypass capacitors (0.1 μF) connected close to the integrated circuit at V_{CC}, V_C, V_{ref} and the error amp non-inverting input may be required depending upon circuit layout. This provides a low impedance path for filtering any high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI.

FIGURE 44 — FOUR PHASE, FOUR STEP, HALF WAVE MOTOR CONTROLLER



MOTOROLA

MC33039

Advance Information

4

CLOSED-LOOP BRUSHLESS MOTOR ADAPTER

The MC33039 is a high performance closed-loop speed control adapter specifically designed for use in brushless dc motor control systems. Implementation will allow precise speed regulation without the need for a magnetic or optical tachometer. This device contains three input buffers each with hysteresis for noise immunity, three digital edge detectors, a programmable monostable, and an internal shunt regulator. Also included is an inverter output for use in systems that require conversion of sensor phasing. Although this device is primarily intended for use with the MC33034 brushless motor controller, it can be used cost effectively in many other closed-loop speed control applications.

- Digital Detection of Each Input Transition for Improved Low Speed Motor Operation
- TTL Compatible Inputs With Hysteresis
- Operation Down to 5.5 V for Direct Powering from MC33034 Reference
- Internal Shunt Regulator Allows Operation from a Non-Regulated Voltage Source
- Inverter Output for Easy Conversion Between 60°/300° and 120°/240° Sensor Phasing Conventions

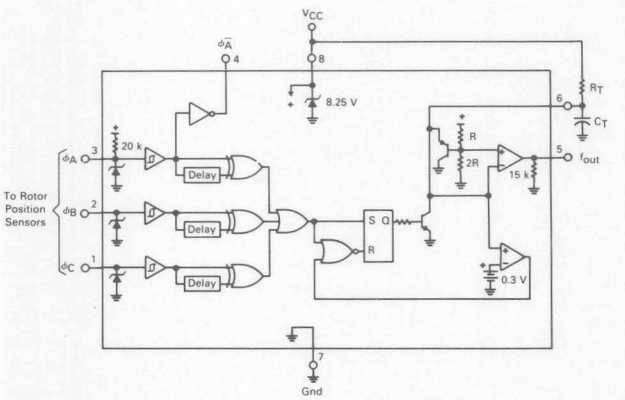
CLOSED-LOOP BRUSHLESS MOTOR ADAPTER

SILICON MONOLITHIC INTEGRATED CIRCUIT

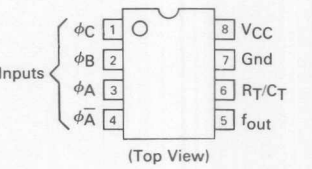


P SUFFIX
PLASTIC PACKAGE
CASE 626-05

REPRESENTATIVE BLOCK DIAGRAM



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC33039P	−40°C to +85°C	Plastic DIP

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
V_{CC} Zener Current	$I_{Z(V_{CC})}$	30	mA
Logic Input Current (Pins 1, 2, 3)	I_{IH}	5.0	mA
Output Current (Pin 4, 5), Sink or Source	I_{DRV}	20	mA
Power Dissipation and Thermal Characteristics Maximum Power Dissipation @ T_A = +85°C Thermal Resistance Junction to Air	 P_D $R_{\theta JA}$	 650 100	 mW °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

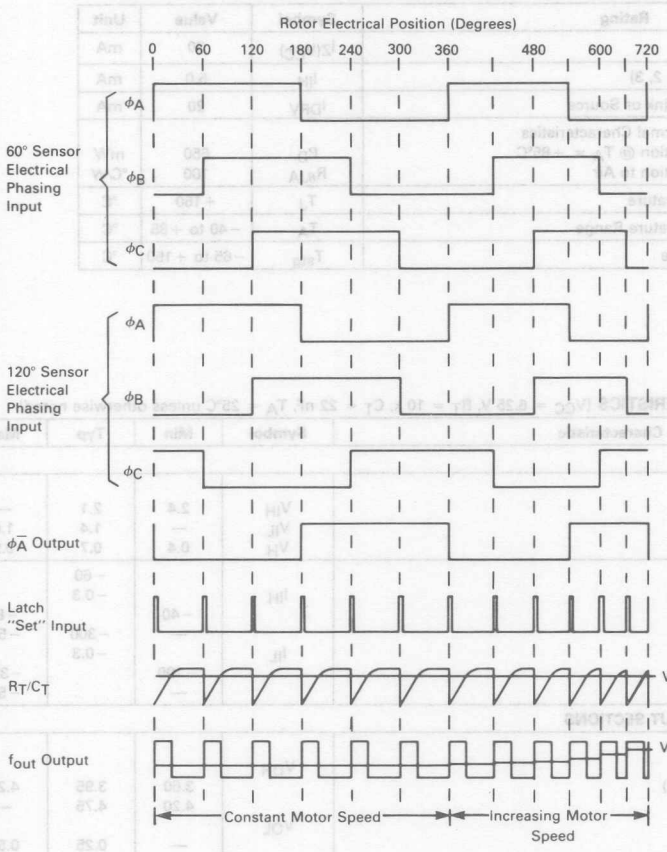
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ELECTRICAL CHARACTERISTICS (V_{CC} = 6.25 V, R_T = 10 k, C_T = 22 nF, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
LOGIC INPUTS					
Input Threshold Voltage					V
High State	V_{IH}	2.4	2.1	—	
Low State	V_{IL}	—	1.4	1.0	
Hysteresis	V_H	0.4	0.7	0.9	
Input Current					μA
High State (V_{IH} = 5.0 V)	I_{IH}		−60		
			−0.3		
ϕA		−40		−80	
ϕB, ϕC		—	−300	−5.0	
Low State (V_{IL} = 0 V)	I_{IL}		−0.3		
ϕA		−190		−380	
ϕB, ϕC		—		−5.0	
MONOSTABLE AND OUTPUT SECTIONS					
Output Voltage					V
High State	V_{OH}				
f_{out} (I_{source} = 5.0 mA)		3.60	3.95	4.20	
$\overline{\phi A}$ (I_{source} = 2.0 mA)		4.20	4.75	—	
Low State	V_{OL}				
f_{out} (I_{sink} = 10 mA)		—	0.25	0.50	
$\overline{\phi A}$ (I_{sink} = 10 mA)		—	0.25	0.50	
Capacitor C_T Discharge Current	I_{dischg}	20	35	60	mA
Output Pulse Width (Pin 5)	t_W	205	225	245	μs
POWER SUPPLY SECTION					
Power Supply Operating Voltage Range (T_A = −40°C to +85°C)	V_{CC}	5.5	—	V_Z	V
Power Supply Current	I_{CC}	1.8	3.9	5.0	mA
Zener Voltage (I_Z = 10 mA)	V_Z	7.5	8.25	9.0	V
Zener Dynamic Impedance (ΔI_Z = 10 mA to 20 mA, f ≤ 1.0 kHz)	$\lvert Z_{ka} \rvert$	—	2.0	5.0	Ω

4

FIGURE 1 — TYPICAL THREE PHASE, SIX STEP MOTOR APPLICATION



OPERATING DESCRIPTION

The MC33039 provides an economical method of implementing closed-loop speed control of brushless dc motors by eliminating the need for a magnetic or optical tachometer. Shown in the timing diagram of Figure 1, the three inputs (Pins 1, 2, 3) monitor the brushless motor rotor position sensors. Each sensor signal transition is digitally detected, OR'ed at the Latch 'Set' Input, and causes C_T to discharge. A corresponding output pulse is generated at f_{out} (Pin 5) of a defined amplitude, and programmable width determined by the values selected for R_T and C_T (Pin 6). The average voltage of the output pulse train increases with motor speed. When fed through a low pass filter or integrator, a dc voltage proportional to speed is generated. Figure 2 shows the proper connections for a typical closed loop application using the MC33034 brushless motor controller. Constant speed operation down to 100 RPM is possible with economical three phase four pole motors.

The ϕ_A inverter output (Pin 4) is used in systems where the controller and motor sensor phasing conventions are not compatible. A method of converting from either convention to the other is shown in Figure 3. For a more detailed explanation of this subject, refer to the text above Figure 39 on the MC33034 data sheet.

The output pulse amplitude V_{OH} is constant with temperature and controlled by the supply voltage on V_{CC} (Pin 8). Operation down to 5.5 V is guaranteed over temperature. For systems without a regulated power supply, an internal 8.25 V shunt regulator is provided.

FIGURE 2 — TYPICAL CLOSED-LOOP SPEED CONTROL APPLICATION

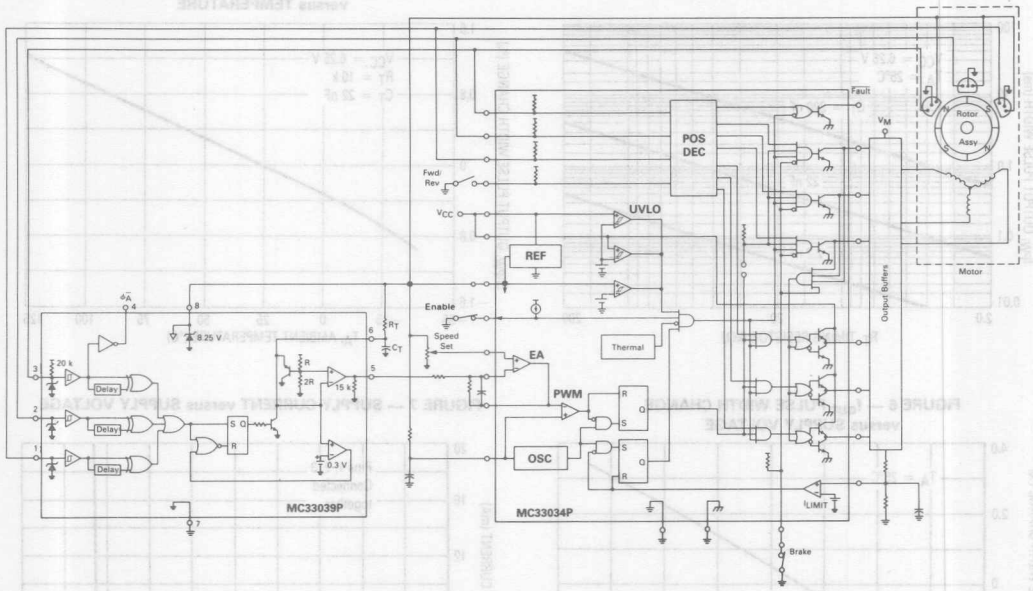
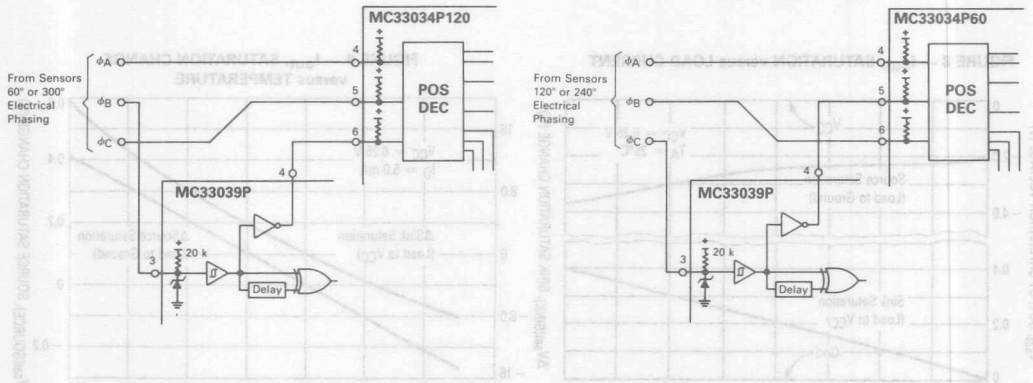
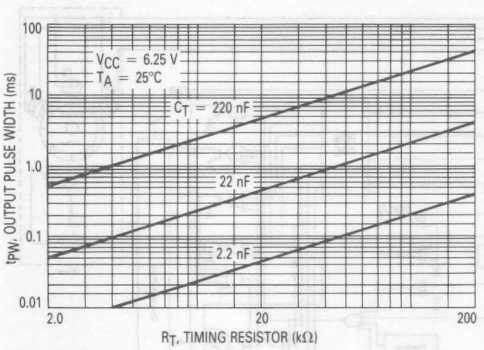


FIGURE 3 — CONVERSION BETWEEN SENSOR PHASING CONVENTIONS





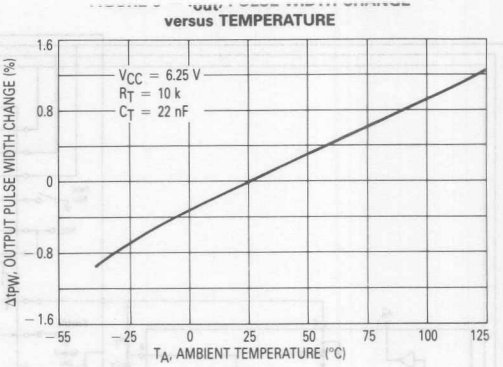


FIGURE 6 — f_{out} PULSE WIDTH CHANGE versus SUPPLY VOLTAGE

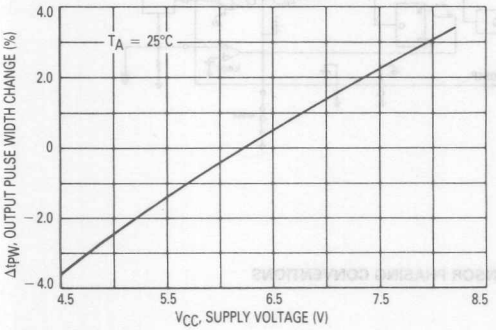


FIGURE 7 — SUPPLY CURRENT versus SUPPLY VOLTAGE

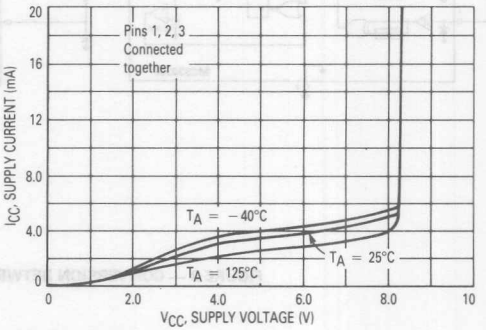


FIGURE 8 — f_{out}, SATURATION versus LOAD CURRENT

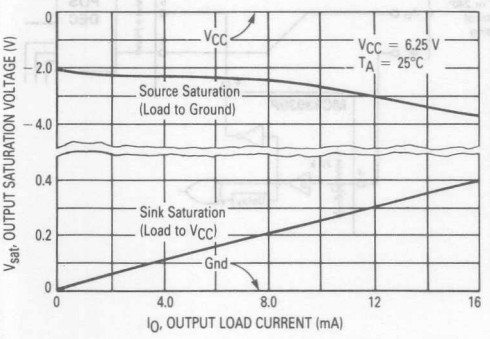
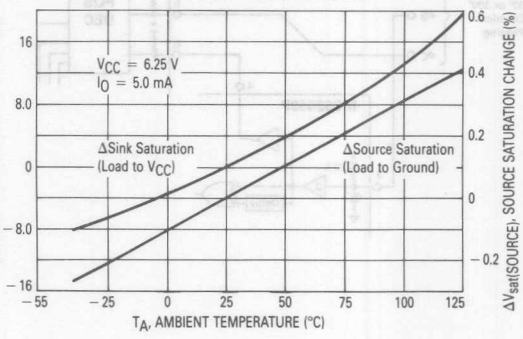


FIGURE 9 — f_{out}, SATURATION CHANGE versus TEMPERATURE



MOTOROLA

SAA1042
SAA1042A

Specifications and Applications Information

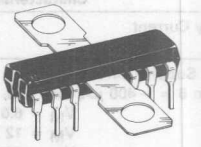
STEPPER MOTOR DRIVER

The SAA1042 drives a two-phase stepper motor in the bipolar mode. The device contains: three input stages, a logic section and two output stages.

- Drive Stages Designed for Motors: 6.0 V and 12 V: SAA1042
  24 V: SAA1042A
- 500 mA/Coil Drive Capability
- Built-In Clamp Diodes for Overvoltage Suppression
- Wide Logic Supply Voltage Range
- Accepts Commands for CW/CCW and Half/Full Step Operation
- Inputs Compatible with Popular Logic Families: MOS, TTL, DTL
- Set Input Defined Output State
- Drive Stage Bias Adaptable to Motor Power Dissipation for Optimum Efficiency

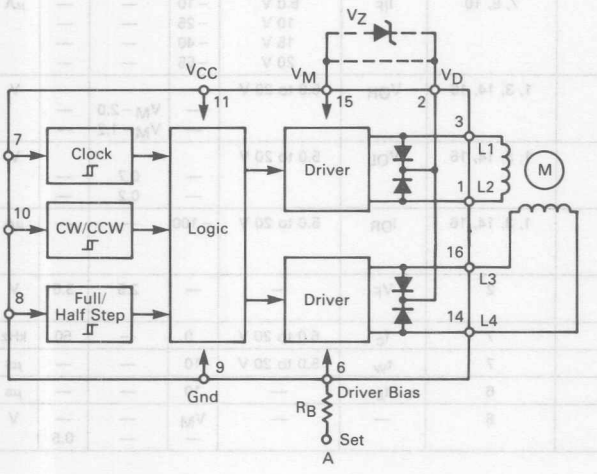
STEPPER MOTOR DRIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT

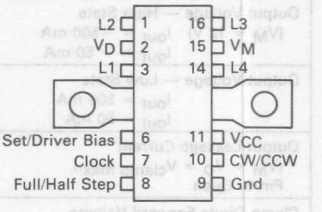


PLASTIC PACKAGE
CASE 721-02

FIGURE 1 — SAA1042 BLOCK DIAGRAM



PIN ASSIGNMENT



(Top View)

Note: Case heat sink is electrically connected to ground (Pin 9) through the die substrate.

MAXIMUM RATINGS (T_A = 25°C unless otherwise stated)

Rating	Symbol	SAA1042	SAA1042A	Unit
Clamping Voltage (Pins 1, 3, 14 & 16)	V_{clamp}	20	30	V
Over Voltage ($V_{OV} = V_{clamp} - V_M$)	V_{OV}	6.0		V
Supply Voltage	V_{CC}	20	30	V
Switching or Motor Current/Coil	I_M	500		mA
Input Voltage (Pins 7, 8 & 10) V_{in} clock V_{in} Full/Half V_{in} CW/CCW	V_{CC}			V
Power Dissipation	P_D*	2.0		W
Derate above T_A = 25°C	$1/\theta JA$	20		mW/°C
Thermal Resistance, Junction to Air	θJA	50		°C/W
Thermal Resistance, Junction to Case	θJC	8.0		°C/W
Operating Junction Temperature Range	T_J	−30 to +125		°C
Storage Temperature Range	T_{stg}	−65 to +150		°C

*The power dissipation, P_D, of the circuit is given by the supply voltage, V_M and V_{CC}, and the motor current, I_M, and can be determined from Figures 3 and 5. $P_D = P_{drive} + P_{logic}$.

ELECTRICAL CHARACTERISTICS (T_A = +25°C)

Characteristic	Pin	Symbol	V_{CC}	Min	Typ	Max	Unit
Supply Current	11	I_{CC}	5.0 V	—	—	3.5	mA
			20 V	—	—	8.5	
Motor Supply Current	15	I_M					mA
(I Pin 6 = −400 μA, Pins 1, 3, 14, 16 Open)							
V_M = 6.0 V			5.0 V	—	25	—	
V_M = 12 V			5.0 V	—	30	—	
V_M = 24 V			5.0 V	—	40	—	
Input Voltage — High State	7, 8, 10	V_{IH}	5.0 V	2.0	—	—	V
			10 V	7.0	—	—	
			15 V	10	—	—	
			20 V	14	—	—	
Input Voltage — Low State	7, 8, 10	V_{IL}	5.0 V	—	—	0.8	V
			10 V	—	—	1.5	
			15 V	—	—	2.5	
			20 V	—	—	3.5	
Input Reverse Current — High State	7, 8, 10	I_{IR}	5.0 V	—	—	2.0	μA
($V_{in} = V_{CC}$)			10 V	—	—	2.0	
			15 V	—	—	3.0	
			20 V	—	—	5.0	
Input Forward Current — Low State	7, 8, 10	I_{IF}	5.0 V	−10	—	—	μA
(V_{in} = Gnd)			10 V	−25	—	—	
			15 V	−40	—	—	
			20 V	−55	—	—	
Output Voltage — High State	1, 3, 14, 16	V_{OH}	5.0 to 20 V				V
(V_M = 12 V) I_{out} = −500 mA				—	$V_M - 2.0$	—	
I_{out} = − 50 mA				—	$V_M - 1.2$	—	
Output Voltage — Low State	1, 3, 14, 16	V_{OL}	5.0 to 20 V				V
I_{out} = 500 mA				—	0.7	—	
I_{out} = 50 mA				—	0.2	—	
Output Leakage Current	1, 3, 14, 16	I_{DR}	5.0 to 20 V	−100	—	—	μA
($V_M = V_D = V_{clamp\ max}$.)							
Pin 6: Open							
Clamp Diode Forward Voltage	2	V_F	—	—	2.5	3.5	V
(Drop at I_M = 500 mA)							
Clock Frequency	7	f_c	5.0 to 20 V	0	—	50	kHz
Clock Pulse Width	7	t_w	5.0 to 20 V	10	—	—	μs
Set Pulse Width	6	t_s	—	10	—	—	μs
Set Control Voltage — High State	6	—	—	V_M	—	—	V
Low State				—	—	0.5	

INPUT/OUTPUT FUNCTIONS

Clock — (Pin 7) This input is active on the positive edge of the clock pulse and accepts Logic '1' input levels dependant on the supply voltage and includes hysteresis for noise immunity.

CW/CCW — (Pin 10) This input determines the motor's rotational direction. When the input is held low, (OV, see the electrical characteristics) the motor's direction is nominally clockwise (CW). When the input is in the high state, Logic '1,' the motor direction will be nominally counter clockwise (CCW), depending on the motor connections.

Full/Half Step — (Pin 8) This input determines the angular rotation of the motor for each clock pulse. In the low state the motor will make a full step for each applied clock pulse, while in the high state, the motor will make half a step.

V_D — (Pin 2) This pin is used to protect the outputs (1, 3, 14, 16) where large positive spikes occur due to switching the motor coils. The maximum allowable voltage on these pins is the clamp voltage (V_{clamp}). Motor performance is improved if a zener diode is connected between Pin 2 and Pin 15 as shown in Figure 1.

The following conditions have to be considered when selecting the zener diode:

$V_{clamp} = V_M + 6.0\ V$

$V_Z = V_{clamp} - V_M - V_F$*

where: V_F = clamp diodes forward voltage drop (see Figure 4)

V_{clamp}:
- ≤ 20 V for SAA1042
- ≤ 30 V for SAA1042A

Pins 2 and 15 can be linked, in this case $V_Z = 0$ V.

Set/Bias Input — (Pin 6) This input has two functions:

The resistor R_B adapts the drivers to the motor current.

A pulse via the resistor R_B sets the outputs (1, 3, 14, 16) to a defined state.

The resistor R_B can be determined from the graph of Figure 2 according to the motor current and voltage. Smaller values of R_B will increase the power dissipation of the circuit and larger values of R_B may increase the saturation voltage of the driver transistors.

When the "set" function is not used, terminal A of the resistor R_B must be grounded. When the set function is used, terminal A has to be connected to an open-collector (buffer) circuit. Figure 7 shows this configuration. The buffer circuit (off-state) has to sustain the motor voltage V_M. When a pulse is applied via the buffer and the bias resistor R_B:

During the pulse duration, the motor driver transistors are turned off.

After elapsing the pulse, the outputs will have defined states.

Figure 6 shows the timing diagram.

Figure 7 illustrates a typical application in which the SAA1042 drives a 12 V stepper motor with a current consumption of 200 mA/coil.

A bias resistor (R_B) of 56 kΩ is chosen according to Figure 2.

The maximum voltage permitted at the output pin is V_M + 6.0 V (see the Maximum Ratings), in this application V_M = 12 V, therefore the maximum voltage is 18 V. The outputs are protected by the internal diodes and an external zener connected between Pins 2 and 15.

From Figure 4, it can be seen that the voltage drop across the internal diodes is about 1.7 V at 200 mA. This results in a zener voltage between Pins 2 and 15 of:

$$V_Z = 6.0\ V - 1.7\ V = 4.3\ V.$$

To allow for production tolerances and a safety margin, a 3.9 V zener has been chosen for this example.

The clock is derived from the line frequency which is phase locked by the MC14046B and the MC14024.

The voltage on the clock input, is normally low (Logic '0'). The motor steps on the positive going transition of the clock pulse.

A Logic '0' applied to the Full/Half input, Pin 8, operates the motor in the Full Step mode. A Logic '1' at this input will result in the Half Step mode. The logic level state on the CW/CCW input, Pin 10, and the connection of the motor coils to the outputs determines the rotational direction of the motor.

These two inputs should be biased to a Logic '0' or '1' and not left floating. In the event of non-use, they should be tied to ground or the logic supply line, V_{CC}.

The output drivers can be set to a fixed operating point by use of the Set input and a bias resistor R_B. A positive pulse to this input turns the drivers off and sets the logic state of the outputs.

After the negative going transition of the Set pulse, and until the first positive going transition of the clock, the outputs will be:

L1 = L3 = high and L2 = L4 = low.

(See Figure 6, the timing diagram).

The Set input can be driven by a MC14007B or a transistor whose collector resistor is R_B. If the input is not used, the 'bottom' of R_B must be grounded.

The total power dissipation of the circuit can be determined from Figures 3 and 5.

$$P_D = 0.9\ W + 0.08\ W = 0.98\ W.$$

This results in a junction to ambient temperature, without a heatsink of:

$$T_J - T_A = 50°C/W \times 0.98\ W = 49°C.$$

or a maximum ambient temperature of 76°C. For operation at elevated temperatures a heatsink is required.

4

FIGURE 2 — BIAS RESISTOR R_B versus MOTOR CURRENT

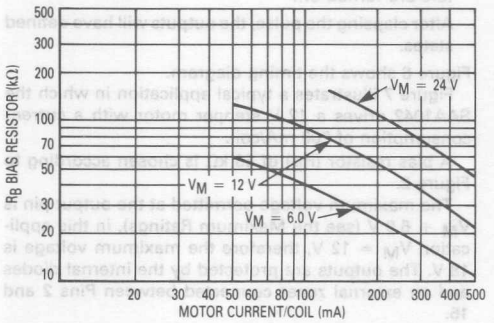


FIGURE 3 — DRIVE STAGE POWER DISSIPATION

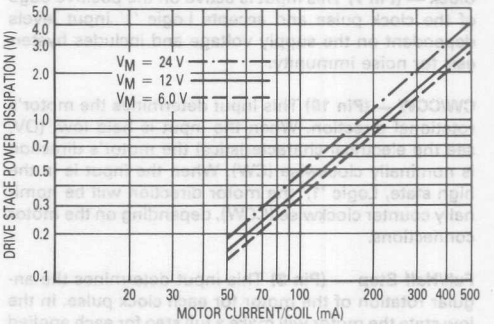


FIGURE 4 — CLAMP DIODE FORWARD CURRENT versus FORWARD VOLTAGE

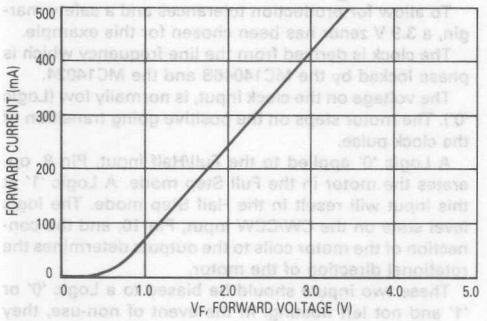


FIGURE 5 — POWER DISSIPATION versus LOGIC SUPPLY VOLTAGE

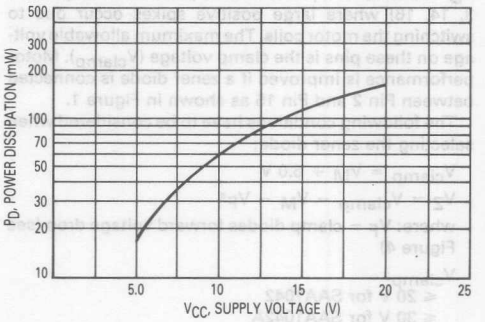


FIGURE 6 — TIMING DIAGRAM

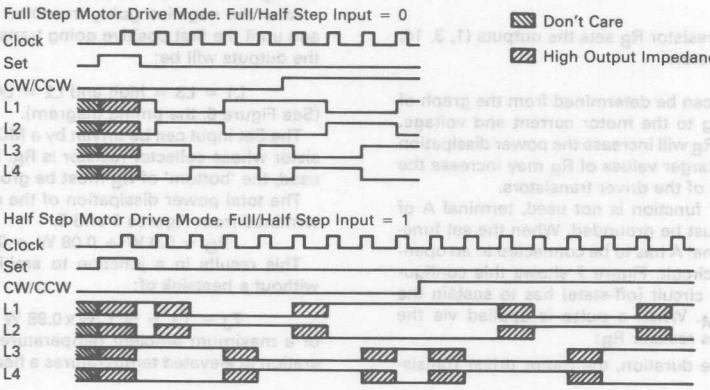
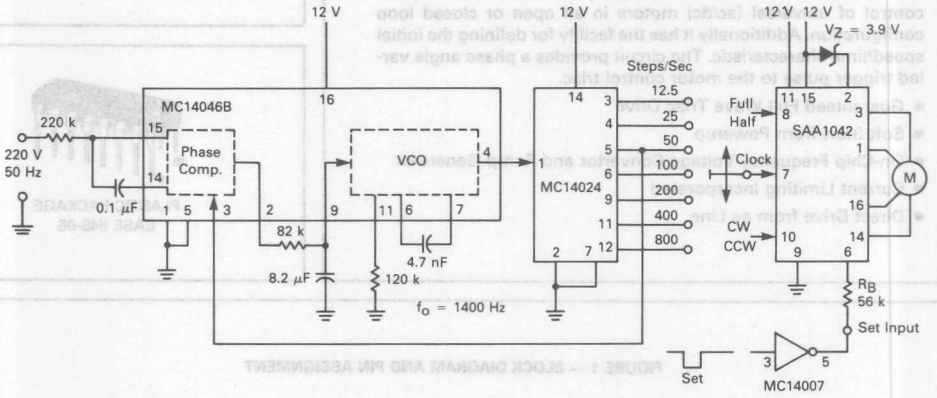


FIGURE 7 — TYPICAL APPLICATION
SELECTABLE STEP RATES WITH THE TIME BASE DERIVED FROM THE LINE FREQUENCY



MOTOROLA

TDA1085A

Specification and Applications Information

UNIVERSAL MOTOR SPEED CONTROLLER

SILICON MONOLITHIC INTEGRATED CIRCUIT

4

UNIVERSAL MOTOR SPEED CONTROLLER

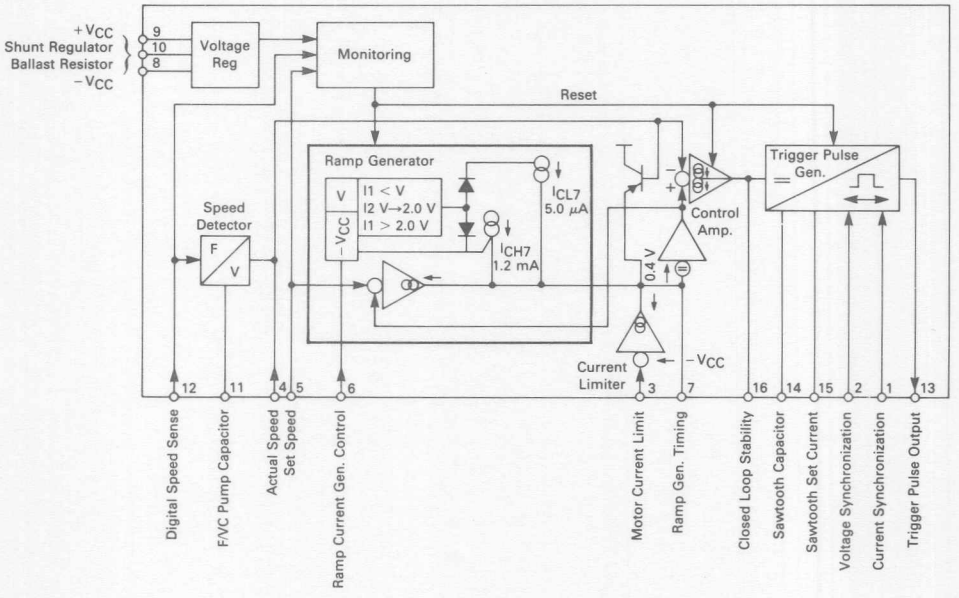
The TDA1085A has all the necessary functions for the speed control of universal (ac/dc) motors in an open or closed loop configuration. Additionally it has the facility for defining the initial speed/time characteristic. The circuit provides a phase angle varied trigger pulse to the motor control triac.

- Guaranteed Full Wave Triac Drive
- Soft Start from Powerup
- On-Chip Frequency/Voltage Convertor and Ramp Generator
- Current Limiting Incorporated
- Direct Drive from ac Line



PLASTIC PACKAGE
CASE 648-06

FIGURE 1 — BLOCK DIAGRAM AND PIN ASSIGNMENT



MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Power Supply Voltage	$V_{Pin\ 9\text{-}8}$	17	V
Power Supply Current (Pin 10 Open)	$I_{Pin\ 9}$	15	mA
Peak Power Supply Regulation Current	$I_{Pin\ 9} + I_{Pin\ 10}$	35	mA
Peak ac Synchronization Input Current	$I_{Pin\ 1}$ $I_{Pin\ 2}$	±1.0	mA
Peak Output Triggering Current (Pulse Width 300 μs; Duty Cycle ≤ 3%)	$I_{Pin\ 13}$	200	mA
Current Drain per Listed Pin	I_{15} I_3 I_{12}	1.0 −5.0 −3.0, +0.1	mA
Power Dissipation (T_A = 25°C) Derate above 25°C	P_D $1/R_{\theta JA}$	625 6.8	mW mW/°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise stated)

Characteristic	Symbol	Min	Typ	Max	Unit
VOLTAGE REGULATOR					
Regulated Voltage* ($I_9 + I_{10}$ = 10 mA)	V_{CC}	—	15.5	—	V
Monitoring Enable Level*	V_{ME}	—	15.1	—	V
Monitoring Disable Level*	V_{MD}	—	14.5	—	V
Internal Current Consumption, Note 1	$I_{Pin\ 9}$	—	4.2	—	mA
RAMP GENERATOR					
Reference Input Voltage Range, Note 2	$V_{Pin\ 5\text{-}8}$	0.08	—	13.5	V
Reference Input Bias Current	$I_{Pin\ 5}$	—	—	−20	μA
Distribute Low Level Voltage Range	$V_{Pin\ 6}$	0	—	2.0	V
Distribute — Low Level (Figure 2)	V_{DL}	—	$V_{Pin\ 6}$	—	V
Distribute — Upper Level* (Figure 2) ($V_{Pin\ 6}$ = 950 mV)	V_{DU}	1.9 V_6	2.0 V_6	2.1 V_6	V
Low–High Acceleration Range (Figure 2)	ΔV_{DA}	—	400	—	mV
High Acceleration Charging Current	I_{CH7}	—	1.2	—	mA
Low Charging Current, Note 3	I_{CL7}	—	5.0	—	μA

NOTES:

1. Pins 1, 2, 11, 12, 14 and 15 not connected; Pins 4, 5, 6 and 7 grounded to Pin 8: V_{CC} = 15.5 V
2. When $V_{Pin\ 5}$ is ≤ 80 mV, the internal monitoring circuit interprets it as a true zero, thus minimizing the effects of control amplifier offsets.
3. This value should be accounted for when externally setting the distribute acceleration charging current.

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Min	Typ	Max	Unit
CURRENT LIMITER					
Stage Current Gain	$\frac{I_{DL7}}{\Delta I_3}$	—	170	—	—
Output Discharge Current Swing	I_{DL7}	—	35	—	mA
CONTROL AMPLIFIER					
Actual Speed Voltage Range	$V_{Pin\ 4\text{-}8}$	0	—	13.5	V
Actual Speed Input Bias Current	$I_{Pin\ 4}$	—	—	−350	nA
Total Input Offset Voltage, Note 4	V_{off}	−60	—	20	mV
Transconductance $\left(\frac{\Delta I_{Pin\ 16}}{V_{Pin\ 4} - V_{Pin\ 7}}\right)$	g_m	—	300	—	μA/V
Output Current Swing	$I_{Pin\ 16}$	—	±100	—	μA
FREQUENCY/VOLTAGE CONVERTER					
Input Signal Low Voltage, Note 5	V_{L12}	−0.1	—	—	V
Input Signal High Voltage	V_{H12}	0.1	—	5.0	V
Polarization Current	$I_{Pin\ 12}$	—	−25	—	μA
Conversion Rate, Note 6*	K_C	—	15	—	mV/Hz
Linearity* (Figure 3)	K_L	—	±4.0	—	%
TRIGGER PULSE GENERATOR					
Voltage Synchronization Levels	$I_{Pin\ 2}$	—	±50	—	μA
Current Synchronization Levels	$I_{Pin\ 1}$	—	±50	—	μA
Input Voltage Swing (for full angle swing)	V	—	11.7	—	V
Trigger Pulse Width, Note 7	t_p	—	55	—	μs
Trigger Pulse Repetition Period	t	—	215	—	μs
Trigger Pulse High Level ($I_{Pin\ 13}$ = 150 mA)	$V_{Pin\ 13}$	$V_{CC}-4$	—	—	V
Output Leakage Current ($V_{Pin\ 13}$ = 0 V)	$I_{oPin\ 13}$	—	—	30	μA

4. V_{off} is defined as being the voltage difference between Pin 5 and 4 with no current flow on Pin 16.
5. The negative swing is clamped to −0.3 V.
6. $V_{Pin\ 4} = k \cdot C_{Pin\ 11} \cdot (V_{CC} - V_a) \cdot R_{Pin\ 4} \cdot \left(1 + \frac{180 \times 10^3}{R_{Pin\ 11}}\right) \cdot 1 \cdot \text{freq in.}$
   Where: $9 < K < 13$ & V_a = 1.3 V.
7. The timing given is when $C_{Pin\ 14}$ = 47 nF.

* These figures apply for the application shown in Figure 4.

INPUT/OUTPUT FUNCTIONS

VOLTAGE REGULATOR — (Pins 8, 9, 10). This is a parallel type voltage regulator able to sink a large amount of current while offering good regulation characteristics.

A resistor between Pins 9 and 10 reduces the internal power dissipation. Under minimal current sink conditions (min. current from the unregulated supply, max. consumption by the circuitry), at least 1.0 mA should flow through this resistor. Under max. sink conditions (max. current from the unregulated supply, min. consumption by the circuitry), the maximum resistor value is chosen so that the voltage at Pin 10 falls towards 3.0 V, but not lower. The above, fixed dynamic range of the regulator must not be exceeded within one line cycle.

A power supply failure causes shutdown.

For operation from an externally regulated voltage, Pin 10 is not connected.

SPEED SENSING — (Pins 4, 11, 12). Speed sensing can be achieved either digitally (tachogenerator frequency) or analogically (tachogenerator amplitude).

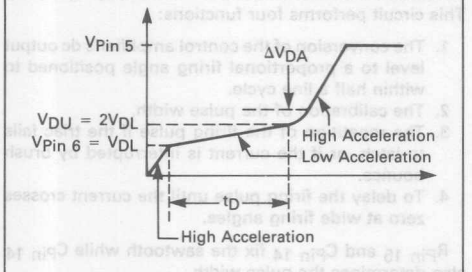
For digital sensing, a bipolar signal with respect to ground is applied to Pin 12. During positive excursions $C_{Pin\ 11}$ is charged. An internal mirror delivers ten times the charge on $C_{Pin\ 11}$ via Pin 4. However, due to internal circuitry, the charge on Pin 4 can vary in the region of 9 to 13 times the charge on $C_{Pin\ 11}$. For that reason it is necessary to calibrate the Frequency/Voltage Convertor (F/VC) with a variable resistor on Pin 4. Thus the relationship between speed and $V_{Pin\ 4}$ is defined by $R_{Pin\ 4}$ and $C_{Pin\ 11}$.

To maintain linearity in the high speed ranges it is important that $C_{Pin\ 11}$ is fully charged across an equivalent resistor of about 180 kΩ. It should be borne in mind that the impedance on Pin 11 should be kept as low as possible as $C_{Pin\ 11}$ has a large influence on the temperature coefficient of the FV/C. The time constant on Pin 4 should also be kept as low as possible.

Pin 12 is also an impedance monitoring input; at high impedances $V_{Pin\ 12}$ increases. Should $V_{Pin\ 12}$ exceed 5.0 V the triac trigger pulses are inhibited and the circuit resets.

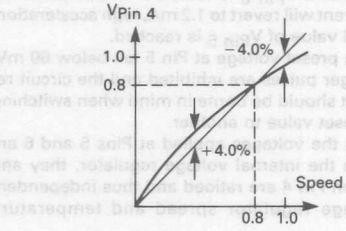
A 470 kΩ resistor from Pin 11 to $+V_{CC}$ significantly reduces the leakage current and reduces the device temperature coefficient to almost zero.

FIGURE 2 — RAMP GENERATOR TRANSFER CHARACTERISTIC



The shape of the curve is determined by $CR_{Pin\ 7}$; where $C_{Pin\ 7}$ defines the high acceleration slope and $R_{Pin\ 7}$ defines that of the low acceleration.

FIGURE 3 — FREQUENCY/VOLTAGE CONVERTER OUTPUT CHARACTERISTIC



4

INPUT/OUTPUT FUNCTIONS (continued)

For analog sensing input 12 should be grounded and a positive signal, with respect to ground, Pin 8, applied to Pin 4.

RAMP GENERATOR — (Pins 5, 6, 7) (refer to Figure 2). A preset voltage applied to Pin 5 will initiate the generation of a ramp whose final value is determined by the voltage applied to Pin 5. The voltage applied to Pin 6 will determine how much of the full ramp, shown in Figure 2, is used. The charging current passing through Pin 7 to the ramp generator timing capacitor determines the ramp slope.

When Pin 6 is held at $-V_{CC}$ a charging current of 1.2 mA is delivered to Pin 7, regardless of the voltage of Pin 5. This represents the high acceleration period shown in Figure 2.

If the preset voltage applied to Pin 5 is equal to or less than the voltage on Pin 6 the charging current will be 1.2 mA, or high acceleration.

If the preset voltage applied to Pin 5 is between $V_{Pin\ 6}$ and 2 $V_{Pin\ 6}$ the charging current is 1.2 mA (high acceleration) until the voltage at the reference input of the control amplifier equals $V_{Pin\ 6}$. At this point the charging current will switch to 5.0 μA; i.e. low acceleration.

If the preset voltage applied to Pin 5 is greater than 2 $V_{Pin\ 6}$ the charging current will be 1.2 mA (high acceleration) until the control amplifier's reference input reaches $V_{Pin\ 6}$ when it will switch to 5.0 μA (low acceleration) until 2 $V_{Pin\ 6}$ is reached. At this point the charging current will revert to 1.2 mA, high acceleration, until the final value of $V_{Pin\ 5}$ is reached.

Should the preset voltage at Pin 5 fall below 80 mV, the triac trigger pulses are inhibited and the circuit resets. This fact should be borne in mind when switching from one preset value to another.

As long as the voltages applied at Pins 5 and 6 are derived from the internal voltage regulator, they and the voltage on Pin 4 are ratioed and thus independent of the voltage regulator spread and temperature coefficient.

CURRENT LIMITER — (Pin 3). Safe operation of the motor and triac under all conditions is ensured by reducing the motor speed if a preset current limit is exceeded.

This is achieved as follows: The motor current will set up an alternating current, consisting of positive and negative peaks through the shunt resistor (0.05 Ω in Figure 4).

The negative peaks of this current are fed through a resistor to Pin 3 where they are compared with a preset current defined by a resistor between Pin 3 and $+V_{CC}$. An excessive shunt current will try to pull Pin 3 below $-V_{CC}$, but the current limiter becomes active at this point and reduces the charge on $C_{Pin\ 7}$, consequently reducing the motor speed.

Thus the value of the shunt and the ratio of the two resistors to Pin 3 fix the level at which the limiter becomes active, while the parallel equivalent of the two resistors determines the magnitude of the discharge current and thus how rapidly the circuit responds to an overcurrent condition.

CONTROL AMPLIFIER — (Pin 16). Connected to this pin is a network which compensates electrically for the mechanical characteristics of the motor and its load to give the circuit optimum closed loop stability and transient response.

The component values are best determined empirically by connecting R and C substitution boxes and looking for the best results.

TRIGGER PULSE GENERATOR — (Pins 1, 2, 13, 14, 15). This circuit performs four functions:

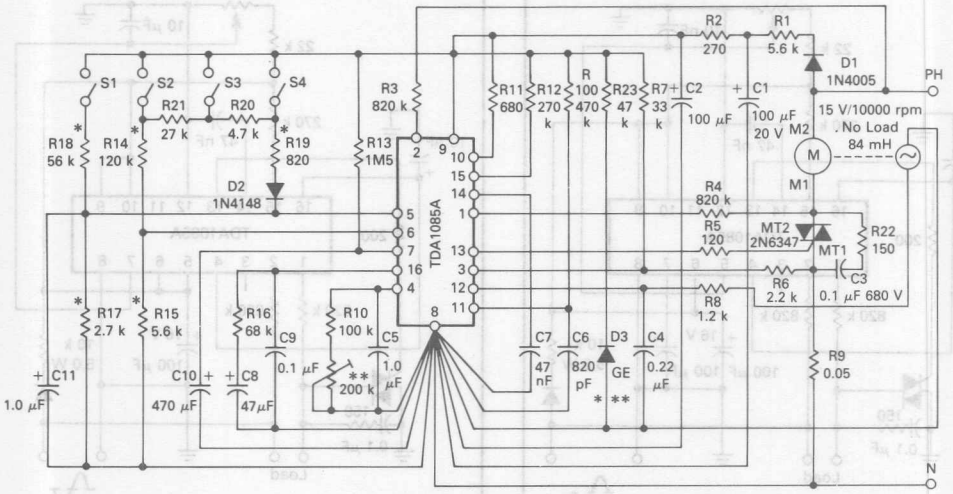
1. The conversion of the control amplifier's dc output level to a proportional firing angle positioned to within half a line cycle.
2. The calibration of the pulse width.
3. The repetition of the firing pulse if the triac fails to latch, or if the current is interrupted by brush bounce.
4. To delay the firing pulse until the current crosses zero at wide firing angles.

$R_{Pin\ 15}$ and $C_{Pin\ 14}$ fix the sawtooth while $C_{Pin\ 14}$ also determines the pulse width.

Pin 13 is the trigger pulse output. A current limiting resistor is essential on this pin. This configuration will drive two thyristors controlling a bridge if the supply for the speed controller is isolated.

TYPICAL APPLICATIONS

FIGURE 4 — CLOSED LOOP, FULLY PROGRAMMED, MULTI-SPEED SYSTEM WITH CURRENT LIMITING



* Chosen to suit the speeds required
** Adjust for the highest speed
*** Required only with 'A' suffix device

Speed Control Resistor Network Equations

R17	=	given
R18	=	$R17\left(\frac{15.5\ V}{V_W} - 1\right)$
R19	=	$R17\left(\frac{14.8\ V}{V_{spin\ 2}} - 1\right)$
R20	=	$R17\left(\frac{14.8\ V}{V_{spin\ 1}} - 1\right) - R19$
R21	=	$R17\left(\frac{14.8\ V}{k.V_W} - 1\right) - R19 - R20$
R15	=	$R21\left(\frac{K.V_W}{15.5\ V\ (2\text{-}K)}\right)$
R14	=	$R15\left(\frac{15.5\ V}{V_W} - 1\right)$

The ratio distribute speed to wash speed can be chosen as:

$$\frac{V_{DIST}}{V_{WASH}} \leq 2 = K$$

	S1	S2	S3	S4	$V_{Pin\ 5}$	$V_{Pin\ 6}$
Wash	sc	oc	oc	oc	V_W	0
Distribute	oc	sc	oc	oc	KV_W	V_W
Spin 1	oc	oc	sc	oc	$>KV_W$	$\frac{K}{2}V_W$
Spin 2	oc	oc	oc	sc	$>>KV_W$	$\simeq\frac{K}{2}V_W$

sc = switch closed
oc = switch open

Note:
When changing from one speed to another $V_{Pin\ 5}$ must not be allowed to fall below 80 mV — otherwise the circuit will reset and restart from zero.

The component values given in Figure 4 correspond to:

V_W = 0.7 V
V_D = 1.13 V
$V_{spin\ 1}$ = 5.0 V
$V_{spin\ 2}$ = 11 V
K = 1.6

4

FIGURE 5 — OPEN LOOP, SOFT START — WITH PROGRAMMED TIME TO MAX. SPEED
($t = C_{Pin\ 7} \cdot 65 \times 10^5$)

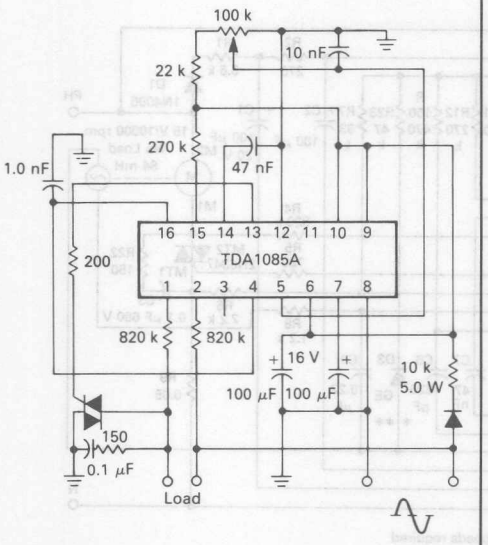
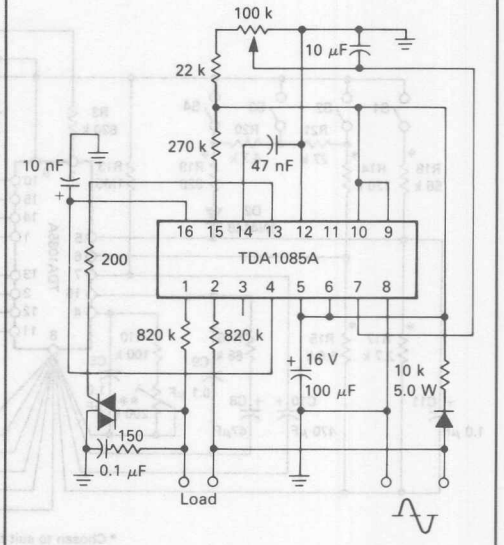


FIGURE 6 — OPEN LOOP, SOFT-START/SOFT-STOP, LIGHTING/INDUCTIVE LOAD CONTROLLER



MOTOROLA

TDA1085C

Designer's Data Sheet

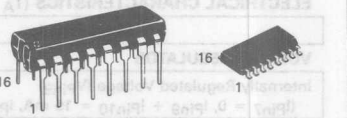
UNIVERSAL MOTOR SPEED CONTROLLER

The TDA1085C is a phase angle triac controller having all the necessary functions for universal motor speed control in washing machines. It operates in closed loop configuration and provides two ramps possibilities.

- On-Chip Frequency to Voltage Converter
- On-Chip Ramps Generator
- Soft Start
- Load Current Limitation
- Tachogenerator Circuit Sensing
- Direct Supply from AC Line
- Security Functions Performed by Monitor

UNIVERSAL MOTOR SPEED CONTROLLER

LINEAR INTEGRATED CIRCUIT

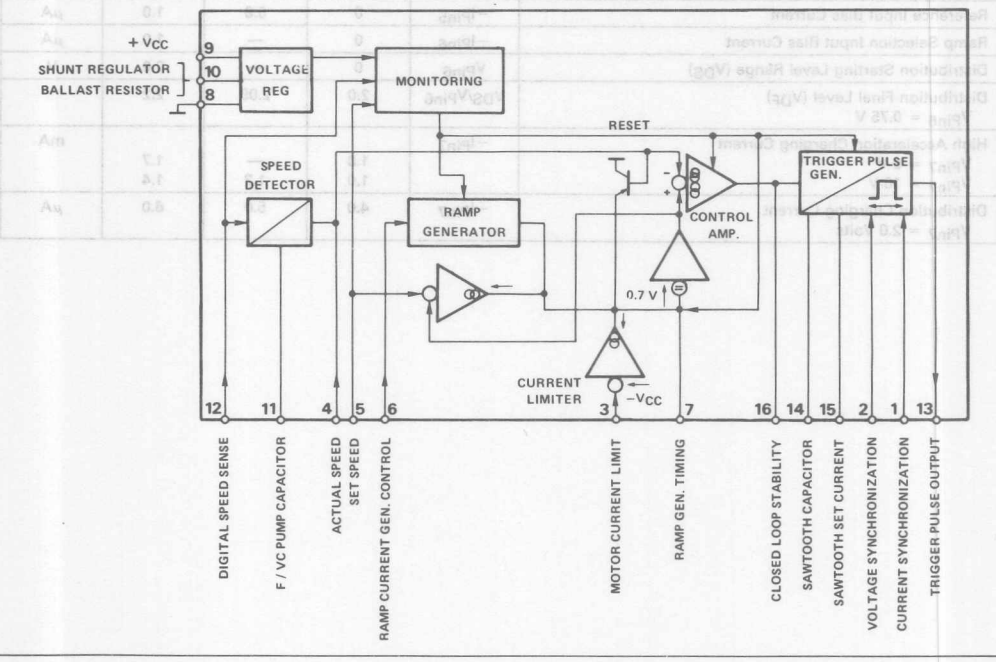


P SUFFIX
PLASTIC PACKAGE
CASE 648-06

D SUFFIX
PLASTIC PACKAGE
CASE 751B-03
SO-16

4

FIGURE 1 – BLOCK DIAGRAM AND PIN ASSIGNMENT



MAXIMUM RATINGS (T_A = 25°C, Voltages are referred to pin 8 [Ground])

Rating	Symbol	Value	Unit
Power Supply, when externally regulated, V_{Pin9}	V_{CC}	15	V
Maximum Voltage per listed pin Pin 3 Pin 4-5-6-7-13-14-16 Pin 10	V_{pin}	 +5.0 0 to +V_{CC} 0 to +17	V
Maximum Current per listed pin Pin 1 and 2 Pin 3 Pin 9 (V_{CC}) Pin 10 shunt regulator Pin 12 Pin 13	I_{pin}	 −3.0 to +3.0 −1.0 to +0 15 35 −1.0 to +1.0 −200	mA
Maximum Power Dissipation	P_D	1.0	W
Junction to Air Thermal Resistance	$R_{\theta JA}$	65	°C/W
Operating Junction Temperature	T_A	−10 to +120	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
VOLTAGE REGULATOR					
Internally Regulated Voltage (V_{Pin9}) (I_{Pin7} = 0, I_{Pin9} + I_{Pin10} = 15 mA, I_{Pin13} = 0)	V_{CC}	15	15.3	15.6	V
V_{CC} Temperature Factor	TF	—	−100	—	ppm/°C
Current Consumption (I_{Pin9}) (V_9 = 15 V, V_{12} = V_8 = 0, I_1 = I_2 = 100 μA, all other pins not connected)	I_{CC}	—	4.5	6.0	mA
V_{CC} Monitoring Enabling Level Disable Level	V_{CC} EN V_{CC} DIS	— —	V_{CC} − 0.4 V_{CC} − 1.0	— —	V
RAMP GENERATOR					
Reference Speed Input Voltage Range	V_{Pin5}	0.08	—	13.5	V
Reference Input Bias Current	$-I_{Pin5}$	0	0.8	1.0	μA
Ramp Selection Input Bias Current	$-I_{Pin6}$	0	—	1.0	μA
Distribution Starting Level Range (V_{DS})	V_{Pin6}	0	—	2.0	V
Distribution Final Level (V_{DF}) V_{Pin6} = 0.75 V	V_{DS}/V_{Pin6}	2.0	2.09	2.2	
High Acceleration Charging Current V_{Pin7} = 0 V V_{Pin7} = 10 V	$-I_{Pin7}$	 1.0 1.0	 — 1.2	 1.7 1.4	mA
Distribution Charging Current V_{Pin7} = 2.0 Volts	$-I_{Pin7}$	4.0	5.0	6.0	μA

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
CURRENT LIMITER					
Limiter Current Gain — I_{Pin7}/I_{Pin3} (I_{Pin3} = −300 μA)	C_g	130	180	250	
Detection Threshold Voltage I_{Pin3} = −10 μA	$V_{Pin3\ TH}$	50	65	80	mV
FREQUENCY TO VOLTAGE CONVERTER					
Input Signal "Low Voltage"	$V_{12\ L}$	−100	—	—	mV
Input Signal "High Voltage"	$V_{12\ H}$	+100	—	—	mV
Monitoring Reset Voltage	$V_{12\ R}$	5.0	—	—	V
Negative Clamping Voltage I_{Pin12} = −200 μA	$-V_{12\ CL}$	—	0.6	—	V
Input Bias Current	$-I_{Pin12}$	—	25	—	μA
Internal Current Source Gain $G = \frac{I_{Pin4}}{I_{Pin11}}$, $V_{Pin4} = V_{Pin11} = 0$	G.0	10	10.3	10.5	
Gain Linearity versus Voltage on Pin 4 ($G_{8.6}$ = Gain for V_{Pin4} = 8.6 Volts)	$G/G_{8.6}$				
V_4 = 0 V		1.04	1.05	1.06	
V_4 = 4.3 V		1.015	1.025	1.035	
V_4 = 12 V		0.965	0.975	0.985	
Gain Temperature Effect (V_{Pin4} = 0)	TF	—	350	—	ppm/°C
Output Leakage Current (I_{Pin11} = 0)	$-I_{Pin4}$	0	—	100	nA
CONTROL AMPLIFIER					
Actual Speed Input Voltage Range	V_{Pin4}	0	—	13.5	V
Input Offset Voltage $V_{Pin5} - V_{Pin4}$ (I_{Pin16} = 0, V_{Pin16} = 3.0 and 8.0 Volts)	V_{off}	0	—	50	mV
Amplifier Transconductance ($I_{Pin16}/\Delta\ (V_5 - V_4)$ (I_{Pin16} = + and −50 μA, V_{Pin16} = 3.0 Volts)	T	270	340	400	μA/V
Output Current Swing Capability	I_{Pin16}				μA
Source		−200	−100	−50	
Sink		50	100	200	
Output Saturation Voltage	$V_{16\ sat}$	—	—	0.8	V
TRIGGER PULSE GENERATOR					
Synchronization Level Currents					μA
Voltage Line Sensing	I_{Pin2}	—	±50	±100	
Triac Sensing	I_{Pin1}	—	±50	±100	
Trigger Pulse Duration (C_{Pin14} = 47 nF, R_{Pin15} = 270 kΩ)	T_p	—	55	—	μs
Trigger Pulse Repetition Period, conditions as a.m.	T_R	—	220	—	μs
Output Pulse Current $V_{Pin13} = V_{CC}$ −4.0 Volts	$-I_{Pin13}$	180	192	—	mA
Output Leakage Current V_{Pin13} = −3.0 Volts	$I_{13\ L}$	—	—	30	μA
Full Angle Conduction Input Voltage	V_{14}	—	11.7	—	V
Saw Tooth "High" Level Voltage	$V_{14\ H}$	12	—	12.7	V
Saw Tooth Discharge Current, I_{Pin15} = 100 μA	I_{Pin14}	95	—	105	μA

4

The TDA 1085C triggers a triac accordingly to the speed regulation requirements. Motor speed is digitally sensed by a tachogenerator and then converted into an analog voltage.

The speed set is externally fixed and is applied to the internal linear regulation input after having been submitted to programmable acceleration ramps. The overall result consists in a full motor speed range with two acceleration ramps which allow efficient washing machine control (Distribute function).

Additionnally, the TDA 1085C protects the whole system against AC line stop or variations, overcurrent in the motor and tachogenerator failure.

4

INPUT/OUTPUT FUNCTIONS
(Referred to Figures 1 and 8)

VOLTAGE REGULATOR – (pins 9 and 10) This is a parallel type regulator able to sink a large amount of current and offering good characteristics. Current flow is provided from AC line by external dropping resistors R1, R2, and rectifier: This half wave current is used to feed a smoothering capacitor, the voltage of which is checked by the IC.

When V_{CC} is reached, the excess of current is derived by another dropping resistor R10 and by pin 10. These three resistors must be determined in order:

- to let 1mA flow through pin 10 when AC line is minimum and V_{CC} consumption is maximum (fast ramps and pulses present).
- to let V_{10} reach 3V when AC line provides maximum current and V_{CC} consumption is minimum (no ramps and no pulses).
- all along the main line cycle, the pin 10 dynamic range must not be exceeded unless loss of regulation.

An AC line supply failure would cause shut down.

The double capacitive filter built with R_1 and R_2 gives an efficient V_{CC} smoothing and helps to remove noise from set speeds.

SPEED SENSING – (pins 4-11-12) The IC is compatible with an external analog speed sensing: its output must be applied to pin 4, and pin 12 connected to pin 8.

In most of the applications it is more convenient to use a digital speed sensing with an unexpensive tachogenerator which doesn't need any tuning. During every positive cycle at pin 12, the capacitor $C_{pin\ 11}$ is charged to almost V_{CC} and during this time, pin 4 delivers a current which is 10 time the one charging $C_{pin\ 11}$. The current source gain is called G and is tightly specified, but nevertheless requires an adjustment on $R_{pin\ 4}$. The current into this resistor is proportional to $C_{pin\ 11}$ and to the motor speed; being filtered by a capacitor, $V_{pin\ 4}$ becomes smoothered and represents the "true actual motor speed".

To maintain linearity into the high speed range, it is important to verify that $C_{pin\ 11}$ is fully charged: the internal source on pin 11 has 100 KΩ impedance. Nevertheless $C_{pin\ 11}$ has to be as high as possible as it has a large influence on FV/C temperature factor. A 470 KΩ resistor between pins 11 and 9 reduces leakage currents and temperature factor as well, down to neglectable effects.

It also senses the tachogenerator continuity and in case of any circuit aperture, it inhibits pulse, avoiding the motor to run out of control. In the TDA 1085C, pin 12 is negatively clamped by an internal diode which removes the necessity of the external one used in the former circuit.

RAMP GENERATOR – (pins 5-6-7) The true Set Speed value taken in consideration by the regulation is the output of the ramp generator (pin 7). With a given value of speed set input (pin 5), the ramp generator charges an external capacitor $C_{pin\ 7}$ up to the moment $V_{pin\ 5}$ (set speed) equals $V_{pin\ 4}$ (true speed), see fig. 2. The IC has an internal charging current source of 1.2mA and delivers it from 0 to 12 V at pin 7. It is the high acceleration ramp (5 seconds typ.) which allows rapid motor speed changes without excessive strains on the mechanics. The TDA 1085C offers in addition the possibility to break this high acceleration with the introduction of a low acceleration ramp (called Distribution) by reducing the pin 7 source current down to 5 μA under pin 6 full control, as shown by following conditions:

- Presence of high acceleration ramp $V_{pin\ 5} > V_{pin\ 4}$
- Distribution occurs in the $V_{pin\ 4}$ range (true motor speed) defined by $V_{pin\ 6} \leqq V_{pin\ 4} \leqq 2V_{pin\ 6}$

For two fixed values of $V_{pin\ 5}$ and $V_{pin\ 6}$, the motor speed will have high acceleration, excluding the time for $V_{pin\ 4}$ to go from $V_{pin\ 6}$ to two times this value, high acceleration again, up to the moment the motor has reached the set speed value, at which it will stay, see fig. 3.

Should a reset happen (whatever the cause would be), the above mentionned successive ramps will be fully reprocessed from 0 to the max. speed. If $V_{pin\ 6} = 0$, only the high acceleration ramp occurs.

To get a real zero speed position, pin 5 has been designed in such a way that its voltage from 0 to 80 mV is interpreted as a true zero. As a consequence, when changing the speed set position, the designer must be sure that any transient zero would not occur: if any, the entire circuit will be reset.

As the voltages applied by pins 5 and 6, are derived from the internal voltage regulator supply and pin 4 voltage is also derived from the same source, motor speed, which is determined by the ratios between above mentioned voltages, is totally independent from V_{CC} variations and temperature factor.

CONTROL AMPLIFIER – (pin 16) It amplifies the difference between true speed (pin 4) and set speed (pin 5), through the ramp generator. Its output available at pin 16 is a double sense current source with a max. capability of ± 100 μA and a specified transconductance (340 μA/v.typ.). Pin 16 drives directly the trigger pulse generator, and must be loaded by an electrical network which compensates the mechanical characteristics of the motor and its load, in order to provide stability in any condition and shortest transient response, see fig. 4.

This network must be adjusted experimentally.

In case of a periodic torque variations, pin 16 provides directly the phase angle oscillations.

TRIGGER PULSE GENERATOR – (pins 5 1-2-13-14-15)
This circuit performs four functions:

- The conversion of the control amplifier DC output level to a proportionnal firing angle at every main line half cycle.
- The calibration of pulse duration.
- The repetition of the pulse if the triac fails to latch on if the current has been interrupted by brush bounce.
- The delay of firing pulse until the current crosses zero at wide firing angles and inductive loads.

$R_{pin\ 15}$ programs the pin 14 discharging current. Saw-tooth signal is then fully determined by R15 and C14 (usually 47 nF). Firing pulse duration and repetition period are in inverse ratio to the saw-tooth slope.

Pin 13 is the pulse output and an external limiting resistor is mandatory. Max current capability is 200 mA.

CURRENT LIMITER – (pin 3) Safe operation of the motor and triac under all conditions is ensured by limiting the peak current. The motor current develops an alternative voltage in the shunt resistor (0.05 ohm in fig. 4). The negative half waves are transferred to pin 3 which is positively preset at a voltage determined by resistors R_3 and R_4. As motor current increases, the dynamical voltage range of pin 3 increases and when pin 3 becomes slightly negative in respect of pin 8 a current starts to circulate in it. This current, amplified typically 180 times, is then used to discharge pin 7 capacitor and, as a result, reduces firing angle down to a value where an equilibrium is reached. The choice of resistors R_3, R_4 and shunt determines the magnitude of the discharge current signals on C_{pin7}.

Notice that the current limiter acts only on peak Triac current.

APPLICATION NOTES
(Referred to Figure 4)

PRINTED CIRCUIT LAYOUT RULES
In the common applications, where TDA1085C is used, there is on the same board, presence of high voltage, high currents as well as low voltage signals where millivolts count. It is of first magnitude importance to separate them each other and to respect following rules:

- Capacitors decoupling pins which are the inputs of the same comparator, must be physically close to the IC, close to each other and grounded in the same point.
- Ground connexion for tachogenerator must be directly connected to pin 8 and should ground only the tacho. In effect the latter is a first magnitude noise generator due to its proximity of the motor which induces high $d\phi/dt$ signals.
- The ground pattern must be in the "star style", in order to fully eliminate power currents flowing in the ground network devoted to capacitors decoupling sensitive pins: (4-5-7-11-12-14-16).

As an example, fig. 5 presents a PC board pattern which concerns the group of sensitive pins and their associated capacitors into which the a.m. rules have been implemented. Notice the full separation of "Signal World" from "Power" one by line AB and their communication by a unique strip.

These rules will lead to much satisfactory volume production in the sense that speed adjustment will stay valid in the entire speed range.

POWER SUPPPLY
As dropping resistor dissipates noticeable power, it is necessary to reduce the I_{CC} needs down to a minimum. Triggering pulses, if a certain number of repetition is in reserve to cope with motor brush wearing at end of its life, are the largest I_{CC} user. Classical worst case configuration have to be considered to select dropping resistor. In addition the parallel regulator must be always into its dynamic range, i.e. $I_{pin\ 10}$ over 1 mA and $V_{pin\ 10}$ over 3 volt in any extreme configuraton. The double filtering cell is mandatory.

TACHOGENERATOR CIRCUIT
The tacho signal voltage is proportional to the motor speed. Stability considerations, in addition, require a RC filter the pole of which must be looked at. The combination of both elements yield a constant amplitude signal on pin 12 in most of the speed range. It is recommended to verify this maximum amplitude to be within 1 volt peak in order to have the largest signal/noise ratio without resetting the integrated circuit (which occurs if $V_{pin\ 12}$ reaches 5.5 V). It must be also verified that the pin 12 signal is approximately balanced between "High" (over 300 mV) and "Low". A 8 poles tacho is a minimum for low speed stability and a 16 poles is even better.

The RC pole of the tacho circuit should be chosen within 30 Hz in order to be as far as possible from the 150 Hz which corresponds to the AC line 3rd harmonic generated by the motor during starting procedure. In addition, a high value resistor coming from V_{CC} introduces a positive offset at pin 12, removes noise to be interpreted as a tacho signal. This offset should be designed in order to let pin 12 to reach at least – 200 mV (negative voltage) at the lowest motor speed. We remember the necessity of an individual tacho ground connection.

FREQUENCY TO VOLTAGE CONVERTER – F V/C
$C_{pin\ 11}$ has a recommended value of 820 pF for 8 poles tachos and max. motor rpm of 15000, and $R_{pin\ 11}$ must be always 470 K.

$R_{pin\ 4}$ should be choosen to deliver within 12 volts at maximum motor speed in order to maximize signal/noise ratio. As the FV/C ratio as well as the $C_{pin\ 11}$ value are dispersed, $R_{pin\ 4}$ must be adjustable and should be made of a fixed resistor in serie with a trimmer representing 25% of the total. Adjustment would become easier.

Once adjusted, for instance at maximum motor speed, the F V/C presents a residual non linearity; the conversion factor (mV per R.P.M.) increases by within 7.7% as speed tends to zero. The guaranteed dispersion of the latter being very narrow, a maximum 1% speed error is guaranteed if during pin 5 network design the small set values are modified, once for ever, according this increase.

The following formulae gives $V_{pin\ 4}$:

$$V_{pin4} = 140 \cdot C_{pin11} \cdot R_4 \cdot f \cdot \frac{1}{(1 + \frac{180\ k}{R_{pin11}})} \text{ in volt per Hertz.}$$

SPEED SET – (pin 5) Upon designer choice, a set of external resistors apply a serie of various voltages corresponding to the various motor speeds. When switching external resistors, verify that a voltage below 80 mV in never applied to pin 5, if no, a full circuit reset will occur.

RAMPS GENERATOR — (pin 6) If only a high acceleration ramp is needed, connect pin 6 to ground.

When a Distribute ramp should occur, pre-set a voltage on pin 6 to which corresponds the motor speed starting ramp point. Distribution (or low ramp) will continue up to the moment the motor speed would have reached twice the starting value.

The ratio of two is imposed by the IC. Nevertheless it could be externally changed downwards (fig. 6) or upwards (fig. 7).

The distribution ramp can be shortened by an external resistor from V_{CC} charging $C_{pin\ 7}$, adding its current to the internal 5 µA generator.

POWER CIRCUITS

Triac Triggering pulse amplitude must be determined by Pin 13 resistor according the needs in Quadrant IV. Trigger pulses duration can be disturbed by noise signals, generated by the triac itself, which interfere within pins 14 and 16, precisely those which determine it. While easily visible this effect is harmless.

Triac must be protected from high AC line dV/dt during external disturbances by 100 nF × 100 Ω network.

Shunt resistor must be as non selfic as possible. It can be made locally by Constantan alloy wiring.

When the load is a DC fed universal motor through a rectifier bridge, the triac must be protected from commutating dV/dt by a 1 to 2 mH coil in serie with MT_2.

Synchronisation functions are performed by resistors sensing AC line and triac conduction. 820 K values are usual but could be reduced down to 330 K in order to detect the Zeros with accuracy and to reduce the residual DC line component below 20 mA.

CURRENT LIMITATION

The current limiter starts to discharge pin 7 capacitor (reference speed) as Motor current reaches the designed threshold level. The loop gain is determined by the resistor connecting pin 3 to the serie shunt. Experience has shown that its optimal value for a 10 A rms limitation is within 2 KΩ. Pin 3 input has a sensitivity in current which is limited to reasonable values and should not react to spikes.

If not used, pin 3 must be connected to a max. positive voltage of 5 V rather to be left open.

LOOP STABILITY

The pin 16 network is predominant and must be adjusted experimentally during module development. The values indicated in fig. 4 are typical for washing machines applications but accept large modifications from one model to another. R16, it is the sole restriction, should not be below 33 k otherwise slew rate limitation will cause large transient errors for load steps.

FIGURE 2 — ACCELERATION RAMP

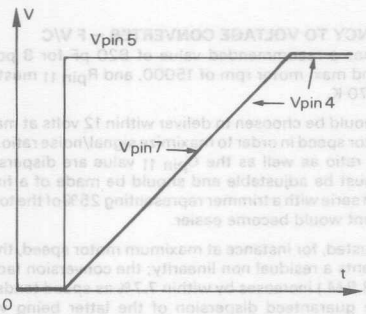


FIGURE 3 — PROGRAMMABLE DOUBLE ACCELERATION RAMP

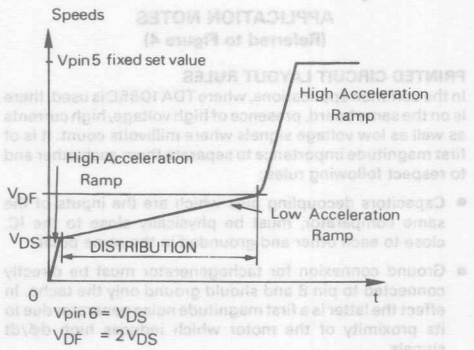
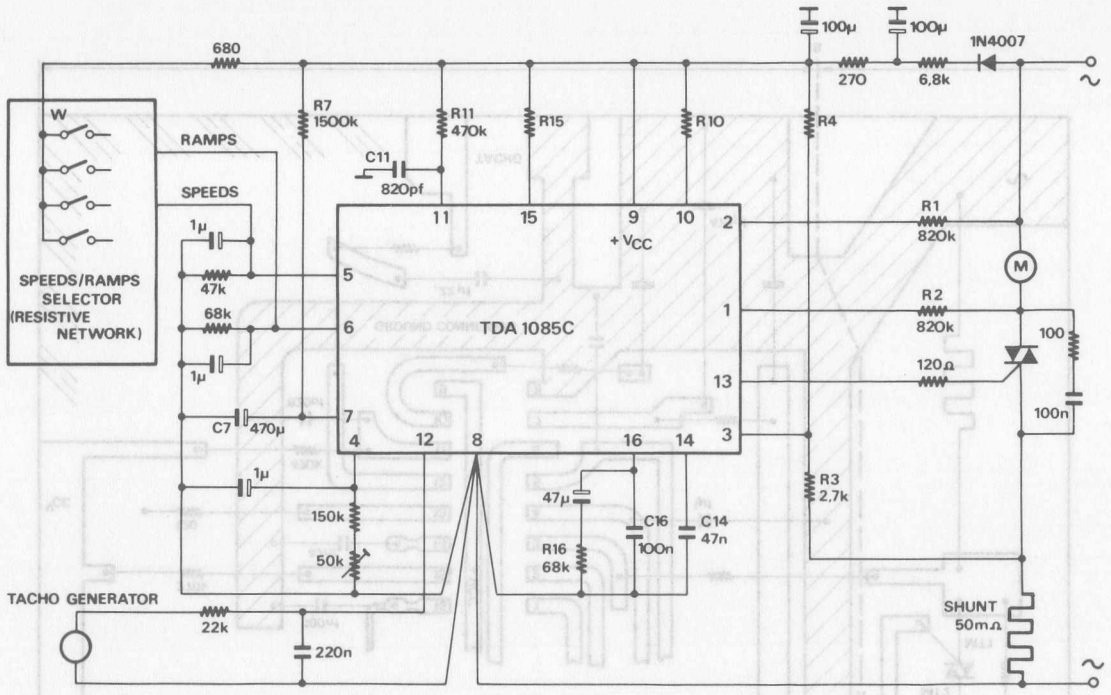


FIGURE 4 – BASIC APPLICATION CIRCUIT



Current limitation: 10 A adjusted by R_4 experimentally

Ramps High acceleration: 3200 rpm per second

Distribution ramp: 10 s from 850 to 1300 rpm

Speeds:	Pin 5 voltage Set:	
Wash 800 rpm	609 mV	Including non linearity corrections
Distribution 1300	996 mV	Including non linearity corrections
Spin 1 : 7500	5,912 V	Including non linearity corrections
Spin 2 : 15 000	12,000V	Adjustment point

Motor Speed Range: 0 to 15 000 rpm

Tachogenerator 8 poles
delivering 30 v peak to peak at 6000 rpm, in open circuit

FV/C Factor: · 8 mV per rpm (12 v full speed) C_{pin11} = 680 pF V_{cc} = 15.3 v

Triac MAC 15 A-8 15 A 600 v
Igt min = 90 mA to cover Quad. IV at – 10 °C

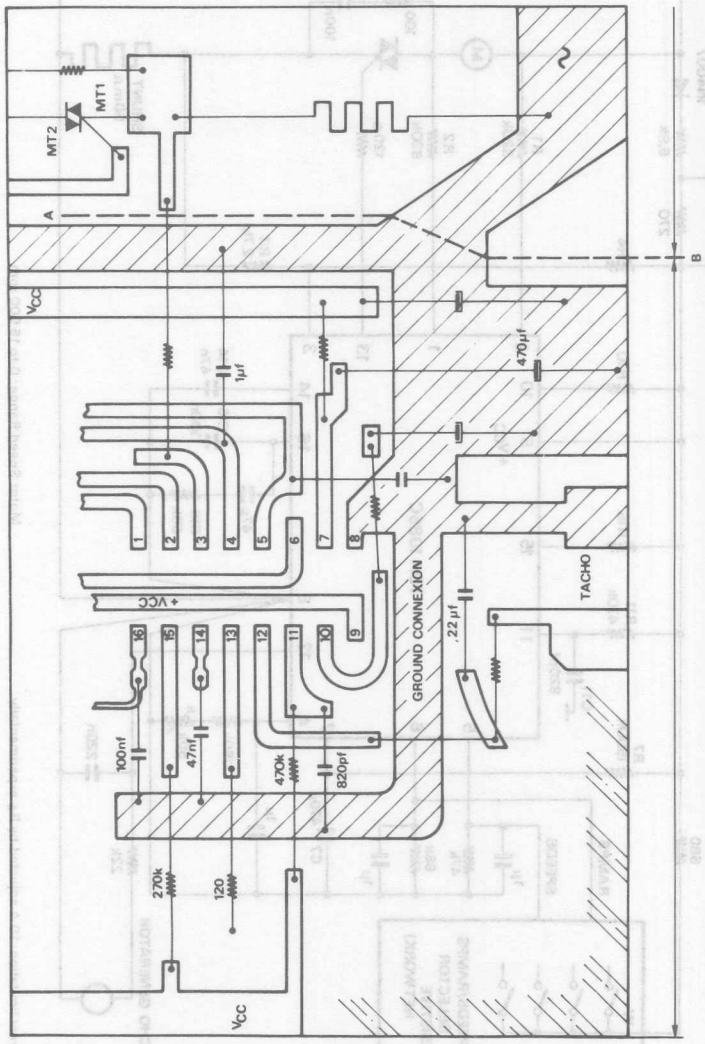


FIGURE 5 – PC BOARD PATERN

FIGURE 6 – DISTRIBUTION SPEED k < 2

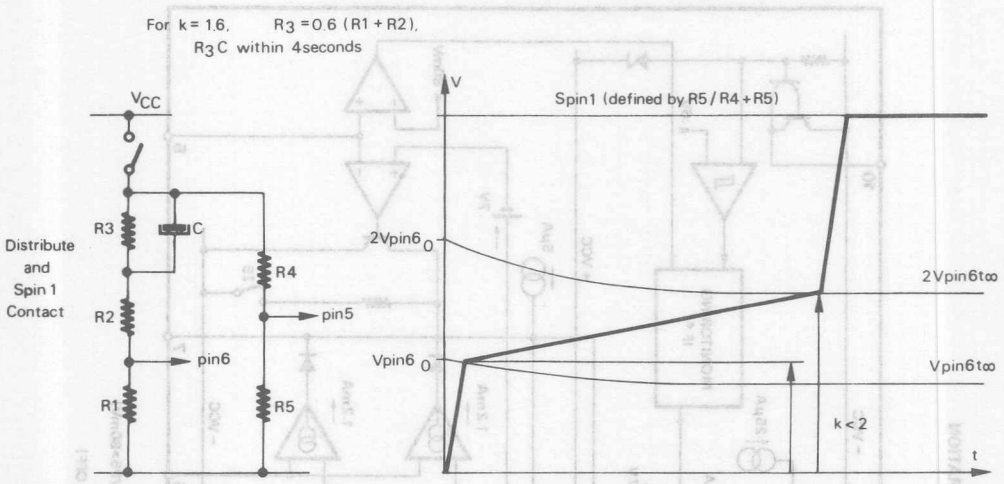
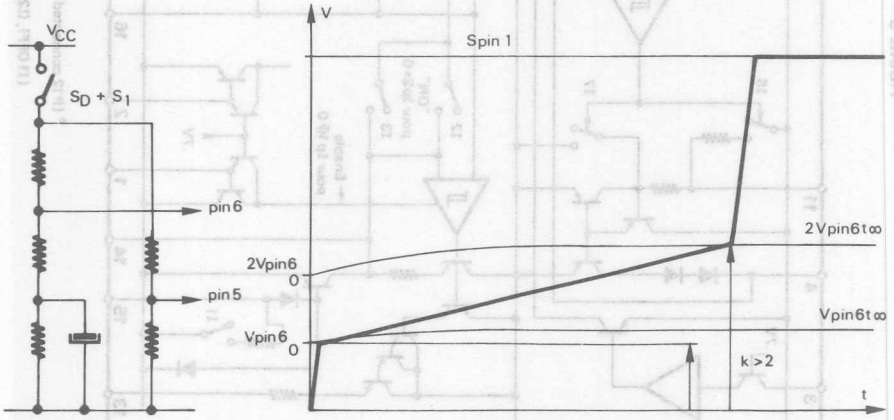


FIGURE 7 – DISTRIBUTON SPEED k > 2



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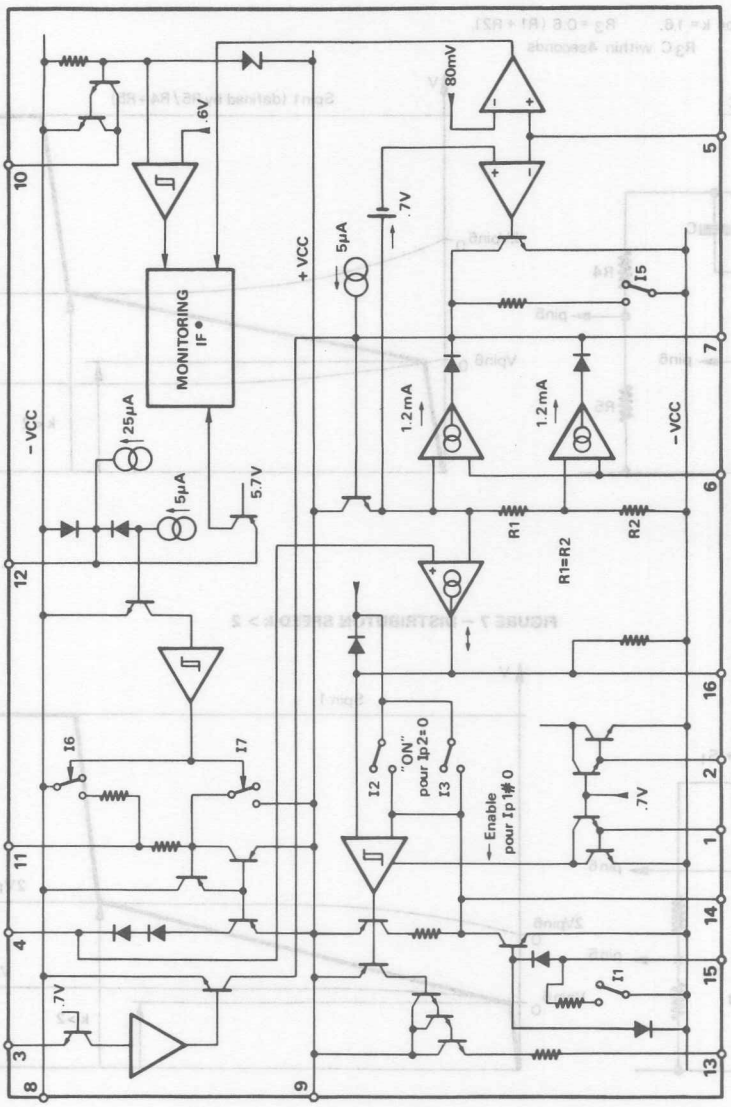


FIGURE 8 – INTERNAL CONFIGURATION

• (P12 connected) AND (VCC OK) AND (VP5>80mV)
THEN
(I1 OFF), (I2 OFF), (I4 OFF) AND (I5 OFF)

MOTOROLA

TDA1185A

Specifications and Applications Information

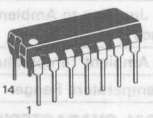
TRIAC PHASE ANGLE CONTROLLER

The TDA1185A generates controlled triac triggering pulses and allows tacholess speed stabilization of universal motors by an integrated positive feedback function. Typical applications are power hand tools, vacuum cleaners, mixers and other small appliances.

- Low Cost External Components Count
- Optimum Triac Firing (2nd and 3rd Quadrants)
- Repetitive Trigger Pulses When Triac Current is Interrupted by Motor Brush Bounce
- Triac Current Sensed to Allow Inductive Loads
- Soft Start
- Power Failure Detection and General Circuit Reset
- Low Power Consumption: 1.0 mA

TRIAC PHASE ANGLE CONTROLLER

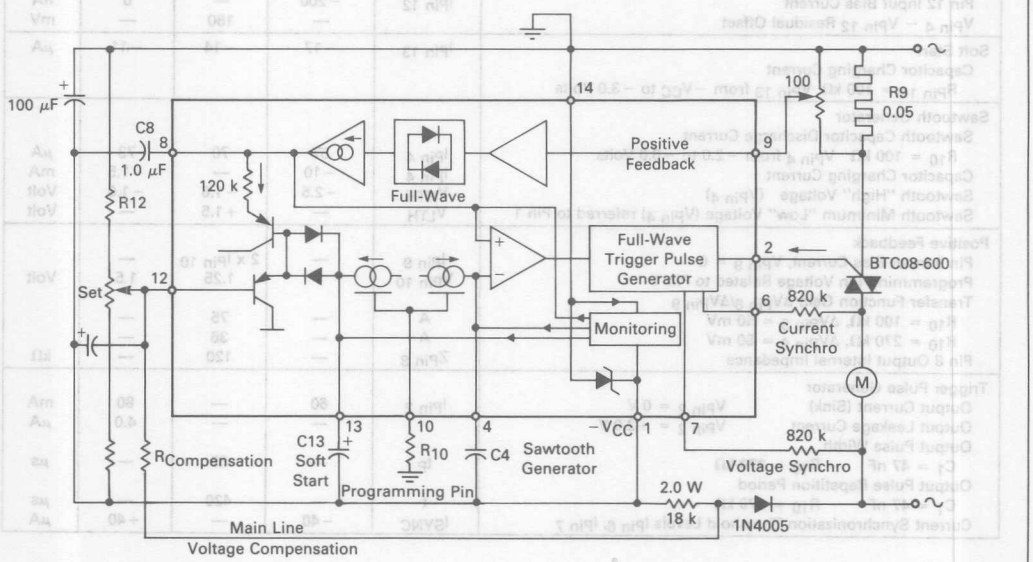
SILICON MONOLITHIC INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 646-06

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FIGURE 1 — TYPICAL SYSTEM CONFIGURATION — INTERNAL BLOCK DIAGRAM/PIN ASSIGNMENT



MAXIMUM RATINGS (Voltages are referred to Pin 14 (ground) unless otherwise noted)

Rating	Symbol	Value	Unit
Maximum Voltage Range per Listed Pin	V_{Pin}		Volt
Pins 3-5-11 (not connected)		−20 to +20	
Pins 4-8-13		$-V_{CC}$ to 0	
Pin 2		−3.0 to +3.0	
Maximum Positive Voltage (No minimum value allowed; see current ratings)	$V_{Pin\ 12}$ $V_{Pin\ 1}$	+0 +0.5	
Maximum Current per Listed Pin	I_{Pin}		
Pin 1		±20	mA
Pins 6 and 7		±2.0	mA
Pin 9		±0.5	mA
Pin 10		±300	μA
Pin 12		−500	μA
Maximum Power Dissipation (at T_A = 25°C)	P_D	250	mW
Maximum Junction to Ambient Thermal Resistance	$R_{\theta JA}$	100	°C/W
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C) Voltages are related to Pin 14 (ground)

Characteristics	Symbol	Min	Typ	Max	Unit
Power Supply					
Zener Regulated Voltage, ($V_{Pin\ 1}$) $I_{Pin\ 1}$ = 2.0 mA	$-V_{CC}$	−9.6	−8.6	−7.6	Volt
Circuit Current Consumption, $I_{Pin\ 1}$					
$V_{Pin\ 1}$ = −6.0 V, $I_{Pin\ 2}$ = 0 V	$-I_{CC}$	−2.0	−1.0	—	mA
Monitoring Enable Supply Voltage (V_{EN})	$V_{Pin\ 1EN}$	V_{CC} + 0.2	—	V_{CC} +0.5	Volt
Monitoring Disable Supply Voltage (V_{DIS})	$V_{Pin\ 1DIS}$	V_{EN} + 0.12	—	V_{EN} + 0.3	
Phase Set					
Control Voltage Static Offset $V_{Pin\ 8}$ − $V_{Pin\ 12}$	V_{off}	1.2	—	1.8	Volt
Pin 12 Input Bias Current	$I_{Pin\ 12}$	−200	—	0	nA
$V_{Pin\ 4}$ − $V_{Pin\ 12}$ Residual Offset		—	180	—	mV
Soft Start	$I_{Pin\ 13}$	−17	−14	−11	μA
Capacitor Charging Current					
$R_{Pin\ 10}$ = 100 kΩ, $V_{Pin\ 13}$ from $-V_{CC}$ to −3.0 Volts					
Sawtooth Generator					
Sawtooth Capacitor Discharge Current					
R_{10} = 100 kΩ $V_{Pin\ 4}$ from −2.0 to −6.0 Volts	$I_{Pin\ 4}$	67	70	73	μA
Capacitor Charging Current	$I_{Pin\ 4}$	−10	—	−1.5	mA
Sawtooth "High" Voltage ($V_{Pin\ 4}$)	V_{HTH}	−2.5	−1.6	−1.0	Volt
Sawtooth Minimum "Low" Voltage ($V_{Pin\ 4}$) referred to Pin 1	V_{LTH}	—	+1.5	—	Volt
Positive Feedback					
Pin 9 Input Bias Current, $V_{Pin\ 9}$ = 0	$I_{Pin\ 9}$	—	2 x $I_{Pin\ 10}$	—	
Programming Pin Voltage Related to Pin 1	$V_{Pin\ 10}$	1	1.25	1.5	Volt
Transfer Function Gain $\Delta V_{Pin\ 8}/\Delta V_{Pin\ 9}$					
R_{10} = 100 kΩ, $\Delta V_{Pin\ 9}$ = 50 mV	A	—	75	—	
R_{10} = 270 kΩ, $\Delta V_{Pin\ 9}$ = 50 mV	A	—	36	—	
Pin 8 Output Internal Impedance	$Z_{Pin\ 8}$	—	120	—	kΩ
Trigger Pulse Generator					
Output Current (Sink) $V_{Pin\ 2}$ = 0 V	$I_{Pin\ 2}$	60	—	80	mA
Output Leakage Current $V_{Pin\ 2}$ = +2.0 V		—	—	4.0	μA
Output Pulse Width					
C_1 = 47 nF R_{10} = 270 kΩ	t_P	—	55	—	μs
Output Pulse Repetition Period					
C_1 = 47 nF R_{10} = 270 kΩ	t	—	420	—	μs
Current Synchronization Threshold Levels $I_{Pin\ 6}$, $I_{Pin\ 7}$	I_{SYNC}	−40	—	+40	μA

CIRCUIT DESCRIPTION

The TDA1185A generates trigger pulses for triac control of power into an ac load. The firing angle is determined by generating a ramp voltage synchronized to the ac line half cycle and compared to an external set voltage representing the conduction angle.

Gate pulses are negative (sink current) and thus the triac is driven in its most effective quadrants (Q2–Q3).

If the load is a Universal motor (the speed of which is decreasing as torque increases), the TDA1185A allows to increase the firing angle proportionally to the motor current, sensed by a low value series resistor.

Notice: Perfect motor speed compensation cannot be provided by open-loop systems, since no negative feedback is used. Due to the low cost of tacholess systems, the TDA1185A is the optimum solution for applications tolerating 5% motor speed variations.

Nevertheless by accurate circuit design, these variations can be reduced down to 2% from no load to full load conditions.

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CIRCUIT FUNCTIONS

DC POWER SUPPLY — DC power is directly derived from the ac line through a 2.0 watt, 18 kΩ resistor, rectifier and filtering capacitor circuit. The latter being directly connected to the dropping resistor protects the whole IC from any ac line overvoltage. The $-V_{CC}$ voltage is internally regulated by an integrated zener. Referred to Pin 14 (ground) the power supply voltage is negative (−8.6 volts). The TDA1185A internal consumption is 1.0 mA.

TRIGGER PULSE GENERATOR — It delivers a 60 mA minimum pulse current (sink) through an internally short-circuit protected output. Pulse width is roughly proportional to $R_{10} \cdot C_4$ and is repeated every 420 μs if triac fails to latch or is switched off by brush bounce. With inductive loads, the current lags in respect of the voltage: Pin 6 delays the triggering pulse up to the moment the triac is off, in order to prevent erratic power control (see Figure 2). The logic structure guarantees full-wave triac operation.

SAWTOOTH GENERATOR — A constant current generator discharges the capacitor C_4, the voltage of which is the sawtooth signal synchronized with main line. Pin 4 voltage is reset to −1.6 volt at every ac line zero crossing (see Figure 3). The constant current generator is externally programmable by an external resistor connected to Pin 10:

$$I_{Pin\ 4} = I_{Pin\ 10}\ 10 \pm 5\%$$

$$I_{Pin\ 10} = \frac{-V_{CC} \pm 1.25}{R_{10}}$$

MAIN COMPARATOR — Its role is to determine the trigger pulse time which occurs as the sawtooth voltage equals set voltage. Fixed set values lead to a constant triac conduction angle unless positive current feedback is connected or soft start capacitor is not charged.

SOFT START — The TDA1185A allows the user to avoid any abrupt inrush current in the load, for various purposes: motor soft start, protection of high performance bulbs or ac line minimum disturbances.

The firing angle is established from zero to the set value according to a voltage ramp generated by a constant current delivered to capacitor C_{13}. The constant current value is:

$$I_{Pin\ 13} = 0.2 \times I_{Pin\ 10} \pm 10\%$$

The voltage ramp lasts as long as $V_{Pin\ 13}$ is lower than $V_{Pin\ 12}$. $V_{Pin\ 13}$ reset voltage is $-V_{CC}$. See Figure 4.

Notice. Universal motors do not have any motion effect as long as a minimum conduction angle is not reached. The time the voltage ramp reaches this threshold value is considered as "dead" time and can be eliminated by a series resistor at Pin 13. The voltage drop developed by $I_{Pin\ 13}$ makes the firing angle immediately reach the threshold value and have the soft start function without dead time. See Figure 5.

POSITIVE CURRENT FEEDBACK — The Universal motor speed drops as load increases. To maintain it as stable as possible, the triac firing angle must be increased. For this purpose the Pin 9 input senses the motor current as a voltage developed in a low resistor value, R_g, amplifies, rectifies and adds it to Pin 12 set voltage. The transfer function $\Delta V_{Pin\ 8} = f(\Delta V_{Pin\ 9})$ and is represented on Figure 6.

The gain in the linear region is dependent on R_{10}. The voltage transferred to Pin 8 is proportional to the average value of the motor current and is very close to its RMS value (as motor current is not far from a sine wave). This averaging effect is represented in Figure 7.

For large amplitude Pin 9 signals, the am function presents a saturation effect which limits the maximum firing angle increase. Figure 8 presents this aspect as well as the total Pin 8 voltage which is:

$$V_{Pin\ 8} = V_{Pin\ 12} + f(|V_{Pin\ 9}|\ R_{10}) + \text{offset}$$

The offset is the addition of two PN Junctions and is compensated with respect to $V_{Pin\ 4}$ (sawtooth) by additional diodes within the main comparator (See Figure 10).

The effect of positive feedback is described per Figure 9.

MONITORING — A central logic block performs the following functions: — ENABLE/DISABLE of the IC with respect to power supply voltage. Under DISABLE conditions, Pins 4, 8, 12, and 13 are forced to appropriate voltages to prepare for the next reset (See Figure 10).

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APPLICATION CONSIDERATIONS

PINS CHARACTERISTICS — Figure 10 describes more details in the internal IC layout and defines the pin characteristics. Pin 9 has a low internal impedance and requires a maximum 100 Ω trimmer on R_g to adjust reaction ratio. Pin 8 must always be connected to $-V_{CC}$ through a filtering capacitor.

TEMPERATURE EFFECTS — The TDA1185A has very efficient internal temperature compensation. If positive current feedback is not connected, the RMS power delivered to the load is stabilized within ±0.2% over a temperature range of +20 to +70°C. The positive feedback introduces in the same temperature range, a drift of 250 mV on $V_{Pin\ 8}$; this slight firing angle increase may be successfully used to compensate a motor ohmic resistance increase with temperature as well.

MAIN LINE VOLTAGE COMPENSATION — As the firing angle is independent of main line voltage, any change in the latter (usually ±15%) induces a very large power variation to the load. An external compensation must be used, introducing a $V_{Pin\ 12}$ decrease as V_{mains} increases. An inexpensive resistor R_{COMP}, connected to the rectifier anode and to Pin 12 performs this role and its value depends on $V_{Pin\ 12}$, $R_{10}C_4$, R_{12}. R_{COMP} can be empirically determined without difficulty under no load conditions.

FIRING ANGLE DYNAMIC — With purely resistive loads, the effective RMS applied power to the load is an increasing function of the firing angle (per Figure 11). We notice the fact that a firing angle of 150° provides 97% of the full power corresponding to 180°.

With inductive loads, as currents lag with respect to Voltage, 100% power corresponds to a firing angle which is smaller than 180°.

These considerations will simplify positive feedback design if maximum firing angle is accepted to be within 150–160°.

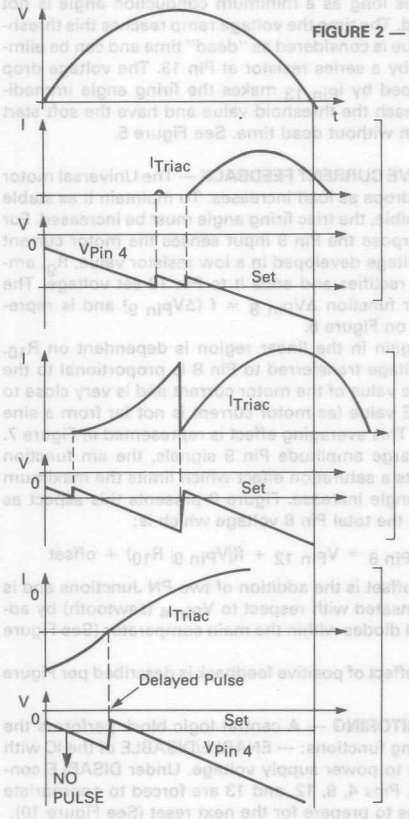


FIGURE 2 — MULTIPULSE GENERATION DELAYED PULSE

The triac failed to latch at the first pulse. Successive pulses are generated up to the moment latching oocurs.

The triac turned off due to brush bounce, a new pulse is immediately delivered.

Approaching full conduction, a pulse would occur when the triac still carries current; the pulse is delayed until the triac turns off.

FIGURE 3 — TRIGGERING PULSE TIMING

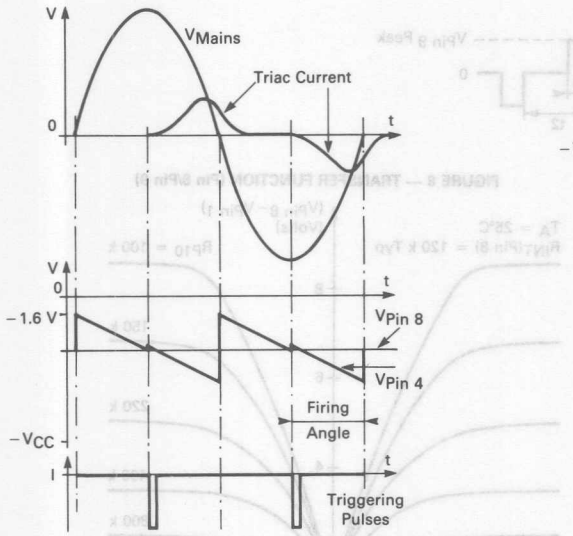


FIGURE 4 — SOFT START

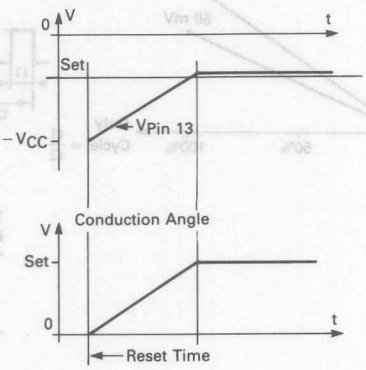


FIGURE 5 — SOFT START WITHOUT DEAD TIME

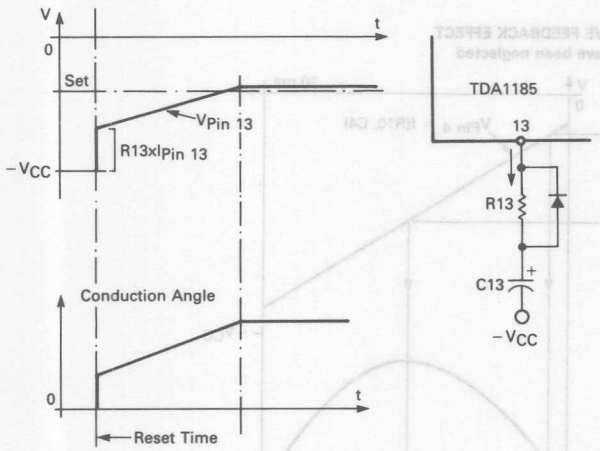


FIGURE 6 — TRANSFER FUNCTION

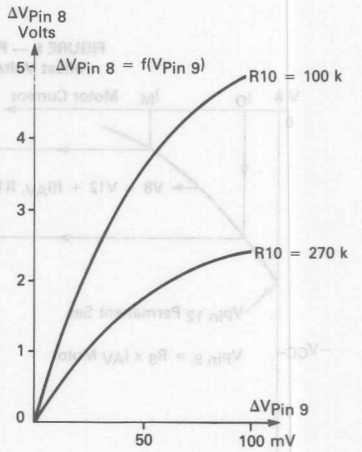


FIGURE 7 — AVERAGING EFFECT OF TRANSFER FUNCTION

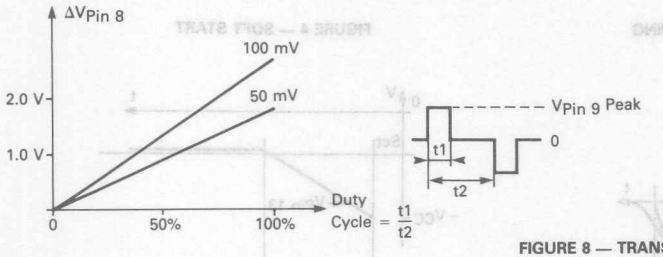


FIGURE 8 — TRANSFER FUNCTION (Pin 8/Pin 9)

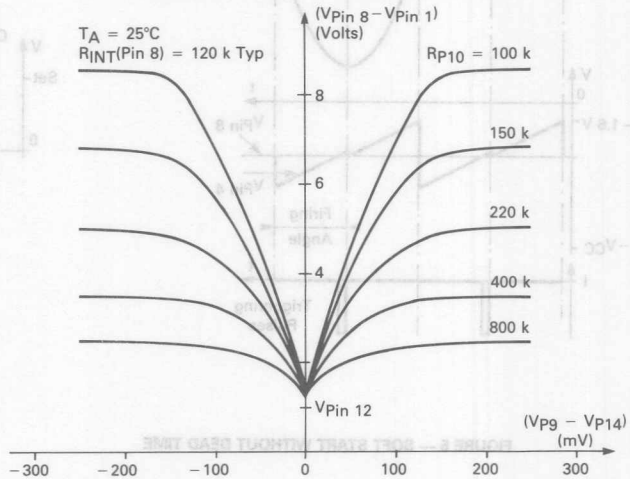


FIGURE 9 — POSITIVE FEEDBACK EFFECT
offset Voltages have been neglected

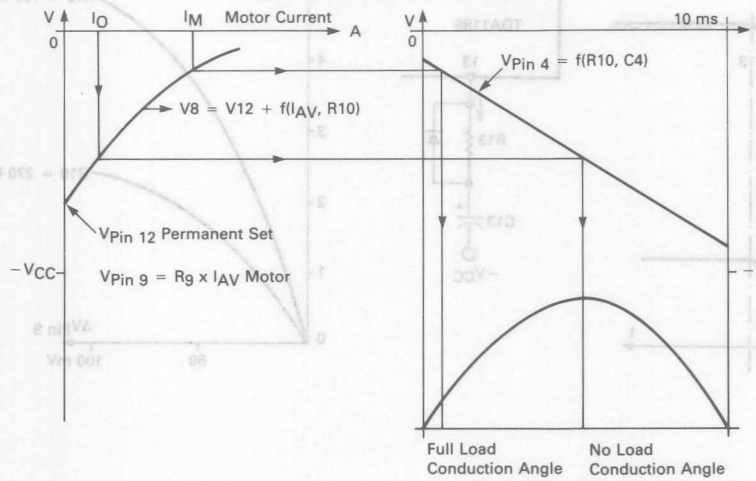


FIGURE 10 — INTERNAL BLOCK DIAGRAM

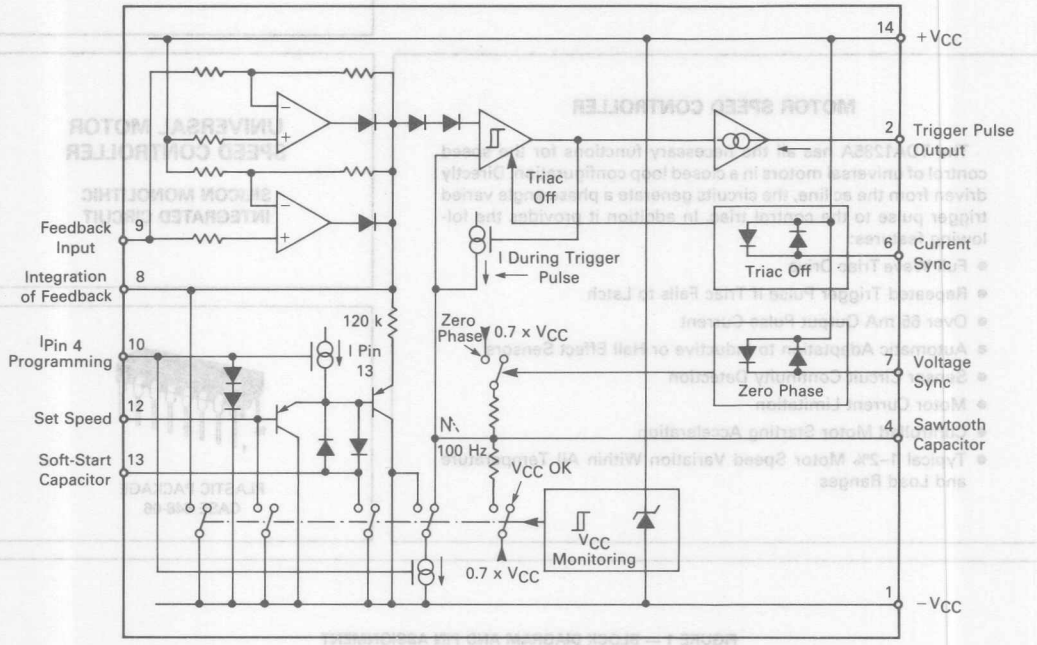
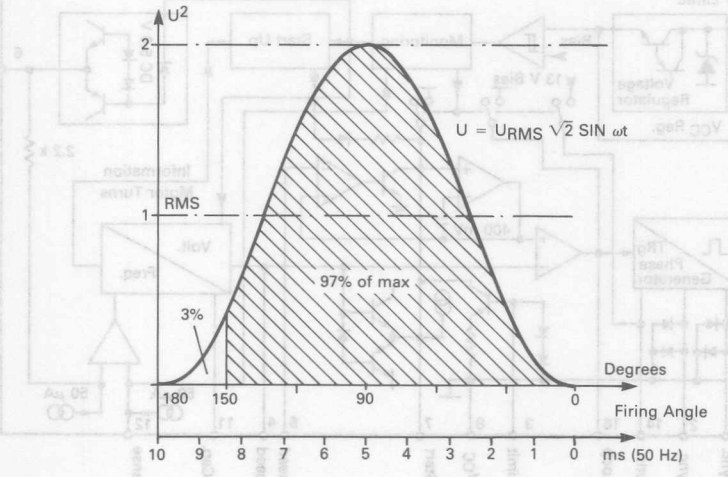


FIGURE 11 — EFFECTIVE POWER AS A FUNCTION OF FIRING ANGLE



MOTOROLA

TDA1285A

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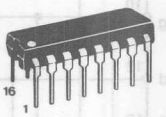
MOTOR SPEED CONTROLLER

The TDA1285A has all the necessary functions for the speed control of universal motors in a closed loop configuration. Directly driven from the ac line, the circuits generate a phase angle varied trigger pulse to the control triac. In addition it provides the following features:

- Full Wave Triac Drive
- Repeated Trigger Pulse if Triac Fails to Latch
- Over 65 mA Output Pulse Current
- Automatic Adaptation to Inductive or Hall Effect Sensors
- Sensor Circuit Continuity Detection
- Motor Current Limitation
- Controlled Motor Starting Acceleration
- Typical 1–2% Motor Speed Variation Within All Temperature and Load Ranges

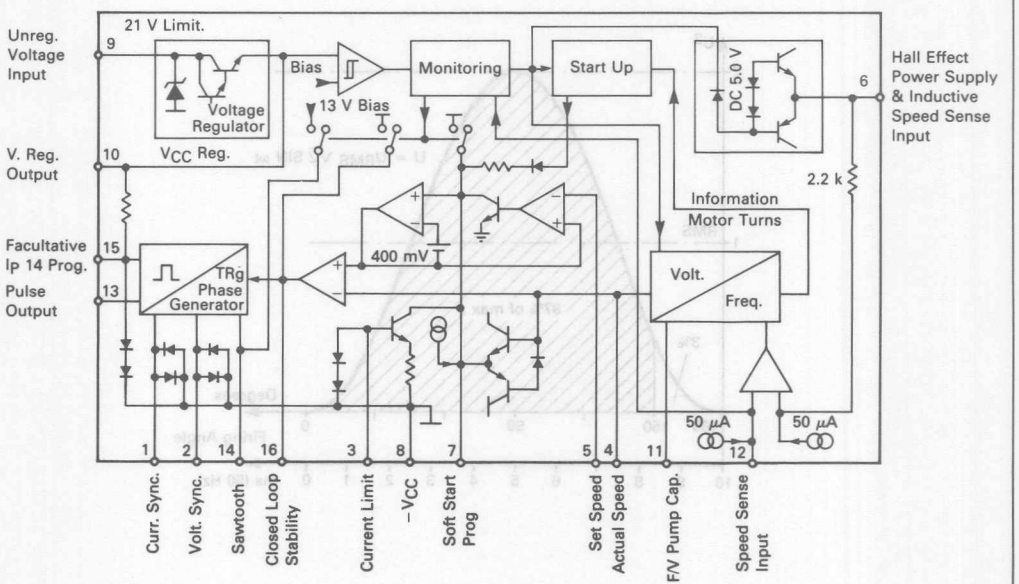
UNIVERSAL MOTOR SPEED CONTROLLER

SILICON MONOLITHIC INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 648-06

FIGURE 1 — BLOCK DIAGRAM AND PIN ASSIGNMENT



MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Supply Current	$I_{Pin\ 9\ RMS}$	20	mA
Peak Supply Current, t < 250 μs	$I_{Pin\ 9\ PEAK}$	200	mA
Regulated Supply Current Drain	$I_{Pin\ 10}$	10	mA
Peak ac Synchronization Input Currents	$I_{Pin\ 1}$ $I_{Pin\ 2}$	±2.0 ±2.0	mA mA
Current Drain per Listed Pin	I_3	−1.0 +2.0	mA
	I_{12}	+500 −4.0	μA mA
	I_6	−7.0 +1.0	mA
	I_{15}	+1.0	mA
Pin 3 Reverse Voltage	$V_{Pin\ 3}$	−5.0	V
Power Dissipation (T_A = 25°C) Derate above 25°C	P_D $1/R_{\theta JA}$	625 6.8	mW mW/°C
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply					
Zener Regulated Voltage, $I_{Pin\ 9}$ = 20 mA	$V_{Pin\ 9}$	19	20.5	23	V
Regulated Supply Voltage (Pin 10) $I_{Pin\ 10}$ = 0; $I_{Pin\ 13}$ = 0; $I_{Pin\ 15}$ = 0 $I_{Pin\ 7}$ = 0; $V_{Pin\ 9}$ = 18 V	V_{CC}	13.6	14.6	15.6	V
Current Consumption ($I_{Pin\ 9}$) $I_{Pin\ 6}$ = 0; $I_{Pin\ 13}$ = 0; $I_{Pin\ 10}$ = 0 $I_{Pin\ 15}$ = 0; $I_{Pin\ 7}$ = 0; $V_{Pin\ 9}$ = 18 V	I_{CC}	—	4.5	7.0	mA
Speed Reference					
Reference Input Voltage Range	$V_{Pin\ 5}$	0	—	12	V
Reference Input Bias Current ($V_{Pin\ 5}$: 0 to +12 V)	$I_{Pin\ 5}$	−2.0	—	0	μA
Frequency to Voltage Converter					
Inductive Sensor Application Range	$I_{Pin\ 6}$	−2.5	—	0	mA
Hall-Effect Sensor Application Range	$I_{Pin\ 6}$	−8.0	—	−3.5	mA
Maximum Input Signal Voltage	$V_{Pin\ 12} - V_{Pin\ 6}$	−5.0	—	+5.0	V
Common-Mode Reference Voltage	$V_{Pin\ 6}$	—	5.0	—	V
Polarization Current (−5.0 V < $V_{Pin\ 12} - V_{Pin\ 6}$ < +5.0 V)	$I_{Pin\ 12}$	—	−50	—	μA
Threshold Hysteresis Voltage (See Figure 4)	$(V_{Sensor} - V_{Pin\ 6})THRS$	—	±60	—	mV
Floating Input Voltage ($I_{Pin\ 12}$ = 0)	$V_{Pin\ 12}$	12	—	—	V
Main Comparator					
Output Voltage Range ($I_{Pin\ 16}$ = 0)	$V_{Pin\ 16}$	—	0; +12	—	V
Output Current Swing	$I_{Pin\ 16}$	—	±100	—	μA
Transconductance ($I_{Pin\ 7}$ = 0; $I_{Pin\ 10}$ = 0; $V_{Pin\ 16}$ = 5.2 V)	$\frac{\Delta I_{Pin\ 16}}{\Delta V_{Pin\ 4}}$	140	205	265	μA/V
Output Resistance	$R_{out\ Pin\ 16}$	—	10^6	—	Ω
Offset Voltage ($I_{Pin\ 7}$ = 0; $I_{Pin\ 16}$ = 0; $V_{Pin\ 16}$ = 5.0 V)	$V_{Pin\ 5} - V_{Pin\ 4}$	−20	0	+20	mV

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Current Limitation					
Detection Level	$V_{Pin\ 3\ Min.}$	—	0.65	—	V
Clamping Voltage Level	$V_{Pin\ 3\ CLAMP}$	—	1.3	—	V
Output Discharge Current	I_{DL7}	—	0.5	—	mA
Saturation Resistance	$R_{sat\ Pin\ 7}$	—	1.6	—	kΩ
Start-up					
Maximum Start-up Voltage ($I_{Pin\ 7}$ = 0)	$V_{Pin\ 7}$	—	4.5	—	V
Start-up Current (until motor turns) ($_{Pin\ 7}$ = 0)	$I_{Pin\ 7}$	—	−1.0	—	mA
Soft-Start		—		—	μA
Acceleration Charging Current	$I_{Pin\ 7}$		−8.0		
Trigger Pulse Generator					
Trigger Pulse Width*	tp	—	100	—	μs
Trigger Pulse Repetition Period*	t	—	600	—	μs
Output Pulse Current ($V_{Pin\ 13}$ = 1.0 V)	$I_{Pin\ 13}$	−70	—	−65	mA
Output Leakage Current ($V_{Pin\ 13}$ = −2.0 V)	$I_{o\ Pin\ 13}$	—	—	10	μA
Current Synchronization Threshold Levels (Pin 1 and Pin 2)	I_{Thrs}	—	±80	—	μA
Sawtooth Current Generator	$I_{Pin\ 14}$	—	−65	—	μA
Pin 15 Voltage ($I_{Pin\ 15}$ = 0)	$V_{Pin\ 15}$	—	1.3	—	Volt

* These figures apply for the application shown in this data sheet.

CIRCUIT DESCRIPTION

The TDA1285A generates trigger pulses for a triac controlling the power into an ac motor connected to a line voltage. The firing angle of the triac is determined by comparison between a sawtooth signal (line voltage synchronized) and the main internal comparator signal. The latter is the difference between a set voltage (externally adjustable) representing the reference speed and the actual motor speed issued from an external sensor and converted by an internal frequency to voltage converter. This sensor may be inductive (tachometer) or Hall-effect. Other functions are also provided by the TDA1285A.

KEY CIRCUIT FUNCTIONS

DC POWER SUPPLY

DC Power is directly derived from the ac line by a low cost resistor-rectifier-capacitor circuit. The voltage on Pin 9 is Zener protected. The voltage on Pin 10 is fully regulated by a series ballast regulator, but is not self-limiting. Special provisions for Hall-effect sensor power are included.

TACHOMETER INPUT (Pins 6 and 12)

The maximum allowable voltage swing is −5.0 to +5.0 V. Circuit continuity is permanently checked by the monitor.

HALL-EFFECT INPUT (Pins 6 and 12)

When $I_{Pin\ 6}$ exceeds 3.0 mA, the circuit detects the use of a Hall-effect sensor and thus sensor circuit continuity is not checked (an open circuit would provide full triac conduction angle).

FREQUENCY TO VOLTAGE CONVERTER

This circuit converts the tachometer input frequency into a proportional voltage on Pin 4 (eventually usable for any feedback). Particular care must be devoted to the conversion ratio of the F/V converter which is under the user control. In effect, it depends on the values of the C_{11} capacitor and on tachometer frequency f(Hz).

$$V_{Pin\ 4} = 1.410 \times 10^{-10} \times C_{11}\ (pF) \times R_4 \times F(Hz) \times (1 \pm 0.15)$$

$V_{Pin\ 4}$ corresponding to maximum allowed motor speed must be chosen as close as possible to 12 V in order to minimize noise disturbance down to a negligible level.

MAIN COMPARATOR

Its role is to amplify the signal error. Negative feedback from the output (Pin 16) to the input may be used to reduce the closed loop gain of the system and increase stability.

SOFT START (Pin 7)

Set speed input (Pin 5) is overruled by similar data from Pin 7 as long as $V_{Pin\ 7}$ is smaller than $V_{Pin\ 5}$ + 400 mV (Typ). An internal 8.0 μA current source allows an external capacitor, C_7 to be charged slowly and thus lets the ac motor soft start (Figure 2). Pin 4 offset may be set appropriately by an external resistor (R_1 = 1 MΩ). Notice that R_1 may affect F/V conversion ratio. An external 10 nF capacitor on Pin 5 reduces noise sensitivity.

START-UP CIRCUIT

From the moment power is applied to the circuit (or the circuit is enabled by Monitoring) to the moment a speed input signal is detected, C_7 is charged at a high current level (typically 1.0 mA). Detection of the first tachometer input resets the Pin 7 current to its nominal value (8.0 μA). The result of such a circuit is to start the acceleration ramp at the moment the motor starts to turn, avoiding any dead time (see Figure 2). When the motor is cycled on and off in close succession, the acceleration ramp is started immediately without waiting for the motor to stop.

MOTOR CURRENT LIMITATION (Pin 3)

The motor current is sensed as a voltage developed across a resistor (R_3) in series with the triac. The limiter acts on positive peak values of R_3 x I filtered by a 22 k and 0.1 μF, RC network (Figure 7). The motor current is reduced, decreasing its speed reference by discharging C_7 until current limit equilibrium is reached (see Figure 3).

TRIGGER PULSE GENERATOR

It delivers a 65 mA min. current pulse to the triac gate and repeats it if the triac fails to latch or if brush bounce has switched it off (Figure 6). Current and voltage detection through the triac are performed by Pins 1 and 2, delaying the trigger pulse until the triac current collapses. The pulse time is determined by the comparison of a sawtooth signal (available at Pin 14 and synchronous with line voltage) and the error signal directly supplied by the comparator.

Sawtooth slope is determined by the external capacitor C_{14}. Under these conditions pulse width is typically 100 μs (Figure 5).

MONITORING

This is an internal function, disabling the circuit when
— V_{CC} is insufficient
— Tachometer circuit is open and $I_{Pin\ 6} < |-3.0\ mA|$

4

4

FIGURE 2 — START-UP AND SOFT-START CIRCUIT ACTIONS

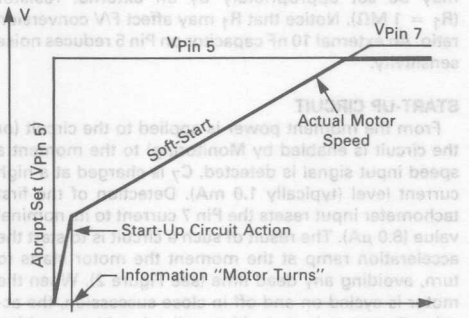


FIGURE 3 — CURRENT LIMITATION

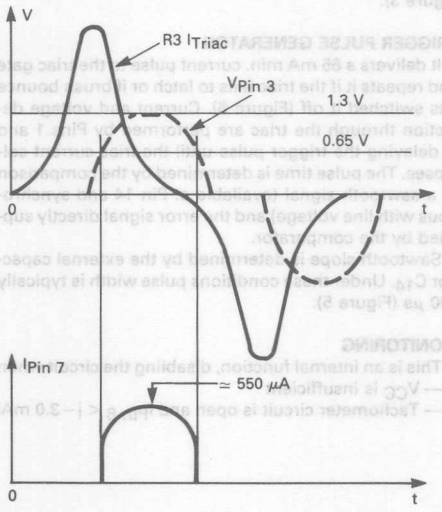
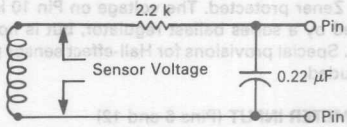


FIGURE 4 — SENSOR VOLTAGE DEFINITION



2.2 k is a recommended value to balance the voltage offset caused by sensor continuity detection circuit.

FIGURE 5 — FIRING PULSE GENERATION

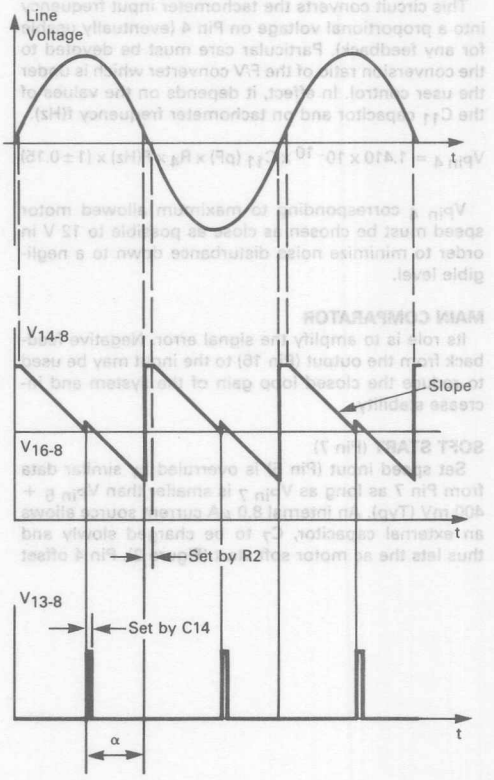
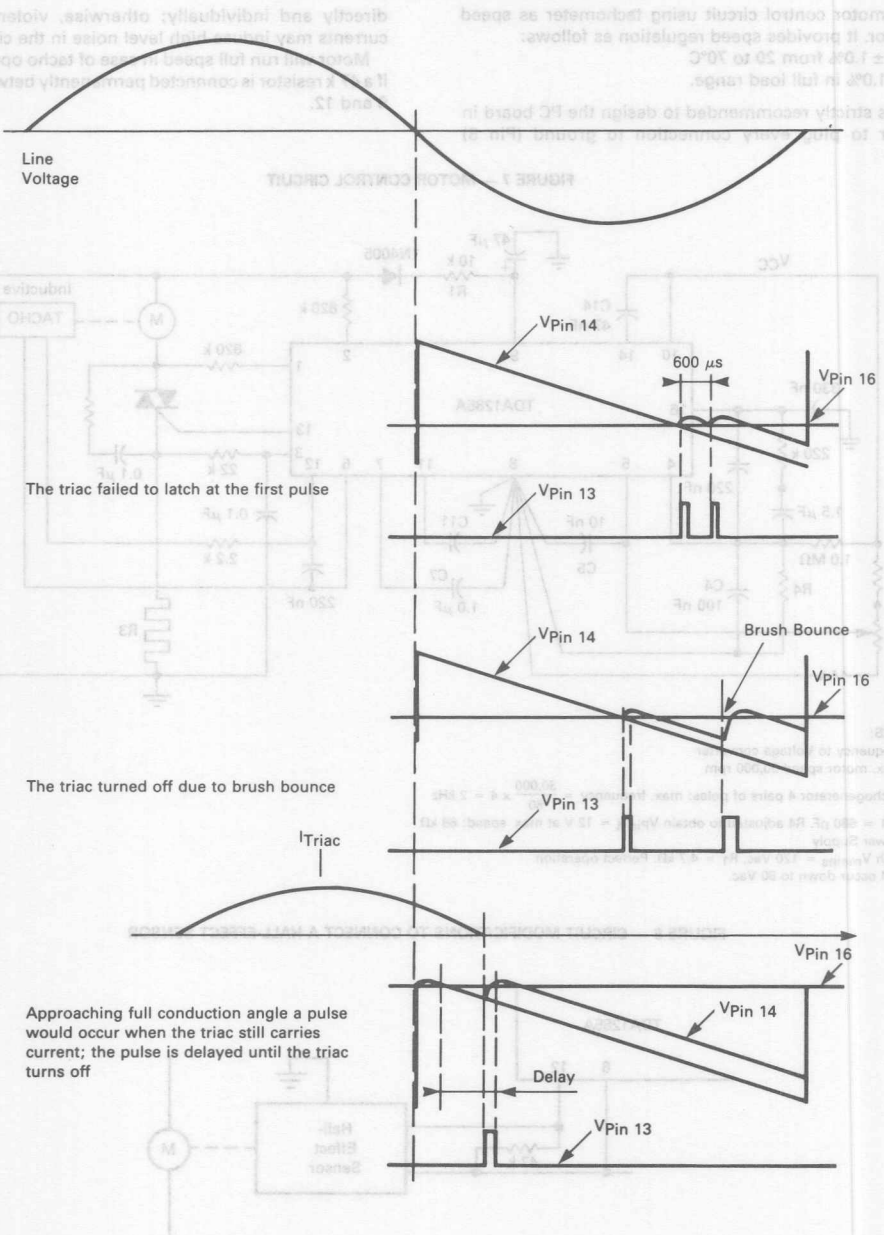


FIGURE 6 — MULTIPLE FIRING PULSE AND FIRING PULSE DELAY



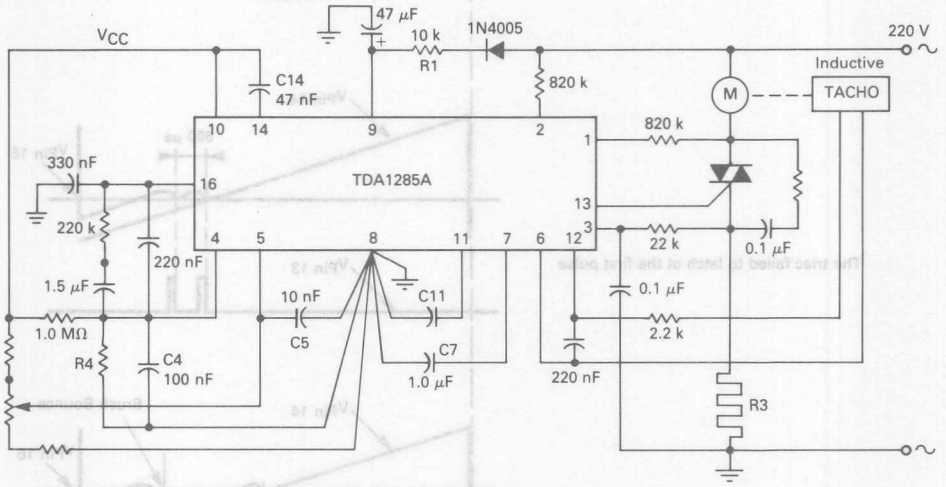
A motor control circuit using tachometer as speed sensor. It provides speed regulation as follows:

- ±1.0% from 20 to 70°C
- 1.0% in full load range.

It is strictly recommended to design the PC board in order to plug every connection to ground (Pin 8) directly and individually; otherwise, violent erratic currents may induce high level noise in the circuitry.

Motor will run full speed in case of tacho open circuit if a 47 k resistor is connncted permanently between Pins 6 and 12.

FIGURE 7 — MOTOR CONTROL CIRCUIT



NOTES:

Frequency to Voltage converter

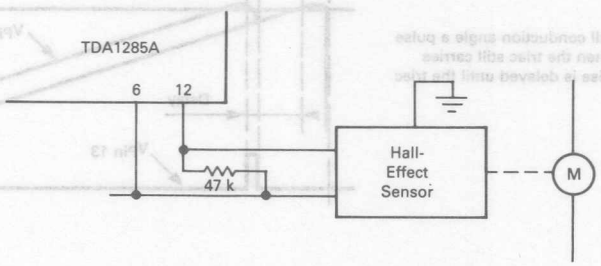
— Max. motor speed 30,000 rpm

— Tachogenerator 4 pairs of poles: max. frequency = $\frac{30{,}000}{60} \times 4 = 2$ kHz

— C11 = 680 pF. R4 adjusted to obtain $V_{Pin\ 4}$ = 12 V at max. speed: 68 kΩ

— Power Supply
with V_{mains} = 120 Vac, R_1 = 4.7 kΩ. Perfect operation will occur down to 80 Vac.

FIGURE 8 — CIRCUIT MODIFICATIONS TO CONNECT A HALL-EFFECT SENSOR



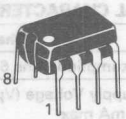
ZERO VOLTAGE CONTROLLER

The UAA1016B is designed to drive triacs with the Zero Voltage technique which allows RFI free power regulation of resistive loads. It provides the following features:

- Proportional Temperature Control Over an Adjustable Band
- Adjustable Burst Frequency (to Comply with Standards)
- Sensor Fail-Safe
- No dc Current Component Through the Main Line (to Comply with Standards)
- Negative Output Current Pulses (Triacs Quadrants 2 and 3)
- Direct ac Line Operation
- Low External Components Count

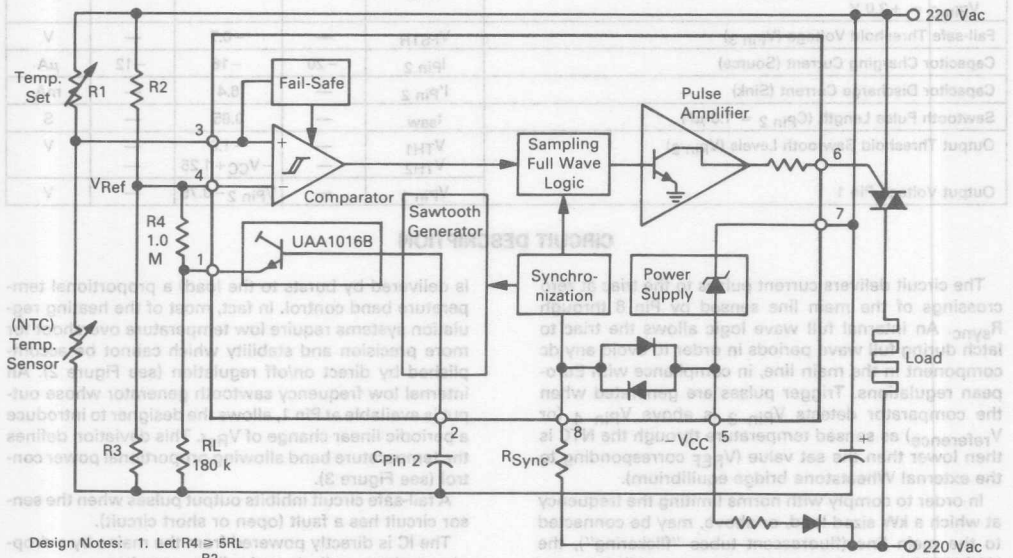
ZERO VOLTAGE SWITCH PROPORTIONAL BAND TEMPERATURE CONTROLLER

SILICON MONOLITHIC INTEGRATED CIRCUITS



P1 SUFFIX
PLASTIC PACKAGE
CASE 626-05

FIGURE 1 — BLOCK DIAGRAM AND PIN ASSIGNMENT



Design Notes: 1. Let R4 ≥ 5RL

2. Select $\frac{R2}{R3}$ Ratio for a symmetrical reference deviation centered about Pin 1 output swing, R2 will be slightly greater than R3.

3. Select R2 and R3 values for the desired reference deviation where $\Delta V_{REF} = \frac{\Delta V_{Pin\ 1}}{\frac{R4}{R2\ ||\ R3} + 1}$

MAXIMUM RATINGS (Voltages referred to Pin 7)

Parameter	Symbol	Max. Rating	Unit
Supply Current ($I_{Pin\ 5}$)	I_{CC}	15	mA
Nonrepetitive Supply Current ($I_{Pin\ 5}$)	I_{CCP}	200	mA
AC Synchronization Current (Pin 8)	I_{syn}	3.0	mA (RMS)
Maximum Pin Voltages	$V_{Pin\ 1}$ $V_{Pin\ 2}$ $V_{Pin\ 3}$ $V_{Pin\ 4}$ $V_{Pin\ 6}$	0; $-V_{CC}$ 0; $-V_{CC}$ 0; $-V_{CC}$ 0; $-V_{CC}$ +2.0; $-V_{CC}$	Volt
Maximum Current Drain	$I_{Pin\ 1}$	1.0	mA
Power Dissipation T_A = 25°C	P_D	625	mW
Maximum Thermal Resistance	$R_{\theta JA}$	100	°C/W
Operating Temperature Range	T_A	−20 to +100	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, Voltages referred to Pin 7 unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
Current Consumption (Pins 6 and 8 not connected)	I_{CC}	—	0.8	1.5	mA
Stabilized Supply Voltage ($V_{Pin\ 5}$) I_{CC} = 2.0 mA max	$-V_{CC}$	−9.6	−8.6	−7.6	V
Output Pulse Current ($V_{Pin\ 6}$ from −1.0 to +1.0 Volt)	I_{out}	60	90	120	mA
Output Pulse Width $R_{Pin\ 8}$ = 220 kΩ, V_{mains} = 220 Vac/50 Hz, (Figures 4 and 5)	t_{p1} t_{p2}	58 160	60 220	120 320	μs
Comparator Input Offset Voltage ($V_{Pin\ 3} - V_{Pin\ 4}$)	V_{off}	−10	—	+10	mV
Comparator Common Mode Voltage Range	V_{CM}	$-V_{CC}+1$	—	−1.5	V
Input Bias Current (Pins 3 and 4)	I_{IB}	—	—	1.0	μA
Output Leakage Current ($I_{Pin\ 6}$) $V_{Pin\ 6}$ = +2.0 V	I_{outL}	—	—	10	μA
Fail-safe Threshold Voltage ($V_{Pin\ 3}$)	V_{FSTH}	—	−0.7	—	V
Capacitor Charging Current (Source)	$I_{Pin\ 2}$	−20	−16	−12	μA
Capacitor Discharge Current (Sink)	$I'_{Pin\ 2}$	—	6.4	—	mA
Sawtooth Pulse Length ($C_{Pin\ 2}$ = 1.0 μF)	t_{saw}	—	0.85	—	S
Output Threshold Sawtooth Levels ($V_{Pin\ 2}$)	V_{TH1} V_{TH2}	— —	−1.0 $-V_{CC}+1.25$	— —	V
Output Voltage Pin 1	$V_{Pin\ 1}$	—	$V_{Pin\ 2}-0.75$	—	V

CIRCUIT DESCRIPTION

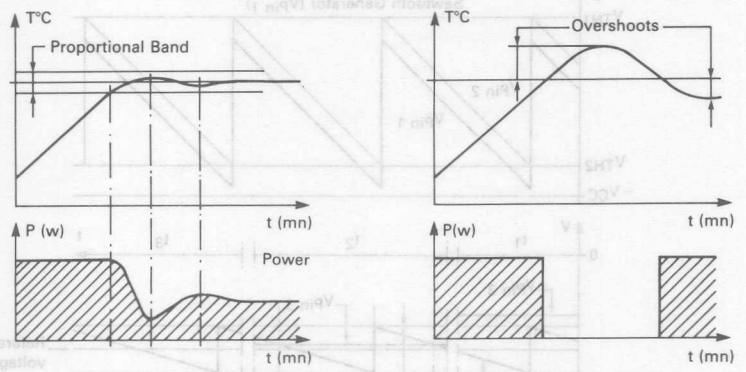
The circuit delivers current pulses to the triac at zero crossings of the main line sensed by Pin 8 through R_{sync}. An internal full wave logic allows the triac to latch during full wave periods in order to avoid any dc component in the main line, in compliance with European regulations. Trigger pulses are generated when the comparator detects $V_{Pin\ 3}$ is above $V_{Pin\ 4}$ (or $V_{reference}$) as sensed temperature through the NTC is then lower than the set value (V_{REF} corresponding to the external Wheatstone bridge equilibrium).

In order to comply with norms limiting the frequency at which a kW sized load, or above, may be connected to the main line (fluorescent tubes "flickering"), the UAA1016B has an internal time base providing (power is delivered by bursts to the load) a proportional temperature band control. In fact, most of the heating regulation systems require low temperature overshoot for more precision and stability which cannot be accomplished by direct on/off regulation (see Figure 2). An internal low frequency sawtooth generator whose output is available at Pin 1, allows the designer to introduce a periodic linear change of V_{Ref}. This deviation defines the temperature band allowing proportional power control (see Figure 3).

A fail-safe circuit inhibits output pulses when the sensor circuit has a fault (open or short circuit).

The IC is directly powered from the mains by a dropping resistor, a diode and a filter capacitor.

FIGURE 2 — PROPORTIONAL TEMPERATURE CONTROL versus ON/OFF CONTROL



PROPORTIONAL TEMPERATURE CONTROL

Reduced Overshoot

Stability

ON/OFF CONTROL

Large Overshoot

Marginal Stability

4

KEY CIRCUIT FUNCTIONS DESCRIPTION

POWER SUPPLY — The rectified supply current is Zener regulated to 8.6 V. Current consumption of the UAA1016B is typically less than 1.0 mA. The major part of the current fed by the dropping resistor is used for the sensor bridge and triac gate pulses. Any excess of supply current is excess power dissipation into the integrated Zener. Current consumption of the triac pulses may be derived from Figure 4 and 5 (Igt max. and pulse duration). Usually an 18 kΩ, 2.0 W dropping resistor is convenient to feed the UAA1016.

COMPARATOR — When $V_{Pin\ 3}$ is higher than $V_{Pin\ 4}$ (V_{Ref}), the comparator allows the triggering logic to deliver pulses to the triac (Figure 3). The offset hysteresis input voltage has been designed to be as low as possible (±10 mV max) in order to minimize the uncontrollable temperature band (proportional to the hysteresis) as per Figure 6. Noise rejection is performed by a synchronous sampling of the comparator output during very short times (typ. less than 100 ns).

SAWTOOTH GENERATOR — A sawtooth voltage signal is generated by a constant current source (typ. 7.5 μA), charging an external capacitor $C_{Pin\ 2}$ between two threshold levels, V_{TH1} and V_{TH2}, which are respectively:

$V_{TH1} = -1.0$ V

$V_{TH2} = -V_{CC} + 1.25$ V.

Charging and discharging currents occur only with negative halfcycles of the line.

In the UAA1016B, the sawtooth signal is available at Pin 1 as a voltage source $V_{Pin\ 1} = V_{Pin\ 2} - 0.75$ V. Maximum source current is 1.0 mA, but to keep good linearity of sawtooth signal, a source current of 40 μA is recommended (see Figure 7).

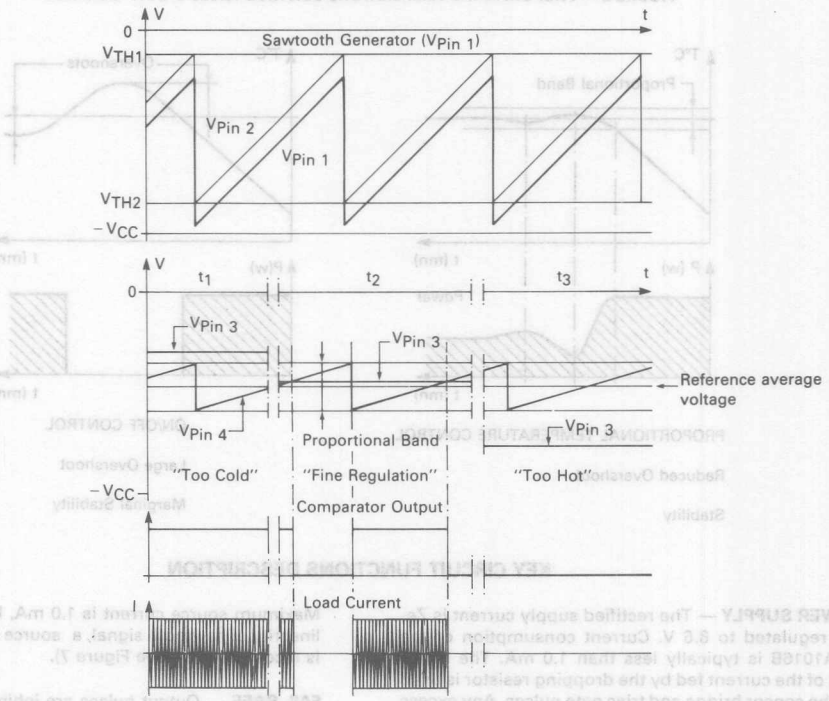
FAIL-SAFE — Output pulses are inhibited by the "fail-safe" circuit if the comparator input voltage exceeds the specified threshold voltage. This would occur if the temperature sensor circuit had a fault.

SAMPLING FULL WAVE LOGIC — Two consecutive zero-crossing trigger pulses are generated at every positive mains half-cycle of the line to minimize generation of noise (as per Figure 8). Within every zero-crossing the pulses are positioned as per Figure 4. Pulse length is also adjustable by R_{sync} on Pin 8 to allow positive triggering of the triac at this critical moment (firing with low voltage between main terminals requires long pulses).

PULSE AMPLIFIER — The pulse amplifier circuit delivers minimum current pulses of 60 mA (sink). The triac is triggered in quadrants II and III.

SYNCHRONIZATION CIRCUIT — This circuit detects mains zero-crossings through R_{sync} and the value selected determines the trigger pulse length. A zero crossing current detector is employed with typical thresholds of ∓27 μA to ±98 μA (see Figures 4 and 5).

FIGURE 3 — SAWTOOTH GENERATOR AND PROPORTIONAL BAND



COMMENTS TO FIGURE 3

Referring to Figure 1, the average value of V_{Ref} is set by R_2 and R_3. R_4 defines the amplitude of the sawtooth signal superimposed on V_{Ref}, defining the Proportional Band.

Figure 3 shows three conditions:

1) During time t_1 we always have $V_{Pin\ 3} > V_{Ref}$, and as a result, the comparator is always "on" and the triac fired (100% max. power)
2) During time t_2, $V_{Pin\ 3}$ is in the proportional band, and the average power delivered to the load is a fraction of maximum power.
3) During time t_3, $V_{Pin\ 3} < V_{Ref}$, and the triac is always "off."

When the sensor temperature is above the set value and is slowly decreasing as no heating occurs, $V_{Pin\ 3} - V_{Pin\ 4}$ must exceed half the hysteresis value before power is applied again (1). A similar effect occurs in the opposite direction when temperature sensor is below the set value and can remain stable as position (2). This defines the "uncontrollable temperature band" which will be very small if hysteresis is also very small.

SUGGESTIONS FOR USE

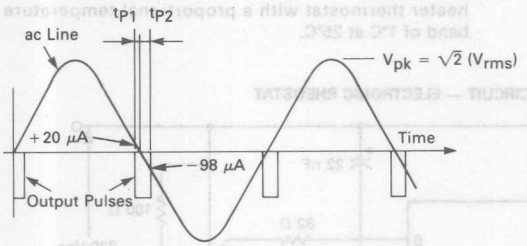
The temperature sensor circuit is a Wheatstone bridge including the sensor element. Comparator inputs may be free from power line noise only if the sensor element is purely resistive (NTC resistor). Usage of any P-N junction sensor would drastically reduce noise rejection.

Fixed phase sensing of the internal comparator output eliminates parasitic signals.

Some loads, even designed to be resistive, have in fact a slight inductive component. A phase shift at Pin 8 can be achieved with external capacitor C_3 connected to Pin 8 network (see Figure 9).

Suggested maximum source current at Pin 1 is 40 μA, in order to have acceptable sawtooth signal linearity.

FIGURE 4 — OUTPUT PULSE WIDTH DEFINITIONS



$$t_{P2} = \frac{\sin^{-1}\left(\frac{98 \times 10^{-6}}{V_{rms} \cdot \sqrt{2}}\right)}{360 f_{ac}} \qquad t_{P1} = \frac{\sin^{-1}\left(\frac{27 \times 10^{-6}}{V_{rms} \cdot \sqrt{2}}\right)}{360 f_{ac}}$$

FIGURE 5 — TYPICAL OUTPUT PULSE LENGTH versus SYNCHRONIZATION RESISTOR

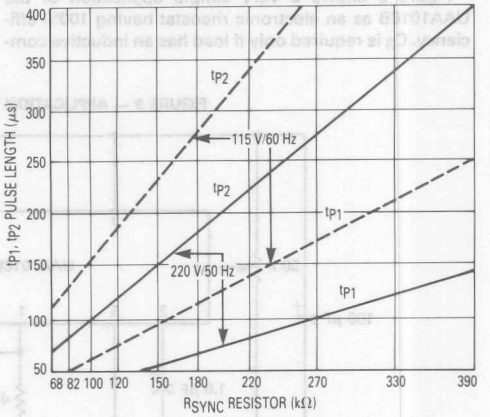


FIGURE 6 — EFFECTS OF INPUTS COMPARATOR HYSTERESIS

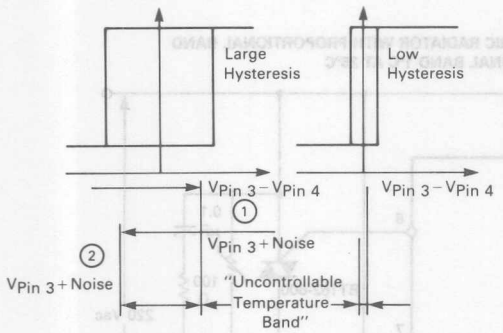


FIGURE 7 — PIN 1 INTERNAL NETWORK

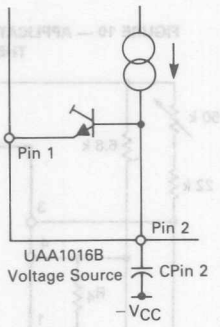
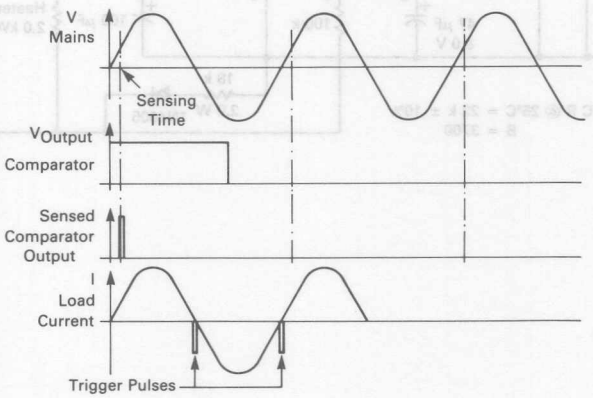


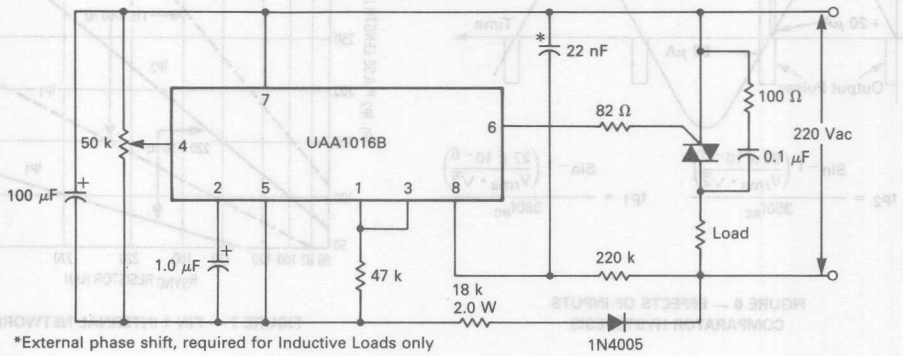
FIGURE 8 — TRIGGER PULSE GENERATION



APPLICATION CIRCUITS

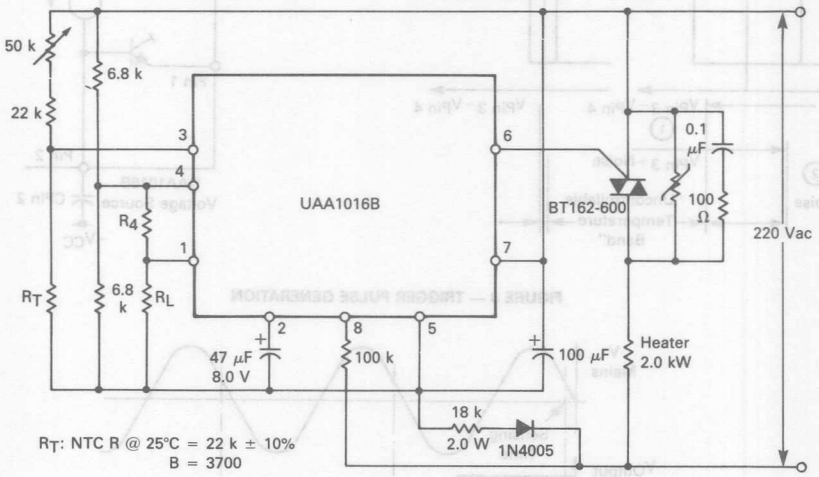
Figure 9 shows a very simple application of the UAA1016B as an electronic rheostat having 100% efficiency. C_3 is required only if load has an inductive component. Figure 10 shows a typical application as a panel heater thermostat with a proportional temperature band of 1°C at 25°C.

FIGURE 9 — APPLICATION CIRCUIT — ELECTRONIC RHEOSTAT

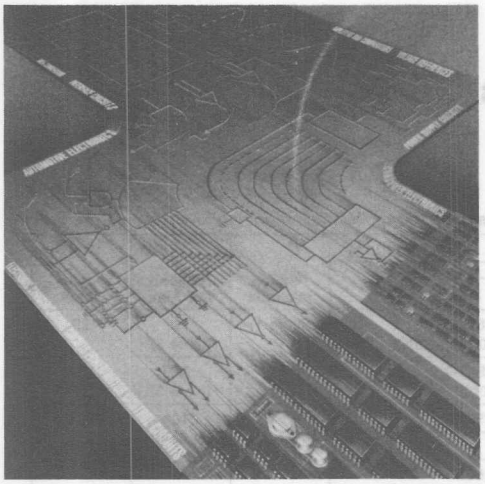


*External phase shift, required for Inductive Loads only

FIGURE 10 — APPLICATION CIRCUIT — ELECTRIC RADIATOR WITH PROPORTIONAL BAND THERMOSTAT, PROPORTIONAL BAND 1°C AT 25°C



RT: NTC R @ 25°C = 22 k ± 10%
B = 3700



Voltage References

5

In Brief . . .

Motorola's line of precision voltage references is designed for applications requiring high initial accuracy, low temperature drift, and long term stability. Initial accuracies of ±1.0%, and ±2.0% means production line adjustments can be eliminated. Temperature coefficients of 25 ppm/°C max (typically 10 ppm/°C) provide excellent stability. Uses for the references include D/A converters, A/D converters, precision power supplies, voltmeter systems, temperature monitors, and others.

Selector Guide
Precision Low Voltage References 5-2
Alphanumeric Listing 5-3
Data Sheets 5-4

Voltage References

Precision Low Voltage References

A family of precision low voltage bandgap reference devices designed for applications requiring low temperature drift.

V_{out} Volts Typ	I_O mA Max	V_{out}/T ppm/°C Max	Device		Reg$_{line}$ mV Max	Reg$_{load}$ mV Max	Case
			0° to 70°C	−55° to +125°C −40° to +85°C			
1.235 ± 12 mV 1.235 ± 25 mV	20	20 Typ	LM385BZ-1.2 LM385Z-1.2	LM285Z-1.2 (−40° to +85°C)	(Note 1)	1.0 (Note 2)	29
2.5 ± 38 mV 2.5 ± 75 mV			LM385BZ-2.5 LM385Z-2.5	LM285Z-2.5 (−40° to +85°C)		2.0 (Note 3)	
2.5 ± 25 mV	10	25	MC1403A	MC1503A	3.0/4.5 (Note 4)	10 (Note 6)	693, 751
		40	MC1403				
		55		MC1503			
5.0 ± 50 mV		25	MC1404AU5		6.0 (Note 5)		693
		40	MC1404U5				
		55		MC1504U5			
6.25 ± 60 mV		25	MC1404AU6				
		40	MC1404U6				
		55		MC1504U6			
10 ± 100 mV		25	MC1404AU10				
		40	MC1404U10				
		55		MC1504U10			
2.5 to 37	100	50 Typ	TL431C,AC	TL431I, AI (−40° to +85°C)	Shunt Reference Dynamic Impedance z ≤ 0.5		29,626 693
				TL431M			693

Notes: 1. Micro-Power Reference Diode Dynamic Impedance (z) ≤ 1.0 Ω at I_R = 100 μA
2. 10 μA ≤ I_R ≤ 1.0 mA
3. 20 μA ≤ I_R ≤ 1.0 mA
4. 4.5 V ≤ V_{in} ≤ 15 V/15 V ≤ V_{in} ≤ 40 V
5. (V_{out} + 2.5 V) ≤ V_{in} ≤ 40 V
6. 0 mA ≤ I_L ≤ 10 mA

VOLTAGE REFERENCES

Device	Function	Page
LM285	Micropower Voltage Reference Diodes	5-4
LM385	Micropower Voltage Reference Diode	5-4
MC1403,A	Precision Low Voltage Reference	5-8
MC1404,A	Precision Low Drift Voltage Reference	5-12
MC1503,A	Precision Low Voltage Reference	5-8
MC1504	Precision Low Drift Voltage Reference	5-12
TL431,A	Programmable Precision References	5-17

5

MOTOROLA

LM285
LM385

MICROPOWER VOLTAGE REFERENCE DIODES

SILICON MONOLITHIC INTEGRATED CIRCUIT

5

MICROPOWER VOLTAGE REFERENCE DIODES

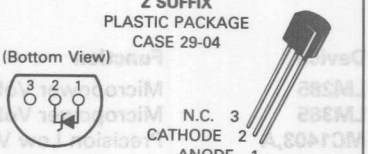
The LM285/LM385 series are micropower two-terminal bandgap voltage regulator diodes. Designed to operate over a wide current range of 10 μA to 20 mA, these devices feature exceptionally low dynamic impedance, low noise and stable operation over time and temperature. Tight voltage tolerances are achieved by on-chip trimming. The large dynamic operating range enables these devices to be used in applications with widely varying supplies with excellent regulation. Extremely low operating current make these devices ideal for micropower circuitry like portable instrumentation, regulators and other analog circuitry where extended battery life is required.

The LM285/LM385 series are packaged in a low cost TO-226AA plastic case and are available in two voltage versions of 1.235 and 2.500 volts as denoted by the device suffix (see ordering information table). The LM285 is specified over a −40°C to +85°C temperature range while the LM385 is rated from 0°C to +70°C.

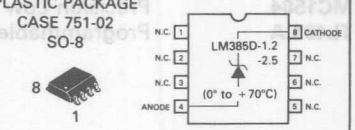
The LM385 is also available in a surface mount plastic package in voltages of 1.235 and 2.500 volts.

- Operating Current from 10 μA to 20 mA
- 1.0%, 1.5%, 2.0% and 3.0% Initial Tolerance Grades
- Low Temperature Coefficient
- 1.0 Ω Dynamic Impedance
- Surface Mount Package Available

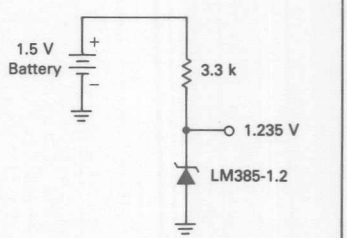
Z SUFFIX
PLASTIC PACKAGE
CASE 29-04



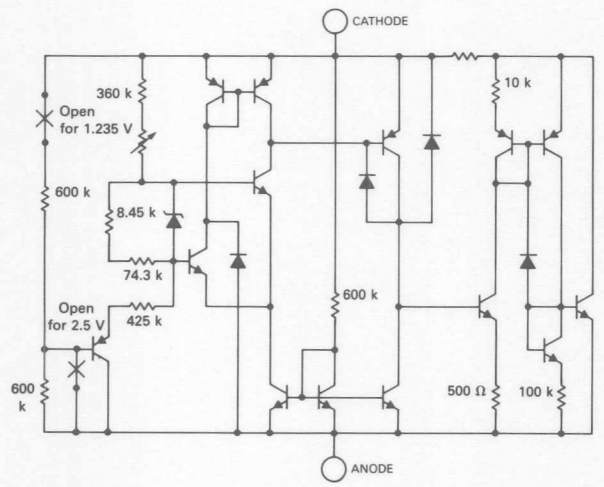
D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SO-8



STANDARD APPLICATION



EQUIVALENT CIRCUIT SCHEMATIC



ORDERING INFORMATION

Device	Temp. Range	Reverse Breakdown Voltage	Tolerance
LM285Z-1.2	−40°C to +85°C	1.235 Volts	±1.0%
LM285Z-2.5		2.500 Volts	±1.5%
LM385BZ-1.2	0°C to +70°C	1.235 Volts	±1.0%
LM385Z-1.2 LM385D-1.2		1.235 Volts	±2.0%
LM385BZ-2.5		2.500 Volts	±1.5%
LM385Z-2.5 LM385D-2.5		2.500 Volts	±3.0%

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Reverse Current	I_R	30	mA
Forward Current	I_F	10	mA
Operating Ambient Temperature Range LM285 LM385	T_A	 −40 to +85 0 to +70	°C
Operating Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	LM285-1.2			LM385-1.2/LM385B-1.2			Unit
		Min	Typ	Max	Min	Typ	Max	
Reverse Breakdown Voltage $I_{Rmin} \leq I_R \leq 20$ mA	$V_{(BR)R}$							V
LM285-1.2/LM385B-1.2		1.223	1.235	1.247	1.223	1.235	1.247	
$T_A = T_{low}$ to T_{high} (Note 1)		1.200	—	1.270	1.210	—	1.260	
LM385-1.2		—	—	—	1.205	1.235	1.260	
$T_A = T_{low}$ to T_{high} (Note 1)		—	—	—	1.192	—	1.273	
Minimum Operating Current	I_{Rmin}							μA
T_A = 25°C		—	8.0	10	—	8.0	15	
$T_A = T_{low}$ to T_{high} (Note 1)		—	—	20	—	—	20	
Reverse Breakdown Voltage Change with Current	$\Delta V_{(BR)R}$							mV
$I_{Rmin} \leq I_R \leq 1.0$ mA, T_A = +25°C		—	—	1.0	—	—	1.0	
$T_A = T_{low}$ to T_{high} (Note 1)		—	—	1.5	—	—	1.5	
1.0 mA $\leq I_R \leq$ 20 mA, T_A = +25°C		—	—	10	—	—	20	
$T_A = T_{low}$ to T_{high} (Note 1)		—	—	20	—	—	25	
Reverse Dynamic Impedance I_R = 100 μA, T_A = +25°C	Z	—	0.6	—	—	0.6	—	Ω
Average Temperature Coefficient 10 μA $\leq I_R \leq$ 20 mA, $T_A = T_{low}$ to T_{high} (Note 1)	$\Delta V_{(BR)}/\Delta T$	—	80	—	—	80	—	ppm/°C
Wideband Noise (RMS) I_R = 100 μA, 10 Hz ≤ f ≤ 10 kHz	n	—	60	—	—	60	—	μV
Long Term Stability I_R = 100 μA, T_A = +25°C ± 0.1°C	S	—	20	—	—	20	—	ppm/kHR

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	LM285-2.5			LM385-2.5/LM385B-2.5			Unit
		Min	Typ	Max	Min	Typ	Max	
Reverse Breakdown Voltage $I_{Rmin} \leq I_R \leq 20$ mA	$V_{(BR)R}$							V
LM285-2.5/LM385B-2.5		2.462	2.5	2.538	2.462	2.5	2.538	
$T_A = T_{low}$ to T_{high} (Note 1)		2.415	—	2.585	2.436	—	2.564	
LM385-2.5		—	—	—	2.425	2.5	2.575	
$T_A = T_{low}$ to T_{high} (Note 1)		—	—	—	2.400	—	2.600	
Minimum Operating Current	I_{Rmin}							μA
T_A = 25°C		—	13	20	—	13	20	
$T_A = T_{low}$ to T_{high} (Note 1)		—	—	30	—	—	30	
Reverse Breakdown Voltage Change with Current	$\Delta V_{(BR)R}$							mV
$I_{Rmin} \leq I_R \leq 1.0$ mA, T_A = +25°C		—	—	1.0	—	—	2.0	
$T_A = T_{low}$ to T_{high} (Note 1)		—	—	1.5	—	—	2.5	
1.0 mA $\leq I_R \leq$ 20 mA, T_A = +25°C		—	—	10	—	—	20	
$T_A = T_{low}$ to T_{high} (Note 1)		—	—	20	—	—	25	
Reverse Dynamic Impedance I_R = 100 μA, T_A = +25°C	Z	—	0.6	—	—	0.6	—	Ω
Average Temperature Coefficient 20 μA $\leq I_R \leq$ 20 mA, $T_A = T_{low}$ to T_{high} (Note 1)	$\Delta V_{(BR)}/\Delta T$	—	80	—	—	80	—	ppm/°C
Wideband Noise (RMS) I_R = 100 μA, 10 Hz ≤ f ≤ 10 kHz	n	—	120	—	—	120	—	μV
Long Term Stability I_R = 100 μA, T_A = +25°C ± 0.1°C	S	—	20	—	—	20	—	ppm/kHR

Note: 1. T_{low} = −40°C for LM285-1.2, LM285-2.5
= 0°C for LM385-1.2, LM385B-1.2, LM385-2.5, LM385B-2.5
T_{high} = +85°C for LM285-1.2, LM285-2.5
= +70°C for LM385-1.2, LM385B-1.2, LM385-2.5, LM385B-2.5

FIGURE 1 — REVERSE CHARACTERISTICS

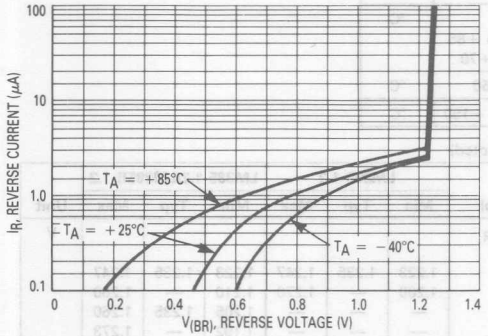


FIGURE 2 — REVERSE CHARACTERISTICS

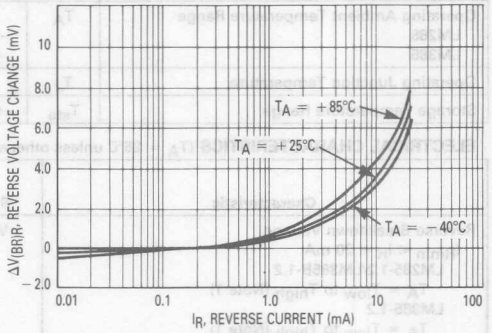


FIGURE 3 — FORWARD CHARACTERISTICS

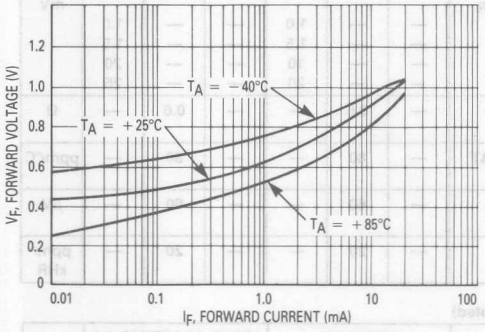


FIGURE 4 — TEMPERATURE DRIFT

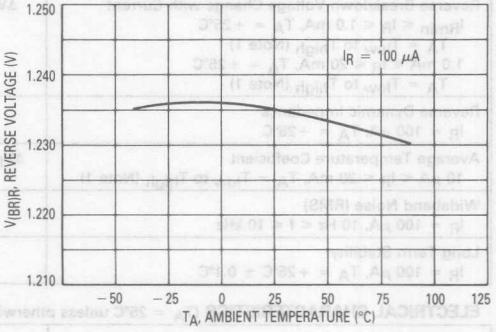


FIGURE 5 — NOISE VOLTAGE

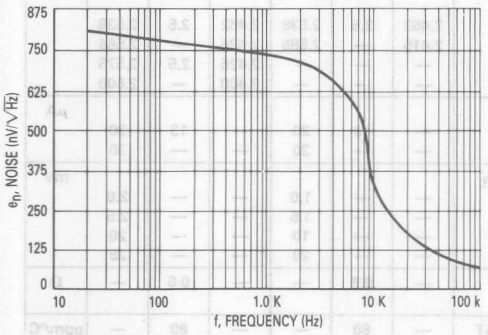
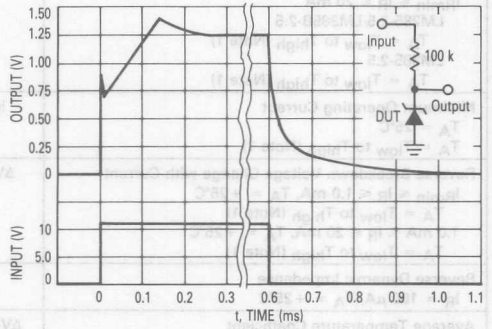


FIGURE 6 — RESPONSE TIME



TYPICAL PERFORMANCE CURVES FOR LM285-2.5/385-2.5/385B-2.5

FIGURE 7 — REVERSE CHARACTERISTICS

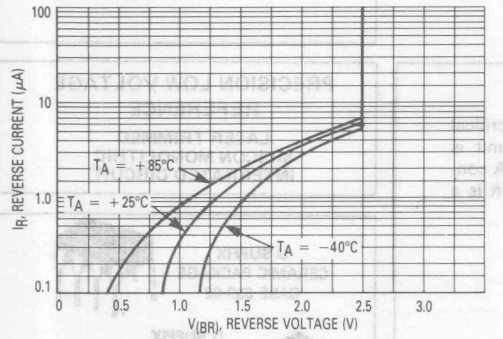


FIGURE 8 — REVERSE CHARACTERISTICS

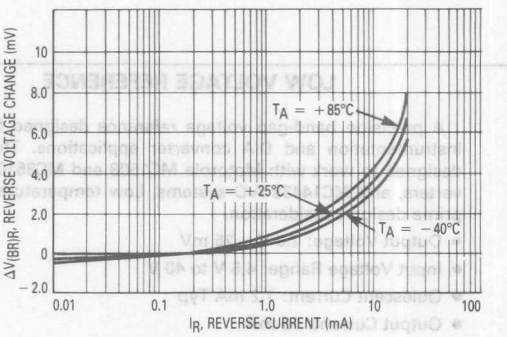


FIGURE 9 — FORWARD CHARACTERISTICS

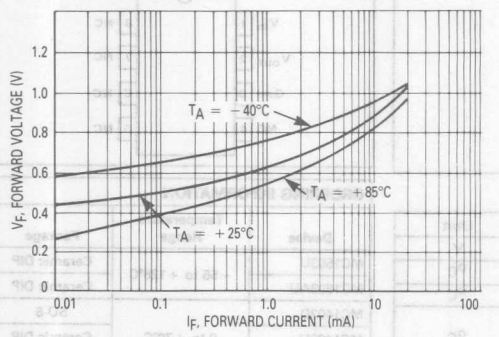


FIGURE 10 — TEMPERATURE DRIFT

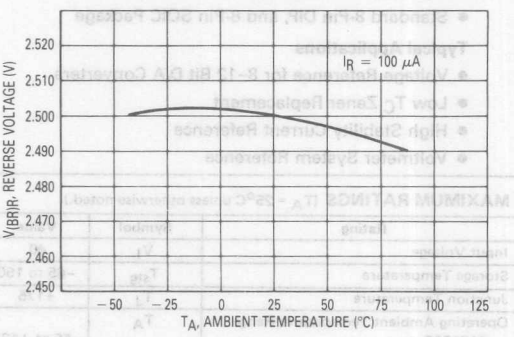


FIGURE 11 — NOISE VOLTAGE

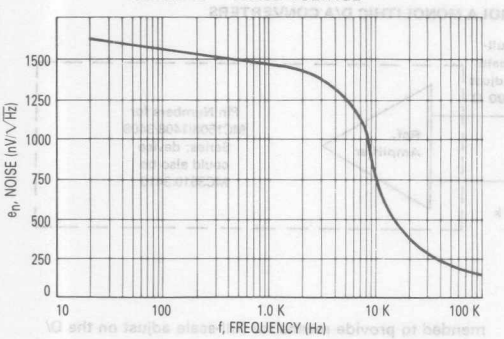
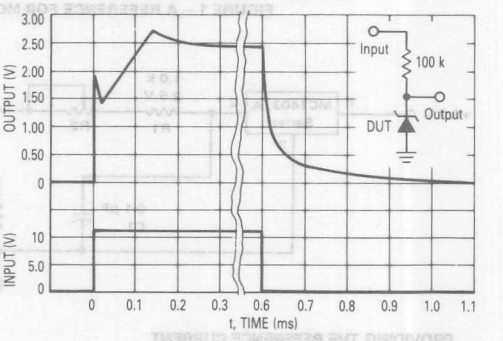


FIGURE 12 — RESPONSE TIME



5

MOTOROLA

MC1403,A
MC1503,A

LOW VOLTAGE REFERENCE

A precision band-gap voltage reference designed for critical instrumentation and D/A converter applications. This unit is designed to work with Motorola MC1508 and MC3510 D/A converters, and MC14433 A/D systems. Low temperature drift is a prime design consideration.

- Output Voltage: 2.5 V ±25 mV
- Input Voltage Range: 4.5 V to 40 V
- Quiescent Current: 1.2 mA Typ
- Output Current: 10 mA
- Temperature Coefficient: 10 ppm/°C Typ
- Guaranteed Temperature Drift Specification
- Equivalent to AD580
- Standard 8-Pin DIP, and 8-Pin SOIC Package

Typical Applications

- Voltage Reference for 8–12 Bit D/A Converters
- Low T_C Zener Replacement
- High Stability Current Reference
- Voltmeter System Reference

PRECISION LOW VOLTAGE REFERENCE

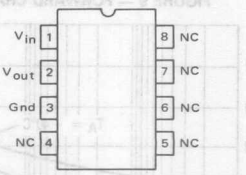
LASER TRIMMED SILICON MONOLITHIC INTEGRATED CIRCUIT



U SUFFIX
CERAMIC PACKAGE
CASE 693-02



D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SO-8



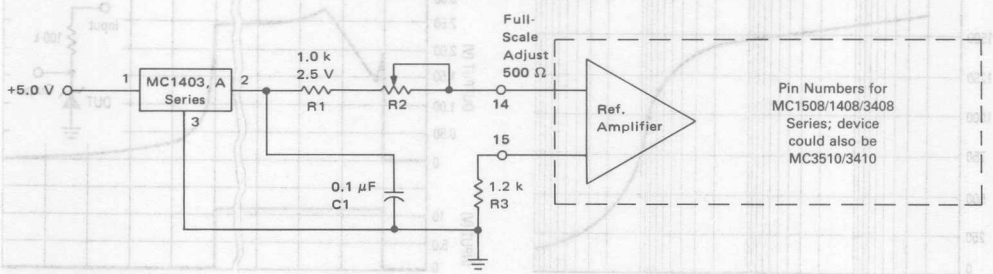
MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage	V_I	40	V
Storage Temperature	T_{stg}	−65 to 150	°C
Junction Temperature	T_J	+175	°C
Operating Ambient Temeprature Range	T_A		
MC1503,A		−55 to +125	°C
MC1403,A		0 to +70	°C

ORDERING INFORMATION

Device	Temperature Range	Package
MC1503U	−55 to +125°C	Ceramic DIP
MC1503AU		Ceramic DIP
MC1403D	0 to +70°C	SO-8
MC1403U		Ceramic DIP
MC1403AU		Ceramic DIP

FIGURE 1 – A REFERENCE FOR MOTOROLA MONOLITHIC D/A CONVERTERS



PROVIDING THE REFERENCE CURRENT FOR MOTOROLA MONOLITHIC D/A CONVERTERS

The MC1403/1503 makes an ideal reference for the Motorola monolithic D/A converters. The MC1408/1508, MC3410/3510 and MC3408 D/A converters all require a stable current reference of nominally 2.0 mA. This can be easily obtained from the MC1403/1503 with the addition of a series resistor, R1. A variable resistor, R2, is recommended to provide means for full-scale adjust on the D/A converter.

The resistor R3 improves temperature performance by matching the impedance on both inputs of the D/A reference amplifier. The capacitor decouples any noise present on the reference line. It is essential if the D/A converter is located any appreciable distance from the reference.

A single MC1403/1503 reference can provide the required current input for up to five of the monolithic D/A converters.

ELECTRICAL CHARACTERISTICS (V_{in} = 15 V, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (I_O = 0 mA)	V_{OUT}	2.475	2.50	2.525	V
Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$				ppm/°C
MC1503		–	–	55	
MC1503A		–	–	25	
MC1403		–	10	40	
MC1403A		–	10	25	
Output Voltage Change (over specified temperature range)	ΔV_O				mV
MC1503, MC1503A (−55°C to +125°C)		–	–	25	
		–	–	11	
MC1403, MC1403A (0°C to +70°C)		–	–	7.0	
		–	–	4.4	
Line Regulation (I_O = 0 mA)	Reg_{line}				mV
(15 V ≤ V_I ≤ 40 V)		–	1.2	4.5	
(4.5 V ≤ V_I ≤ 15 V)		–	0.6	3.0	
Load Regulation (0 mA < I_O < 10 mA)	Reg_{load}	–	–	10	mV
Quiescent Current (I_O = 0 mA)	I_Q	–	1.2	1.5	mA

FIGURE 2 – MC1403/1503 SCHEMATIC

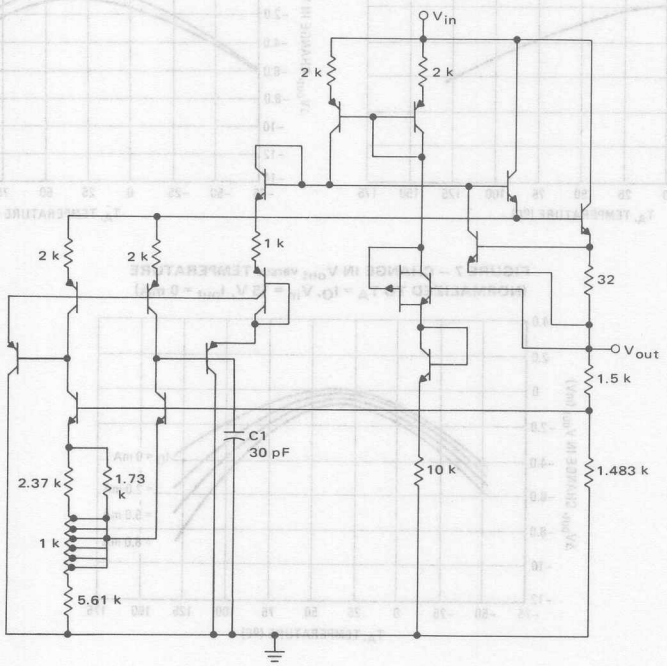


FIGURE 3 – TYPICAL CHANGE IN V_{out} versus V_{in}
(NORMALIZED TO V_{in} = 15 V @ T_C = 25°C)

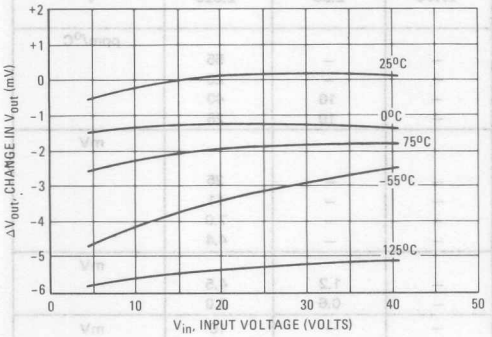


FIGURE 4 – CHANGE IN OUTPUT VOLTAGE
versus LOAD CURRENT
(NORMALIZED TO V_{out} @ V_{in} = 15 V, I_{out} = 0 mA)

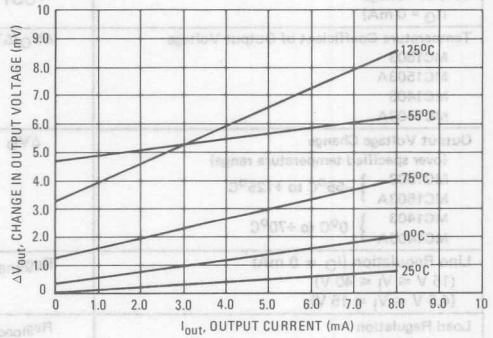


FIGURE 5 – QUIESCENT CURRENT versus TEMPERATURE
(V_{in} = 15 V, I_{out} = 0 mA)

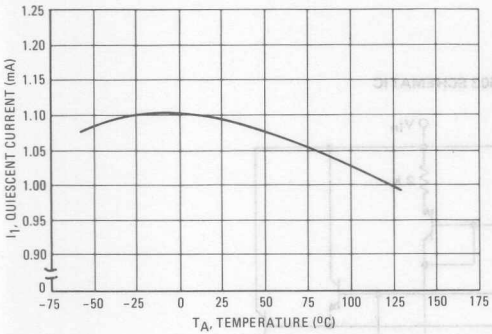


FIGURE 6 – CHANGE IN V_{out} versus TEMPERATURE
(NORMALIZED TO V_{out} @ V_{in} = 15 V)

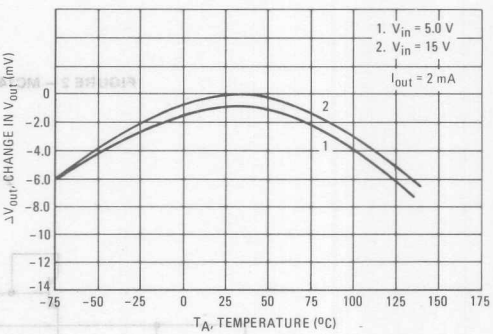
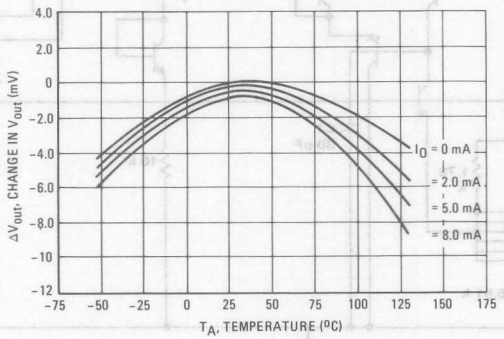


FIGURE 7 – CHANGE IN V_{out} versus TEMPERATURE
(NORMALIZED TO T_A = I_O, V_{in} = 15 V, I_{out} = 0 mA)



3-1/2-DIGIT VOLTMETER – COMMON ANODE DISPLAYS, FLASHING OVERRANGE

An example of a 3-1/2-digit voltmeter using the MC14433 is shown in the circuit diagram of Figure 8. The reference voltage for the system uses an MC1403 2.5 V reference IC. The full scale potentiometer can calibrate for a full scale of 199.9 mV or 1.999 V. When switching from 2 V to 200 mV operation, R_I is also changed, as shown on the diagram.

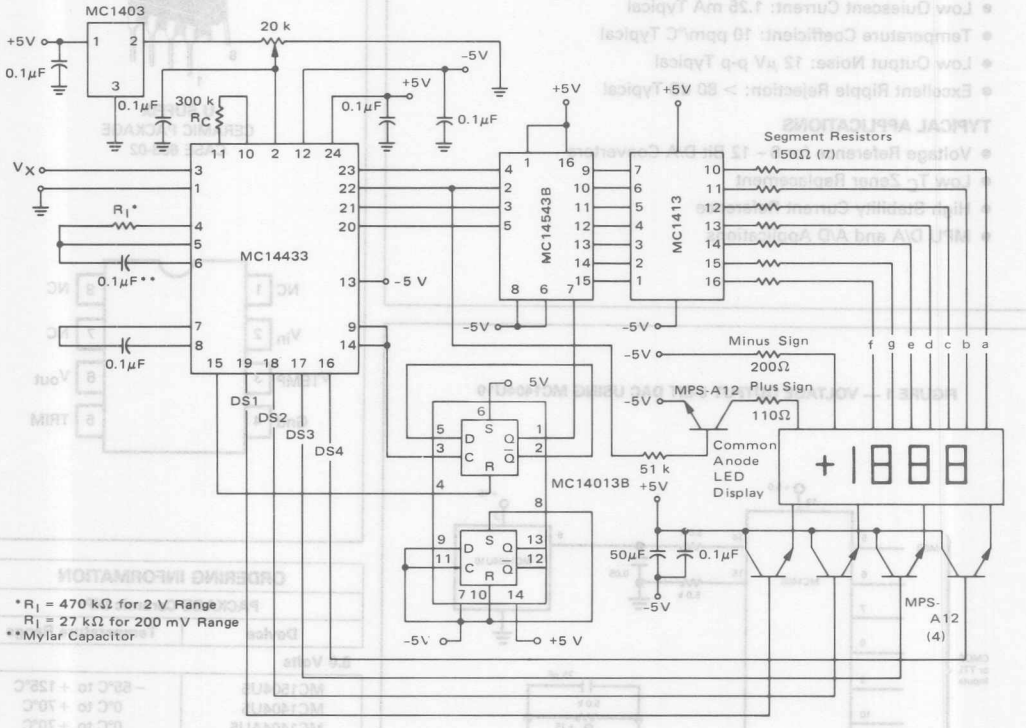
When using R_C equal to 300 kΩ, the clock frequency for the system is about 66 kHz. The resulting conversion time is approximately 250 ms.

When the input is overrange, the display flashes on and off. The flashing rate is one-half the conversion rate. This is done by dividing the EOC pulse rate by 2 with 1/2 MC14013B flip-flop and blanking the display using the blanking input of the MC14543B.

The display uses an LED display with common anode digit lines driven with an MC14543B decoder and an MC1413 LED driver. The MC1413 contains 7 Darlington transistor drivers and resistors to drive the segments of the display. The digit drive is provided by four MPS-A12 Darlington transistors operating in an emitter-follower configuration. The MC14543B, MC14013B and LED displays are referenced to V_{EE} via pin 13 of the MC14433. This places the full power supply voltage across the display. The current for the display may be adjusted by the value of the segment resistors shown as 150 ohms in Figure 8.

5

FIGURE 8 – 3-1/2-DIGIT VOLTMETER



MOTOROLA

MC1404
MC1404A
MC1504

PRECISION LOW DRIFT VOLTAGE REFERENCES

5.0, 6.25, and 10-VOLT OUTPUT VOLTAGES

LASER TRIMMED SILICON MONOLITHIC INTEGRATED CIRCUIT

5

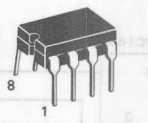
VOLTAGE REFERENCE FAMILY

The MC1404 series of ICs is a family of temperature-compensated voltage references for precision data conversion applications, such as A/D, D/A, V/F, and F/V. Advances in laser-trimming and ion-implanted devices, as well as monolithic fabrication techniques, make these devices stable and accurate to 12 bits over both military and commercial temperature ranges. In addition to excellent temperature stability, these parts offer excellent long-term stability and low noise.

- Output Voltages: Standard, 5.0 V, 6.25 V, 10 V
- Trimmable Output: > ±6%
- Wide Input Voltage Range: V_{ref} + 2.5 V to 40 V
- Low Quiescent Current: 1.25 mA Typical
- Temperature Coefficient: 10 ppm/°C Typical
- Low Output Noise: 12 μV p-p Typical
- Excellent Ripple Rejection: > 80 dB Typical

TYPICAL APPLICATIONS

- Voltage Reference for 8 – 12 Bit D/A Converters
- Low T_C Zener Replacement
- High Stability Current Reference
- MPU D/A and A/D Applications



U SUFFIX
CERAMIC PACKAGE
CASE 693-02

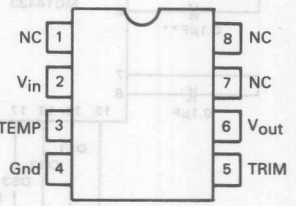
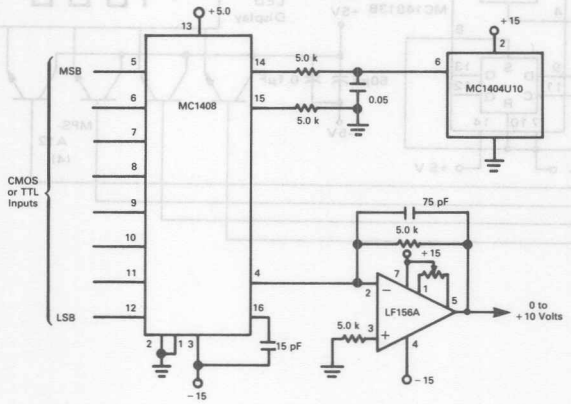


FIGURE 1 — VOLTAGE OUTPUT 8-BIT DAC USING MC1404U10



ORDERING INFORMATION	
PACKAGE Ceramic DIP	
Device	**Temperature Range**
5.0 Volts	
MC1504U5	−55°C to +125°C
MC1404U5	0°C to +70°C
MC1404AU5	0°C to +70°C
6.25 Volts	
MC1504U6	−55°C to +125°C
MC1404U6	0°C to +70°C
MC1404AU6	0°C to +70°C
10 Volts	
MC1504U10	−55°C to +125°C
MC1404U10	0°C to +70°C
MC1404AU10	0°C to +70°C

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	V_{in}	40	V
Storage Temperature	T_{stg}	-65 to +150	°C
Junction Temperature	T_J	+175	°C
Operating Ambient Temperature Range MC1504 MC1404,A	T_A	 -55 to +125 0 to +70	 °C °C

ELECTRICAL CHARACTERISTICS (V_{in} = 15 Volts, T_A = 25°C and Trim Terminal not connected unless otherwise noted)

Characteristic	Symbol	MC1404,A			MC1504			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (I_o = 0 mA)	V_o							Volt
MC1404U5, AU5/MC1504U5		4.95	5.00	5.05	4.95	5.00	5.05	
MC1404U6, AU6/MC1504U6		6.19	6.25	6.31	6.19	6.25	6.31	
MC1404U10, AU10/MC1504U10		9.90	10	10.10	9.90	10	10.10	
Output Voltage Tolerance	–	–	±0.1	±1.0	–	±0.1	±1.0	%
Output Trim Range (Figure 10) (R_P = 100 kΩ)	ΔV_{TRIM}	±6.0	–	–	±6.0	–	–	%
Output Voltage Temperature Coefficient, Over Full Temperature Range	$\Delta V_O/\Delta T$							ppm/°C
MC1404, MC1504		–	10	40	–	–	55	
MC1404A		–	10	25	–	–	–	
Maximum Output Voltage Change Over Temperature Range	ΔV_o							mV
MC1404U5, MC1504U5		–	–	14	–	–	50	
MC1404AU5		–	–	9.0	–	–	–	
MC1404U6, MC1504U6		–	–	17.5	–	–	62	
MC1404AU6		–	–	11	–	–	–	
MC1404U10, MC1504U10		–	–	28	–	–	99	
MC1404AU10		–	–	18	–	–	–	
Line Regulation (1) (V_{in} = V_{out} + 2.5 V to 40 V, I_{out} = 0 mA)	Reg_{line}	–	2.0	6.0	–	2.0	6.0	mV
Load Regulation (1) (0 ≤ I_o ≤ 10 mA)	Reg_{load}	–	–	10	–	–	10	mV
Quiescent Current (I_o = 0 mA)	I_Q	–	1.2	1.5	–	1.2	1.5	mA
Short Circuit Current	I_{sc}	–	20	30	–	–	30	mA
Long Term Stability	–	–	25	–	–	25	–	ppm/1000 hrs

Note 1: Includes thermal effects.

DYNAMIC CHARACTERISTICS (V_{in} = 15 V, T_A = 25°C all voltage ranges unless otherwise noted)

Characteristic	Symbol	MC1404,A			MC1504			Unit
		Min	Typ	Max	Min	Typ	Max	
Turn-On Settling Time (to ±0.01%)	t_S	–	50	–	–	50	–	μs
Output Noise Voltage – P to P (Bandwidth 0.1 to 10 Hz)	V_n	–	12	–	–	12	–	μV
Small-Signal Output Impedance	r_o							Ω
120 Hz		–	0.15	–	–	0.15	–	
500 Hz		–	0.2	–	–	0.2	–	
Power Supply Rejection Ratio	PSRR	70	80	–	70	80	–	dB

5

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FIGURE 2 – SIMPLIFIED DEVICE DIAGRAM

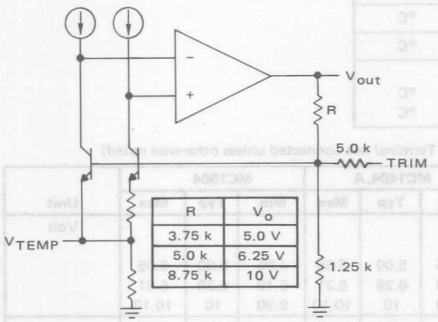


FIGURE 3 – LINE REGULATION versus TEMPERATURE

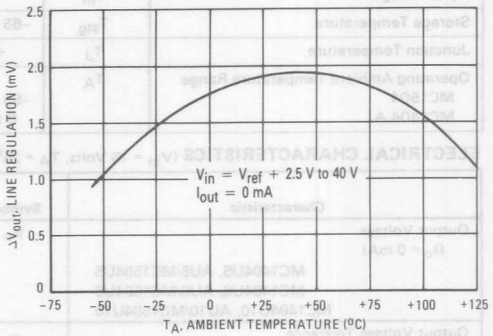


FIGURE 4 – OUTPUT VOLTAGE versus TEMPERATURE
MC1404U10

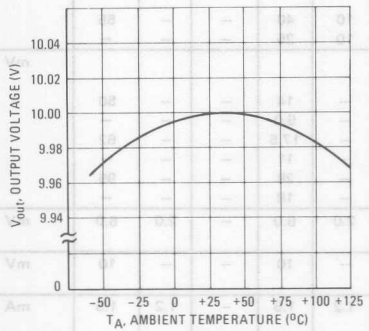


FIGURE 5 – LOAD REGULATION versus TEMPERATURE

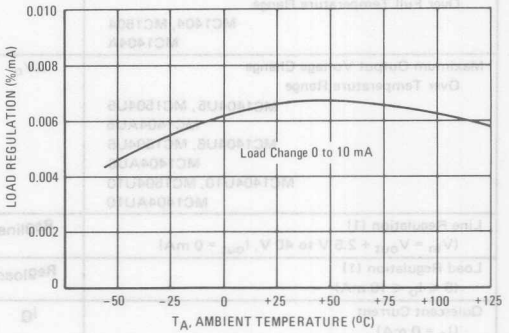


FIGURE 6 – POWER SUPPLY REJECTION RATIO versus FREQUENCY

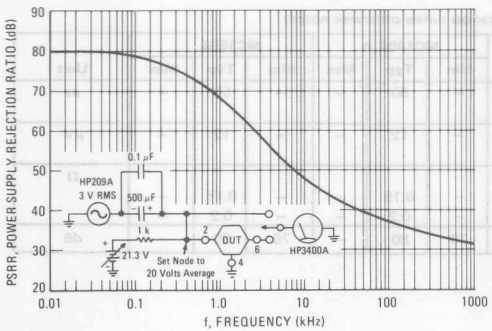


FIGURE 7 – QUIESCENT CURRENT versus TEMPERATURE

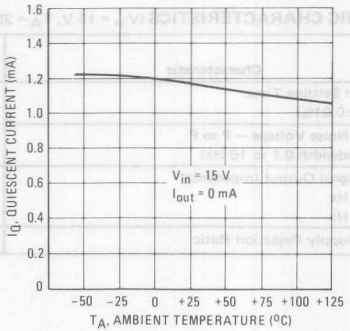


FIGURE 8 – SHORT CIRCUIT CURRENT versus TEMPERATURE

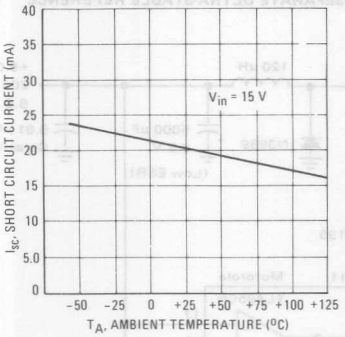
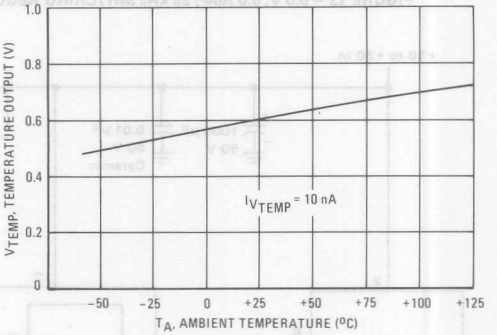
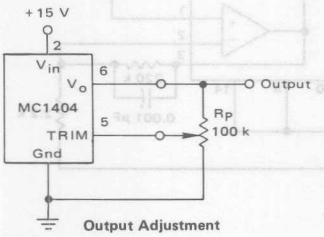


FIGURE 9 – V_{TEMP} OUTPUT versus TEMPERATURE



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FIGURE 10 – OUTPUT TRIM CONFIGURATION

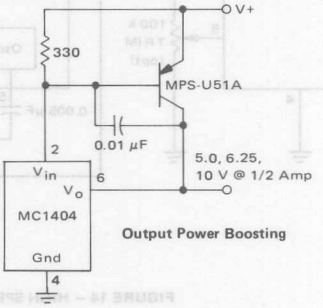


Output Adjustment

The MC1404 trim terminal can be used to adjust the output voltage over a ±6% range. For example, the output can be set to 10.000 V or to 10.240 V for binary applications. For trimming, Bourns type 3059, 100 kΩ or 200 kΩ trimpot is recommended.

Although Figure 10 illustrates a wide trim range, temperature coefficients may become unpredictable for trim > ±6.0%.

FIGURE 11 – PRECISION SUPPLY USING MC1404



Output Power Boosting

The addition of a power transistor, a resistor, and a capacitor converts the MC1404 into a precision supply with one ampere current capability. At V+ = 15 V, the MC1404 can carry in excess of 14 mA of load current with good regulation. If the power transistor current gain exceeds 75, a one ampere supply can be realized.

FIGURE 12 – ULTRA STABLE REFERENCE FOR MC1723 VOLTAGE REGULATOR

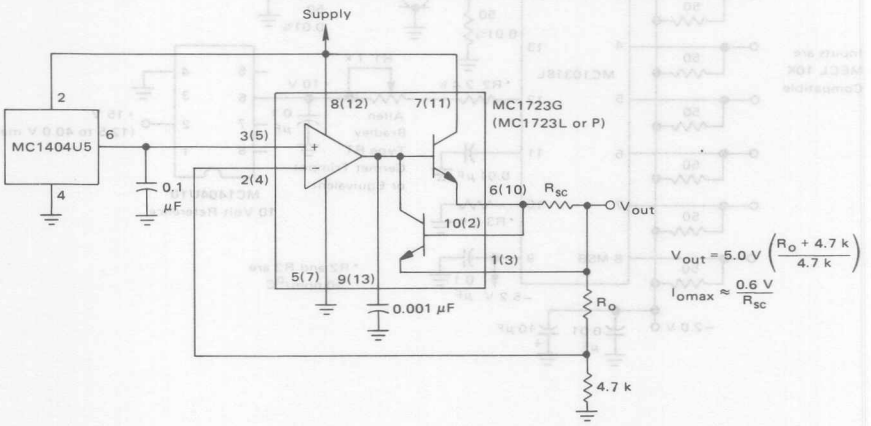


FIGURE 13 – 5.0 V, 6.0 AMP, 25 kHz SWITCHING REGULATOR WITH SEPARATE ULTRA-STABLE REFERENCE

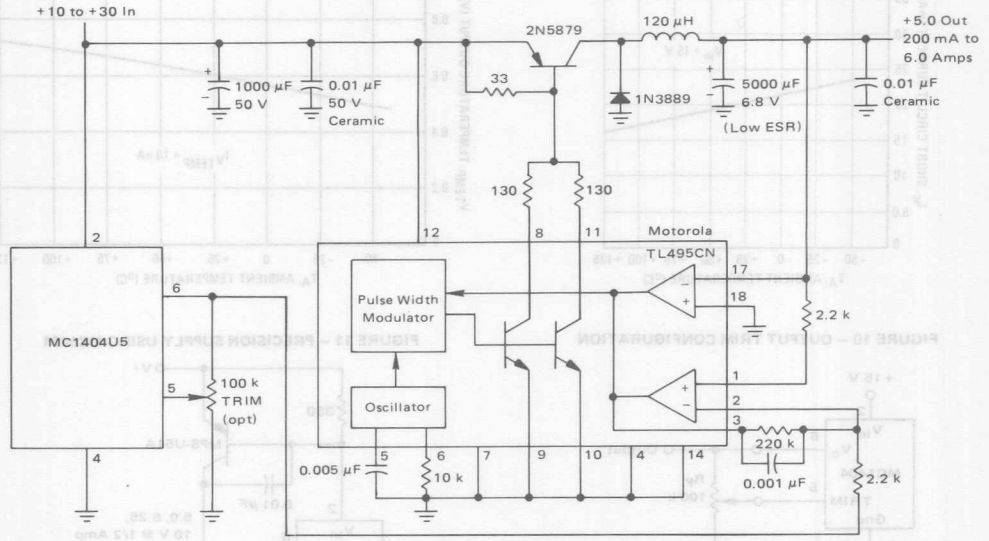
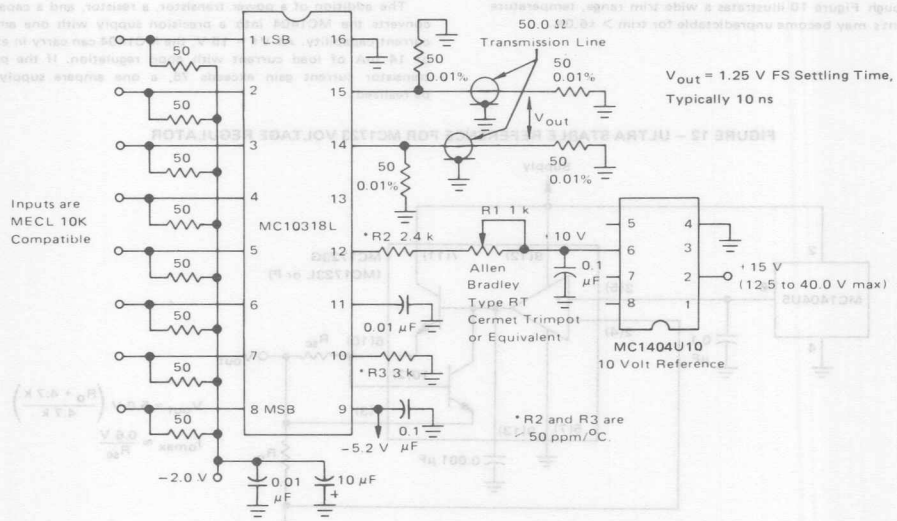


FIGURE 14 – HIGH SPEED 8-BIT D/A CONVERTER USING MC1404U10

I_{FS} is set to 51.000 mA with R1



MOTOROLA

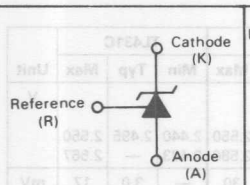
TL431,A Series

Specifications and Applications Information

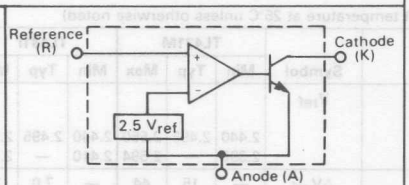
PROGRAMMABLE PRECISION REFERENCES

The TL431,A integrated circuits are three-terminal programmable shunt regulator diodes. These monolithic IC voltage references operate as a low temperature coefficient zener which is programmable from V_{ref} to 36 volts with two external resistors. These devices exhibit a wide operating current range of 1.0 to 100 mA with a typical dynamic impedance of 0.22 Ω. The characteristics of these references make them excellent replacements for zener diodes in many applications such as digital voltmeters, power supplies, and op amp circuitry. The 2.5 volt reference makes it convenient to obtain a stable reference from 5.0 volt logic supplies, and since the TL431,A operates as a shunt regulator, it can be used as either a positive or negative voltage reference.

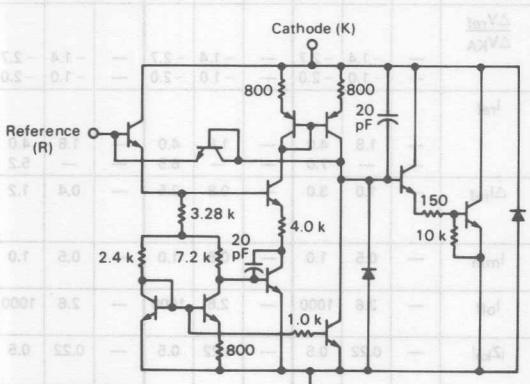
- Programmable Output Voltage to 36 Volts
- Voltage Reference Tolerance: ±1.0% (TL431,A)
- Low Dynamic Output Impedance, 0.22 Ω Typical
- Sink Current Capability of 1.0 to 100 mA
- Equivalent Full-Range Temperature Coefficient of 50 ppm/°C Typical
- Temperature Compensated for Operation over Full Rated Operating Temperature Range
- Low Output Noise Voltage



SYMBOL



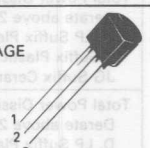
FUNCTIONAL BLOCK DIAGRAM



INTERNAL SCHEMATIC
Component values are nominal

PROGRAMMABLE PRECISION REFERENCES

SILICON MONOLITHIC INTEGRATED CIRCUITS



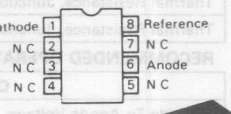
LP SUFFIX
PLASTIC PACKAGE
CASE 29-04

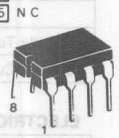
Pin 1. Reference
2. Anode
3. Cathode



P SUFFIX
PLASTIC PACKAGE
CASE 626-05

(Top View)





JG SUFFIX
CERAMIC PACKAGE
CASE 693-02



D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SOP-8

PIN 1. CATHODE
2. ANODE
3. ANODE
4. N.C.
5. N.C.
6. ANODE
7. ANODE
8. REFERENCE

SOP-8 is an internally modified SO-8 Package. Pins 2, 3, 6 and 7 are electrically common to the die attach flag. This internal lead frame modification decreases package thermal resistance and increases power dissipation capability when appropriately mounted on a printed circuit board. SOP-8 conforms to all external dimensions of the standard SO-8 Package.

ORDERING INFORMATION

Device	Temperature Range	Package
TL431CLP,ACLP	0 to +70°C	Plastic
TL431CP,ACP	0 to +70°C	Plastic DIP
TL431CD,ACD	0 to +70°C	SOP-8
TL431CJG	0 to +70°C	Ceramic DIP
TL431ILP,AILP	−40 to +85°C	Plastic
TL431IP,AIP	−40 to +85°C	Plastic DIP
TL431IJG	−40 to +85°C	Ceramic DIP
TL431MJG	−55 to +125°C	Ceramic DIP

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Rating	Symbol	Value	Unit
Cathode To Anode Voltage	V_{KA}	37	V
Cathode Current Range, Continuous	I_K	−100 to +150	mA
Reference Input Current Range, Continuous	I_{ref}	−0.05 to +10	mA
Operating Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range TL431M TL431I, TL431AI TL431C, TL431AC	T_A	 −55 to +125 −40 to +85 0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C Ambient Temperature D, LP Suffix Plastic Package P Suffix Plastic Package JG Suffix Ceramic Package	P_D	 0.70 1.10 1.25	W
Total Power Dissipation @ T_C = 25°C Derate above 25°C Case Temperature D, LP Suffix Plastic Package P Suffix Plastic Package JG Suffix Ceramic Package	P_D	 1.5 3.0 3.3	W

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THERMAL CHARACTERISTICS

Characteristics	Symbol	D, LP Suffix Package	P Suffix Package	JG Suffix package	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	178	114	100	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83	41	38	°C/W

RECOMMENDED OPERATING CONDITIONS

Condition/Value	Symbol	Min	Max	Unit
Cathode To Anode Voltage	V_{KA}	V_{ref}	36	V
Cathode Current	I_K	1.0	100	mA

ELECTRICAL CHARACTERISTICS (Ambient temperature at 25°C unless otherwise noted)

Characteristic	Symbol	TL431M			TL431I			TL431C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reference Input Voltage (Figure 1) $V_{KA} = V_{ref}$, I_K = 10 mA T_A = +25°C $T_A = T_{low}$ to T_{high} (Note 1)	V_{ref}	 2.440 2.396	 2.495 —	 2.550 2.594	 2.440 2.410	 2.495 —	 2.550 2.580	 2.440 2.423	 2.495 —	 2.550 2.567	V
Reference Input Voltage Deviation Over Temperature Range (Figure 1, Note 1, 2, 4) $V_{KA} = V_{ref}$, I_K = 10 mA	ΔV_{ref}	—	15	44	—	7.0	30	—	3.0	17	mV
Ratio of Change in Reference Input Voltage to Change in Cathode to Anode Voltage I_K = 10 mA (Figure 2), ΔV_{KA} = 10 V to V_{ref} ΔV_{KA} = 36 V to 10 V	$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	 — —	 −1.4 −1.0	 −2.7 −2.0	 — —	 −1.4 −1.0	 −2.7 −2.0	 — —	 −1.4 −1.0	 −2.7 −2.0	mV/V
Reference Input Current (Figure 2) I_K = 10 mA, R1 = 10 k, R2 = ∞ T_A = +25°C $T_A = T_{low}$ to T_{high} (Note 1)	I_{ref}	 — —	 1.8 —	 4.0 7.0	 — —	 1.8 —	 4.0 6.5	 — —	 1.8 —	 4.0 5.2	μA
Reference Input Current Deviation Over Temperature Range (Figure 2, Note 1, 4) I_K = 10 mA, R1 = 10 k, R2 = ∞	ΔI_{ref}	—	1.0	3.0	—	0.8	2.5	—	0.4	1.2	μA
Minimum Cathode Current For Regulation $V_{KA} = V_{ref}$ (Figure 1)	I_{min}	—	0.5	1.0	—	0.5	1.0	—	0.5	1.0	mA
Off-State Cathode Current (Figure 3) V_{KA} = 36 V, V_{ref} = 0 V	I_{off}	—	2.6	1000	—	2.6	1000	—	2.6	1000	nA
Dynamic Impedance (Figure 1, Note 3) $V_{KA} = V_{ref}$, ΔI_K = 1.0 mA to 100 mA f ≤ 1.0 kHz	$\lvert Z_{ka} \rvert$	—	0.22	0.5	—	0.22	0.5	—	0.22	0.5	Ω

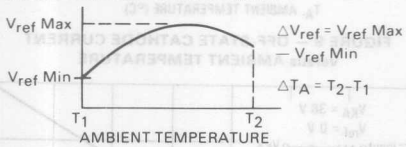
ELECTRICAL CHARACTERISTICS (Ambient temperature at 25°C unless otherwise noted)

Characteristic	Symbol	TL431AI Min	TL431AI Typ	TL431AI Max	TL431AC Min	TL431AC Typ	TL431AC Max	Unit
Reference Input Voltage (Figure 1) $V_{KA} = V_{ref}$, I_K = 10 mA	V_{ref}							V
T_A = +25°C		2.470	2.495	2.520	2.470	2.495	2.520	
$T_A = T_{low}$ to T_{high} (Note 4)		2.440	—	2.550	2.453	—	2.537	
Reference Input Voltage Deviation Over Temperature Range (Figure 1, Note 1, 2) $V_{KA} = V_{ref}$, I_K = 10 mA	ΔV_{ref}	—	7.0	30	—	3.0	17	mV
Ratio of Change in Reference Input Voltage to Change in Cathode to Anode Voltage	$\frac{\Delta V_{ref}}{\Delta V_{KA}}$							mV/V
I_K = 10 mA (Figure 2), ΔV_{KA} = 10 V to V_{ref}		—	−1.4	−2.7	—	−1.4	−2.7	
ΔV_{KA} = 36 V to 10 V		—	−1.0	−2.0	—	−1.0	−2.0	
Reference Input Current (Figure 2) I_K = 10 mA, R1 = 10 k, R2 = ∞	I_{ref}							μA
T_A = +25°C		—	1.8	4.0	—	1.8	4.0	
$T_A = T_{low}$ to T_{high} (Note 1)		—	—	6.5	—	—	5.2	
Reference Input Current Deviation Over Temperature Range (Figure 2, Note 1) I_K = 10 mA, R1 = 10 k, R2 = ∞	ΔI_{ref}	—	0.8	2.5	—	0.4	1.2	μA
Minimum Cathode Current For Regulation $V_{KA} = V_{ref}$ (Figure 1)	I_{min}	—	0.5	1.0	—	0.5	1.0	mA
Off-State Cathode Current (Figure 3) V_{KA} = 36 V, V_{ref} = 0 V	I_{off}	—	2.6	1000	—	2.6	1000	nA
Dynamic Impedance (Figure 1, Note 3) $V_{KA} = V_{ref}$, ΔI_K = 1.0 mA to 100 mA f ≤ 1.0 kHz	$\lvert Z_{ka} \rvert$	—	0.22	0.5	—	0.22	0.5	Ω

Note 1:
T_{low} = −55°C for TL431MJG
= −40°C for TL431AIP, TL431AILP, TL431IP, TL431ILP, TL431IJG
= 0°C for TL431ACP, TL431ACLP, TL431CP, TL431CLP, TL431CJG, TL431CD, TL431ACD

T_{high} = +125°C for TL431MJG
= +85°C for TL431AIP, TL431AILP, TL431IP, TL431ILP, TL431IJG
= +70°C for TL431ACP, TL431ACLP, TL431CP, TL431CLP, TL431CJG, TL431CD, TL431ACD

Note 2:
The deviation parameter ΔV_{ref} is defined as the differences between the maximum and minimum values obtained over the full operating ambient temperature range that applies.



The average temperature coefficient of the reference input voltage, αV_{ref}, is defined as:

$$\alpha V_{ref} \frac{ppm}{°C} = \frac{\left(\frac{\Delta V_{ref}}{V_{ref} @ 25°C}\right) \times 10^6}{\Delta T_A} = \frac{\Delta V_{ref} \times 10^6}{\Delta T_A (V_{ref} @ 25°C)}$$

αV_{ref} can be positive or negative depending on whether V_{ref} Min or V_{ref} Max occurs at the lower ambient temperature. (Refer to Figure 6)

Example: ΔV_{ref} = 8.0 mV and slope is positive, V_{ref} @ 25°C = 2.495 V, ΔT_A = 70°C

$$\alpha V_{ref} = \frac{0.008 \times 10^6}{70\ (2.495)} = 45.8\ ppm/°C$$

Note 3:
The dynamic impedance Z_{ka} is defined as: $\lvert Z_{ka} \rvert = \frac{\Delta V_{KA}}{\Delta I_K}$

When the device is programmed with two external resistors, R1 and R2, (refer to Figure 2) the total dynamic impedance of the circuit is defined as:

$$\lvert Z_{ka}' \rvert \approx \lvert Z_{ka} \rvert \left(1 + \frac{R1}{R2}\right)$$

Note 4:
This test is not applicable to surface mount (D suffix) devices.

FIGURE 1 — TEST CIRCUIT FOR $V_{KA} = V_{ref}$

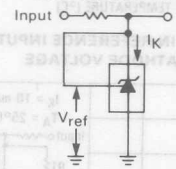


FIGURE 2 — TEST CIRCUIT FOR $V_{KA} > V_{ref}$

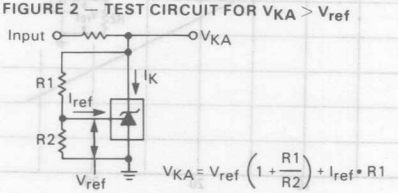
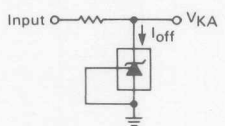


FIGURE 3 — TEST CIRCUIT FOR I_{off}



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FIGURE 4 — CATHODE CURRENT versus CATHODE VOLTAGE

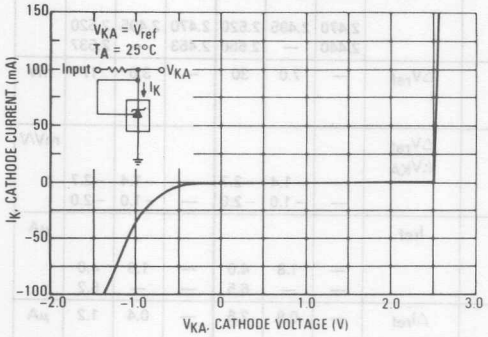


FIGURE 5 — CATHODE CURRENT versus CATHODE VOLTAGE

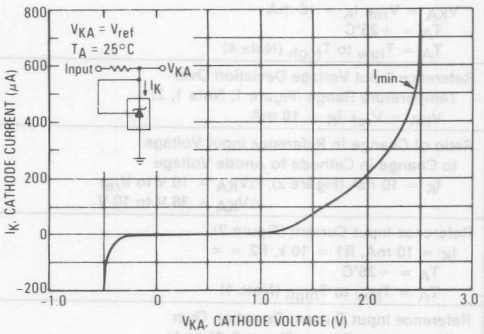


FIGURE 6 — REFERENCE INPUT VOLTAGE versus AMBIENT TEMPERATURE

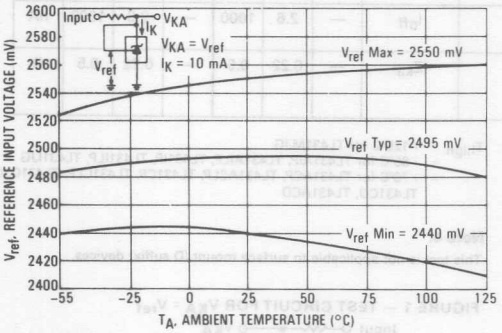


FIGURE 7 — REFERENCE INPUT CURRENT versus AMBIENT TEMPERATURE

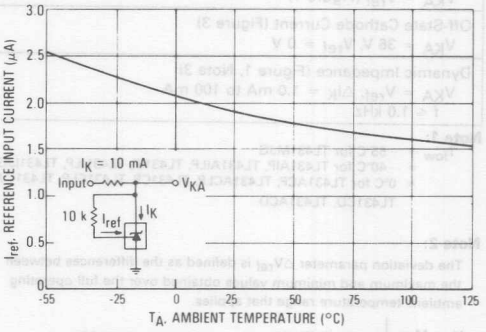


FIGURE 8 — CHANGE IN REFERENCE INPUT VOLTAGE versus CATHODE VOLTAGE

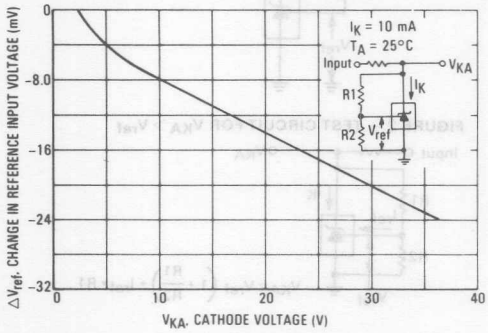


FIGURE 9 — OFF-STATE CATHODE CURRENT versus AMBIENT TEMPERATURE

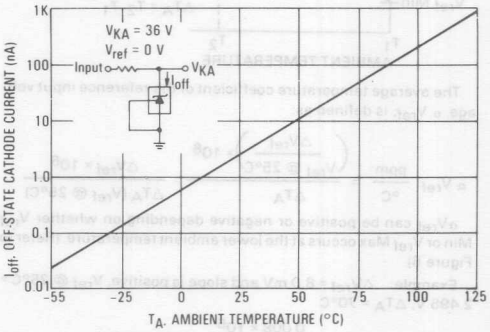


FIGURE 10 — DYNAMIC IMPEDANCE versus FREQUENCY

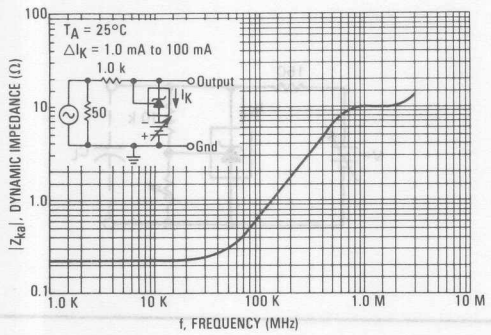
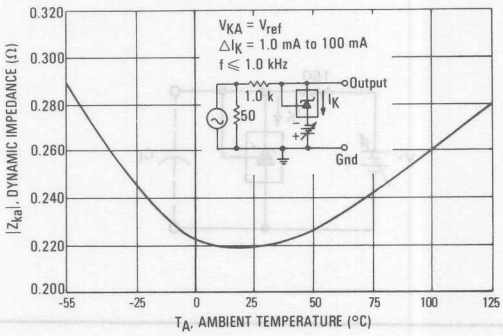


FIGURE 11 — DYNAMIC IMPEDANCE versus AMBIENT TEMPERATURE



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FIGURE 12 — OPEN LOOP VOLTAGE GAIN versus FREQUENCY

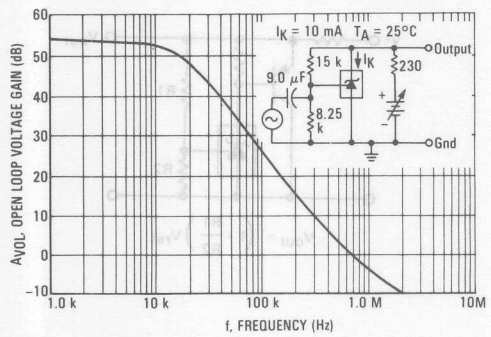


FIGURE 13 — SPECTRAL NOISE DENSITY

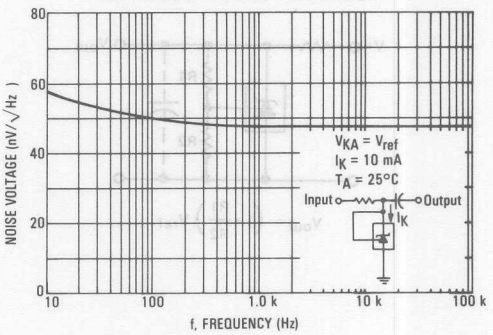


FIGURE 14 — PULSE RESPONSE

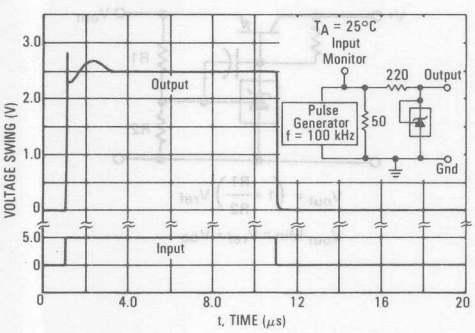
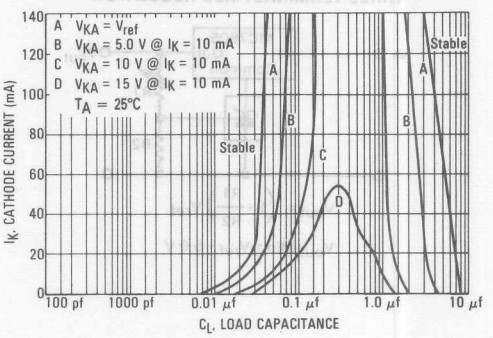
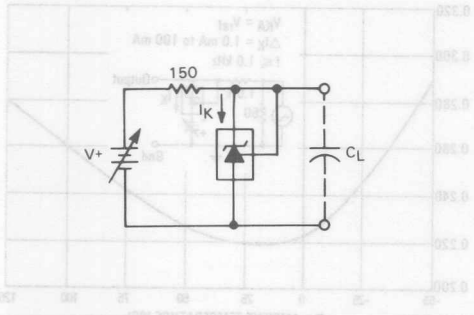


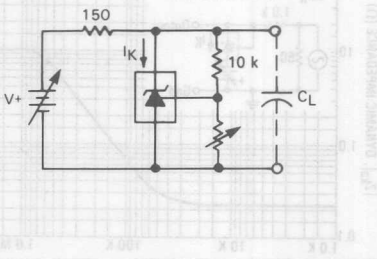
FIGURE 15 — STABILITY BOUNDARY CONDITIONS



OF STABILITY BOUNDARY CONDITIONS



OF STABILITY BOUNDARY CONDITIONS



5

TYPICAL APPLICATIONS

FIGURE 18 — SHUNT REGULATOR

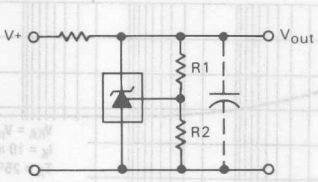


FIGURE 19 — HIGH CURRENT SHUNT REGULATOR

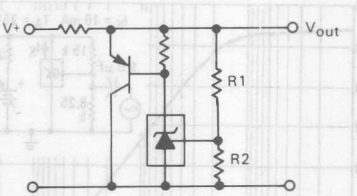


FIGURE 20 — OUTPUT CONTROL OF A THREE-TERMINAL FIXED REGULATOR

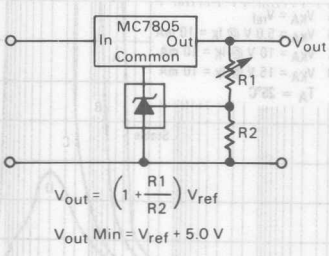


FIGURE 21 — SERIES PASS REGULATOR

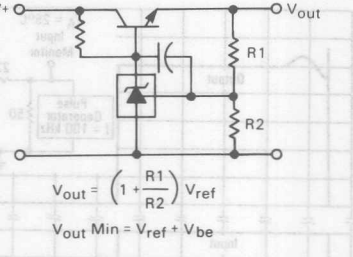


FIGURE 22 — CONSTANT CURRENT SOURCE

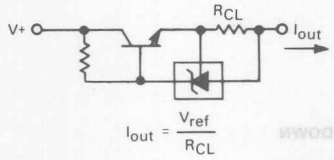


FIGURE 23 — CONSTANT CURRENT SINK

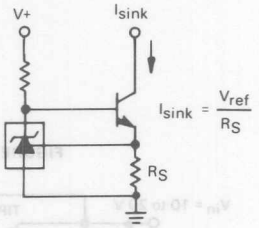


FIGURE 24 — TRIAC CROWBAR

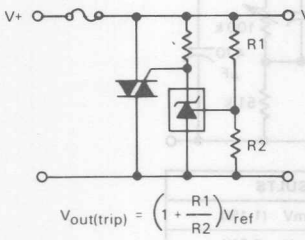


FIGURE 25 — SCR CROWBAR

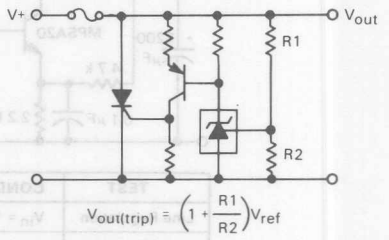
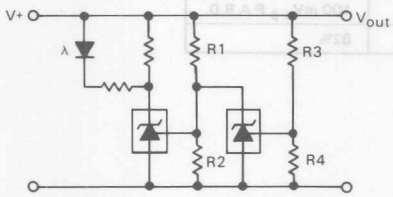


FIGURE 26 — VOLTAGE MONITOR

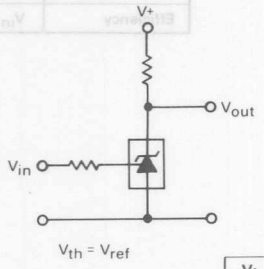


L.E.D. indicator is 'on' when V+ is between the upper and lower limits.

$$\text{Lower Limit} = \left(1 + \frac{R1}{R2}\right)V_{ref}$$

$$\text{Upper Limit} = \left(1 + \frac{R3}{R4}\right)V_{ref}$$

FIGURE 27 — SINGLE-SUPPLY COMPARATOR WITH TEMPERATURE-COMPENSATED THRESHOLD



V_{in}	V_{out}
$<V_{ref}$	V+
$>V_{ref}$	≈ 2.0 V

FIGURE 28 — LINEAR OHMMETER

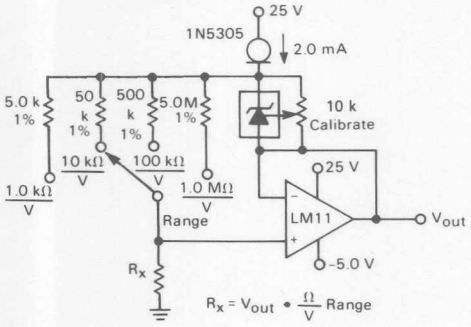
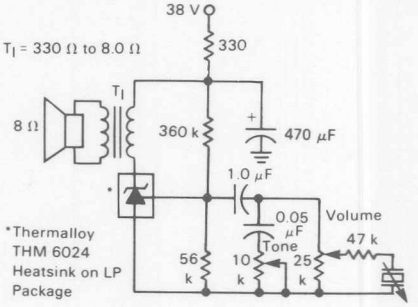
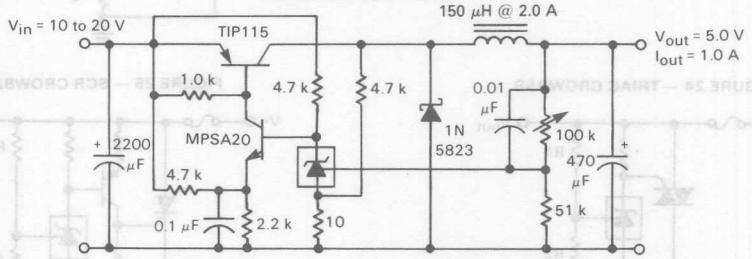


FIGURE 29 — SIMPLE 400 mW PHONO AMPLIFIER

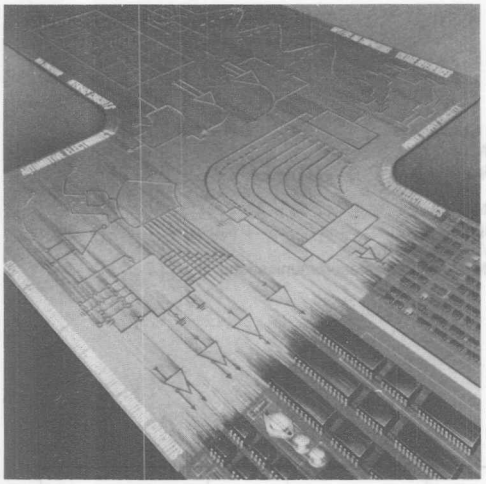


5

FIGURE 30 — HIGH EFFICIENCY STEP-DOWN SWITCHING CONVERTER



TEST	CONDITIONS	RESULTS
Line Regulation	V_{in} = 10 V to 20 V, I_o = 1.0 A	53 mV (1.1%)
Load Regulation	V_{in} = 15 V, I_o = 0A to 1.0 A	25 mV (0.5%)
Output Ripple	V_{in} = 10 V, I_o = 1.0 A	50 mV_{p-p} P.A.R.D.
Output Ripple	V_{in} = 20 V, I_o = 1.0 A	100 mV_{p-p} P.A.R.D.
Efficiency	V_{in} = 15 V, I_o = 1.0 A	82%



In Brief . . .

Motorola's line of digital-to-analog and analog-to-digital converters include several well established industry standards, and many are available in various linearity grades so as to suit most any application.

The A/D converters have 7 and 8-bit flash converters suitable for NTSC and PAL systems, a 1.8 μs SAR converter, CMOS 8 to 10-bit converters, as well as other high-speed digitizing applications.

The D/A converters have 6 and 8-bit devices, video speed (for NTSC and PAL) devices, and triple video DAC with on-board color pallette for color graphics applications.

Data Conversion

6

Selector Guide

A-D Converters 6-2
D-A Converters 6-3
A-D/D-A Converters 6-3

Alphanumeric Listing 6-4

Related Application Notes 6-4

Data Sheets 6-5

Data Conversion

The line of data conversion products which Motorola offers spans a wide spectrum of speed and resolution/accuracy. Features, including bus compatibility, minimize external parts count and provide easy interface to microprocessor systems. Various technologies, such as Bipolar and CMOS, are utilized to achieve functional capability, accuracy and production repeatability. Bipolar technology generally results in higher speed, while CMOS devices offer greatly reduced power consumption.

A-D Converters
CMOS 6-2
Bipolar 6-2
D-A Converters
CMOS 6-3
Bipolar 6-3
A-D/D-A Converters
CMOS — For Telecommunications 6-3

6

A-D Converters

CMOS

Resolution (Bits)	Device	Nonlinearity (Max)	Conversion Time	Input Voltage Range	Supplies (V)	Temperature Range	Package	Comments
8	MC145040	±1/2 LSB	10 μs	0 to V_{DD}	+5.0 ±10%	−40°C to +85°C	P/738 FN/775	Requires External Clock
	MC145041		20 μs					Includes Internal Clock
	MC14442		32 μs			−40°C to +85°C	P/710 FN/776	μP Compatible 11-Channel MUX S.A.R.
	MC14549B MC14559B	successive approximation registers			+3.0 to +18	−55°C to +125°C −40°C to +85°C	L/620 P/648	Compatible with MC1408 S.A.R. 8-bit D-A Converter
8–10	MC14443/47	±0.5% Full Scale	300 μs	Variable w/Supply	+5.0 to +18	−40°C to +85°C	P/648 DW/751G	μP Compatible, Single Slope, 6-Channel MUX
3-1/2 Digit	MC14433	±0.05% ±1 Count	40 ms	±2.0 V ±200 mV	+5.0, +8.0		P/709	Dual Slope

Bipolar

7	MC10321	±1/2 LSB	40 ns	0 to 2.0 V_{p-p} Max	+5.0 V and −3.0 V to −6.0 V	0°C to +70°C	P/738 DW/751D	Video Speed, Grey Code
8	MC10319	±1 LSB					L/623 P/709 DW/751F Die Form	Video Speed Flash Converter, Internal Grey Code
	MC6108	±1/2 LSB	1.8 μs	±5.0 V 0 to 5.0 V 0 to 10 V	+5.0, −5.2		P/710	μP Compatible, Three-State Outputs, includes Reference

D-A Converters

CMOS

Resolution (Bits)	Device	Suffix	Accuracy @ 25°C (Max)	Max Settling Time (±1/2 LSB)	Supplies (V)	Temperature Range	Package	Comments
6	MC144110	P	—	—	+5.0 to +15	0°C to +85°C	707	Serial input, Hex DAC, 6 outputs
	MC144111	P DW					646 751G	Serial input, Quad DAC, 4 outputs

Bipolar

8	DAC-08	Q	±1/2 LSB	150 ns	±4.5 to ±18	−55°C to +125°C	620	High-Speed Multiplying
		AQ	±1/4 LSB	135 ns				
		C	±1 LSB	150 ns		0°C to +70°C	620 648 D/751B	
		E	±1/2 LSB					
		H	±1/4 LSB	135 ns				
	MC1408	L6/P6	±2 LSB	300 ns Typ	+5.0, −5.0 to −15	0°C to +75°C	620 648	Multiplying
		L7/P7	±1 LSB					
		L8/P8	±1/2 LSB					
	MC1508	L8				−55°C to +125°C	620	
	MC10318	CL6	±2 LSB	10 ns Typ	−5.2	0°C to +70°C	620	ECL input Logic Levels Video Applications
		CL7	±1 LSB					
		L	±1/2 LSB				690	
		L9	±1/4 LSB					
4 x 3	MC10320	L		3 ns	+5.0, or ±5.0		733	125 MHz Color Graphics Triple DAC
	MC10320-1							90 MHz Color

A-D/D-A Converters

CMOS — For Telecommunications

Resolution (Bits)	Device	Monotonicity (Bits)	Conversion Time	Input Voltage Range	Supplies (V)	Temperature Range	Package	Comments
13	MC145402	13	31.25 μs	±3.28 V peak	±5.0 to 6.0	−40°C to +85°C	L/620	Digital signal processing (e.g., echo cancelling, high-speed modems, phone systems with conferencing)

6

DATA CONVERTERS

A-D Converters

Device	Function	Page
MC6108	8-Bit MPU Bus-Compatible High Speed A-to-D Converter	6-27
MC10319	High Speed 8-Bit D-to-A Flash Converter	6-62
MC10321	High Speed 7-Bit A-to-D Flash Converter	6-80

D-A Converters

Device	Function	Page
DAC-08	High Speed 8-Bit Multiplying D-to-A Converter	6-5
MC1408	8-Bit Multiplying D-to-A Converter	6-15
MC1508	8-Bit Multiplying D-to-A Converter	6-15
MC10318L, L9, CL6, CL7	High Speed 8-Bit D-to-A Converters	6-45
MC10320, 20-1	Triple 4-Bit Color Palette Video DAC	See Chapter 9

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RELATED APPLICATION NOTES

Application Note	Title	Related Device
EB-51	Successive Approximation BCD A-to-D Converter	**MC1408, MC1508**
AN963	Interfacing the MC6108 A-to-D to a Microprocessor — It's Easier Than You Think!	**MC6108**

MOTOROLA

DAC-08

Specifications and Applications Information

HIGH SPEED 8-BIT MULTIPLYING D-TO-A CONVERTER

SILICON MONOLITHIC INTEGRATED CIRCUIT

HIGH SPEED 8-BIT MULTIPLYING D-TO-A CONVERTER

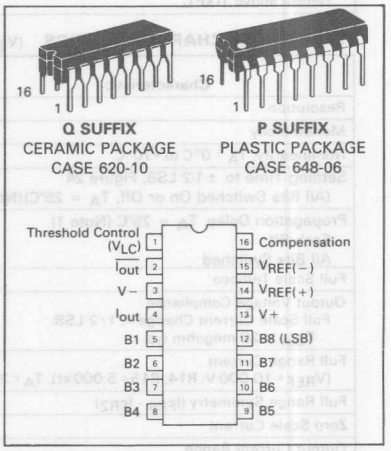
The DAC-08 series is a monolithic 8-bit high speed multiplying digital-to-analog converter, capable of settling to within 1/2 LSB (0.19%) in 85 ns. Monotonic multiplying performance is retained over a wide 40-to-1 reference current range. Full scale and reference currents are matched to within 1 LSB, therefore eliminating the need for full scale trim in most applications.

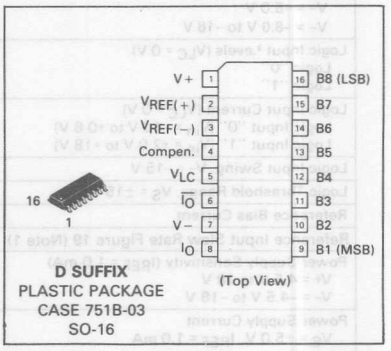
Dual complementry current outputs with high voltage compliance provide added versatility and allow differential mode of operation to effectively double the peak-to-peak output swing. In many applications, output current-to-voltage conversion can be accomplished without requiring an external op amp. Noise-immune inputs permit direct interface with TTL and DTL levels when the logic threshold control, V_{LC}, (Pin 1) is grounded. All other logic family thresholds are attainable by adjusting the voltage level of Pin 1. Performance characteristics are virtually unchanged over the entire ±4.5 V to ±18 V power supply range. Power consumption is typically 33 mW with ±5.0 V supplies.

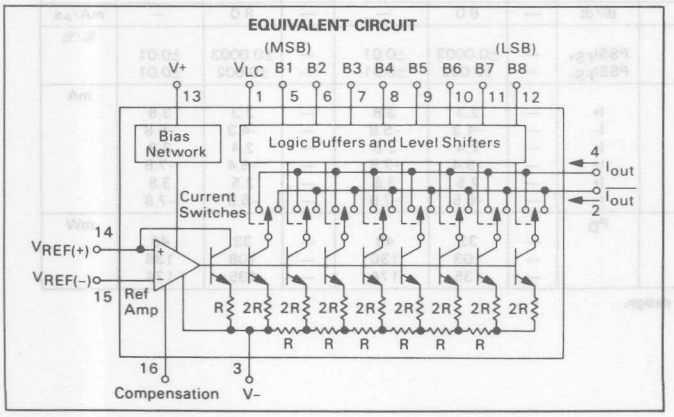
The DAC-08 is available in several versions, with nonlinearity as tight as ±0.1% (±1/4 LSB) over temperature. All versions are guaranteed monotonic over 8 bits. For an extra margin of performance, Motorola utilizes thin-film resistors permitting very accurate resistive values which are extremely stable over temperature.

High performance characteristics along with low cost, make the DAC-08 an excellent selection for applications such as CRT displays, waveform generation, high speed modems, and high speed analog-to-digital converters.

- Fast Settling Time — 85 ns
- Full Scale Current Prematched to ±1 LSB
- Nonlinearity Over Temperature to ±0.1% Max
- Differential Current Outputs
- High Voltage Compliance Outputs −10 V to +18 V
- Wide Range Multiplying Capability
- Inputs Compatable With TTL, DTL, CMOS, PMOS, ECL, HTL
- Low Full Scale Current Drift
- Wide Power Supply Range ±4.5 V to ±18 V
- Low Power Consumption
- Thin-Film Resistors
- Low Cost







Device	Nonlinearity	Temperature Range	Package
DAC-08AQ	±0.1%	−55°C to +125°C	Ceramic
DAC-08Q	±0.19%		Ceramic
DAC-08HQ	±0.1%		Ceramic
DAC-08EQ	±0.19%		Ceramic
DAC-08CQ	±0.39%		Ceramic
DAC-08CD	±0.39%	0°C to +70°C	SO-16
DAC-08ED	±0.19%		SO-16
DAC-08HP	±0.1%		Plastic
DAC-08EP	±0.19%		Plastic
DAC-08CP	±0.39%		Plastic

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MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
V+ Supply to V-Supply	—	36	V
Logic Inputs	—	V- to V- Plus 36	V
Logic Threshold Control	V_{LC}	V- to V+	V
Analog Current Outputs	I_{out}	See Figure 7	mA
Reference Inputs (V14, V15)	V_{REF}	V- to V+	V
Reference Input Differential Voltage (V14 to V15)	$V_{REF(D)}$	±18	V
Reference Input Current (I14)	I_{REF}	5.0	mA
Operating Temperature Range DAC-08AQ, Q DAC-08HQ, EQ, CQ, HP, EP, CP, ED, CD	T_A	 -55 to +125 0 to +70	°C
Storage Temperature	T_A	-65 to +150	°C
Power Dissipation Derate above 100°C	P_D $R_{\theta JA}$	500 10	mW mW/°C

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, I_{REF} = 2.0 mA, T_A = -55°C to +125°C, unless otherwise noted.)

Characteristic	Symbol	DAC-08A			DAC-08			Unit
		Min	Typ	Max	Min	Typ	Max	
Resolution	—	8	8	8	8	8	8	Bits
Monotonicity	—	8	8	8	8	8	8	Bits
Nonlinearity, T_A = 0°C to +70°C	NL	—	—	±0.1	—	—	±0.19	%FS
Settling Time to ±1/2 LSB, Figure 24 (All Bits Switched On or Off, T_A = 25°C)(Note 1)	t_s	—	85	—	—	85	—	ns
Propagation Delay, T_A = 25°C (Note 1) Each Bit All Bits Switched	 t_{PLH} t_{PHL}	 — —	 35 35	 — —	 — —	 35 35	 — —	ns
Full Scale Tempco	TCI_{FS}	—	±10	—	—	±10	—	ppm/°C
Output Voltage Compliance Full Scale Current Change < 1/2 LSB, R_{out} > 20 megohm typ	V_{OC}	-10	—	+18	-10	—	+18	V
Full Range Current (V_{REF} = 10.000 V; R14, R15 = 5.000 kΩ, T_A = 25°C)	I_{FR4}	1.984	1.992	2.000	1.94	1.99	2.04	mA
Full Range Symmetry (I_{FR4} - I_{FR2})	I_{FRS}	—	±0.5	±4.0	—	±1.0	±8.0	μA
Zero Scale Current	I_{ZS}	—	0.1	1.0	—	0.2	2.0	μA
Output Current Range V- = -5.0 V V- = -8.0 V to -18 V	 I_{OR1} I_{OR2}	 0 0	 — —	 2.1 4.2	 0 0	 — —	 2.1 4.2	mA
Logic Input Levels (V_{LC} = 0 V) Logic "0" Logic "1"	 V_{IL} V_{IH}	 — 2.0	 — —	 0.8 —	 — 2.0	 — —	 0.8 —	V
Logic Input Current (V_{LC} = 0 V) Logic Input "0" (V_{in} = -10 V to +0.8 V) Logic Input "1" (V_{in} = +2.0 V to +18 V)	 I_{IL} I_{IH}	 — —	 -2.0 0.002	 -10 10	 — —	 -2.0 0.002	 -10 10	μA
Logic Input Swing, V- = -15 V	V_{IS}	-10	—	+18	-10	—	+18	V
Logic Threshold Range, V_S = ±15 V	V_{THR}	-10	—	+13.5	-10	—	+13.5	V
Reference Bias Current	I_{15}	—	-1.0	-3.0	—	-1.0	-3.0	μA
Reference Input Slew Rate Figure 19 (Note 1)	di/dt	—	8.0	—	—	8.0	—	mA/μs
Power Supply Sensitivity (I_{REF} = 1.0 mA) V+ = 4.5 V to 18 V V- = -4.5 V to -18 V	 $PSSI_{FS+}$ $PSSI_{FS-}$	 — —	 ±0.0003 ±0.002	 ±0.01 ±0.01	 — —	 ±0.0003 ±0.002	 ±0.01 ±0.01	%/%
Power Supply Current V_S = ±5.0 V, I_{REF} = 1.0 mA V_S = +5.0 V, -15 V, I_{REF} = 2.0 mA V_S = ±15 V, I_{REF} = 2.0 mA	 I+ I- I+ I- I+ I-	 — — — — — —	 2.3 -4.3 2.4 -6.4 2.5 -6.5	 3.8 -5.8 3.8 -7.8 3.8 -7.8	 — — — — — —	 2.3 -4.3 2.4 -6.4 2.5 -6.5	 3.8 -5.8 3.8 -7.8 3.8 -7.8	mA
Power Dissipation V_S = ±5.0 V, I_{REF} = 1.0 mA V_S = +5.0 V, -15 V, I_{REF} = 2.0 mA V_S = ±15 V, I_{REF} = 2.0 mA	P_D	 — — —	 33 103 135	 48 136 174	 — — —	 33 108 135	 48 136 174	mW

Note 1. Parameter is not 100% tested; guaranteed by design.

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, I_{REF} = 2.0 mA, T_A = 0°C to 70°C, unless otherwise noted.)

Characteristic	Symbol	DAC-08H			DAC-08E			DAC-08C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Resolution	—	8	8	8	8	8	8	8	8	8	Bits
Monotonicity	—	8	8	8	8	8	8	8	8	8	Bits
Nonlinearity, T_A = 0°C to +70°C	NL	—	—	±0.1	—	—	±0.19	—	—	±0.39	%FS
Settling Time to ±1/2 LSB (All Bits Switched On or Off, (T_A = 25°C) Figure 24 (Note 1)	t_s	—	85	—	—	85	—	—	85	—	ns
Propagation Delay, T_A = 25°C (Note 1)											ns
Each Bit	t_{PLH}	—	35	—	—	35	—	—	35	—	
All Bits Switched	t_{PHL}	—	35	—	—	35	—	—	35	—	
Full Scale Tempco	TCI_{FS}	—	±10	—	—	±10	—	—	±10	—	ppm/°C
Output Voltage Compliance Full Scale Current Change < 1/2 LSB, R_{out} > 20 megohm typ.	V_{OC}	−10	—	+18	−10	—	+18	−10	—	+18	V
Full Range Current (V_{REF} = 10.000 V; R14, R15 = 5.000 kΩ) T_A = 25°C	I_{FR4}	1.984	1.992	2.000	1.94	1.99	2.04	1.94	1.99	2.04	mA
Full Range Symmetry (I_{FR4} - I_{FR2})	I_{FRS}	—	±0.5	±4.0	—	±1.0	±8.0	—	±2.0	±16.0	μA
Zero Scale Current	I_{ZS}	—	0.1	1.0	—	0.2	2.0	—	0.2	4.0	μA
Output Current Range											mA
V− = −5.0 V	I_{OR1}	0	—	2.1	0	—	2.1	0	—	2.1	
V− = −8.0 V to −18 V	I_{OR2}	0	—	4.2	0	—	4.2	0	—	4.2	
Logic Input Levels (V_{LC} = 0 V)											V
Logic "0"	V_{IL}	—	—	0.8	—	—	0.8	—	—	0.8	
Logic "1"	V_{IH}	2.0	—	—	2.0	—	—	2.0	—	—	
Logic Input Current (V_{LC} = 0 V)											μA
Logic Input "0" (V_{in} = −10 V to +0.8 V)	I_{IL}	—	−2.0	−10	—	−2.0	−10	—	−2.0	−10	
Logic Input "1" (V_{in} = +2.0 V to +18 V)	I_{IH}	—	0.002	10	—	0.002	10	—	0.002	10	
Logic Input Swing, V− = −15 V	V_{IS}	−10	—	+18	−10	—	+18	−10	—	+18	V
Logic Threshold Range, V_S = ±15 V	V_{THR}	−10	—	+13.5	−10	—	+13.5	−10	—	+13.5	V
Reference Bias Current	I_{15}	—	−1.0	−3.0	—	−1.0	−3.0	—	−1.0	−3.0	μA
Reference Input Slew Rate Figure 19 (Note 1)	dI/dt	—	8.0	—	—	8.0	—	—	8.0	—	mA/μs
Power Supply Sensitivity (I_{REF} = 1.0 mA)											%/%
V+ = 4.5 V to 18 V	$PSSI_{FS+}$	—	±0.0003	±0.01	—	±0.0003	±0.01	—	±0.0003	±0.01	
V− = −4.5 V to −18 V	$PSSI_{FS-}$	—	±0.002	±0.01	—	±0.002	±0.01	—	±0.002	±0.01	
Power Supply Current	I+	—	2.3	3.8	—	2.3	3.8	—	2.3	3.8	mA
V_S = ±5.0 V, I_{REF} = 1.0 mA	I−	—	−4.3	−5.8	—	−4.3	−25.8	—	−4.3	−5.8	
	I+	—	2.4	3.8	—	2.4	3.8	—	2.4	3.8	
V_S = +5.0 V, −15 V, I_{REF} = 2.0 mA	I−	—	−6.4	−7.8	—	−6.4	−7.8	—	−6.4	−7.8	
	I+	—	2.5	3.8	—	2.5	3.8	—	2.5	3.8	
V_S = ±15 V, I_{REF} = 2.0 mA	I−	—	−6.5	−7.8	—	−6.5	−7.8	—	−6.5	−7.8	
Power Dissipation	P_D										mW
V_S = ±5.0 V, I_{REF} = 1.0 mA		—	33	48	—	33	48	—	33	48	
V_S = +5.0 V, −15 V, I_{REF} = 2.0 mA		—	108	136	—	108	136	—	108	136	
V_S = ±15 V, I_{REF} = 2.0 mA		—	135	174	—	135	174	—	135	174	

Note 1. Parameter is not 100% tested; guaranteed by design.

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TYPICAL PERFORMANCE CURVES

FIGURE 1 — FULL SCALE CURRENT versus REFERENCE CURRENT

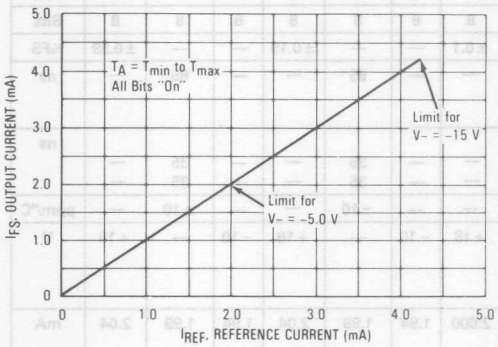
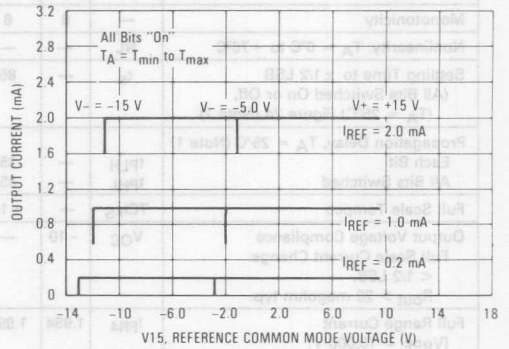
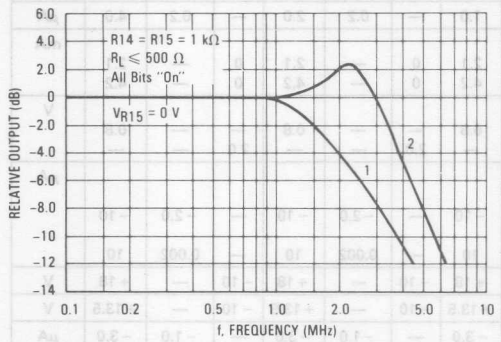


FIGURE 2 — REFERENCE AMP COMMON MODE RANGE



NOTE: Positive Common Mode Range is Always (V+) –1.5 V

FIGURE 3 — REFERENCE INPUT FREQUENCY RESPONSE



Curve 1 — C_C = 15 pF, V_{in} = 2.0 V p-p Centered at +1.0 V (Large-Signal)
Curve 2 — C_C = 15 pF, V_{in} = 50 mV p-p Centered at +200 mV (Small-Signal)

FIGURE 4 — LSB PROPAGATION DELAY versus I_{FS}

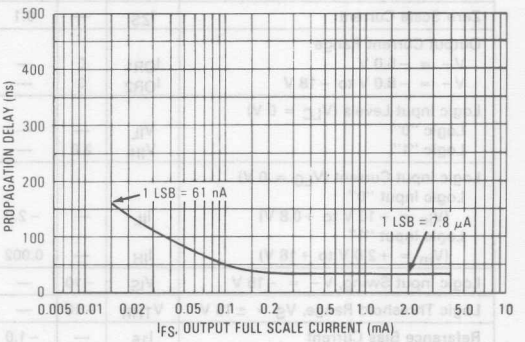


FIGURE 5 — LOGIC INPUT CURRENT versus INPUT VOLTAGE

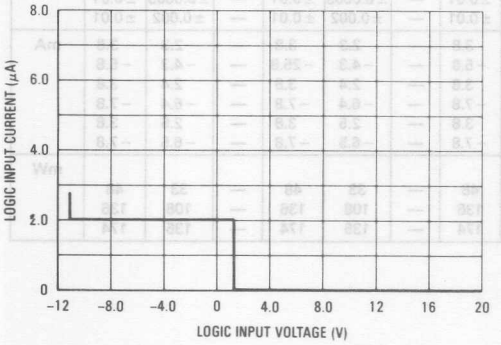
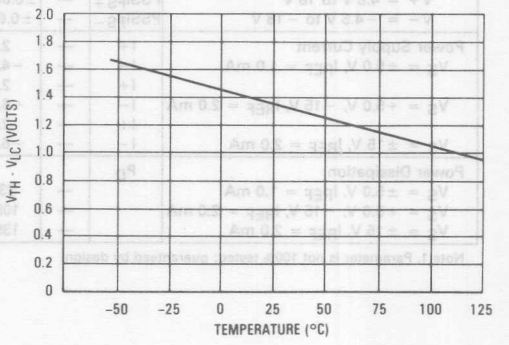


FIGURE 6 — V_{TH} - V_{LC} versus TEMPERATURE



TYPICAL PERFORMANCE CURVES

FIGURE 7 — OUTPUT CURRENT versus OUTPUT VOLTAGE (Output Voltage Compliance)

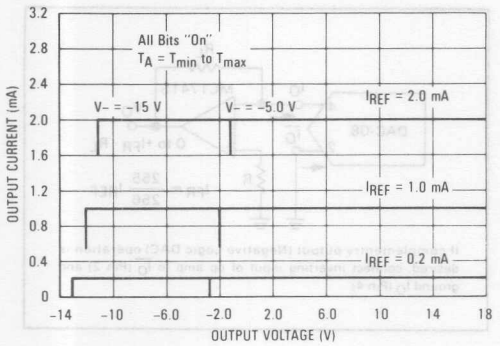


FIGURE 8 — OUTPUT VOLTAGE COMPLIANCE versus TEMPERATURE

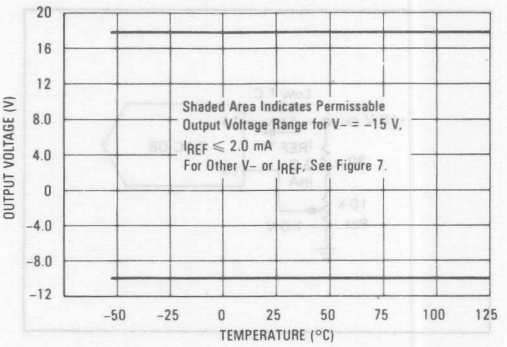
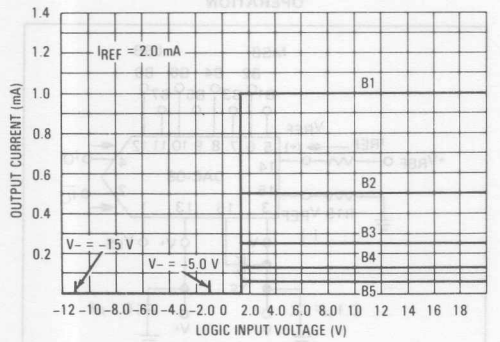


FIGURE 9 — BIT TRANSFER CHARACTERISTICS



NOTE: B1–B8 have identical transfer characteristics. Bits are fully switched with less than 1/2 LSB error, at less than ±100 mV from actual threshold. These switching points are guaranteed to lie between 0.8 V and 2.0 V over operating temperature range (V_{LC} = 0 V).

FIGURE 10 — POWER SUPPLY CURRENT versus V+

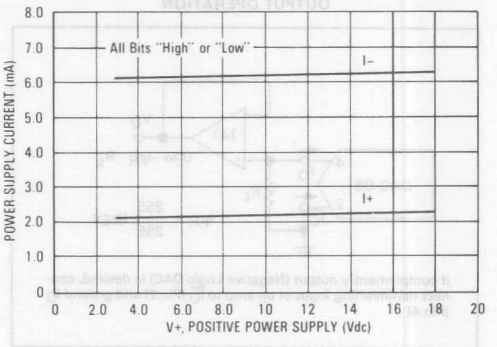


FIGURE 11 — POWER SUPPLY CURRENT versus V–

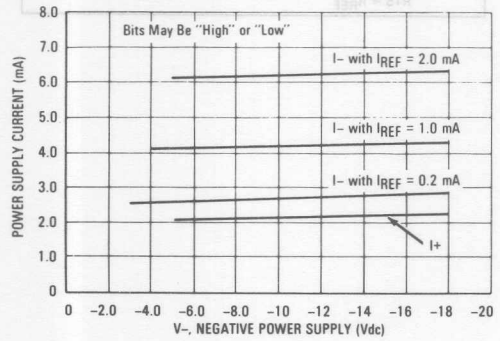


FIGURE 12 — POWER SUPPLY CURRENT versus TEMPERATURE

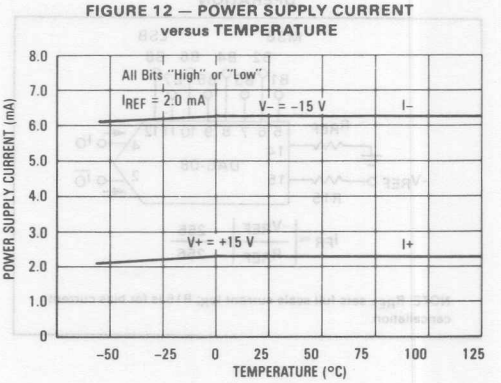


FIGURE 13 — RECOMMENDED FULL SCALE ADJUSTMENT CIRCUIT

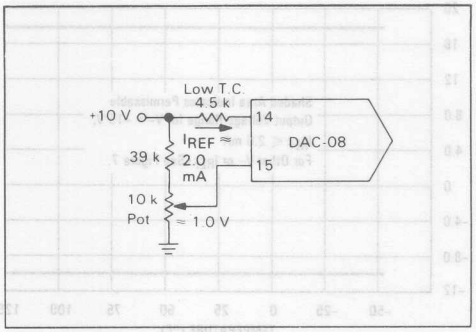
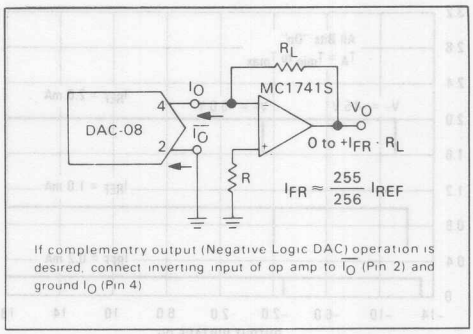


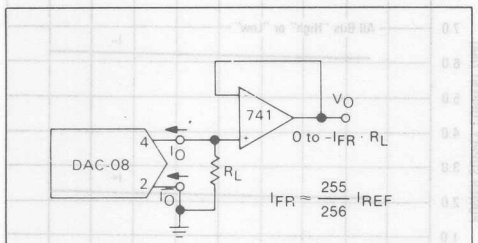
FIGURE 14 — POSITIVE LOW IMPEDANCE OUTPUT OPERATION



If complementry output (Negative Logic DAC) operation is desired, connect inverting input of op amp to $\overline{I_O}$ (Pin 2) and ground I_O (Pin 4)

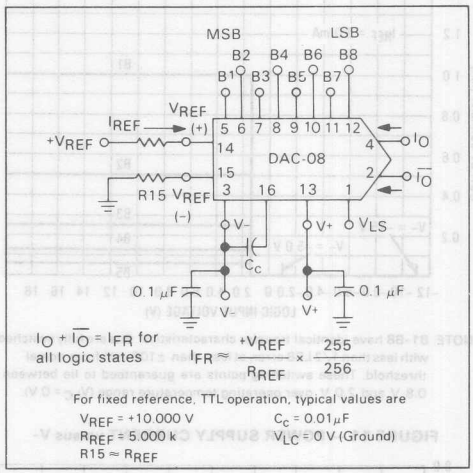
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FIGURE 15 — NEGATIVE LOW IMPEDANCE OUTPUT OPERATION



If complementry output (Negative Logic DAC) is desired, connect noninverting input of op amp to $\overline{I_O}$ (Pin 2) and ground I_O (Pin 4)

FIGURE 16 — BASIC POSITIVE REFERENCE OPERATION



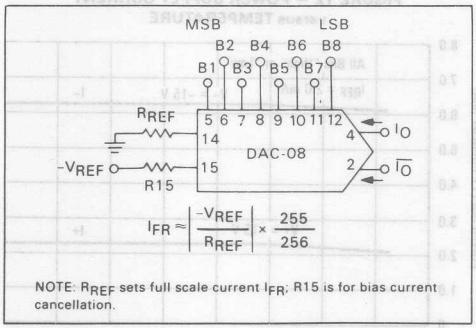
$I_O + \overline{I_O} = I_{FR}$ for all logic states

$$I_{FR} \approx \frac{+V_{REF}}{R_{REF}} \times \frac{255}{256}$$

For fixed reference, TTL operation, typical values are

$V_{REF} = +10.000$ V $C_C = 0.01\mu F$
$R_{REF} = 5.000$ k $V_{LC} = 0$ V (Ground)
$R15 \approx R_{REF}$

FIGURE 17 — BASIC NEGATIVE REFERENCE OPERATION



NOTE: R_{REF} sets full scale current I_{FR}; R15 is for bias current cancellation.

BASIC CIRCUIT CONFIGURATIONS

FIGURE 18 — ACCOMMODATING BIPOLAR REFERENCES

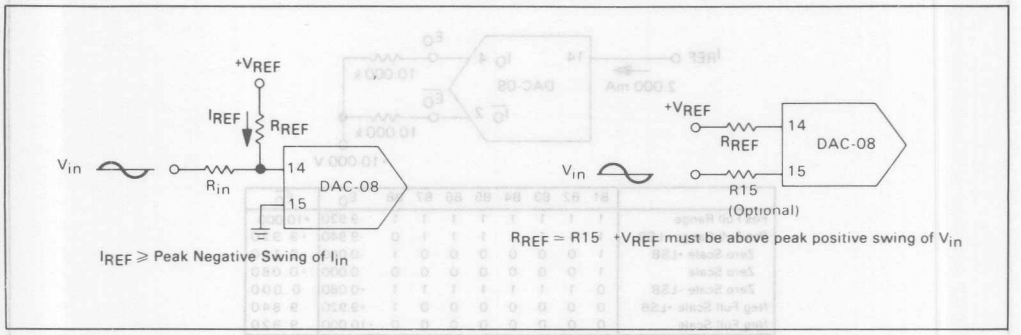


FIGURE 19 — PULSED REFERENCE OPERATION

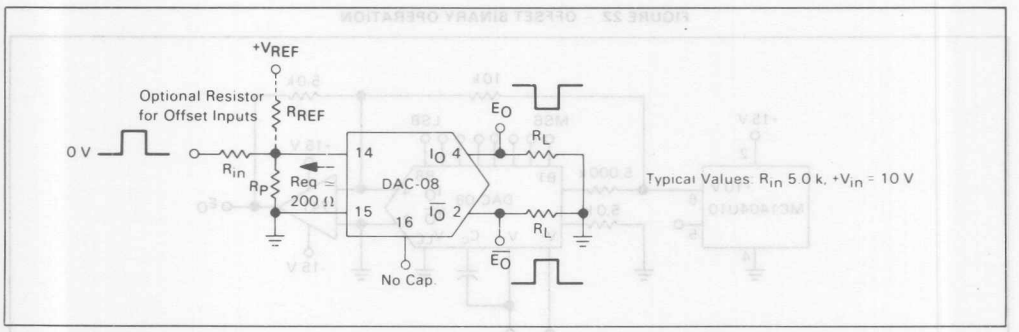
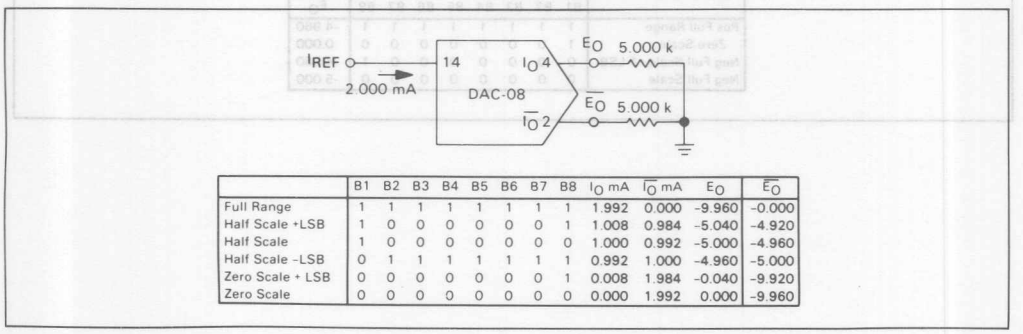


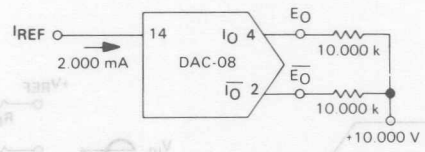
FIGURE 20 — BASIC UNIPOLAR NEGATIVE OPERATION



	B1	B2	B3	B4	B5	B6	B7	B8	I_O mA	$\overline{I_O}$ mA	E_O	$\overline{E_O}$
Full Range	1	1	1	1	1	1	1	1	1.992	0.000	-9.960	-0.000
Half Scale +LSB	1	0	0	0	0	0	0	1	1.008	0.984	-5.040	-4.920
Half Scale	1	0	0	0	0	0	0	0	1.000	0.992	-5.000	-4.960
Half Scale -LSB	0	1	1	1	1	1	1	1	0.992	1.000	-4.960	-5.000
Zero Scale + LSB	0	0	0	0	0	0	0	1	0.008	1.984	-0.040	-9.920
Zero Scale	0	0	0	0	0	0	0	0	0.000	1.992	0.000	-9.960

BASIC CIRCUIT CONFIGURATIONS

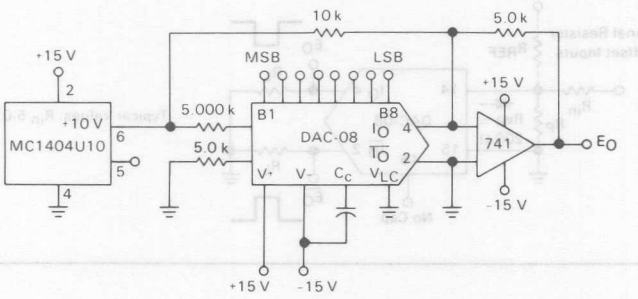
FIGURE 21 – BASIC BIPOLAR OUTPUT OPERATION



	B1	B2	B3	B4	B5	B6	B7	B8	E_O	$\overline{E_O}$
Pos Full Range	1	1	1	1	1	1	1	1	+9.920	+10.000
Pos Full Range -LSB	1	1	1	1	1	1	1	0	+9.840	+9.920
Zero Scale +LSB	1	0	0	0	0	0	0	1	+0.080	+0.160
Zero Scale	1	0	0	0	0	0	0	0	0.000	+0.080
Zero Scale -LSB	0	1	1	1	1	1	1	1	+0.080	0.000
Neg Full Scale +LSB	0	0	0	0	0	0	0	1	+9.920	-9.840
Neg Full Scale	0	0	0	0	0	0	0	0	-10.000	9.920

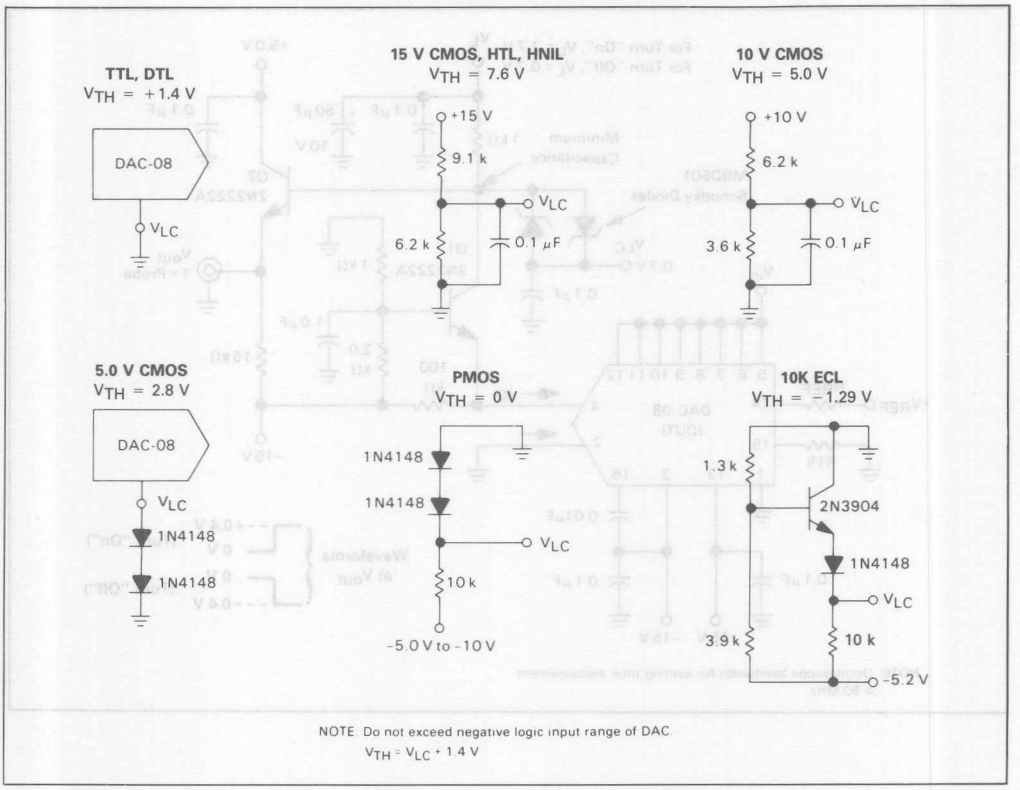
6

FIGURE 22 – OFFSET BINARY OPERATION



	B1	B2	B3	B4	B5	B6	B7	B8	E_O
Pos Full Range	1	1	1	1	1	1	1	1	-4.960
Zero Scale	1	0	0	0	0	0	0	0	0.000
Neg Full Scale +1 LSB	0	0	0	0	0	0	0	1	-4.960
Neg Full Scale	0	0	0	0	0	0	0	0	-5.000

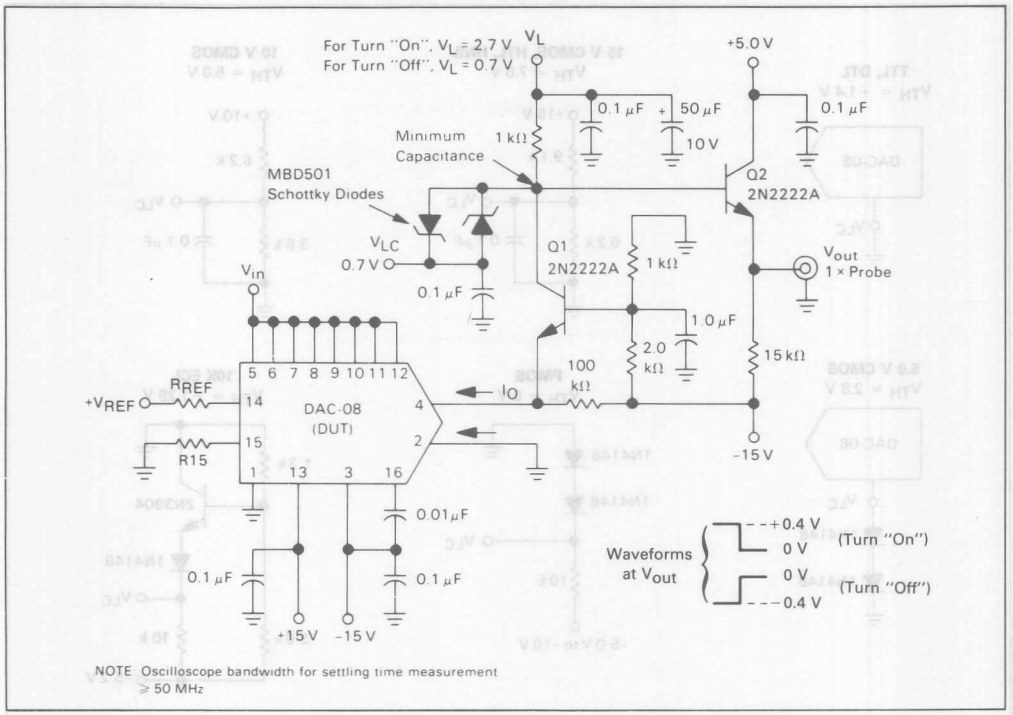
FIGURE 23 — INTERFACING WITH VARIOUS LOGIC FAMILIES



NOTE: Do not exceed negative logic input range of DAC.
$V_{TH} = V_{LC} + 1.4\ V$

6

FIGURE 24 — SETTLING TIME MEASUREMENT CIRCUIT



NOTE Oscilloscope bandwidth for settling time measurement ≥ 50 MHz

6

MOTOROLA

MC1408
MC1508

Specifications and Applications Information

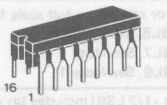
EIGHT-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

SILICON MONOLITHIC INTEGRATED CIRCUIT

EIGHT-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

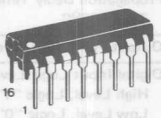
. . . designed for use where the output current is a linear product of an eight-bit digital word and an analog input voltage.

- Eight-Bit Accuracy Available in Both Temperature Ranges
  Relative Accuracy: ±0.19% Error maximum
  (MC1408L8, MC1408P8, MC1508L8)
- Seven and Six-Bit Accuracy Available with MC1408 Designated by 7 or 6 Suffix after Package Suffix
- Fast Settling Time — 300 ns typical
- Noninverting Digital Inputs are MTTL and CMOS Compatible
- Output Voltage Swing — +0.4 V to -5.0 V
- High-Speed Multiplying Input
  Slew Rate 4.0 mA/μs
- Standard Supply Voltages: +5.0 V and -5.0 V to -15 V



L SUFFIX
CERAMIC PACKAGE
CASE 620-10

P SUFFIX
PLASTIC PACKAGE
CASE 648-06



6

FIGURE 1 — D-to-A TRANSFER CHARACTERISTICS

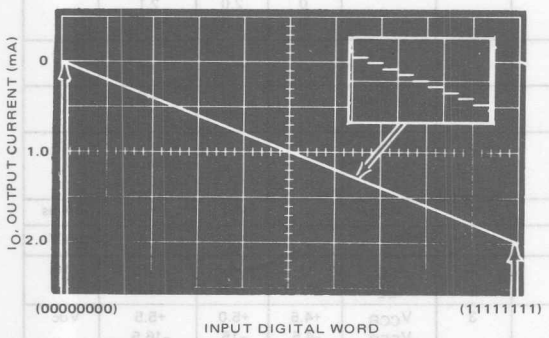
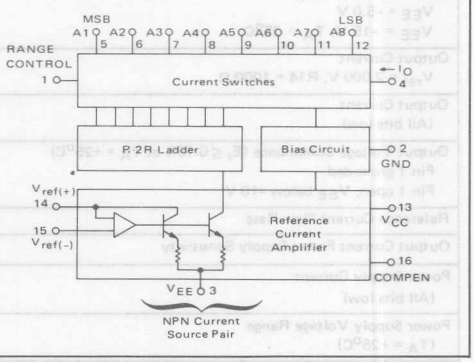


FIGURE 2 — BLOCK DIAGRAM



TYPICAL APPLICATIONS

- Tracking A-to-D Converters
- Successive Approximation A-to-D Converters
- 2 1/2 Digit Panel Meters and DVM's
- Waveform Synthesis
- Sample and Hold
- Peak Detector
- Programmable Gain and Attenuation
- CRT Character Generation
- Audio Digitizing and Decoding
- Programmable Power Supplies
- Analog-Digital Multiplication
- Digital-Digital Multiplication
- Analog-Digital Division
- Digital Addition and Subtraction
- Speech Compression and Expansion
- Stepping Motor Drive

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+5.5 -16.5	Vdc
Digital Input Voltage	V_5 thru V_{12}	0 to +5.5	Vdc
Applied Output Voltage	V_O	+0.5,-5.2	Vdc
Reference Current	I_{14}	5.0	mA
Reference Amplifier Inputs	V_{14},V_{15}	V_{CC},V_{EE}	Vdc
Operating Temperature Range MC1508 MC1408 Series	T_A	 -55 to +125 0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

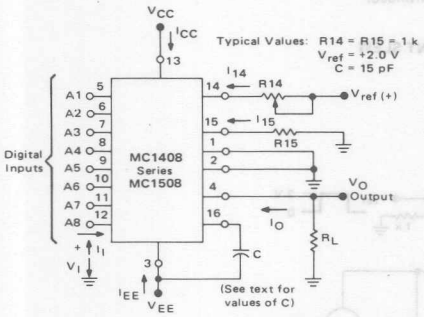
ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = -15 Vdc, $\frac{Vref}{R14}$ = 2.0 mA, MC1508L8: T_A = -55°C to +125°C, MC1408L Series: T_A = 0 to +75°C unless otherwise noted. All digital inputs at high logic level.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Relative Accuracy (Error relative to full scale I_O) MC1508L8, MC1408L8, MC1408P8 MC1408P7, MC1408L7, See Note 1 MC1408P6, MC1408L6, See Note 1	4	E_r	 – – –	 – – –	 ±0.19 ±0.39 ±0.78	%
Settling Time to within ±1/2 LSB [includes t_{PLH}] (T_A=+25°C) See Note 2	5	t_S	–	300	–	ns
Propagation Delay Time T_A = +25°C	5	t_{PLH},t_{PHL}	–	30	100	ns
Output Full Scale Current Drift		TCI_O	–	±20	–	PPM/°C
Digital Input Logic Levels (MSB) High Level, Logic "1" Low Level, Logic "0"	3	 V_{IH} V_{IL}	 2.0 –	 – –	 – 0.8	Vdc
Digital Input Current (MSB) High Level, V_{IH} = 5.0 V Low Level, V_{IL} = 0.8 V	3	 I_{IH} I_{IL}	 – –	 0 -0.4	 0.04 -0.8	mA
Reference Input Bias Current (Pin 15)	3	I_{15}	–	-1.0	-5.0	μA
Output Current Range V_{EE} = -5.0 V V_{EE} = -15 V, T_A = 25°C	3	I_{OR}	 0 0	 2.0 2.0	 2.1 4.2	mA
Output Current V_{ref} = 2.000 V, R14 = 1000 Ω	3	I_O	 1.9	 1.99	 2.1	mA
Output Current (All bits low)	3	$I_{O(min)}$	–	0	4.0	μA
Output Voltage Compliance ($E_r \leq 0.19\%$ at T_A = +25°C) Pin 1 grounded Pin 1 open, V_{EE} below -10 V	3	V_O	 – –	 – –	 -0.55, +0.4 -5.0, +0.4	Vdc
Reference Current Slew Rate	6	SR I_{ref}	–	4.0	–	mA/μs
Output Current Power Supply Sensitivity		PSRR(–)	–	0.5	2.7	μA/V
Power Supply Current (All bits low)	3	I_{CC} I_{EE}	– –	+13.5 -7.5	+22 -13	mA
Power Supply Voltage Range (T_A = +25°C)	3	V_{CCR} V_{EER}	+4.5 -4.5	+5.0 -15	+5.5 -16.5	Vdc
Power Dissipation All bits low V_{EE} = -5.0 Vdc V_{EE} = -15 Vdc All bits high V_{EE} = -5.0 Vdc V_{EE} = -15 Vdc	3	P_D	 – – – –	 105 190 90 160	 170 305 – –	mW

Note 1. All current switches are tested to guarantee at least 50% of rated output current.
Note 2. All bits switched.

TEST CIRCUITS

FIGURE 3 – NOTATION DEFINITIONS TEST CIRCUIT



V_I and I_I apply to inputs A1 thru A8

The resistor tied to pin 15 is to temperature compensate the bias current and may not be necessary for all applications.

$$I_O = K\left\{\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right\}$$

where $K \cong \frac{V_{ref}}{R14}$

and A_N = "1" if A_N is at high level
A_N = "0" if A_N is at low level

FIGURE 4 – RELATIVE ACCURACY TEST CIRCUIT

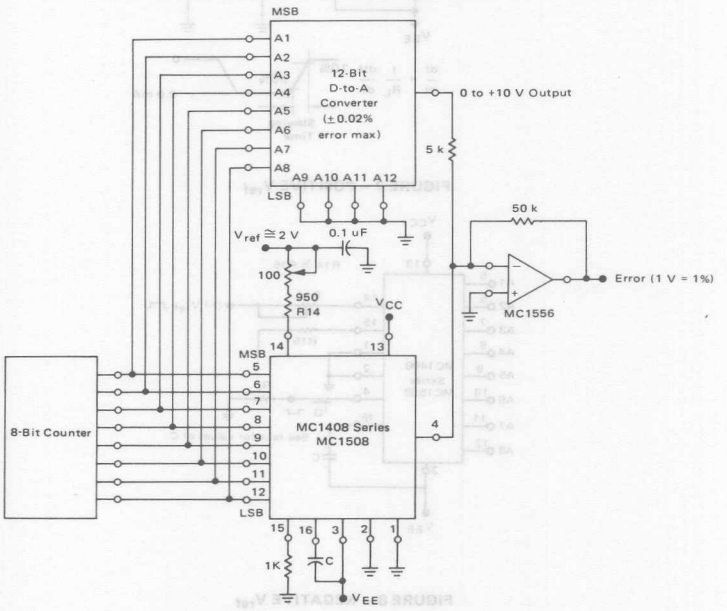
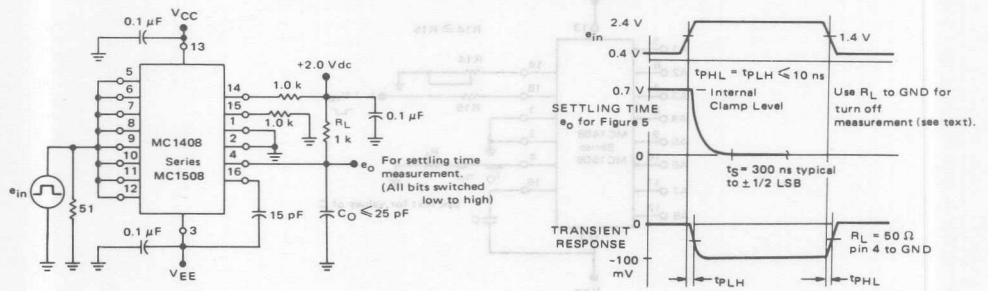
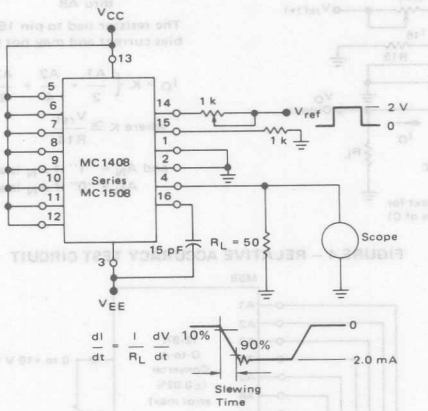


FIGURE 5 – TRANSIENT RESPONSE and SETTLING TIME



TEST CIRCUITS (continued)

FIGURE 6 – REFERENCE CURRENT SLEW RATE MEASUREMENT



6

FIGURE 7 – POSITIVE V_{ref}

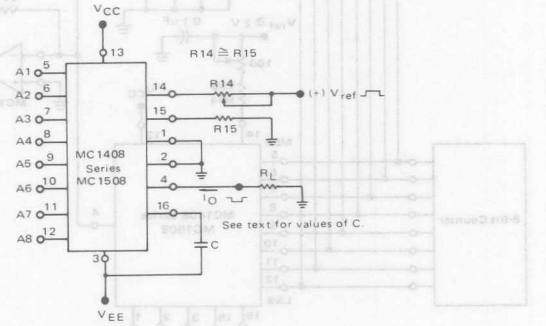


FIGURE 8 – NEGATIVE V_{ref}

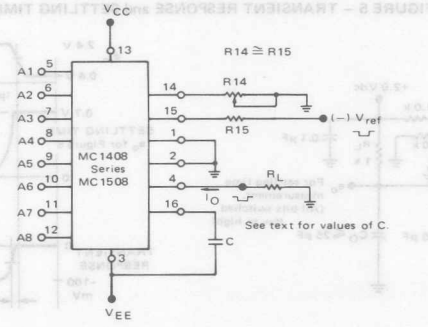
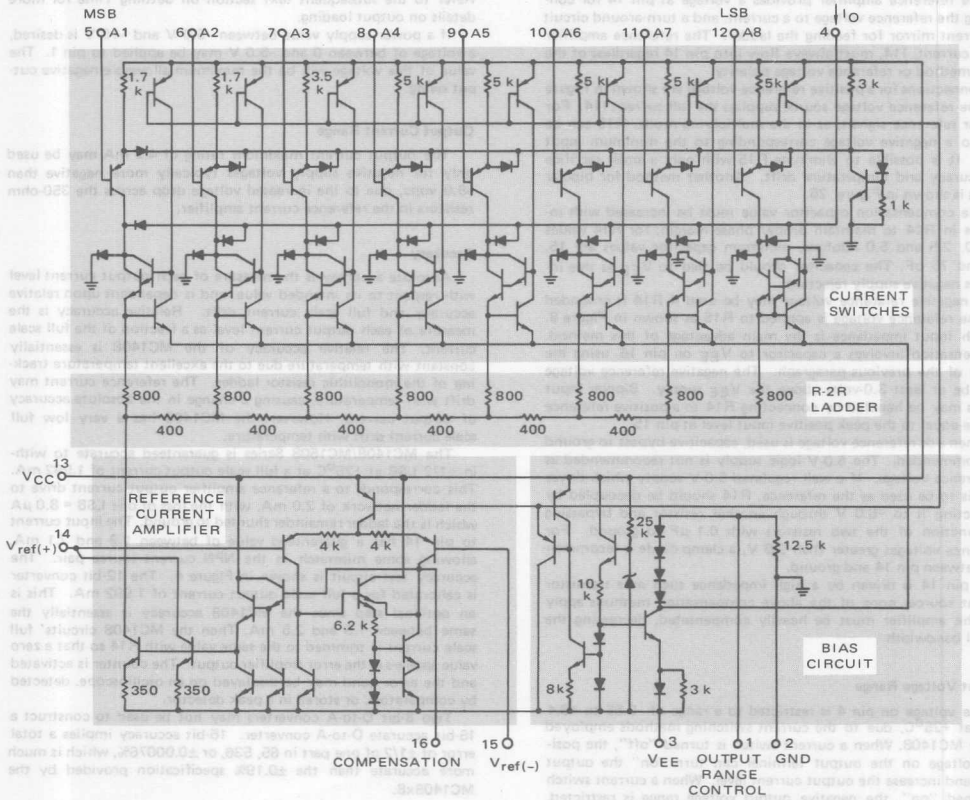


FIGURE 9 – MC1408, MC1508 SERIES EQUIVALENT CIRCUIT SCHEMATIC



CIRCUIT DESCRIPTION

The MC1408 consists of a reference current amplifier, an R-2R ladder, and eight high-speed current switches. For many applications, only a reference resistor and reference voltage need be added.

The switches are noninverting in operation, therefore a high state on the input turns on the specified output current component. The switch uses current steering for high speed, and a termination amplifier consisting of an active load gain stage with unity gain feedback. The termination amplifier holds the parasitic capacitance of the ladder at a constant voltage during switching, and provides a low impedance termination of equal voltage for all legs of the ladder.

The R-2R ladder divides the reference amplifier current into binarily-related components, which are fed to the switches. Note that there is always a remainder current which is equal to the least significant bit. This current is shunted to ground, and the maximum output current is 255/256 of the reference amplifier current, or 1.992 mA for a 2.0 mA reference amplifier current if the NPN current source pair is perfectly matched.

GENERAL INFORMATION

Reference Amplifier Drive and Compensation

The reference amplifier provides a voltage at pin 14 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input current, I14, must always flow into pin 14 regardless of the setup method or reference voltage polarity.

Connections for a positive reference voltage are shown in Figure 7. The reference voltage source supplies the full current I14. For bipolar reference signals, as in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R15 with only a small sacrifice in accuracy and temperature drift. Another method for bipolar inputs is shown in Figure 25.

The compensation capacitor value must be increased with increases in R14 to maintain proper phase margin; for R14 values of 1.0, 2.5 and 5.0 kilohms, minimum capacitor values are 15, 37, and 75 pF. The capacitor should be tied to V_{EE} as this increases negative supply rejection.

A negative reference voltage may be used if R14 is grounded and the reference voltage is applied to R15 as shown in Figure 8. A high input impedance is the main advantage of this method. Compensation involves a capacitor to V_{EE} on pin 16, using the values of the previous paragraph. The negative reference voltage must be at least 3.0-volts above the V_{EE} supply. Bipolar input signals may be handled by connecting R14 to a positive reference voltage equal to the peak positive input level at pin 15.

When a dc reference voltage is used, capacitive bypass to ground is recommended. The 5.0-V logic supply is not recommended as a reference voltage. If a well regulated 5.0-V supply which drives logic is to be used as the reference, R14 should be decoupled by connecting it to +5.0 V through another resistor and bypassing the junction of the two resistors with 0.1 μF to ground. For reference voltages greater than 5.0 V, a clamp diode is recommended between pin 14 and ground.

If pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

Output Voltage Range

The voltage on pin 4 is restricted to a range of -0.55 to +0.4 volts at +25°C, due to the current switching methods employed in the MC1408. When a current switch is turned "off", the positive voltage on the output terminal can turn "on" the output diode and increase the output current level. When a current switch is turned "on", the negative output voltage range is restricted. The base of the termination circuit Darlington transistor is one diode voltage below ground when pin 1 is grounded, so a negative voltage below the specified safe level will drive the low current device of the Darlington into saturation, decreasing the output current level.

The negative output voltage compliance of the MC1408 may be extended to -5.0 V volts by opening the circuit at pin 1. The negative supply voltage must be more negative than -10 volts. Using a full scale current of 1.992 mA and load resistor of 2.5 kilohms between pin 4 and ground will yield a voltage output of 256 levels between 0 and -4.980 volts. Floating pin 1 does not affect the converter speed or power dissipation. However, the value of the load resistor determines the switching time due to increased voltage swing. Values of R_L up to 500 ohms do not significantly affect performance, but a 2.5-kilohm load increases "worst case" settling time to 1.2 μs (when all bits are switched on). Refer to the subsequent text section on Settling Time for more details on output loading.

If a power supply value between -5.0 V and -10 V is desired, a voltage of between 0 and -5.0 V may be applied to pin 1. The value of this voltage will be the maximum allowable negative output swing.

Output Current Range

The output current maximum rating of 4.2 mA may be used only for negative supply voltages typically more negative than -8.0 volts, due to the increased voltage drop across the 350-ohm resistors in the reference current amplifier.

Accuracy

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full scale current. The relative accuracy of the MC1408 is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the MC1408 has a very low full scale current drift with temperature.

The MC1408/MC1508 Series is guaranteed accurate to within ±1/2 LSB at +25°C at a full scale output current of 1.992 mA. This corresponds to a reference amplifier output current drive to the ladder network of 2.0 mA, with the loss of one LSB = 8.0 μA which is the ladder remainder shunted to ground. The input current to pin 14 has a guaranteed value of between 1.9 and 2.1 mA, allowing some mismatch in the NPN current source pair. The accuracy test circuit is shown in Figure 4. The 12-bit converter is calibrated for a full scale output current of 1.992 mA. This is an optional step since the MC1408 accuracy is essentially the same between 1.5 and 2.5 mA. Then the MC1408 circuits' full scale current is trimmed to the same value with R14 so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accurate D-to-A converter. 16-bit accuracy implies a total error of ±1/2 of one part in 65, 536, or ±0.00076%, which is much more accurate than the ±0.19% specification provided by the MC1408x8.

Multiplying Accuracy

The MC1408 may be used in the multiplying mode with eight-bit accuracy when the reference current is varied over a range of 256:1. The major source of error is the bias current of the termination amplifier. Under "worst case" conditions, these eight amplifiers can contribute a total of 1.6 μA extra current at the output terminal. If the reference current in the multiplying mode ranges from 16 μA to 4.0 mA, the 1.6 μA contributes an error of 0.1 LSB. This is well within eight-bit accuracy referenced to 4.0 mA.

A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the MC1408 is monotonic for all values of reference current above 0.5 mA. The recommended range for operation with a dc reference current is 0.5 to 4.0 mA.

GENERAL INFORMATION (Continued)

Settling Time

The "worst case" switching condition occurs when all bits are switched "on", which corresponds to a low-to-high transition for all bits. This time is typically 300 ns for settling to within ±1/2 LSB, for 8-bit accuracy, and 200 ns to 1/2 LSB for 7 and 6-bit accuracy. The turn off is typically under 100 ns. These times apply when $R_L \leq 500$ ohms and $C_O \leq 25$ pF.

The slowest single switch is the least significant bit, which turns "on" and settles in 250 ns and turns "off" in 80 ns. In applications where the D-to-A converter functions in a positive-going ramp mode, the "worst case" switching condition does not occur, and a settling time of less than 300 ns may be realized. Bit A7 turns "on" in 200 ns and "off" in 80 ns, while bit A6 turns "on" in 150 ns and "off" in 80 ns.

The test circuit of Figure 5 requires a smaller voltage swing for the current switches due to internal voltage clamping in the MC-1408. A 1.0-kilohm load resistor from pin 4 to ground gives a typical settling time of 400 ns. Thus, it is voltage swing and not the output RC time constant that determines settling time for most applications.

Extra care must be taken in board layout since this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100 μF supply bypassing for low frequencies, and minimum scope lead length are all mandatory.

TYPICAL CHARACTERISTICS

(V_{CC} = +5.0 V, V_{EE} = -15 V, T_A = +25°C unless otherwise noted.)

6

FIGURE 10 – LOGIC INPUT CURRENT versus INPUT VOLTAGE

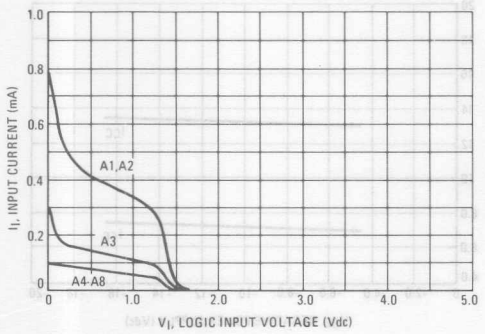


FIGURE 11 – TRANSFER CHARACTERISTIC versus TEMPERATURE
(A5 thru A8 thresholds lie within range for A1 thru A4)

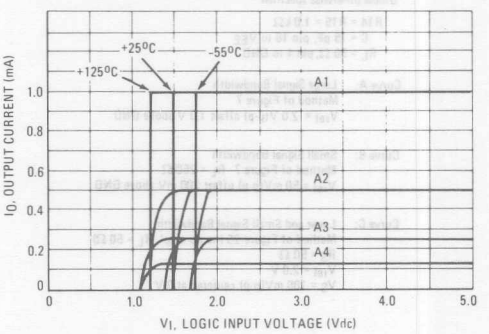


FIGURE 12 – OUTPUT CURRENT versus OUTPUT VOLTAGE
(See text for pin 1 restrictions)

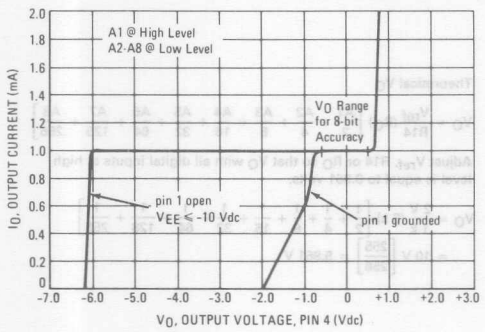
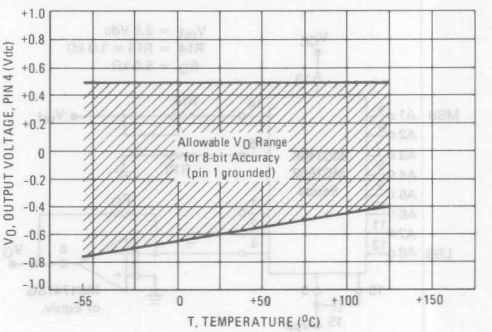


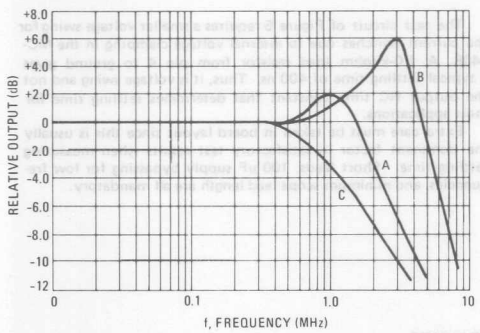
FIGURE 13 – OUTPUT VOLTAGE versus TEMPERATURE
(Negative range with pin 1 open is -5.0 Vdc over full temperature range)



TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +5.0 V, V_{EE} = -15 V, T_A = +25°C unless otherwise noted.)

FIGURE 14 – REFERENCE INPUT FREQUENCY RESPONSE



Unless otherwise specified:

R14 = R15 = 1.0 kΩ
C = 15 pF, pin 16 to V_{EE}
R_L = 50 Ω, pin 4 to GND

Curve A: Large Signal Bandwidth
Method of Figure 7
V_{ref} = 2.0 V(p-p) offset 1.0 V above GND

Curve B: Small Signal Bandwidth
Method of Figure 7 R_L = 250 Ω
V_{ref} = 50 mV(p-p) offset 200 mV above GND

Curve C: Large and Small Signal Bandwidth
Method of Figure 25 (no op-ampl, R_L = 50 Ω)
R_S = 50 Ω
V_{ref} = 2.0 V
V_S = 100 mV(p-p) centered at 0 V

FIGURE 15 – TYPICAL POWER SUPPLY CURRENT versus TEMPERATURE (all bits low)

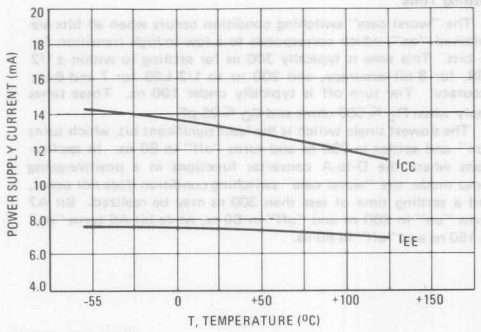
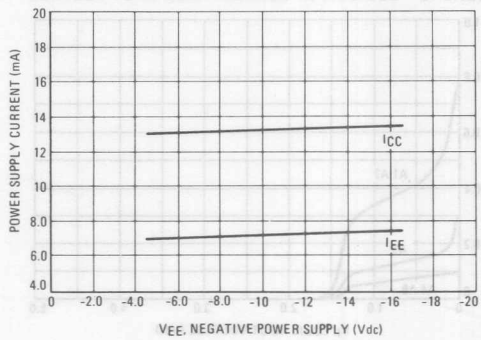
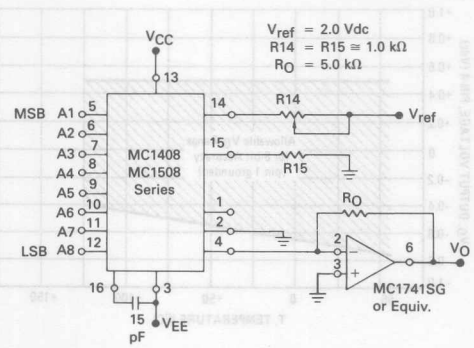


FIGURE 16 – TYPICAL POWER SUPPLY CURRENT versus V_{EE} (all bits low)



APPLICATIONS INFORMATION

FIGURE 17 – OUTPUT CURRENT TO VOLTAGE CONVERSION



Theoretical V_O

$$V_O = \frac{V_{ref}}{R14}(R_O)\left[\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right]$$

Adjust V_{ref}, R14 or R_O so that V_O with all digital inputs at high level is equal to 9.961 volts.

$$V_O = \frac{2\ V}{1\ k}(5\ k)\left[\frac{1}{2}+\frac{1}{4}+\frac{1}{8}+\frac{1}{16}+\frac{1}{32}+\frac{1}{64}+\frac{1}{128}+\frac{1}{256}\right]$$

$$= 10\ V\left[\frac{255}{256}\right] = 9.961\ V$$

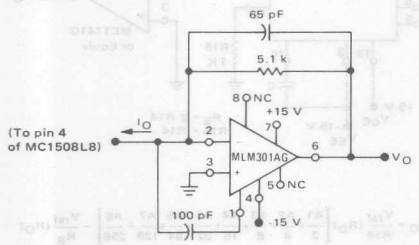
APPLICATIONS INFORMATION (continued)

Voltage outputs of a larger magnitude are obtainable with this circuit which uses an external operational amplifier as a current to voltage converter. This configuration automatically keeps the output of the MC1408 at ground potential and the operational amplifier can generate a positive voltage limited only by its positive supply voltage. Frequency response and settling time are primarily determined by the characteristics of the operational amplifier. In addition, the operational amplifier must be compensated for unity gain, and in some cases overcompensation may be desirable.

Note that this configuration results in a positive output voltage only, the magnitude of which is dependent on the digital input.

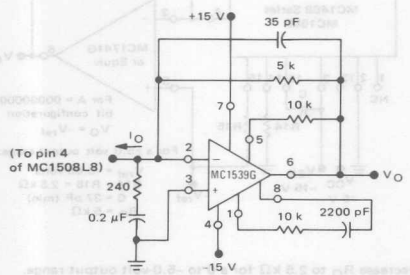
The following circuit shows how the MLM301AG can be used in a feedforward mode resulting in a full scale settling time on the order of 2.0 μs.

FIGURE 18



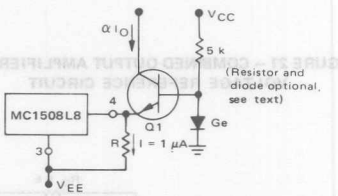
An alternative method is to use the MC1539G and input compensation. Response of this circuit is also on the order of 2.0 μs. See Motorola Application Note AN-459 for more details on this concept.

FIGURE 19



The positive voltage range may be extended by cascading the output with a high beta common base transistor, Q1, as shown.

FIGURE 20 – EXTENDING POSITIVE VOLTAGE RANGE



The output voltage range for this circuit is 0 volts to BV_{CBO} of the transistor. If pin 1 is left open, the transistor base may be grounded, eliminating both the resistor and the diode. Variations in beta must be considered for wide temperature range applications. An inverted output waveform may be obtained by using a load resistor from a positive reference voltage to the collector of the transistor. Also, high-speed operation is possible with a large output voltage swing, because pin 4 is held at a constant voltage. The resistor (R) to V_{EE} maintains the transistor emitter voltage when all bits are "off" and insures fast turn-on of the least significant bit.

Combined Output Amplifier and Voltage Reference

For many of its applications the MC1408 requires a reference voltage and an operational amplifier. Normally the operational amplifier is used as a current to voltage converter and its output need only go positive. With the popular MC1723G voltage regulator both of these functions are provided in a single package with the added bonus of up to 150 mA of output current. See Figure 21. The MC1723G uses both a positive and negative power supply. The reference voltage of the MC1723G is then developed with respect to the negative voltage and appears as a common-mode signal to the reference amplifier in the D-to-A converter. This allows use of its output amplifier as a classic current-to-voltage converter with the non-inverting input grounded.

Since ±15 V and +5.0 V are normally available in a combination digital-to-analog system, only the -5.0 V need be developed. A resistor divider is sufficiently accurate since the allowable range on pin 5 is from -2.0 to -8.0 volts. The 5.0 kilohm pulldown resistor on the amplifier output is necessary for fast negative transitions.

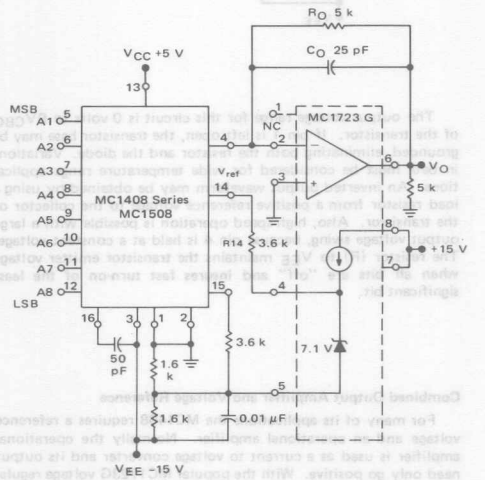
Full scale output may be increased to as much as 32 volts by increasing R_O and raising the +15 V supply voltage to 35 V maximum. The resistor divider should be altered to comply with the maximum limit of 40 volts across the MC1723G. C_O may be decreased to maintain the same R_OC_O product if maximum speed is desired.

APPLICATIONS INFORMATION (continued)

Programmable Power Supply

The circuit of Figure 21 can be used as a digitally programmed power supply by the addition of thumbwheel switches and a BCD-to-binary converter. The output voltage can be scaled in several ways, including 0 to +25.5 volts in 0.1-volt increments, ±0.05 volt; or 0 to 5.1 volts in 20 mV increments, ±10 mV.

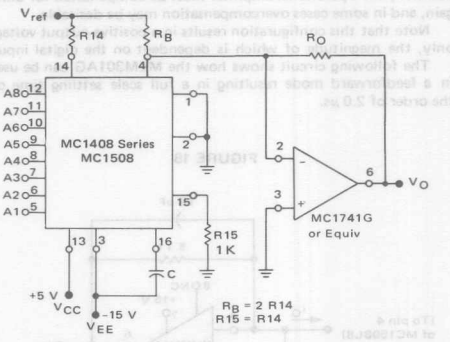
FIGURE 21 – COMBINED OUTPUT AMPLIFIER and VOLTAGE REFERENCE CIRCUIT



Bipolar or Negative Output Voltage

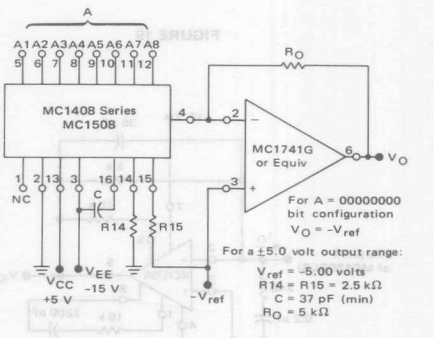
The circuit of Figure 22 is a variation from the standard voltage output circuit and will produce bipolar output signals. A positive current may be sourced into the summing node to offset the output voltage in the negative direction. For example, if approximately 1.0 mA is used a bipolar output signal results which may be described as a 8-bit "1's" complement offset binary. V_{ref} may be used as this auxiliary reference. Note that R_O has been doubled to 10 kilohms because of the anticipated 20 V(p-p) output range.

FIGURE 22 – BIPOLAR OR NEGATIVE OUTPUT VOLTAGE CIRCUIT



$$V_O = \frac{V_{ref}}{R14}(R_O)\left[\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right]-\frac{V_{ref}}{R_B}(R_O)$$

FIGURE 23 – BIPOLAR OR INVERTED NEGATIVE OUTPUT VOLTAGE CIRCUIT



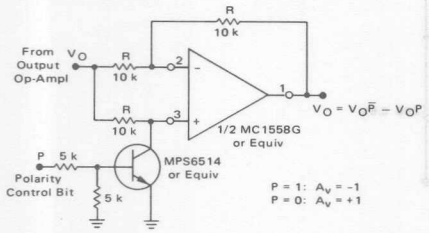
Decrease R_O to 2.5 kΩ for a 0 to -5.0-volt output range. This application provides somewhat lower speed, as previously discussed in the Output Voltage Range section of the General Information.

APPLICATIONS INFORMATION (continued)

Polarity Switching Circuit, 8-Bit Magnitude Plus Sign D-to-A Converter

Bipolar outputs may also be obtained by using a polarity switching circuit. The circuit of Figure 24 gives 8-bit magnitude plus a sign bit. In this configuration the operational amplifier is switched between a gain of +1.0 and −1.0. Although another operational amplifier is required, no more space is taken when a dual operational amplifier such as the MC1558G is used. The transistor should be selected for a very low saturation voltage and resistance.

FIGURE 24 – POLARITY SWITCHING CIRCUIT (8-Bit Magnitude Plus Sign D-to-A Converter)



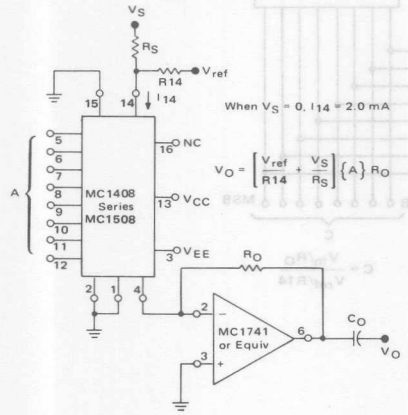
Programmable Gain Amplifier or Digital Attenuator

When used in the multiplying mode the MC1408 can be applied as a digital attenuator. See Figure 25. One advantage of this technique is that if R_S = 50 ohms, no compensation capacitor is needed. The small and large signal bandwidths are now identical and are shown in Figure 14.

The best frequency response is obtained by not allowing I_{14} to reach zero. However, the high impedance node, pin 16, is clamped to prevent saturation and insure fast recovery when the current through R14 goes to zero. R_S can be set for a ±1.0 mA variation in relation to I_{14}. I_{14} can never be negative.

The output current is always unipolar. The quiescent dc output current level changes with the digital word which makes ac coupling necessary.

FIGURE 25 – PROGRAMMABLE GAIN AMPLIFIER OR DIGITAL ATTENUATOR CIRCUIT



Panel Meter Readout

The MC1408 can be used to read out the status of BCD or binary registers or counters in a digital control system. The current output can be used to drive directly an analog panel meter. External meter shunts may be necessary if a meter of less than 2.0 mA full scale is used. Full scale calibration can be done by adjusting R14 or V_{ref}.

FIGURE 26 – PANEL METER READOUT CIRCUIT

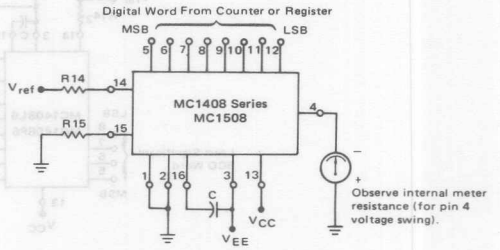
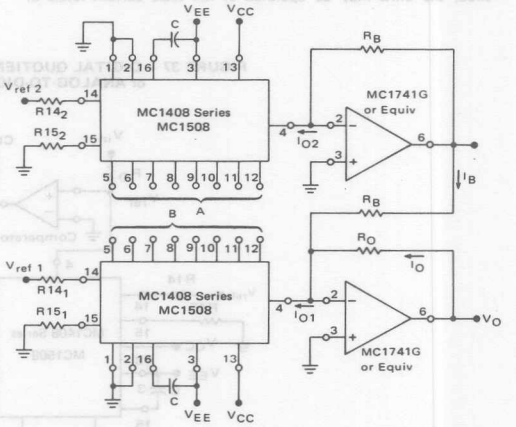


FIGURE 27 – DC COUPLED DIGITAL ATTENUATOR and DIGITAL SUBTRACTION



$$I_O = I_{O1} - I_{O2} = \frac{V_{ref\,1}}{R14_1}\{A\} - \frac{V_{ref\,2}}{R14_2}\{B\} \qquad I_{O2} = -I_B \quad I_B + I_O = I_{O1}$$

Digital Subtraction:

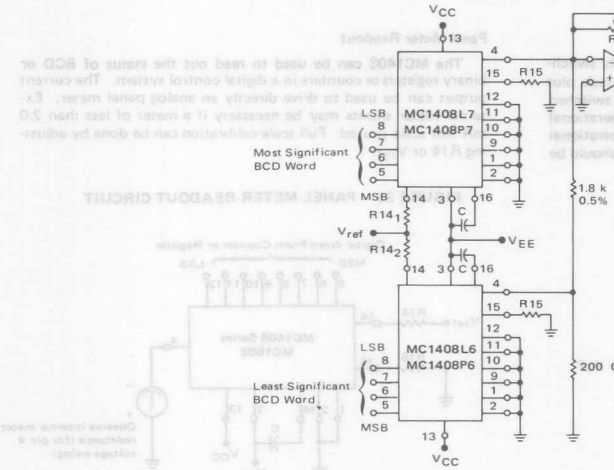
Let $\frac{V_{ref\,1}}{R14_1} = \frac{V_{ref\,2}}{R14_2}$

Programmable Amplifier: Connect Digital Inputs so A = B

$$V_O = \frac{V_{ref\,1}}{R14_1} R_O [\{A\} - \{B\}] \qquad V_O = \{A\}\left[\frac{V_{ref\,1}}{R14_1} - \frac{V_{ref\,2}}{R14_2}\right]$$

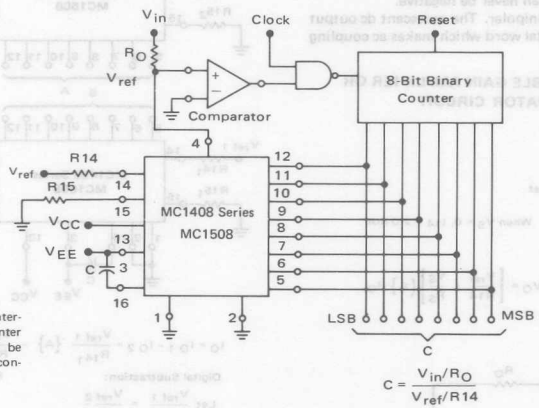
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FIGURE 36 – TWO-DIGIT BCD CONVERSION



Two 8-bit, D-to-A converters can be used to build a two digit BCD D-to-A or A-to-D converter. If both outputs feed the virtual ground of an operational amplifier, 10:1 current scaling can be achieved with a resistive current divider. If current output is desired, the units may be operated at full scale current levels of 4.0 mA and 0.4 mA with the outputs connected to sum the currents. The error of the D-to-A converter handling the least significant bits will be scaled down by a factor of ten and thus an MC1408L6 may be used for the least significant word.

FIGURE 37 – DIGITAL QUOTIENT OF TWO ANALOG VARIABLES or ANALOG-TO-DIGITAL CONVERSION



The circuit shown is a simple counter-ramp converter. An UP/DOWN counter and dual threshold comparator can be used to provide faster operation and continuous conversion.

MOTOROLA

MC6108

Advance Information

8-BIT MPU BUS-COMPATIBLE HIGH SPEED A-TO-D CONVERTER

The MC6108 is a microprocessor compatible, 8-bit, high speed analog-to-digital converter. Included are a precision reference, DAC, comparator, SAR, matched scale resistors, 3-state output buffers, and control logic. Conversion can be completed in under 2.0 μs and input voltage ranges of 0 to +10 V, 0 to +5.0 V, and −5.0 to +5.0 V can be converted without additional external components. With appropriate external resistors, the converter can accommodate other input voltage ranges. 8-bit linearity and monotonic operation with no missing codes are guaranteed over temperature. Bus compatibility is provided for by the 3-state outputs (latches not required).

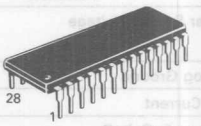
The MC6108 conversion time is short enough to allow most microprocessors to accept the data immediately after requesting a conversion. Applications include process control systems, servo control systems, waveform storage, signal processing, and others.

This device is functionally and pin compatible with the AM6108.

- 1.8 μs Conversion Time (Guaranteed)
- Microprocessor Compatible — Connect Directly to Data Bus
- Trimmed Internal Voltage Reference
- 0.1% Nonlinearity (Typ)
- Low Operating Voltage (+5.0 V, −5.2 V)
- Internal Matched Gain, Reference, and Offset Resistors
- Pin Programmable Natural Binary or Two's Complement
- Conversion Complete Available as Interrupt or on Data Bus
- Max Power Dissipation — 415 mW

8-BIT MPU BUS-COMPATIBLE HIGH SPEED A-TO-D CONVERTER

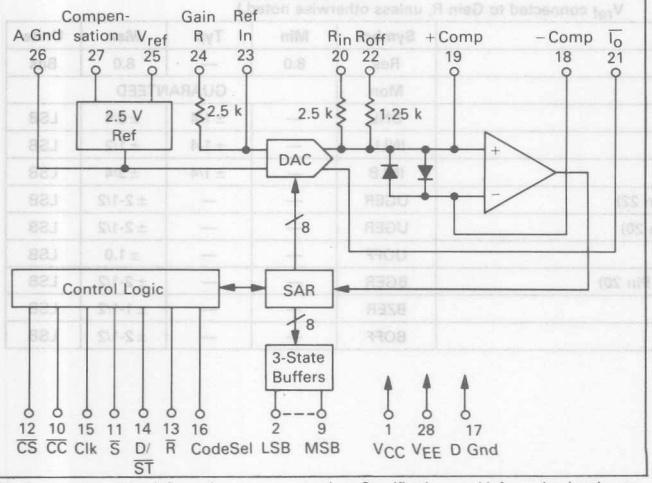
SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 710-02

6

BLOCK DIAGRAM



PIN CONNECTIONS



This document contains information on a new product. Specifications and information herein are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(Voltages referred to D. Gnd except where noted)

Parameter	Value	Units
V_{CC} (Pin 1)	−0.3, +7.0	V
V_{EE} (Pin 28)	+0.3, −7.0	V
Max Differential ($V_{CC} - V_{EE}$)	12	V
Digital Inputs (Pins 11–16)	−0.5, +6.0	V
A. Gnd (Pin 26)	±1.0	V
Input Current @ Ref In, Gain R	3.0	mA
Voltage @ Gain R	V_{CC}, V_{EE}	V
Voltage @ R_{in}, R_{off}	±12	V
Voltage @ +Comp, −Comp, $\overline{I_o}$	−2.5, +12	V
Voltage @ D0–D7 (in 3-state mode)	−0.5, +6.0	V
Junction Temperature	−65, +150	°C

Devices should not be operated at these values. The "Recommended Operating Limits" provide for actual device operation.

RECOMMENDED OPERATING LIMITS

(Voltages referred to D. Gnd except where noted)

Parameter	Symbol	Min	Typ	Max	Units
Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V
	V_{EE}	−5.46	−5.2	−4.94	V
Analog Ground	AGnd	−0.1	0	0.1	V
V_{ref} Current	I_{Vref}	0	—	5.0	mA
Voltage @ Gain R	—	1.25	2.5	5.0	V
Ref In Current	I_{ref}	0.5	1.0	2.0	mA
Voltage @ R_{in}	V_{in}	−8.0	—	10	V
Voltage @ R_{off}	V_{off}	−8.0	—	10	V
Clock Frequency	f_{clk}	0	—	5.0	MHz
Voltage @ −Comp	—	0	0	4.0	V
Voltage @ $\overline{I_o}$	—	−1.0	0	+5.0	V
Digital Input Voltage	—	0	—	5.25	V
Ambient Temperature	T_A	0	—	+70	°C

TRANSFER CHARACTERISTICS (V_{CC} = +5.0 V, ±5.0%, V_{EE} = −5.2 V, ±5.0%, 0 < T_A < 70°C, Clk = 5.0 MHz, V_{ref} connected to Gain R, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Units
Resolution	Res	8.0	—	8.0	Bits
Monotonicity	Mon		GUARANTEED		
Differential NonLinearity	DNL	—	±1/4	±3/4	LSB
Integral NonLinearity (Unipolar)	INLU	—	±1/4	±1/2	LSB
Integral NonLinearity (Bipolar)	INLB	—	±1/4	±3/4	LSB
Unipolar Gain Error (V_{in} = 0 to +5.0 V @ Pin 22)	UGER	—	—	±2-1/2	LSB
Unipolar Gain Error (V_{in} = 0 to +10 V @ Pin 20)	UGER	—	—	±2-1/2	LSB
Unipolar Offset Error (D7–D0 = 00_H to 01_H)	UOFF	—	—	±1.0	LSB
Bipolar Gain Error (V_{in} = −5.0 to +5.0 V @ Pin 20)	BGER	—	—	±2-1/2	LSB
Bipolar Zero Error (D7–D0 = $7F_H$ to 80_H)	BZER	—	—	±1-1/2	LSB
Bipolar Offset Error (D7–D0 = 00_H to 01_H)	BOFF	—	—	±2-1/2	LSB

TRANSFER CHARACTERISTICS (continued)

Parameter	Symbol	Min	Typ	Max	Units
I_o Full Scale Current (D7–D0 = FF_H, T_A = 25°C) (See Text "DAC")	I_{FS}	3.1	3.992	4.9	mA
$\overline{I_o}$ Zero Scale Current (D7–D0 = FF_H, T_A = 25°C) (See Text "DAC")	$\overline{I_{ZS}}$	−5.0	—	+5.0	μA
I_o Zero Scale Current (D7–D0 = 00_H, T_A = 25°C) (See Text "DAC")	I_{ZS}	3.0	7.8	13	μA
$\overline{I_o}$ Full Scale Current (D7–D0 = 00_H, T_A = 25°C) (See Text "DAC")	$\overline{I_{FS}}$	3.1	3.984	4.9	mA
DAC Current Gain (See Text "DAC")	G_{DAC}	3.92	4.0	4.08	—
Gain Sensitivity to V_{CC} Variations ($4.75 < V_{CC} < 5.25$ V, V_{EE} = −5.2 V)	$PSSV_{CC}$	—	±0.01	±0.2	%FS
Gain Sensitivity to V_{EE} Variations ($-5.46 < V_{EE} < -4.94$ V, V_{CC} = +5.0 V)	$PSSV_{EE}$	—	±0.02	±0.2	%FS

INTERNAL REFERENCE SUPPLY

Pin 25 Voltage ($I_{ref} \approx -1.0$ mA, V_{CC} = +5.0, V_{EE} = −5.2)	V_{ref}	2.475	2.5	2.525	V
Temperature Coefficient	T_C	—	±20	—	ppm/°C
Load Regulation (-1.0 mA $< I_{ref} < -5.0$ mA)	Reg_{load}	—	±0.05	±0.2	$\%V_{ref}$
Line Regulation ($4.75 < V_{CC} < 5.25$ V)	Reg_{line}	—	±0.02	±0.2	$\%V_{ref}$
Noise (f_n = 10 kHz to 1.0 MHz, T_A = 25°C)	—	—	20	—	μV_{rms}
Short Circuit Current (T_A = 25°C)	IRSC	−30	−20	−5	mA

POWER SUPPLIES

V_{CC} Current (Outputs unloaded)	I_{CC}	5.0	20	27	mA
V_{EE} Current (Outputs unloaded)	I_{EE}	−50	−38	−5	mA
Power Dissipation (Outputs unloaded)	P_D	—	300	415	mW

ANALOG INPUTS (T_A = 25°C)

Input Resistance @ Gain R (Pin 24)	R_{GR}	—	2.5	—	kΩ
Input Resistance @ R_{in} (Pin 20)	R_{RI}	1.75	2.5	3.25	kΩ
Input Resistance @ R_{off} (Pin 22)	R_{RO}	—	1.25	—	kΩ
Reference Input Offset Voltage (Pin 23–26)	Ref_{off}	−10	—	+10	mV
Comparator Input Clamp Voltage (4.0 mA through the back-to-back diodes)	V_{clamp}	±0.4	±0.8	±1.3	V
Input Capacitance @ +Comp (Pin 19)	C_C	—	20	—	pF
Input Capacitance @ $\overline{I_o}$ (Pin 21)	C_I	—	10	—	pF
Input Capacitance @ R_{in}, R_{off}, Ref In, Gain R, −Comp.	—	—	2.0	—	pF

DIGITAL INPUTS

Input Voltage — High (Pins 11–16)	V_{IH}	2.0	—	5.25	V
Input Voltage — Low (Pins 11–16)	V_{IL}	0	—	0.8	V
Input Current @ 4.0 V (Pins 11–16)	I_{IH}	—	—	10	μA
Input Current @ 0 V (Pins 11–16)	I_{IL}	—	—	10	μA

DIGITAL OUTPUTS

Output Voltage — High (I_{OH} = −400 μA, Pins 2–10)	V_{OH}	2.4	3.2	—	V
Output Voltage — Low (I_{OL} = 8.0 mA, Pins 2–10)	V_{OL}	—	0.15	0.4	V
Short Circuit Current* (Pins 2–10, T_A = 25°C)	I_{SC}	−50	−25	—	mA
Three-State Leakage (V_O = 2.4 V, Pins 2–9) (V_O = 0.4 V, Pins 2–9)	I_{HLK} I_{LLK}	−20 −20	— —	+20 +20	μA
Capacitance (3-State Mode, Pins 2–9)	C_O	—	7.0	—	pF

*Short circuits should be limited to 1.0 second max, 1 output at a time.
Note: Currents into a pin designated as +, currents out of a pin designated as −

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INPUTS

$\overline{S}$ High After CLK High*	t_{CKS}	0	—	—	ns
$\overline{S}$ High Before CLK High*	t_{SS}	25	—	—	ns
CLK Low Time	t_{CKL}	50	—	—	ns
CLK High Time	t_{CKH}	50	—	—	ns
CLK Rise, Fall Time	t_r, t_f	—	—	100	ns
$\overline{CS}$, CLK, $\overline{S}$ Concurrent Low Time*	t_{ST}	50	—	—	ns
Clock Frequency	f_{CLK}	—	—	5.0	MHz

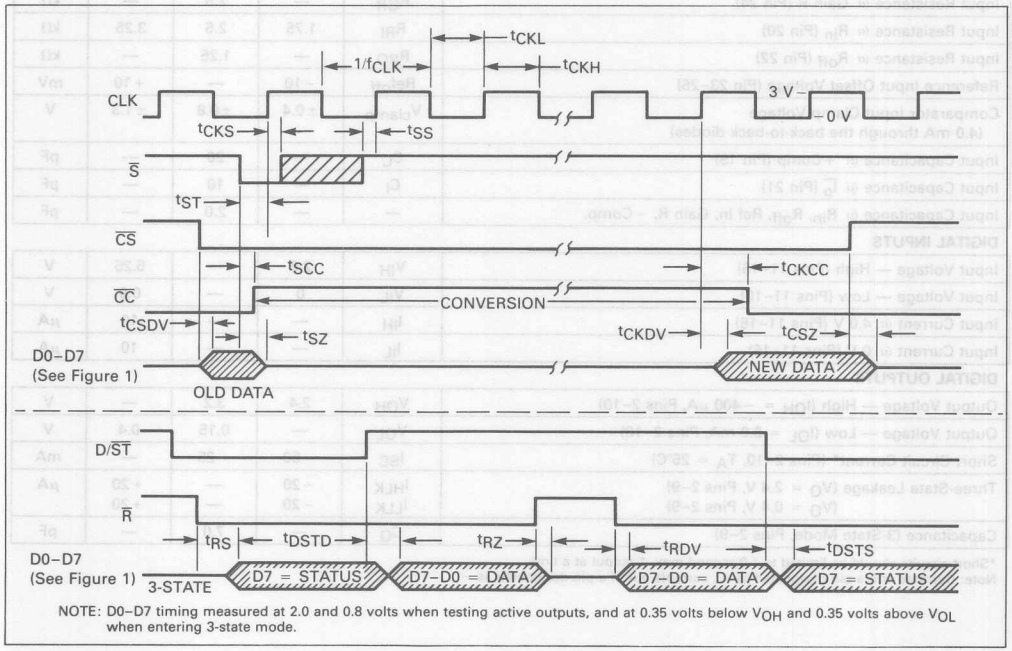
*See text (Sequence of Operation)

OUTPUTS

$\overline{CC}$ High from $\overline{S}$, $\overline{CS}$, or CLK Low	t_{SCC}	—	25	55	ns
Data to 3-State from $\overline{S}$, and CLK Low**	t_{SZ}	—	25	55	ns
$\overline{CC}$ Low from CLK High	t_{CKCC}	—	15	40	ns
Data Valid from CLK High**	t_{CKDV}	—	25	50	ns
Data Valid from $\overline{CS}$ Low**	t_{CSDV}	—	25	40	ns
Data to 3-State from $\overline{CS}$ High**	t_{CSZ}	—	20	40	ns
Data Valid from $\overline{R}$ Low**	t_{RDV}	—	20	40	ns
Data to 3-State from $\overline{R}$ High**	t_{RZ}	—	20	40	ns
D7 to Status from D/$\overline{ST}$ Low**	t_{DSTS}	—	20	40	ns
D7 to Data from D/$\overline{ST}$ High**	t_{DSTD}	—	20	40	ns
D7 to Status from $\overline{R}$ Low**	t_{RS}	—	20	40	ns

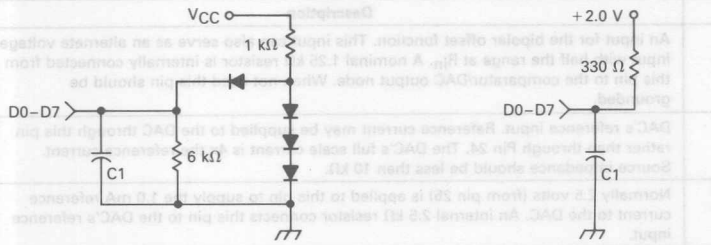
**See Figure 1 for output conditions

SYSTEM TIMING DIAGRAM



NOTE: D0–D7 timing measured at 2.0 and 0.8 volts when testing active outputs, and at 0.35 volts below V_{OH} and 0.35 volts above V_{OL} when entering 3-state mode.

FIGURE 1 — DATA OUTPUT LOAD TEST CIRCUIT



Active Outputs

Outputs To 3-State From Active

TEMPERATURE SPECIFICATIONS ($0° < T_A < 70° C$)

Function	Pin	Typical Change	Units
V_{ref}	25	±20	ppm/°C
DAC Current Gain	—	±8.0	ppm/°C
$\overline{I_O}$ Dynamic Impedance	21	+1.1	%/°C
Reference Input Offset	23–26	±20	μV/°C
Resistance @ R_{in}, R_{off}, Gain R	20,22,24	+0.1	%/°C

PIN DESCRIPTIONS

Symbol	Pin	Description
V_{CC}	1	To be connected to a 5.0 volts (±5.0%) supply.
D0–D7	2–9	TTL level data outputs capable of three-state mode. Pin 2 is the LSB, Pin 9 is the MSB. Pin 9 can also indicate conversion status.
$\overline{CC}$	10	Conversion Complete. TTL level output. High indicates conversion in progress, low indicates conversion complete and valid data at the outputs. This output does not have three-state capability.
$\overline{S}$	11	Start conversion — TTL Input. Taking $\overline{S}$ low (with Clock and Chip Select low) resets the SAR. Taking $\overline{S}$ high allows the conversion to start.
$\overline{CS}$	12	Chip Select — TTL Input. When low, a conversion may be initiated or data read at the outputs. When high, data outputs are in the three-state mode, and other digital inputs are ignored.
$\overline{R}$	13	Read — TTL Input. When low, data may be read at D0–D7. When high, D0–D7 are in three-state condition.
D/$\overline{ST}$	14	Data/$\overline{Status}$ — TTL Input. When high, D0–D7 provide normal data. When low, D7 indicates "Conversion Complete" status, while D0–D6 are in three-state mode.
CLK	15	Clock — TTL Input. 0–5.0 MHz.
CodeSel	16	Code Select — TTL Input. When low, output data is in 2's complement format. When high, output data is straight binary (offset binary when used in the bipolar mode).
D. Gnd	17	Digital Ground. Connect to ground associated with digital side of the circuitry.
−Comp	18	Negative input of the comparator. Normally grounded, a voltage on this pin will provide an offset of the input voltage range.
+Comp	19	Positive input of the comparator. Normally open, this pin may be used for input voltage ranges other than 0–10 volts, or ±5.0 volts.
R_{in}	20	The voltage to be converted to a digital equivalent is normally applied to this pin. A nominal 2.5 kΩ resistor is internally connected from this pin to the comparator/DAC output node.
$\overline{I_O}$	21	Current flows into this pin, complementary in value to the DAC's normal current output (I_O). Normally grounded, it may be connected to a resistor to ground or a positive voltage source in order to provide an analog output.

PIN DESCRIPTIONS — continued

Symbol	Pin	Description
R_{off}	22	An input for the bipolar offset function. This input can also serve as an alternate voltage input with half the range at R_{in}. A nominal 1.25 kΩ resistor is internally connected from this pin to the comparator/DAC output node. When not used this pin should be grounded.
Ref In	23	DAC's reference input. Reference current may be supplied to the DAC through this pin rather than through Pin 24. The DAC's full scale current is 4x the reference current. Source impedance should be less than 10 kΩ.
Gain R	24	Normally 2.5 volts (from pin 25) is applied to this pin to supply the 1.0 mA reference current to the DAC. An internal 2.5 kΩ resistor connects this pin to the DAC's reference input.
V_{ref}	25	Output of the internal precision 2.5 volt reference supply, it can supply up to 5.0 mA. Normally used to supply the DAC's reference current and the bipolar offset current.
A. Gnd	26	Analog Ground. Connect to ground associated with the analog side of the circuitry.
Compen	27	Compensation for the reference supply regulator. Typically, a 0.01 μF capacitor is connected from this pin to A. Gnd or to V_{EE}.
V_{EE}	28	To be connected to a −5.2 volts (±5.0%) supply.

DESIGN GUIDELINES

ANALOG SECTION

DAC (Refer to Figures 2 and 3)

The DAC generates an output current (I_o) which is proportional to both the reference current and the digital input presented to it by the Successive Approximation Register (SAR), according to the following formula:

$$I_o = \frac{I_{ref} \times 4 \times A}{256} + I_{zs} \quad (1)$$

where A is the binary digital code (0–255), and I_{zs} is the zero scale current. I_o flows ***into*** the DAC, never out. The 4x (±2.0%) factor is a current gain built into the DAC. For a nominal I_{ref} of 1.0 mA, the maximum I_o (@A = 255) is 3.992 mA (which includes an I_{zs} of 7.8 μA). I_{zs} is built in so the first transition occurs when the signal voltage (V_{in}) is 1/2 LSB above its minimum value. In normal operation, I_o is supplied from the signal voltage that is being converted to a digital code. Therefore, the signal source must be capable of supplying up to 4.0 mA in the unipolar mode. I_{ref} is the reference current flowing in through either pin 23 or 24. See Figure 2 for the basic unipolar configuration.

In the bipolar mode, an offset current of 2.0 mA is supplied to the I_o node (normally through R_{off}) in order that V_{in} may be symmetrical about zero volts. The signal source must be capable of sinking 2.0 mA when at the negative extreme, and sourcing 2.0 mA when at the positive extreme. See Figure 3 for the basic bipolar configuration.

+Comp (Pin 19) is maintained close to a virtual ground after a conversion as long as −Comp (Pin 18) is at ground. The voltage at +Comp varies (nominally ±0.8 volts) during a conversion as the DAC forces different current values at I_o and will end up close to zero at the end of a conversion. Because of the varying voltage at +Comp, the current from the signal source and the offset source (if used) will vary with each step of the successive approximation sequence, necessitating that the signal source have a dynamic impedance less than

$$\frac{V_1 \times R_X}{1.6\ V} \quad (2)$$

where V_1 = 1/2 LSB of the signal voltage, and
R_X = Resistance between the signal source and Pin 19
(2.5 kΩ if using R_{in}, 1.25 kΩ if using R_{off}).

Normally Pin 19 is left open, although it may be used as a path for the offset current, or the signal current (to be digitized), with appropriate external resistors. See the Applications Information for more details.

I_{ref} flows ***into*** the DAC, never out, and should be between 0.5 mA and 2.0 mA to preserve linearity and accuracy. Linearity specified in the Electrical Characteristics is tested @ I_{ref} of ≈1.0 mA. The reference input stage is depicted in Figure 4. Normally I_{ref} is supplied by the MC6108's internal 2.5 volt reference (Pin 25) through Gain R (Pin 24). If a separate voltage source is used for the reference current, it must be free of noise, spikes, and ripple since the accuracy of a conversion is directly related to the quality and stability of the reference.

SIGNAL VOLTAGE

The input signal voltage (to be digitized) is applied to either R_{in}, R_{off}, or through an appropriate external resistor to +Comp, such that current from the signal source flows into the DAC's I_o port. The preset ranges, with V_{ref} connected to Gain R are as follows:

Input Range	Connect R_{in} to	Connect R_{off} to
0 to +10 V	V_{in}	A. Gnd
0 to +5.0 V	A. Gnd	V_{in}
−5.0 to +5.0 V	V_{in}	V_{ref}

FIGURE 2 — BASIC UNIPOLAR CONFIGURATION

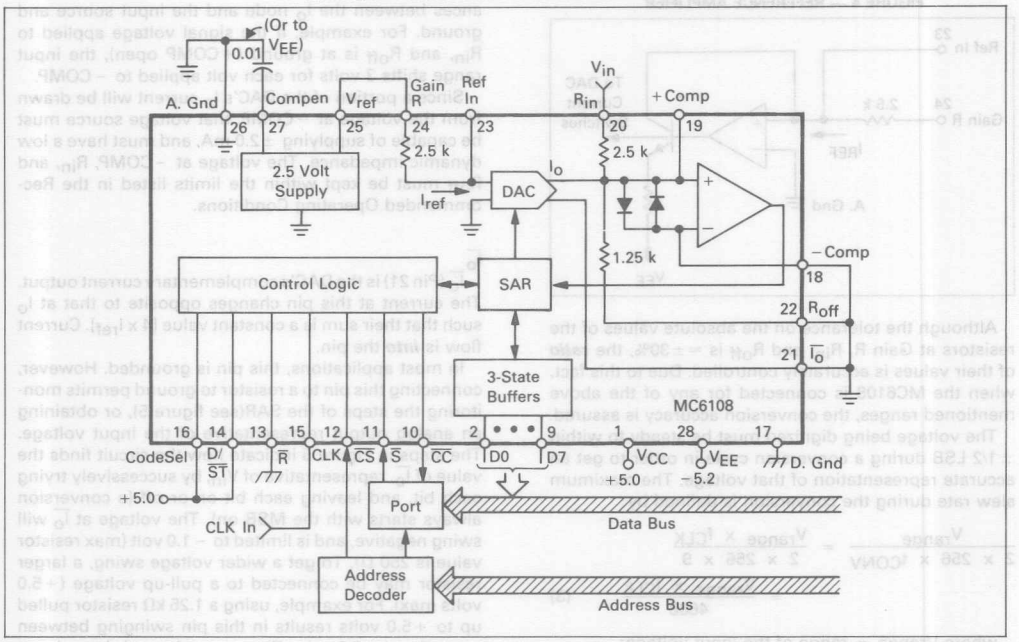
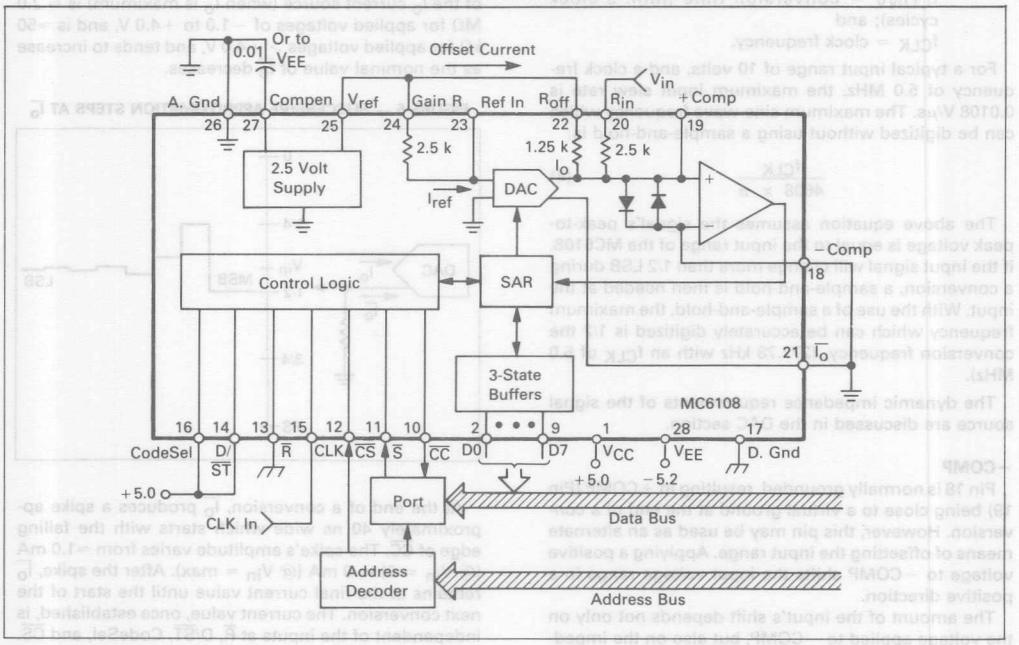
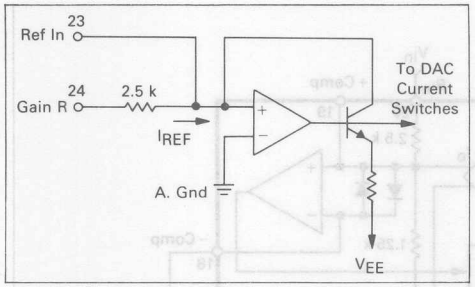


FIGURE 3 — BASIC BIPOLAR CONFIGURATION



6



Although the tolerance on the absolute values of the resistors at Gain R, R_{in}, and R_{off} is $\approx \pm 30\%$, the ***ratio*** of their values is accurately controlled. Due to this fact, when the MC6108 is connected for any of the above mentioned ranges, the conversion accuracy is assured.

The voltage being digitized must be steady to within $\pm 1/2$ LSB during a conversion cycle in order to get an accurate representation of that voltage. The maximum slew rate during the conversion is defined by:

$$\frac{V_{range}}{2 \times 256 \times t_{CONV}} = \frac{V_{range} \times f_{CLK}}{2 \times 256 \times 9} = \frac{V_{range} \times f_{CLK}}{4608} \quad (3)$$

where Vrange = range of the input voltage;
t_{CONV} = conversion time (min. 9 clock cycles); and
f_{CLK} = clock frequency.

For a typical input range of 10 volts, and a clock frequency of 5.0 MHz, the maximum input slew rate is 0.0108 V/μs. The maximum sine-wave frequency which can be digitized without using a sample-and-hold is:

$$\frac{f_{CLK}}{4608 \times \pi} \quad (4)$$

The above equation assumes the signal's peak-to-peak voltage is equal to the input range of the MC6108. If the input signal will change more than 1/2 LSB during a conversion, a sample-and-hold is then needed at the input. With the use of a sample-and-hold, the maximum frequency which can be accurately digitized is 1/2 the conversion frequency, (277.78 kHz with an f_{CLK} of 5.0 MHz).

The dynamic impedance requirements of the signal source are discussed in the DAC section.

–COMP

Pin 18 is normally grounded, resulting in +COMP (Pin 19) being close to a virtual ground at the end of a conversion. However, this pin may be used as an alternate means of offsetting the input range. Applying a positive voltage to –COMP shifts the input voltage range in a positive direction.

The amount of the input's shift depends not only on the voltage applied to –COMP, but also on the impedance to ground. For example, if the signal voltage applied to R_{in}, and R_{off} is at ground (+COMP open), the input range shifts 3 volts for each volt applied to –COMP.

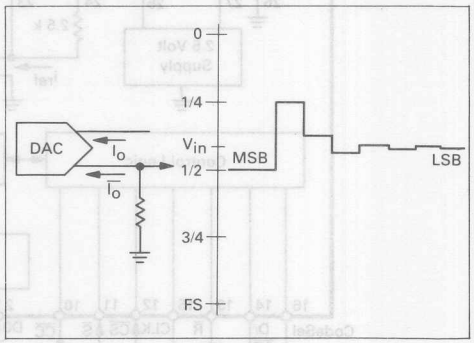
Since a portion of the DAC's I_o current will be drawn from the voltage at –COMP, that voltage source must be capable of supplying ± 2.0 mA, and must have a low dynamic impedance. The voltage at –COMP, R_{in}, and R_{off} must be kept within the limits listed in the Recommended Operating Conditions.

$\overline{I_o}$

$\overline{I_o}$ (Pin 21) is the DAC's complementary current output. The current at this pin changes opposite to that at I_o such that their sum is a constant value [4 x I_{ref}]. Current flow is ***into*** the pin.

In most applications, this pin is grounded. However, connecting this pin to a resistor to ground permits monitoring the steps of the SAR(see figure 5), or obtaining an analog output representative of the input voltage. The steps in Figure 5 indicate how the circuit finds the value of $\overline{I_o}$, representative of V_{in}, by successively trying each bit, and leaving each bit on or off (a conversion always starts with the MSB on). The voltage at $\overline{I_o}$ will swing negative, and is limited to –1.0 volt (max resistor value is 250 Ω). To get a wider voltage swing, a larger resistor may be connected to a pull-up voltage (+5.0 volts max). For example, using a 1.25 kΩ resistor pulled up to +5.0 volts results in this pin swinging between ground and +5.0 volts. The output dynamic impedance of the $\overline{I_o}$ current source (when $\overline{I_o}$ is maximum) is $\approx$ 2.0 MΩ for applied voltages of –1.0 to +4.0 V, and is $\approx$50 kΩ for applied voltages > +4.0 V, and tends to increase as the nominal value of $\overline{I_o}$ decreases.

FIGURE 5 — SUCCESSIVE APPROXIMATION STEPS AT $\overline{I_o}$



At the end of a conversion, $\overline{I_o}$ produces a spike approximately 40 ns wide which starts with the falling edge of $\overline{CC}$. The spike's amplitude varies from $\approx$1.0 mA (@ V_{in} = 0) to 0 mA (@ V_{in} = max). After the spike, $\overline{I_o}$ remains at the final current value until the start of the next conversion. The current value, once established, is independent of the inputs at $\overline{R}$, D/$\overline{ST}$, CodeSel, and $\overline{CS}$.

REFERENCE SUPPLY

The internal bandgap reference produces an output of +2.500 volts, ±25 mV (@ V_{ref}, pin 25), and is primarily intended to supply the reference current and the bipolar offset current. The output impedance is typically <0.5 Ω for load currents up to 5.0 mA, and increases rapidly at higher currents. Variations in V_{ref} are typically < 0.5 mV as V_{CC} is varied from +4.75 to +5.25 volts, and V_{ref} is independent of V_{EE} variations. The output is designed to source, not sink current.

A 0.001 μF capacitor from V_{ref} to A. Gnd is recommended to reduce noise on this output produced by the digital section. A 0.01 μF capacitor from the Compensation pin (Pin 27) to A. Gnd, or to V_{EE}, is necessary to stabilize the regulator.

POWER SUPPLIES

The power supplies are to be +5.0 volts, ±5.0% at V_{CC} (Pin 1), and −5.2 volts, ±5.0% at V_{EE} (Pin 28). For proper operation, bypassing is required for both supplies ***at the IC.*** 10 μF tantalum in parallel with 0.01 μF ceramic is recommended for each supply.

I_{CC} varies with the chip's different operating conditions, and is a maximum (typically 20 mA) during a conversion ($\overline{R}=0$, $D/\overline{ST}=1$, $\overline{CS}=0$) with the signal voltage at its minimum value. Minimum I_{CC} (typically 12 mA) occurs during a conversion with the signal voltage at its maximum value. I_{CC} is typically 16 mA when the MC6108 is deselected ($\overline{CS}=1$), and under all conditions, I_{CC} is independent of clock frequency.

I_{EE} is typically 38 mA, and varies <2.0 mA over different operating conditions. I_{EE} is independent of clock frequency.

DIGITAL SECTION

SEQUENCE OF OPERATION

A conversion is initiated when the $\overline{S}$ (Start), $\overline{CS}$ (Chip select), and CLK (Clock) inputs are simultaneously low for a minimum of 50 ns. The three inputs may be taken low in any sequence, including simultaneously. After all three have been brought low, $\overline{CC}$ (Conversion Complete) will change to a high state ≈25 ns later, indicating the SAR has been reset. A clock low-to-high transition must then occur before or with $\overline{S}$ switching high, and the conversion begins with the next CLK rising edge ($\overline{S}$ must precede that one by >25 ns). The conversion then requires seven complete clock cycles. At the end of the conversion, $\overline{CC}$ will switch low indicating the end of the conversion, and that valid data is available. See Figure 6 for the basic timing sequence.

If the $\overline{S}$, $\overline{CS}$, and CLK inputs appear simultaneously low ***during*** a conversion, the conversion sequence will be re-initiated at that point.

The following truth table describes the relationship of the six digital inputs (Pins 11–16):

Logic Inputs						Function
CLK	$\overline{CS}$	$\overline{S}$	$\overline{R}$	$D/\overline{ST}$	CodeSel	
X	1	X	X	X	X	Chip de-selected, D0–D7 @ Hi-Z
0	0	0	X	X	X	Reset SAR
↑ ↓	X	1	X	X	X	Conversion process (after SAR is reset)
X	0	X	1	X	X	D0–D7 @ Hi-Z
X	0	1	0	1	1	Read binary or offset binary data at D0–D7 after conversion
X	0	1	0	1	0	Read 2's complement data at D0–D7 after conversion
X	0	1	0	0	X	Read $\overline{CC}$ status at D7 (D0–D6 @ Hi-Z)

X = Don't care

Figure 7 depicts the input configurations in order to read the various output formats. Any digital input left open is equivalent to a Logic "0" — however, good design practice dictates that inputs should never be left open.

FIGURE 6 — CONVERSION TIMING DIAGRAM

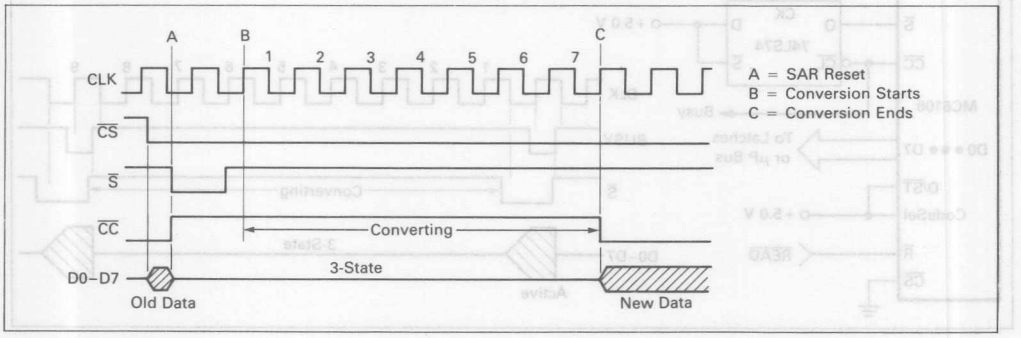
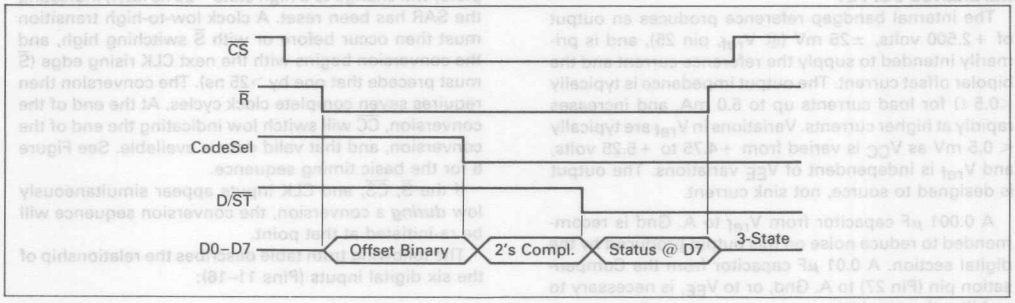


FIGURE 7 — OUTPUT DATA CONTROL



CLOCK

The clock input (Pin 15) is a TTL level input which steps the SAR through the successive approximation conversion process. There is no minimum required frequency, and the maximum operating frequency is listed in the timing characteristics. The clock duty cycle does not have to be 50%, but the minimum low and high times must be observed. The clock is needed only for the conversion, and may be removed or left applied to the MC6108 between conversions. The operation of $\overline{CS}$, D/$\overline{ST}$, $\overline{R}$, and CodeSel are not affected by the presence or absence of the clock.

CHIP SELECT

Chip Select (Pin 12) is a TTL level input which is normally used by a microprocessor's address decoding to select and de-select the device. A Logic "0" selects (enables) the MC6108, while a Logic "1" disables it. $\overline{CS}$ must be low for a conversion to start, and to read data at D0–D7 or status at D7 (see D/$\overline{ST}$ description). $\overline{CS}$ may be taken high during a conversion, as long as the minimum low time for $\overline{CS}$, $\overline{S}$, and CLK is adhered to, and then taken low in order to read the data after $\overline{CC}$ goes low. Alternately $\overline{CS}$ may be left low during the entire conversion.

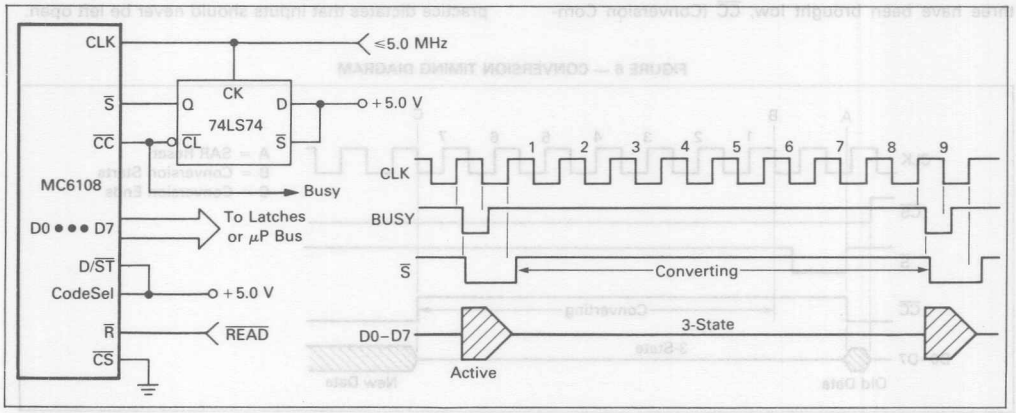
Whenever the MC6108 is de-selected, a conversion cannot be initiated, and D0–D7 are in the high-impedance condition, regardless of the other digital inputs.

START

$\overline{S}$ (Pin 11) is a TTL level input used to reset the SAR, and initiate a conversion. The SAR is reset when this pin is low simultaneous with the Clock and $\overline{CS}$ inputs for a minimum of 50 ns. $\overline{CC}$ output will then change to a high state. A clock rising edge must occur while $\overline{S}$ is low, or no later than coincident with its rising edge. There is no maximum time limit for $\overline{S}$ to stay low, but the conversion will not begin until the next rising edge of the Clock input ***after*** $\overline{S}$ goes high. Seven complete clock cycles are then needed to complete the conversion.

If the $\overline{S}$ input is connected to the $\overline{CC}$ output through a flip-flop (see Figure 8), the MC6108 will operate at the maximum possible conversion repetition rate, i.e. one conversion each 9 clock cycles.

FIGURE 8 — CONFIGURATION FOR MAXIMUM CONVERSION RATE



READ

$\overline{\text{Read}}$ (Pin 13) is a TTL level input which controls the state of the outputs (D0–D7) between conversions as long as the MC6108 is enabled ($\overline{CS}$ = 0). A Logic "1" forces the 8 outputs to a high impedance condition regardless of the other digital inputs. A Logic "0" permits reading the data at D0–D7 after the conversion is complete, or the $\overline{CC}$ status at D7 (depending on the D/$\overline{ST}$ input). During a conversion, $\overline{R}$ is ineffective, except for controlling D7 if D/$\overline{ST}$ is low.

The $\overline{\text{Read}}$ input differs from the $\overline{CS}$ input in that taking $\overline{\text{Read}}$ high does not prevent a conversion from being initiated in response to the $\overline{CS}$, CLK, and $\overline{S}$ inputs (described elsewhere). If desired, the $\overline{\text{Read}}$ input may be kept low at all times in a simple application.

CONVERSION COMPLETE

$\overline{CC}$ (Pin 10) is a TTL level output which indicates the status of the conversion. After $\overline{CS}$, CLK, and $\overline{S}$ are taken low to initiate a conversion, $\overline{CC}$ will go high ≈25 ns later. $\overline{CC}$ will stay high during the conversion, and then go low ≈15 ns after the rising edge of the clock corresponding to the end of the conversion. See Figure 6 and the System Timing Diagram.

The $\overline{CC}$ pin does not have a high impedance capability, and is therefore always active. The $\overline{CC}$ status is typically monitored through a port, or an interrupt pin.

DATA/$\overline{\text{STATUS}}$

D/$\overline{ST}$ (Pin 14) is a TTL level input which controls the information presented at D0–D7. When at a Logic "1", D0–D7 will provide the digital equivalent of the analog input at the end of the conversion (D0–D7 are in a high impedance mode during the conversion). When at a Logic "0", D0–D6 are maintained in a high impedance mode, while D7 provides the Conversion Complete status both during and after the conversion (D7 does not go into a high impedance mode). The rising and falling edges of D7, when providing status, follow those of $\overline{CC}$ (Pin 10) within ≈ 10 ns.

D/$\overline{ST}$ may be used by the microprocessor as a means of reading the Status ***and*** the Data on the bus rather than using a separate port for the $\overline{CC}$ output (Pin 10). However, since D7 is active during the conversion, the microprocessor cannot be busy with other functions during this time. If the microprocessor is to be busy during the conversion, the status may be checked by periodically switching the D/$\overline{ST}$ pin, or the $\overline{CS}$ pin, or by reading the $\overline{CC}$ pin (Pin 10) through a separate port or interrupt pin. $\overline{R}$ (Pin 13) must be low to read data or status.

CODE SELECT

CodeSel (Pin 16) is a TTL level input which controls the format of the binary data presented at D0–D7 at the end of a conversion. When at a Logic "1", the data is presented as natural binary or offset binary, depending on whether the analog input is unipolar or bipolar, respectively. When at a Logic "0", the output code is in 2's complement form (applicable to bipolar operation only). This pin has no effect on D7 when the D/$\overline{ST}$ input is low (see section on Data/$\overline{\text{Status}}$). The following tables illustrate examples of the different codes:

UNIPOLAR

Input	+10 V Range	+5.0 V Range	Natural Binary
FS — 1LSB	9.961 V	4.980 V	1111 1111
3/4 FS	7.500 V	3.750 V	1100 0000
1/2 FS	5.000 V	2.500 V	1000 0000
1/4 FS	2.500 V	1.250 V	0100 0000
0	0.000 V	0.000 V	0000 0000

BIPOLAR

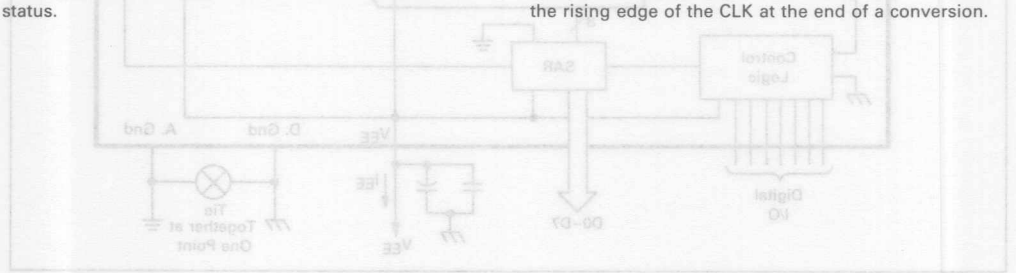
Input	±5.0 V Range	Offset Binary	2's Complement
+FS — 1LSB	4.961 V	1111 1111	0111 1111
+1/2 FS	2.500 V	1100 0000	0100 0000
MidScale	0.000 V	1000 0000	0000 0000
−1/2 FS	−2.500 V	0100 0000	1100 0000
−FS + 1LSB	−4.961 V	0000 0001	1000 0001
−FS	−5.000 V	0000 0000	1000 0000

If an input voltage range other than those listed above is used, and CodeSel is at a Logic "1" (binary format), the code 0000 0000 will correspond to the most negative input voltage, while the code 1111 1111 corresponds to the most positive input voltage (−1 LSB). The 2's complement code is the same as the binary with the MSB (D7) inverted.

DATA OUTPUTS

The data outputs (Pins 2–9) are TTL level outputs with high impedance capability. Pin 2 is the LSB (D0), while Pin 9 is the MSB (D7). The 8 outputs are in the high impedance mode during a conversion ($\overline{CC}$ = high), or if $\overline{CS}$ or $\overline{R}$ are high. D0–D6 are in the high impedance mode, and D7 is active, anytime that D/$\overline{ST}$ is low ($\overline{CS}$ = $\overline{R}$ = 0).

During normal operation, the 8 outputs change from valid data to high impedance within 55 ns after the SAR has been reset ($\overline{CS}$ = CLK = $\overline{S}$ = 0) at the beginning of a conversion, and back to valid data within 50 ns after the rising edge of the CLK at the end of a conversion.



POWER SUPPLIES, GROUNDING

The P.C. board layout, the quality of the power supplies and the ground system ***at the IC*** are very important in order to obtain proper operation. Noise, from any source, coming into the device on V_{CC}, V_{EE}, or ground can cause an incorrect output code due to interaction with the analog portion of the circuit. At the same time, noise generated within the MC6108 can cause incorrect operation if that noise does not have a clear path to ac ground.

Both the V_{CC} and V_{EE} power supplies must be decoupled to ground ***at the IC*** (within 1" max) with a 10 μF tantalum and a 0.01 μF ceramic. Tantalum capacitors are recommended since electrolytic capacitors simply have too much inductance at the frequencies of interest. The quality of the V_{CC} and V_{EE} supplies should then be checked at the IC with a high frequency scope. Noise spikes (always present when digital circuits are present) can easily exceed 400 mV peak, and if they get into the analog portion of the IC, the operation can be disrupted. Noise can be reduced by inserting resistors (<10 Ω, metal film) or inductors between the supplies and the IC.

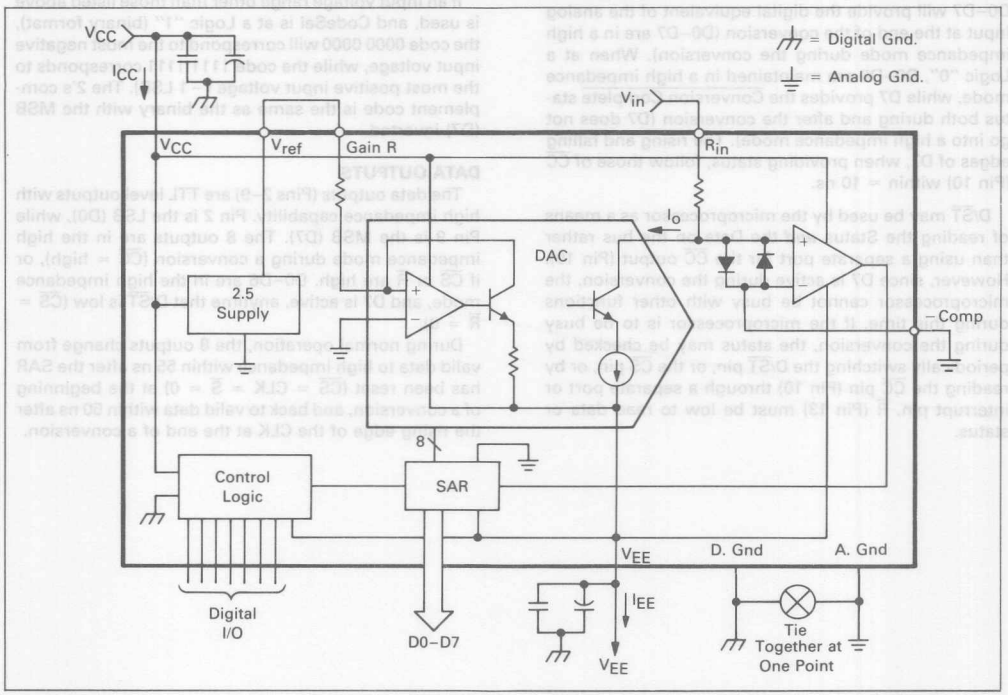
If switching power supplies are used, there will usually be spikes of 0.5 volts or greater at frequencies of 50 – 200 kHz. These spikes are generally more difficult to reduce because of their greater energy content. In extreme cases, 3-terminal regulators (MC78L05ACP, MC7905.2CT), with appropriate high frequency filtering, should be used and dedicated to the MC6108.

The ripple content of the supplies should not allow their magnitude to exceed the values in the Recommended Operating Limits.

The P.C. board tracks supplying V_{CC} and V_{EE} to the MC6108 should preferably not be at the tail end of the bus distribution, after passing through a maze of digital circuitry. The MC6108 should be close to the power supply, or the connector where the supply voltages enter the board. If the V_{CC} and V_{EE} lines are supplying considerable current to other parts of the boards, then it is preferable to have dedicated lines from the supply or connector directly to the MC6108.

The MC6108 has two ground pins — A. Gnd (Pin 26), and D. Gnd. (Pin 17). V_{CC} and V_{EE} should be referenced to D. Gnd. A. Gnd is mainly a signal ground, and is the return path for the internal 2.5 volt reference, and the DAC's reference amplifier. A. Gnd must be connected to D. Gnd, preferably at one point, and in a manner so as to not pick up noise. The dc voltage between A. Gnd and D. Gnd must be <100 mV. Long PC tracks between them should be avoided as the inductance (at 5.0 MHz) can create stability problems. See Figure 9 for a depiction of the major current paths.

FIGURE 9 — MAJOR CURRENT PATHS



FULL SCALE, ZERO ADJUSTMENTS

The unadjusted full scale accuracy (at max. V_{in}) of the MC6108, when the internal resistors are used (Figures 2 and 3), is guaranteed to be within 2-1/2 LSBs. The offset error (at min. V_{in}) is guaranteed to be less than 1LSB for the unipolar configuration, and 2-1/2 LSBs for the bipolar configuration. If the application requires greater accuracy at the end points, then adjustments are needed, as shown in Figures 10 and 11. The potentiometers should be 20-turn type, with low T.C. The 50 Ω resistor is added to the R_{in} pin to ensure that the potentiometers can provide adjustment over the full plus and minus error range.

FIGURE 10 — UNIPOLAR ADJUSTMENTS

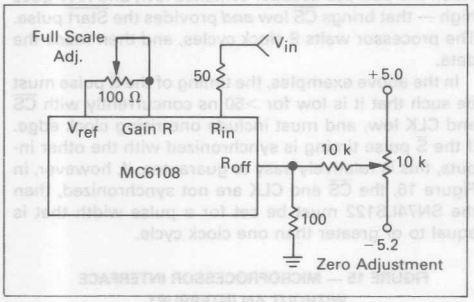
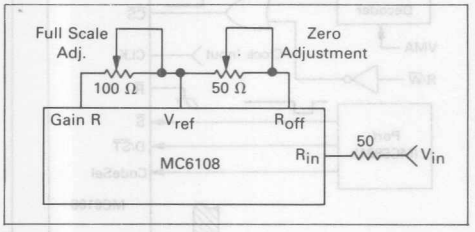


FIGURE 11 — BIPOLAR ADJUSTMENTS

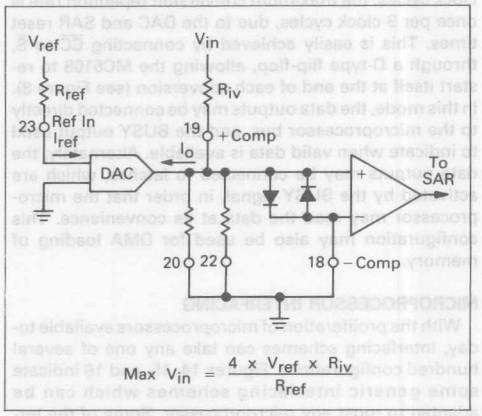


OTHER INPUT RANGES

The MC6108 has internal resistors providing preset input ranges of 0 to +10 volts, 0 to +5.0 volts, and −5.0 to +5.0 volts (see previous section entitled "Signal Voltage"). The input range, and the offset, are determined by the value of the resistors at Pins 20, 22, and 24. Where input ranges other than those listed above are to be digitized, then external resistors of comparable tolerance and temperature coefficient should be used for the reference (at Pin 23), ***and*** for the input signal (at Pin 19), ***and*** for the bipolar offset function (also at Pin 19). See Figures 12 and 13. R_{in} and R_{off} should be connected to A. Gnd when not used. Due to the tolerances of the absolute value of the internal resistors, they should not be used in conjunction with external resistors.

Figure 13 shows the reference current and the offset current supplied from the same reference source, which may be the internal reference (Pin 25). However, separate sources may be used for the two currents if desired.

FIGURE 12 — UNIPOLAR CONVERSION USING EXTERNAL REFERENCE AND RESISTORS

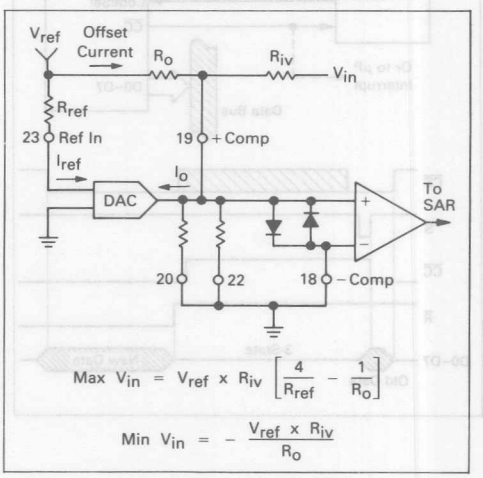


A modulation of the input signal (for waveform manipulation or signal processing) may be done by applying the modulating signal to the reference current. Rewriting equation 1 to determine the output code results in:

$$A = \frac{I_o \times 256}{4 \times I_{ref}} = \frac{V_{in} \times 256}{R_{in} \times 4 \times I_{ref}} \quad (5)$$

(The offset term has been omitted to simplify the equation.) As can be seen, the output code varies inversely with the reference. When varying the reference current, its value must be maintained between 0.5 and 2.0 mA, and the current flow ***must*** always be ***into*** Pin 23 or 24.

FIGURE 13 — BIPOLAR CONVERSION USING EXTERNAL REFERENCE & RESISTORS



6

MAXIMUM CONVERSION RATE

Although a conversion, once initiated, requires 7+ clock cycles, the maximum conversion repetition rate is once per 9 clock cycles, due to the DAC and SAR reset times. This is easily achieved by connecting $\overline{CC}$ to $\overline{S}$, through a D-type flip-flop, allowing the MC6108 to restart itself at the end of each conversion (see Figure 8). In this mode, the data outputs may be connected directly to the microprocessor bus, and the BUSY output used to indicate when valid data is available. Alternately, the data outputs may be connected to latches, which are activated by the BUSY signal, in order that the microprocessor may read the data at its convenience. This configuration may also be used for DMA loading of memory.

MICROPROCESSOR INTERFACING

With the proliferation of microprocessors available today, interfacing schemes can take any one of several hundred configurations. Figures 14, 15, and 16 indicate some generic interfacing schemes which can be adapted to most any microprocessor. Some of the terminology in the Figures is based on the MC6800 series of processors — other processors have similar functions by different names.

Figure 14 depicts a simple basic interface using a port (such as an MC6821) and/or an interrupt. A conversion is initiated when the active low address decoder switches low, R/$\overline{W}$ is high, and the port outputs one active low pulse to $\overline{S}$. At the end of the conversion, $\overline{CC}$ goes low, alerting the processor through the port or through an interrupt. The processor can then read the data at its convenience by switching $\overline{R}$ and $\overline{CS}$ low.

Figure 15 eliminates the need for an interrupt, and instead periodically checks the conversion status at D7 (D/$\overline{ST}$ = low) by reading the data bus. When D7 is low, the conversion is complete, and the D/$\overline{ST}$ input is then taken high so as to read the data at D0–D7.

Figure 16 eliminates the need for an interrupt or a port, but requires the processor to wait during the conversion until it is complete. The conversion is initiated when the address decoder switches low, and R/$\overline{W}$ goes high — that brings $\overline{CS}$ low ***and*** provides the $\overline{Start}$ pulse. The processor waits 9 clock cycles, and then reads the data.

In the above examples, the timing of the $\overline{S}$ pulse must be such that it is low for >50 ns concurrently with $\overline{CS}$ and CLK low, and must include one rising clock edge. If the $\overline{S}$ pulse timing is synchronized with the other inputs, this is relatively easy to guarantee. If, however, in Figure 16, the $\overline{CS}$ and CLK are not synchronized, then the SN74LS122 must be set for a pulse width that is equal to or greater than one clock cycle.

FIGURE 14 — BASIC MICROPROCESSOR INTERFACE

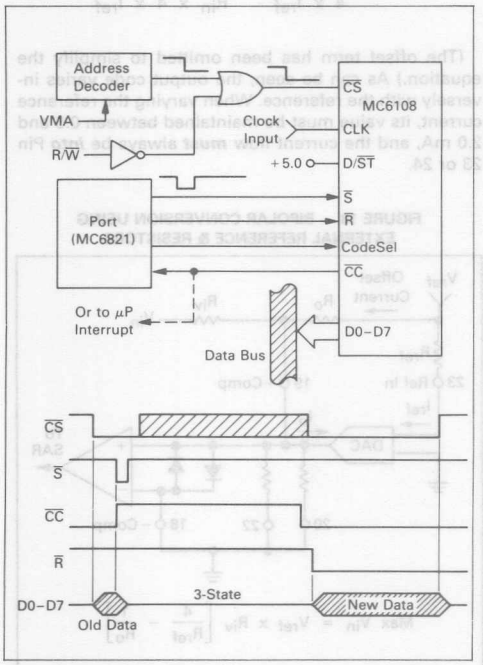


FIGURE 15 — MICROPROCESSOR INTERFACE WITHOUT AN INTERRUPT

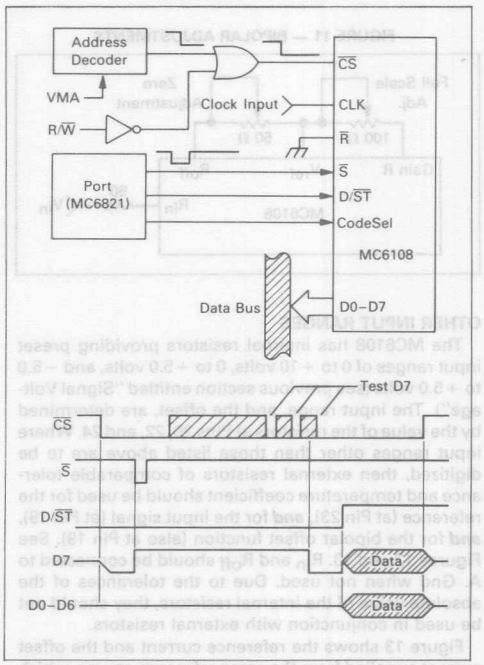
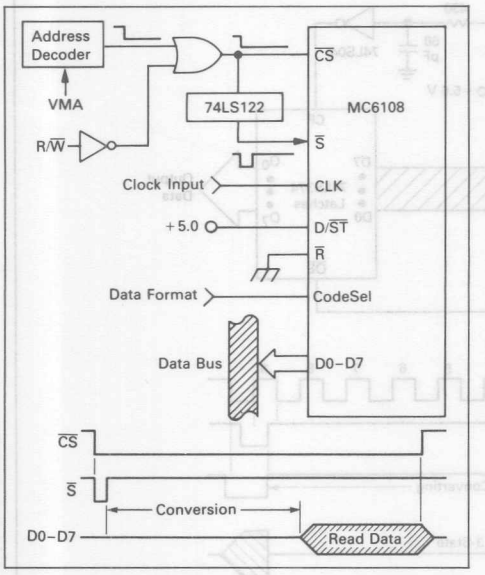


FIGURE 16 — MICROPROCESSOR INTERFACE WITHOUT USING A PORT OR INTERRUPT



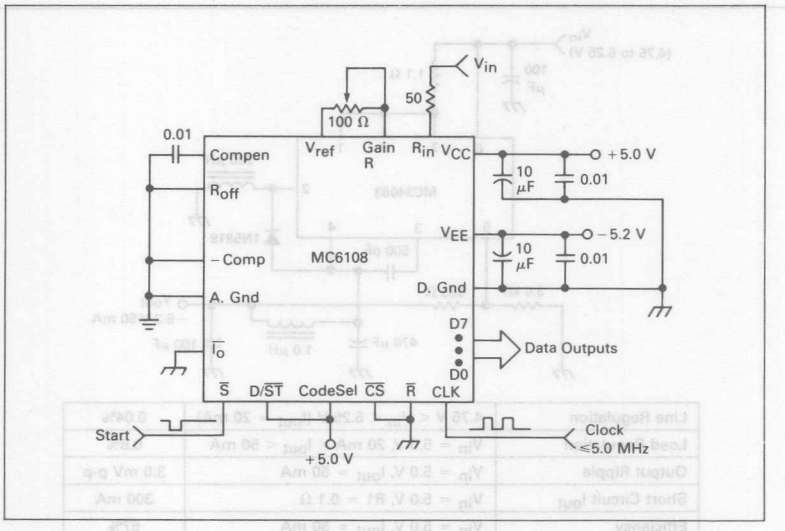
STAND-ALONE USE

Although the MC6108 was designed for use with microprocessors, it can be used in a stand-alone mode. The digital inputs may be controlled by other digital circuitry, or hard-wired in a simple application. Figure 17 shows a simple configuration whereby the MC6108 is permanently enabled, and each $\overline{S}$ input pulse provides new data at the outputs. Figure 18 shows a circuit whereby the MC6108 is continually self-updating the information into latches. The latches are necessary since in this mode of operation, the MC6108 data outputs are in the 3-state mode the majority of the time. The 430 Ω resistor and 68 pF capacitor provide a ≈60 ns delay from $\overline{CC}$'s falling edge to allow D0–D7 to stabilize, and to allow the setup time required by the SN74LS374 latches. The clock high time in this circuit must be ≥100 ns.

NEGATIVE VOLTAGE REGULATOR

In the cases where a negative power supply is not available — neither the −5.2 volts, nor a higher negative voltage from which to derive the −5.2 volts — the circuit of Figure 19 can be used to generate the −5.2 volts from the +5.0 volts supply. The PC board space required is small (≈2.0 in^2), and it can be located physically close to the MC6108. The MC34063 is a switching regulator, and in Figure 19 is configured in an inverting mode of operation. The regulator operating specifications are given in the Figure.

FIGURE 17 — STAND-ALONE OPERATION (CONTINUOUSLY ENABLED)



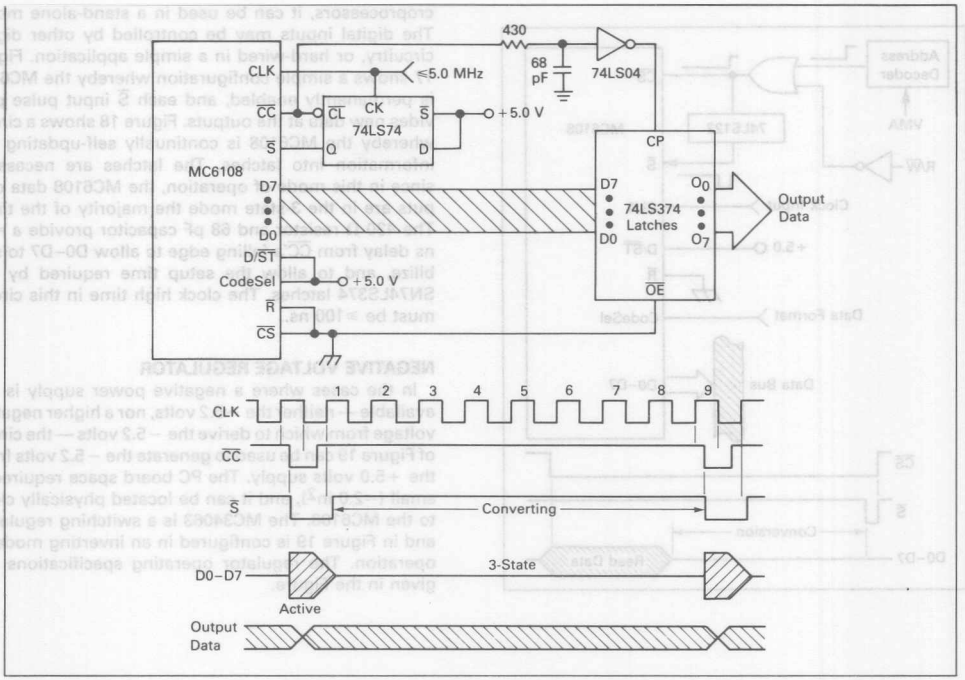
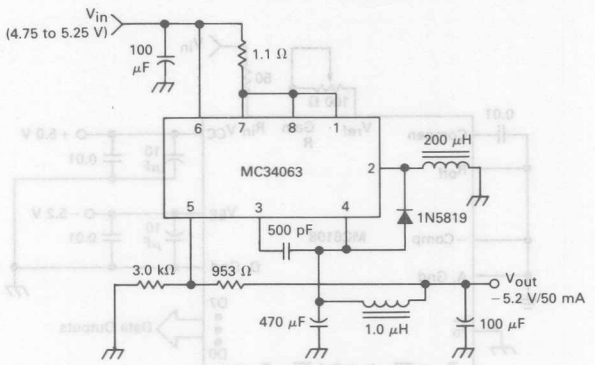


FIGURE 19 — −5.2 VOLTAGE REGULATOR



Line Regulation	4.75 V < V_{in} < 5.25 V (I_{out} = 20 mA)	0.04%
Load Regulation	V_{in} = 5.0 V, 20 mA < I_{out} < 50 mA	0.8%
Output Ripple	V_{in} = 5.0 V, I_{out} = 50 mA	3.0 mV p-p
Short Circuit I_{out}	V_{in} = 5.0 V, R1 = 0.1 Ω	300 mA
Efficiency	V_{in} = 5.0 V, I_{out} = 50 mA	57%

GLOSSARY

BANDGAP REFERENCE — A voltage reference circuit based on the predictable base-emitter voltage of a transistor. The silicon bandgap voltage of ≈1.2 volts is the basis for generating other voltages which are stable with time and temperature.

BIPOLAR INPUT — A mode of operation whereby the analog input (of an A-D), or output (of a DAC), includes both negative and positive values. Examples are −5 to +5 V, −2 to +8 V, etc.

BIPOLAR OFFSET ERROR — The difference between the actual and ideal locations of the 00_H to 01_H transition, where the ideal location is 1/2 LSB above the most negative input voltage.

BIPOLAR ZERO ERROR — The error (usually expressed in LSBs) of the input voltage location (of an A-D) of the $7F_H$ to 80_H transition. The ideal location is 1/2 LSB below zero volts in the case of an A-D set up for a symmetrical bipolar input (e.g., −5 to +5 V).

DAC CURRENT GAIN — The internal gain the DAC applies to the reference current to determine the full scale output current. The actual maximum current out of a DAC is one LSB less than the full scale current.

DIFFERENTIAL NON-LINEARITY — The maximum deviation in the actual step size (one transition level to another) from the ideal step size. The ideal step size is defined as the Full Scale Range divided by 2^n (n = number of bits). This error must be within ±1 LSB for proper operation.

FULL SCALE CURRENT or RANGE (ACTUAL) — The difference between the actual minimum and maximum end points of the analog input (of an A-D), or output (of a DAC).

FULL SCALE RANGE (IDEAL) — The difference between the actual minimum and maximum end points of the analog input (of an A-D), or output (of a DAC), plus one LSB.

GAIN ERROR — The difference between the actual and expected gain (end point to end point) of a data converter, with respect to the device's internal reference. The gain error is usually expressed in LSBs.

INTEGRAL NON-LINEARITY — The maximum error of an A-D, or DAC, transfer function from the ideal straight line connecting the analog end points. This parameter is sensitive to dynamics, and test conditions must be specified in order to be meaningful. This parameter is the best overall indicator of the device's performance.

LSB — Least Significant Bit. It is the lowest order bit of a binary code.

LINE REGULATION — The ability of a voltage regulator to maintain a certain output voltage as the input to the regulator is varied. The error is typically expressed as a percent of the nominal output voltage.

LOAD REGULATION — The ability of a voltage regulator to maintain a certain output voltage as the load current is varied. The error is typically expressed as a percent of the nominal output voltage.

MONOTONICITY — The characteristic of the transfer function whereby increasing the input code (of a DAC), or the input signal (of an A-D), results in the output never decreasing.

MSB — Most Significant Bit. It is the highest order bit of a binary code.

NATURAL BINARY CODE — A binary code whose normalized decimal value is defined by:

$$N = A_n 2^n + \ldots + A_3 2^3 + A_2 2^2 + A_1 2^1 + A_0 2^0$$

where each "A" coefficient has a value of 1 or 0. Typically, all zeroes corresponds to a zero input voltage of an A-D, and all ones corresponds to the most positive input voltage.

OFFSET BINARY CODE — Applicable only to bipolar input (or output) data converters, it is the same as Natural Binary, except that all zeroes corresponds to the most negative input voltage (of an A-D), while all ones corresponds to the most positive input.

POWER SUPPLY SENSITIVITY — The change in a data converter's performance with changes in the power supply voltage(s). This parameter is usually expressed in percent of full scale versus ΔV.

QUANTITIZATION ERROR — Also known as digitization error or uncertainty. It is the inherent error involved in digitizing an analog signal due to the finite number of steps at the digital output versus the infinite number of values at the analog input. This error is a minimum of ±1/2 LSB.

RESOLUTION — The smallest change which can be discerned by an A-D converter, or produced by a DAC. It is usually expressed as the number of bits, n, where the converter has 2^n possible states.

SAMPLING THEOREM — Also known as the Nyquist Theorem. It states that the sampling frequency of an A-D must be no less than 2x the highest frequency (of interest) of the analog signal to be digitized in order to preserve the information of that analog signal.

TWO'S COMPLEMENT CODE — A binary code applicable to bipolar operation, in which the positive and negative codes of the same analog magnitude sum to all zeroes, plus a carry. It is the same as Offset Binary Code, with the MSB inverted.

UNIPOLAR INPUT — A mode of operation whereby the analog input range (of an A-D), or output range (of a DAC), includes values of a single polarity. Examples are 0 to +10 V, 0 to −5 V, +2 to +8 V, etc.

UNIPOLAR OFFSET ERROR — The difference between the actual and ideal locations of the 00_H to 01_H transition, where the ideal location is 1/2 LSB above the most negative input voltage.

6

MOTOROLA

MC10318L9
MC10318L
MC10318CL7
MC10318CL6

Specifications and Applications Information

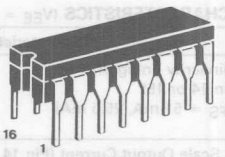
HIGH SPEED 8-BIT DIGITAL-TO-ANALOG CONVERTER

HIGH SPEED
8-BIT DIGITAL-TO-ANALOG CONVERTER

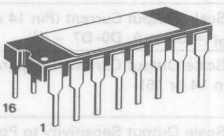
SILICON MONOLITHIC INTEGRATED CIRCUIT

The MC10318 (Series) is a high-speed D/A converter capable of data conversion rates in excess of 25 MHz. The digital inputs are compatible with MECL 10,000 Series Logic. Complementary current outputs provide up to 56 mA full scale capability. The MC10318 Series is available in 4 accuracy grades (over temperature) to meet the requirements of many applications, including: high-speed instrumentation and test equipment, storage oscilliscopes, display processing, radar systems, and digital video systems (broadcast and receiver applications).

- Fast Settling Time — 10 ns (Typ to ±0.19%)
- Four Accuracy Grades
  - — 9-Bit Linearity (±0.10%) — MC10318L9
  - — 8-Bit Linearity (±0.19%) — MC10318L
  - — 7-Bit Linearity (±0.39%) — MC10318CL7
  - — 6-Bit Linearity (±0.78%) — MC10318CL6
- Inputs MECL 10,000 Compatible
- Complementary Current Outputs
- Output Compliance: −1.3 V to +2.5 V
- Single MECL Supply: −5.2 V
- Standard 16-Pin Dual-In-Line Package
- Evaluation Kit MCK8DA Available

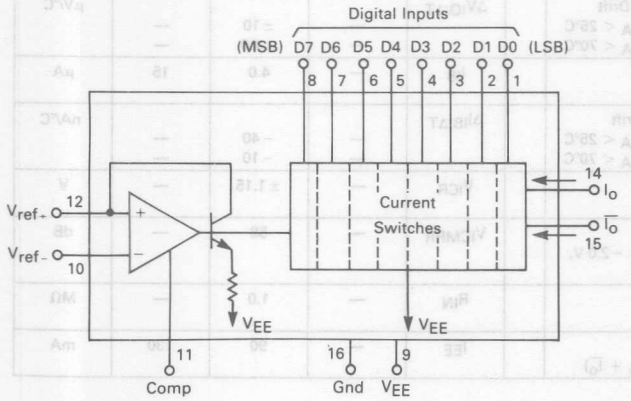


L SUFFIX
CERAMIC PACKAGE
CASE 620-10

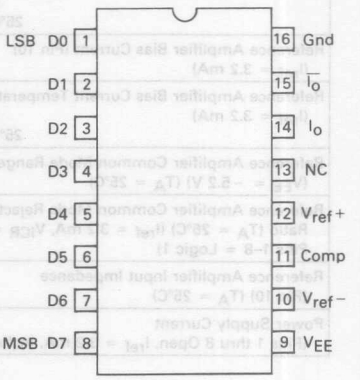


L SUFFIX
CERAMIC PACKAGE
CASE 690-13

BLOCK DIAGRAM



PIN CONNECTIONS
(TOP VIEW)



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{EE}	−6.0 to +0.5	Vdc
Digital Input Voltage	V_I	0 to V_{EE}	Vdc
Applied Output Voltage	V_O	+5.0 to V_{EE}	Vdc
Reference Current	$I_{ref}(12)$	5.0	mA
Output Current	I_{FS}	−75	mA
Reference Amplifier Input Range	V_{ref}	+0.5 to V_{EE}	Vdc
Reference Amplifier Differential Inputs	$V_{ref}(D)$	±5.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Junction Temperature Ceramic Package	T_J	+175	°C
Thermal Resistance, Junction to Ambient — Still Air	$R\theta_{JA}$	80	°C/W
Thermal Resistance, Junction to Ambient — With 500 LFPM	$R\theta_{JA}$	50	°C/W

DC CHARACTERISTICS (V_{EE} = −5.2 V, ±5% T_A = 0°C to +70°C after thermal equilibrium is reached.)

Characteristics	Fig.	Symbol	Min	Typ	Max	Unit
Nonlinearity (Integral) (Pin 14 or 15) (@ I_{FS} = 51 mA, 25.5 mA) — MC10318L9		—	—	—	±0.10	% FS
MC10318L		—	—	—	±0.19	
MC10318CL7		—	—	—	±0.39	
MC10318CL6		—	—	—	±0.78	
Zero Scale Output Current (Pin 14 or 15) (T_A = 25°C)	10	I_{ZS}	—	5.0	50	µA
Zero Scale Output Current Temperature Drift (Pin 14 or 15) 0 < T_A < 25°C		$I_{ZS}/\Delta T$	—	±17	—	nA/°C
25°C < T_A < 70°C			—	±2.0	—	
Full Scale Output Current (Pin 14 or 15) (I_{ref} = 3.2 mA, D0–D7 = 1)	10	I_{FS}	−46.00	−51.00	−56.00	mA
Full Scale Output Current Temperature Drift (Pin 14 or 15) 0 < T_A < 25°C		$\Delta I_{FS}/°C$	—	±50	—	ppm/°C
25°C < T_A < 70°C			—	±10	—	
Full Scale Output Sensitivity to Power Supply Variations (Pin 14 or 15) ($-4.94\ V < V_{EE} < -5.46\ V$) — MC10318L,9		I_{FSPSS}	—	±0.005	±0.02	%/%
MC10318CL6,7			—	±0.005	±0.04	
Full Scale Symmetry ($I_{FS} - \overline{I_{FS}}$)	10	I_{FSS}	—	±21	±100	µA
Output Voltage Compliance (Pin 14 or 15) Full Scale Current Change ≤ ½ LSB (Specified Nonlinearity) (T_A = 25°C)		V_{OC}	−1.3	—	+2.5	V
Output Resistance (Pin 14 or 15) (T_A = 25°C)	12	R_O	—	69	—	kΩ
Reference Amplifier Offset Voltage (T_A = 25°C)		V_{IO}	—	±3.2	—	mV
Reference Amplifier Offset Voltage Temperature Drift 0 < T_A < 25°C		$\Delta V_{IO}/\Delta T$	—	±10	—	µV/°C
25°C < T_A < 70°C			—	±4.0	—	
Reference Amplifier Bias Current (Pin 10) (I_{ref} = 3.2 mA)		I_{IB}	—	4.0	15	µA
Reference Amplifier Bias Current Temperature Drift (I_{ref} = 3.2 mA) 0 < T_A < 25°C		$\Delta I_{IB}/\Delta T$	—	−40	—	nA/°C
25°C < T_A < 70°C			—	−10	—	
Reference Amplifier Common Mode Range (V_{EE} = −5.2 V) (T_A = 25°C)		V_{ICR}	—	±1.15	—	V
Reference Amplifier Common Mode Rejection Ratio (T_A = 25°C) (I_{ref} = 3.2 mA, V_{ICR} = 0 to −2.0 V, Pins 1–8 = Logic 1)		V_{ICMRR}	—	58	—	dB
Reference Amplifier Input Impedance (Pin 10) (T_A = 25°C)		R_{IN}	—	1.0	—	MΩ
Power Supply Current (Pins 1 thru 8 Open, I_{ref} = 3.2 mA, Includes $I_O + \overline{I_O}$)		I_{EE}	—	90	130	mA

AC CHARACTERISTICS (T_A = 25°C, V_{EE} = −5.2 V, ±5%)

Characteristics	Fig.	Symbol	Min	Typ	Max	Unit
Feedthrough Current — All Bits Off	9	I_{FC}				μA p-p
f = 10 kHz			—	2.0	—	
f = 100 kHz			—	18	—	
Distortion — (@ I_O) (Sinewave applied to reference amplifier Input, D0–D7 = Logic 1)						%
C = 0.01 μF, f = 20 kHz		THD	—	1.0	—	
C = 0.01 μF, f = 65 kHz		THD	—	5.0	—	
C = 0.001 μF, f = 340 kHz		THD	—	1.0	—	
C = 0.001 μF, f = 600 kHz		THD	—	2.0	—	
C = 240 pF, f = 600 kHz		THD	—	0.8	—	
Reference Amplifier Slew Rate (Step change at Pin 10, all bits on)	13					mA/μs
C = 0.01 μF			—	0.5	—	
C = 0.001 μF			—	5.0	—	
C = 240 pF			—	20	—	
Settling Time (to ±0.19% of Full Scale)	1,22	t_s				ns
1 LSB Change			—	7.0	—	
All Bits Switched			—	10	—	
Propagation Delay	2	t_p	—	5.0	—	ns
Output Glitch Energy (with De-Skewing Capacitors) (Input Change: 01111111 ⟷ 10000000)			—	50	—	LSB·ns
Glitch Duration			—	5.0	—	ns

DIGITAL INPUT VOLTAGE LEVELS				
Volts (See Note)				
T_A	V_{IH}max	V_{IHA}min	V_{ILA}max	V_{IL}min
0°C	−0.845	−1.151	−1.516	−1.868
25°C	−0.810	−1.105	−1.505	−1.850
70°C	−0.727	−1.052	−1.480	−1.830

FUNCTIONAL PIN DESCRIPTION

D0–D7 (Pins 1-8) The eight ECL digital inputs compatible with MECL 10,000 series devices. Logic "0" is nominally −1.8 V, and Logic "1" is nominally −0.9 V.

V_{ref-} (Pin 10) The high impendance input of the reference amplifier. This input is normally grounded, but may be used for ac applications involving modulation, digitally controlled gain, etc. Normal operating range is from ground to V_{EE} + 2.9 V (nominally −2.3 V).

V_{ref+} (Pin 12) The noninverting input of the reference amplifier. The inverted output of the reference amplifier is internally fed back to this input, thus causing it to track Pin 10. A nominal 3.2 mA is to be supplied to this pin from an external (stable and noise free) voltage source and current setting resistor.

Comp. (Pin 11) A nominal 0.01 μF capacitor is connected to this pin and to ground to stabilize the reference amplifier. Lower values of capacitor may be used if a good PC board layout is used, where frequencies higher than 10 kHz are applied to the reference amplifier.

I_O, $\overline{I_O}$ (Pins 14,15) The complementary current outputs. Current flow is into the DAC and varies linearily with I_{ref} and the digital input code. I_{out} increases as the digital input increases. Output compliance range is −1.3 V to +2.5 V.

V_{EE} (Pin 9) The power supply pin. V_{EE} is nominal −5.2 V, ±5%.

Gnd (Pin 16) The ground pin. This line should be as noise-free as possible in order to obtain a noise-free output.

NOTE: V_{EE} = −5.2 V, ±5% Inputs are MECL 10,000 compatible within the temperature and power supply ranges listed. See MECL System Design Handbook for further details. See Fig. 19 in this data sheet.

FIGURE 1 — SETTLING TIME

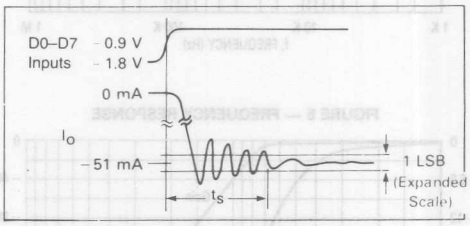
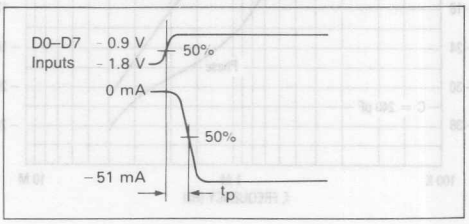


FIGURE 2 — PROPAGATION DELAY



REFERENCE AMPLIFIER RESPONSE

Inverting Input (V_{ref-})
Test Circuit of Fig. 14

FIGURE 3 — FREQUENCY RESPONSE

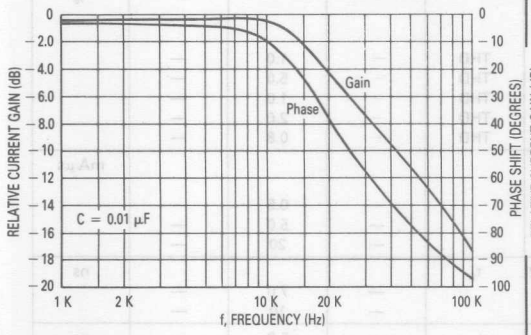


FIGURE 4 — FREQUENCY RESPONSE

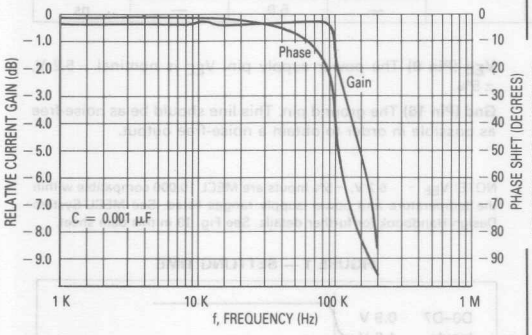
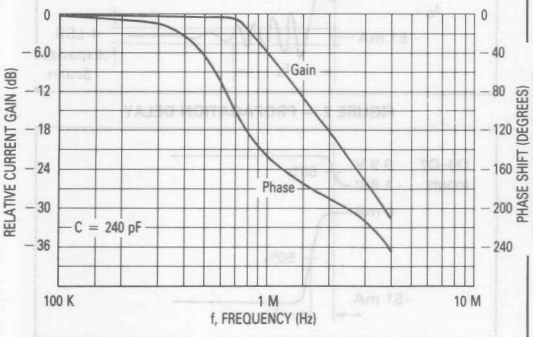


FIGURE 5 — FREQUENCY RESPONSE



Noninverting Input (V_{ref+})
Test Circuit of Fig. 11

FIGURE 6 — FREQUENCY RESPONSE

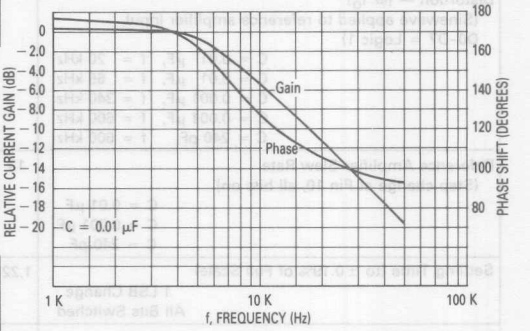


FIGURE 7 — FREQUENCY RESPONSE

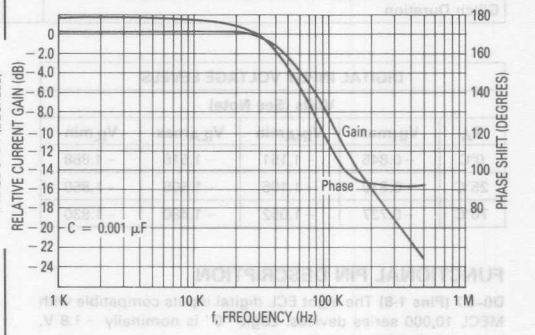
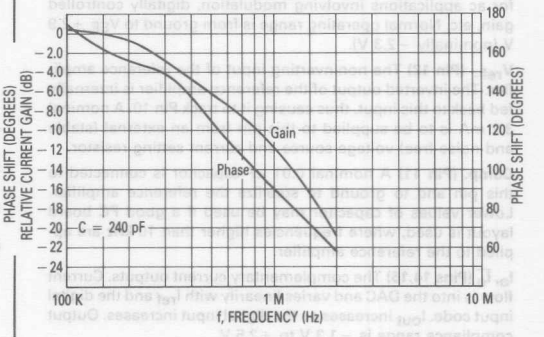


FIGURE 8 — FREQUENCY RESPONSE



TEST CIRCUITS

FIGURE 9 — FEEDTHROUGH MEASUREMENT

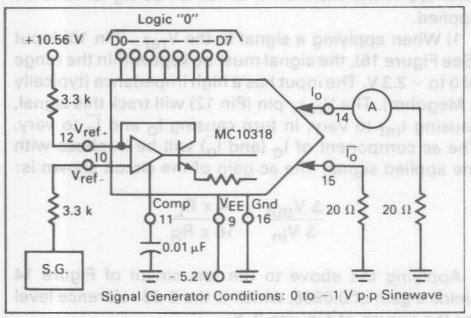


FIGURE 10 — ZERO/FULL SCALE CURRENT

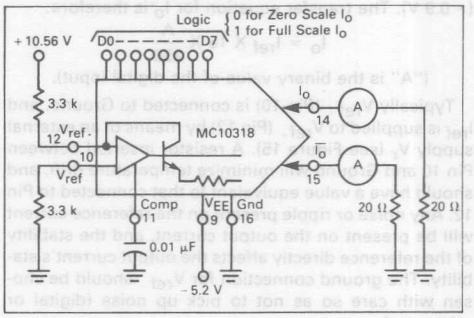
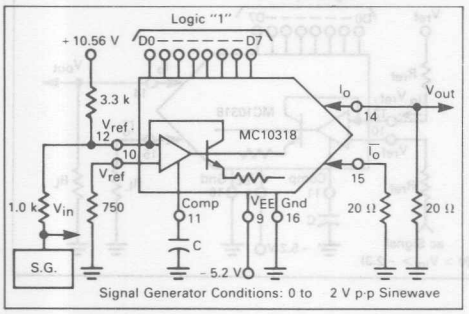


FIGURE 11 — GAIN/PHASE MEASUREMENT



Reference dB Level: See Text

See Figures 6-8

FIGURE 12 — OUTPUT RESISTANCE

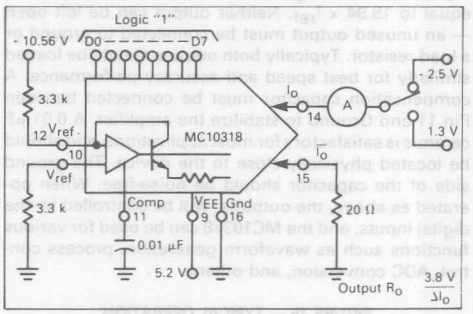


FIGURE 13 — REFERENCE AMPLIFIER SLEW RATE

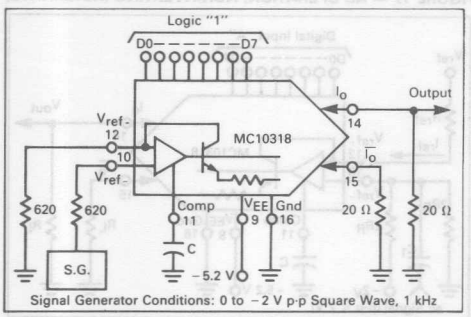
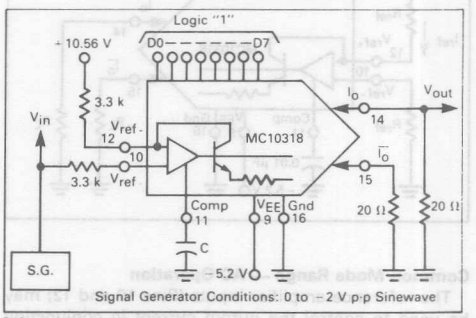


FIGURE 14 — GAIN/PHASE MEASUREMENT



Reference dB Level: See Text.

See Figures 3-5

6

6

Typical DAC Operation

The MC10318 is designed to be operated with an I_{ref} (Pin 12) of 3.2 mA, resulting in a full scale output current (I_O) of 51 mA when D0 through D7 are at a Logical "1" (−0.9 V). The transfer equation for I_O is therefore:

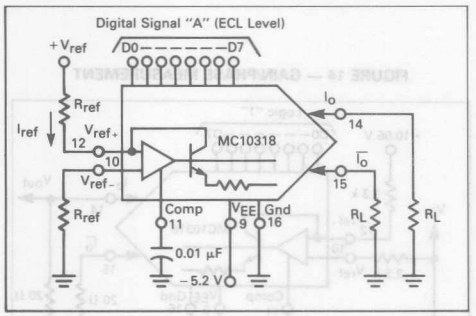
$$I_O = I_{ref} \times 16 \times \frac{A}{256}$$

("A" is the binary value of the digital input).

Typically V_{ref-} (Pin 10) is connected to Ground, and I_{ref} is supplied to V_{ref+} (Pin 12) by means of an external supply V_r (see Figure 15). A resistor inserted between Pin 10 and Ground will minimize temperature drift, and should have a value equivalent to that connected to Pin 12. Any noise or ripple present on the reference current will be present on the output current, and the stability of the reference directly affects the output current's stability. The ground connection for V_{ref-} should be chosen with care so as not to pick up noise (digital or otherwise).

The complementary outputs (I_O and $\overline{I_O}$) are high impedance current sources having a compliance range of 3.8 V (−1.3 to +2.5 V). I_O increases with increasing digital input, while $\overline{I_O}$ decreases. Their sum is a constant equal to 15.94 x I_{ref}. Neither output can be left open — an unused output must be connected to ground or a load resistor. Typically both outputs should be loaded similarly for best speed and accuracy performance. A compensation capacitor must be connected between Pin 11 and Ground to stabilize the amplifier. A 0.01 μF ceramic is satisfactory for most applications, and should be located physically close to the device. The ground side of the capacitor should be noise-free. When operated as above, the output(s) will be controlled by the digital inputs, and the MC10318 can be used for various functions such as waveform generation, process control, ADC conversion, and others.

FIGURE 15 — TYPICAL OPERATION



Common Mode Range — AC Operation

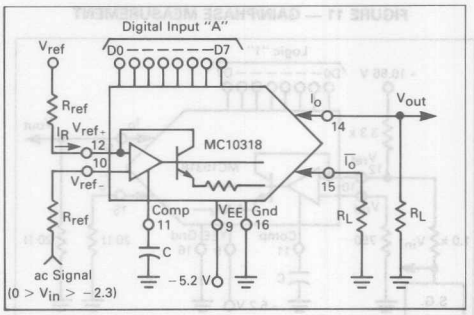
The reference amplifier inputs (Pins 10 and 12) may be used to control the output current in conjunction with the digital inputs for applications such as digitally controlled gain of an ac signal, digitally controlled amplitude modulation, and others. Either the positive or negative input of the reference amplifier may be used, depending on the application. There are, however, differences in the manner in which an ac signal is to be applied.

1) When applying a signal to the V_{ref-} (Pin 10) input (See Figure 16), the signal must be kept within the range of 0 to −2.3 V. The input has a high impedance (typically 1 Megohm). The V_{ref+} pin (Pin 12) will track this signal, causing I_{ref} to vary, in turn causing I_O and $\overline{I_O}$ to vary. The ac component of I_O (and $\overline{I_O}$) will be in phase with the applied signal. The ac gain of the circuit shown is:

$$\frac{\Delta V_{out}}{\Delta V_{in}} = \frac{A \times R_L}{16 \times R_R}$$

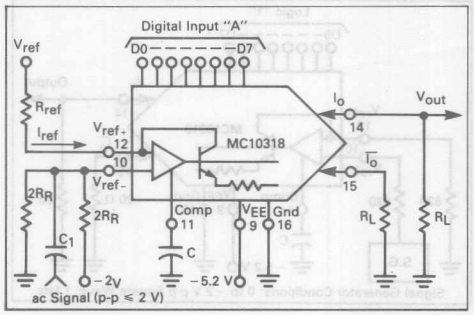
Applying the above to the test circuit of Figure 14 yields a gain of 0.0966, which is the 0 dB reference level for the curves of Figures 3–5.

FIGURE 16 — AC OPERATION, NONINVERTING



If the peak values of the applied ac signal cannot be kept within the above mentioned voltage range, an alternate circuit is shown in Figure 17.

FIGURE 17 — AC OPERATION, NONINVERTING (ALTERNATE)



The compensation capacitor (Pin 11) of Figures 16 and 17 is to be nominally 0.01 μF for best overall stability. If frequencies higher than 10 kHz are to be applied to the reference input, a smaller value capacitor will be necessary as indicated by Figures 3–5. However, greater care will be necessary in the breadboarding and PC layout to prevent instabilities caused by unintended feedback paths.

2) When applying a signal to the V_{ref+} (Pin 12) input (see Figure 18), the effect is a direct modulation of the reference current supplied by V_{ref}. Pin 12 is a virtual ground, and therefore the current I_{ref} is equal to:

$$I_{ref} = \frac{V_{ref}}{R_{ref}} + \frac{V_i}{R_i}$$

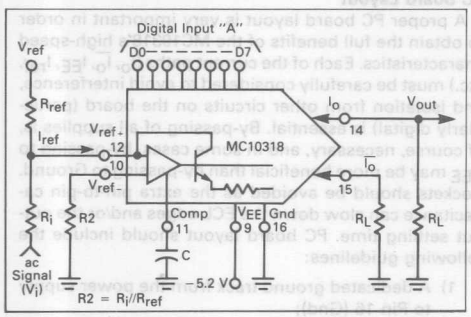
I_o and $\overline{I_o}$ will vary with the reference current, but the ac component will be 180° out of phase with the applied signal. The ac gain of the circuit shown is:

$$\frac{\Delta V_{out}}{\Delta V_i} = \frac{-A \times R_L}{16 \times R_i}$$

Applying the above to the test circuit of Figure 11 yields a gain of −0.3188, which is the 0 dB reference level for the curves of Figures 6–8.

The reference current I_{ref} must always flow **into** Pin 12, requiring that the values of V_{ref}, R_{ref}, R_i, and V_i be chosen so as to guarantee this.

FIGURE 18 — AC OPERATION, INVERTING

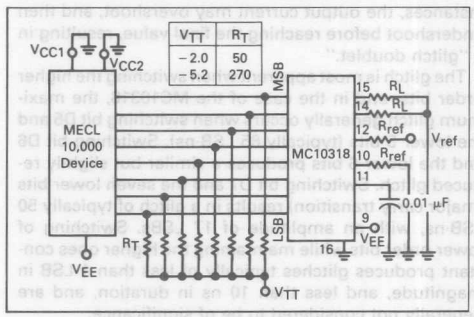


The compensation capacitor (Pin 11) of Figure 18 is to be nominally 0.01 μF for best overall stability. If frequencies higher than 4 kHz are to be applied, a smaller value capacitor will be necessary as indicated by Figures 6–8. However, greater care will be necessary in the breadboarding and PC layout to prevent instabilities caused by unintended feedback paths.

DIGITAL INTERFACE

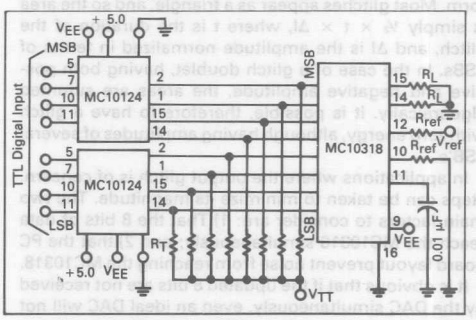
The digital inputs (Pins 1–8) are compatible with MECL 10,000 series devices over the temperature and V_{EE} range listed on page 3. Standard MECL 10,000 design guidelines apply, and should be implemented. Maximum speed response requires careful PC board layout and choice of components. See Motorola's MECL System Design Handbook for a complete explanation of specifications and characteristics. Figure 19 shows a typical ECL interconnection with recommended values for optimum speed performance. Other values of R_T and V_{TT} may be used, but at a slight increase in overall propagation delay. Unused inputs should not be left open, but should be connected to a Logic 0 (−1.8 V), or a Logic 1 (−0.9 V). Resistors R_T should be connected at the receiving end of the interconnection, i.e. physically located adjacent to the MC10318 inputs, for best speed performance.

FIGURE 19 — STANDARD MECL INTERFACE



Interfacing a TTL system to the MC10318 is easily accomplished by the use of two MC10124 devices (Figure 20).

FIGURE 20 — TTL INTERFACE



OUTPUT CHARACTERISTICS

The MC10318 DAC has been designed specifically for high-speed operation by incorporating ECL structured inputs, bit switching circuits which are small in size and

simple in operation, and high-current complementary outputs (which permits current steering rather than on-off switching). In this manner, very short propagation delays and settling times are possible.

Output Glitch

All DAC's will produce a glitch at the output when various bits are switched in opposite directions, due to differences in transition times of the switching transistors. During the switching period, typically the output current will momentarily seek a value other than the desired final value, and then return to and settle at the final value. This glitch can be several LSBs in magnitude, but of a very short duration (5–6 ns). In some instances, the output current may overshoot, and then undershoot before reaching the final value, resulting in a "glitch doublet."

The glitch is most apparent when switching the higher order bits, and in the case of the MC10318, the maximum glitch generally occurs when switching bit D5 and the lower 5 bits (typically 85 LSB·ns). Switching bit D6 and the lower 6 bits produces a similar but slightly reduced glitch. Switching bit D7 and the seven lower bits (major carry transition) results in a glitch of typically 50 LSB·ns, with an amplitude of 17 LSBs. Switching of lower order bits while maintaining the higher ones constant produces glitches typically of less than 1 LSB in magnitude, and less than 10 ns in duration, and are generally not considered to be of significance.

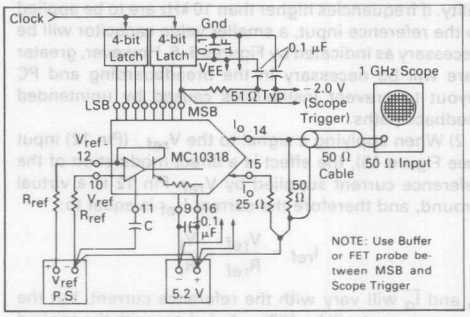
Glitches can be removed from the output by filtering, or by using a sample-and-hold circuit on the output, or by using de-skewing capacitors on the higher order bits. See Fig. 31.

Output glitch is generally specified in terms of glitch energy, which is the area under the curve of the waveform. Most glitches appear as a triangle, and so the area is simply ½ × t × ΔI, where t is the duration of the glitch, and ΔI is the amplitude normalized in terms of LSBs. In the case of a glitch doublet, having both positive and negative amplitude, the areas are summed algebraically. It is possible, therefore to have a glitch with zero energy, although having amplitudes of several LSB's.

In applications where the output glitch is of concern, steps can be taken to minimize its magnitude. The two main factors to consider are: 1) That the 8 bits of data reach the MC10318 simultaneously; and 2) that the PC board layout prevent noise from reaching the MC10318.

It is obvious that if the updated 8 bits are not received by the DAC simultaneously, even an ideal DAC will not produce an ideal waveform. Where simultaneous transmission by the sending device(s) cannot be guaranteed (such as two cascaded counters), latches should be used ahead of the MC10318. The latches should then be clocked after their inputs have settled. Suggested latches are the MC10133/MC10153/MC10168 at the ECL level, and the SN74LS273 at the TTL level.

FIGURE 21 — PRECISION HIGH-SPEED MEASUREMENTS



Nonlinearity

Integral nonlinearity has been specified, rather than differential nonlinearity, as this is a better indicator of the maximum error to be expected. Integral nonlinearity is measured by comparing the **actual** output (at each digital value) with the expected ideal value. The expected values lie along a straight line between zero and the full scale output current. The MC10318 series will not differ from the **ideal** value by more than the specified nonlinearity.

PC Board Layout

A proper PC board layout is very important in order to obtain the full benefits of the MC10318's high-speed characteristics. Each of the current paths (I_O, $\overline{I_O}$, I_{EE}, I_{ref}, etc.) must be carefully considered to avoid interference, and isolation from other circuits on the board (particularly digital) is essential. By-passing of all supplies is, of course, necessary, and in some cases, by-passing to V_{EE} may be more beneficial than by-passing to Ground. Sockets should be avoided as the extra pin-to-pin capacitance can slow down the ECL edges and/or the output settling time. PC board layout should include the following guidelines:

1) A dedicated ground track from the power supply to Pin 16 (Gnd);
2) A single dedicated ground track from the power supply to the **two** load resistors associated with I_O and $\overline{I_O}$ — this results in a constant dc current in this track;
3) A separate ground for the circuitry associated with V_{ref+}, V_{ref-}, and Comp (Pins 10–12). Any noise on this ground will feed through the reference amplifier and show up on the output;
4) The compensation capacitor must be physically adjacent to Pin 11;
5) Bypass V_{EE} (Pin 9) with a 0.1 µF to the ground line feeding the load resistors;
6) Provide proper terminations at the inputs — the suggested values for R_T and V_{TT} will provide best speed response;

7) Bypass V_{TT} to V_{EE} **and** to Ground with 0.1 μF capacitors;
8) If the power supplies are not on the same PC board with the MC10318, bypass V_{EE} and V_{TT} to Ground with (minimum) 10 μF and 0.1 μF where the supply voltages enter the PC board;
9) Use of a ground plane is mandatory in all high speed applications;
10) Keep all TTL circuitry tracks separate from the MC10318 by means of ground tracks and/or ground planes.

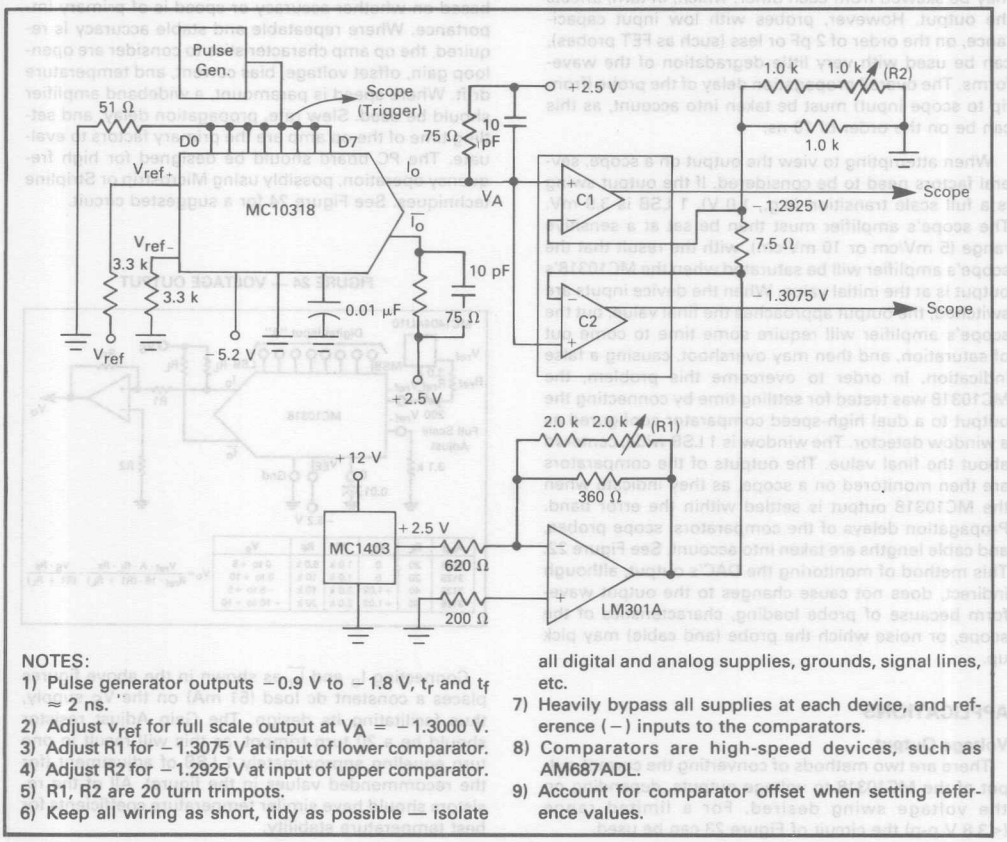
Many of the above points have to do with isolating the device from all other circuitry, since most applications involve using the MC10318 (which is 50% analog) in a (noisy) digital circuit. If the output voltage swing is typically 1 volt, then 1 LSB is approximately 4 mV. Since TTL circuitry can easily generate 50 mV noise on the ground line, the need for isolation is apparent.

The above points are not the only ones to be considered by the designer, as each application will have its own individual additional requirements.

Propagation Delay

The propagation delay is measured from the 50% point of the input transition to the 50% point of the output transition. Since the typical propagation delay is on the order of 5 ns, see Figure 21 and the information in Settling Time if this parameter is to be measured. Switching 1 LSB or all of the bits simultaneously produces no significant difference in propagation delay.

FIGURE 22 — SETTLING TIME MEASUREMENT



NOTES:
1) Pulse generator outputs −0.9 V to −1.8 V, t_r and t_f ≈ 2 ns.
2) Adjust v_{ref} for full scale output at V_A = −1.3000 V.
3) Adjust R1 for −1.3075 V at input of lower comparator.
4) Adjust R2 for −1.2925 V at input of upper comparator.
5) R1, R2 are 20 turn trimpots.
6) Keep all wiring as short, tidy as possible — isolate all digital and analog supplies, grounds, signal lines, etc.
7) Heavily bypass all supplies at each device, and reference (−) inputs to the comparators.
8) Comparators are high-speed devices, such as AM687ADL.
9) Account for comparator offset when setting reference values.

Settling Time

The settling time is defined as the time from the 50% point of the input transition to the point at which the output enters into **and** stays within ± ½LSB (the error band) of the final value. Minimum settling time occurs when the output enters the error band at the maximum slew rate, and then settles out within the band. In actuality, however, the output's slew rate will lessen prior to entering the error band, and then may exit and enter the band once or twice as it settles to its final value. The settling time is determined by the last time the output enters the error band. See Figure 1.

When testing for settling time, the measurement technique used will have an effect on the result. Simply connecting scope probes to an input and output is generally not satisfactory due to the capacitive loading (typically 10–20 pF) of the probes. The rise (fall) time of an ECL input can be significantly increased by such a probe, with the result that the inputs of the MC10318 may be skewed from each other, which, in turn, affects the output. However, probes with low input capacitance, on the order of 2 pF or less (such as FET probes), can be used with very little degradation of the waveforms. The overall propagation delay of the probe (from tip to scope input) must be taken into account, as this can be on the order of 10 ns.

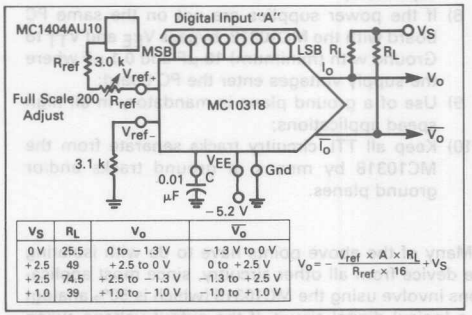
When attempting to view the output on a scope, several factors need to be considered. If the output swing is a full scale transition (e.g., 1.0 V), 1 LSB is 3.9 mV. The scope's amplifier must then be set at a sensitive range (5 mV/cm or 10 mV/cm), with the result that the scope's amplifier will be saturated when the MC10318's output is at the initial value. When the device inputs are switched, the output approaches the final value, but the scope's amplifier will require some time to come out of saturation, and then may overshoot, causing a false indication. In order to overcome this problem, the MC10318 was tested for settling time by connecting the output to a dual high-speed comparator configured as a window detector. The window is 1 LSB wide, centered about the final value. The outputs of the comparators are then monitored on a scope, as they indicate when the MC10318 output is settled within the error band. Propagation delays of the comparators, scope probes, and cable lengths are taken into account. See Figure 22. This method of monitoring the DAC's output, although indirect, does not cause changes to the output waveform because of probe loading, characteristics of the scope, or noise which the probe (and cable) may pick up.

APPLICATIONS

Voltage Output

There are two methods of converting the current output of the MC10318 to voltage outputs, depending on the voltage swing desired. For a limited range (<3.8 V p-p) the circuit of Figure 23 can be used.

FIGURE 23 — VOLTAGE OUTPUT

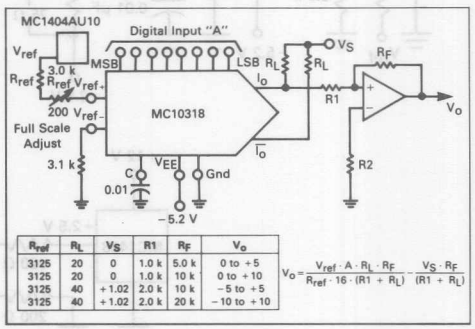


V_S	R_L	V_o	$\overline{V_o}$
0 V	25.5	0 to −1.3 V	−1.3 V to 0 V
+2.5	49	+2.5 to 0 V	0 to +2.5 V
+2.5	74.5	+2.5 to −1.3 V	−1.3 to +2.5 V
+1.0	39	+1.0 to −1.0 V	−1.0 to +1.0 V

$$V_o = -\frac{V_{ref} \times A \times R_L}{R_{ref} \times 16} + V_S$$

Where a larger voltage swing is required, an op amp is required at the output. The choice of op amp will be based on whether accuracy or speed is of primary importance. Where repeatable and stable accuracy is required, the op amp characteristics to consider are open-loop gain, offset voltage, bias current, and temperature drift. Where speed is paramount, a wideband amplifier should be used. Slew rate, propagation delay, and settling time of the op amp are the primary factors to evaluate. The PC board should be designed for high frequency operation, possibly using Microstrip or Stripline techniques. See Figure 24 for a suggested circuit.

FIGURE 24 — VOLTAGE OUTPUT



R_{ref}	R_L	V_S	R1	R_F	V_o
3125	20	0	1.0 k	5.0 k	0 to +5
3125	20	0	1.0 k	10 k	0 to +10
3125	40	+1.02	2.0 k	10 k	−5 to +5
3125	40	+1.02	2.0 k	20 k	−10 to +10

$$V_o = \frac{V_{ref} \cdot A \cdot R_L \cdot R_F}{R_{ref} \cdot 16 \cdot (R1 + R_L)} \cdot \frac{V_S \cdot R_F}{(R1 + R_L)}$$

Connecting I_o and $\overline{I_o}$ as shown in the above figures places a constant dc load (51 mA) on the V_S supply, thus facilitating its design. The Gain Adjust resistor should be a 20 turn trimpot, as this will result in one turn equaling approximately 1 LSB of adjustment (for the recommended values in the figure). All of the resistors should have similar temperature coefficients for best temperature stability.

WAVEFORM GENERATION

FIGURE 25 — SAWTOOTH GENERATOR

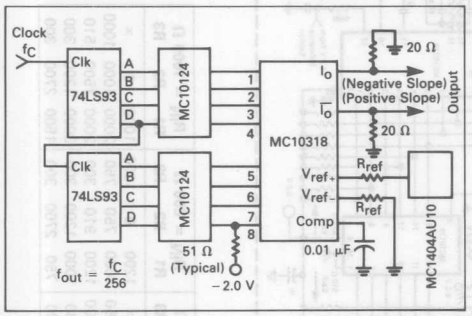


FIGURE 26 — TRIANGLE GENERATOR

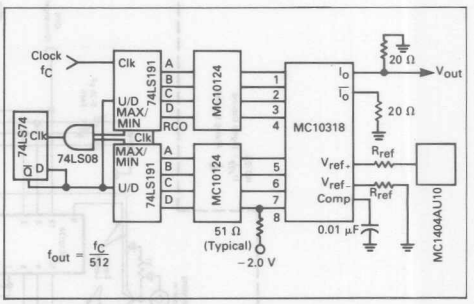
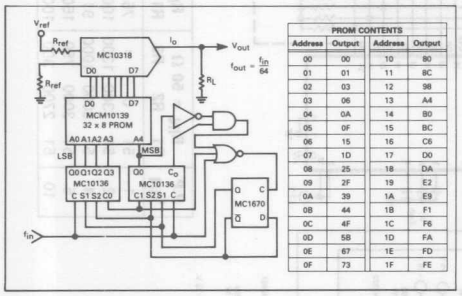


FIGURE 27 — SINEWAVE GENERATOR



PROM CONTENTS			
Address	Output	Address	Output
00	00	10	80
01	01	11	8C
02	03	12	98
03	06	13	A4
04	0A	14	B0
05	0F	15	BC
06	15	16	C6
07	1D	17	D0
08	25	18	DA
09	2F	19	E2
0A	39	1A	E9
0B	44	1B	F1
0C	4F	1C	F6
0D	5B	1D	FA
0E	67	1E	FD
0F	73	1F	FE

FIGURE 28 — OUTPUT CONNECTED TO 75 Ω LINE

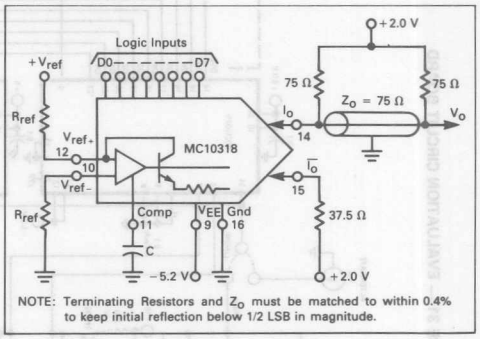


FIGURE 29 — OUTPUT CONNECTED TO 50 Ω LINE

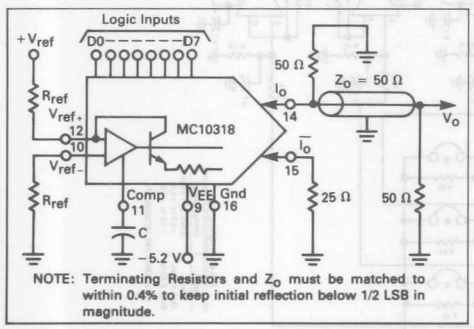
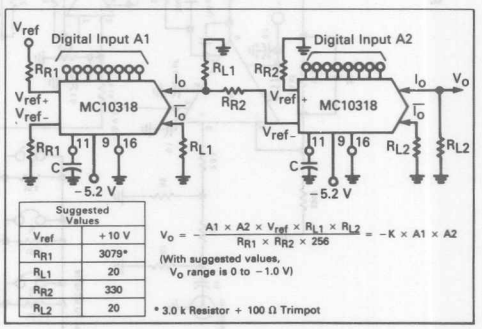


FIGURE 30 — DIGITAL MULTIPLICATION



Suggested Values	
Vref	+10 V
RR1	3079*
RL1	20
RR2	330
RL2	20

NOTES:

1) When generating waveforms at low frequencies, filtering the output is recommended to smooth out the steps.

2) In many applications, bipolar voltage output may be obtained by monitoring the differential voltage at Pins 14 and 15 (with equal load resistors).

3) When connecting the outputs to transmission lines (See Figures 28 and 29), proper transmission line theory and techniques must be used for optimum performance.

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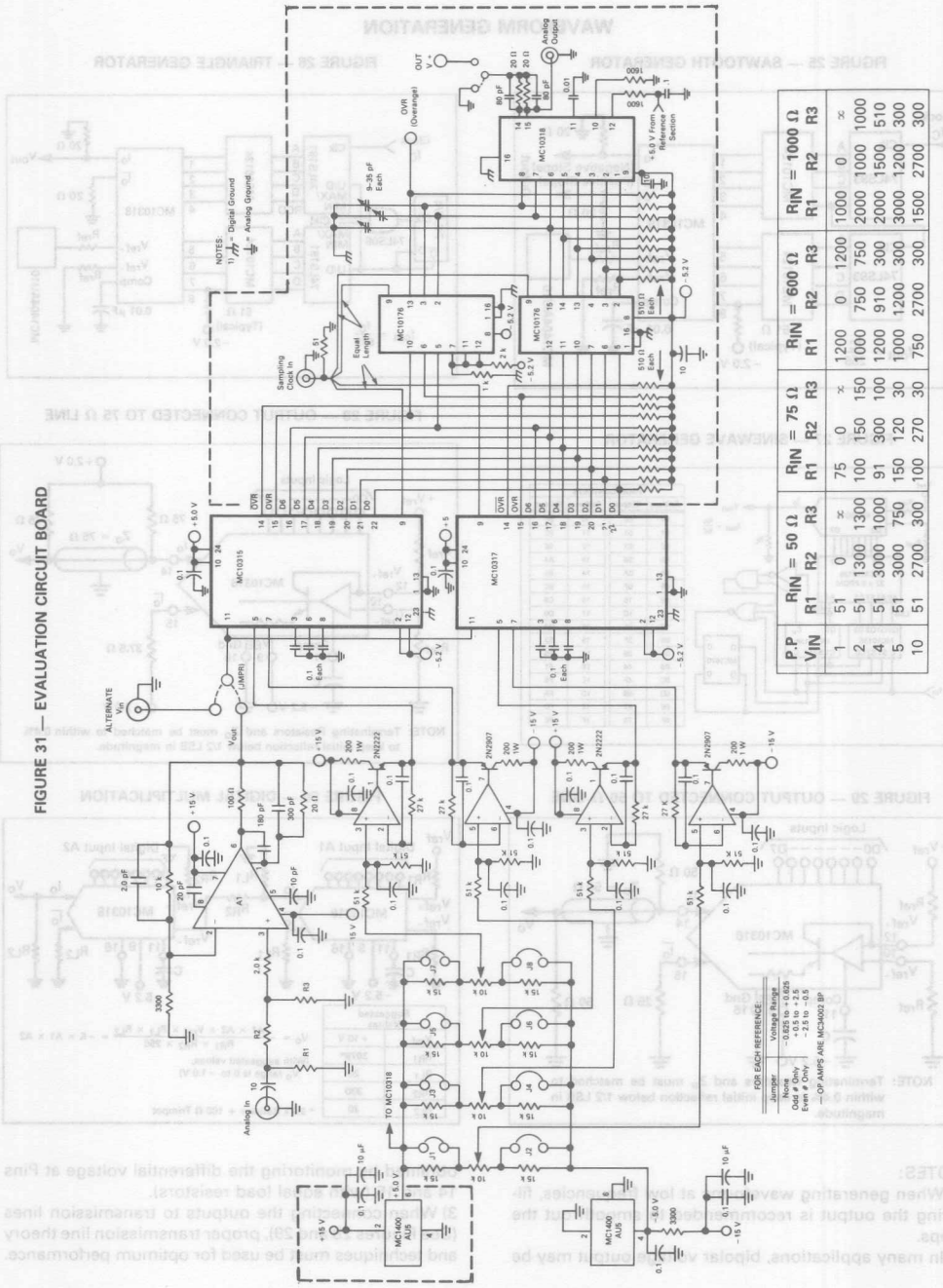


FIGURE 31 — EVALUATION CIRCUIT BOARD

P-P V_{IN}	R_{IN} = 50 Ω R1	R2	R3	R_{IN} = 75 Ω R1	R2	R3	R_{IN} = 600 Ω R1	R2	R3	R_{IN} = 1000 Ω R1	R2	R3
1	51	0	∞	75	0	∞	1200	0	1200	1000	0	∞
2	51	1300	1300	100	150	150	1000	750	750	2000	1000	1000
4	51	3000	1000	91	300	100	1200	910	300	2000	1500	510
5	51	3000	750	150	120	30	1000	1200	300	3000	1200	300
10	51	2700	300	100	270	30	750	2700	300	1500	2700	300

EVALUATION BOARD FOR HIGH SPEED TESTING

Introduction

In order to facilitate evaluation of the MC10318 DAC, a PC board layout has been developed providing the appropriate signal levels and timing requirements. The board is designed to simultaneously evaluate the MC10315 and the MC10317 flash ADC's in conjunction with the MC10318 DAC, and the system is capable of passing video speed signals at sampling rates of up to 15 MHz. However, the MC10318 may be evaluated alone by installing only the appropriate components. The board may be purchased from Motorola (blank), or the user may make his own from the artwork shown on Figures 33 and 34.

Board Specifications

Power supply requirements: +15 V @ 100 mA.
− 15 V @ 120 mA.
−5.2 V @ 550 mA.
+5.0 V @ 300 mA.

Sampling clock: V_{IH} = −0.9 V, V_{IL} = −1.8 V (ECL levels) terminated with 50 ohms, 15 MHz max.
Analog Input level: Selectable, see chart.
Analog Input Impedance: Selectable, see chart.
Output level: 0 to −1.0 V, user alterable.
Digital Input levels: (When ADC converters are not included) V_{IH} = −0.9 V, V_{IL} = −1.8 V (ECL levels).

Operation

The power supplies should be connected as shown in Figure 32. The leads should be short and direct.

The CLK Input (necessary if the ADC converters and/or the latches are used) uses a BNC connector, and is terminated with 50 ohms to ground.

The Analog Input level (if the ADC converters are installed) depends on the input resistors selected (see chart). The output of the buffer amplifier should produce a maximum 4 V p-p signal, or an amplitude equal to the references (user adjustable).

The Analog Output is 0 to −1.0 V, corresponding to a digital input (to the MC10318) of FF and 00 respectively. Output impedance is normally 20 ohms, but may be varied by the user (see previous text).

Options

Input Signal — The p-p voltage level of the analog input signal (when using the ADC converters) is accommodated by selection of the input resistors from the chart (see schematic).

ALT IN — The analog signal may be applied directly to the ADC converters (by-passing the on-board amplifier) by applying the input signal to this connector, and relocating the jumper adjacent to the ALT IN connector. The signal source must be capable of driving 2.5 k ohms in parallel with approx. 140 pF.

V+ OUT — A pullup voltage (max. +2.5 V) may be applied to this connector in order to increase the output voltage swing. See the APPLICATIONS section of this data sheet. The 20 ohm load resistors may then be changed to other values. The jumper adjacent to the A OUT connector must be relocated.

Evaluating the MC10318 only — Only those components within the dotted line on the schematic are required. The digital inputs (ECL level) are to be applied to a connector strip located in pins 15–22 of the MC10317 position. +15 V and −5.2 V supplies are required. The latches transfer the information on the rising edge of the clock.

Video Testing

The above described printed circuit board has been tested, with a standard video test signal, for differential phase and differential gain (40 IRE sub-carrier on a 100 IRE ramp, sampled at 14.3 MHz) with results of 1% gain error and 2° phase error. The signal was obtained from a Tektronix 147A video test generator, applied to the ALT IN connector. The output (of the MC10318) was configured into a 75 ohm output impedance, and applied to a vector scope.

Tests conducted with the Evaluation Board in a video system (video camera and a TV monitor) showed no visible degradation of picture quality (at 8 bits resolution). The board provides an easy means of testing picture quality at reduced number of bits, or for conducting any test on a digitized video signal.

FIGURE 32 — COMPONENT LOCATION AND EXTERNAL CONNECTIONS

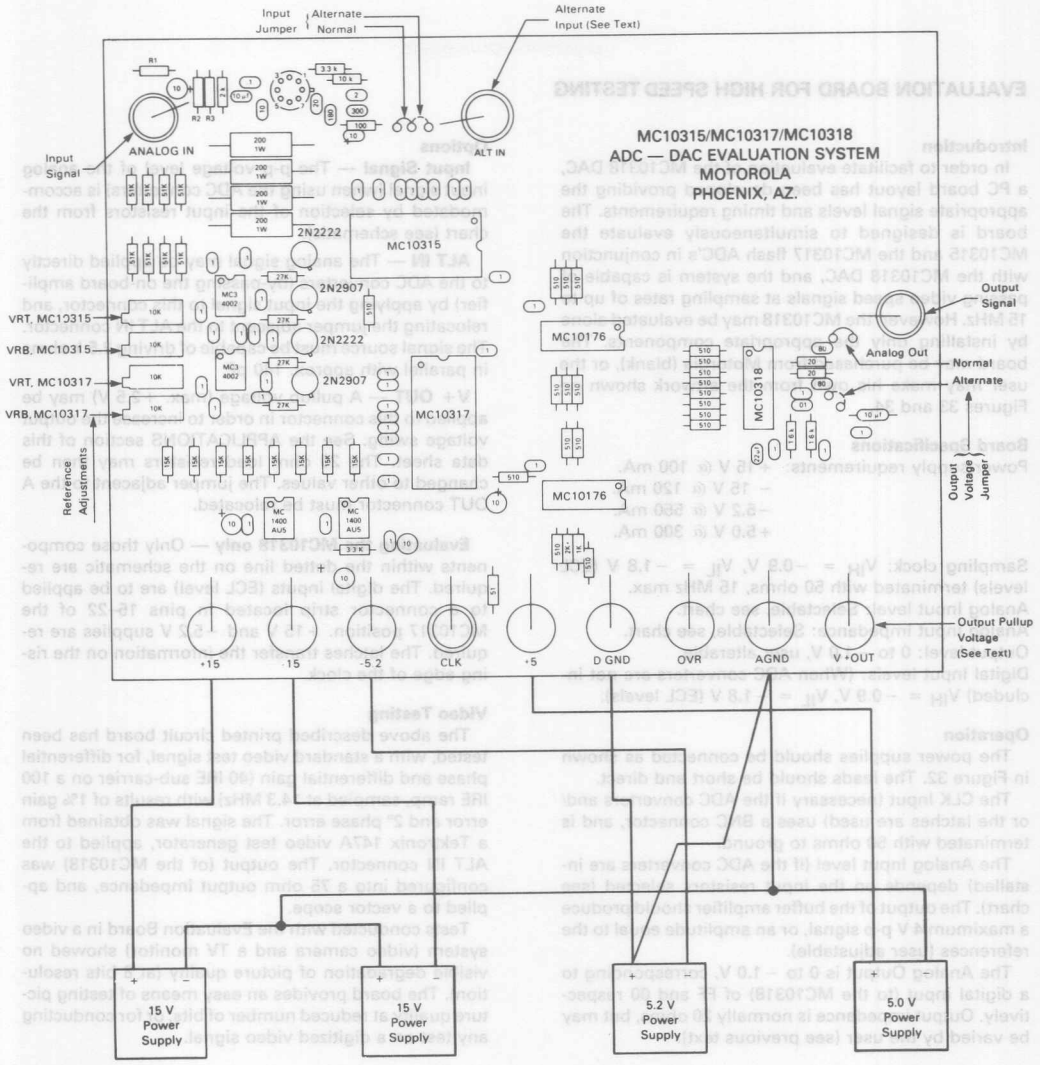
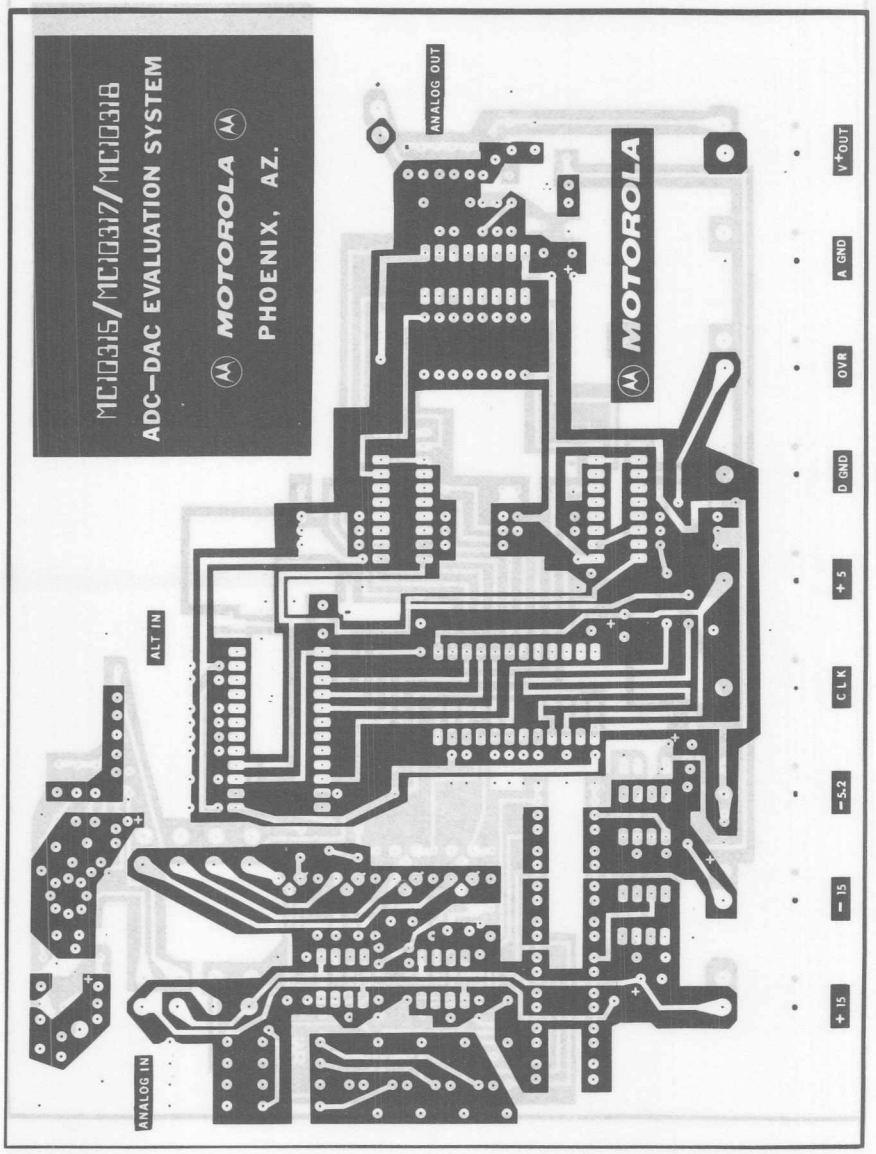


FIGURE 33 — COMPONENT SIDE ARTWORK (TOP)
(OVERALL SIZE = 6.00″ × 8.00″)



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FIGURE 34 — SOLDER SIDE ARTWORK (BOTTOM)

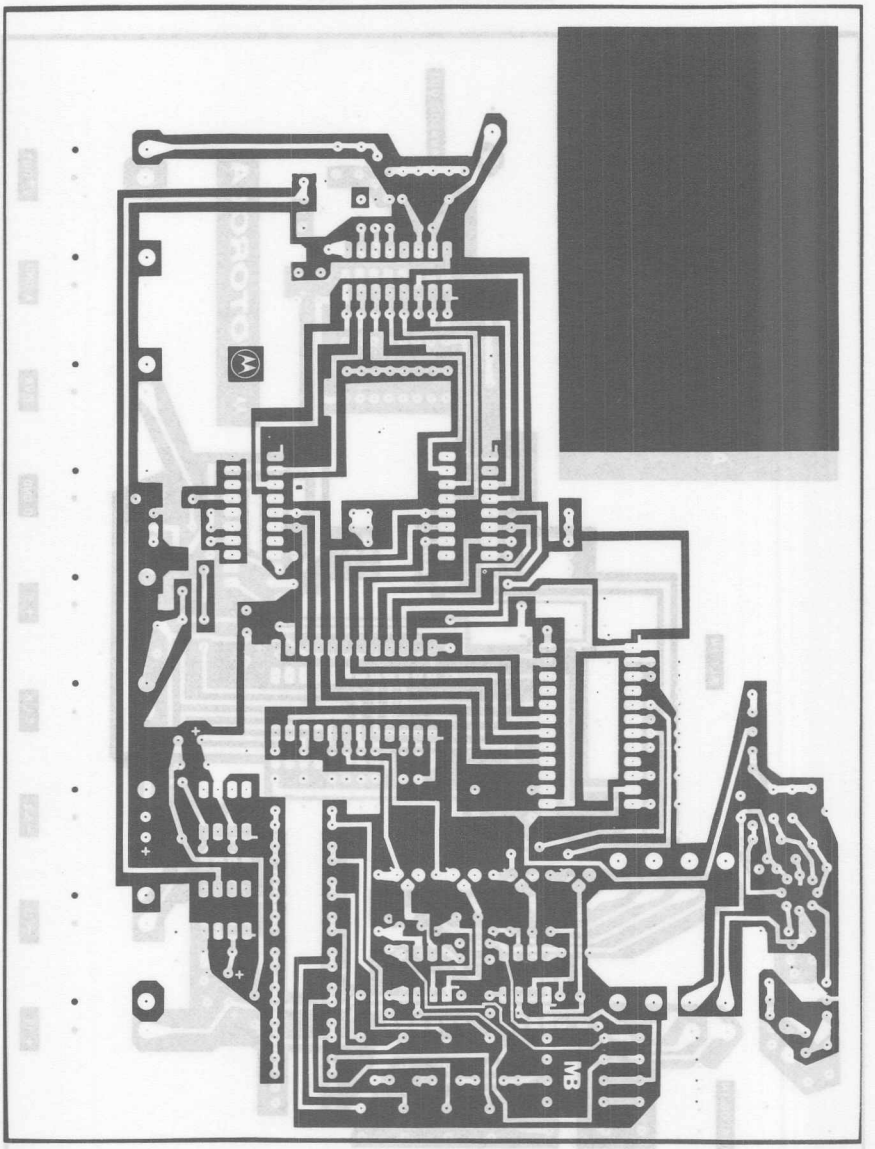
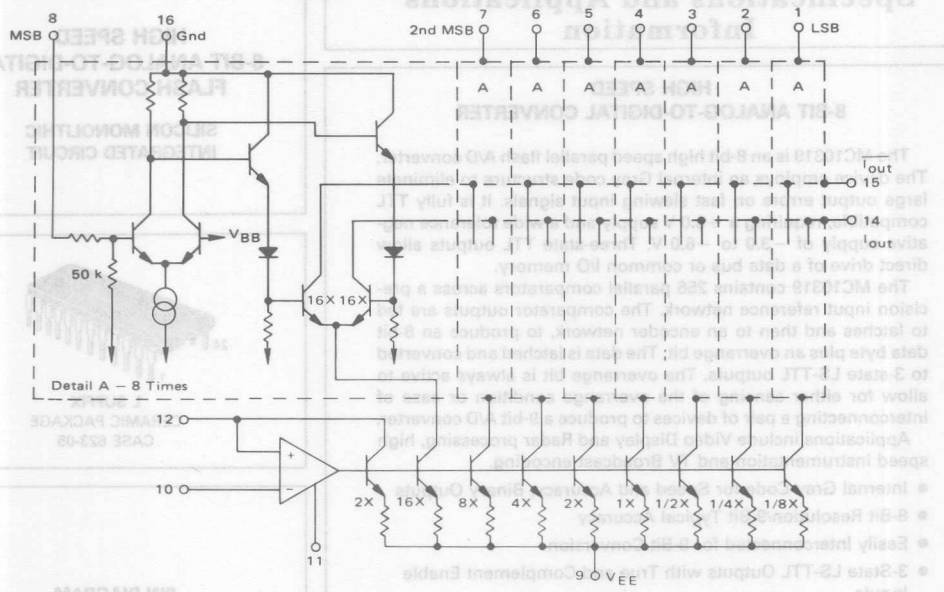


FIGURE 35 — MC10318 EQUIVALENT CIRCUIT



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Specifications and Applications Information

HIGH SPEED 8-BIT ANALOG-TO-DIGITAL CONVERTER

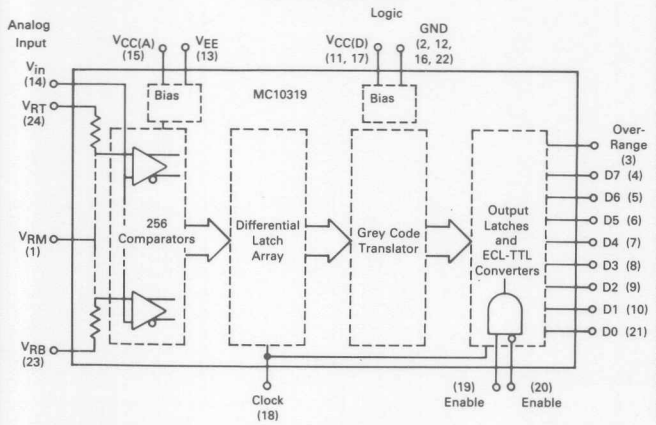
The MC10319 is an 8-bit high speed parallel flash A/D converter. The device employs an internal Grey code structure to eliminate large output errors on fast slewing input signals. It is fully TTL compatible, requiring a +5.0 V supply and a wide tolerance negative supply of −3.0 to −6.0 V. Three-state TTL outputs allow direct drive of a data bus or common I/O memory.

The MC10319 contains 256 parallel comparators across a precision input reference network. The comparator outputs are fed to latches and then to an encoder network, to produce an 8-bit data byte plus an overrange bit. The data is latched and converted to 3-state LS-TTL outputs. The overrange bit is always active to allow for either sensing of the overrange condition or ease of interconnecting a pair of devices to produce a 9-bit A/D converter.

Applications include Video Display and Radar processing, high speed instrumentation and TV Broadcast encoding.

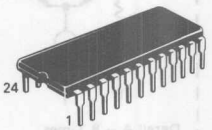
- Internal Grey Code for Speed and Accuracy, Binary Outputs
- 8-Bit Resolution/9-Bit Typical Accuracy
- Easily Interconnected for 9-Bit Conversion
- 3-State LS-TTL Outputs with True and Complement Enable Inputs
- 25 MHz Sampling Rate
- Wide Input Range: 1.0–2.0 V_{p-p} Between ±2.0 V
- Low Input Capacitance: 50 pF
- Low Power Dissipation: 618 mW
- No Sample/Hold Required for Video Bandwidth Signals
- Single Clock Cycle Conversion

BLOCK DIAGRAM



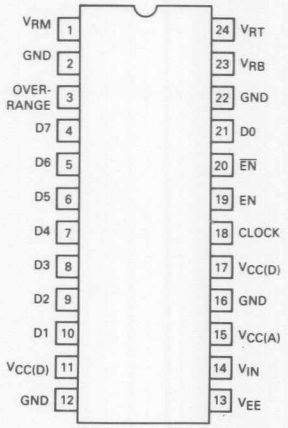
HIGH SPEED 8-BIT ANALOG-TO-DIGITAL FLASH CONVERTER

SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 623-05

PIN DIAGRAM



ORDERING INFORMATION

Device	Temperature Range	Package
MC10319L	0° to +70°C	Ceramic

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Supply Voltage	$V_{CC(A),(D)}$ V_{EE}	+7.0 −7.0	Vdc
Positive Supply Voltage Differential	$V_{CC(D)}-V_{CC(A)}$	−0.3 to +0.3	Vdc
Digital Input Voltage (Pins 18–20)	$V_{I(D)}$	−0.5 to +7.0	Vdc
Analog Input Voltage (Pins 1, 14, 23, 24)	$V_{I(A)}$	−2.5 to +2.5	Vdc
Reference Voltage Span (Pin 24–Pin 23)	—	2.3	Vdc
Applied Output Voltage (Pins 4–10, 21 in 3-State)	—	−0.3 to +7.0	Vdc
Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	−65 to +150	°C

Devices should not be operated at these values. The "Recommended Operating Limits" provide guidelines for actual device operation.

RECOMMENDED OPERATING LIMITS

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage (Pin 15) (Pins 11, 17)	$V_{CC(A)}$ $V_{CC(D)}$	+4.5	+5.0	+5.5	Vdc
$V_{CC(D)} - V_{CC(A)}$	ΔV_{CC}	−0.1	0	+0.1	Vdc
Power Supply Voltage (Pin 13)	V_{EE}	−6.0	−5.0	−3.0	Vdc
Digital Input Voltages (Pins 18–20)	$V_{I(D)}$	0	—	+5.0	Vdc
Analog Input (Pin 14)	$V_{I(A)}$	−2.1	—	+2.1	Vdc
Voltage @ V_{RT} (Pin 24)	V_{RT}	−1.0	—	+2.1	Vdc
Voltage @ V_{RB} (Pin 23)	V_{RB}	−2.1	—	+1.0	Vdc
$V_{RT} - V_{RB}$	ΔV_R	+1.0	—	+2.1	Vdc
$V_{RB} - V_{EE}$	—	1.3	—	—	Vdc
Applied Output Voltage (Pins 4–10, 21 in 3-State)	V_o	0	—	5.5	Vdc
Clock Pulse Width — High Low	t_{CKH} t_{CKL}	5.0 15	20 20	— —	ns
Clock Frequency	f_{CLK}	0	—	25	MHz
Operating Ambient Temperature	T_A	0	—	+70	°C

ELECTRICAL CHARACTERISTICS ($0° < T_A < 70°C$, V_{CC} = 5.0 V, V_{EE} = −5.2 V, V_{RT} = +1.0 V, V_{RB} = −1.0 V, except where noted.)

Parameter	Symbol	Min	Typ	Max	Unit
TRANSFER CHARACTERISTICS (f_{CKL} = 25 MHz)					
Resolution	N	—	—	8.0	Bits
Monotonicity	MON		Guaranteed		Bits
Integral Nonlinearity	INL	—	±1/4	±1.0	LSB
Differential Nonlinearity	DNL	—	—	±1.0	LSB
Differential Phase (See Figure 16)	DP	—	1.0	—	Deg.
Differential Gain (See Figure 16)	DG	—	1.0	—	%
Power Supply Rejection Ratio (4.5 V < V_{CC} < 5.5 V, V_{EE} = −5.2 V) (−6.0 V < V_{EE} < −3.0 V, V_{CC} = +5.0 V)	PSRR	— —	0.1 0	— —	LSB/V

ELECTRICAL CHARACTERISTICS — continued ($0° < T_A < 70°C$, V_{CC} = 5.0 V, V_{EE} = −5.2 V, V_{RT} = +1.0 V, V_{RB} = −1.0 V, except where noted.)

Parameter	Symbol	Min	Typ	Max	Unit
ANALOG INPUT (PIN 14)					
Input Current @ $V_{in} = V_{RB}$ (See Figure 5)	I_{INL}	−100	0	—	μA
Input Current @ $V_{in} = V_{RT}$ (See Figure 5)	I_{INH}	—	60	150	μA
Input Capacitance ($V_{RT} - V_{RB}$ = 2.0 V, See Figure 4)	C_{in}	—	36	—	pF
Input Capacitance ($V_{RT} - V_{RB}$ = 1.0 V, See Figure 4)	C_{in}	—	55	—	pF
Bipolar Offset Error	V_{OS}	—	0.1	—	LSB
REFERENCE					
Ladder Resistance (V_{RT} to V_{RB}, T_A = 25°C)	R_{ref}	104	130	156	Ω
Temperature Coefficient	T_C	—	+0.29	—	%/°C
Ladder Capacitance (Pin 1 open)	C_{ref}	—	25	—	pF
ENABLE INPUTS (V_{CC} = 5.5 V) (See Figure 6)					
Input Voltage — High (Pins 19–20)	V_{IHE}	2.0	—	—	V
Input Voltage — Low (Pins 19–20)	V_{ILE}	—	—	0.8	V
Input Current @ 2.7 V	I_{IHE}	—	0	20	μA
Input Current @ 0.4 V @ $\overline{EN}$ (0 < EN < 5.0 V)	I_{IL1}	−400	−100	—	μA
Input Current @ 0.4 V @ EN ($\overline{EN}$ = 0 V)	I_{IL2}	−400	−100	—	μA
Input Current @ 0.4 V @ EN ($\overline{EN}$ = 2.0 V)	I_{IL3}	−20	−2.0	—	μA
Input Clamp Voltage (I_{IK} = −18 mA)	V_{IKE}	−1.5	−1.3	—	V
CLOCK INPUT (V_{CC} = 5.5 V)					
Input Voltage High	V_{IHC}	2.0	—	—	Vdc
Input Voltage Low	V_{ILC}	—	—	0.8	Vdc
Input Current @ 0.4 V (See Figure 7)	I_{ILC}	−400	−80	—	μA
Input Current @ 2.7 V (See Figure 7)	I_{IHC}	−100	−20	—	μA
Input Clamp Voltage (I_{IK} = −18 mA)	V_{IKC}	−1.5	−1.3	—	Vdc
DIGITAL OUTPUTS					
High Output Voltage (I_{OH} = −400 μA, V_{CC} = 4.5 V, See Figure 8)	V_{OH}	2.4	3.0	—	V
Low Output Voltage (I_{OL} = 4.0 mA, See Figure 9)	V_{OL}	—	0.35	0.4	V
Output Short Circuit Current* (V_{CC} = 5.5 V)	I_{SC}	—	35	—	mA
Output Leakage Current (0.4 < V_O < 2.4 V, See Figure 3, V_{CC} = 5.5 V, D0–D7 in 3-State Mode)	I_{LK}	−50	—	+50	μA
Output Capacitance (D0–D7 in 3-State Mode)	C_{out}	—	9.0	—	pF
POWER SUPPLIES					
$V_{CC(A)}$ Current (4.5 V < $V_{CC(A)}$ < 5.5 V) (Outputs unloaded)	$I_{CC(A)}$	10	17	25	mA
$V_{CC(D)}$ Current (4.5 V < $V_{CC(D)}$ < 5.5 V) (Outputs unloaded)	$I_{CC(D)}$	50	90	133	mA
V_{EE} Current (−6.0 V < V_{EE} < −3.0 V)	I_{EE}	−14	−10	−6.0	mA
Power Dissipation ($V_{RT} - V_{RB}$ = 2.0 V) (Outputs unloaded)	P_D	—	618	995	mW

*Only one output is to be shorted at a time, not to exceed 1 second.

TIMING CHARACTERISTICS (T_A = 25°C, V_{CC} = +5.0 V, V_{EE} = −5.2 V, V_{RT} = +1.0 V, V_{RB} = −1.0 V, See System Timing Diagram.)

Parameter	Symbol	Min	Typ	Max	Unit
INPUTS					
Min Clock Pulse Width — High	t_{CKH}	—	5.0	—	ns
Min Clock Pulse Width — Low	t_{CKL}	—	15	—	ns
Max Clock Rise, Fall Time	$t_{R,F}$	—	100	—	ns
Clock Frequency	f_{CLK}	0	30	25	MHz
OUTPUTS					
New Data Valid from Clock Low	t_{CKDV}	—	19	—	ns
Aperture Delay	t_{AD}	—	4.0	—	ns
Hold Time	t_H	—	6.0	—	ns
Data High to 3-State from Enable Low*	t_{EHZ}	—	27	—	ns
Data Low to 3-State from Enable Low*	t_{ELZ}	—	18	—	ns
Data High to 3-State from $\overline{\text{Enable}}$ High*	$t_{\overline{E}HZ}$	—	32	—	ns
Data Low to 3-State from $\overline{\text{Enable}}$ High*	$t_{\overline{E}LZ}$	—	18	—	ns
Valid Data from Enable High (Pin 20 = 0 V)*	t_{EDV}	—	15	—	ns
Valid Data from $\overline{\text{Enable}}$ Low (Pin 19 = 5.0 V)*	$t_{\overline{E}DV}$	—	16	—	ns
Output Transition Time* (10%–90%)	t_{tr}	—	8.0	—	ns

*See Figure 2 for output loading.

PIN DESCRIPTIONS

Symbol	Pin	Description
V_{RM}	1	The midpoint of the reference resistor ladder. Bypassing can be done at this point to improve performance at high frequencies.
GND	2,12 16,22	Power supply and signal ground. The four pins should be connected directly together, and through a low impedance to the power supply.
OVR	3	Overrange output. Indicates V_{in} is more positive than V_{RT}-1/2 LSB. This output does not have 3-state capability.
D7–D0	4–10, 21	Digital Outputs. D7 (Pin 4) is the MSB, D0 (Pin 21) is the LSB. LSTTL compatible with 3-state capability.
$V_{CC(D)}$	11,17	Power supply for the digital section. +5.0 V, ±10% required.
V_{EE}	13	Negative Power supply. Nominally −5.2 V, it can range from −3.0 to −6.0 V, and must be more negative than V_{RB} by > 1.3 V.
V_{in}	14	Signal voltage input. This voltage is compared to the reference to generate a digital equivalent. Input impedance is nominally 16–33 kΩ in parallel with 36 pF.
$V_{CC(A)}$	15	Power supply for the analog section. +5.0 V, ±10% required.
CLK	18	Clock input. TTL compatible.
EN	19	Enable input. TTL compatible, a Logic "1" (and Pin 20 a Logic "0") enables the data outputs. A Logic "0" puts the outputs in a 3-state mode.
$\overline{\text{EN}}$	20	$\overline{\text{Enable}}$ input. TTL compatible, a Logic "0" (and Pin 19 a Logic "1") enables the data outputs. A Logic "1" puts the outputs in a 3-state mode.
V_{RB}	23	The bottom (most negative point) of the internal reference resistor ladder.
V_{RT}	24	The top (most positive point) of the internal reference resistor ladder.

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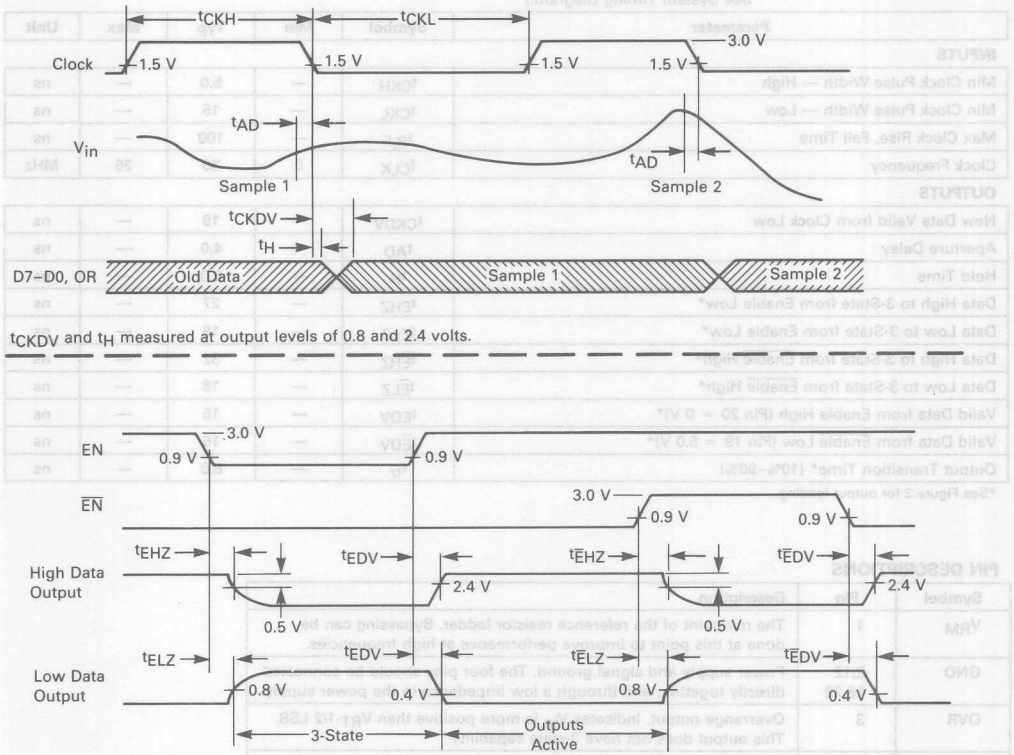
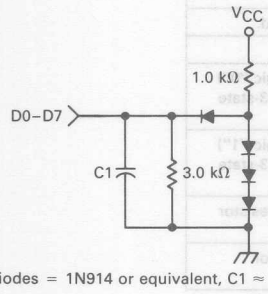


FIGURE 2 — DATA OUTPUT TEST CIRCUIT



Diodes = 1N914 or equivalent, C1 ≈ 15 pF

FIGURE 3 — OUTPUT 3-STATE LEAKAGE CURRENT

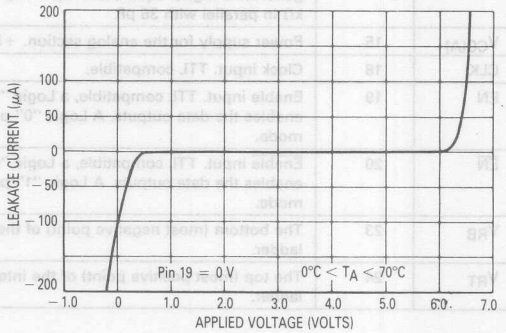


FIGURE 4 — INPUT CAPACITANCE @ V_{IN} (PIN 14)

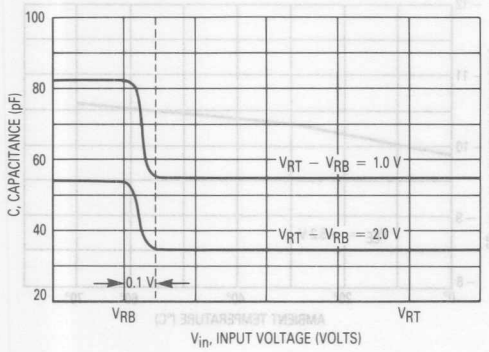


FIGURE 5 — INPUT CURRENT @ V_{IN} (PIN 14)

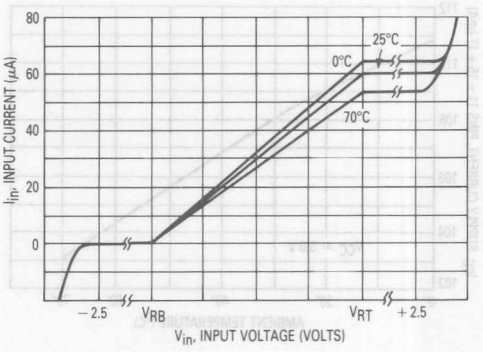


FIGURE 6 — INPUT CURRENT @ ENABLE, $\overline{\text{ENABLE}}$

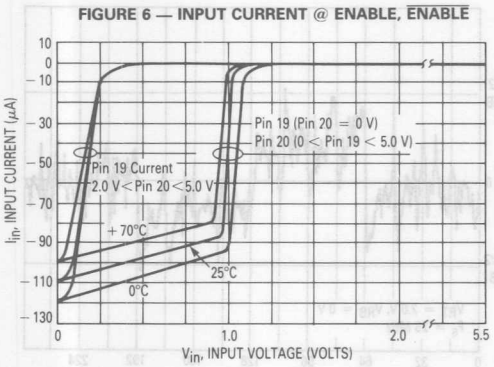


FIGURE 7 — CLOCK INPUT CURRENT

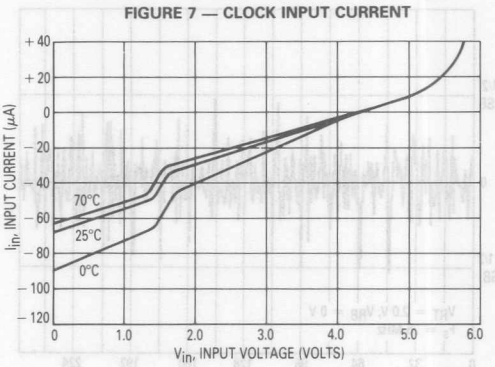


FIGURE 8 — OUTPUT VOLTAGE versus OUTPUT CURRENT

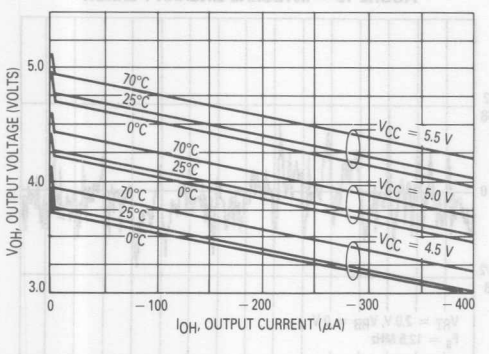
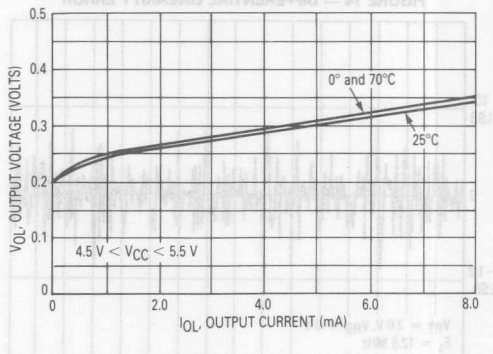


FIGURE 9 — OUTPUT VOLTAGE versus OUTPUT CURRENT



6

FIGURE 10 — SUPPLY CURRENT versus TEMPERATURE

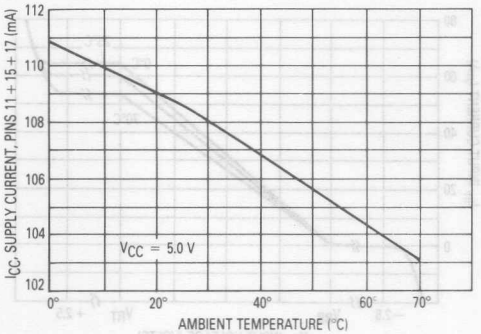


FIGURE 11 — SUPPLY CURRENT versus TEMPERATURE

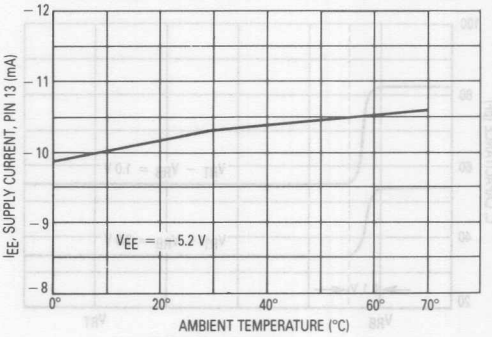


FIGURE 12 — DIFFERENTIAL LINEARITY ERROR

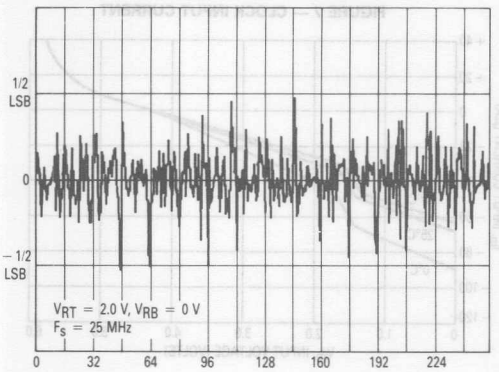


FIGURE 13 — INTEGRAL LINEARITY ERROR

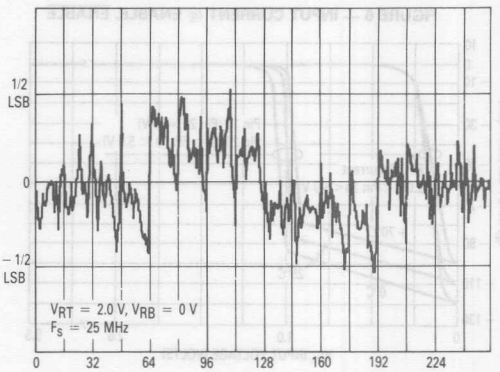


FIGURE 14 — DIFFERENTIAL LINEARITY ERROR

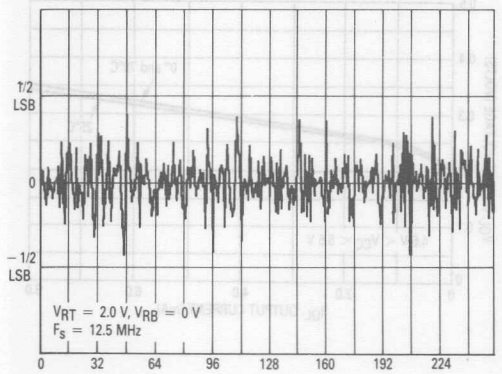
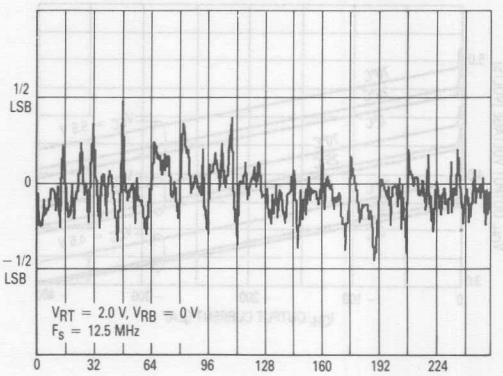


FIGURE 15 — INTEGRAL LINEARITY ERROR



DESIGN GUIDELINES

INTRODUCTION

The MC10319 is a high-speed, 8-bit, parallel ("Flash") type analog-to-digital converter containing 256 comparators at the front end. See Figure 17 for a block diagram. The comparators are arranged such that one input of each is referenced to evenly spaced voltages, derived from the reference resistor ladder. The other input of the comparators is connected to the input signal (V_{in}). Some of the comparator's differential outputs will be "true," while other comparators will have "not true" outputs, depending on their relative position. Their outputs are then latched, and converted to an 8-bit Grey code by the Differential Latch Array. The Grey code ensures any input errors due to cross talk, feed-thru, or timing disparaties, result in glitches at the output of only a few LSBs, rather than the more traditional 1/2 scale and 1/4 scale glitches.

The Grey code is then translated to an 8-bit binary code, and the differential levels are translated to TTL levels before being applied to the output latches. ENABLE inputs at this final stage permit the TTL outputs (except Overrange) to be put into a high impedance (3-state) condition.

ANALOG SECTION

SIGNAL INPUT

The signal voltage to be digitized (V_{in}) is applied simultaneously to one input of each of the 256 comparators through Pin 14. The other inputs of the comparators are connected to 256 evenly spaced voltages derived from the reference ladder. The output code depends on the relative position of the input signal and the reference voltages. The comparators have a bandwidth of >50 MHz, which is more than sufficient for the allowable (Nyquist theory) input frequency of 12.5 MHz.

The current into Pin 14 varies linearly from 0 (when $V_{in} = V_{RB}$) to ≈60 μA (when $V_{in} = V_{RT}$). If V_{in} is taken below V_{RB} or above V_{RT}, the input current will remain at the value corresponding to V_{RB} and V_{RT} respectively (see Figure 5). However, V_{in} must be maintained within the absolute range of ±2.5 volts (with respect to ground) — otherwise excessive currents will result at Pin 14, due to internal clamps.

The input capacitance at Pin 14 is typically 36 pF if [$V_{RT} - V_{RB}$] is 2.0 volts, and increases to 55 pF if [$V_{RT} - V_{RB}$] is reduced to 1.0 volt (see Figure 4). The capacitance is constant as V_{in} varies from V_{RT} down to ≈0.1 volt above V_{RB}. Taking V_{in} to V_{RB} will show an increase in the capacitance of ≈50%. If V_{in} is taken above V_{RT}, or below V_{RB}, the capacitance will stay at the values corresponding to V_{RT} and V_{RB}, respectively.

The source impedance of the signal voltage should be maintained below 100 Ω (at the frequencies of interest) in order to avoid sampling errors.

REFERENCE

The reference resistor ladder is composed of a string of equal value resistors so as to provide 256 equally spaced voltages for the comparators (see Figure 17 for the actual configuration). The voltage difference between adjacent comparators corresponds to 1 LSB of the input range. The first comparator (closest to V_{RB}) is referenced 1/2 LSB above V_{RB}, and the 256th comparator (for the overrange) is referenced 1/2 LSB below V_{RT}. The total resistance of the ladder is nominally 130 Ω, ±20%, requiring 15.4 mA @ 2.0 volts, and 7.7 mA @ 1.0 volt. There is a nominal warm-up change of ≈ +9.0% in the ladder resistance due to the +0.29%/°C temperature coefficient.

The minimum recommended span [$V_{RT} - V_{RB}$] is 1.0 volt. A lower span will allow offsets and nonlinearities to become significant. The maximum recommended span is 2.1 volts due to power limitations of the resistor ladder. The span may be anywhere within the range of −2.1 to +2.1 volts with respect to ground, and V_{RB} must be at least 1.3 volts more positive than V_{EE}. The reference voltages must be stable and free of noise and spikes, since the accuracy of a conversion is directly related to the quality of the reference.

In most applications, the reference voltages will remain fixed. In applications involving a varying reference for modulation or signal scrambling, the modulating signal may be applied to V_{RT}, or V_{RB}, or both. The output will vary inversly with the reference signal, introducing a nonlinearity into the transfer function. The addition of the modulating signal and the dc level applied to the reference must be such that the absolute voltage at V_{RT} and V_{RB} are maintained within the values listed in the Recommended Operating Limits. The RMS value of the span must be maintained ≤2.1 volts.

V_{RM} (Pin 1) is the midpoint of the resistor ladder, excluding the Overrange comparator. The voltage at V_{RM} is:

$$\frac{V_{RT} + V_{RB}}{2.0} - 1/2 \text{ LSB}$$

In most applications, bypassing this pin to ground (0.1 μF) is sufficient to maintain accuracy. In applications involving very high frequencies, and where linearity is critical, it may be necessary to trim the voltage at the midpoint. A means for accomplishing this is indicated in Figure 18.

POWER SUPPLIES

$V_{CC(A)}$ (Pin 15) is the positive power supply for the comparators, and $V_{CC(D)}$ (Pins 11, 17) is the positive power supply for the digital portion. Both are to be +5.0 volts, ±10%, and the two are to be within 100 millivolts of each other. There is indirect internal coupling between $V_{CC(D)}$ and $V_{CC(A)}$. If they are powered separately, and one supply fails, there will be current flow through the MC10319 to the failed supply.

clock frequency or with V_{in}. It does vary linearly with $V_{CC(A)}$. $I_{CC(D)}$ is nominally 90 mA, and is independent of clock frequency. It does vary, however, by 6–7 mA as V_{in} is changed, with the lowest current occuring when $V_{in} = V_{RT}$. It varies linearly with $V_{CC(D)}$.

V_{EE} is the negative power supply for the comparators, and is to be within the range −3.0 to −6.0 volts. Additionally, V_{EE} must be at least 1.3 volts more negative than V_{RB}. I_{EE} is a nominal −10 mA, and is independent of clock frequency, V_{in}, and V_{EE}.

For proper operation, the supplies **must** be bypassed **at the IC**. A 10 μF tantalum, in parallel with a 0.1 μF ceramic is recommended for each supply to ground.

DIGITAL SECTION

CLOCK

The Clock input (Pin 18) is TTL compatible with a typical frequency range of 0 to 30 MHz. There is no duty cycle limitation, but the minimum low and high times must be adhered to. See Figure 7 for the input current requirements.

The conversion sequence is shown in Figure 19, and is as follows:

- On the rising edge, the data output latches are latched with old data, and the comparator output latches are released to follow the input signal (V_{in}).
- During the high time, the comparators track the input signal. The data output latches retain the old data.
- On the falling edge, the comparator outputs are latched with the data immediately prior to this edge. The conversion to digital occurs within the device, and the data output latches are released to indicate the new data within 20 ns.
- During the clock low time, the comparator outputs remain latched, and the data output latches remain transparent.

A summary of the sequence is that data present at V_{in} just prior to the Clock falling edge is digitized and available at the data outputs immediately after that same falling edge.

with an effective sample-and-hold function, eliminating the need for an external sample-and-hold.

ENABLE INPUTS

The two Enable inputs (Pins 19, 20) are TTL compatible, and are used to change the data outputs (D7–D0) from active to 3-state. This capability allows cascading two MC10319s into a 9-bit configuration, flip-flopping two MC10319s into a 50 MHz configuration, connecting the outputs directly to a data bus, multiplexing multiple converters, etc. See the Applications Information section for more details. For the outputs to be active, Pin 19 must be a Logic "1," and Pin 20 must be a Logic "0." Changing either input will put the outputs into the high impedance mode. The Enable inputs affect **only** the state of the outputs — they do not inhibit a conversion. The input current into Pins 19 and 20 is shown in Figure 6, and the input — output timing is shown in Figure 1 and 20. Leaving either pin open is equivalent to a Logic "1," although good design practice dictates that an input should never be left open.

The Overrange output (Pin 3) is not affected by the Enable inputs as it does not have 3-state capability.

OUTPUTS

The data outputs (Pins 4–10, 21) are TTL level outputs with high impedance capability. Pin 4 is the MSB (D7), and Pin 21 is the LSB (D0). The eight outputs are active as long as the Enable inputs are true (Pin 19 = high, Pin 20 = low). The timing of the outputs relative to the Clock input and the Enable inputs is shown in Figures 1 and 20. Figures 8 and 9 indicate the output voltage versus load current, while Figure 3 indicates the leakage current when in the high impedance mode.

The output code is natural binary, depicted in the table below.

The Overrange output (Pin 3) goes high when the input, V_{in}, is more positive than V_{RT} − 1/2 LSB. This output is always active — it does not have high impedance capability. Besides being used to indicate an input overrange, it is additionally used for cascading two MC10319s to form a 9-bit A/D converter (see Figure 27).

Input	V_{RT}, V_{RB} (volts)			Output Code	Overrange
	2.048 V, 0 V	+1.0 V, −1.0 V	+1.0 V, 0 V		
$>V_{RT}$ − 1/2 LSB	>2.044 V	>0.9961 V	>0.9980 V	FF_H	1
V_{RT} − 1/2 LSB	2.044 V	0.9961 V	0.9980 V	FF_H	0 ↔ 1
V_{RT} − 1 LSB	2.040 V	0.992 V	0.9961 V	FF_H	0
V_{RT} − 1-1/2 LSB	2.036 V	0.988 V	0.9941 V	$FE_H \leftrightarrow FF_H$	0
Midpoint	1.024 V	0.000 V	0.5000 V	80_H	0
V_{RB} + 1/2 LSB	4.0 mV	−0.9961 V	1.95 mV	$00_H \leftrightarrow 01_H$	0
$<V_{RB}$	<0 V	<−1.0 V	<0 V	00_H	0

APPLICATIONS INFORMATION

POWER SUPPLIES, GROUNDING

The PC board layout, and the quality of the power supplies and the ground system **at the IC** are very important in order to obtain proper operation. Noise, from any source, coming into the device on V_{CC}, V_{EE}, or ground can cause an incorrect output code due to interaction with the analog portion of the circuit. At the same time, noise generated within the MC10319 can cause incorrect operation if that noise does not have a clear path to ac ground.

Both the V_{CC} and V_{EE} power supplies must be decoupled to ground **at the IC** (within 1" max) with a 10 μF tantalum and a 0.1 μF ceramic. Tantalum capacitors are recommended since electrolytic capacitors simply have too much inductance at the frequencies of interest. The quality of the V_{CC} and V_{EE} supplies should then be checked at the IC with a high frequency scope. Noise spikes (always present when digital circuits are present) can easily exceed 400 mV peak, and if they get into the analog portion of the IC, the operation can be disrupted. Noise can be reduced by inserting resistors and/or inductors between the supplies and the IC.

If switching power supplies are used, there will usually be spikes of 0.5 volts or greater at frequencies of 50–200 kHz. These spikes are generally more difficult to reduce because of their greater energy content. In extreme cases, 3-terminal regulators (MC78L05ACP, MC7905.2CT), with appropriate high frequency filtering, should be used and dedicated to the MC10319.

The ripple content of the supplies should not allow their magnitude to exceed the values in the Recommended Operating Limits.

The PC board tracks supplying V_{CC} and V_{EE} to the MC10319 should preferably not be at the tail end of the bus distribution, after passing through a maze of digital circuitry. The MC10319 should be close to the power supply, or the connector where the supply voltages enter the board. If the V_{CC} and V_{EE} lines are supplying considerable current to other parts of the boards, then it is preferable to have dedicated lines from the supply or connector directly to the MC10319.

The four ground pins (2, 12, 16, 22) must be connected directly together. Any long path beween them can cause stability problems due to the inductance (@ 25 MHz) of the PC tracks. The ground return for the signal source must be noise free.

REFERENCE VOLTAGE CIRCUITS

Since the accuracy of the conversion is directly related to the quality of the references, it is imperative that accurate and stable voltages be provided to V_{RT} and V_{RB}. If the reference span is 2 volts, then 1/2 LSB is only 3.9 millivolts, and it is desireable that V_{RT} and V_{RB} be accurate to within this amount, and furthermore, that they do not drift more than this amount once set. Over the temperature range of 0 to 70°C, a maximum temperature coefficient of 28 ppm/°C is required.

The voltage supplies used for digital circuits should preferably **not** be used as a source for generating V_{RT} and V_{RB}, due to the noise spikes (50–400 mV) present on the supplies and on their ground lines. Generally $\pm$15 volts, or $\pm$12 volts, are available for analog circuits, and are usually clean compared to supplies used for digital circuits, although ripple may be present in varying amounts. Ripple is easier to filter out than spikes, however, and so these supplies are preferred.

Figure 21 depicts a circuit which can provide an extremely stable voltage to V_{RT} **at the current required** (the maximum reference current is 19.2 mA @2.0 volts). The MC1400 and MC1403 series of reference sources have very low temperature coefficients, good noise rejection, and a high initial accuracy, allowing the circuit to be built without an adjustment pot if the V_{RT} voltage is to remain fixed at one value. Using 0.1% wirewound resistors for the divider provides sufficient accuracy and stability in many cases. Alternately, resistor networks provide high ratio accuracies, and close temperature tracking. If the application requires V_{RT} to be changed periodically, the two resistors can be replaced with a 20 turn, cermet potentiometer. Wirewound potentiometers should not be used for this type of application since the pot's slider jumps from winding to winding, and an exact setting can be difficult to obtain. Cermet pots allow for a smooth continuous adjustment.

In Figure 21, R1 reduces the power dissipation in the transistor, and can be carbon composition. The 0.1 μF capacitor in the feedback path provides stability in the unity gain configuration. Recommended op amps are: LM358, MC34001 series, LM308A, LM324, and LM11C. Offset drift is the key parameter to consider in choosing an op amp, and the LM308A has the lowest drift of those mentioned. Bypass capacitors are not shown in Figure 21, but should always be provided at the input to the 2.5 volt reference, and at the power supply pins of the op amp.

Figure 22 shows a simpler and more economical circuit, using the LM317LZ regulator, but with lower initial accuracy and temperature stability. The op amp/current booster is not needed since the LM317LZ can supply the current directly. In a well controlled environment, this circuit will suffice for many applications. Because of the lower initial accuracy, an adjustment pot is a necessity.

Figure 23 shows two circuits for providing the voltage to V_{RB}. The circuits are similar to those of Figures 21 and 22, and have similar accuracy and stability. Although the MC1400G2 is meant to provide a positive voltage, it can be configured to provide a negative regulated voltage by grounding the input and output, and deriving the regulated voltage at the ground pin (Pin 4). The MC1403 series of regulators cannot be used in this manner. The output transistor is a PNP in this case since the circuit must sink the reference current.

VIDEO APPLICATIONS

The MC10319 is suitable for digitizing video signals directly without signal conditioning, although the standard 1 volt p-p video signal can be amplified to a 2.0 volt p-p signal for slightly better accuracy. Figure 24 shows the input (top trace) and reconstructed output of a standard NTSC test signal, sampled at 25 MSPS, consisting of a sync pulse, 3.58 MHz color burst, a 3.58 MHz signal in a Sin^2x envelope, a pulse, a white level signal, and a black level signal. Figure 25 shows a Sin^2x pulse that has been digitized and reconstructed at 25 MSPS. The width of the pulse is ≈450 ns at the base. Figure 26 shows an application circuit for digitizing video.

9-BIT A/D CONVERTER

Figure 27 shows how two MC10319s can be connected to form a 9-bit converter. In this configuration, the outputs (D7–D0) of the two 8-bit converters are paralleled. The outputs of one device are active, while the outputs of other are in the 3-state mode. The selection is made by the OVERRANGE output of the lower MC10319, which controls Enable inputs on the two devices. Additionally, this output provides the 9th bit.

The reference ladders are connected in series, providing the 512 steps required for 9 bits. The input voltage range is determined by V_{RT} of the upper MC10319, and V_{RB} of the lower device. A minimum of 1.0 volt is required across each converter. The 500 Ω pot (20 turn cermet) allows for adjustment of the midpoint since the reference resistors of the two MC10319s may not be identical in value. Without the adjustment, a non-equal voltage division would occur, resulting in a nonlinear conversion. If the references are to be symmetrical about ground (e.g., ±1.0 volt), the adjustment can be eliminated, and the midpoint connected to ground.

The use of latches on the outputs is optional, depending on the application.

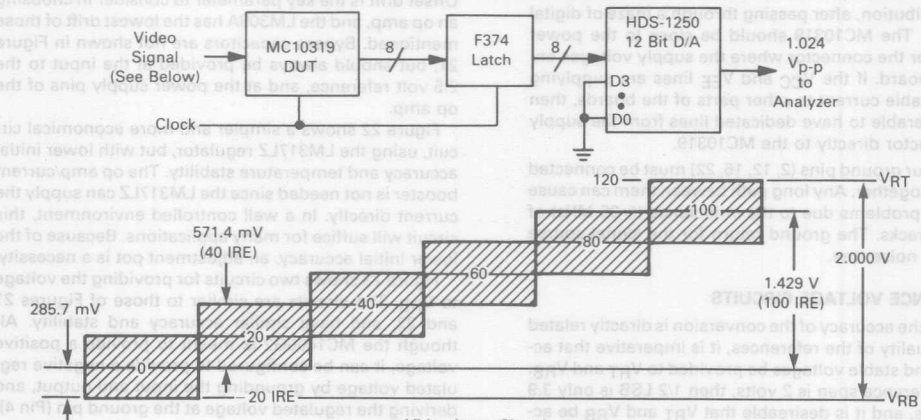
50 MHz, 8-BIT A/D CONVERTER

Figure 28 shows how two MC10319s can be connected together in a flip-flop arrangement in order to have an effective conversion speed of 50 MHz. The 74F74 D-type flip-flop provides a 25 MHz clock to each converter, and at the same time, controls the ENABLES so as to alternately enable and disable the outputs. The Overranges do not have 3-state capability, and so cannot be paralleled. Instead they are OR'd together. The use of latches is optional, and depends on the application. Data should be latched, or written to RAM (in a DMA operation), on the high-to-low transition of the 50 MHz clock.

NEGATIVE VOLTAGE REGULATOR

In the cases where a negative power supply is not available — neither the −3.0 to −6.0 volts, nor a higher negative voltage from which to derive it — the circuit of Figure 29 can be used to generate −5.0 volts from the +5.0 volts supply. The PC board space required is small (≈2.0 in^2), and it can be located physically close to the MC10319. The MC34063 is a switching regulator, and in Figure 29 is configured in an inverting mode of operation. The regulator operating specifications are given in the Figure.

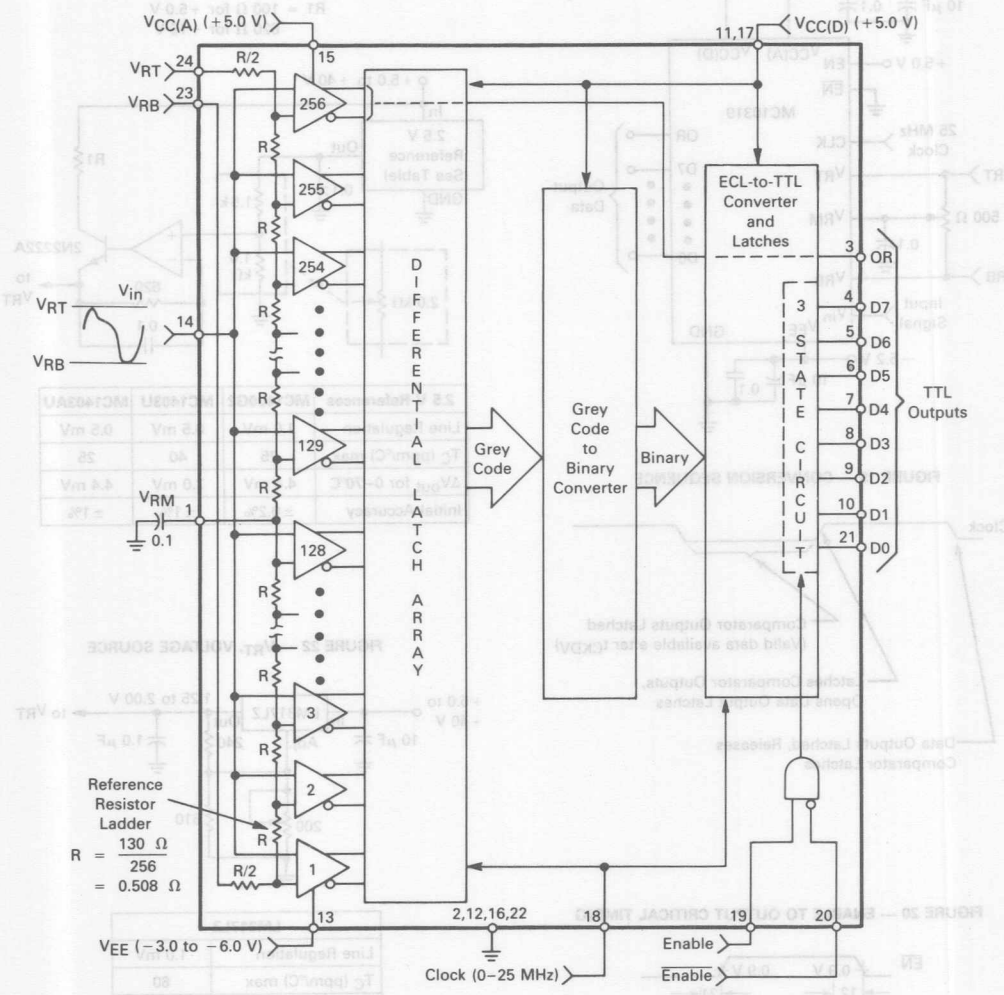
FIGURE 16 — DIFFERENTIAL PHASE AND GAIN TEST



Video Input Signal

— Input waveform: 571.4 mV_{p-p} sine wave @ 3.579545 MHz, dc levels as shown above.
— MC10319 clock at 14.31818 MHz (4x) asynchronous to input.
— Differential gain: p-p output @ each IRE level compared to that at 0 IRE.
— Differential phase: Phase @ each IRE level compared to that @ 0 IRE.

FIGURE 17 — MC10319



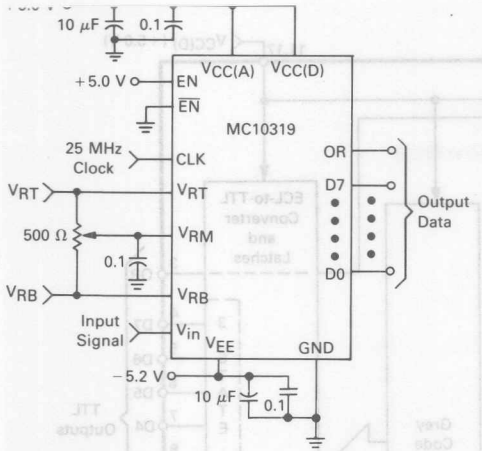


FIGURE 19 — CONVERSION SEQUENCE

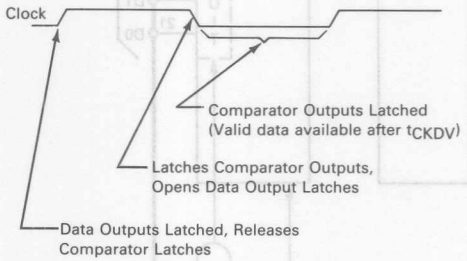
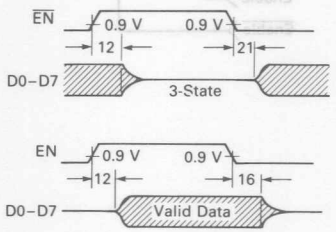
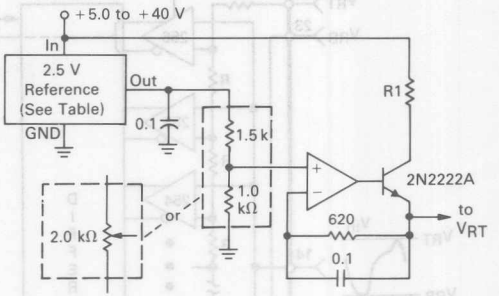


FIGURE 20 — ENABLE TO OUTPUT CRITICAL TIMING



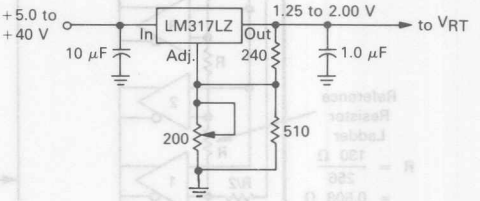
Timing @ D7–D0 measured where waveform starts to change.
Indicated time values are typical @ 25°C, and are in ns.

R1 = 100 Ω for +5.0 V
620 Ω for +15 V



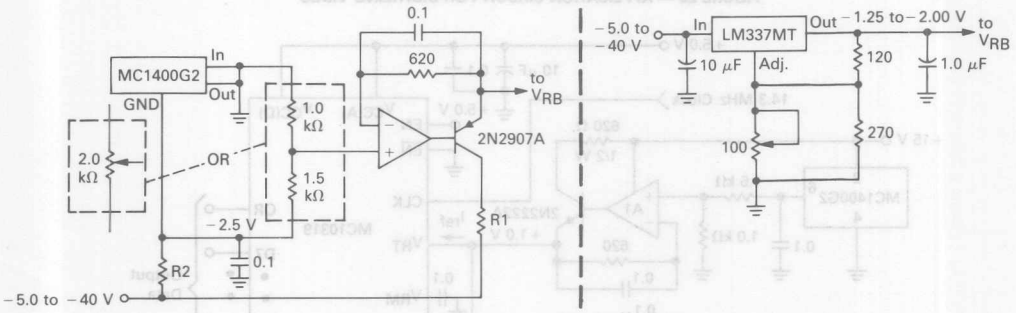
2.5 V References	MC1400G2	MC1403U	MC1403AU
Line Regulation	1.0 mV	0.5 mV	0.5 mV
T_C (ppm/°C) max	25	40	25
ΔV_{out} for 0–70°C	4.4 mV	7.0 mV	4.4 mV
Initial Accuracy	±0.2%	±1%	±1%

FIGURE 22 — V_{RT}, VOLTAGE SOURCE



LM317LZ	
Line Regulation	1.0 mV
T_C (ppm/°C) max	60
ΔV_{out} for 0–70°C	8.4 mV
Initial Accuracy	±4%

FIGURE 23 — V_{RB} VOLTAGE SOURCES



	MC1400G2	LM337MT
Line Regulation	1.0 mV	1.0 mV
T_C (ppm/°C) max	25	48
ΔV_{out} for 0–70°C	4.4 mV	6.7 mV
Initial Accuracy	±0.2%	±4%

R1 = 100 Ω for −5.0 V
620 Ω for −15 V
R2 = 620 Ω for −5.0 V
3.0 kΩ for −15 V

FIGURE 24 — COMPOSITE VIDEO WAVEFORM

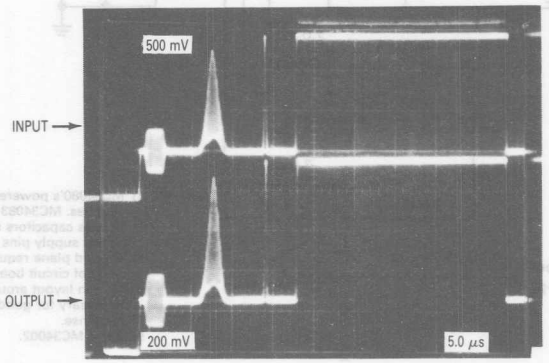


FIGURE 25 — SIN^2 X WAVEFORM

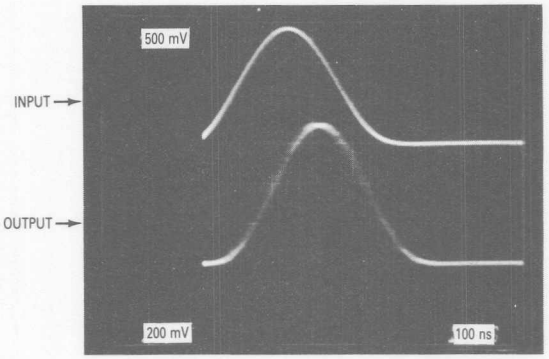
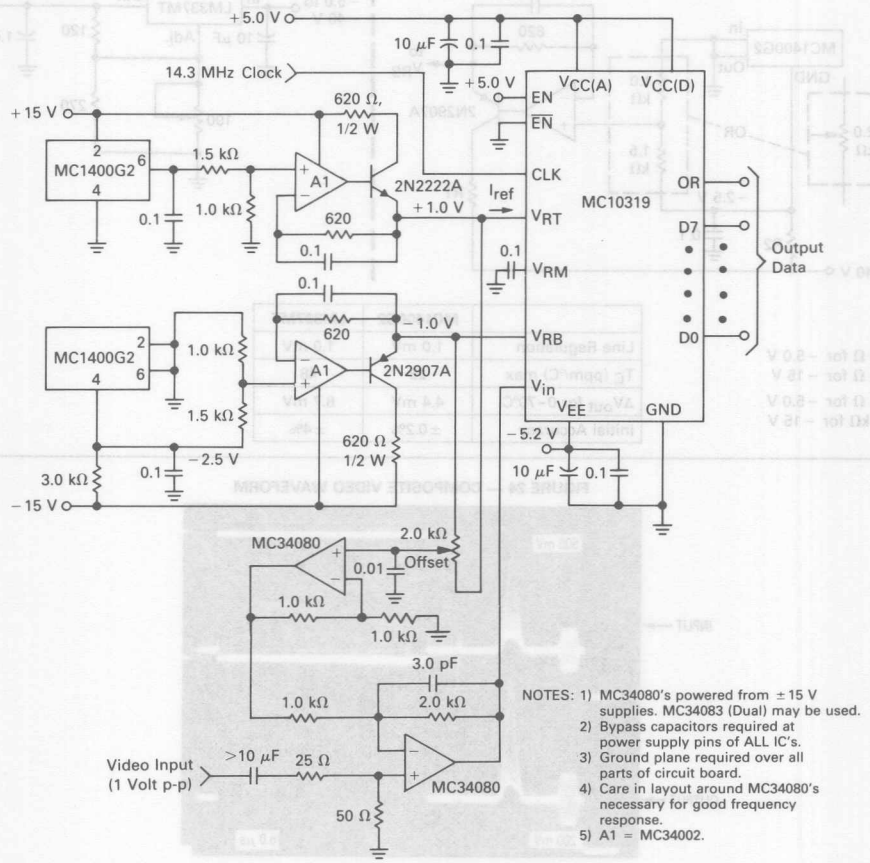
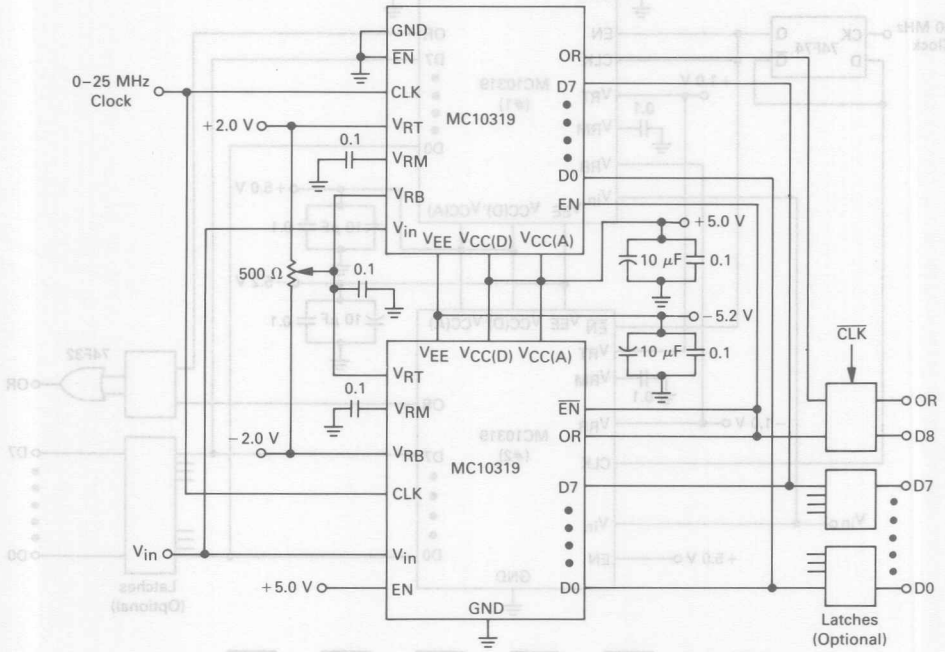


FIGURE 26 — APPLICATION CIRCUIT FOR DIGITIZING VIDEO



NOTES: 1) MC34080's powered from ±15 V supplies. MC34083 (Dual) may be used.
2) Bypass capacitors required at power supply pins of ALL IC's.
3) Ground plane required over all parts of circuit board.
4) Care in layout around MC34080's necessary for good frequency response.
5) A1 = MC34002.

FIGURE 27 — 9-BIT A/D CONVERTER



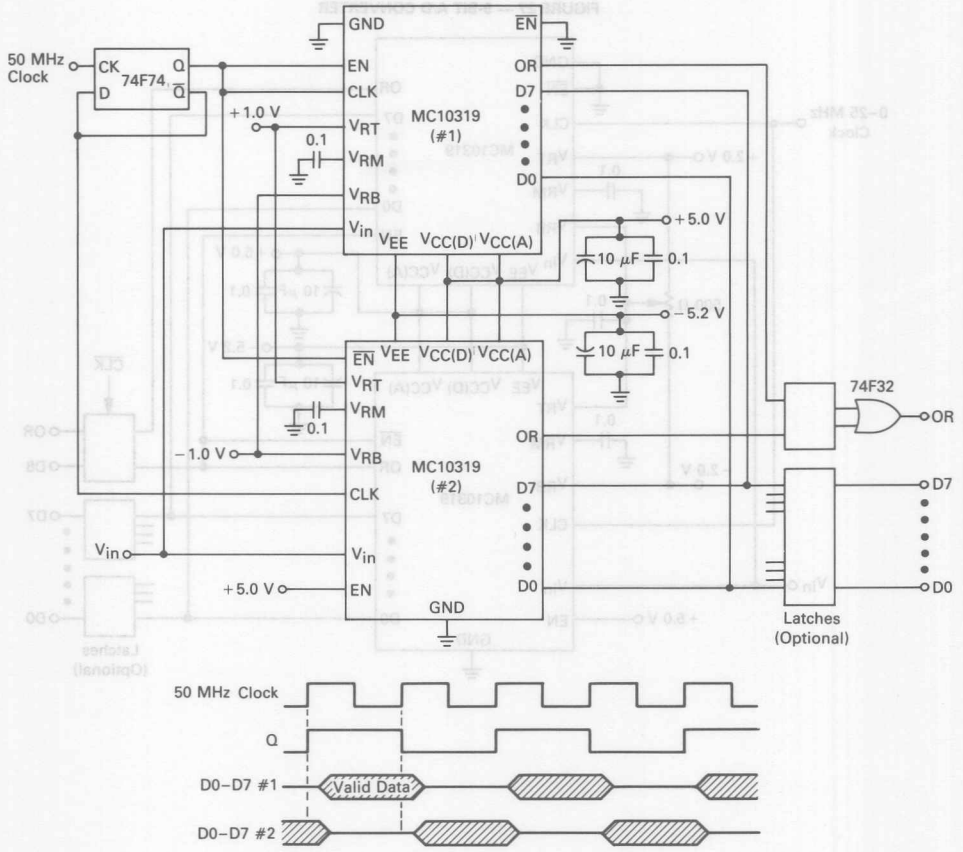
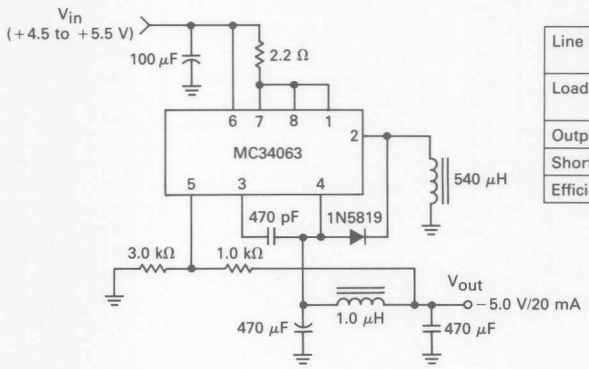


FIGURE 29 — −5.0 VOLT REGULATOR



Line Regulation	$4.5\ V < V_{in} < 5.5\ V$, $I_{out} = 10\ mA$	0.16%
Load Regulation	$V_{in} = 5.0\ V$, $8.0\ mA < I_{out} < 20\ mA$	0.4%
Output Ripple	$V_{in} = 5.0\ V$, $I_{out} = 20\ mA$	$2\ mV_{p-p}$
Short Circuit I_{out}	$V_{in} = 5.0\ V$, $R1 = 0.1\ \Omega$	140 mA
Efficiency	$V_{in} = 5.0\ V$, $I_{out} = 50\ mA$	52%

GLOSSARY

APERTURE DELAY — The time difference between the sampling signal (typically a clock edge) and the actual analog signal converted. The actual signal converted may occur before or after the sampling signal, depending on the internal configuration of the converter.

BIPOLAR INPUT — A mode of operation whereby the analog input (of an A-D), or output (of a DAC), includes both negative and positive values. Examples are −1.0 to +1.0 V, −5.0 to +5.0 V, −2.0 to +8.0 V, etc.

BIPOLAR OFFSET ERROR — The difference between the actual and ideal locations of the 00_H to 01_H transition, where the ideal location is 1/2 LSB above the most negative reference voltage.

BIPOLAR ZERO ERROR — The error (usually expressed in LSBs) of the input voltage location (of an A-D) of the 80_H to 81_H transition. The ideal location is 1/2 LSB above zero volts in the case of an A-D setup for a symmetrical bipolar input (e.g., −1.0 to +1.0 V).

DIFFERENTIAL NONLINEARITY — The maximum deviation in the actual step size (one transition level to another) from the ideal step size. The ideal step size is defined as the Full Scale Range divided by 2^n (n = number of bits). This error must be within ±1 LSB for proper operation.

ECL — Emitter coupled logic.

FULL SCALE RANGE (ACTUAL) — The difference between the actual minimum and maximum end points of the analog input (of an A-D).

FULL SCALE RANGE (IDEAL) — The difference between the actual minimum and maximum end points of the analog input (of an A-D), plus one LSB.

GAIN ERROR — The difference between the actual and expected gain (end point to end point), with respect to the reference, of a data converter. The gain error is usually expressed in LSBs.

GREY CODE — Also known as *reflected binary code,* it is a digital code such that each code differs from adjacent codes by only one bit. Since more than one bit is never changed at each transition, race condition errors are eliminated.

INTEGRAL NONLINEARITY — The maximum error of an A-D, or DAC, transfer function from the ideal straight line connecting the analog end points. This parameter is sensitive to dynamics, and test conditions must be specified in order to be meaningfull. This parameter is the best overall indicator of the device's performance.

LSB — Least Significant Bit. It is the lowest order bit of a binary code.

LINE REGULATION — The ability of a voltage regulator to maintain a certain output voltage as the input to the regulator is varied. The error is typically expressed as a percent of the nominal output voltage.

LOAD REGULATION — The ability of a voltage regulator to maintain a certain output voltage as the load current is varied. The error is typically expressed as a percent of the nominal output voltage.

MONOTONICITY — The characteristic of the transfer function whereby increasing the input code (of a DAC), or the input signal (of an A-D), results in the output never decreasing.

MSB — Most Significant Bit. It is the highest order bit of a binary code.

NATURAL BINARY CODE — A binary code defined by:

$$N = A_n2^n + \ldots + A_32^3 + A_22^2 + A_12^1 + A_02^0$$

where each "A" coefficient has a value of 1 or 0. Typically, all zeroes correspond to a zero input voltage of an A-D, and all ones correspond to the most positive input voltage.

NYQUIST THEORY — See Sampling Theorem.

OFFSET BINARY CODE — Applicable only to bipolar input (or output) data converters, it is the same as Natural Binary, except that all zeroes correspond to the most negative input voltage (of an A-D), while all ones correspond to the most positive input.

POWER SUPPLY SENSITIVITY — The change in a data converter's performance with changes in the power supply voltage(s). This parameter is usually expressed in percent of full scale versus ΔV.

QUANTITIZATION ERROR — Also known as digitization error or uncertainty. It is the inherent error involved in digitizing an analog signal due to the finite number of steps at the digital output versus the infinite number of values at the analog input. This error is a minimum of ±1/2 LSB.

RESOLUTION — The smallest change which can be discerned by an A-D converter, or produced by a DAC. It is usually expressed as the number of bits, n, where the converter has 2^n possible states.

SAMPLING THEOREM — Also known as the Nyquist Theorem. It states that the sampling frequency of an A-D must be no less than 2x the highest frequency (of interest) of the analog signal to be digitized in order to preserve the information of that analog signal.

UNIPOLAR INPUT — A mode of operation whereby the analog input range (of an A-D), or output range (of a DAC), includes values of a signal polarity. Examples are 0 to +2.0 V, 0 to −5.0 V, +2.0 to +8.0 V, etc.

UNIPOLAR OFFSET ERROR — The difference between the actual and ideal locations of the 00_H to 01_H transition, where the ideal location is 1/2 LSB above the most negative input voltage.

6

MOTOROLA

MC10321

Specifications and Applications Information

HIGH SPEED 7-BIT ANALOG-TO-DIGITAL FLASH CONVERTER

The MC10321 is a 7-bit high speed parallel flash A/D converter, which employs an internal Grey Code structure to eliminate large output errors on fast slewing input signals. It is fully TTL compatible, requiring a +5.0 volt supply, and a negative supply between −3.0 and −6.0 volts. Three-state TTL outputs allow direct connection to a data bus or common I/O memory.

The MC10321 contains 128 parallel comparators wired along a precision input reference network. The comparator outputs are fed to latches, and then to an encoder network which produces a 7-bit data byte, plus an overrange bit. The data is latched and converted to three-state LSTTL levels. Enable inputs permit setting the outputs to a three-state condition. The overrange bit is always active to allow for sensing of the overrange condition, and to ease the interconnection of two MC10321s into an 8-bit configuration.

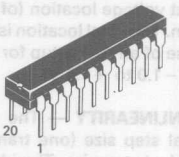
The MC10321 is available in a 20-pin standard plastic and SOIC packages.

Applications include Video displays (digital TV, picture-in-picture, special effects), radar processing, high speed instrumentation, and TV broadcast.

- Internal Grey Code for Speed and Accuracy
- 25 MHz Sampling Rate
- 7-Bit Resolution with 8-Bit Accuracy
- Easily Cascadable into an 8-Bit System
- Three-State LSTTL Outputs with True and Complement Enable Inputs
- Low Input Capacitance: 25 pF
- No Clock Kick-Out Currents on Input or Reference
- Wide Input Range: 1.0–2.1 Volts within a ±2.1 Volt Range
- No Sample and Hold Required for Video Applications
- Edge Triggered Conversion — No Pipeline Delay
- True and Complement Enable Inputs for Three-State Control
- Standard DIP and Surface Mount Packages Available
- Operating Temperature Range: −40° to +85°C

HIGH SPEED 7-BIT ANALOG-TO-DIGITAL FLASH CONVERTER

SILICON MONOLITHIC INTEGRATED CIRCUIT



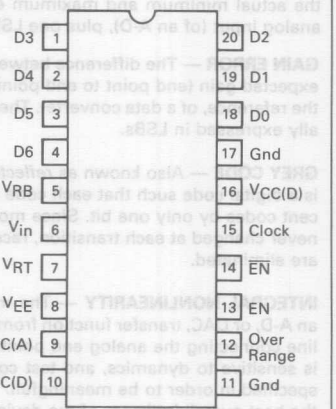
P SUFFIX
PLASTIC PACKAGE
CASE 738-03



DW SUFFIX
PLASTIC PACKAGE
CASE 751D-03
SO-20

PIN CONNECTIONS

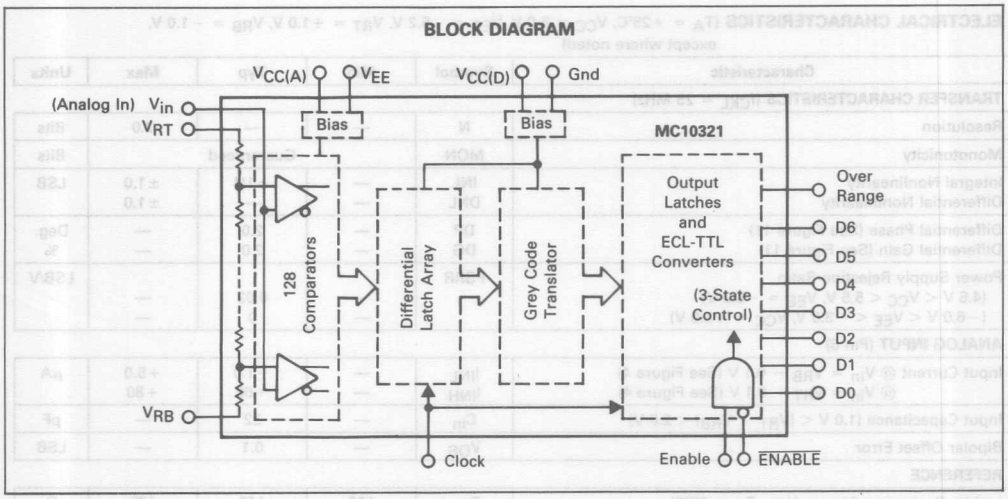
(Top View)



ORDERING INFORMATION

Device	Temperature Range	Package
MC10321P	−40° to +85°C	Plastic DIP
MC10321DW		SO-20

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Supply Voltage	$V_{CC(A)}$, $V_{CC(D)}$ V_{EE}	+7.0 −7.0	Vdc
Positive Supply Voltage Differential	$V_{CC(D)}-V_{CC(A)}$	−0.3, +0.3	Vdc
Digital Input Voltage (Pins 13–15)	$V_{I(D)}$	−0.5, +7.0	Vdc
Analog Input Voltage (Pins 5, 6, 7)	$V_{I(A)}$	−2.5, +2.5	Vdc
Reference Voltage Span (Pin 7–Pin 5)	—	+2.3	Vdc
Applied Output Voltage (D0–D6 in 3-State)	—	−0.3, +7.0	Vdc
Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	−65, +150	°C

Devices should not be operated at these values. The "Recommended Operating Limits" provide guidelines for actual device operation.

RECOMMENDED OPERATING LIMITS

Parameter	Symbol	Min	Typ	Max	Units
Power Supply Voltage (Pin 9) Power Supply Voltage (Pins 10, 16) $V_{CC(D)}-V_{CC(A)}$	$V_{CC(A)}$ $V_{CC(D)}$ ΔV_{CC}	+4.5 +4.5 −0.1	+5.0 +5.0 0	+5.5 +5.5 +0.1	Vdc
Power Supply Voltage (Pin 8)	V_{EE}	−6.0	−5.0	−3.0	Vdc
Digital Input Voltages (Pins 13–15)	—	0	—	$V_{CC(D)}$	Vdc
Analog Input (Pin 6)	V_{in}	−2.1	—	+2.1	Vdc
Voltage @ V_{RT} (Pin 7) @ V_{RB} (Pin 5) $V_{RT}-V_{RB}$ $V_{RB}-V_{EE}$	V_{RT} V_{RB} ΔV_R —	−1.0 −2.1 +1.0 1.3	— — — —	+2.1 +1.0 +2.1 —	Vdc
Applied Output Voltage (Pins D0–D6 in 3-State)	V_O	0	—	$V_{CC(D)}$	Vdc
Clock Pulse Width — High — Low	t_{CKH} t_{CKL}	5.0 15	— —	— —	ns
Clock Frequency	f_{CLK}	0	—	25	MHz
Operating Ambient Temperature	T_A	−40	—	+85	°C

All limits are not necessarily functional concurrently.

except where noted)

Characteristic	Symbol	Min	Typ	Max	Units
TRANSFER CHARACTERISTICS (f_{CKL} = 25 MHz)					
Resolution	N	—	—	7.0	Bits
Monotonicity	MON		Guaranteed		Bits
Integral Nonlinearity Differential Nonlinearity	INL DNL	— —	±1/4 —	±1.0 ±1.0	LSB
Differential Phase (See Figure 11) Differential Gain (See Figure 11)	DP DG	— —	2.0 2.0	— —	Deg. %
Power Supply Rejection Ratio (4.5 V < V_{CC} < 5.5 V, V_{EE} = −5.2 V) (−6.0 V < V_{EE} < −3.0 V, V_{CC} = +5.0 V)	PSRR	 — —	 0.02 0	 — —	LSB/V
ANALOG INPUT (Pin 6)					
Input Current @ V_{in} = V_{RB} − 0.1 V (See Figure 4) @ V_{in} = V_{RT} + 0.1 V (See Figure 4)	I_{INL} I_{INH}	— —	+1.0 +60	+5.0 +80	μA
Input Capacitance (1.0 V < (V_{RT} − V_{RB}) < 2.0 V)	C_{in}	—	22	—	pF
Bipolar Offset Error	V_{OS}	—	0.1	—	LSB
REFERENCE					
Ladder Resistance (V_{RT} to V_{RB}, T_A = 25°C)	R_{ref}	100	140	175	Ω
Temperature Coefficient	T_C	—	+0.29	—	%/°C
Ladder Capacitance (Pin 1 Open)	C_{ref}	—	5.0	—	pF
ENABLE INPUTS (V_{CC} = 5.5 V)					
Input Voltage — High — Low	V_{IHE} V_{ILE}	2.0 —	— —	— 0.8	V
Input Current @ 2.4 Volts (See Figure 5) @ 0.4 Volts (See Figure 5)	I_{IHE} I_{ILE}	— −200	+0.2 −120	2.0 —	μA
Input Clamp Voltage (I_{IK} = −18 mA)	V_{IKE}	−1.5	−1.3	—	V
CLOCK INPUT (V_{CC} = 5.5 V)					
Input Voltage — High — Low	V_{IHC} V_{ILC}	2.0 —	— —	— 0.8	Vdc
Input Current @ 0.4 V (See Figure 6) @ 2.7 V (See Figure 6)	I_{ILC} I_{IHC}	−150 −80	−80 −40	— —	μA
Input Clamp Voltage (I_{IK} = −18 mA)	V_{IKC}	−1.5	−1.3	—	Vdc
DIGITAL OUTPUTS					
High Output Voltage (I_{OH} = −400 μA @ D6–D0, OR, V_{CC} = 4.5 V, See Figure 7)	V_{OH}	2.4	3.0	—	V
Low Output Voltage (I_{OL} = 4.0 mA @ D6–D0, OR, V_{CC} = 4.5 V, See Figure 8)	V_{OL}	—	0.3	0.4	V
Output Short Circuit Current* (D6–D0, OR, V_{CC} = 5.5 V)	I_{SC}	—	−35	—	mA
Output Leakage Current (0.4 < V_O < 2.4 V, See Figure 3, V_{CC} = 5.5 V, D0–D6 in 3-State Mode)	I_{LK}	−10	—	+10	μA
Output Capacitance (D0–D6 in 3-State Mode)	C_{out}	—	5.0	—	pF

*Only one output to be shorted at a time, not to exceed 1 second.

POWER SUPPLIES					
$V_{CC(A)}$ Current (4.5 V < $V_{CC(A)}$ < 5.5 V, Outputs Unloaded) $V_{CC(D)}$ Current (4.5 V < $V_{CC(D)}$ < 5.5 V, Outputs Unloaded) V_{EE} Current (−6.0 V < V_{EE} < −3.0 V)	$I_{CC(A)}$ $I_{CC(D)}$ I_{EE}	10 40 −16	13 60 −13	16 80 −8.0	mA
Power Dissipation (V_{RT} − V_{RB} = 2.0 V, Outputs Unloaded)	P_D	—	459	668	mW

TIMING CHARACTERISTICS (T_A = 25°C, V_{CC} = +5.0 V, V_{EE} = −5.2 V, V_{RT} = +1.0 V, V_{RB} = −1.0 V, See System Timing Diagram)

Parameter	Symbol	Min	Typ	Max	Units
INPUTS					
Min Clock Pulse Width — High — Low	t_{CKH} t_{CKL}	— —	5.0 15	— —	ns
Max Clock Rise, Fall Time	$t_{R,F}$	—	100	—	ns
Clock Frequency	f_{CLK}	0	30	25	MHz
OUTPUTS					
New Data Valid from Clock Low	t_{CKDV}	—	22	—	ns
Aperture Delay	t_{AD}	—	3.0	—	ns
Hold Time	t_H	—	6.0	—	ns
Data High to 3-State from Enable Low*	t_{EHZ}	—	22	—	ns
Data Low to 3-State from Enable Low*	t_{ELZ}	—	17	—	ns
Data High to 3-State from $\overline{\text{ENABLE}}$ High*	$t_{E'HZ}$	—	27	—	ns
Data Low to 3-State from $\overline{\text{ENABLE}}$ High*	$t_{E'LZ}$	—	19	—	ns
Valid Data from Enable High (Pin 14 = 0 V)*	t_{EDV}	—	13	—	ns
Valid Data from $\overline{\text{ENABLE}}$ Low (Pin 13 = 5.0 V)*	$t_{E'DV}$	—	20	—	ns
Output Transition Time (10%–90%)*	t_{tr}	—	6.0	—	ns

*See Figure 2 for output loading.

TEMPERATURE CHARACTERISTICS

Parameter	Typical Value @ 25°C	Typical Change −40 to +85°C
I_{CC} (+5.0 V Supply Current)	73 mA	−100 μA/°C
I_{EE} (−5.2 V Supply Current)	−13 mA	+7.0 μA/°C
Ladder Resistance	140 Ω	+0.29%/°C
V_{OL} (Output Low Voltage @ 4.0 mA)	0.3 V	+8.0 μV/°C
V_{OH} (Output High Voltage @ −400 μA)	3.0 V	2.1 mV/°C
Differential Nonlinearity	—	−0.0008 LSB/°C
Integral Nonlinearity	0.25 LSB	−0.001 LSB/°C

PIN DESCRIPTIONS

Symbol	Pin	Description
GND	11,17	Power supply ground. The two pins should be connected directly together, and through a low impedance path to the power supply.
OR	12	Overrange output. Indicates V_{in} is more positive than V_{RT}-1/2 LSB. This output does not have 3-state capability, and therefore is always active.
D6–D0	1–4, 18–20	Digital Outputs. D6 (Pin 4) is the MSB, D0 (Pin 18) is the LSB. LSTTL compatible with 3-state capability.
$V_{CC(D)}$	10,16	Power supply for the digital section. +5.0 V, ±10% required.
V_{EE}	8	Negative Power supply. Nominally −5.2 V, it can range from −3.0 to −6.0 V, and must be more negative than V_{RB} by >1.3 V.
V_{in}	6	Signal voltage input. This voltage is compared to the reference to generate a digital equivalent. Input impedance is nominally 16–33 kΩ (See Figure 4) in parallel with 22 pF.

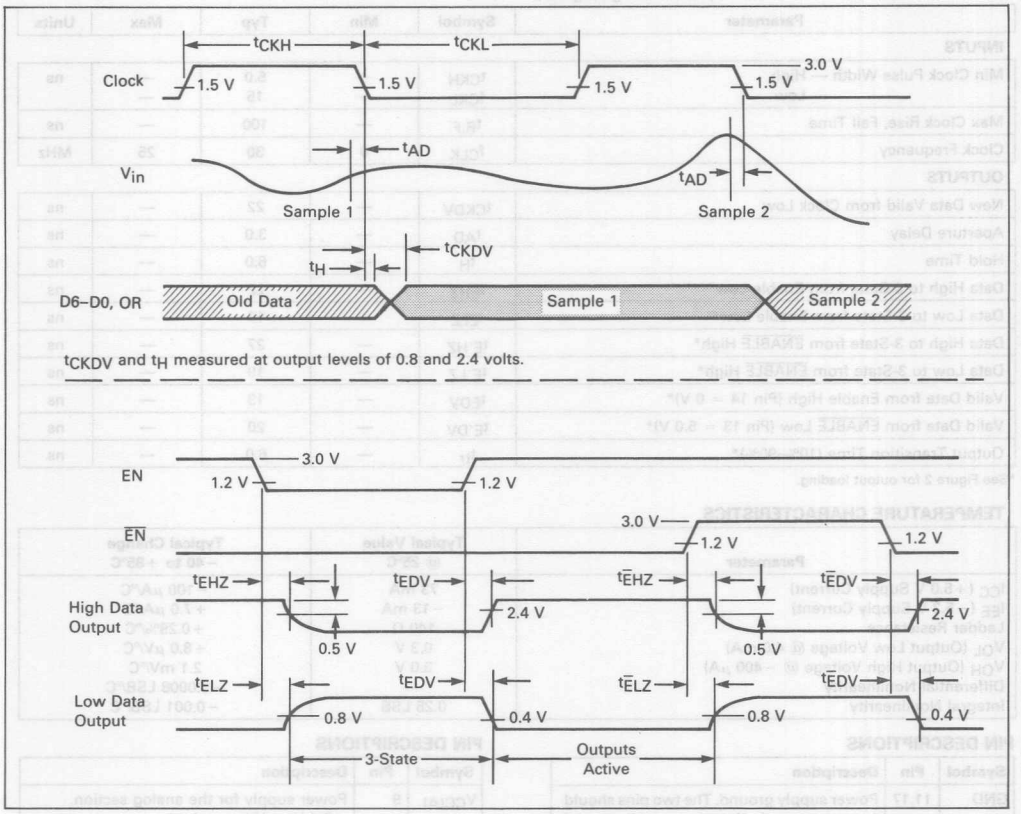
PIN DESCRIPTIONS

Symbol	Pin	Description
$V_{CC(A)}$	9	Power supply for the analog section. +5.0 V, ±10% required.
CLK	15	Clock input, TTL compatible, and can range from dc to 25 MHz. Conversion occurs on the negative edge of the clock.
EN	13	Enable input. TTL compatible, a Logic "1" (and Pin 14 a Logic "0") enables the data outputs. A Logic "0" sets the outputs (except Overrange) to a 3-state mode.
$\overline{\text{EN}}$	14	$\overline{\text{ENABLE}}$ input. TTL compatible, a Logic "0" (and Pin 13 a Logic "1") enables the data outputs. A Logic "1" sets the outputs (except Overrange) to a 3-state mode.
V_{RB}	5	The bottom (most negative point) of the internal reference resistor ladder. The ladder resistance is typically 140 Ω to V_{RT}.
V_{RT}	7	The top (most positive point) of the internal reference resistor ladder.

Pin assignments are the same for the standard DIP package and the surface mount package.

6

FIGURE 1 — SYSTEM TIMING DIAGRAM



6

FIGURE 2 — DATA OUTPUT TEST CIRCUIT

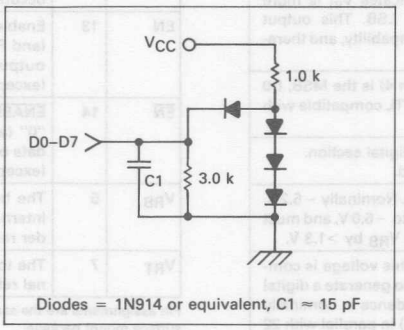


FIGURE 3 — OUTPUT 3-STATE LEAKAGE CURRENT

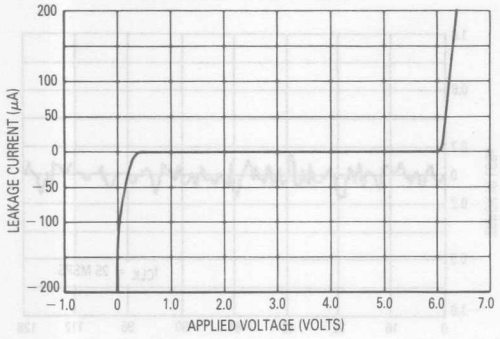


FIGURE 4 — INPUT CURRENT @ V_{in}

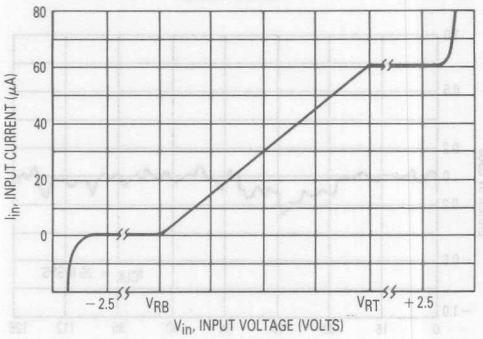


FIGURE 5 — INPUT CURRENT AT ENABLE, $\overline{\text{ENABLE}}$

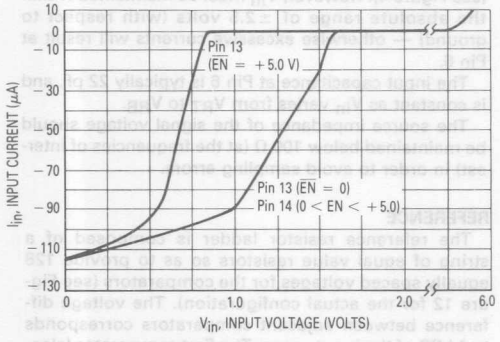


FIGURE 6 — CLOCK INPUT CURRENT

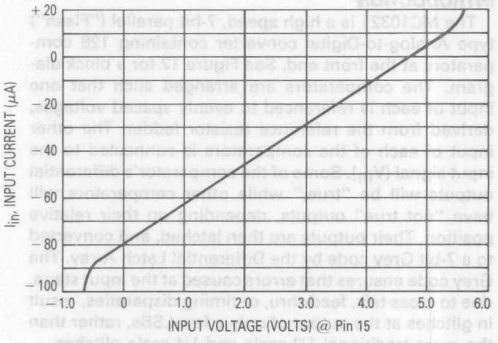


FIGURE 7 — OUTPUT VOLTAGE versus OUTPUT CURRENT

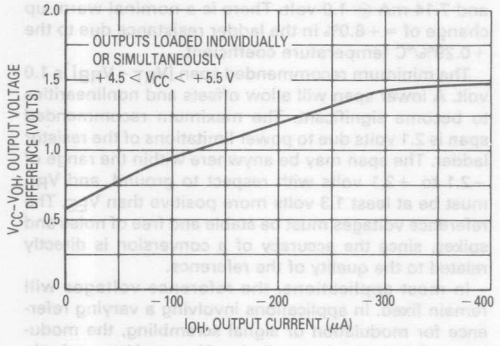
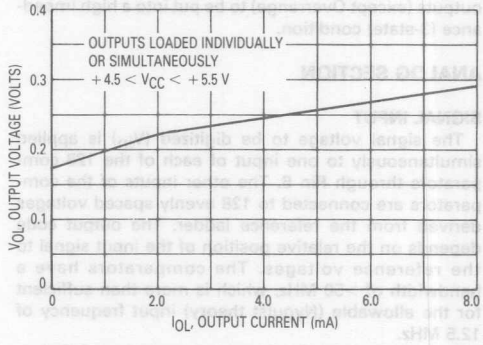
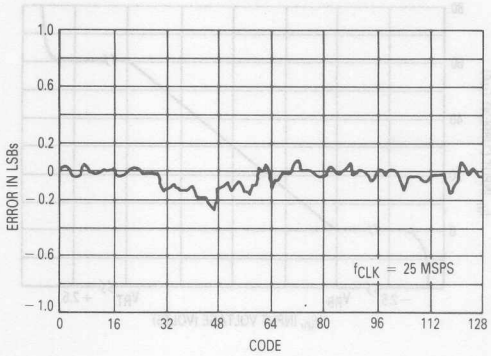


FIGURE 8 — OUTPUT VOLTAGE versus OUTPUT CURRENT

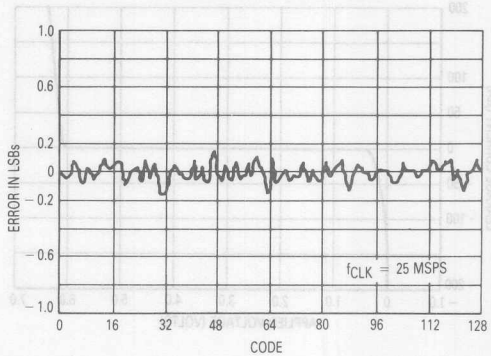


6

versus CODE



IN LSBs versus LOWER CODE



DESIGN GUIDELINES

6

INTRODUCTION

The MC10321 is a high speed, 7-bit parallel ("Flash") type Analog-to-Digital converter containing 128 comparators at the front end. See Figure 12 for a block diagram. The comparators are arranged such that one input of each is referenced to evenly spaced voltages, derived from the reference resistor ladder. The other input of each of the comparators is connected to the input signal (V_{in}). Some of the comparator's differential outputs will be "true," while other comparators will have "not true" outputs, depending on their relative position. Their outputs are then latched, and converted to a 7-bit Grey code by the Differential Latch Array. The Grey code ensures that errors caused at the input stage, due to cross talk, feed-thru, or timing disparaties, result in glitches at the output of only a few LSBs, rather than the more traditional 1/2 scale and 1/4 scale glitches.

The Grey code is then translated to a 7-bit binary code, and the differential levels are translated to TTL levels before being applied to the output latches. ENABLE inputs (EN and $\overline{EN}$) at this final stage permit the TTL outputs (except Overrange) to be put into a high impedance (3-state) condition.

ANALOG SECTION

SIGNAL INPUT

The signal voltage to be digitized (V_{in}) is applied simultaneously to one input of each of the 128 comparators through Pin 6. The other inputs of the comparators are connected to 128 evenly spaced voltages derived from the reference ladder. The output code depends on the relative position of the input signal to the reference voltages. The comparators have a bandwidth of >50 MHz, which is more than sufficient for the allowable (Nyquist theory) input frequency of 12.5 MHz.

The current into Pin 6 varies linearly from 0 (when $V_{in} = V_{RB}$) to ≈60 μA (when $V_{in} = V_{RT}$). If V_{in} is taken below V_{RB} or above V_{RT}, the input current will remain at the value corresponding to V_{RB} and V_{RT} respectively (see Figure 4). However, V_{in} must be maintained within the absolute range of ±2.5 volts (with respect to ground) — otherwise excessive currents will result at Pin 6.

The input capacitance at Pin 6 is typically 22 pF, and is constant as V_{in} varies from V_{RT} to V_{RB}.

The source impedance of the signal voltage should be maintained below 100 Ω (at the frequencies of interest) in order to avoid sampling errors.

REFERENCE

The reference resistor ladder is composed of a string of equal value resistors so as to provide 128 equally spaced voltages for the comparators (see Figure 12 for the actual configuration). The voltage difference between adjacent comparators corresponds to 1 LSB of the input range. The first comparator (closest to V_{RB}) is referenced 1/2 LSB above V_{RB}, and the 128th comparator (for the overrange) is referenced 1/2 LSB below V_{RT}. The total resistance of the ladder is nominally 140 Ω, ±25%, requiring 14.3 mA @ 2.0 volts and 7.14 mA @ 1.0 volt. There is a nominal warm up change of ≈ +8.0% in the ladder resistance due to the +0.29%/°C temperature coefficient.

The minimum recommended span [$V_{RT} - V_{RB}$] is 1.0 volt. A lower span will allow offsets and nonlinearities to become significant. The maximum recommended span is 2.1 volts due to power limitations of the resistor ladder. The span may be anywhere within the range of −2.1 to +2.1 volts with respect to ground, and V_{RB} must be at least 1.3 volts more positive than V_{EE}. The reference voltages must be stable and free of noise and spikes, since the accuracy of a conversion is directly related to the quality of the reference.

In most applications, the reference voltages will remain fixed. In applications involving a varying reference for modulation or signal scrambling, the modulating signal may be applied to V_{RT}, or V_{RB}, or both. The output will vary inversely with the reference signal, introducing a nonlinearity into the transfer function. The addition of the modulating signal and the dc level

applied to the reference must be such that the absolute voltage at V_{RT} and V_{RB} are maintained within the values listed in the Recommended Operating Limits. The RMS value of the span must be maintained ≤2.1 volts.

POWER SUPPLIES

$V_{CC(A)}$ (Pin 9) is the positive power supply for the comparators, and $V_{CC(D)}$ (Pins 10, 16) is the positive power supply for the digital portion. Both are to be +5.0 volts, ±10%, and the two are to be within 100 millivolts of each other. There is indirect internal coupling between $V_{CC(D)}$ and $V_{CC(A)}$. If they are powered separately, and one supply fails, there will be current flow through the MC10321 to the failed supply.

$I_{CC(A)}$ is nominally 13 mA, and does not vary with clock frequency or with V_{in}, but does vary slightly with $V_{CC(A)}$. $I_{CC(D)}$ is nominally 60 mA, and is independent of clock frequency. It does vary, however, by 4–5 mA as V_{in} is varied from V_{RT} to V_{RB}, and varies directly with $V_{CC(D)}$.

V_{EE} is the negative power supply for the comparators, and is to be within the range −3.0 to −6.0 volts. Additionally, V_{EE} must be at least 1.3 volts more negative than V_{RB}. I_{EE} is a nominal −13 mA, and is independent of clock frequency, V_{in} and V_{EE}.

For proper operation, the supplies **must** be bypassed **at the IC.** A 10 μF tantalum, in parallel with a 0.1 μF ceramic is recommended for each supply to ground.

DIGITAL SECTION

CLOCK

The Clock input (Pin 15) is TTL compatible with a typical frequency range of 0 to 30 MHz. There is no duty cycle limitation, but the minimum low and high times must be adhered to. See Figure 6 for the input current requirements.

The conversion sequence is shown in Figure 13, and is as follows:

— On the rising edge, the data output latches are latched with old data, and the comparator output latches are released to follow the input signal (V_{in}).

— During the high time, the comparators track the input signal. The data output latches retain the old data.

— On the falling edge, the comparator outputs are latched with the data immediately prior to this edge. The conversion to digital occurs within the device, and the data output latches are released to indicate the new data in ≈22 ns.

— During the clock low time, the comparator outputs remain latched, and the data output latches remain transparent.

A summary of the sequence is that data present at V_{in} just prior to the Clock falling edge is digitized and available at the data outputs immediately after that same falling edge. The minimum amount of time the data must be present prior to the clock falling edge (aperture delay) is 2.0–6.0 ns, typically 3.0 ns.

The comparator output latches provide the circuit with an effective sample-and-hold function, eliminating the need for an external sample-and-hold.

ENABLE INPUTS

The two Enable inputs (Pins 13, 14) are TTL compatible, and are used to change the data outputs (D6–D0) from active to 3-state. This capability allows cascading two MC10321s into an 8-bit configuration, connecting the outputs directly to a data bus, multiplexing multiple converters, etc. See the Applications Information section for more details. For the outputs to be active, Pin 13 must be Logic "1," and Pin 14 must be a Logic "0." Changing either input will put the outputs into the high impedance mode. The Enable inputs affect **only** the state of the outputs — they do not inhibit a conversion. Both pins have a nominal threshold of ≈1.2 volts, their input currents are shown in Figure 5, and their input-output timing is shown in Figure 1 and 14. Leaving either pin open is equivalent to a Logic "1," although good design practice dictates that an input should never be left open.

The Overrange output (Pin 12) is not affected by the Enable inputs as it does not have 3-state capability.

OUTPUTS

The data outputs (Pins 1–4, 12, 18–20) are TTL level outputs with high impedance capability (except Overrange). Pin 4 is the MSB (D6), and Pin 18 is the LSB (D0). The seven outputs are active as long as the Enable inputs are true (EN = high, $\overline{EN}$ = low). The timing of the outputs relative to the Clock input and the Enable inputs is shown in Figures 1 and 14. Figures 7 and 8 indicate the output voltage versus load current, while Figure 3 indicates the leakage current when in the high impedance mode.

The output code is natural binary, depicted in Table 1.

The Overrange output (Pin 12) goes high when the input, V_{in}, is more positive than V_{RT} − 1/2 LSB. This output is always active — it does not have high impedance capability. Besides used to indicate an input overrange, it is additionally used for cascading two MC10321s to form an 8-bit A/D converter (see Figure 21).

TABLE 1

Input	V_{RT}, V_{RB} (Volts)			Output Code	Overrange
	2.048, 0	+1.0 V, −1.0 V	+1.0 V, 0 V		
$>V_{RT}$ − 1/2 LSB	>2.040 V	>0.9922 V	>0.9961 V	$7F_H$	1
V_{RT} − 1/2 LSB	2.040 V	0.9922 V	0.9961 V	$7F_H$	0 ↔ 1
V_{RT} − 1 LSB	2.032 V	0.9844 V	0.9922 V	$7F_H$	0
V_{RT} − 1 1/2 LSB	2.024 V	0.9766 V	0.9883 V	$7E_H \leftrightarrow 7F_H$	0
Midpoint	1.024 V	0.000 V	0.5000 V	40_H	0
V_{RB} + 1/2 LSB	8.0 mV	−0.9922 V	3.9 mV	$00_H \leftrightarrow 01_H$	0
$< V_{RB}$ + 1/2 LSB	<8.0 mV	<−0.9922 V	<3.9 mV	00_H	0

APPLICATIONS INFORMATION

POWER SUPPLIES, GROUNDING

The PC board layout, and the quality of the power supplies and the ground system **at the IC** are very important in order to obtain proper operation. Noise, from any source, coming into the device on V_{CC}, V_{EE}, or ground can cause an incorrect output code due to interaction with the analog portion of the circuit. At the same time, noise generated within the MC10321 can cause incorrect operation if that noise does not have a clear path to ac ground.

Both the V_{CC} and V_{EE} power supplies must be decoupled to ground **at the IC** (within 1" max) with a 10 μF tantalum and a 0.1 μF ceramic. Tantalum capacitors are recommended since electrolytic capacitors simply have too much inductance at the frequencies of interest. The quality of the V_{CC} and V_{EE} supplies should then be checked at the IC with a high frequency scope. Noise spikes (always present when digital circuits are present) can easily exceed 400 mV peak, and if they get into the analog portion of the IC, the operation can be disrupted. Noise can be reduced by inserting resistors and/or inductors between the supplies and the IC.

If switching power supplies are used, there will usually be spikes of 0.5 volts or greater at frequencies of 50–200 kHz. These spikes are generally more difficult to reduce because of their greater energy content. In extreme cases, 3-terminal regulators (MC78L05ACP, MC7905.2CT), with appropriate high frequency filtering, should be used and dedicated to the MC10321.

The ripple content of the supplies should not allow their magnitude to exceed the values in the Recommended Operating Limits.

The PC board tracks supplying V_{CC} and V_{EE} to the MC10321 should preferably not be at the tail end of the bus distribution, after passing through a maze of digital circuitry. The MC10321 should be close to the power supply, or the connector where the supply voltages enter the board. If the V_{CC} and V_{EE} lines are supplying considerable current to other parts of the boards, then it is preferable to have dedicated lines from the supply or connector directly to the MC10321.

The two ground pins (11, 17) must be connected directly together. Any long path between them can cause stability problems due to the inductance (@ 25 MHz) of the PC tracks. The ground return for the signal source must be noise free.

REFERENCE VOLTAGE CIRCUITS

Since the accuracy of the conversion is directly related to the quality of the references, it is imperative that accurate and stable voltages be provided to V_{RT} and V_{RB}. If the reference span is 2.0 volts, then 1/2 LSB is only 7.8 millivolts, and it is desireable that V_{RT} and V_{RB} be accurate to within this amount, and furthermore, that they do not drift more than this amount once set. Over the temperature range of −40 to +85°C, a maximum temperature coefficient of 31 ppm/°C is required.

The voltage supplies used for digital circuits should preferably **not** be used as a source for generating V_{RT} and V_{RB}, due to the noise spikes (up to 500 mV) present on the supplies and on their ground lines. Generally ±15 volts, or ±12 volts, are available for analog circuits, and are usually clean compared to supplies used for digital circuits, although ripple may be present in varying amounts. Ripple is easier to filter out than spikes, however, and so these supplies are preferred.

Figure 15 depicts a circuit which can provide an extremely stable voltage to V_{RT} **at the current required** (the maximum reference current is 20 mA @ 2.0 volts). The MC1403 series of references have very low temperature coefficients, good noise rejection, and a high initial accuracy, allowing the circuit to be built without an adjustment pot if the V_{RT} voltage is to remain fixed at one value. Using 0.1% wirewound resistors for the divider provides sufficient accuracy and stability in many cases. Alternately, resistor networks provide high ratio accuracies, and close temperature tracking. If the application requires V_{RT} to be changed periodically, the two resistors can be replaced with a 20 turn, cermet potentiometer. Wirewound potentiometers should not be used for this type of application since the pot's slider jumps from winding to winding, and an exact setting can be difficult to obtain. Cermet pots allow for a smooth continuous adjustment.

In Figure 15, R1 reduces the power dissipation in the transistor, and can be carbon composition. The 0.1 μF capacitor in the feedback path provides stability in the unity gain configuration. Recommended op amps are: LM358, MC34001 series, LM308A, LM324, and LM11C. Offset drift is the key parameter to consider in choosing an op amp, and the LM308A has the lowest drift of those mentioned. Bypass capacitors are not shown in Figure 15, but should always be provided at the input to the 2.5 volt reference, and at the power supply pins of the op amp.

Figure 16 shows a simpler and more economical circuit, using the LM317LZ regulator, but with lower initial accuracy and temperature stability. The op amp/current booster is not needed since the LM317LZ can supply the current directly. In a well controlled environment, this circuit will suffice for many applications. Because of the lower initial accuracy, an adjustment pot is a necessity.

Figure 17 shows two circuits for providing the voltage to V_{RB}. The circuits are similar to those of Figures 15 and 16, and have similar accuracy and stability. The MC1403 reference is used in conjunction with an op amp configured as an inverter, providing the negative voltage. The output transistor is a PNP in this case since the circuit must sink the reference current.

VIDEO APPLICATIONS

The MC10321 is suitable for digitizing video signals directly without signal conditioning, although the standard 1.0 volt p-p video signal can be amplified to a 2.0 volt p-p signal for slightly better accuracy. Figure 18 shows the input (top trace) and reconstructed output of a standard NTSC test signal, sampled at 25 MSPS, consisting of a sync pulse, 3.58 MHz color burst, a 3.58 MHz signal in a Sin^2x envelope, a pulse, a white level signal, and a black level signal. Figure 19 shows a Sin^2x pulse that has been digitized and reconstructed at 25 MSPS. The width of the pulse is ≈225 ns at the base. Figure 20 shows an application circuit for digitizing video.

8-BIT A/D CONVERTER

Figure 21 shows how two MC10321s can be connected to form an 8-bit converter. In this configuration, the outputs (D6–D0) of the two 7-bit converters are paralleled. The outputs of one device are active, while the outputs of other are in the 3-state mode. The selection is made by the OVERRANGE output of the lower MC10321, which controls Enable inputs on the two devices. Additionally, this output provides the 8th bit.

The reference ladders are connected in series, providing the 256 steps required for 8 bits. The input voltage range is determined by V_{RT} of the upper MC10321, and V_{RB} of the lower device. A minimum of 1.0 volt is required across each converter. The 500 Ω pot (20 turn cermet) allows for adjustment of the midpoint since the reference resistors of the two MC10321s may not be identical in value. Without the adjustment, a nonequal voltage division could occur, resulting in a nonlinear conversion. If the references are to be symmetrical about ground (e.g., ±1.0 volt or ±2.0 volts), the adjustment can be eliminated, and the midpoint connected to ground.

The use of latches on the outputs is optional, depending on the application. If latches are required, SN74LS173As are recommended.

50 MHz, 7 BIT A/D CONVERTER

Figure 22 shows how two MC10321s can be connected together in a flip-flop arrangement in order to have an effective conversion speed of 50 MHz. The 74F74D-type flip-flop provides a 25 MHz clock to each converter, and at the same time, controls the SELECT input to the MC74F257 multiplexers to alternately select the outputs of the two converters. A brief timing diagram is shown in the figure.

NEGATIVE VOLTAGE REGULATOR

In the cases where a negative power supply is not available — neither the −3.0 to −6.0 volts, nor a higher negative voltage from which to derive it — the circuit of Figure 23 can be used to generate −5.0 volts from the +5.0 volts supply. The PC board space required is small (≈2.0 in^2), and it can be located physically close to the MC10321. The MC34063 is a switching regulator, and in Figure 23 is configured in an inverting mode of operation. The regulator operating specifications are given in the figure.

6

GLOSSARY

APERTURE DELAY — The time difference between the sampling signal (typically a clock edge) and the actual analog signal converted. The actual signal converted may occur before or after the sampling signal, depending on the internal configuration of the converter.

BIPOLAR INPUT — A mode of operation whereby the analog input (of an A-D), or output (of a DAC), includes both negative and positive values. Examples are −1.0 to +1.0 V, −5.0 to +5.0 V, −2.0 to +8.0 V, etc.

BIPOLAR OFFSET ERROR — The difference between the actual and ideal locations of the 00_H to 01_H transition, where the ideal location is 1/2 LSB above the most negative reference voltage.

BIPOLAR ZERO ERROR — The error (usually expressed in LSBs) of the input voltage location (of a 7-bit A/D) of the 40_H to 41_H transition. The ideal location is 1/2 LSB above zero volts in the case of an A/D set up for a symmetrical bipolar input (e.g., −1.0 to +1.0 V).

DIFFERENTIAL NONLINEARITY — The maximum deviation in the actual step size (one transition level to another) from the ideal step size. The ideal step size is defined as the Full Scale Range divided by 2^n (n = number of bits). This error must be within ±1 LSB for proper operation.

FULL SCALE RANGE (ACTUAL) — The difference between the actual minimum and maximum end points of the analog input (of an A-D).

FULL SCALE RANGE (IDEAL) — The difference between the actual minimum and maximum end points of the analog input (of an A-D), plus one LSB.

GAIN ERROR — The difference between the actual and expected gain (end point to end point), with respect to the reference of a data converter. The gain error is usually expressed in LSBs.

GREY CODE — Also known as **reflected binary code,** it is a digital code such that each code differs from adjacent codes by only one bit. Since more than one bit is never changed at each transition, race condition errors are eliminated.

INTEGRAL NONLINEARITY — The maximum error of an A/D, or DAC, transfer function from the ideal straight line connecting the analog end points. This parameter is sensitive to dynamics, and test conditions must be specified in order to be meaningfull. This parameter is the best overall indicator of the device's performance.

LSB — Least Significant Bit. It is the lowest order bit of a binary code.

LINE REGULATION — The ability of a voltage regulator to maintain a certain output voltage as the input to the regulator is varied. The error is typically expressed as a percent of the nominal output voltage.

LOAD REGULATION — The ability of a voltage regulator to maintain a certain output voltage as the load current is varied. The error is typically expressed as a percent of the nominal output voltage.

MONOTONICITY — The characteristic of the transfer function whereby increasing the input code (of a DAC), or the input signal (of an A/D), results in the output never decreasing.

MSB — Most Significant Bit. It is the highest order bit of a binary code.

NATURAL BINARY CODE — A binary code defined by:

$$N = A_n 2^n + \ldots + A_3 2^3 + A_2 2^2 + A_1 2^1 + A_0 2^0$$

where each "A" coefficient has a value of 1 or 0. Typically, all zeroes corresponds to a zero input voltage of an A/D, and all ones corresponds to the most positive input voltage.

NYQUIST THEORY — See Sampling Theorem.

OFFSET BINARY CODE — Applicable only to bipolar input (or output) data converters, it is the same as Natural Binary, except that all zeroes corresponds to the most negative input voltage (of an A/D), while all ones corresponds to the most positive input.

POWER SUPPLY SENSITIVITY — The change in a data converters performance with changes in the power supply voltage(s). This parameter is usually expressed in percent of full scale versus ΔV.

QUANTITIZATION ERROR — Also known as digitization error or uncertainty. It is the inherent error involved in digitizing an analog signal due to the finite number of steps at the digital output versus the infinite number of values at the analog input. This error is a minimum of $\pm 1/2$ LSB.

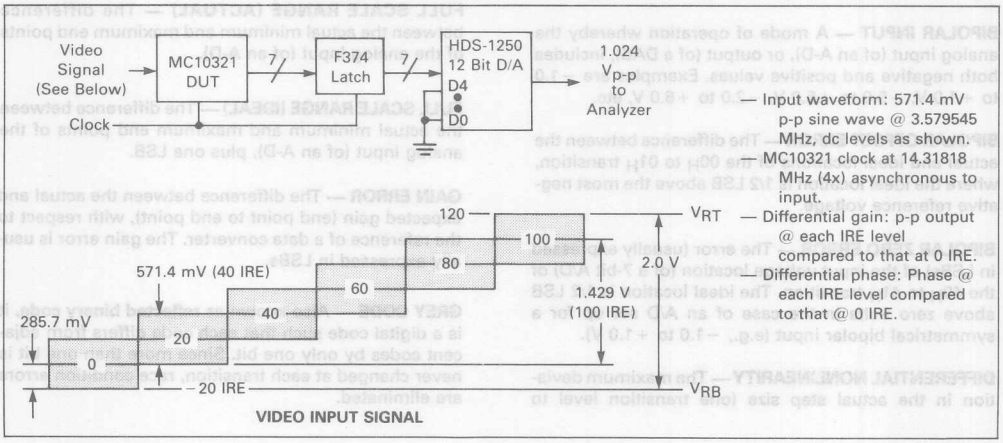
RESOLUTION — The smallest change which can be discerned by an A/D converter, or produced by a DAC. It is usually expressed as the number of bits, n, where the converter has 2^n possible states.

SAMPLING THEOREM — Also known as the Nyquist Theorem. It states that the sampling frequency of an A/D must be no less than 2x the highest frequency (of interest) of the analog signal to be digitized in order to preserve the information of that analog signal.

UNIPOLAR INPUT — A mode of operation whereby the analog input range (of an A/D), or output range (of a DAC), includes values of a single polarity. Examples are 0 to +2.0 V, 0 to −5.0 V, +2.0 to +8.0 V, etc.

UNIPOLAR OFFSET ERROR — The difference between the actual and ideal locations of the 00_H to 01_H transition, where the ideal location is 1/2 LSB above the most negative input voltage.

FIGURE 11 — DIFFERENTIAL PHASE AND GAIN TEST



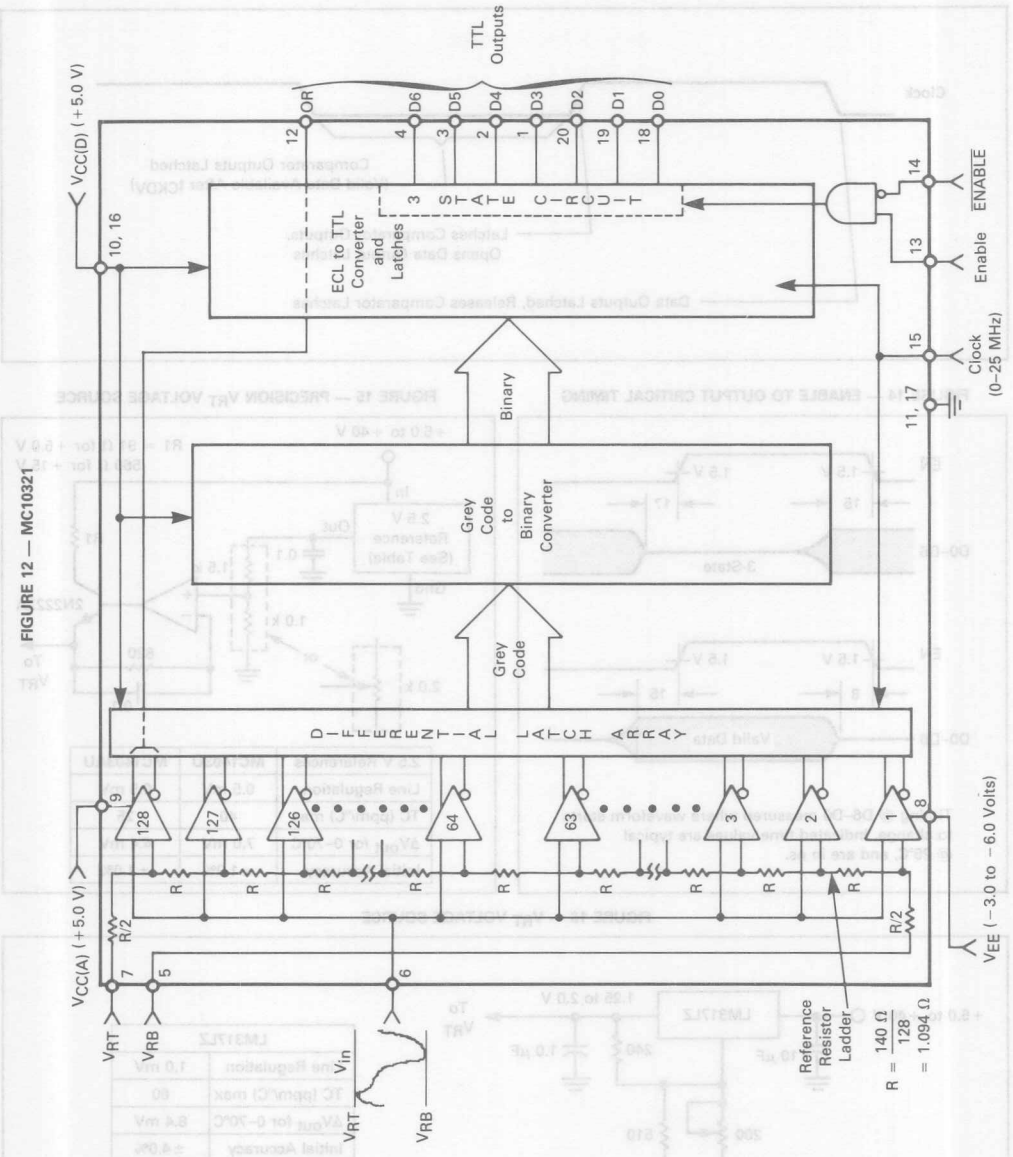


FIGURE 12 — MC10321

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FIGURE 13 — CONVERSION SEQUENCE

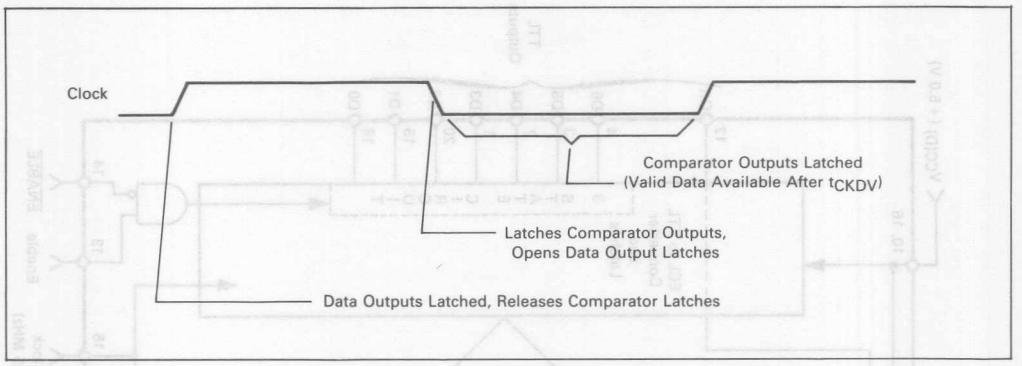
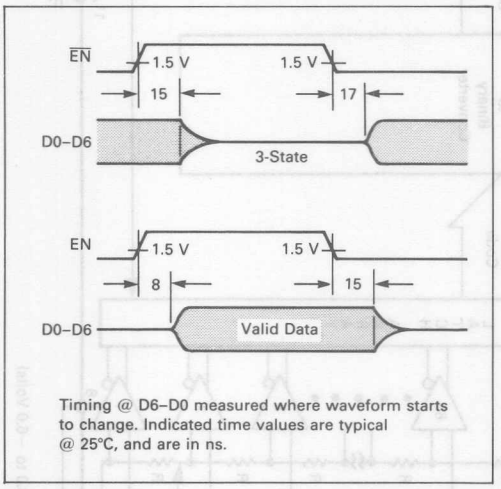
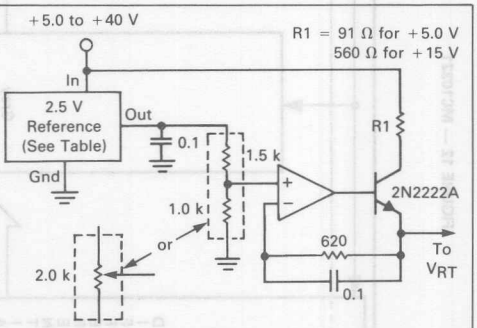


FIGURE 14 — ENABLE TO OUTPUT CRITICAL TIMING



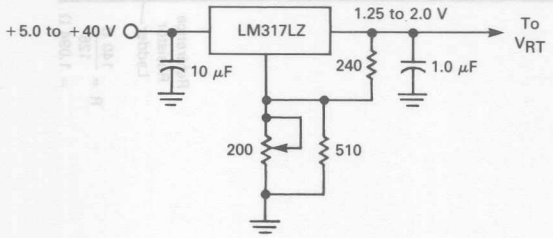
Timing @ D6–D0 measured where waveform starts to change. Indicated time values are typical @ 25°C, and are in ns.

FIGURE 15 — PRECISION V_{RT} VOLTAGE SOURCE



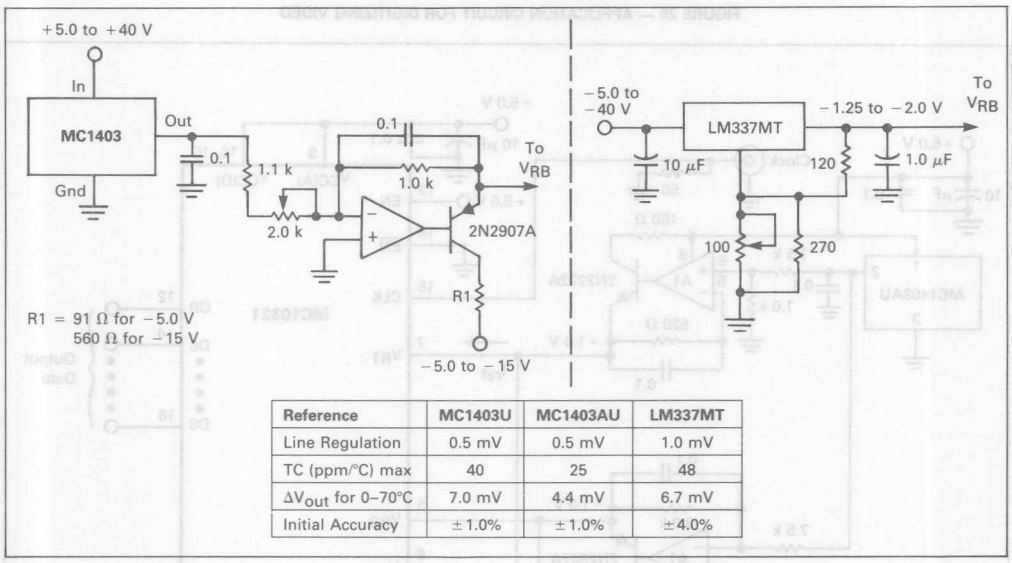
2.5 V References	MC1403U	MC1403AU
Line Regulation	0.5 mV	0.5 mV
TC (ppm/°C) max	40	25
ΔV_{out} for 0–70°C	7.0 mV	4.4 mV
Initial Accuracy	±1.0%	±1.0%

FIGURE 16 — V_{RT} VOLTAGE SOURCE



LM317LZ	
Line Regulation	1.0 mV
TC (ppm/°C) max	60
ΔV_{out} for 0–70°C	8.4 mV
Initial Accuracy	±4.0%

FIGURE 17 — V_{RB} VOLTAGE SOURCES



Reference	MC1403U	MC1403AU	LM337MT
Line Regulation	0.5 mV	0.5 mV	1.0 mV
TC (ppm/°C) max	40	25	48
ΔV_{out} for 0–70°C	7.0 mV	4.4 mV	6.7 mV
Initial Accuracy	±1.0%	±1.0%	±4.0%

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FIGURE 18

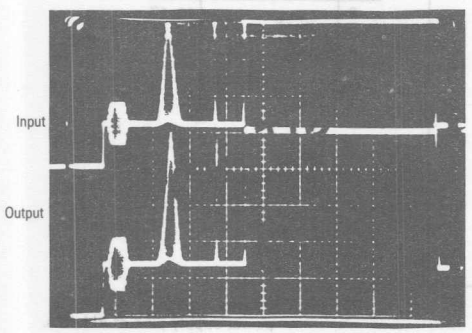


FIGURE 19

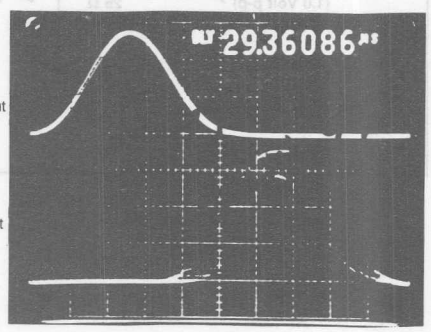
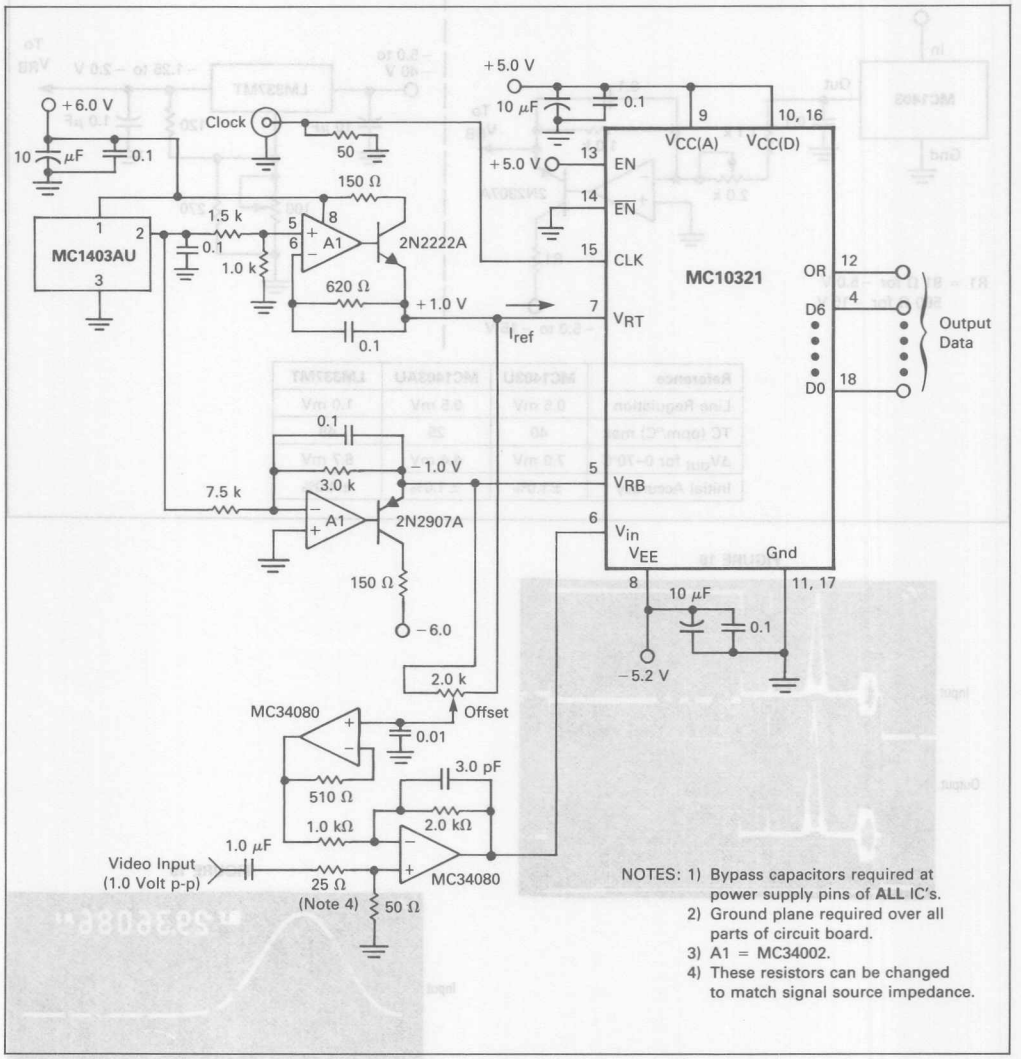


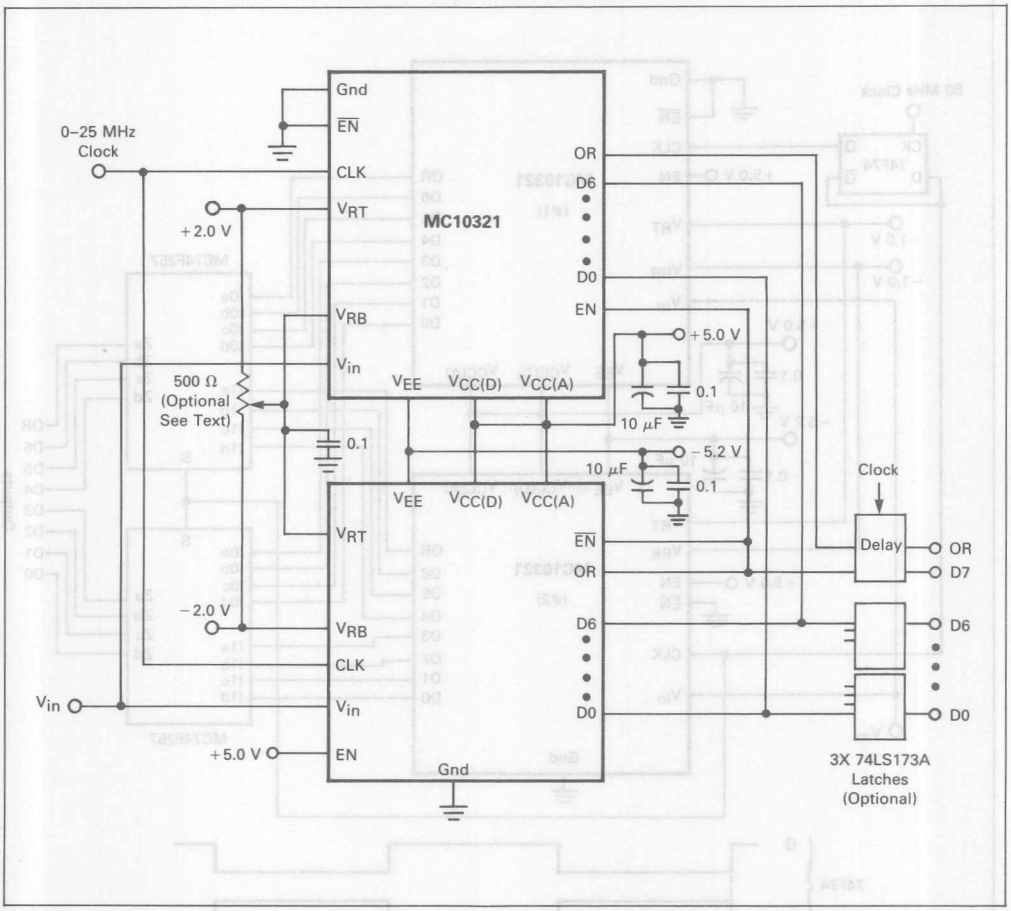
FIGURE 20 — APPLICATION CIRCUIT FOR DIGITIZING VIDEO



NOTES: 1) Bypass capacitors required at power supply pins of **ALL** IC's.
2) Ground plane required over all parts of circuit board.
3) A1 = MC34002.
4) These resistors can be changed to match signal source impedance.

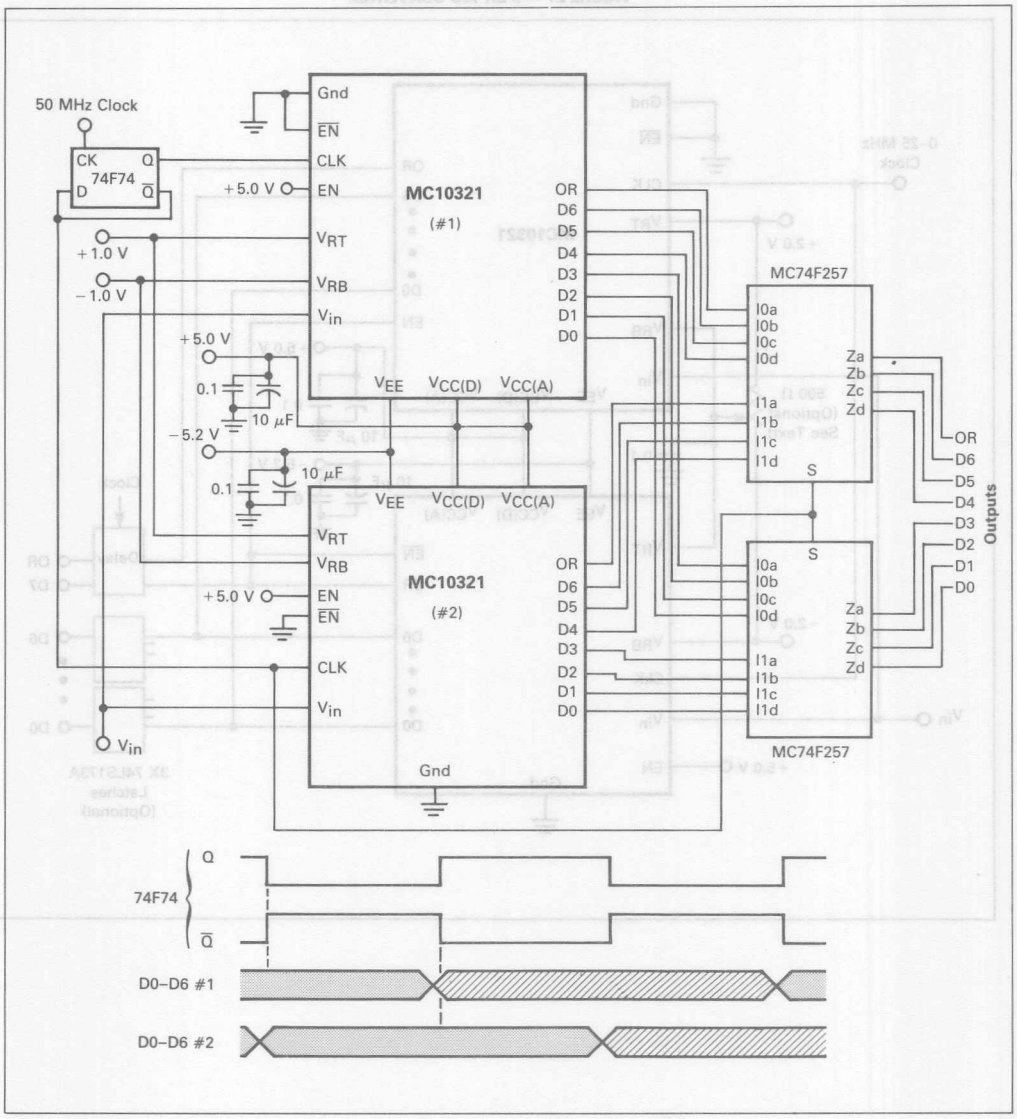
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FIGURE 21 — 8-BIT A/D CONVERTER



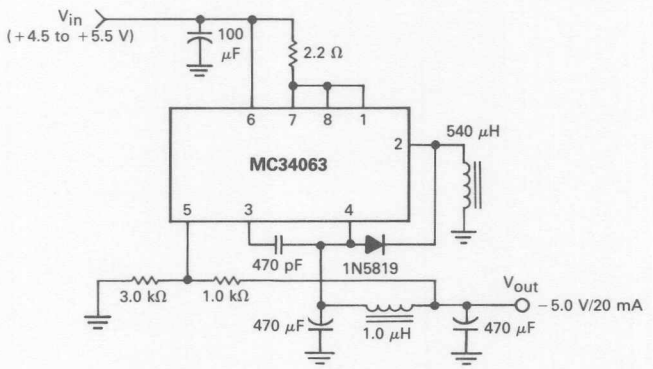
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FIGURE 22 — 50 MHz 7 BIT A/D CONVERTER

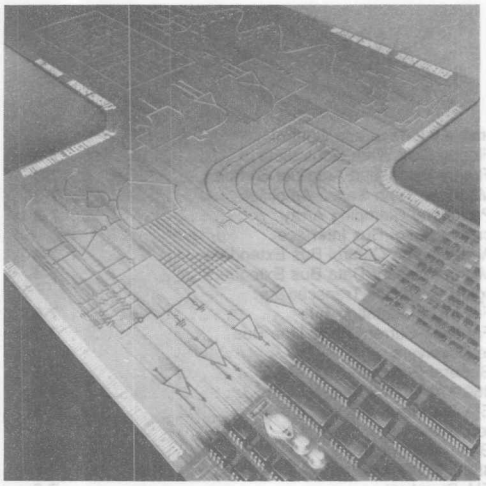


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FIGURE 23 — −5.0 VOLT REGULATOR



Line Regulation	$4.5\ V < V_{in} < 5.5\ V$, $I_{out} = 10\ mA$	0.16%
Load Regulation	$V_{in} = 5.0\ V$, $8.0\ mA < I_{out} < 20\ mA$	0.4%
Output Ripple	$V_{in} = 5.0\ V$, $I_{out} = 20\ mA$	2.0 mV p-p
Short Circuit I_{out}	$V_{in} = 5.0\ V$, $R_L = 0.1\ \Omega$	140 mA
Efficiency	$V_{in} = 5.0\ V$, $I_{out} = 50\ mA$	52%



Interface Circuits

7

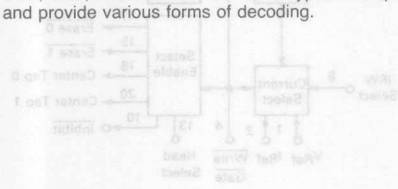
In Brief . . .

Described in this section is Motorola's line of interface circuits, which provide the means for interfacing microprocessor or digital systems to the external world, or to other systems.

Included are devices for reading and writing to a floppy disk or tape drive system, devices which allow a microprocessor to communicate with its own array of memory and peripheral I/O circuits.

The line drivers, receivers, and transceivers permit communications between systems over cables of several thousand feet in length, and at data rates of up to several megahertz. The common EIA data transmission standards, several European standards, IEEE-488, and IBM 360/370 are addressed by these devices.

The peripheral drivers are designed to handle high current loads such as relay coils, lamps, stepper motors, and others. Input levels to these drivers can be TTL, CMOS, High Voltage MOS, or other user defined levels. The display drivers are designed for LCD, LED, incandescent and other types of displays, and provide various forms of decoding.



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Interface Circuits

Memory Interface and Control

Motorola's line of circuits in this category have well established industry standards for reading and writing in a floppy disk system. The write circuits are designed for both straddle erase and tunnel erase heads, and provide both the writing and erasing functions. The read circuits include all the circuitry for peak detection, filtering, wave shaping, and guaranteed peak shift specifications.

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- Floppy Disk Write Controllers 7-2
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Microprocessor Bus Interface
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- 360/370 I/O Interface 7-6
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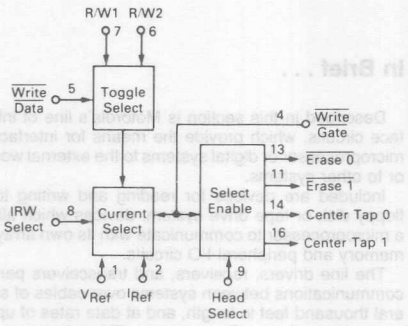
Floppy Disk Write Controllers

Straddle Erase Controller

MC3469P — T_A = 0° to +70°C, Case 648

Designed to provide the entire interface between floppy disk heads and the head control and write data signals for straddle-erase heads.

Provisions are made for selecting a range of accurately controlled write currents and for head selection during both read and write operation. Additionally, provisions are included for externally adjusting degauss period and inner/outer track compensation.

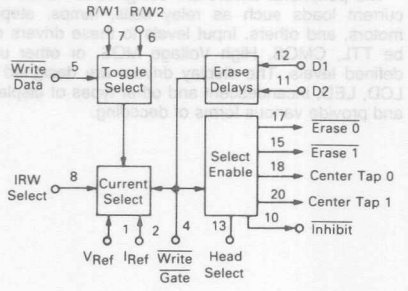


Tunnel/Straddle Erase Controller

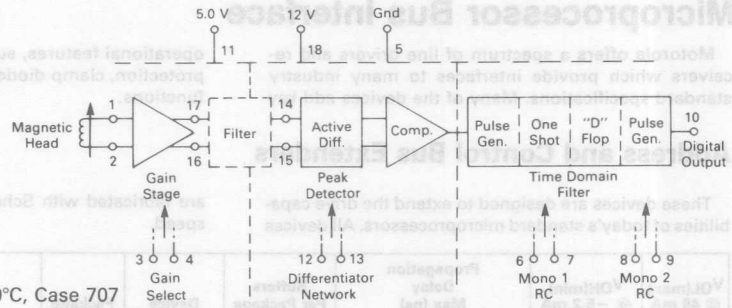
MC3471P — T_A = 0° to +70°C, Case 738

Provides the entire interface between the write data and head control signals and the heads (write and erase) for either tunnel or straddle-erase floppy disk systems.

Has provisions for external adjustment of degauss period, inner/outer track compensation, and the delay from write gate to erase turn-on and turn-off.



Floppy Disk Read Amplifier System



MC3470,A — T_A = 0° to +70°C, Case 707

Designed as monolithic Read Amplifier System for obtaining digital information from floppy disk storage. These devices accept differential ac signals produced by the magnetic head and provides a digital output pulse that corresponds to each peak of the input signal. A gain stage amplifies the input waveform and applies it to an external filter network, enabling the active differentiator and time domain filter to produce the desired output. These devices provide all the active circuitry to perform the floppy disk Read amplifier function, and guarantee to have a maximum peak shift of 5.0%, adjustable to zero, for the MC3470P and 2.0%, adjustable to zero, for the MC3470AP.

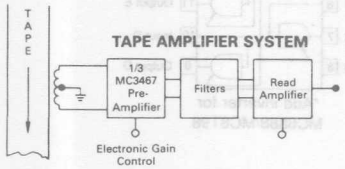
Device Number	Peak Shift (f = 250 kHz, V_{ID} = 1.0 V_{PP})	Differential Input Voltage Gain (f = 200 kHz, V_{ID} = 5.0 mV [RMS])		Input Common Mode Range (5% Max THD)	
		V/V		V	
	% Max	Min	Max	Min	Max
MC3470	5.0	80	130	−0.1	1.5
MC3470A	2.0	100	130		

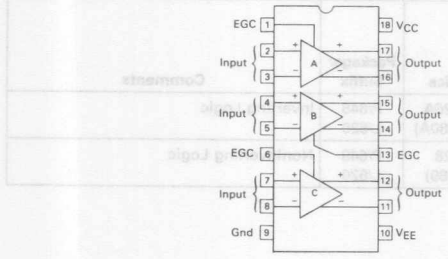
Magnetic Tape Sense Amplifier

MC3467L,P — T_A = 0° to +70°C, Case 726, 707

The MC3467 provides three independent preamplifiers with individual electronic gain control, optimized for use in 9-track magnetic tape memory systems where low noise and low distortion are paramount objectives.

The electronic gain control allows each amplifier's gain to be set anywhere from essentially zero to a maximum of approximately 100 V/V. Minimum small-signal bandwidth is 10 MHz, and Common-Mode Input Voltage range is 1.5 V min.



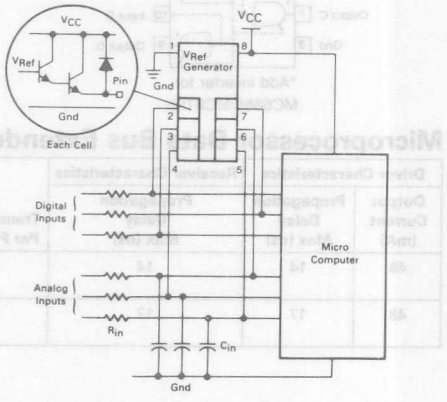


Peripheral Clamping Array

TCF6000P1,D — T_A = −40° to +85°C, Case 626, 751

. . . designed to protect input/output lines of microprocessor systems against voltage transients.

- Optimized for HMOS System
- Minimal Component Count
- Low Board Space Requirement
- No P.C.B. Track Crossovers Required
- Applications Areas Include Automotive, Industrial, Telecommunications and Consumer Goods



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Motorola offers a spectrum of line drivers and receivers which provide interfaces to many industry standard specifications. Many of the devices add key operational features, such as hysteresis, short circuit protection, clamp diode protection, or special control functions.

Address and Control Bus Extenders

These devices are designed to extend the drive capabilities of today's standard microprocessors. All devices are fabricated with Schottky TTL technology for high speed.

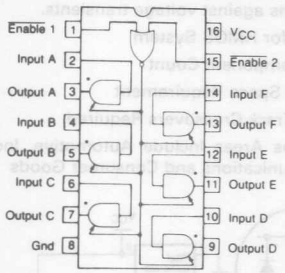
$V_{OL(max)}$ @ 48 mA	$V_{OH(min)}$ @ −5.2 mA	Propagation Delay Max (ns)	Buffers Per Package	Device	Package	Comments
0.5	2.4	13	6	MC8T95/ MC6885	L/620 P/648	Noninverting
0.5	2.4	11	6	MC8T96/ MC6886	L/620 P/648	Inverting
0.5	2.4	13	6	MC8T97/ MC6887	L/620 P/648	Noninverting
0.5	2.4	11	6	MC8T98/ MC6888	L/620 P/648	Inverting

Hex 3-State Buffers/Inverters — T_A = 0° to +75°C

These devices differ in that the non-inverting MC8T95/MC6885 and inverting MC8T96/MC6886 provide a two-input Enable which controls all six buffers, while the noninverting MC8T97/MC6887 and inverting MC8T98/MC6888 provide two Enable inputs — one controlling four buffers and the other controlling the remaining two buffers.

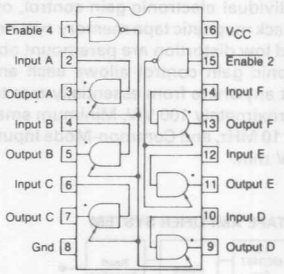
#These devices may be ordered by either of the paired numbers.

MC8T95/MC6885# — Noninverting
MC8T96/MC6886# — Inverting
Two-input Enable controls all six buffers



*Add inverter for MC6886/MC8T96.

MC8T97/MC6887# — Noninverting
MC8T98/MC6888# — Inverting
Two Enable inputs, one controlling four buffers and the other controlling the remaining two buffers.



*Add inverter for MC6888/MC8T98.

Microprocessor Data Bus Extenders

Driver Characteristics		Receiver Characteristics				
Output Current (mA)	Propagation Delay Max (ns)	Propagation Delay Max (ns)	Transceivers Per Package	Device	Package/ Suffix	Comments
48	14	14	4	MC8T26A (MC6880A)	P/648 L/620	Inverting Logic
48	17	17	4	MC8T28 (MC6889)	P/648 L/620	Noninverting Logic

Single-Ended Bus Transceivers

For Instrumentation Bus, Meets GPIB/IEEE Standard 488

Driver Characteristics		Receiver Characteristics				
Output Current (mA)	Propagation Delay Max (ns)	Propagation Delay Max (ns)	Transceivers Per Package	Device	Package/ Suffix	Comments
48	50	50	4	MC3446A	P/648	MOS Compatible, Input Hysteresis
48	30	50	8	MC3447	P3/724 L/623	Input Hysteresis, Open Collector, 3-State Outputs with Terminations
48	17	25	4	MC3448A	P/648 L/620	Input Hysteresis, Open Collector 3-State Outputs with Terminations
100	30	30	4	MC3440A	P/648	Input Hysteresis, Enable for 3 Drivers
				MC3441A		Common Enable, Input Hysteresis

For High-Current Party-Line Bus for Industrial and Data Communications

100	15	15	4	MC26S10	P/648 L/620	Open Collector Outputs, Common Enable

Line Receivers

General-Purpose

S = Single Ended D = Differential	Type* Of Output	t_{prop} Delay Time Max (ns)	Party-Line Operation	Strobe Or Enable	Power Supplies (V)	Device	Package/ Suffix	Receivers Per Package	Companion Drivers	Comments
D D	TP OC	25 25	Yes Yes	Yes Yes	±5 ±5	MC3450 MC3452	P/648 L/620	4 4	MC3453	Quad version of MC75107/8
D D	TP OC	25 25	Yes Yes	Yes Yes	±5 ±5	MC75107 MC75108	P/646 L/632	2 2	MC75S110	Dual version of MC3450/2
S	TP	30	Yes	Yes	+5	MC3437	P/648 L/620	6		Input Hysteresis

360/370 I/O Interface

S	TP	30	Yes	No	+5	MC75125 MC75127	P/648 L/620	7	MC3481 MC3485	Schottky Circuitry
S	TP	30	Yes	Yes	+5	MC75128 MC75129	P/738 L/732	8	MC3481 MC3485	Active high strobe Active low strobe

*OC = Open Collector, TP = Totem-pole output

EIA Standard

S = Single Ended D = Differential	Type* Of Output	t_{prop} Delay Time Max (ns)	Party-Line Operation	Strobe Or Enable	Power Supplies (V)	Device	Package/ Suffix	Receivers Per Package	Companion Drivers	EIA Standard
S	R	85	No	No	+5	MC1489 MC1489A	P/646 L/632	4	MC1488	(RS-232) EIA-232-D
S, D S, D	TP TP	30 30	Yes Yes	Yes Yes	+5 +5	AM26LS32 MC3486	P/648 L/620	4 4	AM26LS31 MC3487	(RS-422/423) EIA-422/423
S, D S, D	TP TP	35 35	Yes Yes	Yes Yes	+5 +5	SN75173 SN75175	N/648 J/620	4 4	SN75172 SN75174	(RS-422/423/485) EIA-422/423/485

*R = Resistor Pull-up, TP = Totem-pole output

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Line Drivers

General Purpose

Output Current Capability (mA)	t_{prop} Delay Time Max (ns)	S = Single Ended D = Differential	Party-Line Operation	Strobe Or Enable	Power Supplies (V)	Device	Package/ Suffix	Drivers Per package	Companion Receivers	Comments
15	15	D	Yes	Yes	±5	MC3453	P/648 L/620	4	MC3450 MC3452	Quad version of MC75S110
15	15	D	Yes	Yes	±5	MC75S110	P/646 L/632	2	MC75107 MC75108	Dual version of MC3453

360/370 I/O Interface

60	45	S	Yes	Yes	+5	MC3481	P/648 L/620	4	MC75125 MC75127	Short Circuit Fault Flag
60	45	S	Yes	Yes	+5	MC3485	P/648 L/620	4	MC75128 MC75129	Short Circuit Fault Flag

EIA Standard

Output Current Capability (mA)	t_{prop} Delay Time Max (ns)	S = Single Ended D = Differential	Party-Line Operation	Strobe Or Enable	Power Supplies (V)	Device	Package/ Suffix	Drivers Per Package	Companion Receivers	EIA Standard
85 85	35 35	D D	Yes Yes	Yes Yes	+5 +5	SN75172 SN75174	N/648 J/620	4 4	SN75173 SN75175	(RS-485) EIA-485
48	20	D	Yes	Yes	+5	MC3487	P/648 L/620	4	MC3486	(RS-422) EIA-422 with 3-State Outputs
48	20	D	Yes	Yes	+5	AM26LS31	P/648 D/620	4	AM26LS32	
20	—	S	No	No	±12	MC3488A (μA9636A)	P1/626 U/693	2	MC3486 AM26LS32	(RS-423/232) EIA-423/232-D
10	350	S	No	Yes	±9 to ±12	MC1488	P/646 L/632	4	MC1489 MC1489A	(RS-232) EIA-232-D

Line Transceivers

Driver Prop Delay (Max ns)	Receiver Prop Delay (Max ns)	CE = Common Enable DE = Driver Enable RE = Receiver Enable	Party Line Operation	Power Supply (V)	Device	Package/ Suffix	Drivers Per Package	Receivers Per Package	EIA Standard
20	30	DE, RE	Yes	+5	MC34050	L/620 P/648	2	2	(RS-422) EIA-422
20	30	DE	Yes	+5	MC34051	L/620 P/648	2	2	(RS-422) EIA-422

Peripheral Drivers

Output Current Capability (mA)	Input Capability	Propagation Delay Time Max (μs)	Output Clamp Diode	Off State Voltage Max (V)	Device	Drivers Per Package	Package/ Suffix	Logic Function
300	TTL, DTL	1.0	Yes	70	MC1472	2	P1/626 U/693	NAND
500	TTL, CMOS, PMOS	1.0	Yes	50	ULN2801	8	A/707	Invert
500	14 V to 25 V PMOS	1.0	Yes	50	ULN2802	8	A/707	Invert
500	TTL, CMOS	1.0	Yes	50	ULN2803	8	A/707	Invert
500	6.0 V to 15 V MOS	1.0	Yes	50	ULN2804	8	A/707	Invert
500	TTL, CMOS PMOS	1.0	Yes	50	MC1411,B	7	P/648	Invert
500	14 V to 25 V PMOS	1.0	Yes	50	MC1412,B	7	P/648	Invert
500	TTL, 5.0 V CMOS	1.0	Yes	50	MC1413,B	7	P/648	Invert
500	8.0 V to 18 V MOS	1.0	Yes	50	MC1416,B	7	P/648	Invert
1500	TTL, 5.0 V CMOS	1.0	Yes	50	ULN2068B	4	B/648	Invert
1500	TTL, 5.0 V CMOS	1.0	No	50	ULN2074B	4	B/648	Collector, Emitter available at Pins

Memory Interface and Control

Device	Function	Page
MC3467	Triple Preamplifier	7-83
MC3469P	Floppy Disk Write Controller	7-88
MC3470P,AP	Floppy Disk Read Amplifier System	7-98
MC3471P	Floppy Disk Write Controller/Head Driver	7-112
MC3480	Memory Controller Circuit	7-123
TCF6000	Peripheral Clamping Array	7-196

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Device	Function	Page
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MC8T28	Noninverting Bus Transceiver	7-21
MC8T95	Hex Three-State Buffer/Inverter	7-26
MC8T96	Hex Three-State Buffer/Inverter	7-26
MC8T97	Hex Three-State Buffer/Inverter	7-26
MC8T98	Hex Three-State Buffer/Inverter	7-26
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MC6880A	Quad Three-State Bus Transceiver	7-16
MC6885	Hex Three-State Buffer/Inverter	7-26
MC6886	Hex Three-State Buffer/Inverter	7-26
MC6887	Hex Three-State Buffer/Inverter	7-26
MC6888	Hex Three-State Buffer/Inverter	7-26
MC6889	Noninverting Bus Transceiver	7-21

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Single-Ended Bus Transceivers

Device	Function	Page
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MC3440A	Quad Interface Bus Transceiver	7-54
MC3441A	Quad Interface Bus Transceiver	7-54
MC3446A	Quad Interface Bus Transceiver	7-58
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MC3448A	Quad Three-State Bus Transceiver	7-67

Line Receivers

Device	Function	Page
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MC1489,A	Quad MDTL Line Receiver	7-43
MC3437	Hex Unified Bus Receiver	7-51
MC3450	Quad Line Receiver	7-72
MC3452	Quad Line Receiver	7-72
MC3486	Quad EIA-422/423 Line Receiver	7-142
MC75107	Dual Line Receiver	7-171
MC75108	Dual Line Receiver	7-171
MC75125	Seven-Channel Line Receivers	7-181
MC75127	Seven-Channel Line Receivers	7-181
MC75128	Eight-Channel Line Receivers	7-185
MC75129	Eight-Channel Line Receivers	7-185
SN75173	Quad EIA-422A/3 Line Receiver with Three-State Output	7-191
SN75175	Quad EIA-422A/3 Line Receiver with Three-State Output	7-191

Line Drivers

Device	Function	Page
AM26LS31	Quad EIA-422 Line with Three-State Output	7-10
MC1488	Quad MDTL Line Driver	7-37
MC3453	Quad Line Driver	7-79
MC3481	Quad Single-Ended Line Driver	7-137
MC3485	Quad Single-Ended Line Driver	7-137
MC3487	Quad EIA-422 Line Driver with Three-State Outputs	7-145
MC3488A	Dual EIA-423/232C Driver	7-149
MC75S110	Dual Line Driver	7-176
SN75172	Quad EIA-485 Line Driver with Three-State Output	7-189
SN75174	Quad EIA-485 Line Driver with Three-State Output	7-189

Line Transceivers

Device	Function	Page
MC34050	Dual EIA-422/423 Transceiver	7-164
MC34051	Dual EIA-422/423 Transceiver	7-164

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Device	Function	Page
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MC1413,B	Peripheral Driver Array	7-30
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ULN2074B	Quad 1.5 A Darlington Switch	7-204
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ULN2802	Octal Peripheral Driver Array	7-208
ULN2803	Octal Peripheral Driver Array	7-208
ULN2804	Octal Peripheral Driver Array	7-208

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RELATED APPLICATION NOTES

Application Note	Title	Related Device
AN708A	Line Driver and Receiver Considerations	MC3486
AN781A	Revised Data — Interface Standards	MC3488
AN917	Reading and Writing in Floppy Disk Systems Using Motorola Integrated Circuits	MC3467

MOTOROLA

AM26LS31

QUAD LINE DRIVER WITH NAND ENABLED THREE-STATE OUTPUTS

The Motorola AM26LS31 is a quad differential line driver intended for digital data transmission over balanced lines. It meets all the requirements of EIA-422 Standard and Federal Standard 1020.

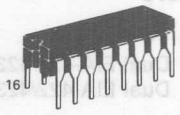
The AM26LS31 provides an enable/disable function common to all four drivers as opposed to the split enables on the MC3487 EIA-422 driver.

The high impedance output state is assured during power down.

- Full EIA-422 Standard Compliance
- Single +5.0 V Supply
- Meets Full V_O = 6.0 V, V_{CC} = 0 V, I_O < 100 μA Requirement
- Output Short Circuit Protection
- Complementary Outputs for Balanced Line Operation
- High Output Drive Capability
- Advanced LS Processing
- PNP Inputs for MOS Compatibility

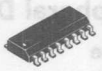
QUAD EIA-422 LINE DRIVER WITH THREE-STATE OUTPUTS

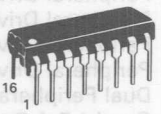
SILICON MONOLITHIC INTEGRATED CIRCUIT



D SUFFIX
CERAMIC PACKAGE
CASE 620-10

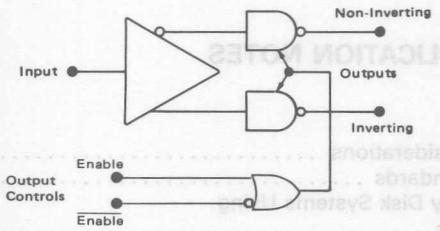
D SUFFIX
PLASTIC PACKAGE
CASE 751B-03
SO-16



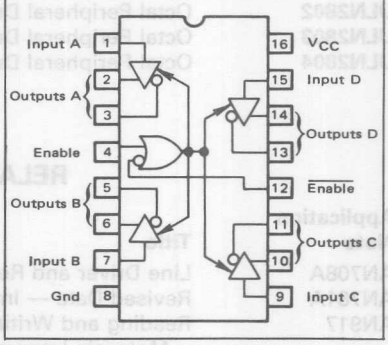


P SUFFIX
PLASTIC PACKAGE
CASE 648-06

DRIVER BLOCK DIAGRAM



PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
AM26LS31DC	0 to 70°C	Ceramic DIP
AM26LS31PC		Plastic DIP
MC26LS31D*		SO-16

*Note that the surface mount MC26LS31D devices use the same die as in the ceramic and plastic DIP AM26LS31DC devices, but with an MC prefix to prevent confusion with the package suffixes.

TRUTH TABLE

Input	Control Inputs (E/$\overline{E}$)	Non-Inverting Output	Inverting Output
H	H/L	H	L
L	H/L	L	H
X	L/H	Z	Z

L = Low Logic State
H = High Logic State
X = Irrelevant
Z = Third-State (High Impedance)

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.0	Vdc
Input Voltage	V_I	5.5	Vdc
Operating Ambient Temperature Range	T_A	0 to +70	°C
Operating Junction Temperature Range Ceramic Package Plastic Package	T_J	 175 150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted specifications apply 4.75 V ≤ V_{CC} ≤ 5.25 V and 0°C ≤ T_A ≤ 70°C. Typical values measured at V_{CC} = 5.0 V, and T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage — Low Logic State	V_{IL}	—	—	0.8	Vdc
Input Voltage — High Logic State	V_{IH}	2.0	—	—	Vdc
Input Current — Low Logic State (V_{IL} = 0.4 V)	I_{IL}	—	—	−360	μA
Input Current — High Logic State (V_{IH} = 2.7 V) (V_{IH} = 7.0 V)	I_{IH}	 — —	 — —	 +20 +100	μA
Input Clamp Voltage (I_{IK} = −18 mA)	V_{IK}	—	—	−1.5	V
Output Voltage — Low Logic State (I_{OL} = 20 mA)	V_{OL}	—	—	0.5	V
Output Voltage — High Logic State (I_{OH} = −20 mA)	V_{OH}	2.5	—	—	V
Output Short Circuit Current (V_{IH} = 2.0 V) Note 1	I_{OS}	−30	—	−150	mA
Output Leakage Current — Hi-Z State (V_{OL} = 0.5 V, $V_{IL(E)}$ = 0.8 V, $V_{IH(\overline{E})}$ = 2.0 V) (V_{OH} = 2.5 V, $V_{IL(E)}$ = 0.8 V, $V_{IH(\overline{E})}$ = 2.0 V)	$I_{O(Z)}$	 — —	 — —	 −20 +20	μA
Output Leakage Current — Power OFF (V_{OH} = 6.0 V, V_{CC} = 0 V) (V_{OL} = −0.25 V, V_{CC} = 0 V)	$I_{O(off)}$	 — —	 — —	 +100 −100	μA
Output Offset Voltage Difference, Note 2	$V_{OS} - \overline{V}_{OS}$	—	—	±0.4	V
Output Differential Voltage, Note 2	V_{OD}	2.0	—	—	V
Output Differential Voltage Difference, Note 2	$\lvert\Delta V_{OD}\rvert$	—	—	±0.4	V
Power Supply Current (Output Disabled) Note 3	I_{CCX}	—	60	80	mA

1. Only one output may be shorted at a time.
2. See EIA Specification EIA-422 for exact test conditions.
3. Circuit in three-state condition.

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Times High to Low Output Low to High Output	 t_{PHL} t_{PLH}	 — —	 — —	 20 20	ns
Output Skew		—	—	6.0	ns
Propagation Delay — Control to Output (C_L = 10 pF, R_L = 75 Ω to Gnd) (C_L = 10 pF, R_L = 180 Ω to V_{CC}) (C_L = 30 pF, R_L = 75 Ω to Gnd) (C_L = 30 pF, R_L = 180 Ω to V_{CC})	 $t_{PHZ(E)}$ $t_{PLZ(E)}$ $t_{PZH(E)}$ $t_{PZL(E)}$	 — — — —	 — — — —	 30 35 40 45	ns

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FIGURE 1 – THREE-STATE ENABLE TEST CIRCUIT AND WAVEFORMS

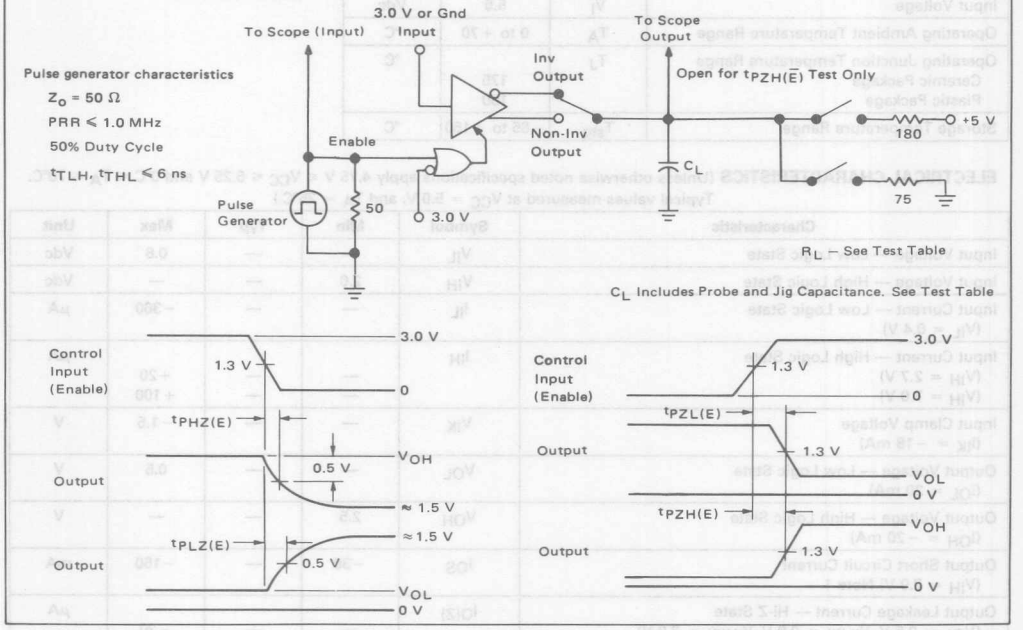
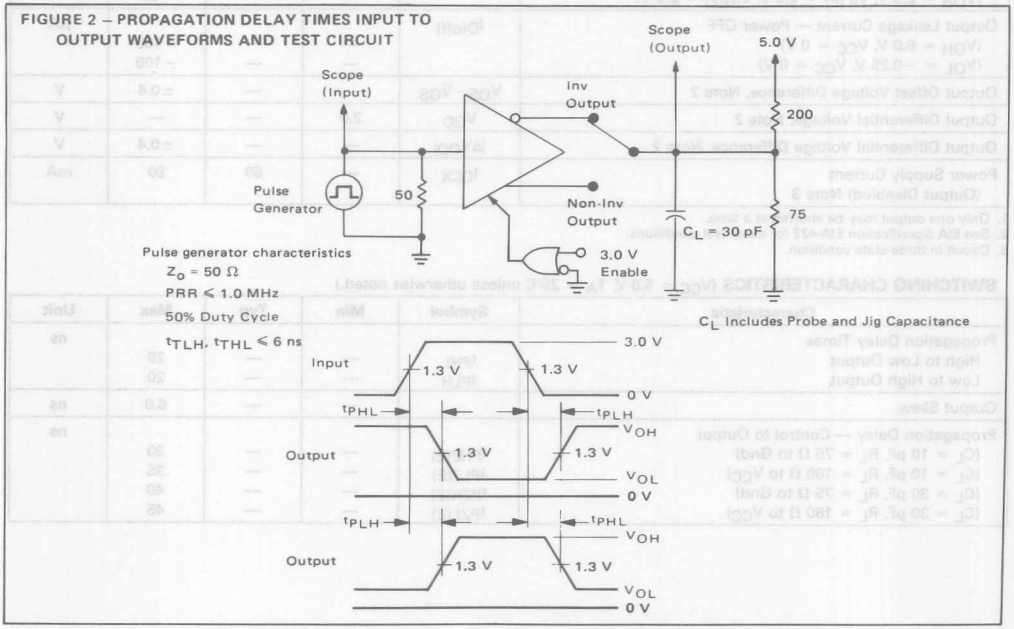


FIGURE 2 – PROPAGATION DELAY TIMES INPUT TO OUTPUT WAVEFORMS AND TEST CIRCUIT



MOTOROLA

AM26LS32

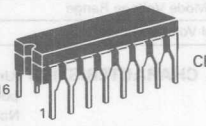
QUAD EIA-422/423 LINE RECEIVER

Motorola's Quad EIA-422/3 Receiver features four independent receiver chains which comply with EIA Standards for the Electrical Characteristics of Balanced/Unbalanced Voltage Digital Interface Circuits. Receiver outputs are 74LS compatible, three-state structures which are forced to a high impedance state when Pin 4 is a Logic "0" and Pin 12 is a Logic "1." A PNP device buffers each output control pin to assure minimum loading for either Logic "1" or Logic "0" inputs. In addition, each receiver chain has internal hysteresis circuitry to improve noise margin and discourage output instability for slowly changing input waveforms. A summary of AM26LS32 features include:

- Four Independent Receiver Chains
- Three-State Outputs
- High Impedance Output Control Inputs (PIA Compatible)
- Internal Hysteresis — 30 mV (Typ) @ Zero Volts Common Mode
- Fast Propagation Times — 25 ns (Typ)
- TTL Compatible
- Single 5 V Supply Voltage
- Fail-Safe Input-Output Relationship. Output Always High When Inputs Are Open, Terminated or Shorted
- 6K Minimum Input Impedance

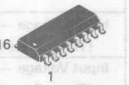
QUAD EIA-422/3 LINE RECEIVER WITH THREE-STATE OUTPUTS

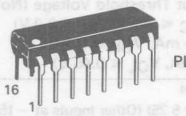
SILICON MONOLITHIC INTEGRATED CIRCUIT



D SUFFIX
CERAMIC PACKAGE
CASE 620-10

D SUFFIX
PLASTIC PACKAGE
CASE 751B-03
SO-16

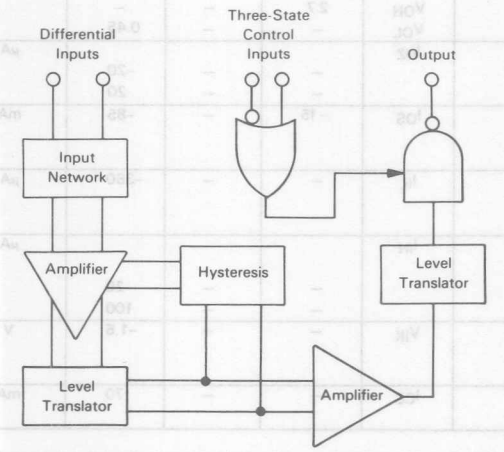




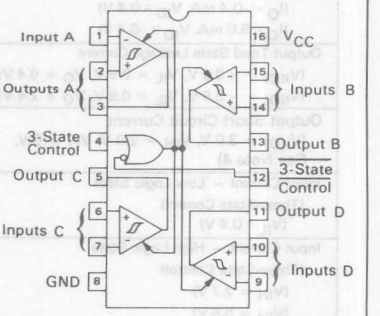
P SUFFIX
PLASTIC PACKAGE
CASE 648-06

7

RECEIVER CHAIN BLOCK DIAGRAM



PIN CONNECTIONS



ORDERING INFORMATION		
Device	**Temperature**	**Package**
AM26LS32DC	0 to 70°C	Ceramic DIP
AM26LS32PC		Plastic DIP
MC26LS32D*		SO-16

*Note that the surface mount MC26LS32D devices use the same die as in the ceramic and plastic DIP AM26LS32DC devices, but with an MC prefix to prevent confusion with the package suffixes.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Input Common Mode Voltage	V_{ICM}	±25	Vdc
Input Differential Voltage	V_{ID}	±25	Vdc
Three-State Control Input Voltage	V_I	7.0	Vdc
Output Sink Current	I_O	50	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Operating Junction Temperature	T_J		°C
Ceramic Package		+175	
Plastic Package		+150	

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	4.75 to 5.25	Vdc
Operating Ambient Temperature	T_A	0 to +70	°C
Input Common Mode Voltage Range	V_{ICR}	−7.0 to +7.0	Vdc
Input Differential Voltage Range	V_{IDR}	6.0	Vdc

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted minimum and maximum limits apply over recommended temperature and power supply voltage ranges. Typical values are for T_A = 25°C, V_{CC} = 5.0 V and V_{IC} = 0.V. See Note 1.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage — High Logic State (Three-State Control)	V_{IH}	2.0	—	—	V
Input Voltage — Low Logic State (Three-State Control)	V_{IL}	—	—	0.8	V
Differential Input Threshold Voltage (Note 2) ($-7.0\ V \leq V_{IC} \leq 7.0\ V$, V_{IH} = 2.0 V)	$V_{TH(D)}$				V
(I_O = −0.4 mA, $V_{OH} \geq$ 2.7 V)		—	—	0.2	
(I_O = 8.0 mA, $V_{OL} \leq$ 0.45 V)		—	—	−0.2	
Input Bias Current (V_{CC} = 0 V or 5.25) (Other Inputs at $-15\ V \leq V_{in} \leq +15\ V$)	$I_{IB(D)}$				mA
V_{in} = +15 V		—	—	2.3	
V_{in} = −15 V		—	—	−2.8	
Input Resistance ($-15\ V \leq V_{in} \leq +15\ V$)	R_{in}	6.0 K	—	—	Ohms
Input Balance and Output Level ($-7.0\ V \leq V_{IC} \leq 7.0\ V$, V_{IH} = 2.0 V, See Note 3)					V
(I_O = −0.4 mA, V_{ID} = 0.4 V)	V_{OH}	2.7	—	—	
(I_O = 8.0 mA, V_{ID} = −0.4 V)	V_{OL}	—	—	0.45	
Output Third State Leakage Current	I_{OZ}				μA
($V_{I(D)}$ = +3.0 V, V_{IL} = 0.8 V, V_O = 0.4 V)		—	—	−20	
($V_{I(D)}$ = −3.0 V, V_{IL} = 0.8 V, V_O = 2.4 V)		—	—	20	
Output Short Circuit Current ($V_{I(D)}$ = 3.0 V, V_{IH} = 2.0 V, V_O = 0 V, See Note 4)	I_{OS}	−15	—	−85	mA
Input Current — Low Logic State (Three-State Control) (V_{IL} = 0.4 V)	I_{IL}	—	—	−360	μA
Input Current — High Logic State (Three-State Control)	I_{IH}				μA
(V_{IH} = 2.7 V)		—	—	20	
(V_{IH} = 5.5 V)		—	—	100	
Input Clamp Diode Voltage (Three-State Control) (I_{IC} = −18 mA)	V_{IK}	—	—	−1.5	V
Power Supply Current (V_{IL} = 0 V) (All Inputs Grounded)	I_{CC}	—	—	70	mA

1. All currents into device pins are shown as positive, out of device pins are negative. All voltages referenced to ground unless otherwise noted.
2. Differential input threshold voltage and guaranteed output levels are done simultaneously for worst case.
3. Refer to EIA-422/3 for exact conditions. Input balance and guaranteed output levels are done simultaneously for worst case.
4. Only one output at a time should be shorted.

SWITCHING CHARACTERISTICS (Unless otherwise noted, V_{CC} = 5.0 V and T_A = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time — Differential Inputs to Output					ns
(Output High to Low)	$t_{PHL(D)}$	—	—	30	
(Output Low to High)	$t_{PLH(D)}$	—	—	30	
Propagation Delay Time — Three-State Control to Output					ns
(Output Low to Third State)	t_{PLZ}	—	—	35	
(Output High to Third State)	t_{PHZ}	—	—	35	
(Output Third State to High)	t_{PZH}	—	—	30	
(Output Third State to Low)	t_{PZL}	—	—	30	

SWITCHING TEST CIRCUIT AND WAVE FOR
FIGURE 1 - PROPAGATION DELAY DIFFERENTIAL INPUT TO OUTPUT

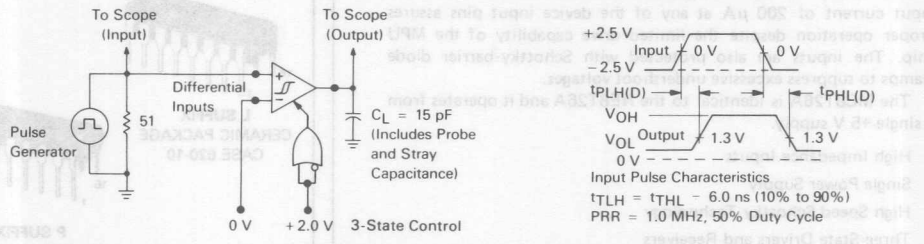
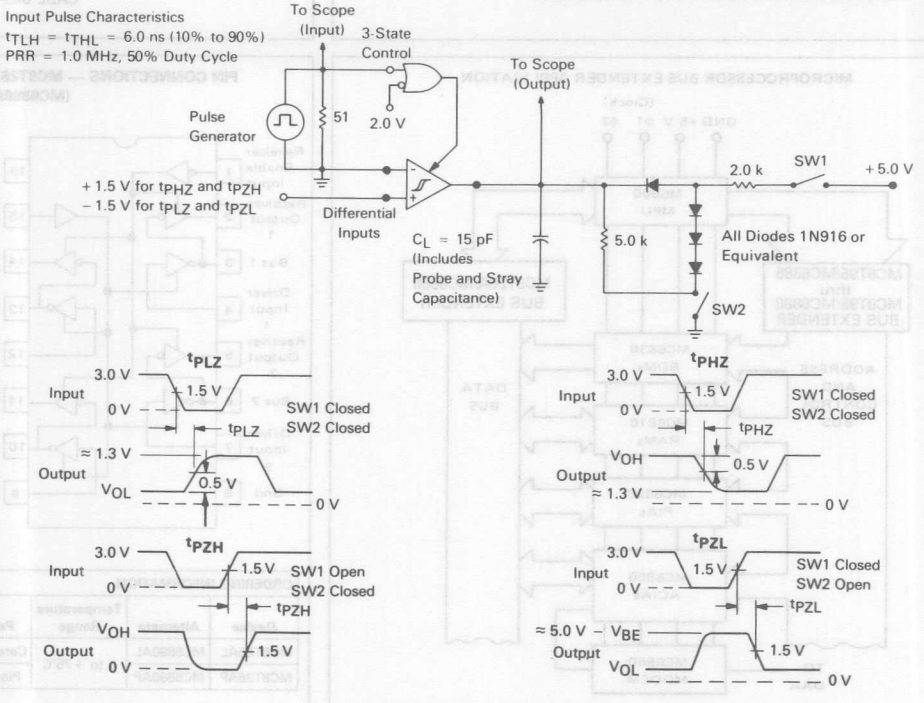


FIGURE 2 — PROPAGATION DELAY THREE-STATE CONTROL INPUT TO OUTPUT



7

MOTOROLA

MC8T26A
(MC6880A)

QUAD THREE-STATE BUS TRANSCEIVER

This quad three-state bus transceiver features both excellent MOS or MPU compatibility, due to its high impedance PNP transistor input, and high-speed operation made possible by the use of Schottky diode clamping. Both the −48 mA driver and −20 mA receiver outputs are short-circuit protected and employ three-state enabling inputs.

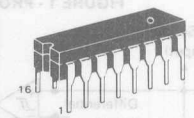
The device is useful as a bus extender in systems employing the M6800 family or other comparable MPU devices. The maximum input current of 200 μA at any of the device input pins assures proper operation despite the limited drive capability of the MPU chip. The inputs are also protected with Schottky-barrier diode clamps to suppress excessive undershoot voltages.

The MC8T26A is identical to the NE8T26A and it operates from a single +5 V supply.

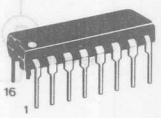
- High Impedance Inputs
- Single Power Supply
- High Speed Schottky Technology
- Three-State Drivers and Receivers
- Compatible with M6800 Family Microprocessor

QUAD THREE-STATE BUS TRANSCEIVER

MONOLITHIC SCHOTTKY INTEGRATED CIRCUITS



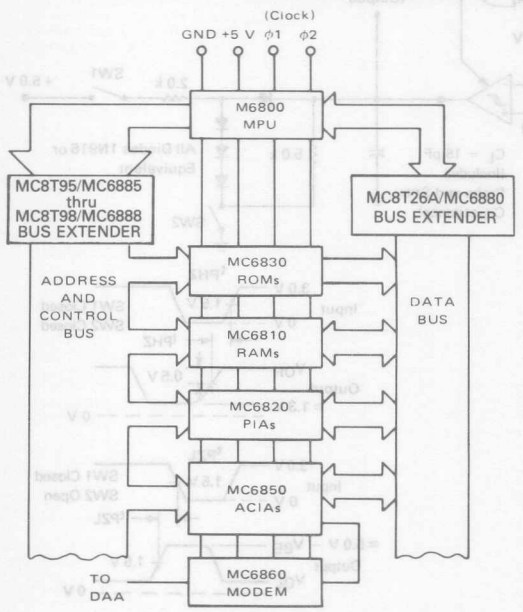
L SUFFIX
CERAMIC PACKAGE
CASE 620-10



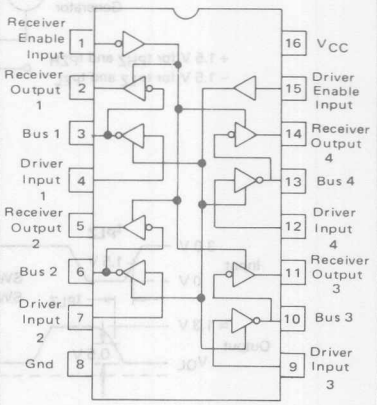
P SUFFIX
PLASTIC PACKAGE
CASE 648-06

7

MICROPROCESSOR BUS EXTENDER APPLICATION



PIN CONNECTIONS — MC8T26A (MC6880A)



ORDERING INFORMATION

Device	Alternate	Temperature Range	Package
MC8T26AL	MC6880AL	0 to +75°C	Ceramic DIP
MC8T26AP	MC6880AP		Plastic DIP

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.0	Vdc
Input Voltage	V_I	5.5	Vdc
Junction Temperature Ceramic Package Plastic Package	T_J	 175 150	°C
Operating Ambient Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (4.75 V ≤ V_{CC} ≤ 5.25 V and 0°C ≤ T_A ≤ 75°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current – Low Logic State					
(Receiver Enable Input, $V_{IL(RE)}$ = 0.4 V)	$I_{IL(\overline{RE})}$	–	–	-200	μA
(Driver Enable Input, $V_{IL(DE)}$ = 0.4 V)	$I_{IL(DE)}$	–	–	-200	
(Driver Input, $V_{IL(D)}$ = 0.4 V)	$I_{IL(D)}$	–	–	-200	
(Bus (Receiver) Input, $V_{IL(B)}$ = 0.4 V)	$I_{IL(B)}$	–	–	-200	
Input Disabled Current – Low Logic State (Driver Input, $V_{IL(D)}$ = 0.4 V)	$I_{IL(D)\ DIS}$	–	–	-25	μA
Input Current-High Logic State					
(Receiver Enable Input, $V_{IH(RE)}$ = 5.25 V)	$I_{IH(\overline{RE})}$	–	–	25	μA
(Driver Enable Input, $V_{IH(DE)}$ = 5.25 V)	$I_{IH(DE)}$	–	–	25	
(Driver Input, $V_{IH(D)}$ = 5.25 V)	$I_{IH(D)}$	–	–	25	
(Receiver Input, $V_{IH(B)}$ = 5.25 V)	$I_{IH(B)}$	–	–	100	
Input Voltage – Low Logic State					
(Receiver Enable Input)	$V_{IL(\overline{RE})}$	–	–	0.85	V
(Driver Enable Input	$V_{IL(DE)}$	–	–	0.85	
(Driver Input)	$V_{IL(D)}$	–	–	0.85	
(Receiver Input)	$V_{IL(B)}$	–	–	0.85	
Input Voltage – High Logic State					
(Receiver Enable Input)	$V_{IH(\overline{RE})}$	2.0	–	–	V
(Driver Enable Input)	$V_{IH(DE)}$	2.0	–	–	
(Driver Input)	$V_{IH(D)}$	2.0	–	–	
(Receiver Input)	$V_{IH(B)}$	2.0	–	–	
Output Voltage – Low Logic State					
(Bus Driver) Output, $I_{OL(B)}$ = 48 mA)	$V_{OL(B)}$	–	–	0.5	V
(Receiver Output, $I_{OL(R)}$ = 20 mA)	$V_{OL(R)}$	–	–	0.5	
Output Voltage – High Logic State					
(Bus (Driver) Output, $I_{OH(B)}$ = –10 mA)	$V_{OH(B)}$	2.4	3.1	–	V
(Receiver Output, $I_{OH(R)}$ = –2.0 mA)	$V_{OH(R)}$	2.4	3.1	–	
(Receiver Output, $I_{OH(R)}$ = –100 μA, V_{CC} = 5.0 V)		3.5	–	–	
Output Disabled Leakage Current – High Logic State					
(Bus Driver) Output, $V_{OH(B)}$ = 2.4 V)	$I_{OHL(B)}$	–	–	100	μA
(Receiver Output, $V_{OH(R)}$ = 2.4 V)	$I_{OHL(R)}$	–	–	100	
Output Disabled Leakage Current – Low Logic State					
(Bus Output, $V_{OL(B)}$ = 0.5 V)	$I_{OLL(B)}$	–	–	–100	μA
(Receiver Output, $V_{OL(R)}$ = 0.5 V)	$I_{OLL(R)}$	–	–	–100	
Input Clamp Voltage					
(Driver Enable Input $I_{ID(DE)}$ = –12 mA)	$V_{IC(DE)}$	–	–	-1.0	V
(Receiver Enable Input $I_{IC(RE)}$ = +12 mA)	$V_{IC(RE)}$	–	–	-1.0	
(Driver Input $I_{IC(D)}$ = –12 mA)	$V_{IC(D)}$	–	–	-1.0	
Output Short Circuit Current, V_{CC} = 5.25 V, Note 1 (Bus (Driver) Output) (Receiver Output)	 $I_{OS(B)}$ $I_{OS(R)}$	 -50 -30	 – –	 -150 -75	mA
Power Supply Current (V_{CC} = 5.25 V)	I_{CC}	–	–	87	mA

Note 1. Only one output may be short-circuited at a time.

7

SWITCHING CHARACTERISTICS (Unless otherwise noted, specifications apply at $T_A = 25^oC$ and $V_{CC} = 5.0$ V)

Characteristic	Symbol	Figure	Min	Max	Unit
Propagation Delay Time from Receiver (Bus) Input to High Logic State Receiver Output	$t_{PLH(R)}$	1	–	14	ns
Propagation Delay Time from Receiver (Bus) Input to Low Logic State Receiver Output	$t_{PHL(R)}$	1	–	14	ns
Propagation Delay Time from Driver Input to High Logic State Driver (Bus) Output	$t_{PLH(D)}$	2	–	14	ns
Propagation Delay Time from Driver Input to Low Logic State Driver (Bus) Output	$t_{PHL(D)}$	2	–	14	ns
Propagation Delay Time from $\overline{\text{Receiver Enable}}$ Input to High Impedance (Open) Logic State Receiver Output	$t_{PLZ(RE)}$	3	–	15	ns
Propagation Delay Time from $\overline{\text{Receiver Enable}}$ Input to Low Logic Level Receiver Output	$t_{PZL(RE)}$	3	–	20	ns
Propagation Delay Time from Driver Enable Input to High Impedance Logic State Driver (Bus) Output	$t_{PLZ(DE)}$	4	–	20	ns
Propagation Delay Time from Driver Enable Input to Low Logic State Driver (Bus) Output	$t_{PZL(DE)}$	4	–	25	ns

FIGURE 1 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY FROM BUS (RECEIVER) INPUT TO RECEIVER OUTPUT, $t_{PLH(R)}$ AND $t_{PHL(R)}$

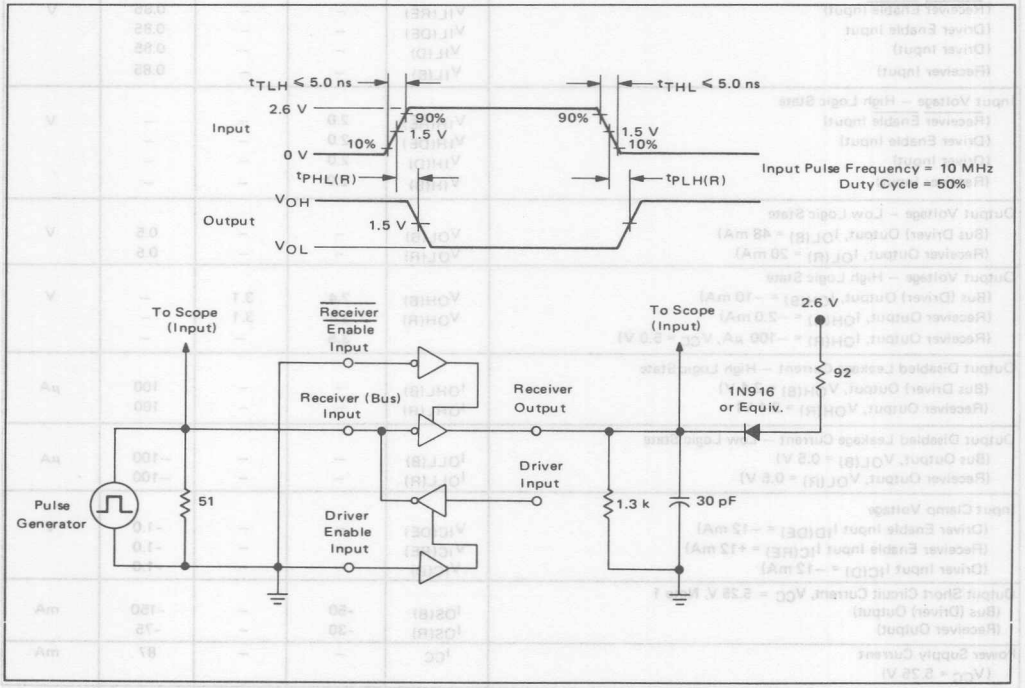


FIGURE 2 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM DRIVER INPUT TO BUS (DRIVER) OUTPUT, $t_{PLH(D)}$ AND $t_{PHL(D)}$

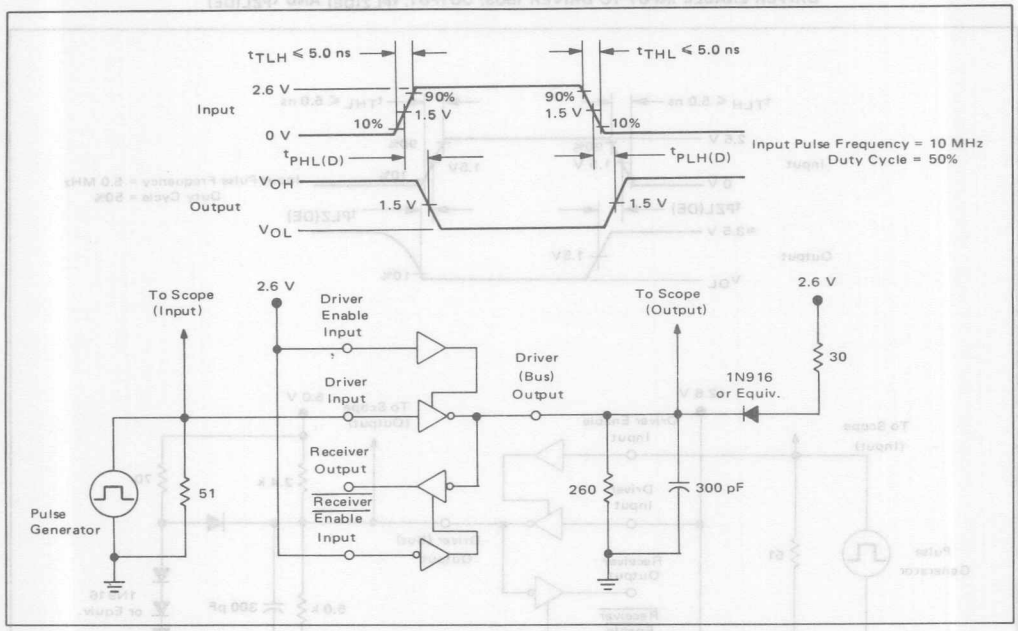
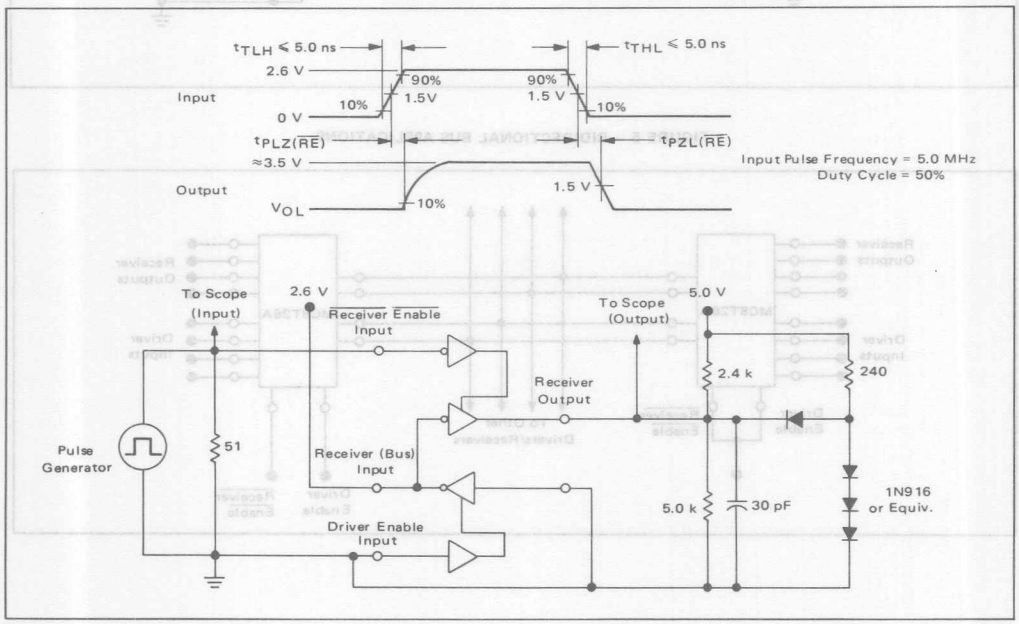


FIGURE 3 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM RECEIVER ENABLE INPUT TO RECEIVER OUTPUT, $t_{PLZ(RE)}$ AND $t_{PZL(RE)}$



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FIGURE 4 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIMES FROM DRIVER ENABLE INPUT TO DRIVER (BUS) OUTPUT, $t_{PLZ(DE)}$ AND $t_{PZL(DE)}$

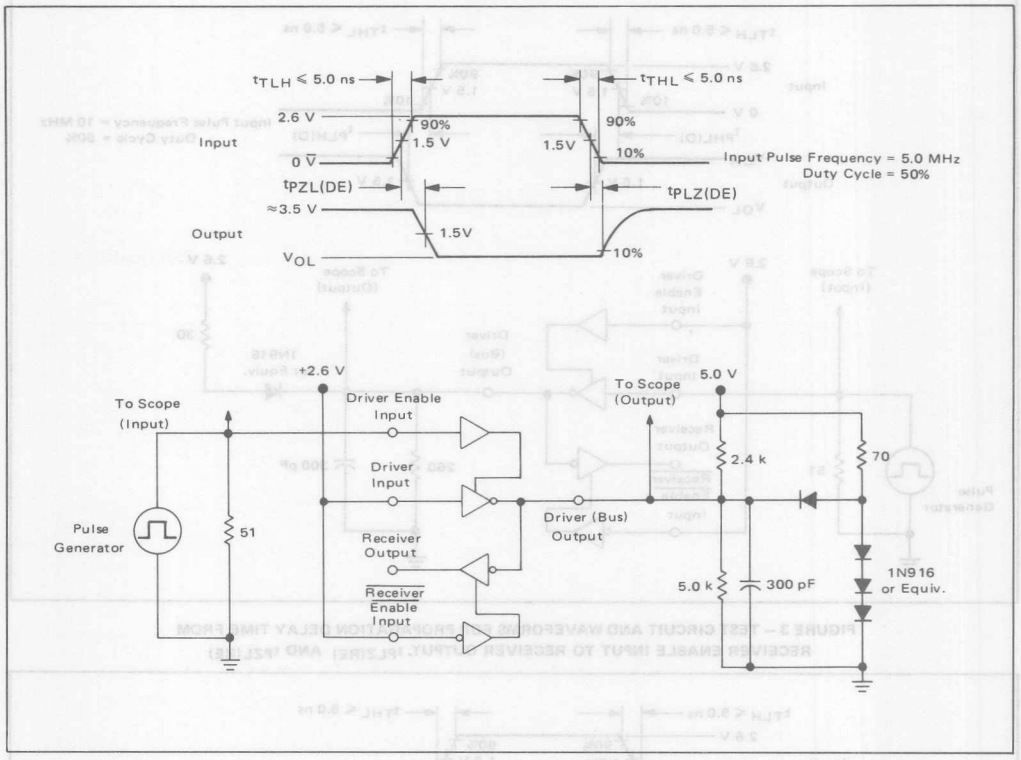
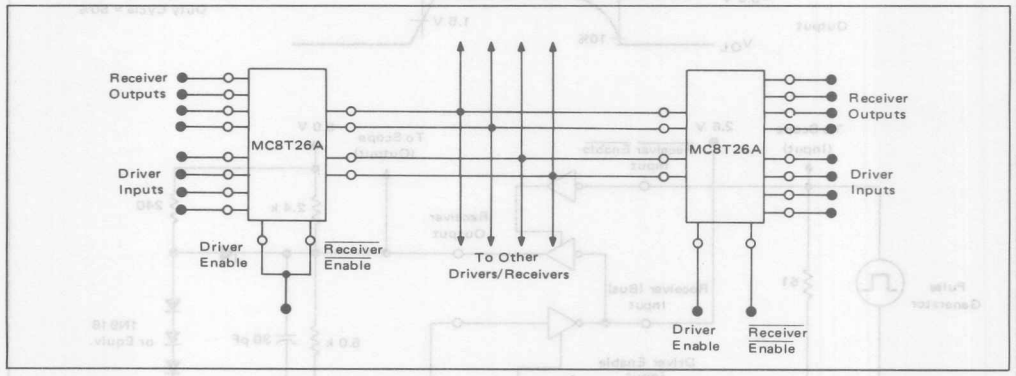


FIGURE 5 – BIDIRECTIONAL BUS APPLICATIONS



MOTOROLA

MC8T28
(MC6889)

NONINVERTING
QUAD THREE-STATE BUS TRANSCEIVER

This quad three-state bus transceiver features both excellent MOS or MPU compatibility, due to its high impedance PNP transistor input, and high-speed operation made possible by the use of Schottky diode clamping. Both the −48 mA driver and −20 mA receiver outputs are short circuit protected and employ three-state enabling inputs.

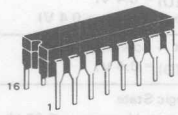
The device is useful as a bus extender in systems employing the M6800 family or other comparable MPU devices. The maximum input current of 200 μA at any of the device input pins assures proper operation despite the limited drive capability of the MPU chip. The inputs are also protected with Schottky-barrier diode clamps to suppress excessive undershoot voltages.

Propagation delay times for the driver portion are 17 ns maximum while the receiver portion runs 17 ns. The MC8T28 is identical to the NE8T28 and it operates from a single +5 V supply.

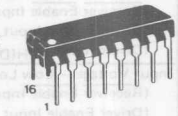
- High Impedance Inputs
- Single Power Supply
- High Speed Schottky Technology
- Three-State Drivers and Receivers
- Compatible with M6800 Family Microprocessor
- Non-Inverting

NONINVERTING
BUS TRANSCEIVER

MONOLITHIC SCHOTTKY INTEGRATED CIRCUITS



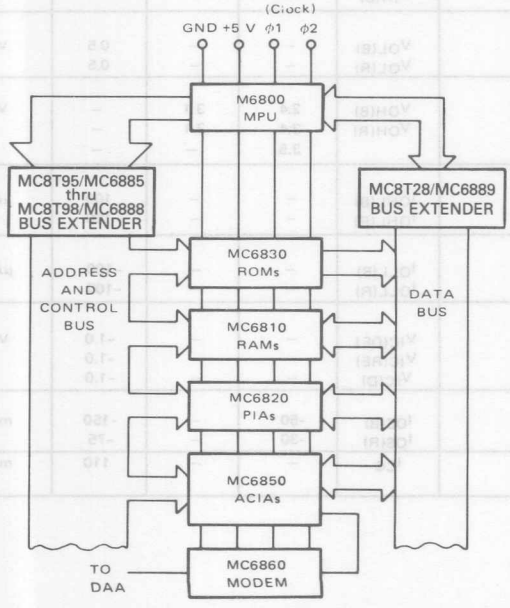
L SUFFIX
CERAMIC PACKAGE
CASE 620-10



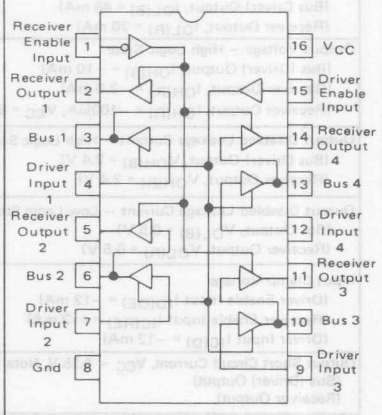
P SUFFIX
PLASTIC PACKAGE
CASE 648-06

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MICROPROCESSOR BUS EXTENDER APPLICATION



PIN CONNECTIONS — MC8T28 (MC6889)



ORDERING INFORMATION

Device	Alternate	Temperature Range	Package
MC8T28L	MC6889L	0 to +75°C	Ceramic DIP
MC8T28P	MC6889P	0 to +75°C	Plastic DIP

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.0	Vdc
Input Voltage	V_I	5.5	Vdc
Junction Temperature Ceramic Package Plastic Package	T_J	 175 150	°C
Operating Ambient Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS ($4.75\ V \leq V_{CC} \leq 5.25\ V$ and $0°C \leq T_A \leq 75°C$ unless otherwise noted.)

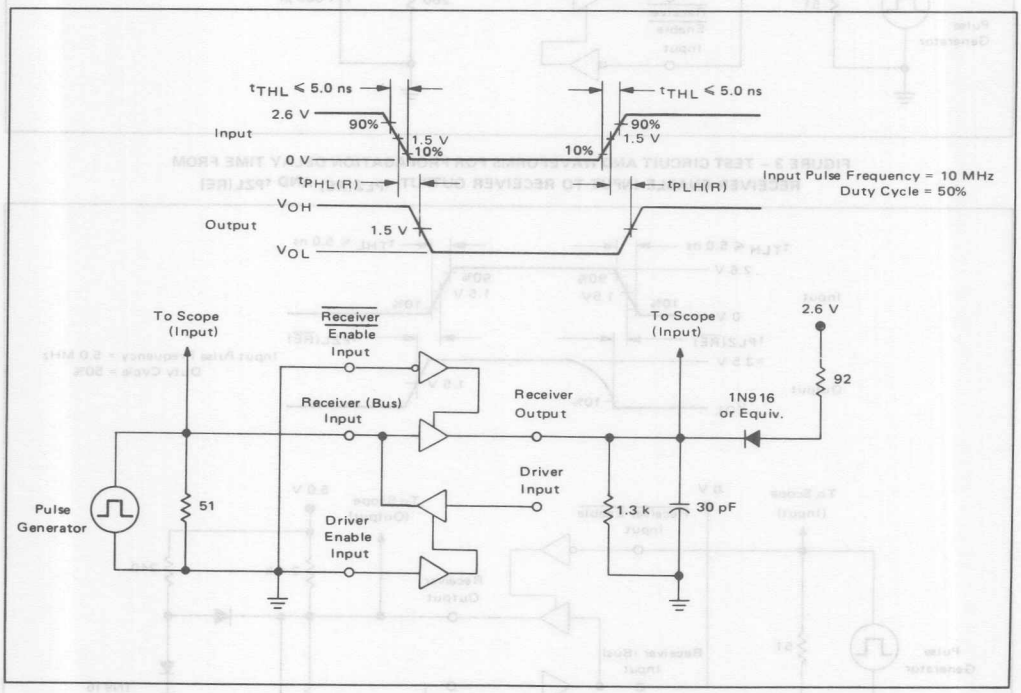
Characteristic	Symbol	Min	Typ	Max	Unit
Input Current — Low Logic State					
(Receiver Enable Input, $V_{IL(\overline{RE})} = 0.4$ V)	$I_{IL(\overline{RE})}$	–	–	-200	μA
(Driver Enable Input, $V_{IL(DE)} = 0.4$ V)	$I_{IL(DE)}$	–	–	-200	
(Driver Input, $V_{IL(D)} = 0.4$ V)	$I_{IL(D)}$	–	–	-200	
(Bus (Receiver) Input, $V_{IL(B)} = 0.4$ V)	$I_{IL(B)}$	–	–	-200	
Input Disabled Current — Low Logic State					
(Driver Input, $V_{IL(D)} = 0.4$ V)	$I_{IL(D)\ DIS}$	–	–	-25	μA
Input Current-High Logic State					
(Receiver Enable Input, $V_{IH(RE)} = 5.25$ V)	$I_{IH(\overline{RE})}$	–	–	25	μA
(Driver Enable Input, $V_{IH(DE)} = 5.25$ V)	$I_{IH(DE)}$	–	–	25	
(Driver Input, $V_{IH(D)} = 5.25$ V)	$I_{IH(D)}$	–	–	25	
Input Voltage — Low Logic State					
(Receiver Enable Input)	$V_{IL(\overline{RE})}$	–	–	0.85	V
(Driver Enable Input	$V_{IL(DE)}$	–	–	0.85	
(Driver Input)	$V_{IL(D)}$	–	–	0.85	
(Receiver Input)	$V_{IL(B)}$	–	–	0.85	
Input Voltage — High Logic State					
(Receiver Enable Input)	$V_{IH(\overline{RE})}$	2.0	–	–	V
(Driver Enable Input)	$V_{IH(DE)}$	2.0	–	–	
(Driver Input)	$V_{IH(D)}$	2.0	–	–	
(Receiver Input)	$V_{IH(B)}$	2.0	–	–	
Output Voltage — Low Logic State					
(Bus Driver) Output, $I_{OL(B)} = 48$ mA)	$V_{OL(B)}$	–	–	0.5	V
(Receiver Output, $I_{OL(R)} = 20$ mA)	$V_{OL(R)}$	–	–	0.5	
Output Voltage — High Logic State					
(Bus (Driver) Output, $I_{OH(B)} = -10$ mA)	$V_{OH(B)}$	2.4	3.1	–	V
(Receiver Output, $I_{OH(R)} = -2.0$ mA)	$V_{OH(R)}$	2.4	3.1	–	
(Receiver Output, $I_{OH(R)} = -100/\mu A$, $V_{CC} = 5.0$ V)		3.5	–	–	
Output Disabled Leakage Current — High Logic State					
(Bus Driver) Output, $V_{OH(B)} = 2.4$ V)	$I_{OHL(B)}$	–	–	100	μA
(Receiver Output, $V_{OH(R)} = 2.4$ V)	$I_{OHL(R)}$	–	–	100	
Output Disabled Leakage Current — Low Logic State					
(Bus Output, $V_{OL(B)} = 0.5$ V)	$I_{OLL(B)}$	–	–	-100	μA
(Receiver Output, $V_{OL(R)} = 0.5$ V)	$I_{OLL(R)}$	–	–	-100	
Input Clamp Voltage					
(Driver Enable Input $I_{ID(DE)} = -12$ mA)	$V_{IC(DE)}$	–	–	-1.0	V
(Receiver Enable Input $I_{IC(RE)} = +12$ mA)	$V_{IC(RE)}$	–	–	-1.0	
(Driver Input $I_{IC(D)} = -12$ mA)	$V_{IC(D)}$	–	–	-1.0	
Output Short Circuit Current, $V_{CC} = 5.25$ V, Note 1					
(Bus (Driver) Output)	$I_{OS(B)}$	-50	–	-150	mA
(Receiver Output)	$I_{OS(R)}$	-30	–	-75	
Power Supply Current					
($V_{CC} = 5.25$ V)	I_{CC}	–	–	110	mA

Note 1. Only one output may be short-circuited at a time.

SWITCHING CHARACTERISTICS (Unless otherwise noted, V_{CC} = 5.0 V and T_A = 25°C)

Characteristic	Symbol	Min	Max	Unit
Propagation Delay Time—Receiver (C_L = 30 pF)	$t_{PLH(R)}$ $t_{PHL(R)}$	–	17 17	ns
Propagation Delay Time—Driver (C_L = 300 pF)	$t_{PLH(D)}$ $t_{PHL(D)}$	–	17 17	ns
Propagation Delay Time—Enable (C_L = 30 pF) – Receiver	$t_{PZL(R)}$ $t_{PLZ(R)}$	– –	23 18	ns
– Driver Enable (C_L 300 pF)	$t_{PZL(D)}$ $t_{PLZ(D)}$	– –	28 23	

FIGURE 1 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY FROM BUS (RECEIVER) INPUT TO RECEIVER OUTPUT, $t_{PLH(R)}$ AND $t_{PHL(R)}$



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FIGURE 2 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM DRIVER INPUT TO BUS (DRIVER) OUTPUT, $t_{PLH(D)}$ AND $t_{PHL(D)}$

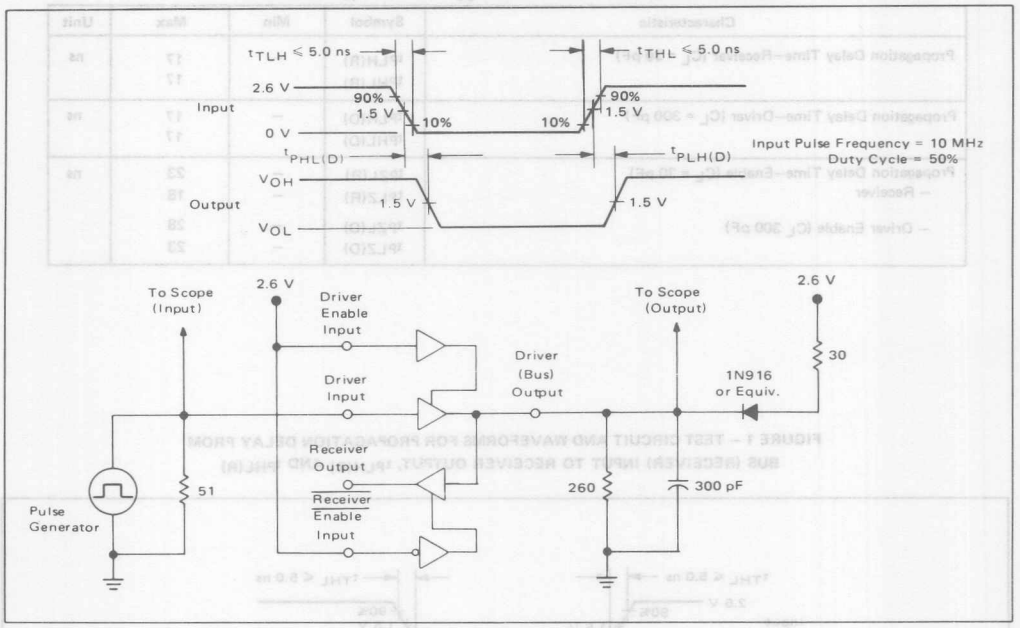


FIGURE 3 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM RECEIVER ENABLE INPUT TO RECEIVER OUTPUT, $t_{PLZ(RE)}$ AND $t_{PZL(RE)}$

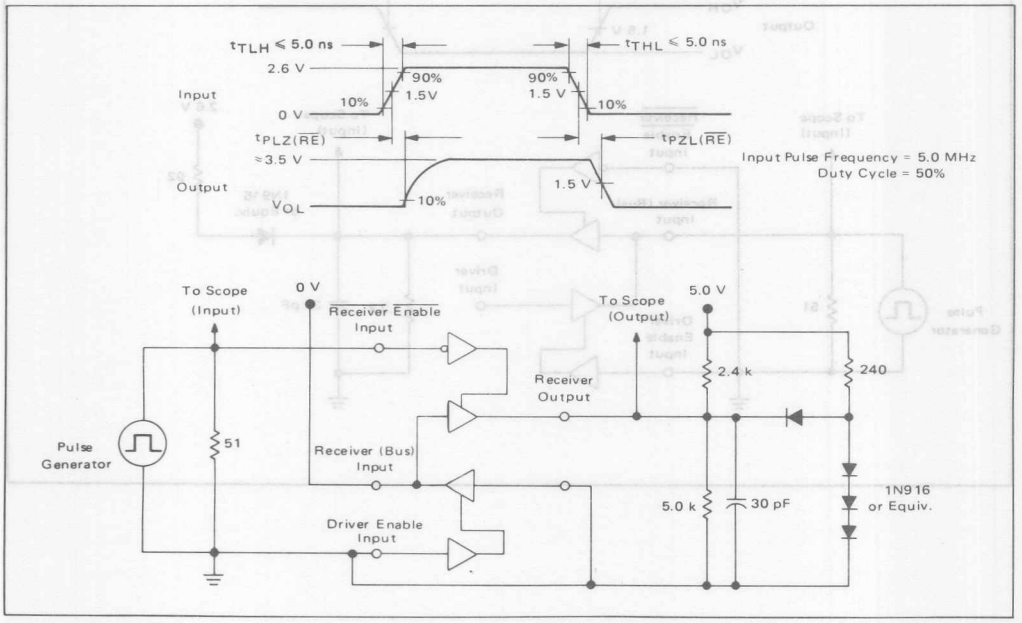


FIGURE 4 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIMES FROM DRIVER ENABLE INPUT TO DRIVER (BUS) OUTPUT, $t_{PLZ(DE)}$ AND $t_{PZL(DE)}$

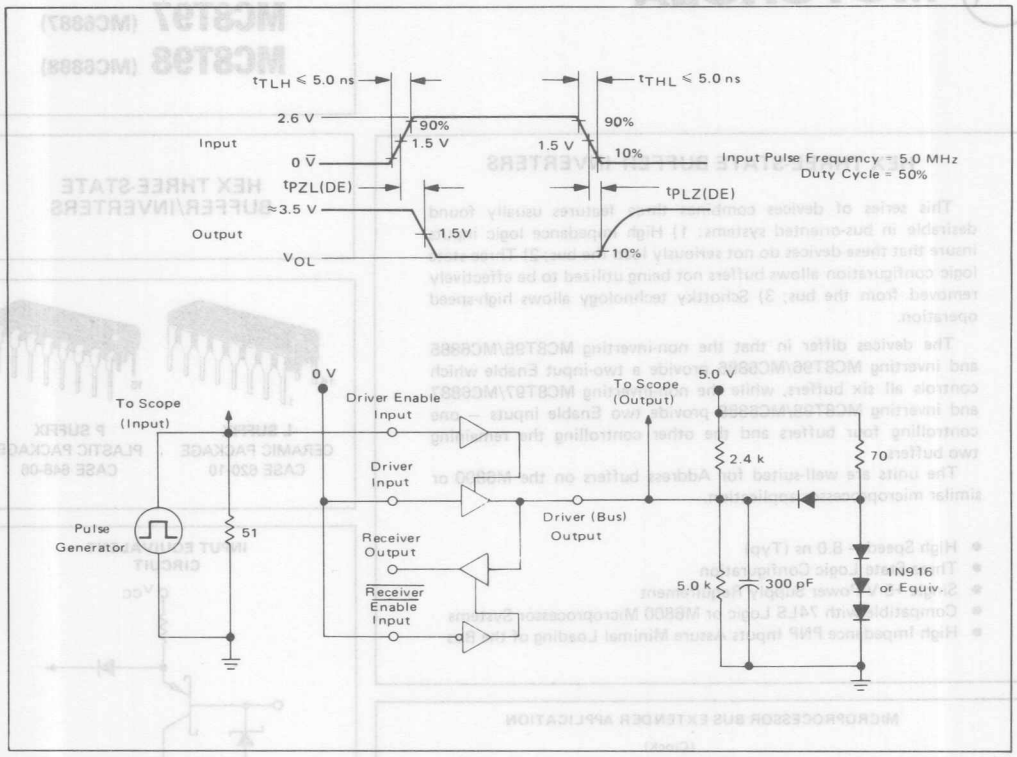
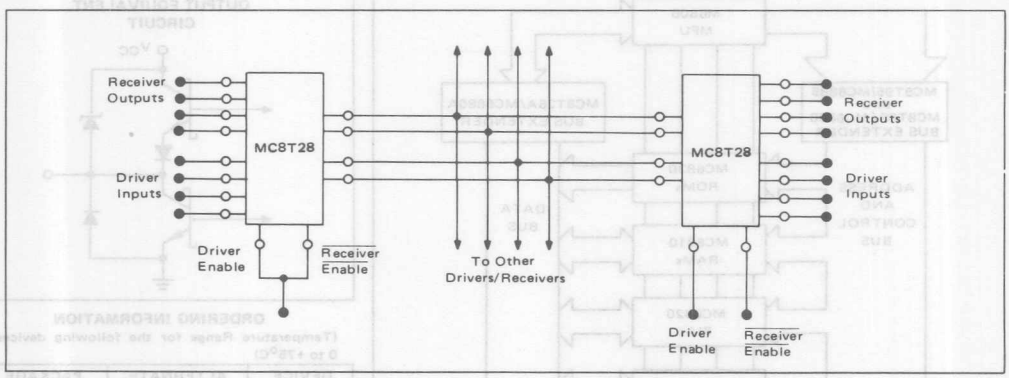


FIGURE 5 – BIDIRECTIONAL BUS APPLICATIONS



7

MOTOROLA

MC8T95 (MC6885)
MC8T96 (MC6886)
MC8T97 (MC6887)
MC8T98 (MC6888)

HEX THREE-STATE BUFFER INVERTERS

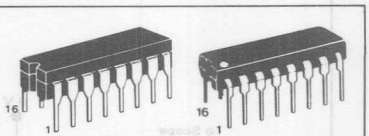
This series of devices combines three features usually found desirable in bus-oriented systems: 1) High impedance logic inputs insure that these devices do not seriously load the bus; 2) Three-state logic configuration allows buffers not being utilized to be effectively removed from the bus; 3) Schottky technology allows high-speed operation.

The devices differ in that the non-inverting MC8T95/MC6885 and inverting MC8T96/MC6886 provide a two-input Enable which controls all six buffers, while the non-inverting MC8T97/MC6887 and inverting MC8T98/MC6888 provide two Enable inputs – one controlling four buffers and the other controlling the remaining two buffers.

The units are well-suited for Address buffers on the M6800 or similar microprocessor application.

- High Speed – 8.0 ns (Typ)
- Three-State Logic Configuration
- Single +5 V Power Supply Requirement
- Compatible with 74LS Logic or M6800 Microprocessor Systems
- High Impedance PNP Inputs Assure Minimal Loading of the Bus

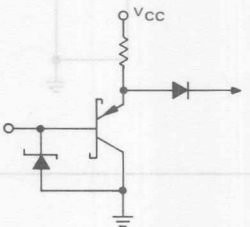
HEX THREE-STATE BUFFER/INVERTERS



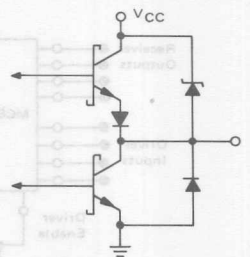
L SUFFIX
CERAMIC PACKAGE
CASE 620-10

P SUFFIX
PLASTIC PACKAGE
CASE 648-06

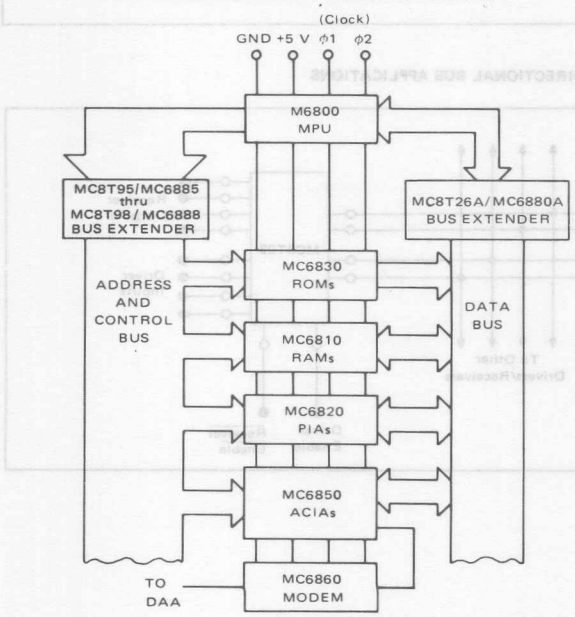
INPUT EQUIVALENT CIRCUIT



OUTPUT EQUIVALENT CIRCUIT



MICROPROCESSOR BUS EXTENDER APPLICATION



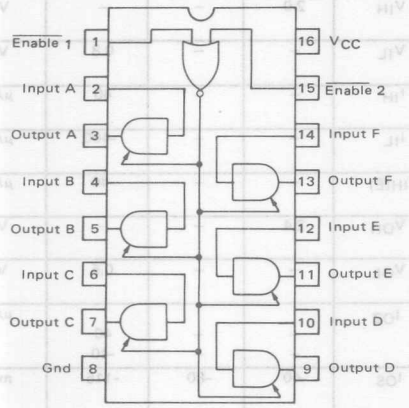
ORDERING INFORMATION

(Temperature Range for the following devices = 0 to +75°C)

DEVICE	ALTERNATE	PACKAGE
MC8T95L	MC6885L	Ceramic DIP
MC8T96L	MC6886L	Ceramic DIP
MC8T97L	MC6887L	Ceramic DIP
MC8T98L	MC6888L	Ceramic DIP
MC8T95P	MC6885P	Plastic DIP
MC8T96P	MC6886P	Plastic DIP
MC8T97P	MC6887P	Plastic DIP
MC8T98P	MC6888P	Plastic DIP

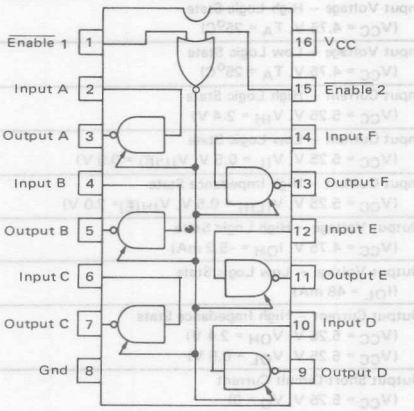
PIN CONNECTIONS AND TRUTH TABLES

MC8T95/MC8885



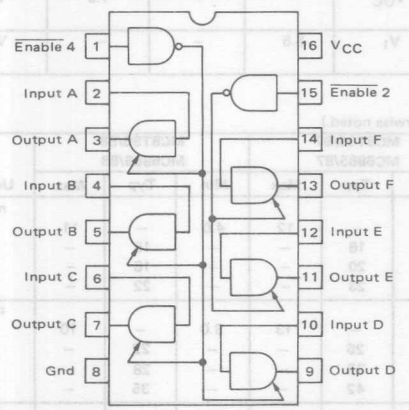
Enable 2	Enable 1	Input	Output
L	L	L	L
L	L	H	H
L	H	X	Z
H	L	X	Z
H	H	X	Z

MC8T96/MC6886



Enable 2	Enable 1	Input	Output
L	L	L	H
L	L	H	L
L	H	X	Z
H	L	X	Z
H	H	X	Z

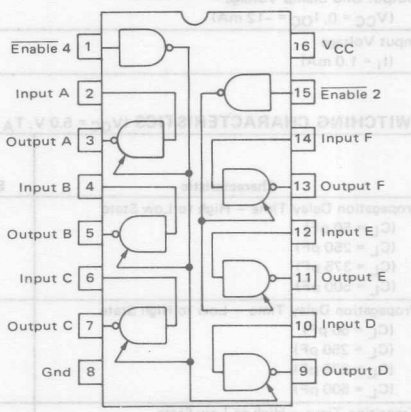
MC8T97/MC6887



Enable	Input	Output
L	L	L
L	H	H
H	X	Z

L = Low Logic State
H = High Logic State
Z = Third (High Impedance) State
X = Irrelevant

MC8T98/MC6888



Enable	Input	Output
L	L	H
L	H	L
H	X	Z

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.0	Vdc
Input Voltage	V_I	5.5	Vdc
Operating Ambient Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J		°C
Plastic Package		150	
Ceramic Package		175	

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, $0^{\circ}C \leq T_A \leq 75^{\circ}C$ and $4.75\ V \leq V_{CC} \leq 5.25\ V$)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage – High Logic State (V_{CC} = 4.75 V, T_A = 25°C)	V_{IH}	2.0	–	–	V
Input Voltage – Low Logic State (V_{CC} = 4.75 V, T_A = 25°C)	V_{IL}	–	–	0.8	V
Input Current – High Logic State (V_{CC} = 5.25 V, V_{IH} = 2.4 V)	I_{IH}	–	–	40	μA
Input Current – Low Logic State (V_{CC} = 5.25 V, V_{IL} = 0.5 V, $V_{IL(\overline{E})}$ = 0.5 V)	I_{IL}	–	–	-400	μA
Input Current – High Impedance State (V_{CC} = 5.25 V, $V_{IL(I)}$ = 0.5 V, $V_{IH(\overline{E})}$ = 2.0 V)	$I_{IH(\overline{E})}$	–	–	-40	μA
Output Voltage – High Logic State (V_{CC} = 4.75 V, I_{OH} = -5.2 mA)	V_{OH}	2.4	–	–	V
Output Voltage – Low Logic State (I_{OL} = 48 mA)	V_{OL}	–	–	0.5	V
Output Current – High Impedance State (V_{CC} = 5.25 V, V_{OH} = 2.4 V) (V_{CC} = 5.25 V, V_{OL} = 0.5 V)	I_{OZ}	– –	– –	40 -40	μA
Output Short-Circuit Current (V_{CC} = 5.25 V, V_O = 0) (only one output can be shorted at a time)	I_{OS}	-40	-80	-115	mA
Power Supply Current (V_{CC} = 5.25 V) MC8T95, MC8T97, MC6885, MC6887 MC8T96, MC8T98, MC6886, MC6888	I_{CC}	– –	65 59	98 89	mA
Input Clamp Voltage (V_{CC} = 4.75 V, I_{IC} = -12 mA)	V_{IC}	–	–	-1.5	V
Output V_{CC} Clamp Voltage (V_{CC} = 0, I_{OC} = 12 mA)	V_{OC}	–	–	1.5	V
Output Gnd Clamp Voltage (V_{CC} = 0, I_{OC} = -12 mA)	V_{OC}	–	–	-1.5	V
Input Voltage (I_I = 1.0 mA)	V_I	5.5	–	–	V

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	MC8T95/97 MC6885/87 Min	MC8T95/97 MC6885/87 Typ	MC8T95/97 MC6885/87 Max	MC8T96/98 MC6886/88 Min	MC8T96/98 MC6886/88 Typ	MC8T96/98 MC6886/88 Max	Unit
Propagation Delay Time – High to Low State	t_{PHL}							ns
(C_L = 50 pF)		3.0	–	12	4.0	–	11	
(C_L = 250 pF)		–	16	–	–	15	–	
(C_L = 375 pF)		–	20	–	–	18	–	
(C_L = 500 pF)		–	23	–	–	22	–	
Propagation Delay Time – Low to High State	t_{PLH}							ns
(C_L = 50 pF)		3.0	–	13	3.0	–	10	
(C_L = 250 pF)		–	25	–	–	22	–	
(C_L = 375 pF)		–	33	–	–	28	–	
(C_L = 500 pF)		–	42	–	–	35	–	
Transition Time – High to Low State	t_{THL}							ns
(C_L = 250 pF)		–	10	–	–	10	–	
(C_L = 375 pF)		–	11	–	–	13	–	
(C_L = 500 pF)		–	14	–	–	15	–	
Transition Time – Low to High State	t_{TLH}							ns
(C_L = 250 pF)		–	32	–	–	28	–	
(C_L = 375 pF)		–	42	–	–	38	–	
(C_L = 500 pF)		–	60	–	–	53	–	
Propagation Delay Time – High State to Third State (C_L = 5.0 pF)	$t_{PHZ(\overline{E})}$	–	–	10	–	–	10	ns
Propagation Delay Time – Low State to Third State (C_L = 5.0 pF)	$t_{PLZ(\overline{E})}$	–	–	12	–	–	16	ns
Propagation Delay Time – Third State to High State (C_L = 50 pF)	$t_{PZH(\overline{E})}$	–	–	25	–	–	22	ns
Propagation Delay Time – Third State to Low State (C_L = 50 pF)	$t_{PZL(\overline{E})}$	–	–	25	–	–	24	ns

7

FIGURE 1 – TEST CIRCUIT FOR SWITCHING CHARACTERISTICS

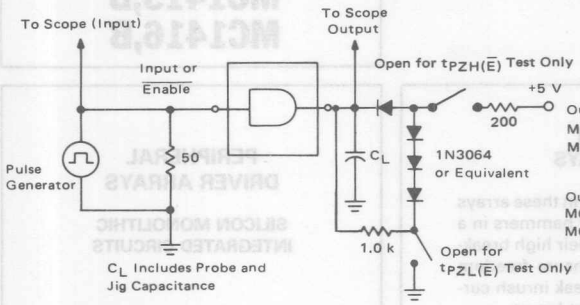


FIGURE 2 – WAVEFORMS FOR PROPAGATION DELAY TIMES INPUT TO OUTPUT

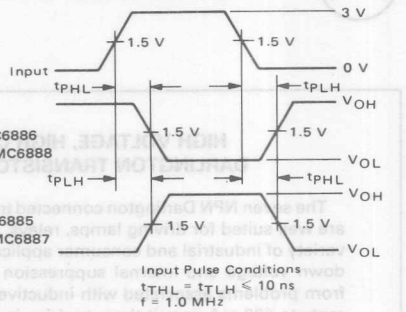
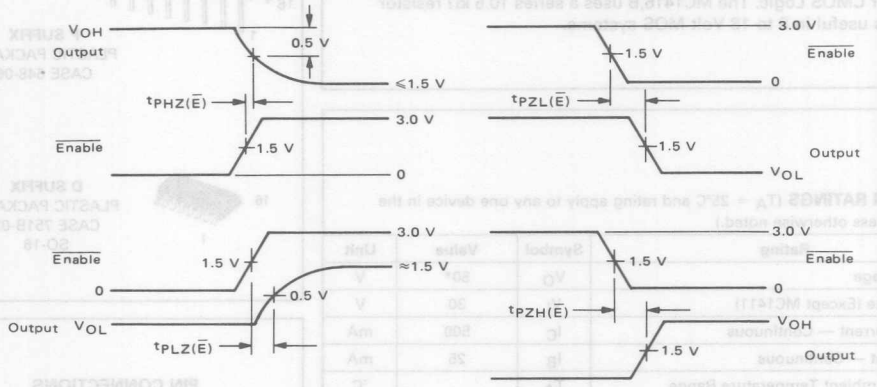


FIGURE 3 – WAVEFORMS FOR PROPAGATION DELAY TIMES – $\overline{\text{ENABLE}}$ TO OUTPUT



H = High-Logic State, L = Low-Logic State, Z = High Impedance State

7

MOTOROLA

MC1411,B
MC1412,B
MC1413,B
MC1416,B

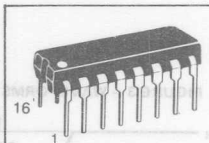
HIGH VOLTAGE, HIGH CURRENT DARLINGTON TRANSISTOR ARRAYS

The seven NPN Darlington connected transistors in these arrays are well suited for driving lamps, relays, or printer hammers in a variety of industrial and consumer applications. Their high breakdown voltage and internal suppression diodes insure freedom from problems associated with inductive loads. Peak inrush currents to 600 mA permit them to drive incandescent lamps.

The MC1411,B device is a general purpose array for use with DTL, TTL, PMOS, or CMOS Logic. The MC1412,B contains a zener diode and resistor in series with the input to limit input current for use with 14 to 25 Volt PMOS Logic. The MC1413,B with a 2.7 kΩ series input resistor is well suited for systems utilizing a 5 Volt TTL or CMOS Logic. The MC1416,B uses a series 10.5 kΩ resistor and is useful in 8 to 18 Volt MOS systems.

PERIPHERAL DRIVER ARRAYS

SILICON MONOLITHIC INTEGRATED CIRCUITS



P SUFFIX
PLASTIC PACKAGE
CASE 648-06



D SUFFIX
PLASTIC PACKAGE
CASE 751B-03
SO-16

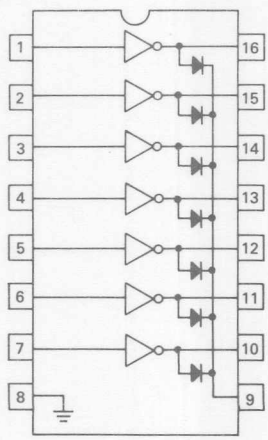
7

MAXIMUM RATINGS (T_A = 25°C and rating apply to any one device in the package unless otherwise noted.)

Rating	Symbol	Value	Unit
Output Voltage	V_O	50*	V
Input Voltage (Except MC1411)	V_I	30	V
Collector Current — Continuous	I_C	500	mA
Base Current — Continuous	I_B	25	mA
Operating Ambient Temperature Range MC1411-16 MC1411B-16B	T_A	 −20 to +85 −40 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Junction Temperature	T_J	150	°C

Maximum Package Power Dissipation (See Thermal Information Section)
*Higher voltage selection available. See your local representative.

PIN CONNECTIONS



ORDERING INFORMATION

MC1411P (ULN2001A)	MC1411D	−20° to +85°C
MC1412P (ULN2002A)	MC1412D	
MC1413P (ULN2003A)	MC1413D	
MC1416P (ULN2004A)	MC1416D	
MC1411BP (ULQ2001A)	MC1411BD	−40° to +85°C
MC1412BP (ULQ2002A)	MC1412BD	
MC1413BP (ULQ2003A)	MC1413BD	
MC1416BP (ULQ2004A)	MC1416BD	

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Output Leakage Current		I_{CEX}				μA
(*V_O = 50 V, T_A = +85°C)	All Types		—	—	100	
(*V_O = 50 V, T_A = +25°C)	All Types		—	—	50	
(*V_O = 50 V, T_A = +85°C, V_I = 6.0 V)	MC1412,B		—	—	500	
(*V_O = 50 V, T_A = +85°C, V_I = 1.0 V)	MC1416,B		—	—	500	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$				V
(I_C = 350 mA, I_B = 500 μA)	All Types		—	1.1	1.6	
(I_C = 200 mA, I_B = 350 μA)	All Types		—	0.95	1.3	
(I_C = 100 mA, I_B = 250 μA)	All Types		—	0.85	1.1	
Input Current — On Condition		$I_{I(on)}$				mA
(V_I = 17 V)	MC1412,B		—	0.85	1.3	
(V_I = 3.85 V)	MC1413,B		—	0.93	1.35	
(V_I = 5.0 V)	MC1416,B		—	0.35	0.5	
(V_I = 12 V)	MC1416,B		—	1.0	1.45	
Input Voltage — On Condition		$V_{I(on)}$				V
(V_{CE} = 2.0 V, I_C = 300 mA)	MC1412,B		—	—	13	
(V_{CE} = 2.0 V, I_C = 200 mA)	MC1413,B		—	—	2.4	
(V_{CE} = 2.0 V, I_C = 250 mA)	MC1413,B		—	—	2.7	
(V_{CE} = 2.0 V, I_C = 300 mA)	MC1413,B		—	—	3.0	
(V_{CE} = 2.0 V, I_C = 125 mA)	MC1416,B		—	—	5.0	
(V_{CE} = 2.0 V, I_C = 200 mA)	MC1416,B		—	—	6.0	
(V_{CE} = 2.0 V, I_C = 275 mA)	MC1416,B		—	—	7.0	
(V_{CE} = 2.0 V, I_C = 350 mA)	MC1416,B		—	—	8.0	
Input Current — Off Condition (I_C = 500 μA, T_A = +85°C)	All Types	$I_{I(off)}$	50	100	—	μA
DC Current Gain (V_{CE} = 2.0 V, I_C = 350 mA)	MC1411,B	h_{FE}	1000	—	—	—
Input Capacitance		C_I	—	15	30	pF
Turn-On Delay Time (50% E_I to 50% E_O)		t_{on}	—	0.25	1.0	μs
Turn-Off Delay Time (50% E_I to 50% E_O)		t_{off}	—	0.25	1.0	μs
Clamp Diode Leakage Current (V_R = 50 V)	T_A = +25°C	I_R	—	—	50	μA
	T_A = +85°C		—	—	100	
Clamp Diode Forward Voltage (I_F = 350 mA)		V_F	—	1.5	2.0	V

*Higher voltage selections available, contact your local representative.

TYPICAL PERFORMANCE CURVES — T_A = 25°C

FIGURE 1 — OUTPUT CURRENT versus INPUT VOLTAGE

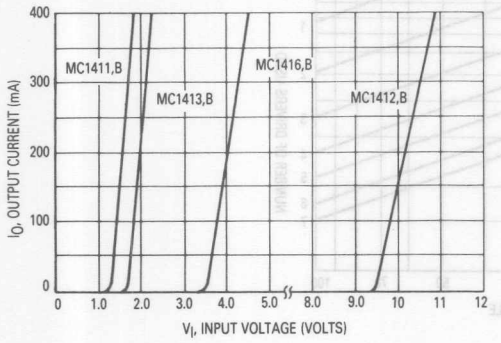
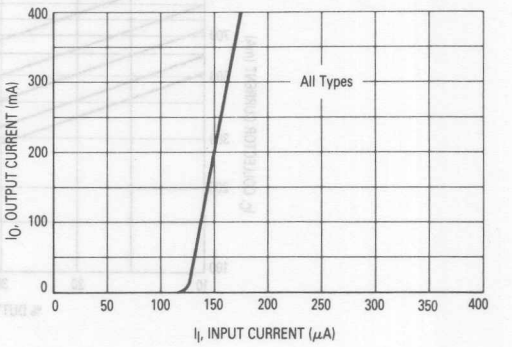


FIGURE 2 — OUTPUT CURRENT versus INPUT CURRENT



TYPICAL CHARACTERISTIC CURVES – T_A = 25°C (continued)

FIGURE 3 — TYPICAL OUTPUT CHARACTERISTICS

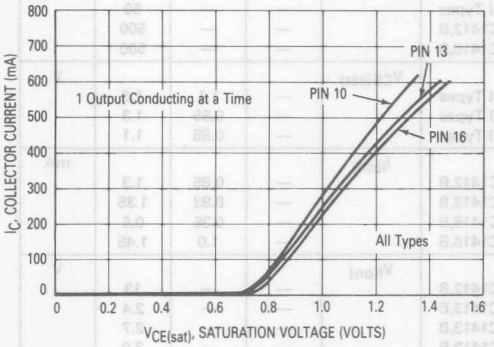


FIGURE 4 — INPUT CHARACTERISTICS — MC1412,B

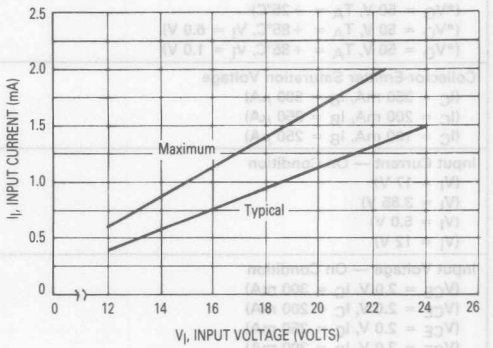


FIGURE 5 — INPUT CHARACTERISTICS — MC1413,B

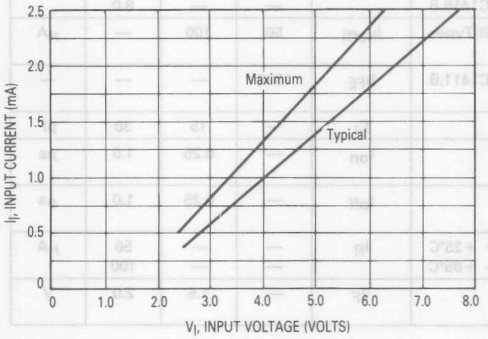


FIGURE 6 — INPUT CHARACTERISTICS — MC1416,B

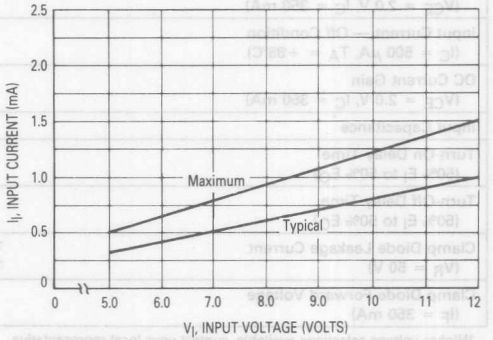
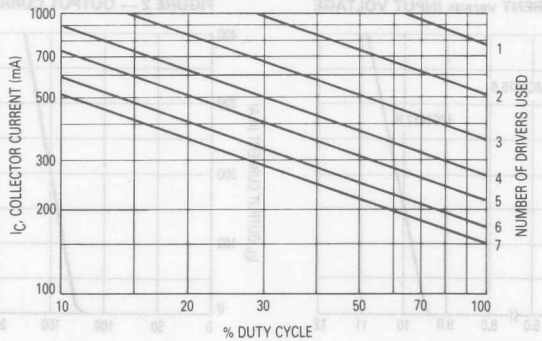
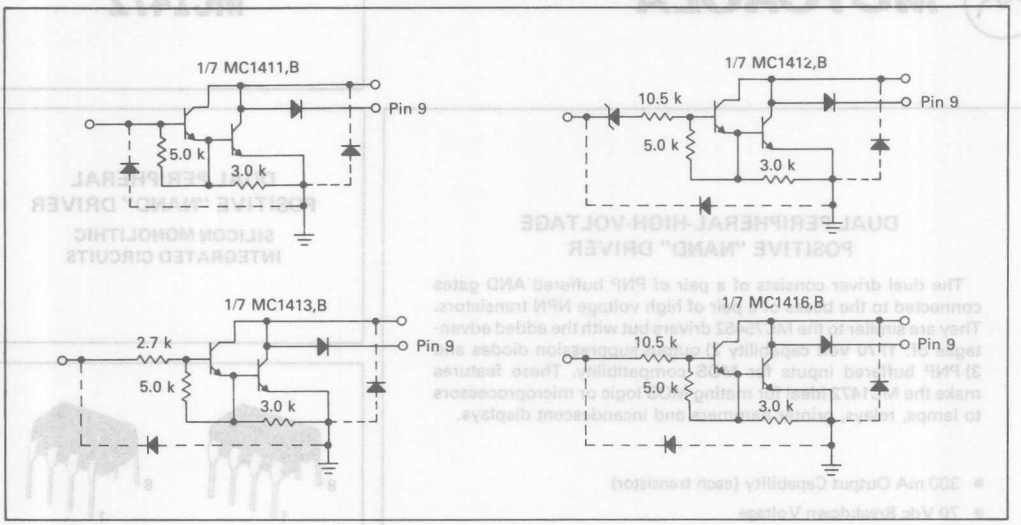


FIGURE 7 — MAXIMUM COLLECTOR CURRENT versus DUTY CYCLE (AND NUMBER OF DRIVERS IN USE)



REPRESENTATIVE CIRCUIT SCHEMATICS



7

MOTOROLA

MC1472

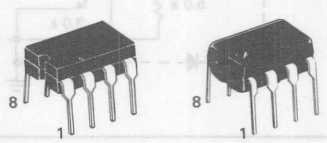
DUAL PERIPHERAL-HIGH-VOLTAGE POSITIVE "NAND" DRIVER

The dual driver consists of a pair of PNP buffered AND gates connected to the bases of a pair of high voltage NPN transistors. They are similar to the MC75452 drivers but with the added advantages of: 1) 70 Volt capability 2) output suppression diodes and 3) PNP buffered inputs for MOS compatibility. These features make the MC1472 ideal for mating MOS logic or microprocessors to lamps, relays, printer hammers and incandescent displays.

- 300 mA Output Capability (each transistor)
- 70 Vdc Breakdown Voltage
- Internal Output Clamp Diodes
- Low Input Loading for MOS Compatibility (PNP buffered)

DUAL PERIPHERAL POSITIVE "NAND" DRIVER

SILICON MONOLITHIC INTEGRATED CIRCUITS



U SUFFIX
CERAMIC PACKAGE
CASE 693-02

P1 SUFFIX
PLASTIC PACKAGE
CASE 626-05

MAXIMUM RATINGS (T_A = 25°C)

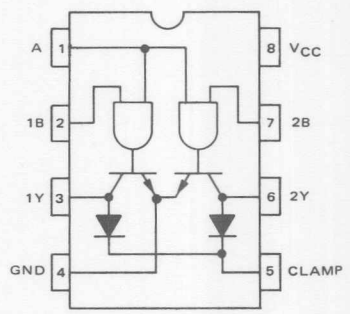
Rating	Value	Unit
Supply Voltage	7.0	Volts
Input Voltage	5.5	Volts
Output Voltage	80	Volts
Clamp Voltage	80	Volts
Output Current (Continuous)	300	mA
Operating Junction Temperature Ceramic Package Plastic Package	 +175 +150	°C
Storage Temperature Range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	Volts
Operating Ambient Temperature	T_A	0	70	°C
Output Voltage	V_O	V_{CC}	70	Volts
Clamp Voltage	V_C	V_O	70	Volts

ORDERING INFORMATION

Device	Temperature Range	Package
MC1472U	0 to +70°C	Ceramic DIP
MC1472P1	0 to +70°C	Plastic DIP



Positive Logic: Y=AB*

TRUTH TABLE

A	B	Y
L	L	H ("OFF" STATE)
L	H	H ("OFF" STATE)
H	L	H ("OFF" STATE)
H	H	L ("ON" STATE)

H = Logic One
L = Logic Zero

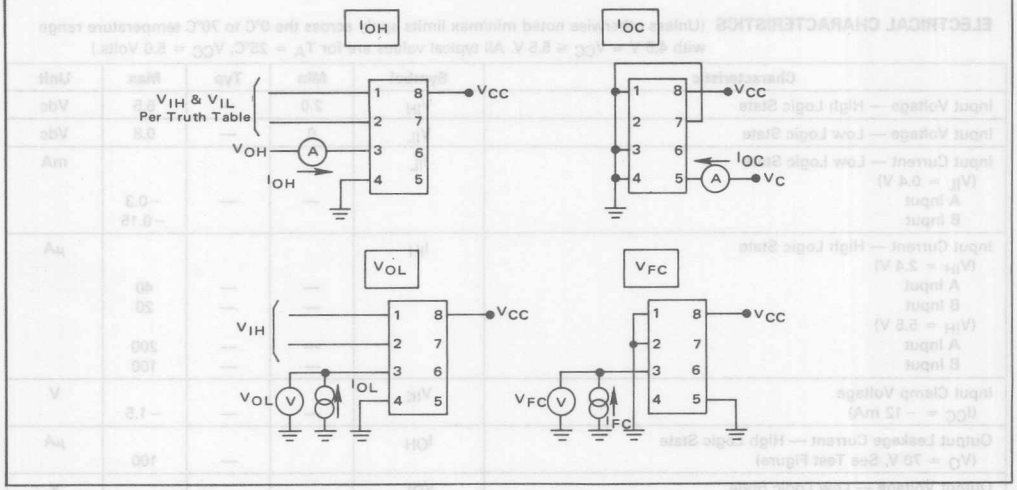
ELECTRICAL CHARACTERISTICS (Unless otherwise noted min/max limits apply across the 0°C to 70°C temperature range with 4.5 V ≤ V_{CC} ≤ 5.5 V. All typical values are for T_A = 25°C, V_{CC} = 5.0 Volts.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage — High Logic State	V_{IH}	2.0	—	5.5	Vdc
Input Voltage — Low Logic State	V_{IL}	0	—	0.8	Vdc
Input Current — Low Logic State (V_{IL} = 0.4 V) A Input B Input	I_{IL}	 — —	 — —	 −0.3 −0.15	mA
Input Current — High Logic State (V_{IH} = 2.4 V) A Input B Input (V_{IH} = 5.5 V) A Input B Input	I_{IH}	 — — — —	 — — — —	 40 20 200 100	μA
Input Clamp Voltage (I_{CC} = −12 mA)	V_{IK}	—	—	−1.5	V
Output Leakage Current — High Logic State (V_O = 70 V, See Test Figure)	I_{OH}		—	100	μA
Output Voltage — Low Logic State (I_{OL} = 100 mA) (I_{OL} = 300 mA)	V_{OL}	 — —	 — —	 0.4 0.7	V
Output Clamp Diode Leakage Current (V_C = 70 V, See Test Figure)	I_{OC}	—	—	100	V
Output Clamp Forward Voltage (I_{FC} = 300 mA, See Test Figure)	V_{FC}	—	—	1.7	V
Power Supply Current (All Inputs at V_{IH}) (All Inputs at V_{IL})	I_{CC}	 — —	 — —	 70 15	mA

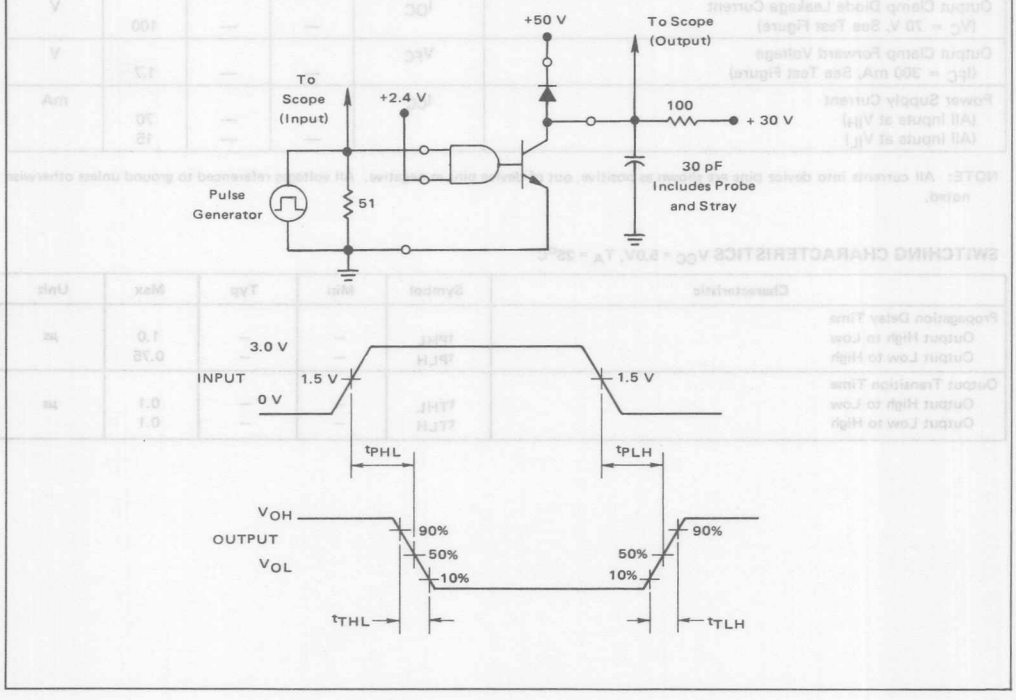
NOTE: All currents into device pins are shown as positive, out of device pins as negative. All voltages referenced to ground unless otherwise noted.

SWITCHING CHARACTERISTICS V_{CC} = 5.0V, T_A = 25°C

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time Output High to Low Output Low to High	 t_{PHL} t_{PLH}	 – –	 – –	 1.0 0.75	μs
Output Transition Time Output High to Low Output Low to High	 t_{THL} t_{TLH}	 – –	 – –	 0.1 0.1	μs



SWITCHING TEST CIRCUIT AND WAVEFORM



7

MOTOROLA

MC1488

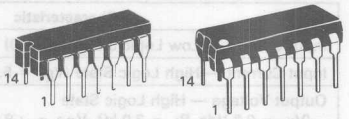
QUAD MDTL LINE DRIVER
EIA-232C
SILICON MONOLITHIC INTEGRATED CIRCUIT

QUAD LINE DRIVER

The MC1488 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. EIA-232C.

Features:

- Current Limited Output ±10 mA typ
- Power-Off Source Impedance 300 Ohms min
- Simple Slew Rate Control with External Capacitor
- Flexible Operating Supply Range
- Compatible with All Motorola MDTL and MTTL Logic Families



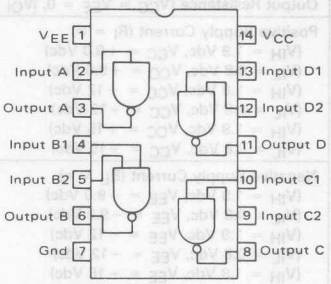
L SUFFIX
CERAMIC PACKAGE
CASE 632-08

P SUFFIX
PLASTIC PACKAGE
CASE 646-06

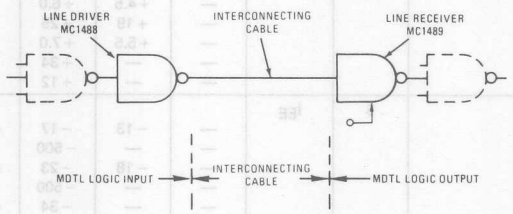
D SUFFIX
PLASTIC PACKAGE
CASE 751A-02
SO-14



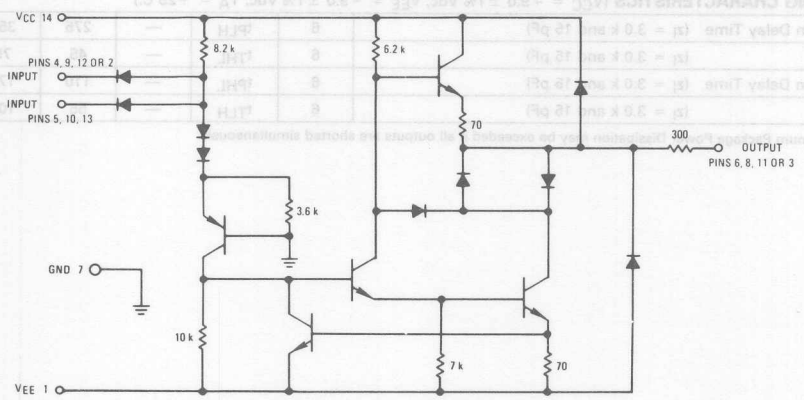
PIN CONNECTIONS



TYPICAL APPLICATION



CIRCUIT SCHEMATIC
(1/4 OF CIRCUIT SHOWN)



7

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+15 −15	Vdc
Input Voltage Range	V_{IR}	$-15 \leq V_{IR} \leq 7.0$	Vdc
Output Signal Voltage	V_O	±15	Vdc
Power Derating (Package Limitation, Ceramic and Plastic Dual-In-Line Package) Derate above T_A = +25°C	P_D $1/R_{\theta JA}$	1000 6.7	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	−65 to +175	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +9.0 ±1% Vdc, V_{EE} = −9.0 ±1% Vdc, T_A = 0 to 75°C unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Input Current — Low Logic State (V_{IL} = 0)	1	I_{IL}	—	1.0	1.6	mA
Input Current — High Logic State (V_{IH} = 5.0 V)	1	I_{IH}	—	—	10	µA
Output Voltage — High Logic State (V_{IL} = 0.8 Vdc, R_L = 3.0 kΩ, V_{CC} = +9.0 Vdc, V_{EE} = −9.0 Vdc) (V_{IL} = 0.8 Vdc, R_L = 3.0 kΩ, V_{CC} = +13.2 Vdc, V_{EE} = −13.2 Vdc)	2	V_{OH}	 +6.0 +9.0	 +7.0 +10.5	 — —	Vdc
Output Voltage — Low Logic State (V_{IH} = 1.9 Vdc, R_L = 3.0 kΩ, V_{CC} = +9.0 Vdc, V_{EE} = −9.0 Vdc) (V_{IH} = 1.9 Vdc, R_L = 3.0 kΩ, V_{CC} = +13.2 Vdc, V_{EE} = −13.2 Vdc)	2	V_{OL}	 −6.0 −9.0	 −7.0 −10.5	 — —	Vdc
Positive Output Short-Circuit Current, Note 1	3	I_{OS+}	+6.0	+10	+12	mA
Negative Output Short-Circuit Current, Note 1	3	I_{OS-}	−6.0	−10	−12	mA
Output Resistance (V_{CC} = V_{EE} = 0, $\|V_O\|$ = ±2.0 V)	4	r_o	300	—	—	Ohms
Positive Supply Current (R_l = ∞) (V_{IH} = 1.9 Vdc, V_{CC} = +9.0 Vdc) (V_{IL} = 0.8 Vdc, V_{CC} = +9.0 Vdc) (V_{IH} = 1.9 Vdc, V_{CC} = +12 Vdc) (V_{IL} = 0.8 Vdc, V_{CC} = +12 Vdc) (V_{IH} = 1.9 Vdc, V_{CC} = +15 Vdc) (V_{IL} = 0.8 Vdc, V_{CC} = +15 Vdc)	5	I_{CC}	 — — — — — —	 +15 +4.5 +19 +5.5 — —	 +20 +6.0 +25 +7.0 +34 +12	mA
Negative Supply Current (R_L = ∞) (V_{IH} = 1.9 Vdc, V_{EE} = −9.0 Vdc) (V_{IL} = 0.8 Vdc, V_{EE} = −9.0 Vdc) (V_{IH} = 1.9 Vdc, V_{EE} = −12 Vdc) (V_{IL} = 0.8 Vdc, V_{EE} = −12 Vdc) (V_{IH} = 1.9 Vdc, V_{EE} = −15 Vdc) (V_{IL} = 0.8 Vdc, V_{EE} = −15 Vdc)	5	I_{EE}	 — — — — — —	 −13 — −18 — — —	 −17 −500 −23 −500 −34 −2.5	 mA µA mA µA mA mA
Power Consumption (V_{CC} = 9.0 Vdc, V_{EE} = −9.0 Vdc) (V_{CC} = 12 Vdc, V_{EE} = −12 Vdc)		P_C	 — —	 — —	 333 576	mW

SWITCHING CHARACTERISTICS (V_{CC} = +9.0 ±1% Vdc, V_{EE} = −9.0 ±1% Vdc, T_A = +25°C.)

Propagation Delay Time	(z_l = 3.0 k and 15 pF)	6	t_{PLH}	—	275	350	ns
Fall Time	(z_l = 3.0 k and 15 pF)	6	t_{THL}	—	45	75	ns
Propagation Delay Time	(z_l = 3.0 k and 15 pF)	6	t_{PHL}	—	110	175	ns
Rise Time	(z_l = 3.0 k and 15 pF)	6	t_{TLH}	—	55	100	ns

Note 1. Maximum Package Power Dissipation may be exceeded if all outputs are shorted simultaneously.

CHARACTERISTIC DEFINITIONS

FIGURE 1 – INPUT CURRENT

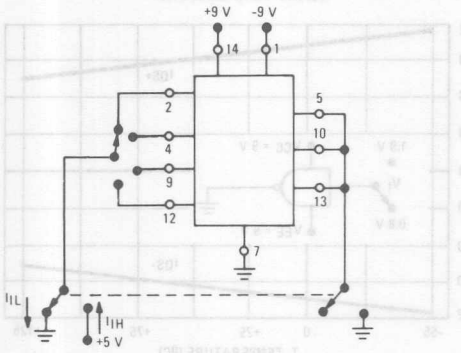


FIGURE 2 – OUTPUT VOLTAGE

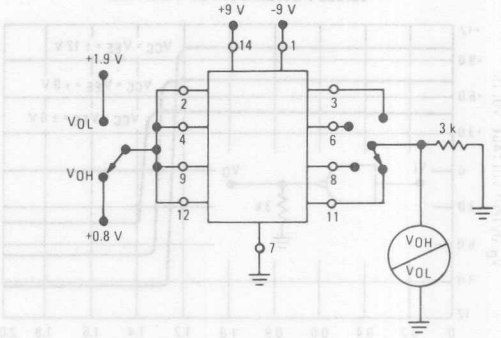


FIGURE 3 – OUTPUT SHORT-CIRCUIT CURRENT

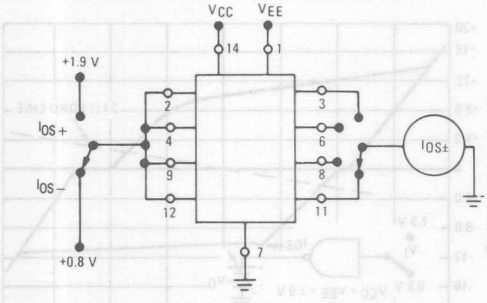


FIGURE 4 – OUTPUT RESISTANCE (POWER-OFF)

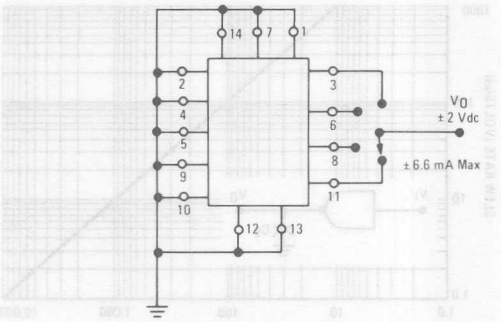


FIGURE 5 – POWER-SUPPLY CURRENTS

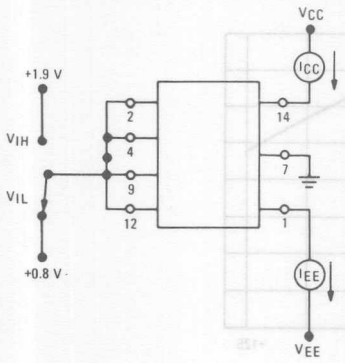
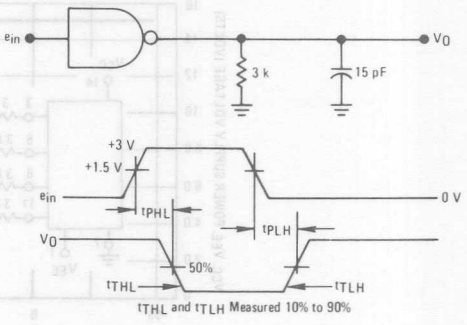


FIGURE 6 – SWITCHING RESPONSE



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TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted.)

FIGURE 7 — TRANSFER CHARACTERISTICS versus POWER-SUPPLY VOLTAGE

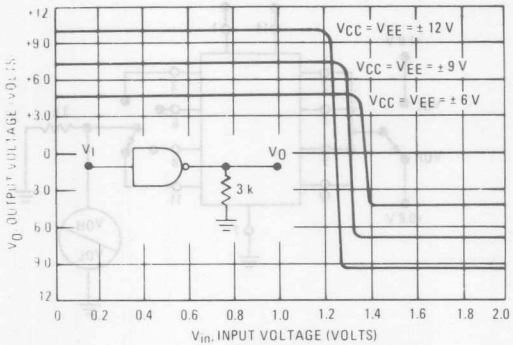


FIGURE 8 — SHORT-CIRCUIT OUTPUT CURRENT versus TEMPERATURE

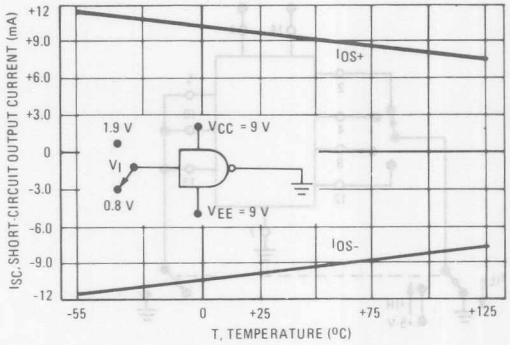


FIGURE 9 — OUTPUT SLEW RATE versus LOAD CAPACITANCE

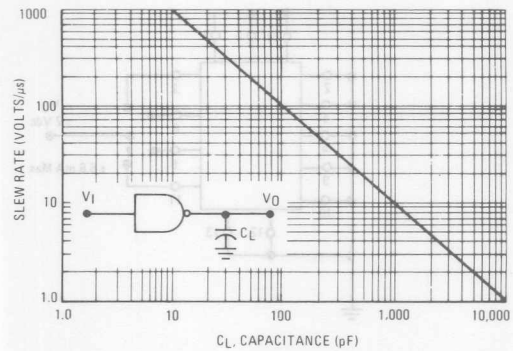


FIGURE 10 — OUTPUT VOLTAGE AND CURRENT-LIMITING CHARACTERISTICS

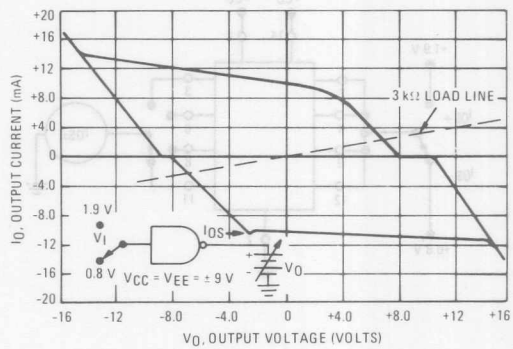
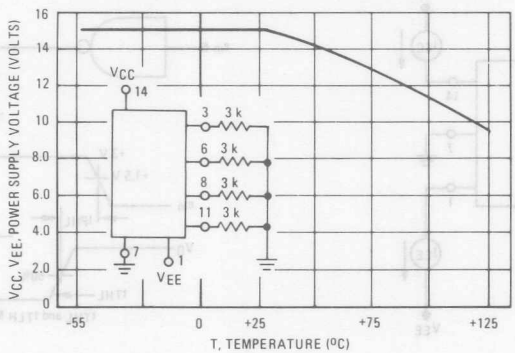


FIGURE 11 — MAXIMUM OPERATING TEMPERATURE versus POWER-SUPPLY VOLTAGE



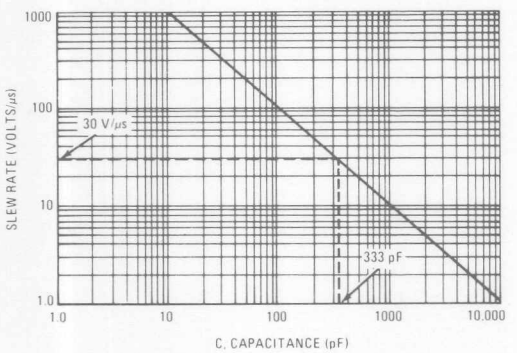
APPLICATIONS INFORMATION

The Electronic Industries Association EIA-232C specification detail the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the EIA-232C defined levels. The EIA-232C requirements as applied to drivers are discussed herein.

The required driver voltages are defined as between 5 and 15-volts in magnitude and are positive for a Logic "0" and negative for a Logic "1." These voltages are so defined when the drivers are terminated with a 3000 to 7000-ohm resistor. The MC1488 meets this voltage requirement by converting a DTL/TTL logic level into EIA-232C levels with one stage of inversion.

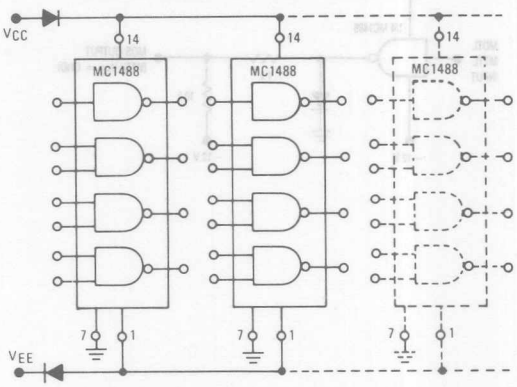
The EIA-232C specification further requires that during transitions, the driver output slew rate must not exceed 30 volts per microsecond. The inherent slew rate of the MC1488 is much too fast for this requirement. The current limited output of the device can be used to control this slew rate by connecting a capacitor to each driver output. The required capacitor can be easily determined by using the relationship $C = I_{OS} \times \Delta T/\Delta V$ from which Figure 12 is derived. Accordingly, a 330 pF capacitor on each output will guarantee a worst case slew rate of 30 volts per microsecond.

FIGURE 12 – SLEW RATE versus CAPACITANCE FOR I_{SC} = 10 mA



The interface driver is also required to withstand an accidental short to any other conductor in an interconnecting cable. The worst possible signal on any conductor would be another driver using a plus or minus 15 volt, 500 mA source. The MC1488 is designed to indefinitely withstand such a short to all four outputs in a package as long as the power-supply voltages are greater than 9.0 volts (i.e., $V_{CC} \geq 9.0$ V; $V_{EE} \leq -9.0$ V). In some power-supply designs, a loss of system power causes a low impedance on the power-supply outputs. When this occurs, a low impedance to ground would exist at the power inputs to the MC1488 effectively shorting the 300 ohm output resistors to ground. If all four outputs were then shorted to plus or minus 15 volts, the power dissipation in these resistors would be excessive. Therefore, if the system is designed to permit low impedances to ground at the power-supplies of the drivers, a diode should be placed in each power-supply lead to prevent overheating in this fault condition. These two diodes, as shown in Figure 13, could be used to decouple all the driver packages in a system. (These same diodes will allow the MC1488 to withstand momentary shorts to the ±25 volt limits specified in the earlier Standard EIA-232B.) The addition of the diodes also permits the MC1488 to withstand faults with power-supplies of less than the 9.0 volts stated above.

FIGURE 13 – POWER-SUPPLY PROTECTION TO MEET POWER-OFF FAULT CONDITIONS



The maximum short-circuit current allowable under fault conditions is more than guaranteed by the previously mentioned 10 mA output current limiting.

Other Applications

The MC1488 is an extremely versatile line driver with a myriad of possible applications. Several features of the drivers enhance this versatility:

1. Output Current Limiting — this enables the circuit designer to define the output voltage levels independent of power-supplies and can be accomplished by diode clamping of the output pins. Figure 14 shows the MC1488 used as a DTL to MOS translator where the high level voltage output is clamped one diode above ground. The resistor divider shown is used to reduce the output voltage below the 300 mV above ground MOS input level limit.

2. Power Supply Range — as can be seen from the schematic drawing of the drivers, the positive and negative driving elements of the device are essentially independent and do not require matching power-supplies. In fact, the positive supply can vary from a minimum seven volts (required for driving the negative pulldown section) to the maximum specified 15 volts. The negative supply can vary from approximately −2.5 volts to the minimum specified −15 volts. The MC1488 will drive the output to within 2 volts of the positive or negative supplies as long as the current output limits are not exceeded. The combination of the current-limiting and supply-voltage features allow a wide combination of possible outputs within the same quad package. Thus if only a portion of the four drivers are used for driving EIA-232C lines, the remainder could be used for DTL to MOS or even DTL to DTL translation. Figure 15 shows one such combination.

7

FIGURE 14 – MDTL/MTTL-TO-MOS TRANSLATOR

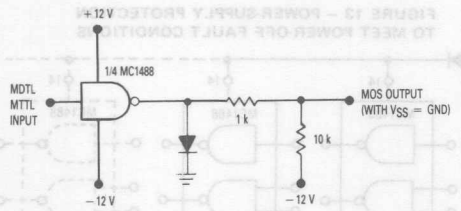
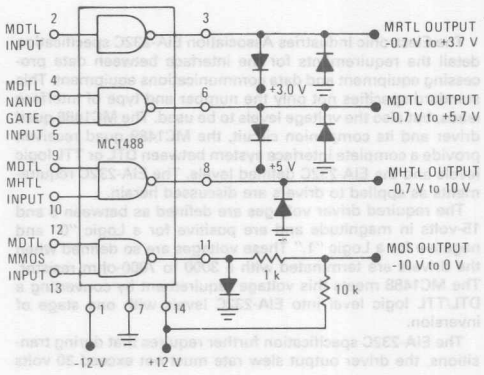


FIGURE 15 – LOGIC TRANSLATOR APPLICATIONS



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MOTOROLA

MC1489
MC1489A

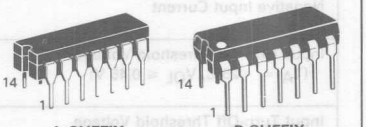
QUAD LINE RECEIVERS

The MC1489 monolithic quad line receivers are designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. EIA-232C.

- Input Resistance – 3.0 k to 7.0 kilohms
- Input Signal Range – ± 30 Volts
- Input Threshold Hysteresis Built In
- Response Control
  - a) Logic Threshold Shifting
  - b) Input Noise Filtering

QUAD MDTL LINE RECEIVERS EIA-232C

SILICON MONOLITHIC INTEGRATED CIRCUIT

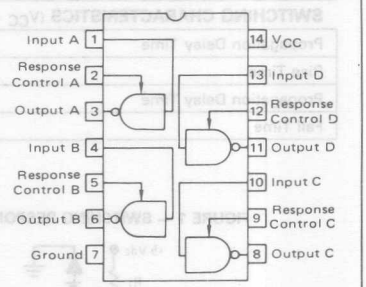


L SUFFIX
CERAMIC PACKAGE
CASE 632-08

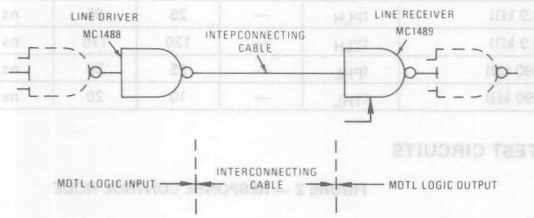
P SUFFIX
PLASTIC PACKAGE
CASE 646-06

D SUFFIX
PLASTIC PACKAGE
CASE 751A-02
SO-14

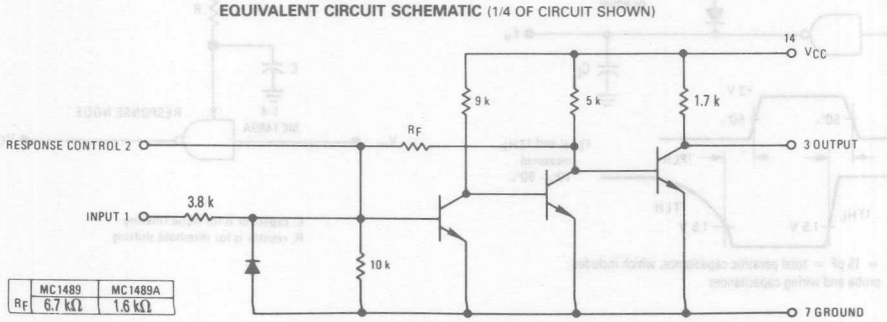




TYPICAL APPLICATION



EQUIVALENT CIRCUIT SCHEMATIC (1/4 OF CIRCUIT SHOWN)



	MC1489	MC1489A
R_F	6.7 kΩ	1.6 kΩ

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MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	10	Vdc
Input Voltage Range	V_{IR}	±30	Vdc
Output Load Current	I_L	20	mA
Power Dissipation (Package Limitation, Ceramic and Plastic Dual In-Line Package) Derate above T_A = +25°C	P_D $1/\theta JA$	1000 6.7	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	−65 to +175	°C

ELECTRICAL CHARACTERISTICS (Response control pin is open.) (V_{CC} = +5.0 Vdc ±10%, T_A = 0 to +75°C unless otherwise noted)

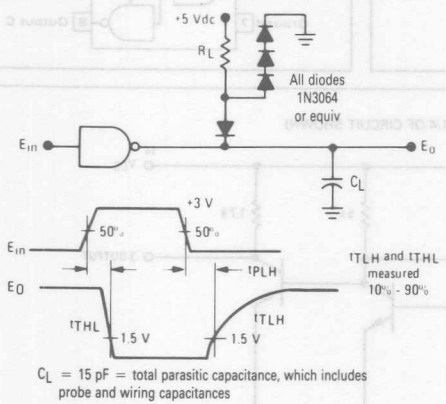
Characteristics		Symbol	Min	Typ	Max	Unit
Positive Input Current	(V_{IH} = +25 Vdc) (V_{IH} = +3.0 Vdc)	I_{IH}	3.6 0.43	— —	8.3 —	mA
Negative Input Current	(V_{IL} = −25 Vdc) (V_{IL} = −3.0 Vdc)	I_{IL}	−3.6 −0.43	— —	−8.3 —	mA
Input Turn-On Threshold Voltage (T_A = +25°C, V_{OL} ≤ 0.45 V)	MC1489 MC1489A	V_{IH}	1.0 1.75	— 1.95	1.5 2.25	Vdc
Input Turn-Off Threshold Voltage (T_A = +25°C, V_{OH} ≥ 2.5 V, I_L = −0.5 mA)	MC1489 MC1489A	V_{IL}	0.75 0.75	— 0.8	1.25 1.25	Vdc
Output Voltage High	(V_{IH} = 0.75 V, I_L = −0.5 mA) (Input Open Circuit, I_L = −0.5 mA)	V_{OH}	2.5 2.5	4.0 4.0	5.0 5.0	Vdc
Output Voltage Low	(V_{IL} = 3.0 V, I_L = 10 mA)	V_{OL}	—	0.2	0.45	Vdc
Output Short-Circuit Current		I_{OS}	—	−3.0	−4.0	mA
Power Supply Current (All Gates "on," I_{out} = 0 mA, V_{IH} = +5.0 Vdc)		I_{CC}	—	16	26	mA
Power Consumption	(V_{IH} = +5.0 Vdc)	P_C	—	80	130	mW

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 Vdc ±1%, T_A = +25°C, See Figure 1.)

Propagation Delay Time	(R_L = 3.9 kΩ)	t_{PLH}	—	25	85	ns
Rise Time	(R_L = 3.9 kΩ)	t_{TLH}	—	120	175	ns
Propagation Delay Time	(R_L = 390 kΩ)	t_{PHL}	—	25	50	ns
Fall Time	(R_L = 390 kΩ)	t_{THL}	—	10	20	ns

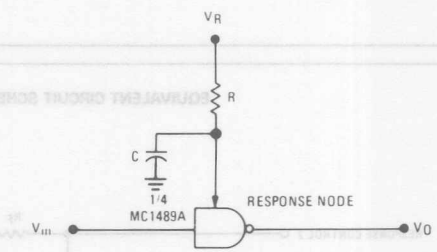
TEST CIRCUITS

FIGURE 1 — SWITCHING RESPONSE



C_L = 15 pF = total parasitic capacitance, which includes probe and wiring capacitances

FIGURE 2 — RESPONSE CONTROL NODE



C, capacitor is for noise filtering.
R, resistor is for threshold shifting.

(V_{CC} = 5.0 Vdc, T_A = +25°C unless otherwise noted)

FIGURE 3 — INPUT CURRENT

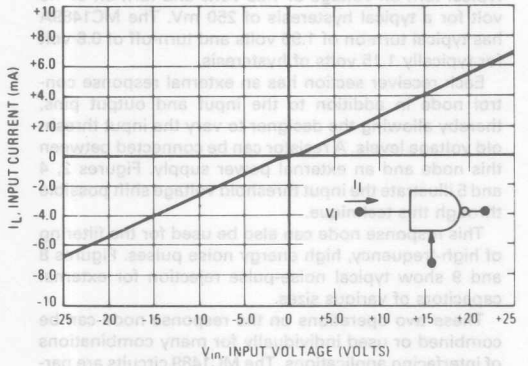


FIGURE 4 — MC1489 INPUT THRESHOLD VOLTAGE ADJUSTMENT

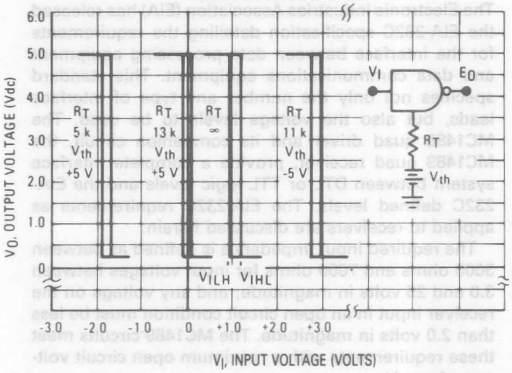


FIGURE 5 — MC1489A INPUT THRESHOLD VOLTAGE ADJUSTMENT

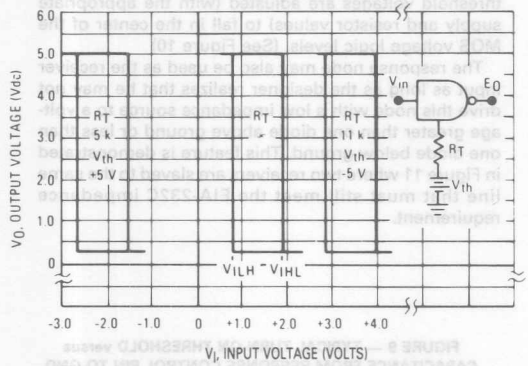


FIGURE 6 — INPUT THRESHOLD VOLTAGE versus TEMPERATURE

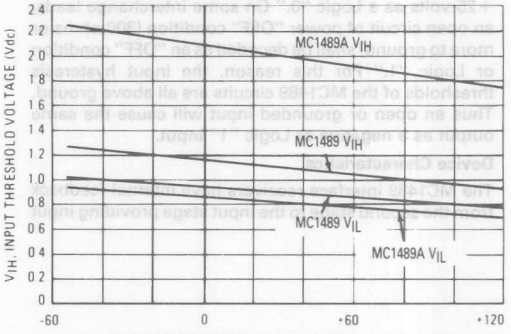
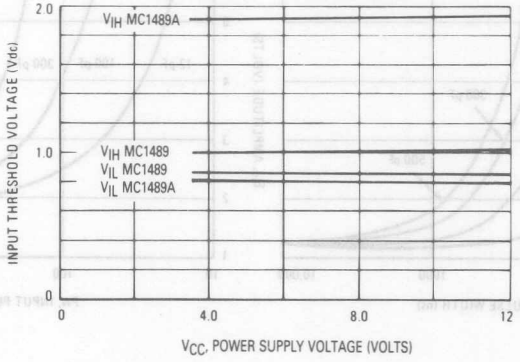


FIGURE 7 — INPUT THRESHOLD versus POWER-SUPPLY VOLTAGE



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APPLICATIONS INFORMATION

General Information

The Electronic Industries Association (EIA) has released the EIA-232C specification detailing the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the EIA-232C defined levels. The EIA-232C requirements as applied to receivers are discussed herein.

The required input impedance is defined as between 3000 ohms and 7000 ohms for input voltages between 3.0 and 25 volts in magnitude; and any voltage on the receiver input in an open circuit condition must be less than 2.0 volts in magnitude. The MC1489 circuits meet these requirements with a maximum open circuit voltage of one V_{BE}.

The receiver shall detect a voltage between −3.0 and −25 volts as a Logic "1" and inputs between +3.0 and +25 volts as a Logic "0." On some interchange leads, an open circuit of power "OFF" condition (300 ohms or more to ground) shall be decoded as an "OFF" condition or Logic "1." For this reason, the input hysteresis thresholds of the MC1489 circuits are all above ground. Thus an open or grounded input will cause the same output as a negative or Logic "1" input.

Device Characteristics

The MC1489 interface receivers have internal feedback from the second stage to the input stage providing input hysteresis for noise rejection. The MC1489 input has typical turn-on voltage of 1.25 volts and turn-off of 1.0 volt for a typical hysteresis of 250 mV. The MC1489A has typical turn-on of 1.95 volts and turn-off of 0.8 volt for typically 1.15 volts of hysteresis.

Each receiver section has an external response control node in addition to the input and output pins, thereby allowing the designer to vary the input threshold voltage levels. A resistor can be connected between this node and an external power supply. Figures 2, 4 and 5 illustrate the input threshold voltage shift possible through this technique.

This response node can also be used for the filtering of high-frequency, high energy noise pulses. Figures 8 and 9 show typical noise-pulse rejection for external capacitors of various sizes.

These two operations on the response node can be combined or used individually for many combinations of interfacing applications. The MC1489 circuits are particularly useful for interfacing between MOS circuits and MDTL/MTTL logic systems. In this application, the input threshold voltages are adjusted (with the appropriate supply and resistor values) to fall in the center of the MOS voltage logic levels. (See Figure 10)

The response node may also be used as the receiver input as long as the designer realizes that he may not drive this node with a low impedance source to a voltage greater than one diode above ground or less than one diode below ground. This feature is demonstrated in Figure 11 where two receivers are slaved to the same line that must still meet the EIA-232C impedance requirement.

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FIGURE 8 — TYPICAL TURN-ON THRESHOLD versus CAPACITANCE FROM RESPONSE CONTROL PIN TO GND

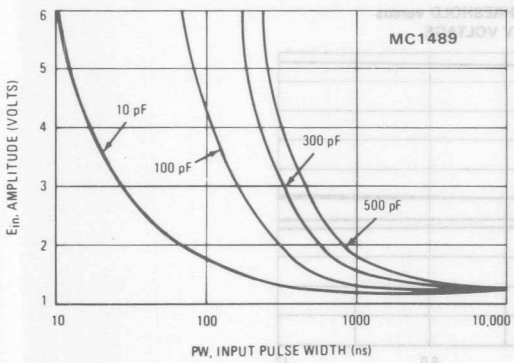
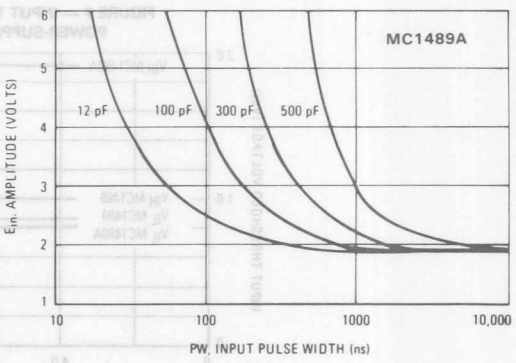


FIGURE 9 — TYPICAL TURN-ON THRESHOLD versus CAPACITANCE FROM RESPONSE CONTROL PIN TO GND



APPLICATIONS INFORMATION (continued)

FIGURE 10 — TYPICAL TRANSLATOR APPLICATION — MOS TO DTL OR TTL

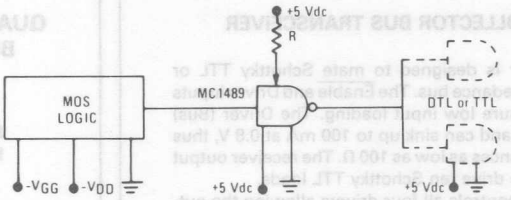
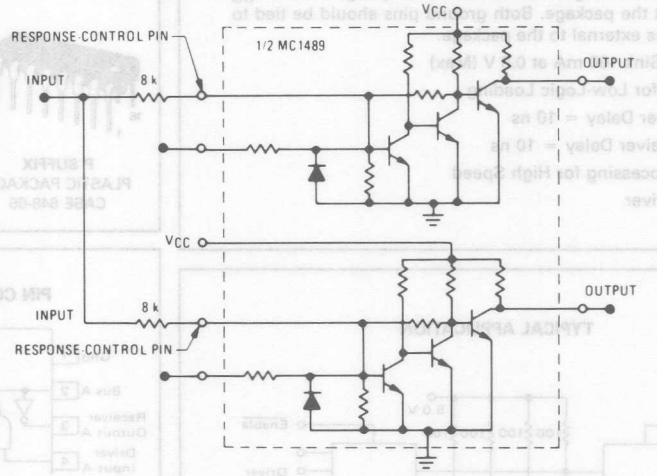


FIGURE 11 — TYPICAL PARALLELING OF TWO MC1489,A RECEIVERS TO MEET EIA-232C



7

QUAD OPEN-COLLECTOR BUS TRANSCEIVER

This quad transceiver is designed to mate Schottky TTL or NMOS logic to a low impedance bus. The $\overline{\text{Enable}}$ and Driver inputs are PNP buffered to ensure low input loading. The Driver (Bus) output is open-collector and can sink up to 100 mA at 0.8 V, thus the bus can drive impedances as low as 100 Ω. The receiver output is active pull-up and can drive ten Schottky TTL loads.

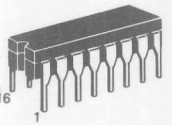
An active-low $\overline{\text{Enable}}$ controls all four drivers allowing the outputs of different device drivers to be connected together for party-line operation. The line can be terminated at both ends and still give considerable noise margin at the receiver. Typical receiver threshold is 2.0 V.

Advanced Schottky processing is utilized to assure fast propagation delay times. Two ground pins are provided to improve ground current handling and allow close decoupling between V_{CC} and ground at the package. Both ground pins should be tied to the ground bus external to the package.

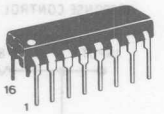
- Driver Can Sink 100 mA at 0.8 V (Max)
- PNP Inputs for Low-Logic Loading
- Typical Driver Delay = 10 ns
- Typical Receiver Delay = 10 ns
- Schottky Processing for High Speed
- Inverting Driver

QUAD OPEN-COLLECTOR BUS TRANSCEIVER

SCHOTTKY SILICON MONOLITHIC INTEGRATED CIRCUIT

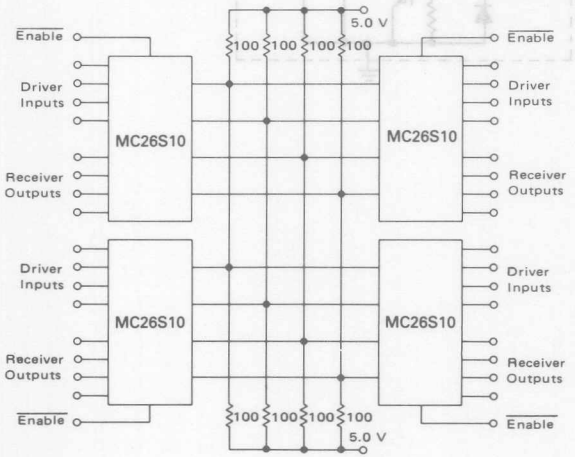


L SUFFIX
CERAMIC PACKAGE
CASE 620-10

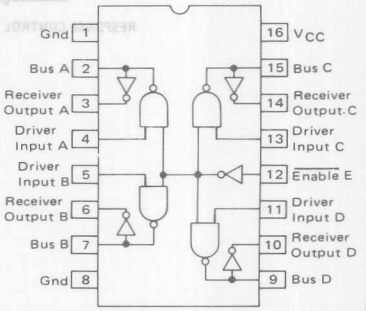


P SUFFIX
PLASTIC PACKAGE
CASE 648-06

TYPICAL APPLICATION



PIN CONNECTIONS



TRUTH TABLE

$\overline{\text{Enable}}$	Driver Input	Bus	Receiver Output
L	L	H	L
L	H	L	H
H	X	Y	Y

L = Low Logic State
H = High Logic State
X = Irrelevant
Y = Assumes condition controlled by other elements on the bus

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	-0.5 to +7.0	Vdc
Input Voltage	V_I	-0.5 to +5.5	Vdc
Input Current	I_I	-3.0 to +5.0	mA
Output Voltage — High Impedance State	$V_{O(Hi-z)}$	-0.5 to V_{CC}	V
Output Current—Bus	$I_{O(B)}$	200	mA
Output Current—Receiver	$I_{O(R)}$	30	mA
Operating Ambient Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	-65 to +150	°C
Junction Temperature Ceramic Package Plastic Package	T_J	 175 150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted V_{CC} = 4.75 to 5.25 V and T_A = 0 to +70°C. Typical values measured at V_{CC} = 5.0 V and T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage — Low Logic State (Driver and $\overline{\text{Enable}}$ Inputs)	V_{IL}	–	–	0.8	V
Input Voltage — High Logic State (Driver and $\overline{\text{Enable}}$ Inputs)	V_{IH}	2.0	–	–	V
Input Clamp Voltage (Driver and Enable Inputs) (I_{IK} = -18 mA)	V_{IK}	–	–	-1.2	V
Input Current — Low Logic State (V_{IL} = 0.4 V) ($\overline{\text{Enable}}$ Input) (Driver Inputs)	I_{IL}	 – –	 – –	 -0.36 -0.54	mA
Input Current — High Logic State (V_{IH} = 2.7 V) ($\overline{\text{Enable}}$ Input) (Driver Inputs)	I_{IH}	 – –	 – –	 20 30	μA
Input Current — Maximum Voltage (V_{IH1} = 5.5 V) ($\overline{\text{Enable}}$ or Driver Inputs)	I_{IH1}	–	–	100	μA
Driver Output Voltage — Low Logic State (I_{OL} = 40 mA) (I_{OL} = 70 mA) (I_{OL} = 100 mA)	$V_{OL(D)}$	 – – –	 0.33 0.42 0.51	 0.5 0.7 0.8	V
Driver (Bus) Leakage Current (V_{OH} = 4.5 V) (V_{OL} = 0.8 V)	$I_{O(D)}$	 – –	 – –	 100 -50	μA
Driver (Bus) Leakage Current (V_{CC} = 0 V, V_{OH} = 4.5 V)	$I_{O1(D)}$	–	–	100	μA
Receiver Input High Threshold ($V_{IH(\overline{E})}$ = 2.4 V)	$V_{TH(R)}$	2.25	2.0	–	V
Receiver Input Low Threshold ($V_{IH(\overline{E})}$ = 2.4 V)	$V_{TL(R)}$	–	2.0	1.75	V
Receiver Output Voltage — Low Logic State (I_{OL} = 20 mA)	$V_{OL(R)}$	–	–	0.5	V
Receiver Output Voltage — High Logic State (I_{OH} = -1.0 mA)	$V_{OH(R)}$	2.7	3.4	–	V
Receiver Output Short-Circuit Current (Note 1)	$I_{OS(R)}$	-18	–	-60	mA
Power Supply Current — Output Low State ($V_{IL(\overline{E})}$ = 0 V)	I_{CC}	–	45	70	mA

NOTE 1: One output shorted at a time. Duration not to exceed 1.0 second.

7

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time Driver Input to Output	$t_{PLH(D)}$	—	10	15	ns
	$t_{PHL(D)}$	—	10	15	
Propagation Delay Time $\overline{\text{Enable}}$ Input to Output	$t_{PLH(\bar{E})}$	—	14	18	ns
	$t_{PHL(\bar{E})}$	—	13	18	
Propagation Delay Time Bus to Receiver Output	$t_{PLH(R)}$	—	10	15	ns
	$t_{PHL(R)}$	—	10	15	
Rise and Fall Time of Driver Output	$t_{TLH(D)}$	4.0	10	—	ns
	$t_{THL(D)}$	2.0	4.0	—	

SWITCHING WAVEFORMS AND CIRCUITS

FIGURE 1 — DATA INPUT TO BUS OUTPUT (DRIVER)

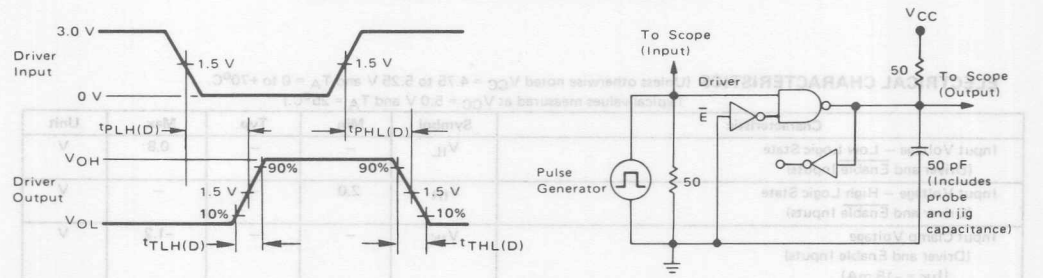


FIGURE 2 — ENABLE INPUT TO BUS OUTPUT (DRIVER)

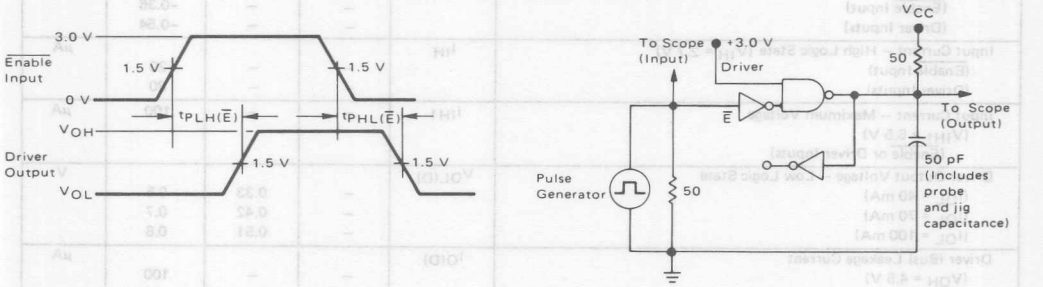
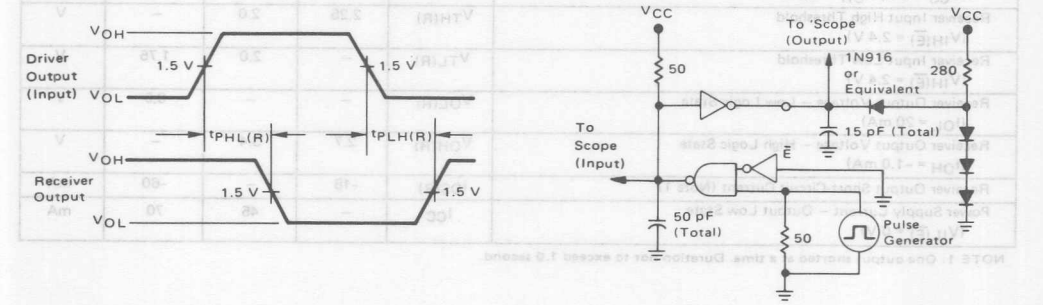


FIGURE 3 — BUS INPUT TO RECEIVER OUTPUT



7

MOTOROLA

MC3437

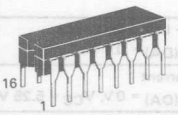
HEX BUS RECEIVER WITH INPUT HYSTERESIS

These high-speed bus receivers are useful in bus organized data transmission systems employing terminated 120 Ω lines. The receivers feature input hysteresis to obtain improved noise immunity. The receivers low input current requirement allows up to 27 driver/receiver pairs to share a common bus. A pair of Disable Inputs are provided. These Disable Inputs along with the receiver outputs are MTTL compatible.

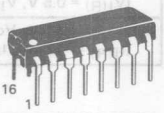
- Built in receiver hysteresis
- Receiver input threshold is not affected by temperature
- Propagation delay time – 20 ns (Typ)
- Direct Replacement for DM8837

HEX BUS RECEIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT



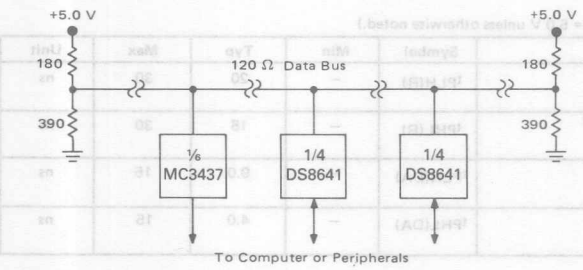
L SUFFIX
CERAMIC PACKAGE
CASE 620-10



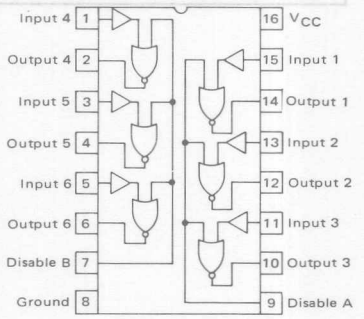
P SUFFIX
PLASTIC PACKAGE
CASE 648-06

7

FIGURE 1 – TYPICAL APPLICATION



PIN CONNECTIONS



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	7.0	Vdc
Input Voltage	V_I	5.5	Vdc
Power Dissipation Derate above 25°C	P_D	625 3.85	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

Input	Disable	Output
O	L	H
O	H	L
I	L	L
I	H	L

O = < 1.05 V
I = > 2.5 V
H = High Logic State
L = Low Logic State

Characteristic	Symbol	Min	Typ	Max	Unit
Receiver Input Threshold Voltage — High Logic State ($V_{IL(DA)}$ = 0.8 V, I_{OL} = 16 mA, $V_{OL} \leq$ 0.4 V)	$V_{ILH(R)}$	1.80	2.25	2.50	V
Receiver Input Threshold Voltage — Low Logic State ($V_{IL(DA)}$ = 0.8 V, I_{OH} = -400 μA, $V_{OH} \geq$ 2.4 V)	$V_{IHL(R)}$	1.05	1.30	1.55	V
Receiver Input Current ($V_{I(R)}$ = 4.0 V, V_{CC} = 5.25 V) ($V_{I(R)}$ = 4.0 V, V_{CC} = 0 V)	$I_{I(R)}$	 – –	 15 1.0	 50 50	μA
Disable Input Voltage — High Logic State ($V_{I(R)}$ = 0.5 V, $V_{OL} \leq$ 0.4 V, I_{OL} = 16 mA)	$V_{IH(DA)}$	2.0	–	–	V
Disable Input Voltage — Low Logic State ($V_{I(R)}$ = 0.5 V, $V_{OH} \geq$ 2.4 V, I_{OH} = -400 μA)	$V_{IL(DA)}$	–	–	0.8	V
Output Voltage — High Logic State ($V_{I(R)}$ = 0.5 V, $V_{IL(DA)}$ = 0.8 V, I_{OH} = -400 μA)	V_{OH}	2.4	–	–	V
Output Voltage — Low Logic State ($V_{I(R)}$ = 4.0 V, $V_{IL(DA)}$ = 0.8 V, I_{OL} = 16 mA)	V_{OL}	–	0.25	0.4	V
Disable Input Current — High Logic State ($V_{IH(DA)}$ = 2.4 V) ($V_{IH(DA)}$ = 5.5 V)	$I_{IH(DA)}$	 – –	 – –	 80 2.0	 μA mA
Disable Input Current — Low Logic State ($V_{I(R)}$ = 4.0 V, $V_{IL(DA)}$ = 0.4 V)	$I_{IL(DA)}$	–	–	-3.2	mA
Output Short Circuit Current ($V_{I(R)}$ = 0.5 V, $V_{IL(DA)}$ = 0 V, V_{CC} = 5.25 V)	I_{OS}	-18	–	-55	mA
Power Supply Current ($V_{I(R)}$ = 0.5 V, $V_{IL(DA)}$ = 0 V)	I_{CC}	–	45	65	mA
Input Clamp Diode Voltage ($I_{I(R)}$ = -12 mA, $I_{I(DA)}$ = -12 mA,	V_I	–	-1.0	-1.5	V

SWITCHING CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time from Receiver Input to High Logic State Output	$t_{PLH(R)}$	–	20	30	ns
Propagation Delay Time from Receiver Input to Low Logic State Output	$t_{PHL(R)}$	–	18	30	ns
Propagation Delay Time from Disable Input to High Logic State Output	$t_{PLH(DA)}$	–	9.0	15	ns
Propagation Delay Time from Disable Input to Low Logic State Output	$t_{PHL(DA)}$	–	4.0	15	ns

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS

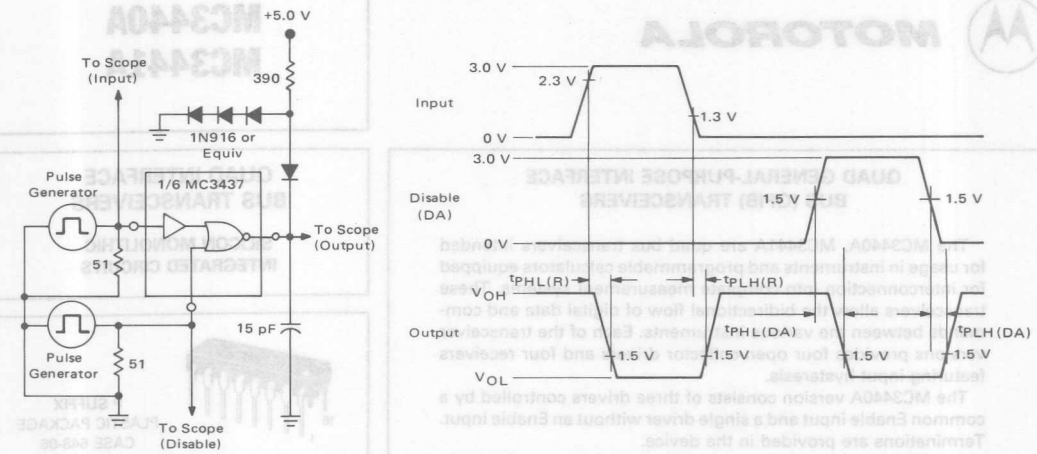
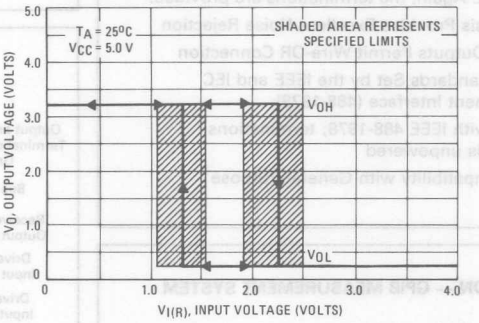
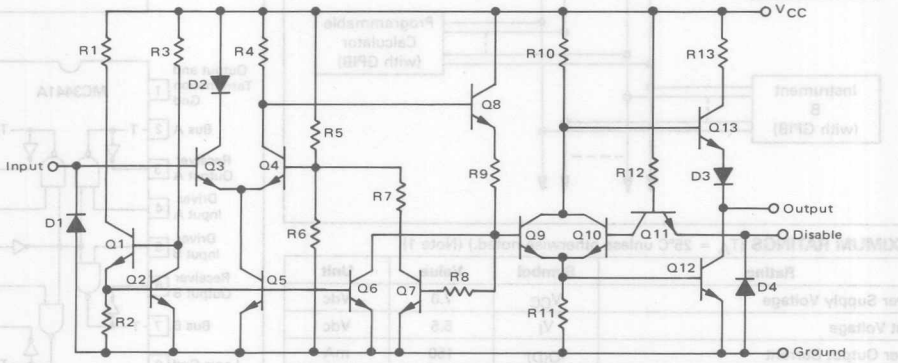


FIGURE 3 – TYPICAL HYSTERESIS



REPRESENTATIVE CIRCUIT SCHEMATIC
(1/6 Shown)



7

MOTOROLA

MC3440A
MC3441A

QUAD GENERAL-PURPOSE INTERFACE BUS (GPIB) TRANSCEIVERS

The MC3440A, MC3441A are quad bus transceivers intended for usage in instruments and programmable calculators equipped for interconnection into complete measurement systems. These transceivers allow the bidirectional flow of digital data and commands between the various instruments. Each of the transceiver versions provides four open-collector drivers and four receivers featuring input hysteresis.

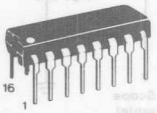
The MC3440A version consists of three drivers controlled by a common Enable input and a single driver without an Enable input. Terminations are provided in the device.

The MC3441A differs in that all four drivers are controlled by the common Enable input. Again, the terminations are provided.

- Receiver Input Hysteresis Provides Excellent Noise Rejection
- Open-Collector Driver Outputs Permit Wire-OR Connection
- Tailored to Meet the Standards Set by the IEEE and IEC Committees on Instrument Interface (488-1978)
- Terminations comply with IEEE 488-1978; terminations removed when device is unpowered
- Provides Electrical Compatibility with General-Purpose Interface Bus

QUAD INTERFACE BUS TRANSCEIVERS

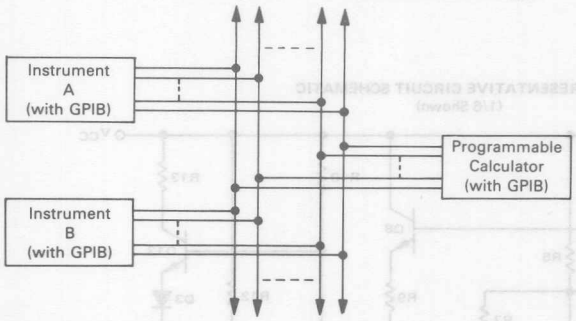
SILICON MONOLITHIC INTEGRATED CIRCUITS



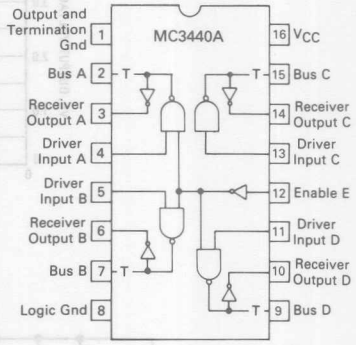
P SUFFIX
PLASTIC PACKAGE
CASE 648-06

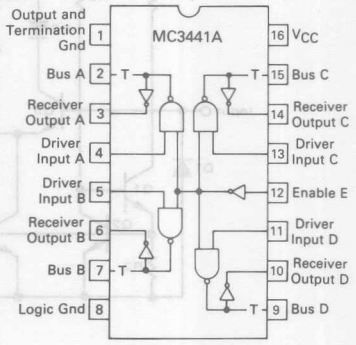
7

TYPICAL APPLICATION — GPIB MEASUREMENT SYSTEM



PIN CONNECTIONS





— T — = Bus Termination

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.) (Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Input Voltage	V_I	5.5	Vdc
Driver Output Current	$I_{O(D)}$	150	mA
Power Dissipation (Package Limitation) Derate above 25°C	P_D	830 6.7	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

Note 1: Devices should not be operated at these values. The "Electrical Characteristics" provide conditions for actual device operation.

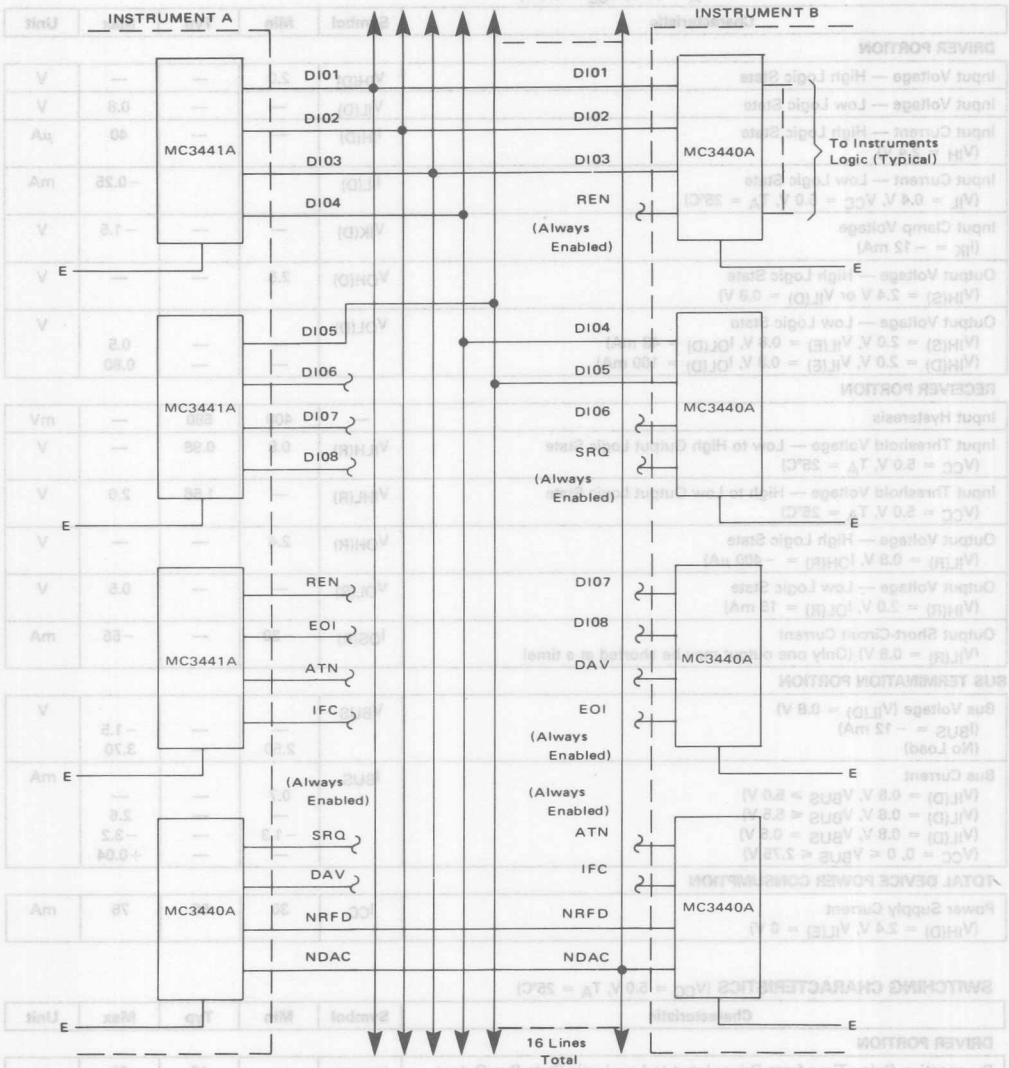
ELECTRICAL CHARACTERISTICS (Unless otherwise noted, 4.5 V ≤ V_{CC} ≤ 5.5 V and 0 ≤ T_A ≤ 70°C, typical values are at T_A = 25°C, V_{CC} = 5.0 V)

Characteristic	Symbol	Min	Typ	Max	Unit
DRIVER PORTION					
Input Voltage — High Logic State	$V_{IH(D)}$	2.0	—	—	V
Input Voltage — Low Logic State	$V_{IL(D)}$	—	—	0.8	V
Input Current — High Logic State (V_{IH} = 2.4 V)	$I_{IH(D)}$	—	—	40	μA
Input Current — Low Logic State (V_{IL} = 0.4 V, V_{CC} = 5.0 V, T_A = 25°C)	$I_{IL(D)}$			−0.25	mA
Input Clamp Voltage (I_{IK} = −12 mA)	$V_{IK(D)}$	—	—	−1.5	V
Output Voltage — High Logic State ($V_{IH(S)}$ = 2.4 V or $V_{IL(D)}$ = 0.8 V)	$V_{OH(D)}$	2.5	—	—	V
Output Voltage — Low Logic State ($V_{IH(S)}$ = 2.0 V, $V_{IL(E)}$ = 0.8 V, $I_{OL(D)}$ = 48 mA) ($V_{IH(D)}$ = 2.0 V, $V_{IL(E)}$ = 0.8 V, $I_{OL(D)}$ = 100 mA)	$V_{OL(D)}$	— —	— —	0.5 0.80	V
RECEIVER PORTION					
Input Hysteresis	—	400	580	—	mV
Input Threshold Voltage — Low to High Output Logic State (V_{CC} = 5.0 V, T_A = 25°C)	$V_{ILH(R)}$	0.8	0.98	—	V
Input Threshold Voltage — High to Low Output Logic State (V_{CC} = 5.0 V, T_A = 25°C)	$V_{IHL(R)}$	—	1.56	2.0	V
Output Voltage — High Logic State ($V_{IL(R)}$ = 0.8 V, $I_{OH(R)}$ = −400 μA)	$V_{OH(R)}$	2.4	—	—	V
Output Voltage — Low Logic State ($V_{IH(R)}$ = 2.0 V, $I_{OL(R)}$ = 16 mA)	$V_{OL(R)}$	—	—	0.5	V
Output Short-Circuit Current ($V_{IL(R)}$ = 0.8 V) (Only one output may be shorted at a time)	$I_{OS(R)}$	−20	—	−55	mA
BUS TERMINATION PORTION					
Bus Voltage ($V_{IL(D)}$ = 0.8 V) (I_{BUS} = −12 mA) (No Load)	V_{BUS}	— 2.50	— —	−1.5 3.70	V
Bus Current ($V_{IL(D)}$ = 0.8 V, V_{BUS} ≥ 5.0 V) ($V_{IL(D)}$ = 0.8 V, V_{BUS} ≤ 5.5 V) ($V_{IL(D)}$ = 0.8 V, V_{BUS} = 0.5 V) (V_{CC} = 0, 0 ≤ V_{BUS} ≤ 2.75 V)	I_{BUS}	0.7 — −1.3 —	— — — —	— 2.5 −3.2 +0.04	mA
TOTAL DEVICE POWER CONSUMPTION					
Power Supply Current ($V_{IH(D)}$ = 2.4 V, $V_{IL(E)}$ = 0 V)	I_{CC}	30	56	75	mA

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
DRIVER PORTION					
Propagation Delay Time from Driver Input to Low Logic State Bus Output	$t_{PHL(D)}$	—	13	30	ns
Propagation Delay Time from Driver Input to High Logic State Bus Output	$t_{PLH(D)}$	—	17	30	ns
Propagation Delay Time from Enable Input to Low Logic State Bus Output	$t_{PHL(E)}$	—	25	40	ns
Propagation Delay Time from Enable Input to High Logic State Bus Output	$t_{PLH(E)}$	—	25	40	ns
RECEIVER PORTION					
Propagation Delay Time from Bus Input to High Logic State Receiver Output	$t_{PLH(R)}$	—	15	30	ns
Propagation Delay Time from Bus Input to Low Logic State Receiver Output	$t_{PHL(R)}$	—	15	30	ns

7



GPIB SIGNALS:

8 Line Data Bus: DI01 – DI08

5 General Interrupt Transfer Control Bus:
- REN – Remote Enable
- SRQ – Service Request
- EOI – End or Identify
- ATN – Attention
- IFC – Interface Clear

3 Data Byte Transfer Control Bus
- DAV – Data Valid
- NRFD – Not Ready for Data
- NDAC – Not Data Accepted

16 Total Signal Lines

FIGURE 1 — TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM RECEIVER INPUT (BUS) TO OUTPUT

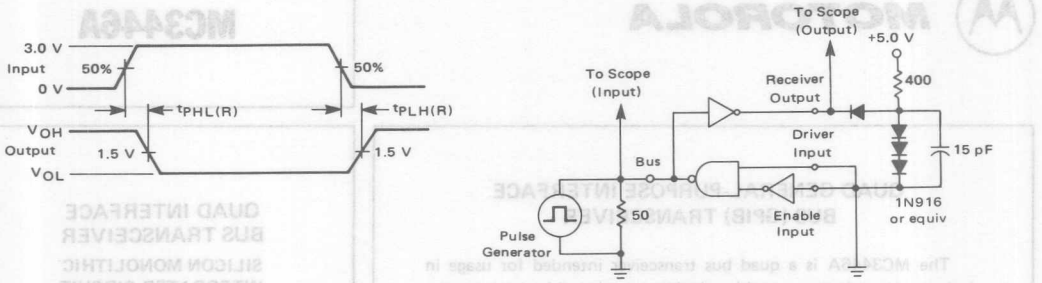


FIGURE 2 — TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM DRIVER AND COMMON ENABLE INPUTS TO OUTPUT (BUS)

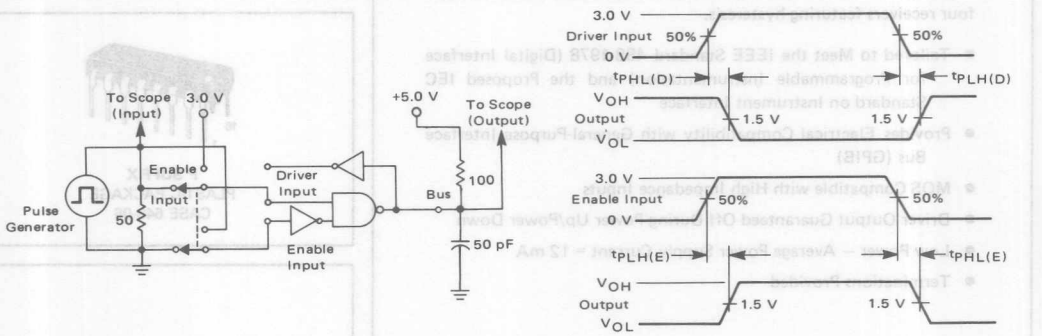
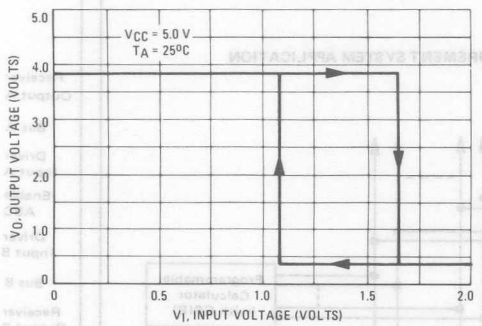


FIGURE 3 — TYPICAL RECEIVER HYSTERESIS CHARACTERISTICS



7

MOTOROLA

MC3446A

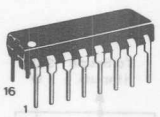
QUAD GENERAL-PURPOSE INTERFACE BUS (GPIB) TRANSCEIVER

The MC3446A is a quad bus transceiver intended for usage in instruments and programmable calculators equipped for interconnection into complete measurement systems. This transceiver allows the bidirectional flow of digital data and commands between the various instruments. The transceiver provides four open-collector drivers and four receivers featuring hysteresis.

- Tailored to Meet the IEEE Standard 488-1978 (Digital Interface for Programmable Instrumentation) and the Proposed IEC Standard on Instrument Interface
- Provides Electrical Compatibility with General-Purpose Interface Bus (GPIB)
- MOS Compatible with High Impedance Inputs
- Driver Output Guaranteed Off During Power Up/Power Down
- Low Power — Average Power Supply Current = 12 mA
- Terminations Provided

QUAD INTERFACE BUS TRANSCEIVER

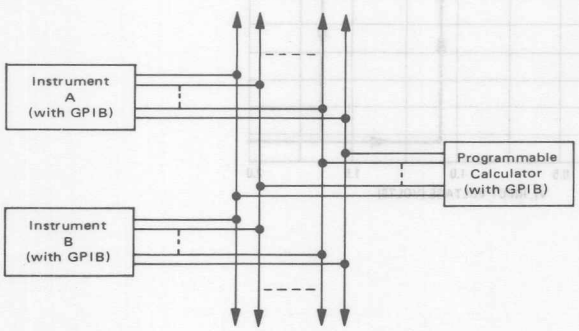
SILICON MONOLITHIC INTEGRATED CIRCUIT



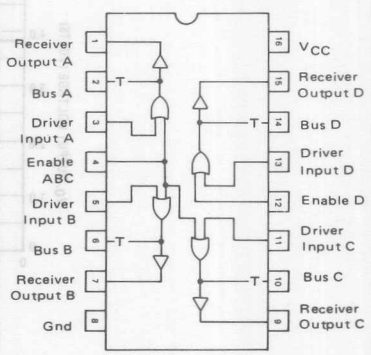
P SUFFIX
PLASTIC PACKAGE
CASE 648-06

7

TYPICAL MEASUREMENT SYSTEM APPLICATION



PIN CONNECTIONS



— T — = Bus Termination

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Input Voltage	V_I	5.5	Vdc
Driver Output Current	$I_{O(D)}$	150	mA
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, 4.5 V ≤ V_{CC} ≤ 5.5 V and 0 ≤ T_A ≤ 70°C, typical values are at T_A = 25°C, V_{CC} = 5.0 V)

Characteristic	Symbol	Min	Typ	Max	Unit
DRIVER PORTION					
Input Voltage – High Logic State	$V_{IH(D)}$	2.0	–	–	V
Input Voltage – Low Logic State	$V_{IL(D)}$	–	–	0.8	V
Input Current – High Logic State (V_{IH} = 2.4 V)	$I_{IH(D)}$	–	5.0	40	μA
Input Current – Low Logic State (V_{IL} = 0.4 V, V_{CC} = 5.0 V, T_A = 25°C)	$I_{IL(D)}$	–	-0.2	-0.25	mA
Input Clamp Voltage (I_{IK} = -12 mA)	$V_{IK(D)}$	–	–	-1.5	V
Output Voltage – High Logic State (1) ($V_{IH(S)}$ = 2.4 V or $V_{IH(D)}$ = 2.0 V)	$V_{OH(D)}$	2.5	3.3	3.7	V
Output Voltage – Low Logic State ($V_{IL(S)}$ = 0.8 V, $V_{IL(D)}$ = 0.8 V, $I_{OL(D)}$ = 48 mA)	$V_{OL(D)}$	–	–	0.5	
Input Breakdown Current ($V_{I(D)}$ = 5.5 V)	$I_{IB(D)}$	–	–	1.0	mA
RECEIVER PORTION					
Input Hysteresis	–	400	625	–	mV
Input Threshold Voltage – Low to High Output Logic State	$V_{ILH(R)}$	–	1.66	2.0	V
Input Threshold Voltage – High to Low Output Logic State	$V_{IHL(R)}$	0.8	1.03	–	V
Output Voltage – High Logic State ($V_{IH(R)}$ = 2.0 V, $I_{OH(R)}$ = -400 μA)	$V_{OH(R)}$	2.4	–	–	V
Output Voltage – Low Logic State ($V_{IL(R)}$ = 0.8 V, $I_{OL(R)}$ = 8.0 mA)	$V_{OL(R)}$	–	–	0.5	V
Output Short-Circuit Current ($V_{IH(R)}$ = 2.0 V) (Only one output may be shorted at a time)	$I_{OS(R)}$	4.0	–	14	mA
BUS LOAD CHARACTERISTICS					
Bus Voltage ($V_{IH(E)}$ = 2.4 V)	$V_{(BUS)}$	2.5	3.3	3.7	V
(I_{BUS} = -12 mA)		–	–	-1.5	
Bus Current ($V_{IH(O)}$ = 2.4 V, V_{BUS} ≥ 5.0 V)	$I_{(BUS)}$	0.7	–	–	mA
($V_{IH(D)}$ = 2.4 V, V_{BUS} = 0.5 V)		-1.3	–	-3.2	
(V_{BUS} ≤ 5.5 V)		–	–	2.5	
(V_{CC} = 0, 0 V ≤ V_{BUS} ≤ 2.75 V)		–	–	0.04	
TOTAL DEVICE POWER CONSUMPTION					
Power Supply Current	I_{CC}				mA
(All Drivers OFF)		–	12	19	
(All Drivers ON)		–	32	40	

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
DRIVER PORTION					
Propagation Delay Time from Driver Input to Low Logic State Bus Output	$t_{PHL(D)}$	–	–	50	ns
Propagation Delay Time from Driver Input to High Logic State Bus Output	$t_{PLH(D)}$	–	–	40	ns
Propagation Delay Time from Enable Input to Low Logic State Bus Output	$t_{PHL(E)}$	–	–	50	ns
Propagation Delay Time from Enable Input to High Logic State Bus Output	$t_{PLH(E)}$	–	–	50	ns
RECEIVER PORTION					
Propagation Delay Time from Bus Input to High Logic State Receiver Output	$t_{PLH(R)}$	–	–	50	ns
Propagation Delay Time from Bus Input to Low Logic State Receiver Output	$t_{PHL(R)}$	–	–	40	ns

FIGURE 1 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM RECEIVER INPUT (BUS) TO OUTPUT

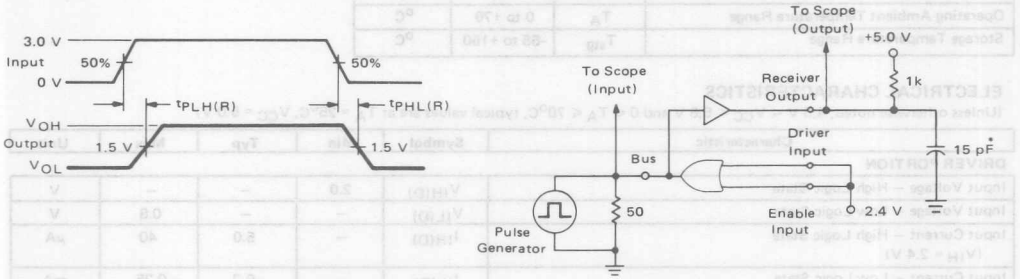
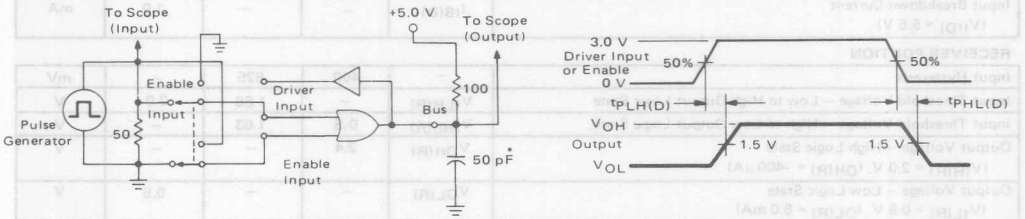


FIGURE 2 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM DRIVER AND COMMON ENABLE INPUTS TO OUTPUT (BUS)



* Includes Probe and Jig Capacitance

FIGURE 3 – TYPICAL RECEIVER HYSTERESIS CHARACTERISTICS

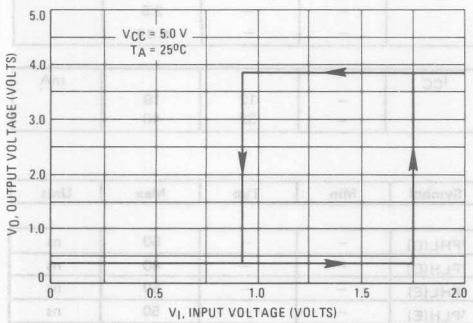
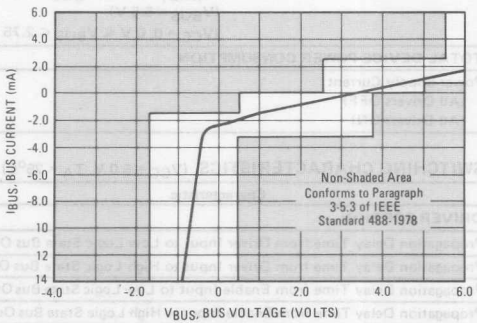


FIGURE 4 – TYPICAL BUS LOAD LINE



MOTOROLA

MC3447

BIDIRECTIONAL INSTRUMENTATION BUS (GPIB) TRANSCEIVER

This bidirectional bus transceiver is intended as the interface between TTL or MOS logic and the IEEE Standard Instrumentation Bus (488-1978, often referred to as GPIB). The required bus termination is internally provided.

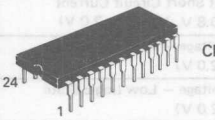
Low power consumption has been achieved by trading a minimum of speed for low current drain on non-critical channels. A fast channel is provided for critical ATN and EOI paths.

Each driver/receiver pair forms the complete interface between the bus and an instrument. Either the driver or the receiver of each channel is enabled by a Send/Receive input with the disabled output of the pair forced to a high impedance state. The receivers have input hysteresis to improve noise margin, and their input loading follows the bus standard specifications.

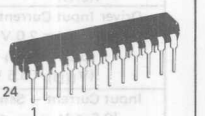
- Low Power — Average Power Supply Current = 30 mA Listening
  75 mA Talking
- Eight Driver/Receiver Pairs
- Three-State Outputs
- High Impedance Inputs
- Receiver Hysteresis — 600 mV (Typ)
- Fast Propagation Times — 15–20 ns (Typ)
- TTL Compatible Receiver Outputs
- Single +5 Volt Supply
- Open Collector Driver Output with Terminations
- Power Up/Power Down Protection (No Invalid Information Transmitted to Bus)
- No Bus Loading When Power is Removed From Device
- Required Termination Characteristics Provided

OCTAL BIDIRECTIONAL BUS TRANSCEIVER WITH TERMINATION NETWORKS

SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 623-05

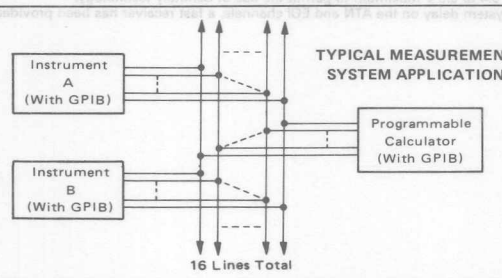


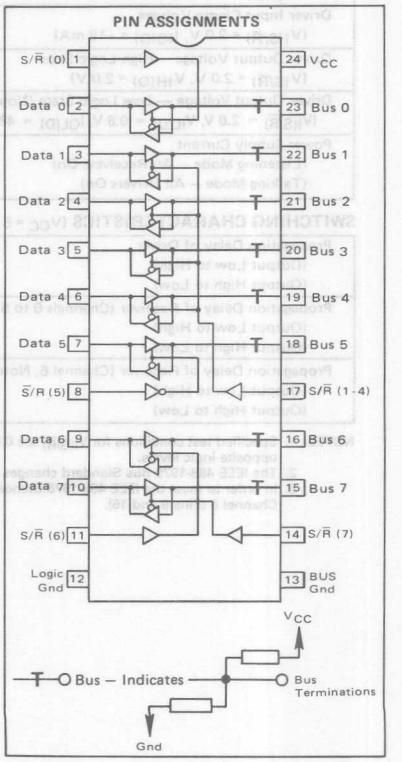
P3 SUFFIX
PLASTIC PACKAGE
CASE 724-03

7

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Input Voltage	V_I	5.5	Vdc
Driver Output Current	$I_{O(D)}$	150	mA
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C





ELECTRICAL CHARACTERISTICS

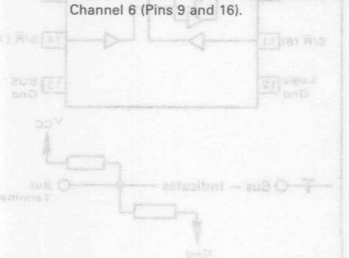
(Unless otherwise noted 4.50 V ≤ V_{CC} ≤ 5.50 V and 0 ≤ T_A ≤ 70°C; typical values are at T_A = 25°C, V_{CC} = 5.0 V)

Characteristic — Note 1		Symbol	Min	Typ	Max	Unit
Bus Voltage						V
(Bus Pin Open) ($V_{I(S/\overline{R})}$ = 0.8 V)		$V_{(Bus)}$	2.5	–	3.7	
($I_{(Bus)}$ = –12 mA)		$V_{IC(Bus)}$	–	–	–1.5	
Bus Current		$I_{(Bus)}$				mA
(5.0 V ≤ $V_{(Bus)}$ ≤ 5.5 V)			0.7	–	2.5	
($V_{(Bus)}$ = 0.5 V)			–1.3	–	–3.2	
(V_{CC} = 0 V, 0 V ≤ $V_{(Bus)}$ ≤ 2.75 V)			–	–	+0.04	
Receiver Input Hysteresis ($V_{I(S/\overline{R})}$ = 0.8 V)		–	400	600	–	mV
Receiver Input Threshold ($V_{I(S/\overline{R})}$ = 0.8 V)						V
	Low to High	$V_{ILH(R)}$	–	1.6	2.0	
	High to Low	$V_{IHL(R)}$	0.8	1.0	–	
Receiver Output Voltage — High Logic State ($V_{I(S/\overline{R})}$ = 0.8 V, $I_{OH(R)}$ = –200 μA, $V_{(Bus)}$ = 2.0 V)		$V_{OH(R)}$	2.4	–	–	V
Receiver Output Voltage — Low Logic State ($V_{I(S/\overline{R})}$ = 0.8 V, $I_{OL(R)}$ = 4.0 mA, $V_{(Bus)}$ = 0.8 V		$V_{OL(R)}$	–	–	0.5	V
Receiver Output Short Circuit Current ($V_{I(S/\overline{R})}$ = 0.8 V, $V_{(Bus)}$ = 2.0 V)		$I_{OS(R)}$	–4.0	–	–20	mA
Driver Input Voltage — High Logic State ($V_{I(S/\overline{R})}$ = 2.0 V)		$V_{IH(D)}$	2.0	–	–	V
Driver Input Voltage — Low Logic State ($V_{I(S/\overline{R})}$ = 2.0 V)		$V_{IL(D)}$	–	–	0.8	V
Driver Input Current — Data Pins						μA
($V_{I(S/\overline{R})}$ = 2.0 V)		$I_{I(D)}$	–100	–	40	
(0.5 ≤ $V_{I(D)}$ ≤ 2.7 V)		$I_{IB(D)}$	–	–	200	
($V_{I(D)}$ = 5.5 V)						
Input Current — Send/Receive						μA
(0.5 ≤ $V_{I(S/R)}$ ≤ 2.7 V)		$I_{I(S/\overline{R})}$	–250	–	20	
($V_{I(S/\overline{R})}$ = 5.5 V)		$I_{IB(S/\overline{R})}$	–	–	100	
Driver Input Clamp Voltage ($V_{I(S/\overline{R})}$ = 2.0 V, $I_{IC(D)}$ = –18 mA)		$V_{IC(D)}$	–	–	–1.5	V
Driver Output Voltage — High Logic State ($V_{IS/\overline{R})}$ = 2.0 V, $V_{IH(D)}$ = 2.0 V)		$V_{OH(D)}$	2.5	–	–	V
Driver Output Voltage — Low Logic State (Note 2) ($V_{I(S/\overline{R})}$ = 2.0 V, $V_{IL(D)}$ = 0.8 V, $I_{OL(D)}$ = 48 mA)		$V_{OL(D)}$	–	–	0.5	V
Power Supply Current						mA
(Listening Mode — All Receivers On)		I_{CCL}	–	30	45	
(Talking Mode — All Drivers On)		I_{CCH}	–	75	95	

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted)

Propagation Delay of Driver					ns
(Output Low to High)	$t_{PLH(D)}$	–	7.0	15	
(Output High to Low)	$t_{PHL(D)}$	–	16	30	
Propagation Delay of Receiver (Channels 0 to 5, 7)					ns
(Output Low to High)	$t_{PLH(R)}$	–	28	50	
(Output High to Low)	$t_{PHL(R)}$	–	15	30	
Propagation Delay of Receiver (Channel 6, Note 3)					ns
(Output Low to High)	$t_{PLH(R)}$	–	17	30	
(Output High to Low)	$t_{PHL(R)}$	–	12	22	

NOTES: 1. Specified test conditions for $V_{I(S/\overline{R})}$ are 0.8 V (Low) and 2.0 V (High). Where $V_{I(S/\overline{R})}$ is specified as a test condition, $V_{I(S/R)}$ uses the opposite logic levels.
2. The IEEE 488-1979 Bus Standard changes $V_{OL(D)}$ from 0.4 to 0.5 V maximum to permit the use of Schottky technology.
3. In order to meet the IEEE 488-1978 Standard for total system delay on the ATN and EOI channels, a fast receiver has been provided on Channel 6 (Pins 9 and 16).



SWITCHING CHARACTERISTICS (continued) (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time — Send/Receiver to Data					ns
Logic High to Third State	$t_{PHZ(R)}$	—	15	30	
Third State to Logic High	$t_{PZH(R)}$	—	15	30	
Logic Low to Third State	$t_{PLZ(R)}$	—	15	25	
Third State to Logic Low	$t_{PZL(R)}$	—	10	25	
Propagation Delay Time — Send/Receiver to Bus					ns
Logic Low to Third State	$t_{PLZ(D)}$	—	13	25	
Third State to Logic Low	$t_{PZL(D)}$	—	30	50	

PROPAGATION DELAY TEST CIRCUITS AND WAVEFORMS

FIGURE 1 — BUS INPUT TO DATA OUTPUT (RECEIVER)

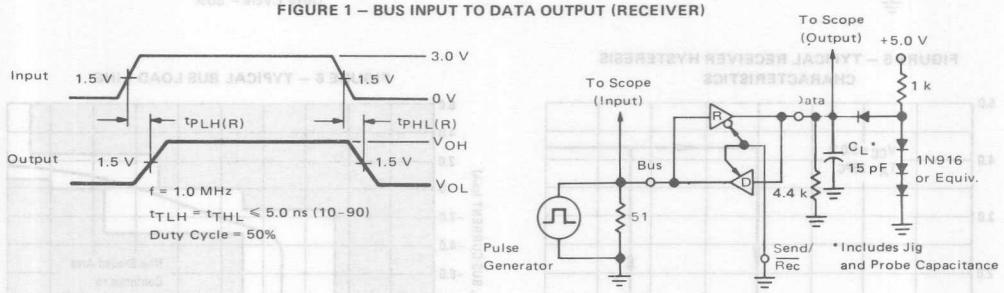


FIGURE 2 — DATA INPUT TO BUS OUTPUT (DRIVER)

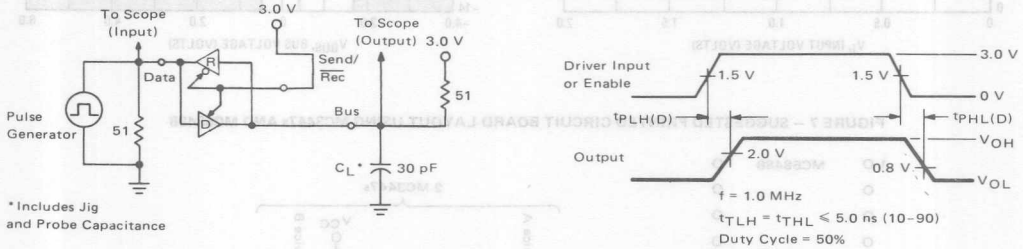
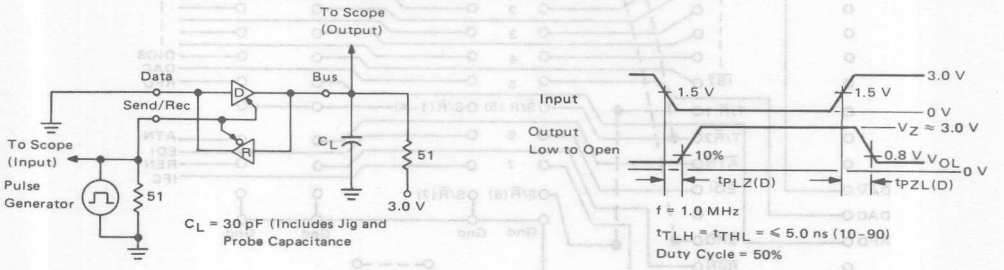


FIGURE 3 — SEND/RECEIVE INPUT TO BUS OUTPUT (DRIVER)



7

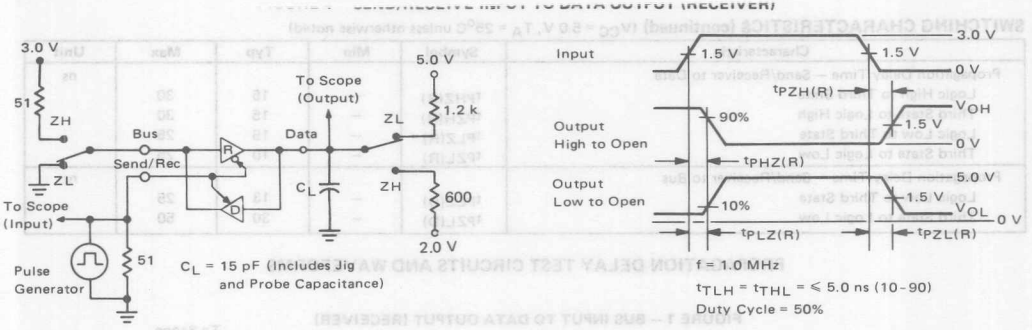


FIGURE 5 – TYPICAL RECEIVER HYSTERESIS CHARACTERISTICS

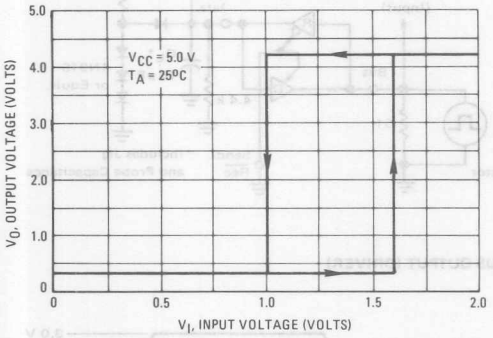


FIGURE 6 – TYPICAL BUS LOAD LINE

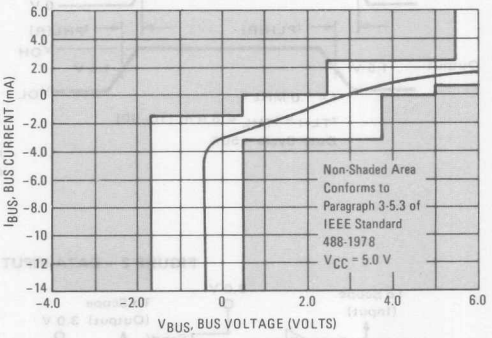


FIGURE 7 – SUGGESTED PRINTED CIRCUIT BOARD LAYOUT USING MC3447s AND MC68488

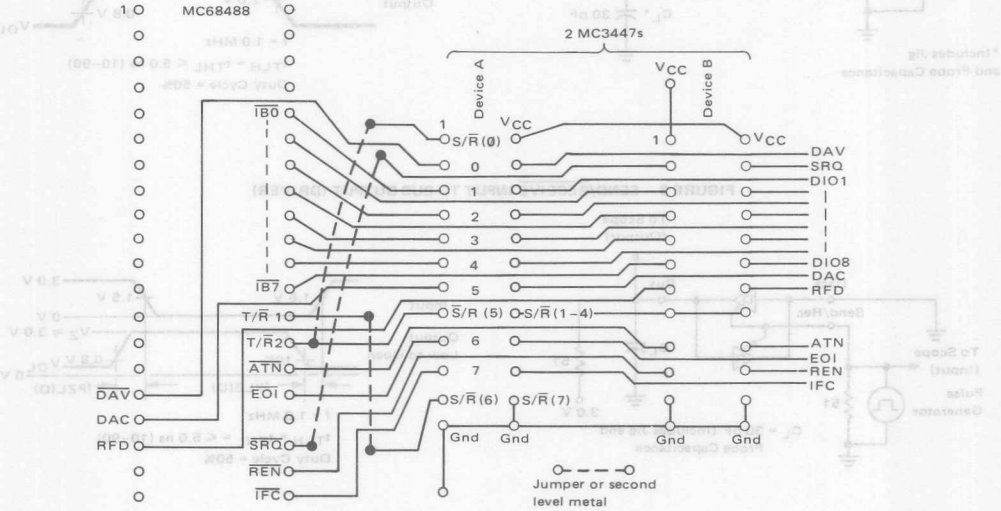
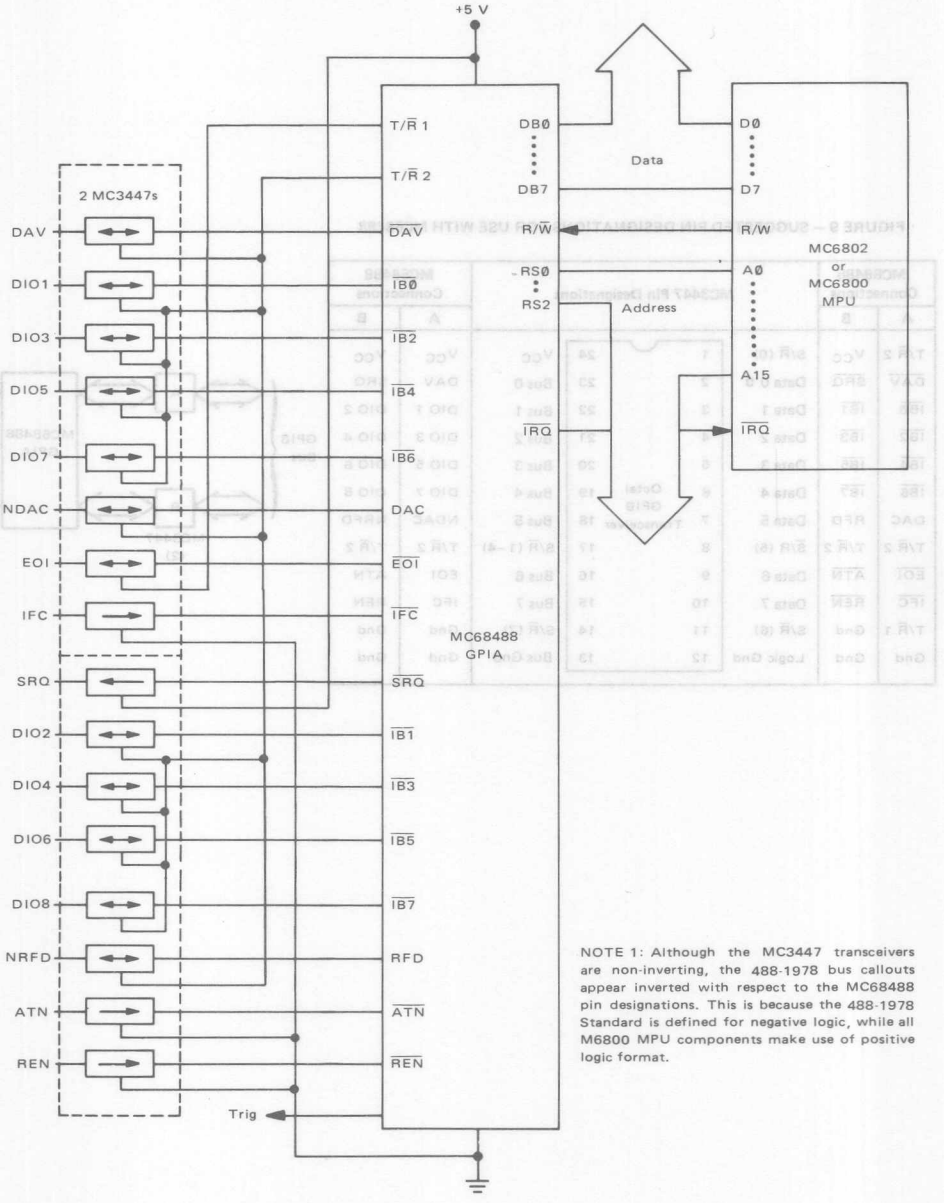


FIGURE 8 – SIMPLE SYSTEM CONFIGURATION

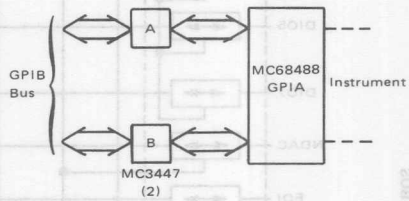


NOTE 1: Although the MC3447 transceivers are non-inverting, the 488-1978 bus callouts appear inverted with respect to the MC68488 pin designations. This is because the 488-1978 Standard is defined for negative logic, while all M6800 MPU components make use of positive logic format.

7

FIGURE 9 – SUGGESTED PIN DESIGNATIONS FOR USE WITH MC68488

MC68488 Connections		MC3447 Pin Designations			MC68488 Connections	
A	B				A	B
T/$\overline{R}$ 2	V_{CC}	S/$\overline{R}$ (0)	1	24 V_{CC}	V_{CC}	V_{CC}
$\overline{DAV}$	$\overline{SRQ}$	Data 0 0	2	23 Bus 0	DAV	SRQ
$\overline{IB0}$	$\overline{IB1}$	Data 1	3	22 Bus 1	DIO 1	DIO 2
$\overline{IB2}$	$\overline{IB3}$	Data 2	4	21 Bus 2	DIO 3	DIO 4
$\overline{IB4}$	$\overline{IB5}$	Data 3	5	20 Bus 3	DIO 5	DIO 6
$\overline{IB6}$	$\overline{IB7}$	Data 4	6	Octal GPIB 19 Bus 4	DIO 7	DIO 8
DAC	RFD	Data 5	7	Transceiver 18 Bus 5	NDAC	NRFD
T/$\overline{R}$ 2	T/$\overline{R}$ 2	$\overline{S}$/R (5)	8	17 S/$\overline{R}$ (1–4)	T/$\overline{R}$ 2	T/$\overline{R}$ 2
$\overline{EOI}$	$\overline{ATN}$	Data 6	9	16 Bus 6	EOI	ATN
$\overline{IFC}$	$\overline{REN}$	Data 7	10	15 Bus 7	IFC	REN
T/$\overline{R}$ 1	Gnd	S/$\overline{R}$ (6)	11	14 S/$\overline{R}$ (7)	Gnd	Gnd
Gnd	Gnd	Logic Gnd	12	13 Bus Gnd	Gnd	Gnd



7

MOTOROLA

MC3448A

BIDIRECTIONAL INSTRUMENTATION BUS (GPIB) TRANSCEIVER

QUAD THREE-STATE BUS TRANSCEIVER WITH TERMINATION NETWORKS

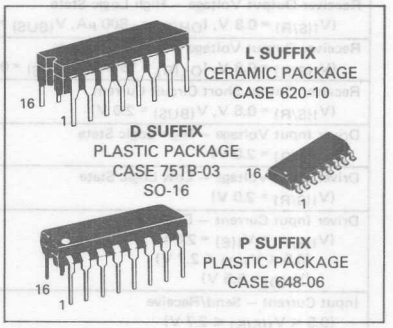
SILICON MONOLITHIC INTEGRATED CIRCUIT

This bidirectional bus transceiver is intended as the interface between TTL or MOS logic and the IEEE Standard Instrumentation Bus (488-1978, often referred to as GPIB). The required bus termination is internally provided.

Each driver/receiver pair forms the complete interface between the bus and an instrument. Either the driver or the receiver of each channel is enabled by its corresponding Send/Receive input with the disabled output of the pair forced to a high impedance state. An additional option allows the driver outputs to be operated in an open collector(1) or active pull-up configuration. The receivers have input hysteresis to improve noise margin, and their input loading follows the bus standard specifications.

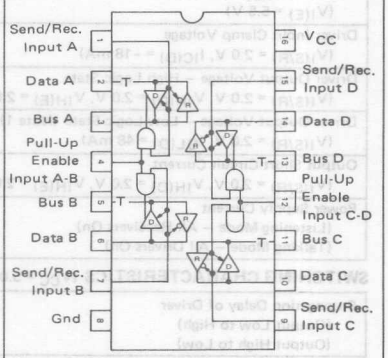
- Four Independent Driver/Receiver Pairs
- Three-State Outputs
- High Impedance Inputs
- Receiver Hysteresis – 600 mV (Typ)
- Fast Propagation Times – 15–20 ns (Typ)
- TTL Compatible Receiver Outputs
- Single +5 Volt Supply
- Open Collector Driver Output Option(1)
- Power Up/Power Down Protection
  (No Invalid Information Transmitted to Bus)
- No Bus Loading When Power Is Removed From Device
- Required Termination Characteristics Provided

(1) Selection of the "Open Collector" configuration, in fact, selects an open collector device with a passive pull-up load/termination which conforms to Figure 7, IEEE 488-1978 Bus Standard.

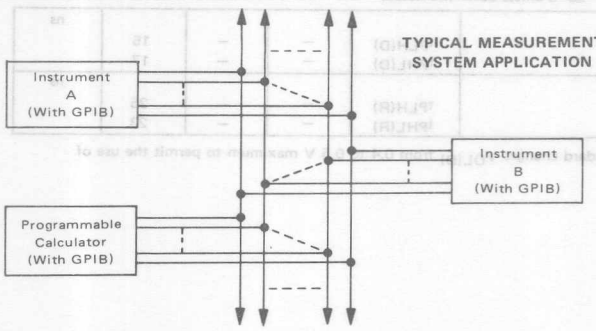


MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Input Voltage	V_I	5.5	Vdc
Driver Output Current	$I_{O(D)}$	150	mA
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C



-T- = Bus Termination



TRUTH TABLE

Send/Rec.	Enable	Info. Flow	Comments
0	X	Bus → Data	–
1	1	Data → Bus	Active Pull-Up
1	0	Data → Bus	Open Col.

X = Don't Care

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ELECTRICAL CHARACTERISTICS

(Unless otherwise noted 4.75 V ≤ V_{CC} ≤ 5.25 V and 0 ≤ T_A ≤ 70°C; typical values are at T_A = 25°C, V_{CC} = 5.0 V)

Characteristic	Symbol	Min	Typ	Max	Unit
Bus Voltage					V
(Bus Pin Open) ($V_{I(S/R)}$ = 0.8 V)	$V_{(BUS)}$	2.75	–	3.7	
($I_{(BUS)}$ = –12 mA)	$V_{IC(BUS)}$	–	–	–1.5	
Bus Current	$I_{(BUS)}$				mA
(5.0 V ≤ $V_{(BUS)}$ ≤ 5.5 V)		0.7	–	2.5	
($V_{(BUS)}$ = 0.5 V)		–1.3	–	–3.2	
(V_{CC} = 0 V, 0 V ≤ $V_{(BUS)}$ ≤ 2.75 V)		–	–	+0.04	
Receiver Input Hysteresis	–	400	600	–	mV
($V_{I(S/R)}$ = 0.8 V)					
Receiver Input Threshold					V
($V_{I(S/R)}$ = 0.8 V, Low to High)	$V_{ILH(R)}$	–	1.6	1.8	
($V_{I(S/R)}$ = 0.8 V, High to Low)	$V_{IHL(R)}$	0.8	1.0	–	
Receiver Output Voltage – High Logic State	$V_{OH(R)}$	2.7	–	–	V
($V_{I(S/R)}$ = 0.8 V, $I_{OH(R)}$ = –800 μA, $V_{(BUS)}$ = 2.0 V)					
Receiver Output Voltage – Low Logic State	$V_{OL(R)}$	–	–	0.5	V
($V_{I(S/R)}$ = 0.8 V, $I_{OL(R)}$ = 16 mA, $V_{(BUS)}$ = 0.8 V)					
Receiver Output Short Circuit Current	$I_{OS(R)}$	–15	–	–75	mA
($V_{I(S/R)}$ = 0.8 V, $V_{(BUS)}$ = 2.0 V)					
Driver Input Voltage – High Logic State	$V_{IH(D)}$	2.0	–	–	V
($V_{I(S/R)}$ = 2.0 V)					
Driver Input Voltage – Low Logic State	$V_{IL(D)}$	–	–	0.8	V
($V_{I(S/R)}$ = 2.0 V)					
Driver Input Current – Data Pins					μA
($V_{I(S/R)}$ = $V_{I(E)}$ = 2.0 V)					
(0.5 ≤ $V_{I(D)}$ ≤ 2.7 V)	$I_{I(D)}$	–200	–	40	
($V_{I(D)}$ = 5.5 V)	$I_{IB(D)}$	–	–	200	
Input Current – Send/Receive					μA
(0.5 ≤ $V_{I(S/R)}$ ≤ 2.7 V)	$I_{I(S/R)}$	–100	–	20	
($V_{I(S/R)}$ = 5.5 V)	$I_{IB(S/R)}$	–	–	100	
Input Current – Enable					μA
(0.5 ≤ $V_{I(E)}$ ≤ 2.7 V)	$I_{I(E)}$	–200	–	20	
($V_{I(E)}$ = 5.5 V)	$I_{IB(E)}$	–	–	100	
Driver Input Clamp Voltage	$V_{IC(D)}$	–	–	–1.5	V
($V_{I(S/R)}$ = 2.0 V, $I_{IC(D)}$ = –18 mA)					
Driver Output Voltage – High Logic State	$V_{OH(D)}$	2.5	–	–	V
($V_{I(S/R)}$ = 2.0 V, $V_{IH(D)}$ = 2.0 V, $V_{IH(E)}$ = 2.0 V, I_{OH} = –5.2 mA)					
Driver Output Voltage – Low Logic State (Note 1)	$V_{OL(D)}$	–	–	0.5	V
($V_{I(S/R)}$ = 2.0 V, $I_{OL(D)}$ = 48 mA)					
Output Short Circuit Current	$I_{OS(D)}$	–30	–	–120	mA
($V_{I(S/R)}$ = 2.0 V, $V_{IH(D)}$ = 2.0 V, $V_{IH(E)}$ = 2.0 V)					
Power Supply Current					mA
(Listening Mode – All Receivers On)	I_{CCL}	–	63	85	
(Talking Mode – All Drivers On)	I_{CCH}	–	106	125	

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted)

Propagation Delay of Driver					ns
(Output Low to High)	$t_{PLH(D)}$	–	–	15	
(Output High to Low)	$t_{PHL(D)}$	–	–	17	
Propagation Delay of Receiver					ns
(Output Low to High)	$t_{PLH(R)}$	–	–	25	
(Output High to Low)	$t_{PHL(R)}$	–	–	23	

NOTE 1. A modification of the IEEE 488-1978 Bus Standard changes $V_{OL(D)}$ from 0.4 to 0.5 V maximum to permit the use of Schottky technology.

SWITCHING CHARACTERISTICS (continued) (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time — Send/Receive to Data					ns
Logic High to Third State	$t_{PHZ(R)}$	–	–	30	
Third State to Logic High	$t_{PZH(R)}$	–	–	30	
Logic Low to Third State	$t_{PLZ(R)}$	–	–	30	
Third State to Logic Low	$t_{PZL(R)}$	–	–	30	
Propagation Delay Time — Send/Receive to Bus					ns
Logic High to Third State	$t_{PHZ(D)}$	–	–	30	
Third State to Logic High	$t_{PZH(D)}$	–	–	30	
Logic Low to Third State	$t_{PLZ(D)}$	–	–	30	
Third State to Logic Low	$t_{PZL(D)}$	–	–	30	
Turn-On Time — Enable to Bus					ns
Pull-Up Enable to Open Collector	$t_{POFF(E)}$	–	–	30	
Open Collector to Pull-Up Enable	$t_{PON(E)}$	–	–	20	

PROPAGATION DELAY TEST CIRCUITS AND WAVEFORMS

FIGURE 1 — BUS INPUT TO DATA OUTPUT (RECEIVER)

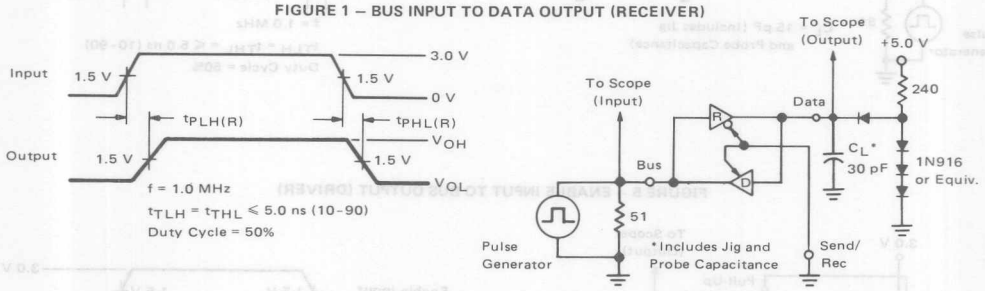


FIGURE 2 — DATA INPUT TO BUS OUTPUT (DRIVER)

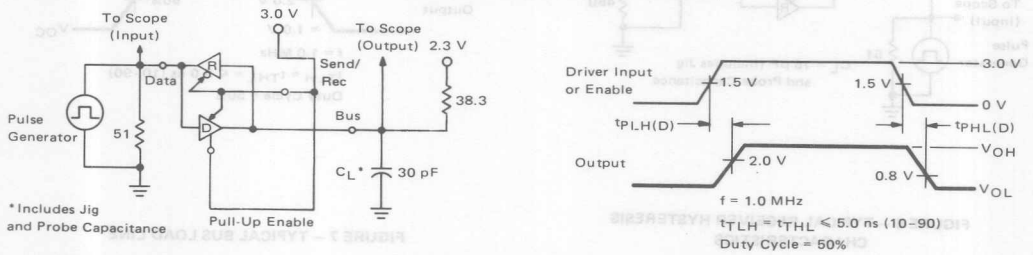
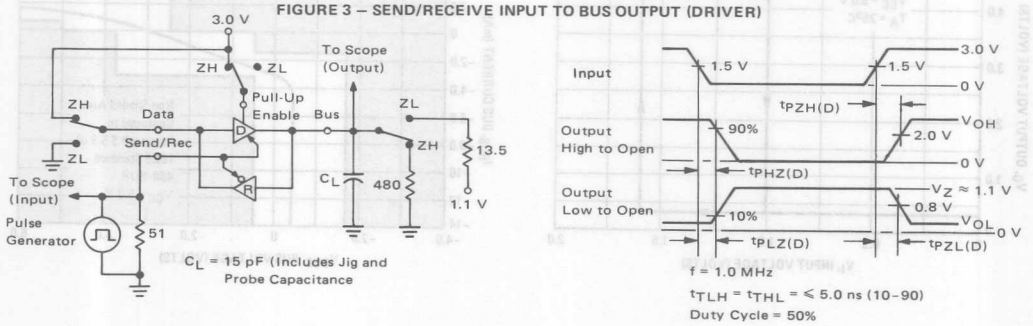


FIGURE 3 — SEND/RECEIVE INPUT TO BUS OUTPUT (DRIVER)



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FIGURE 4 – SEND/RECEIVE INPUT TO DATA OUTPUT (RECEIVER)

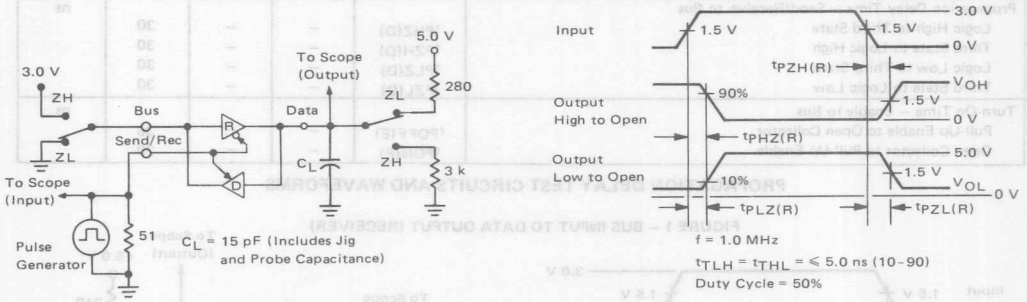


FIGURE 5 – ENABLE INPUT TO BUS OUTPUT (DRIVER)

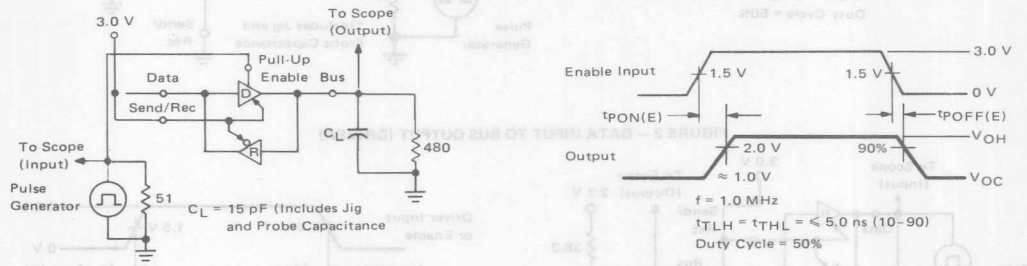


FIGURE 6 – TYPICAL RECEIVER HYSTERESIS CHARACTERISTICS

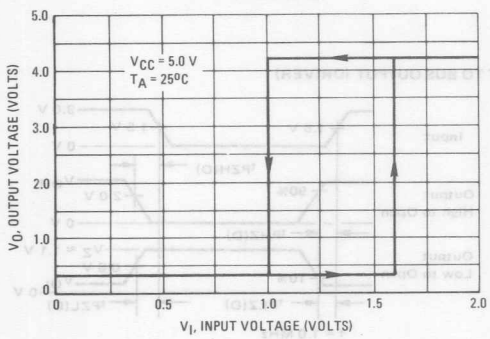


FIGURE 7 – TYPICAL BUS LOAD LINE

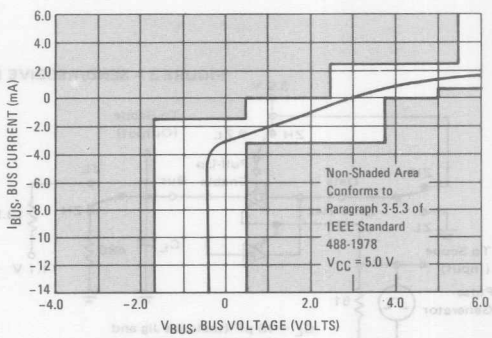
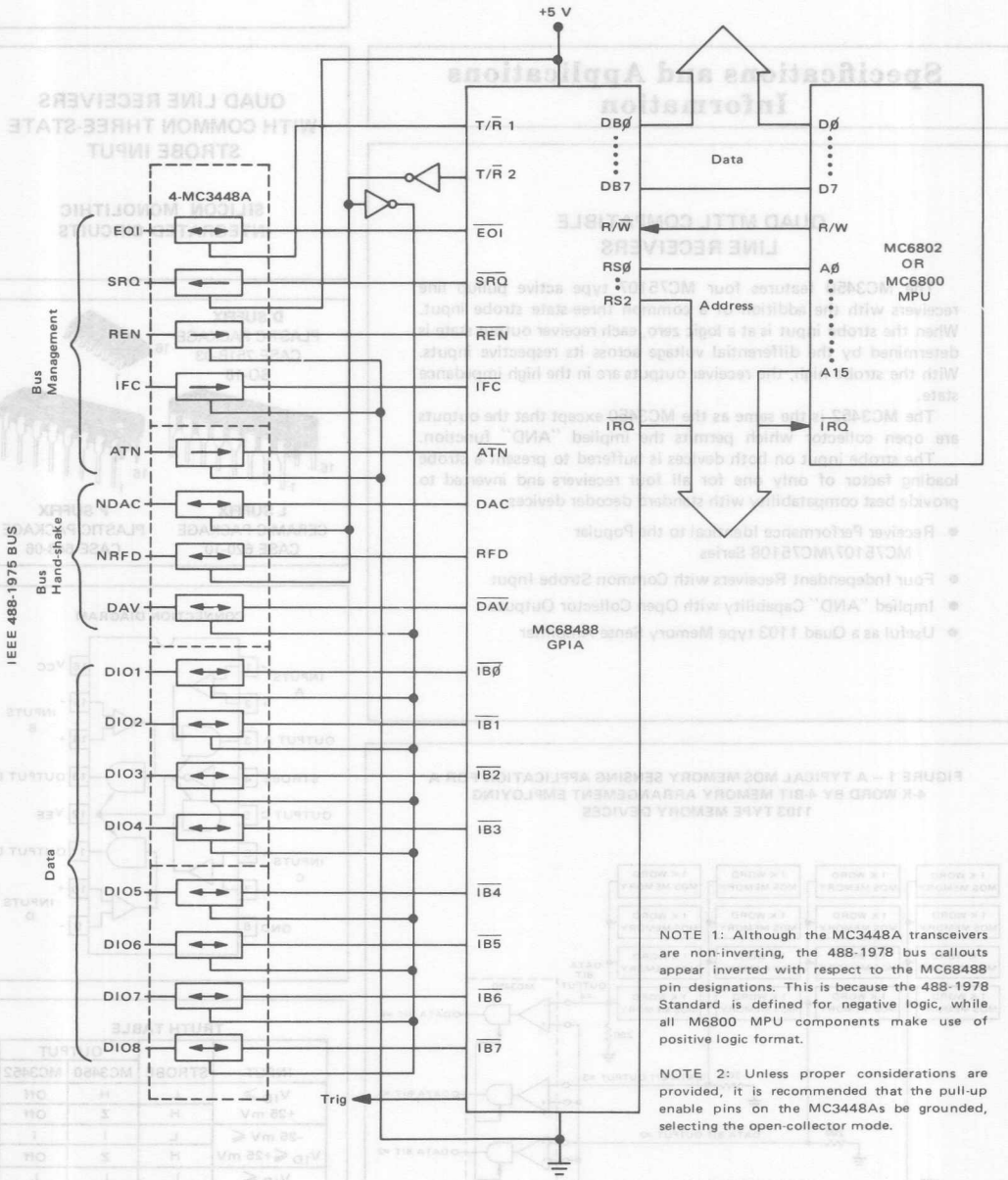


FIGURE 8 – SIMPLE SYSTEM CONFIGURATION



NOTE 1: Although the MC3448A transceivers are non-inverting, the 488-1978 bus callouts appear inverted with respect to the MC68488 pin designations. This is because the 488-1978 Standard is defined for negative logic, while all M6800 MPU components make use of positive logic format.

NOTE 2: Unless proper considerations are provided, it is recommended that the pull-up enable pins on the MC3448As be grounded, selecting the open-collector mode.

7

MC3452

Specifications and Applications Information

QUAD MTTL COMPATIBLE LINE RECEIVERS

The MC3450 features four MC75107 type active pullup line receivers with the addition of a common three-state strobe input. When the strobe input is at a logic zero, each receiver output state is determined by the differential voltage across its respective inputs. With the strobe high, the receiver outputs are in the high impedance state.

The MC3452 is the same as the MC3450 except that the outputs are open collector which permits the implied "AND" function.

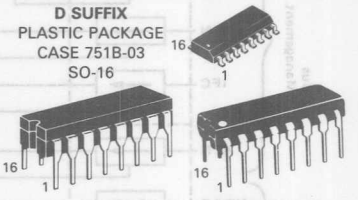
The strobe input on both devices is buffered to present a strobe loading factor of only one for all four receivers and inverted to provide best compatability with standard decoder devices.

- Receiver Performance Identical to the Popular MC75107/MC75108 Series
- Four Independent Receivers with Common Strobe Input
- Implied "AND" Capability with Open Collector Outputs
- Useful as a Quad 1103 type Memory Sense Amplifier

QUAD LINE RECEIVERS WITH COMMON THREE-STATE STROBE INPUT

SILICON MONOLITHIC INTEGRATED CIRCUITS

D SUFFIX
PLASTIC PACKAGE
CASE 751B-03
SO-16



L SUFFIX
CERAMIC PACKAGE
CASE 620-10

P SUFFIX
PLASTIC PACKAGE
CASE 648-06

CONNECTION DIAGRAM

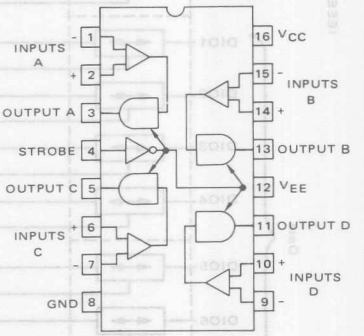
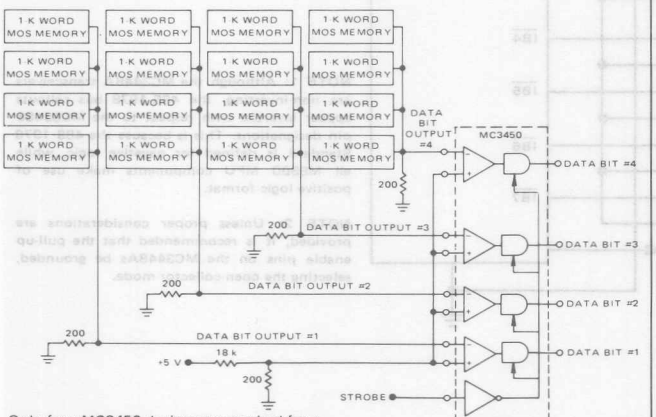


FIGURE 1 – A TYPICAL MOS MEMORY SENSING APPLICATION FOR A 4-K WORD BY 4-BIT MEMORY ARRANGEMENT EMPLOYING 1103 TYPE MEMORY DEVICES



Only four MC3450 devices are required for a 4-k word by 16-bit memory system.

TRUTH TABLE

INPUT	STROBE	OUTPUT MC3450	OUTPUT MC3452
$V_{ID} \geq$ +25 mV	L	H	Off
	H	Z	Off
-25 mV $\leq V_{ID} \leq$ +25 mV	L	I	I
	H	Z	Off
$V_{ID} \leq$ -25 mV	L	L	L
	H	Z	Off

L = Low Logic State
H = High Logic State
Z = Third (High Impedance) State
I = Indeterminate State

MAXIMUM RATINGS (T_A = 0 to +70°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC}, V_{EE}	±7.0	Vdc
Differential-Mode Input Signal Voltage Range	V_{IDR}	±6.0	Vdc
Common-Mode Input Voltage Range	V_{ICR}	±5.0	Vdc
Strobe Input Voltage	$V_{I(S)}$	5.5	Vdc
Power Dissipation (Package Limitation) Ceramic Dual In-Line Package Derate above T_A = +25°C Plastic Dual In-Line Package Derate above T_A = +25°C	P_D	 1000 6.6 1000 6.6	 mW mW/°C mW mW/°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltages	V_{CC} V_{EE}	+4.75 -4.75	+5.0 -5.0	+5.25 -5.25	Vdc
Output Load Current	I_{OL}	–	–	16	mA
Differential-Mode Input Voltage Range	V_{IDR}	-5.0	–	+5.0	Vdc
Common-Mode Input Voltage Range	V_{ICR}	-3.0	–	+3.0	Vdc
Input Voltage Range (any input to Ground)	V_{IR}	-5.0	–	+3.0	Vdc

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = -5.0 Vdc, T_A = 0 to +70°C unless otherwise noted.)

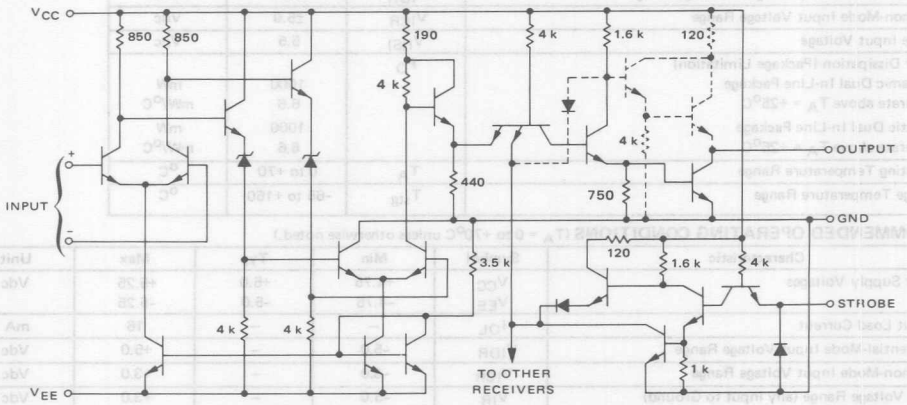
Characteristic	Symbol	Fig.	MC3450			MC3452			Unit
			Min	Typ	Max	Min	Typ	Max	
High Level Input Current to Receiver Input	$I_{IH(I)}$	7	–	–	75	–	–	75	μA
Low Level Input Current to Receiver Input	$I_{IL(I)}$	8	–	–	-10	–	–	-10	μA
High Level Input Current to Strobe Input $V_{IH(S)}$ = +2.4 V $V_{IH(S)}$ = +5.25 V	$I_{IH(S)}$	5	 – –	 – –	 40 1.0	 – –	 – –	 40 1.0	 μA mA
Low Level Input Current to Strobe Input $V_{IH(S)}$ = +0.4 V	$I_{IL(S)}$	5	–	–	-1.6	–	–	-1.6	mA
High Level Output Voltage	V_{OH}	3	2.4	–	–	–	–	–	Vdc
High Level Output Leakage Current	I_{CEX}	3	–	–	–	–	–	250	μA
Low Level Output Voltage	V_{OL}	3	–	–	0.5	–	–	0.5	Vdc
Short-Circuit Output Current	I_{OS}	6	-18	–	-70	–	–	–	mA
Output Disable Leakage Current	I_{off}	9	–	–	40	–	–	–	μA
High Logic Level Supply Current from V_{CC}	I_{CCH}	4	–	45	60	–	45	60	mA
High Logic Level Supply Current from V_{EE}	I_{EEH}	4	–	-17	-30	–	-17	-30	mA

SWITCHING CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = -5.0 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	Fig.	MC3450			MC3452			Unit
			Min	Typ	Max	Min	Typ	Max	
High to Low Logic Level Propagation Delay Time (Differential Inputs)	$t_{PHL(D)}$	10	–	–	25	–	–	25	ns
Low to High Logic Level Propagation Delay Time (Differential Inputs)	$t_{PLH(D)}$	10	–	–	25	–	–	25	ns
Open State to High Logic Level Propagation Delay Time (Strobe)	$t_{PZH(S)}$	11	–	–	21	–	–	–	ns
High Logic Level to Open State Propagation Delay Time (Strobe)	$t_{PHZ(S)}$	11	–	–	18	–	–	–	ns
Open State to Low Logic Level Propagation Delay Time (Strobe)	$t_{PZL(S)}$	11	–	–	27	–	–	–	ns
Low Logic Level to Open State Propagation Delay Time (Strobe)	$t_{PLZ(S)}$	11	–	–	29	–	–	–	ns
High Logic to Low Logic Level Propagation Delay Time (Strobe)	$t_{PHL(S)}$	12	–	–	–	–	–	25	ns
Low Logic to High Logic Level Propagation Delay Time (Strobe)	$t_{PLH(S)}$	12	–	–	–	–	–	25	ns

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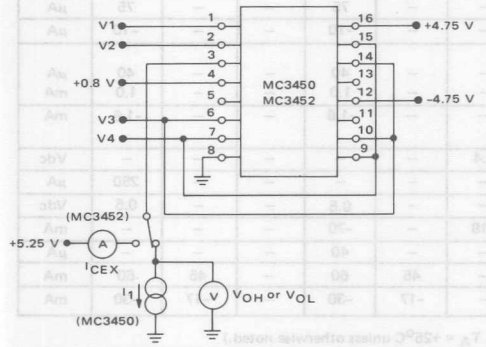
FIGURE 2 – CIRCUIT SCHEMATIC
(1/4 Circuit Shown)



Dashed components apply to the MC3450 circuit only.

TEST CIRCUITS

FIGURE 3 – I_{CEX}, V_{OH}, AND V_{OL}



TEST TABLE

	V1		V2		V3		V4		
	MC3450	MC3452	MC3450	MC3452	MC3450	MC3452	MC3450	MC3452	I1
V_{OH}	+2.975 V	–	+3.0 V	–	+3.0 V	–	GND	–	+0.4 mA
	-3.0 V	–	-2.975 V	–	GND	–	-3.0 V	–	
I_{CEX}	–	+2.975 V	–	+3.0 V	–	+3.0 V	–	GND	–
	–	-3.0 V	–	-2.975 V	–	GND	–	-3.0 V	–
V_{OL}	+3.0 V	+3.0 V	+2.975 V	+2.975 V	GND	GND	+3.0 V	+3.0 V	-16 mA
	-2.975 V	-2.975 V	-3.0 V	-3.0 V	-3.0 V	-3.0 V	GND	GND	

Channel A shown under test. Other channels are tested similarly.

FIGURE 4 – I_{CCH} AND I_{EEH}

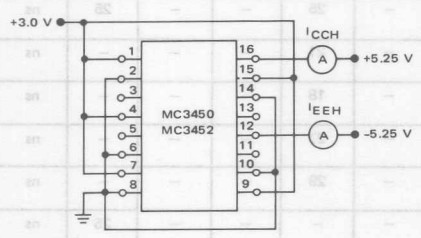
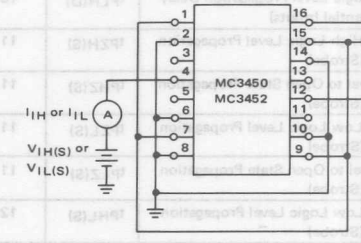
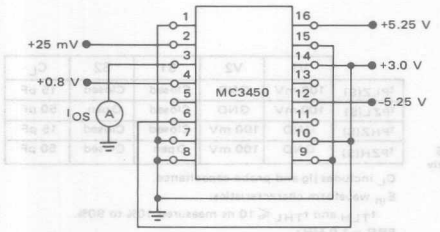


FIGURE 5 – $I_{IH(S)}$ AND $I_{IL(S)}$



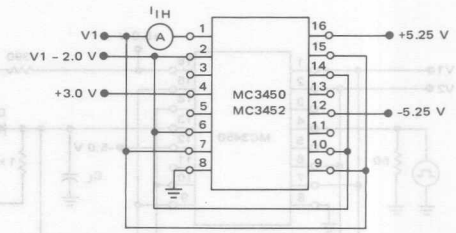
TEST CIRCUITS (continued)

FIGURE 6 – I_{OS}



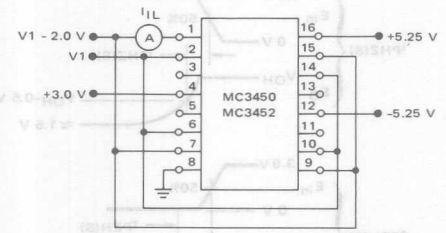
Channel A shown under test, other channels are tested similarly. Only one output shorted at a time.

FIGURE 7 – I_{IH}



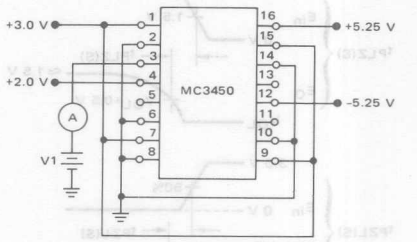
Channel A(-) shown under test, other channels are tested similarly. Devices are tested with V1 from +3.0 V to -3.0 V.

FIGURE 8 – I_{IL}



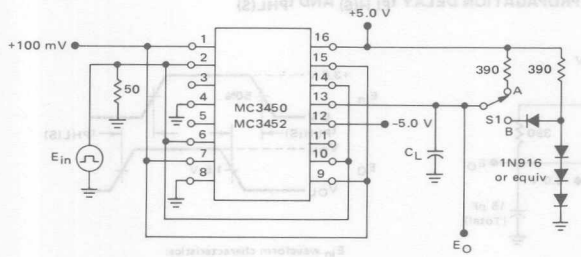
Channel A(-) shown under test, other channels are tested similarly. Devices are tested with V1 from +3.0 V to -3.0 V.

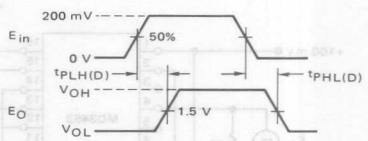
FIGURE 9 – I_{off}



Output of Channel A shown under test, other outputs are tested similarly for V1 = 0.4 V and +2.4 V.

FIGURE 10 – RECEIVER PROPAGATION DELAY $t_{PLH(D)}$ AND $t_{PHL(D)}$





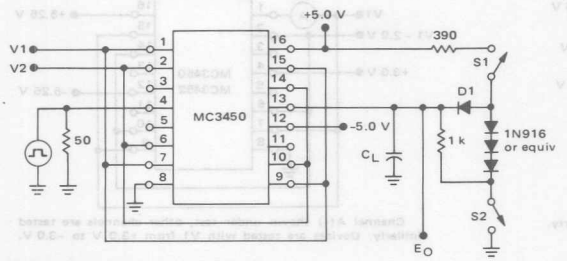
Output of Channel B shown under test, other channels are tested similarly.

S1 at "A" for MC3452
S1 at "B" for MC3450
C_L = 15 pF total for MC3452
C_L = 50 pF total for MC3450

E_{in} waveform characteristics:
t_{TLH} and $t_{THL} \leq$ 10 ns measured 10% to 90%
PRR = 1.0 MHz
Duty Cycle = 500 ns

7

FIGURE 11 – STROBE PROPAGATION DELAY TIMES $t_{PLZ(S)}$, $t_{PZL(S)}$, $t_{PHZ(S)}$ and $t_{PZH(S)}$



Output of Channel B shown under test, other channels are tested similarly.

	V1	V2	S1	S2	C_L
$t_{PLZ(S)}$	100 mV	GND	Closed	Closed	15 pF
$t_{PZL(S)}$	100 mV	GND	Closed	Open	50 pF
$t_{PHZ(S)}$	GND	100 mV	Closed	Closed	15 pF
$t_{PZH(S)}$	GND	100 mV	Open	Closed	50 pF

C_L includes jig and probe capacitance.
E_{in} waveform characteristics:
t_{TLH} and $t_{THL} \leqslant 10$ ns measured 10% to 90%.
PRR = 1.0 MHz
Duty Cycle = 50%

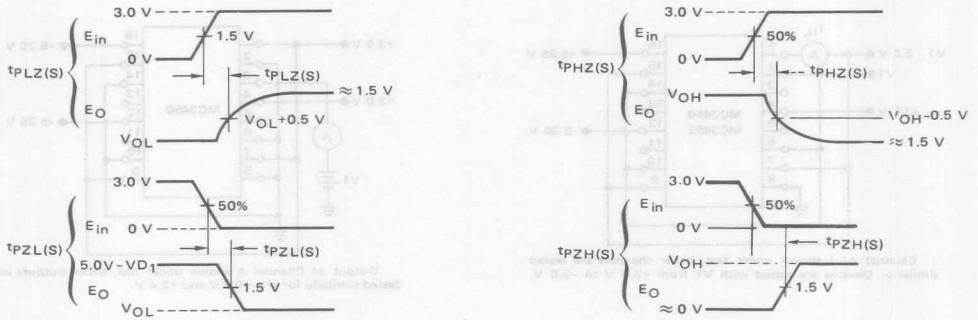
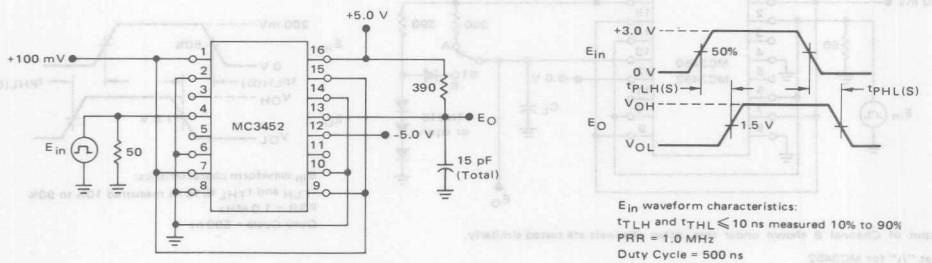


FIGURE 12 – STROBE PROPAGATION DELAY $t_{PLH(S)}$ AND $t_{PHL(S)}$

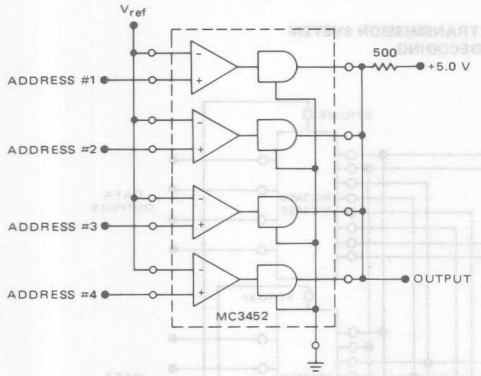


Output of Channel B shown under test, other channels are tested similarly.

E_{in} waveform characteristics:
t_{TLH} and $t_{THL} \leqslant 10$ ns measured 10% to 90%
PRR = 1.0 MHz
Duty Cycle = 500 ns

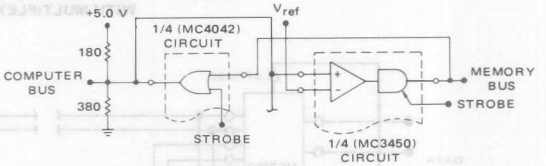
APPLICATIONS INFORMATION

FIGURE 13 – IMPLIED "AND" GATING



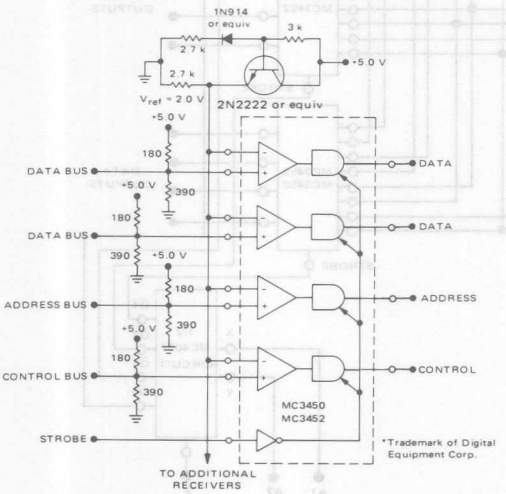
The MC3452 can be used for address decoding as illustrated above. All outputs of the MC3452 are tied together through a common resistor to +5.0 volts. In this configuration the MC3452 provides the "AND" function. All addresses have to be true before the output will go high. This scheme eliminates the need for an "AND" gate and enhances speed throughput for address decoding.

FIGURE 14 – BIDIRECTIONAL DATA TRANSMISSION



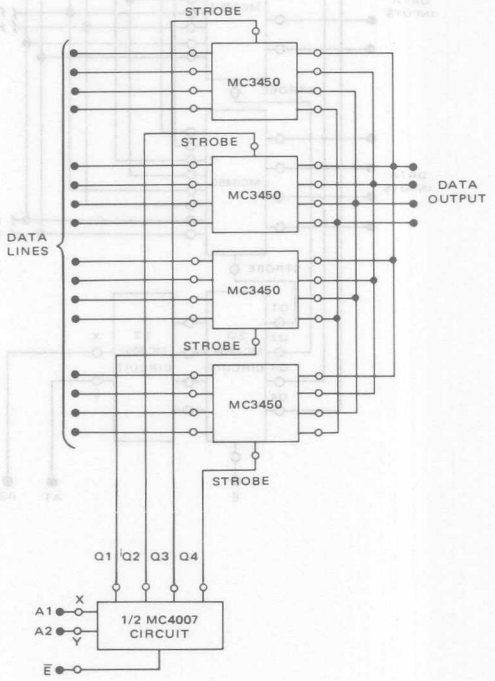
The three-state capability of the MC3450 permits bidirectional data transmission as illustrated.

FIGURE 15 – SINGLE-ENDED UNI-BUS* LINE RECEIVER APPLICATION FOR MINICOMPUTERS



The MC3450/3452 can be used for single-ended as well as differential line receiving. For single-ended line receiver applications, such as are encountered in minicomputers, the configuration shown in Figure 15 can be used. The voltage source, which generates V_{ref}, should be designed so that the V_{ref} voltage is halfway between V_{OH}(min) and V_{OL}(max). The maximum input overdrive required to guarantee a given logic state is extremely small, 25 mV maximum. This low-input overdrive enhances differential noise immunity. Also the high-input impedance of the line receiver permits many receivers to be placed on a single line with minimum load effects.

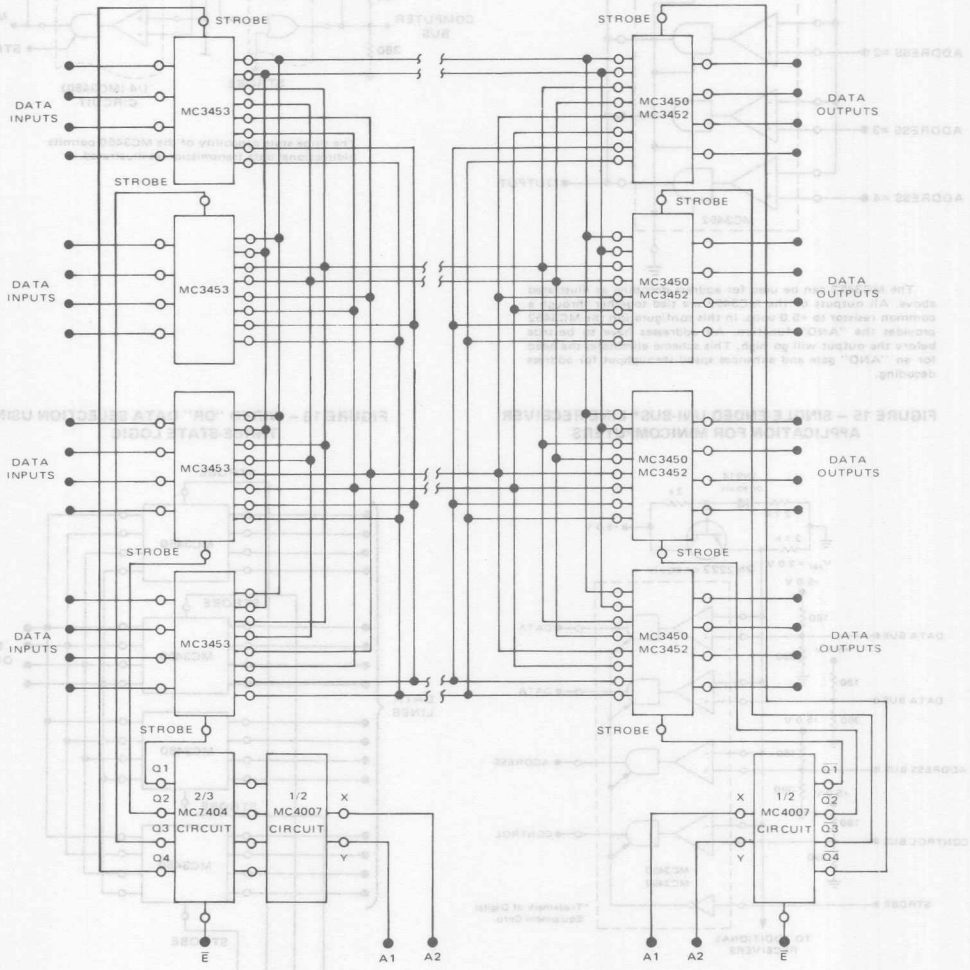
FIGURE 16 – WIRED "OR" DATA SELECTION USING THREE-STATE LOGIC



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APPLICATIONS INFORMATION (continued)

FIGURE 17 – PARTY-LINE DATA TRANSMISSION SYSTEM WITH MULTIPLEX DECODING



MOTOROLA

MC3453

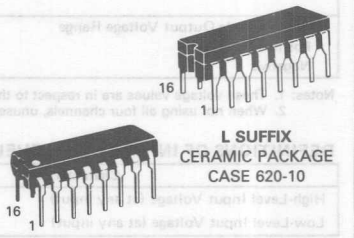
QUAD LINE DRIVER WITH COMMON INHIBIT INPUT

SILICON MONOLITHIC INTEGRATED CIRCUIT

MTTL COMPATIBLE QUAD LINE DRIVER

The MC3453 features four SN75110 type line drivers with a common inhibit input. When the inhibit input is high, a constant output current is switched between each pair of output terminals in response to the logic level at that channel's input. When the inhibit is low, all channel outputs are nonconductive (transistors biased to cut-off). This minimizes loading in party-line systems where a large number of drivers share the same line.

- Four Independent Drivers with Common Inhibit Input
- −3.0 Volts Output Common-Mode Voltage Over Entire Operating Range
- Improved Driver Design Exceeds Performance of Popular SN75110

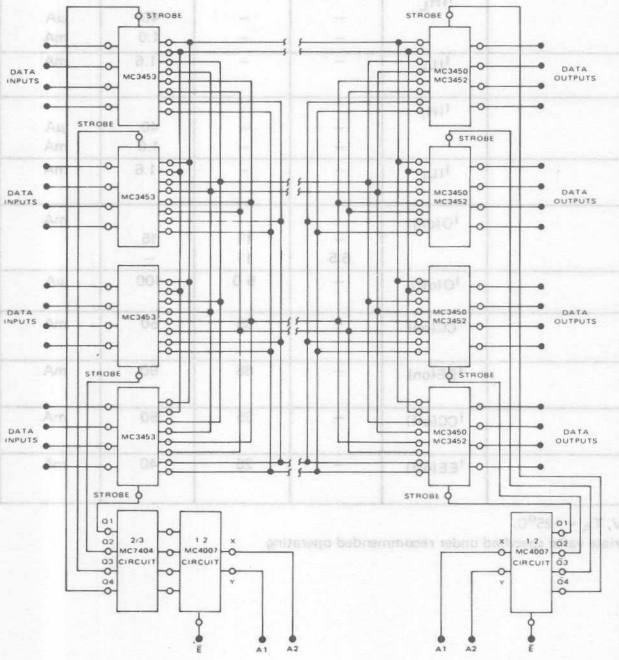


L SUFFIX
CERAMIC PACKAGE
CASE 620-10

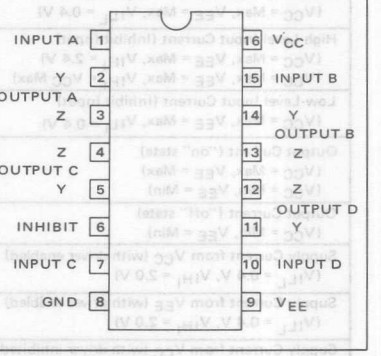
P SUFFIX
PLASTIC PACKAGE
CASE 648-06

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FIGURE 1 – PARTY-LINE DATA TRANSMISSION SYSTEM WITH MULTIPLEX DECODING



CONNECTION DIAGRAM



TRUTH TABLE
(positive logic)

LOGIC INPUT	INHIBIT INPUT	OUTPUT CURRENT	
		Z	Y
H	H	On	Off
L	H	Off	On
H	L	Off	Off
L	L	Off	Off

L = Low Logic Level
H = High Logic Level

Power Supply Voltage	V_{CC} V_{EE}	+7.0 -7.0	Volts
Logic and Inhibitor Input Voltages	V_{in}	5.5	Volts
Common-Mode Output Voltage Range	V_{OCR}	-5.0 to +12	Volts
Power Dissipation (Package Limitation) Plastic and Ceramic Dual In-Line Packages Derate above T_A = +25°C	P_D	 1000 6.6	 mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range Plastic and Ceramic Dual In-Line Packages	T_{stg}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (See Notes 1 and 2.)

Characteristic	Symbol	Min	Nom	Max	Unit
Power Supply Voltages	V_{CC} V_{EE}	+4.75 -4.75	+5.0 -5.0	+5.25 -5.25	Volts
Common-Mode Output Voltage Range Positive Negative	V_{OCR}	 0 0	 – –	 +10 -3.0	Volts

Notes: 1. These voltage values are in respect to the ground terminal.
2. When not using all four channels, unused outputs must be grounded.

DEFINITIONS OF INPUT LOGIC LEVELS*

Characteristic	Symbol	Min	Max	Unit
High-Level Input Voltage (at any input)	V_{IH}	2.0	5.5	Volts
Low-Level Input Voltage (at any input)	V_{IL}	0	0.8	Volts

*The algebraic convention, where the most positive limit is designated maximum, is used with Logic Level Input Voltage Levels only.

7

ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C unless otherwise noted.)

Characteristic##	Symbol	Min	Typ#	Max	Unit
High-Level Input Current (Logic Inputs) (V_{CC} = Max, V_{EE} = Max, V_{IH_L} = 2.4 V) (V_{CC} = Max, V_{EE} = Max, V_{IH_L} = V_{CC} Max)	I_{IH_L}	 – –	 – –	 40 1.0	 µA mA
Low-Level Input Current (Logic Inputs) (V_{CC} = Max, V_{EE} = Max, V_{IL_L} = 0.4 V)	I_{IL_L}	–	–	-1.6	mA
High-Level Input Current (Inhibit Input) (V_{CC} = Max, V_{EE} = Max, V_{IH_I} = 2.4 V) (V_{CC} = Max, V_{EE} = Max, V_{IH_I} = V_{CC} Max)	I_{IH_I}	 – –	 – –	 40 1.0	 µA mA
Low-Level Input Current (Inhibit Input) (V_{CC} = Max, V_{EE} = Max, V_{IL_I} = 0.4 V)	I_{IL_I}	–	–	-1.6	mA
Output Current ("on" state) (V_{CC} = Max, V_{EE} = Max) (V_{CC} = Min, V_{EE} = Min)	$I_{O(on)}$	 – 6.5	 11 11	 15 –	mA
Output Current ("off" state) (V_{CC} = Min, V_{EE} = Min)	$I_{O(off)}$	–	5.0	100	µA
Supply Current from V_{CC} (with driver enabled) (V_{IL_L} = 0.4 V, V_{IH_I} = 2.0 V)	$I_{CC(on)}$	–	35	50	mA
Supply Current from V_{EE} (with driver enabled) (V_{IL_L} = 0.4 V, V_{IH_I} = 2.0 V)	$I_{EE(on)}$	–	65	90	mA
Supply Current from V_{CC} (with driver inhibited) (V_{IL_L} = 0.4 V, V_{IL_I} = 0.4 V)	$I_{CC(off)}$	–	35	50	mA
Supply Current from V_{EE} (with driver inhibited) (V_{IL_L} = 0.4 V, V_{IL_I} = 0.4 V)	$I_{EE(off)}$	–	25	40	mA

#All typical values are at V_{CC} = +5.0 V, V_{EE} = -5.0 V, T_A = +25°C.
##For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable device type.
Ground unused inputs and outputs.

SWITCHING CHARACTERISTICS (V_{CC} = +5.0 V, V_{EE} = -5.0 V, T_A = +25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time from Logic Input to Output Y or Z (R_L = 50 ohms, C_L = 40 pF)	t_{PLH_L}	–	9.0	17	ns
	t_{PHL_L}	–	9.0	17	
Propagation Delay Time from Inhibit Input to Output Y or Z (R_L = 50 ohms, C_L = 40 pF)	t_{PLH_I}	–	16	25	ns
	t_{PHL_I}	–	20	25	

FIGURE 2 – LOGIC INPUT TO OUTPUTS PROPAGATION DELAY TIME WAVEFORMS

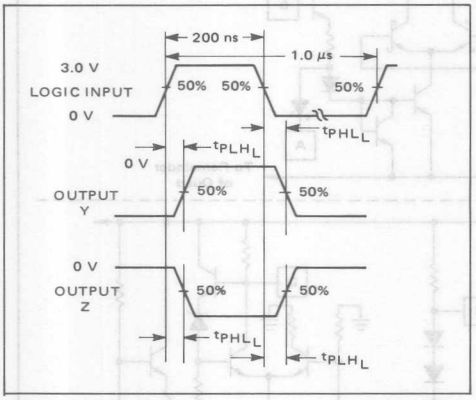
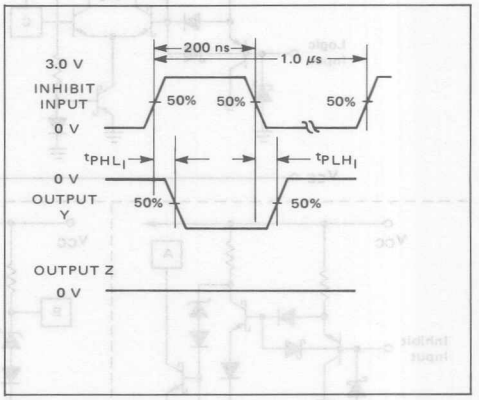


FIGURE 3 – INHIBIT INPUT TO OUTPUTS PROPAGATION DELAY TIME WAVEFORMS



TEST CIRCUITS

FIGURE 4 – LOGIC INPUT TO OUTPUT PROPAGATION DELAY TIME TEST CIRCUIT

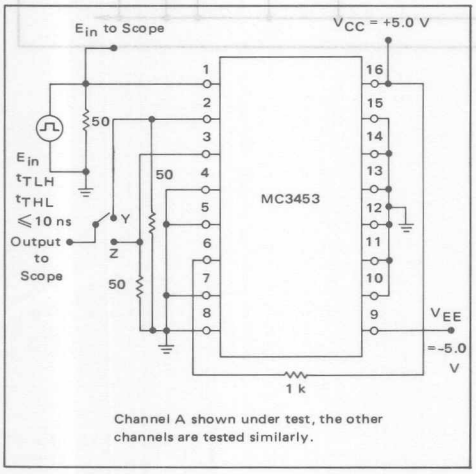
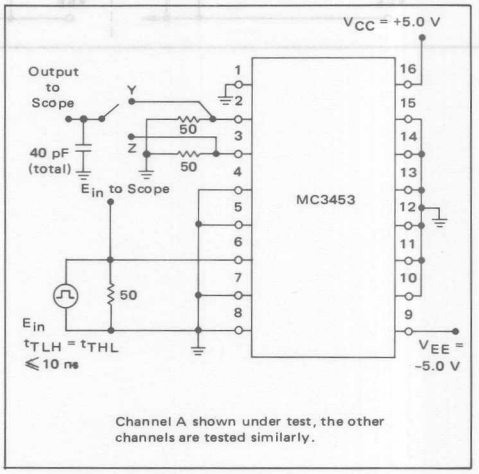
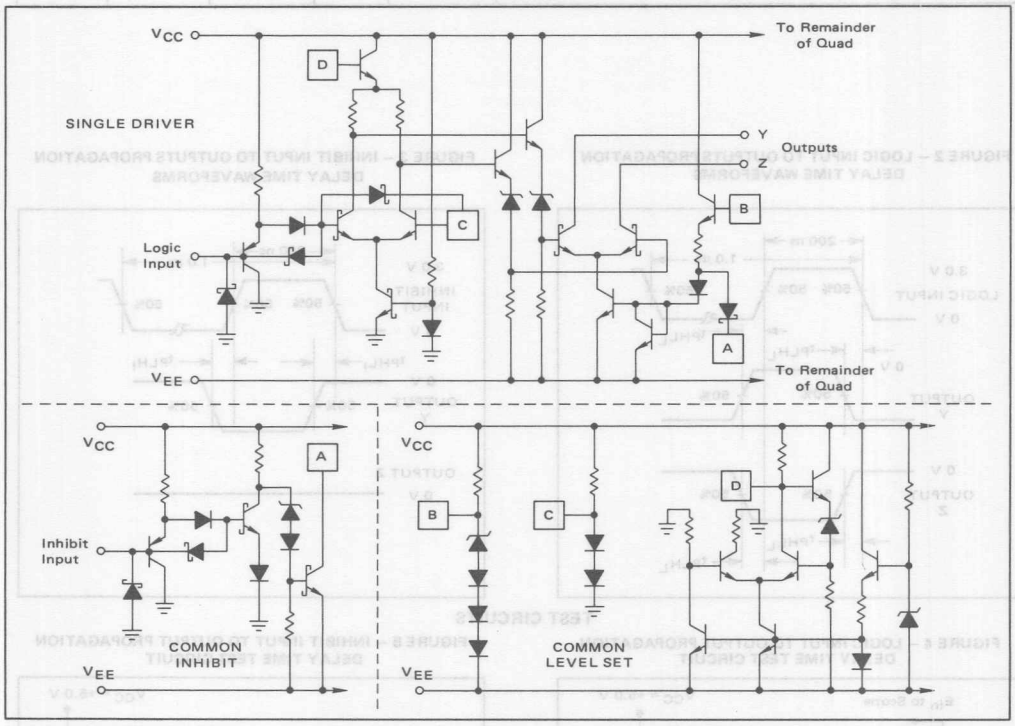


FIGURE 5 – INHIBIT INPUT TO OUTPUT PROPAGATION DELAY TIME TEST CIRCUIT



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FIGURE 6 – CIRCUIT SCHEMATIC
(1/4 Circuit Shown)



7

MOTOROLA

MC3467

TRIPLE WIDEBAND PREAMPLIFIER WITH ELECTRONIC GAIN CONTROL (EGC)

The MC3467 provides three independent preamplifiers with individual electronic gain control in a single 18-pin package. Each preamplifier has differential inputs and outputs allowing operation in completely balanced systems. The device is optimized for use in 9-track magnetic tape memory systems where low noise and low distortion are paramount objectives.

The electronic gain control allows each amplifier's gain to be set anywhere from essentially zero to a maximum of approximately 100 V/V.

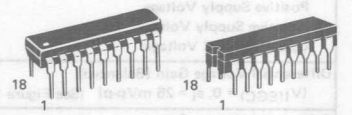
- Wide Bandwidth – 15 MHz (Typ)
- Individual Electronic Gain Control
- Differential Input/Output

TRIPLE MAGNETIC TAPE MEMORY PREAMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

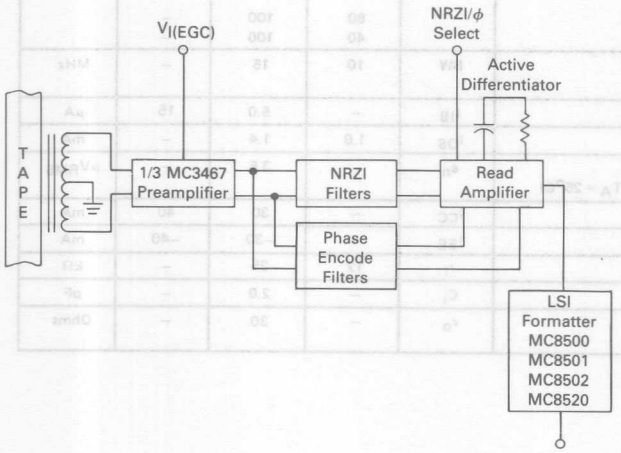
P SUFFIX
PLASTIC PACKAGE
707-02

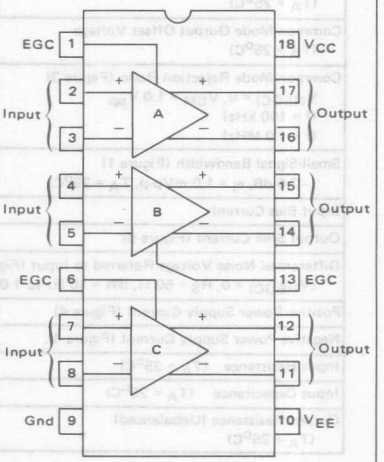
L SUFFIX
CERAMIC PACKAGE
CASE 726-04



7

TYPICAL APPLICATION
HIGH PERFORMANCE 9-TRACK OPEN REEL TAPE SYSTEM





MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltages Positive Supply Voltage Negative Supply Voltage	 V_{CC} V_{EE}	 6.0 −9.0	V
EGC Voltages (Pins 1, 6 and 13)	$V_{I(EGC)}$	−5.0 to V_{CC}	V
Input Differential Voltage	V_{ID}	±5.0	V
Input Common-Mode Voltage	V_{IC}	±5.0	V
Amplifier Output Short Circuit Duration (to Ground)	t_{sc}	10	s
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Junction Temperature	T_J	+150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = −6.0 V, f = 100 kHz, T_A = 0 to +70°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage Range Positive Supply Voltage Negative Supply Voltage Operating EGC Voltage	 V_{CCR} V_{EER} $V_{I(EGC)}$	 4.75 −5.5 0	 5.0 −6.0 –	 5.25 −7.0 V_{CC}	 V V V
Differential Voltage Gain (Balanced) ($V_{I(EGC)}$ = 0, e_i = 25 mVp-p) (See Figure 1)	A_{VD}	85	100	120	V/V
Differential Voltage Gain ($V_{I(EGC)}$ = V_{CC})	A_{VD}	–	0.5	2.0	V/V
Maximum Input Differential Voltage (Balanced) (T_A = 25°C)	V_{IDR}	0.2	–	–	V_{pp}
Output Voltage Swing (Balanced) (Figure 1) (e_i = 200 mVp-p)	V_{OR}	6.0	8.0	–	V_{pp}
Input Common-Mode Range	V_{ICR}	±1.5	±2.0	–	V
Differential Output Offset Voltage (T_A = 25°C)	V_{OOD}	–	500	–	mV
Common-Mode Output Offset Voltage (T_A = 25°C)	V_{OOC}	–	500	–	mV
Common Mode Rejection Ratio (Figure 2) $V_{I(EGC)}$ = 0, V_{CM} = 1.0 V_{pp} (f = 100 kHz) (f = 1.0 MHz)	CMRR 60 40	 100 100	 – –	dB
Small-Signal Bandwidth (Figure 1) (−3.0 dB, e_i = 1.0 mVp-p, T_A = 25°C)	BW	10	15	–	MHz
Input Bias Current	I_{IB}	–	5.0	15	μA
Output Sink Current (Figure 5)	I_{OS}	1.0	1.4	–	mA
Differential Noise Voltage Referred to Input (Figure 3) ($V_{I(EGC)}$ = 0, R_S = 50 Ω, BW = 10 Hz to 1.0 MHz, T_A = 25°C)	e_n	–	3.5	–	μV_{RMS}
Positive Power Supply Current (Figure 4)	I_{CC}	–	30	40	mA
Negative Power Supply Current (Figure 4)	I_{EE}	–	−30	−40	mA
Input Resistance (T_A = 25°C)	r_i	12	25	–	kΩ
Input Capacitance (T_A = 25°C)	C_i	–	2.0	–	pF
Output Resistance (Unbalanced) (T_A = 25°C)	r_o	–	30	–	Ohms

FIGURE 1 – DIFFERENTIAL VOLTAGE GAIN, BANDWIDTH AND OUTPUT VOLTAGE SWING TEST CIRCUIT
(Channel A under test, other channels tested similarly)

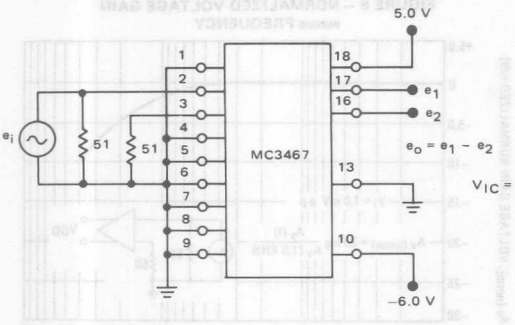


FIGURE 2 – COMMON-MODE REJECTION RATIO
(Channel A under test, other amplifiers tested similarly)

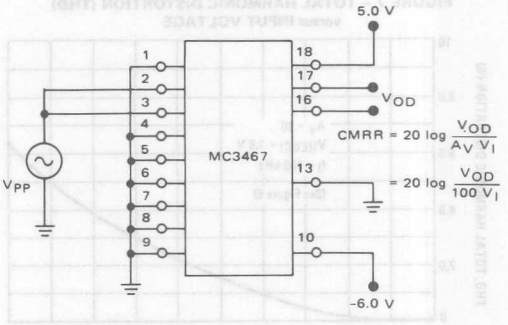


FIGURE 3 – DIFFERENTIAL NOISE VOLTAGE REFERRED TO THE INPUT

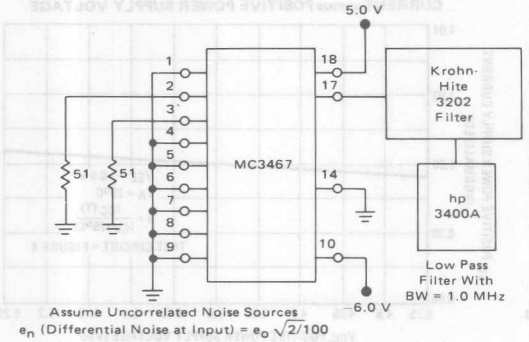


FIGURE 4 – POWER SUPPLY CURRENT TEST CIRCUIT

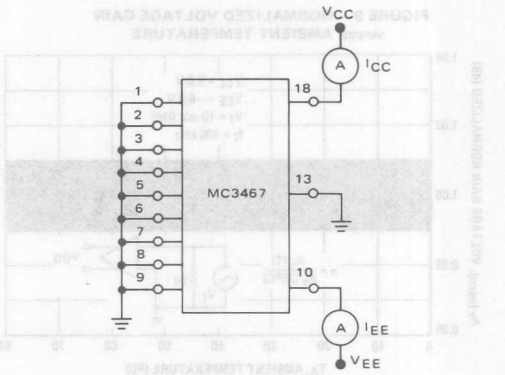


FIGURE 5 – OUTPUT SINK CURRENT TEST CIRCUIT
(Channel A under test, other channels tested similarly)

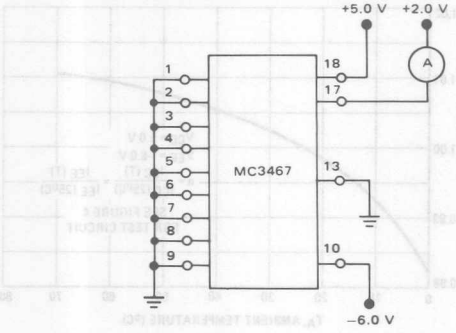
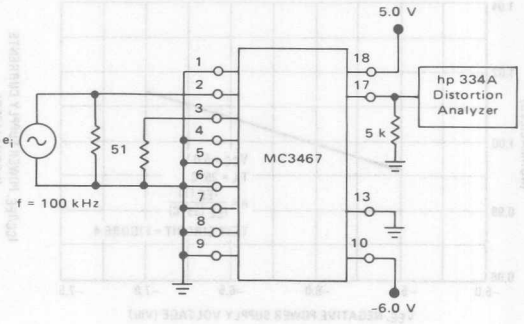


FIGURE 6 – TOTAL HARMONIC DISTORTION TEST CIRCUIT
(Channel A under test, other channels tested similarly)



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TYPICAL CHARACTERISTICS
(V_{CC} = 5.0 V, V_{EE} = -6.0 V, T_A = 25° unless otherwise noted)

FIGURE 7 – TOTAL HARMONIC DISTORTION (THD) versus INPUT VOLTAGE

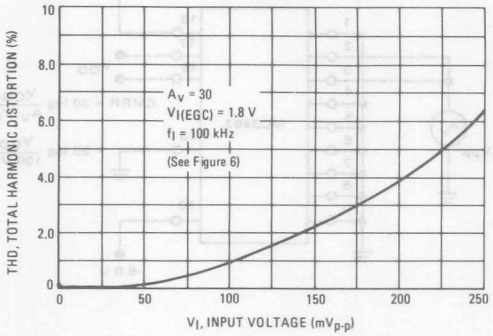


FIGURE 8 – NORMALIZED VOLTAGE GAIN versus FREQUENCY

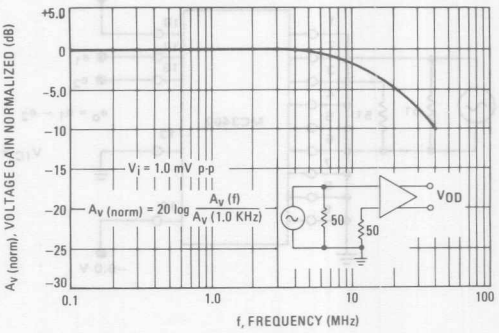


FIGURE 9 – NORMALIZED VOLTAGE GAIN versus AMBIENT TEMPERATURE

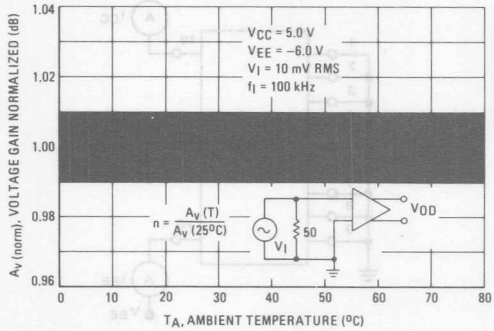


FIGURE 10 – NORMALIZED POSITIVE POWER SUPPLY CURRENT versus POSITIVE POWER SUPPLY VOLTAGE

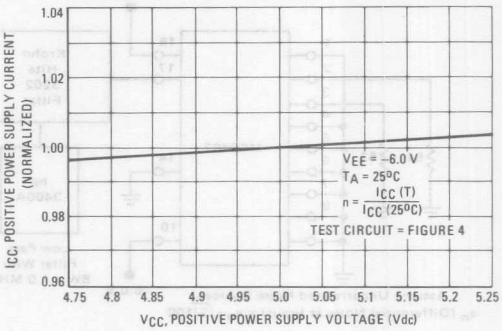


FIGURE 11 – NORMALIZED NEGATIVE POWER SUPPLY CURRENT versus NEGATIVE POWER SUPPLY VOLTAGE

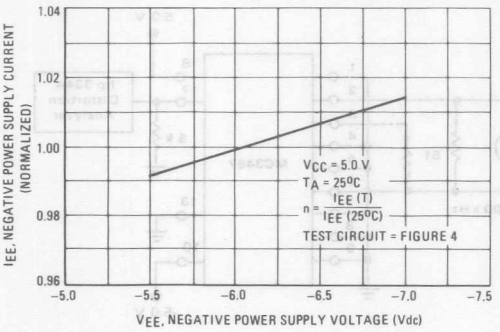
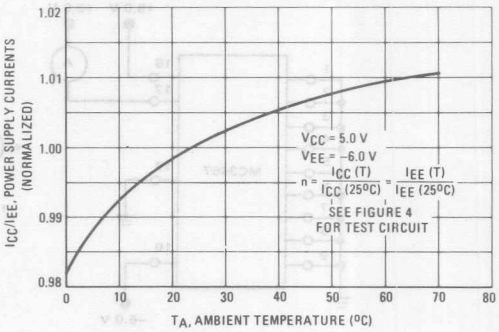


FIGURE 12 – NORMALIZED POWER SUPPLY CURRENTS versus AMBIENT TEMPERATURE



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FIGURE 13 – DIFFERENTIAL VOLTAGE GAIN versus ELECTRONIC GAIN CONTROL VOLTAGE ($V_{I(EGC)}$)

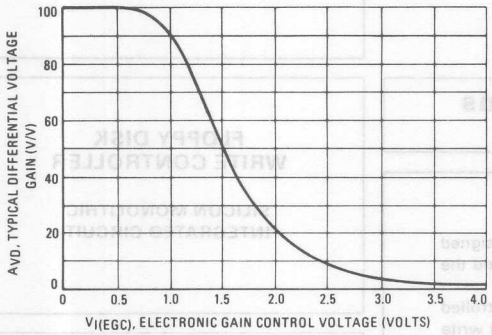


FIGURE 14 – COMMON-MODE REJECTION RATIO (CMRR) versus FREQUENCY

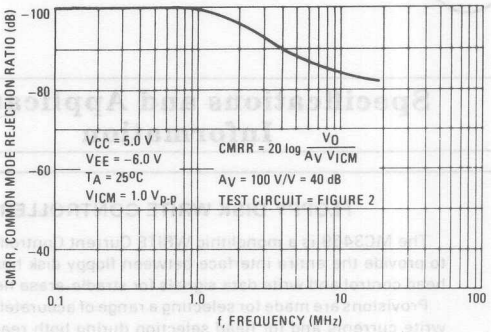


FIGURE 15 – PHASE SHIFT versus FREQUENCY

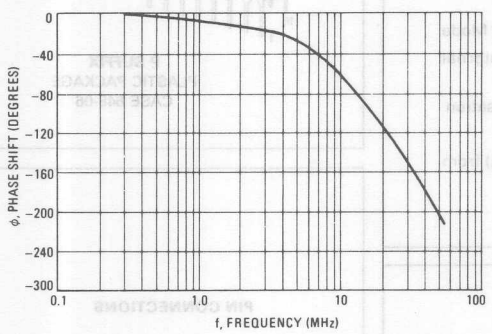
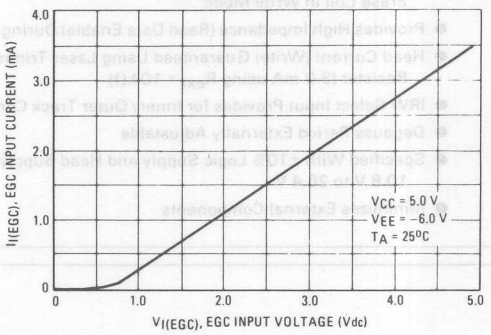
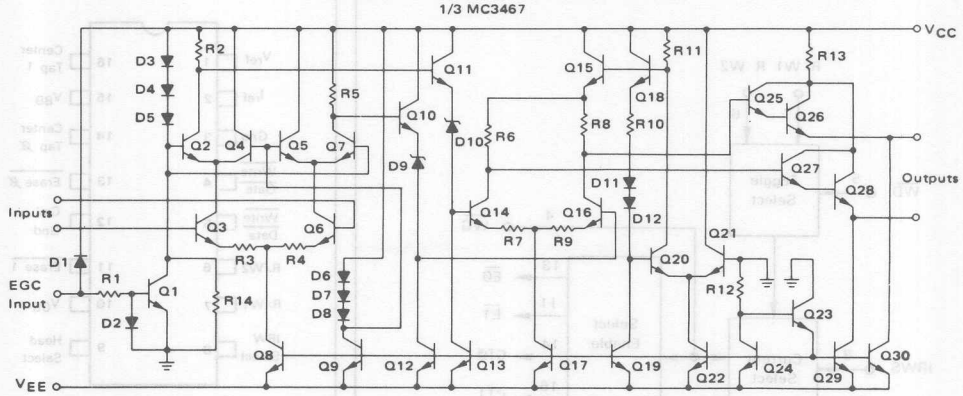


FIGURE 16 – TYPICAL EGC INPUT CURRENT versus EGC INPUT VOLTAGE



REPRESENTATIVE CIRCUIT SCHEMATIC

1/3 MC3467



Specifications and Applications Information

FLOPPY DISK WRITE CONTROLLER

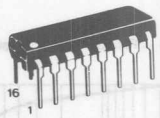
The MC3469 is a monolithic WRITE Current Controller designed to provide the entire interface between floppy disk heads and the head control and write data signals for stradle-erase heads.

Provisions are made for selecting a range of accurately controlled write currents and for head selection during both read and write operation. Additionally, provisions are included for externally adjusting degauss period and inner/outer track compensation.

- Head Selection — Current Steering Through Write Head and Erase Coil in Write Mode
- Provides High Impedance (Read Data Enable) During Read Mode
- Head Current (Write) Guaranteed Using Laser Trimmed Internal Resistor (3.0 mA using R_{ext} = 10 kΩ)
- IRW Select Input Provides for Inner/Outer Track Compensation
- Degauss Period Externally Adjustable
- Specified With ±10% Logic Supply and Head Supply (V_{BB}) from 10.8 V to 26.4 V
- Minimizes External Components

FLOPPY DISK WRITE CONTROLLER

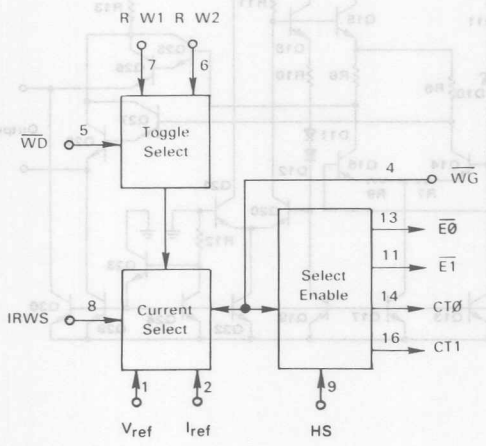
SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 643-06

7

BLOCK DIAGRAM



PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 10)	V_{CC}	7.0	Vdc
Power Supply Voltage (Pin 15)	V_{BB}	30	Vdc
Input Voltage (Pins 4, 5, 8, 9)	V_I	5.75	Vdc
Storage Temperature	T_{stg}	−55 to +150	°C
Operating Junction Temperature	T_J	150	°C

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 10)	V_{CC}	+4.5 to +5.5	Vdc
Power Supply Voltage (Pin 15)	V_{BB}	+10.8 to +26.4	Vdc
Operating Ambient Temperature Range	T_A	0 to +70	°C

ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = 4.5 to 5.5 V, V_{BB} = 10.8 to 26.4 V unless otherwise noted. Typicals given for V_{CC} = 5.0 V, V_{BB} = 12 V and T_A = 25°C unless otherwise noted.)

Characteristics	Pins	Symbol	Min	Typ	Max	Unit
DIGITAL INPUT VOLTAGES						
Power Supply Current — V_{CC}		I_{CC}	—	22	50	mA
V_{BB}		I_{BB}	—	15	30	
High Level Input Voltage (V_{CC} = 4.5 V)	4, 8, 9	V_{IH}	2.0	—	—	V
Low Level Input Voltage (V_{CC} = 5.5 V)	4, 8, 9	V_{IL}	—	—	0.8	V
Input Clamp Voltage (I_{IK} = −12 mA)	4, 5, 8, 9	V_{IK}	—	−0.87	−1.5	V
Positive Threshold (V_{CC} = 5.0)	5	$V_{T(+)}$	1.5	1.75	2.0	V
Negative Threshold (V_{CC} = 5.0)	5	$V_{T(-)}$	0.7	0.98	1.3	V
Hysteresis ($V_{T(+)} - V_{T(-)}$)		V_{HTS}				V
T_A = 0°C to +70°C			0.2	—	—	
T_A = 25°C			0.4	0.76	—	
DIGITAL INPUT CURRENTS						
High Level Input Current (V_{CC} = 5.5 V, V_{BB} = 26.4 V, V_I = 2.4 V)	4, 5, 8, 9	I_{IH}	—	0.1	40	μA
Low Level Input Current (V_{CC} = 5.5 V, V_{BB} = 26.4 V, T_A = 25°C unless noted below)	4, 5, 8, 9	I_{IL}	—	—	−1.6	mA
V_{BB} = 12 V	4		—	0.36	—	
V_{BB} = 24 V	4		—	0.76	—	
V_{CC} = 5.0 V	5		—	0.46	—	
V_{CC} = 5.0 V	8, 9		—	0.39	—	

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ELECTRICAL CHARACTERISTICS (continued) (T_A = 0 to +70°C, V_{CC} = 4.5 to 5.5 V, V_{BB} = 10.8 to 26.4 V unless otherwise noted. Typicals given for V_{CC} = 5.0 V, V_{BB} = 12 V and T_A = 25°C unless otherwise noted.)

Characteristics	Pins	Symbol	Min	Typ	Max	Unit
CENTER-TAP and ERASE OUTPUTS						
Output High Voltage (See Figure 9) (I_{OH} = -100 mA, V_{CC} = 4.5 V) V_{BB} = 10.8 to 26.4 V	14, 16	V_{OH}	V_{BB}-1.5	V_{BB}-1.0	—	V
Output Low Voltage (See Figure 9) (I_{OL} = 1.0 mA) V_{BB} = 12 V V_{BB} = 24 V	14, 16	V_{OL}	— —	70 70	150 150	mV
Output High Leakage (V_{OH} = 24 V, V_{CC} = 4.5 V, V_{BB} = 24 V)	11, 13	I_{OH}	—	0.01	100	μA
Output Low Voltage (See Figure 10) (I_{OL} = 90 mA, V_{CC} = 4.5 V) V_{BB} = 12 V V_{BB} = 24 V	11, 13	V_{OL}	— —	0.27 0.27	0.60 0.60	V
CURRENT SOURCE						
Reference Voltage	1	V_{ref}	—	5.7	—	V
Degauss Voltage (See Text) (Voltage Pin 1 – Voltage Pin 2)	1	V_{DEG}	—	1.0	—	V
Bias Voltage	2	V_F	—	0.7	—	V
Write Current Off Leakage (V_{OH} = 35 V)	6, 7	I_{OH}	—	0.03	15	μA
Saturation Voltage (V_{BB} = 12 V)	6, 7	V_{sat}	—	0.85	2.7	V
Current Sink Compliance (For $V_{6,7}$ = 4.0 V to 24 V, $V_{\overline{WG}}$ = 0.8 V)	6, 7	$\Delta I/RW2, 1$	—	15	40	μA
Average Value Write Current $\left(\frac{(I_{Pin\ 6} + I_{Pin\ 7})}{2}\right.$ for V_{BB} = 10.8 to 26.4 V)	6, 7					
@ $I_{R/W}$ = I_{LOW}, R = 10 k T_A = 25°C T_A = 0 to +70°C @ $I_{R/W}$ = I_{LOW}, R = 5.0 k T_A = 25°C T_A = 0 to +70°C		$\overline{I_{R/W(L)}}$	 2.91 2.84 5.64 5.51	 3.0 — 5.89 —	 3.09 3.16 6.14 6.28	mA
@ $I_{R/W}$ = I_{HI}, R = 10 k (I_{HI} = I_{LOW} + % I_{LOW}) T_A = 25°C T_A = 0 to +70°C		$\Delta\overline{I_{R/W(H)}}$	 31.3 30.3	 33.3 33.3	 35.5 36.6	%
Difference in Write Current ($\lvert I_{Pin\ 6} - I_{Pin\ 7} \rvert$ @ $I_{R/W}$ = I_{LOW}, V_{BB} = 10.8 V to 26.4 V) R = 10 k T_A = 25°C T_A = 0 to +70°C R = 5.0 k T_A = 25°C T_A = 0 to +70°C	6, 7	$I_{R/W\Delta}$	 — — — —	 0.003 — — —	 0.015 0.023 0.030 0.046	mA

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AC SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C, V_{BB} = 24 V, I_{RWS} = 0.4 and $I_{R/W}$ = 3.0 mA unless otherwise noted — refer to Figure 2 and Figure 11.)

Characteristics (Note 1)	f_{in} (Note 3)	Min	Typ	Max	Unit
1. Delay from Head Select going low through 0.8 V to CT0 going high through 20 V.	HS, Pin 9	—	1.6	4.0	μs
2. Delay from Head Select going low through 0.8 V to CT1 going low through 1.0 V.	HS, Pin 9	—	2.1	4.0	μs
3. Delay from Head Select going high through 2.4 V to CT0 going low through 1.0 V.	HS, Pin 9	—	1.7	4.0	μs
4. Delay from Head Select going high through 2.4 V to CT1 going high through 20 V.	HS, Pin 9	—	1.4	4.0	μs
5. Delay from $\overline{WG}$ going low through 0.8 V to CT0 going low through 1.0 V.	$\overline{WG}$, Pin 4	—	1.3	4.0	μs
6. Delay from $\overline{WG}$ going low through 0.8 V to CT1 going high through 20 V.	$\overline{WG}$, Pin 4	—	0.8	4.0	μs
7. Delay from $\overline{WG}$ going low through 0.8 V to CT0 going high through 20 V.	$\overline{WG}$, Pin 4	—	0.75	4.0	μs
8. Delay from $\overline{WG}$ going low through 0.8 V to CT1 going low through 1.0 V.	$\overline{WG}$, Pin 4	—	1.2	4.0	μs
9. After $\overline{WG}$ goes high, delay from R/W1 turning off through 10% to CT0 going high through 20 V.	$\overline{WG}$, Pin 4	20	750	—	ns
10. After $\overline{WG}$ goes high, delay from R/W1 turning off through 10% to CT1 going low through 1.0 V.	$\overline{WG}$, Pin 4	20	1200	—	ns
11. After $\overline{WG}$ goes high, delay from R/W2 turning off through 10% to CT0 going low through 1.0 V.	$\overline{WG}$, Pin 4	20	1200	—	ns
12. After $\overline{WG}$ goes high, delay from R/W2 turning off through 10% to CT1 going high through 20 V.	$\overline{WG}$, Pin 4	20	600	—	ns
13. Delay from $\overline{WG}$ going low through 0.8 V to $\overline{E0}$ going low through 1.0 V.	$\overline{WG}$, Pin 4	—	0.085	4.0	μs
14. Delay from $\overline{WG}$ going low through 0.8 V to $\overline{E1}$ going low through 1.0 V.	$\overline{WG}$, Pin 4	—	0.085	4.0	μs
15. Delay from $\overline{WG}$ going high through 2.0 V to $\overline{E0}$ going high through 23 V.	$\overline{WG}$, Pin 4	—	0.7	4.0	μs
16. Delay from $\overline{WG}$ going high through 2.0 V to $\overline{E1}$ going high through 23 V.	$\overline{WG}$, Pin 4	—	0.7	4.0	μs
17. After $\overline{WG}$ goes low, delay from CT0 going low through 1.0 V to R/W1 turning on through 10%.	$\overline{WG}$, Pin 4	20	750	—	ns
18. After $\overline{WG}$ goes low, delay from CT1 going low through 1.0 V to R/W2 turning on through 10%.	$\overline{WG}$, Pin 4	20	750	—	ns
19. After $\overline{WG}$ goes low, fall time (10% to 90%) of R/W1.	$\overline{WG}$, Pin 4	—	5.0	200	ns
20. After $\overline{WG}$ goes low, fall time (10% to 90%) of R/W2.	$\overline{WG}$, Pin 4	—	5.0	200	ns
21. Setup time, Head Select going low before $\overline{WG}$ going low.	$\overline{WG}$, Pin 4	4.0	—	—	μs
22. $\overline{\text{Write Data}}$ low Hold Time	$\overline{WD}$, Pin 5	200	—	—	ns
23. $\overline{\text{Write Data}}$ high Hold Time	$\overline{WD}$, Pin 5	500	—	—	ns
24. Delay from $\overline{WG}$ going high through 2.0 V to R/W 1 turning off through 10% of on value.	$\overline{WG}$, Pin 4	—	3.9	—	μs

Notes 1. Test numbers refer to encircled numbers in Figure 2.
2. AC test waveforms applied to the designated pins as follows:

Pin	f_{in}	Amplitude	Duty Cycle
HS, Pin 9	50 kHz	0.4 to 2.4 V	50%
$\overline{WG}$, Pin 4	50 kHz	0.4 to 2.4 V	50%
$\overline{WD}$, Pin 5	1.0 MHz	0.2 to 2.4 V	50%

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(V_{CC} = 5.0 V, T_A = 25°C, V_{BB} = 24 V, WG = 0.4 unless otherwise noted — refer to Figure 3 and Figure 11.)

Characteristics (Note 3)	Min	Typ	Max	Unit
1. Delay from $\overline{\text{Write Data}}$ going low through 0.9 V to R/W1 turning on through 50%.	—	85	—	ns
2. Delay skew, difference of R/W1 turning off and R/W2 turning on through 50% after $\overline{\text{Write Data}}$ going low through 0.9 V.	—	1.0	±40	ns
3. Delay from $\overline{\text{Write Data}}$ going low through 0.9 V to R/W1 turning off through 50%.	—	80	—	ns
4. Delay skew, difference of R/W1 turning on and R/W2 turning off 50% after $\overline{\text{Write Data}}$ going low through 0.9 V.	—	1.0	±40	ns
5. Rise time, 10% to 90%, of R/W1	—	1.7	200	ns
6. Rise time, 10% to 90%, of R/W2	—	1.7	200	ns
7. Fall time, 90% to 10%, of R/W1	—	12	200	ns
8. Fall time, 90% to 10%, of R/W2	—	12	200	ns

Note 3. Test numbers refer to encircled numbers in Figure 4.
f_{in} = 1.0 MHz, 50% Duty Cycle and Amplitude of 0.2 V to 2.4 V.

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PIN DESCRIPTION TABLE

Name	Symbol	Pin	Description
Head Select	HS	9	Head Select input selects between the head I/O pins: center-tap, erase, and read/write. A HIGH selects Head 0 and a LOW selects Head 1.
$\overline{\text{Write Gate}}$	$\overline{\text{WG}}$	4	$\overline{\text{Write Gate}}$ input selects the mode of operation. HIGH selects the read mode, while LOW selects the Write Control mode and forces the write current.
$\overline{\text{Write Data}}$	$\overline{\text{WD}}$	5	$\overline{\text{Write Data}}$ input controls the turn on/off of the write current. The internal divide-by-two flip-flop toggles on the negative going edge of this input to direct the current alternately to the two halves of the head coils.
IRW Select	IRWS	8	IRW Select input selects the amount of write current to be used. When LOW, the current equals the value found in Figure 5, according to the external resistor. When HIGH, the current equals the low current + 33%.
V_{ref} I_{ref}	V_{ref} I_{ref}	1 2	A resistor between these pins sets the write current. Laser trimming reliably produces 3 mA of current for a 10 k resistor. A capacitor from V_{ref} to Gnd will adjust the Degauss period.
Center-tap 0	CT0	14	Center-tap 0 output is connected to the center tap of Head 0. It will be pulled to Gnd or V_{BB} (+12 or +24) depending on mode and head selection.
$\overline{\text{Erase 0}}$	$\overline{\text{E0}}$	13	$\overline{\text{Erase 0}}$ will be LOW for writing on Head 0, and floating for other conditions.
Center-tap 1	CT1	16	Center-tap 1 output is connected to the center tap of Head 1. It will be pulled to Gnd or V_{BB} (+12 or +24) depending on mode and head selection.
$\overline{\text{Erase 1}}$	$\overline{\text{E1}}$	11	$\overline{\text{Erase 1}}$ will be LOW for writing on Head 1, and floating for other conditions.
R/W2	R/W2	6	R/W2 input is one of the differential inputs that sinks current during writing, being the opposite phase of R/W1. It will be connected to one side of the heads.
R/W1	R/W1	7	R/W1 input is one of the differential inputs that sinks current during writing, being the opposite phase of R/W2. It will be connected to one side of the heads.
	V_{CC}	10	+5 V Power
	V_{BB}	15	+12 V or + 24 V Power
	Gnd	12	Coil grounds
	Gnd	3	Reference and logic ground

FIGURE 1 — LOGIC DIAGRAM

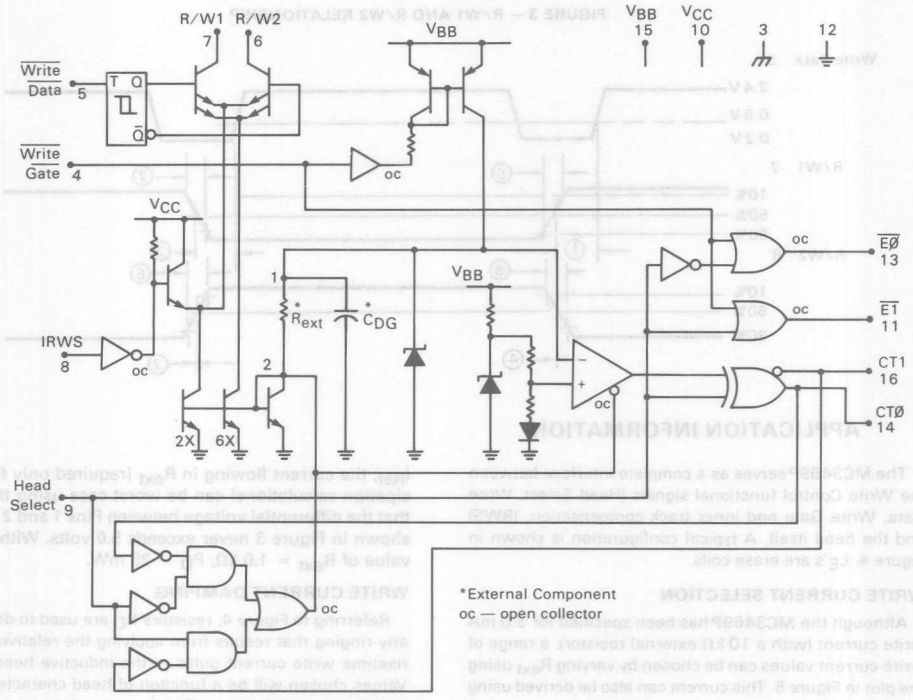
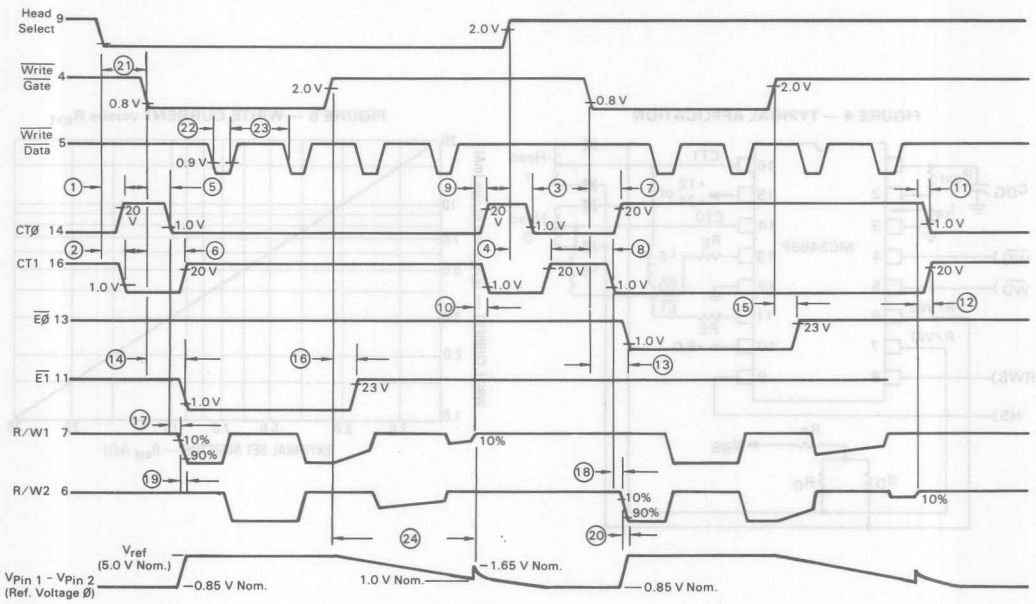
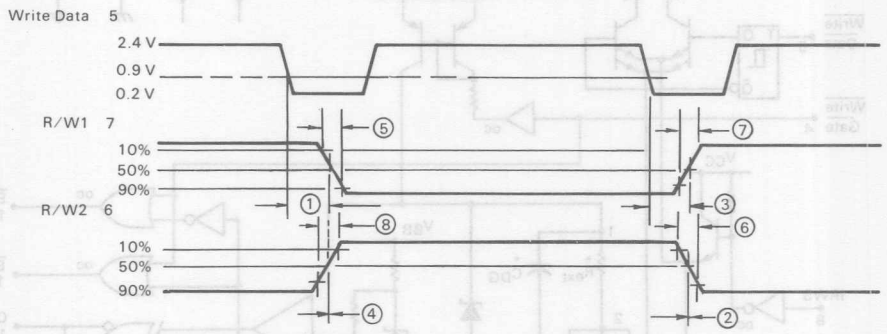


FIGURE 2 — AC TIMING DIAGRAM



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FIGURE 3 — R/W1 AND R/W2 RELATIONSHIP



APPLICATION INFORMATION

The MC3469P serves as a complete interface between the Write Control functional signals (Head Select, Write Data, Write Gate and inner track compensation, IRWS) and the head itself. A typical configuration is shown in Figure 4. L_E's are erase coils.

WRITE CURRENT SELECTION

Although the MC3469P has been specified for 3.0 mA write current (with a 10 kΩ external resistor), a range of write current values can be chosen by varying R_{ext} using the plot in Figure 5. This current can also be derived using the relationship $I_{Write}\,(mA) = \frac{30}{R_{ext}(k\Omega)}$

I_{Ref}, the current flowing in R_{ext} (required only for dissipation calculations) can be worst case using the fact that the differential voltage between Pins 1 and 2 (V_{Ref}) shown in Figure 3 never exceeds 5.0 volts. With a low value of R_{ext} = 1.0 kΩ, P_D = 25 mW.

WRITE CURRENT DAMPING

Referring to Figure 4, resistors R_D are used to dampen any ringing that results from applying the relatively fast risetime write current pulse to the inductive head load. Values chosen will be a funciton of head characteristics and the desired damping. R_P serves as a common pullup resistor to the head supply V_{BB}.

FIGURE 4 — TYPICAL APPLICATION

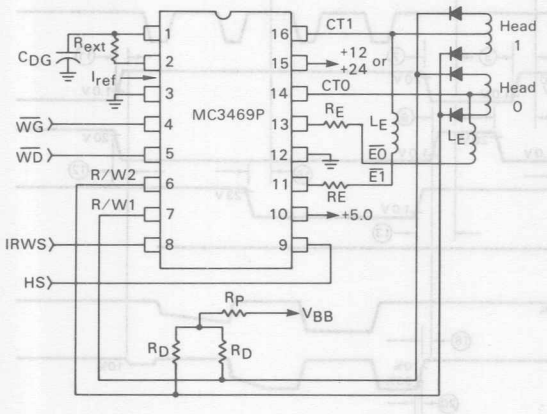
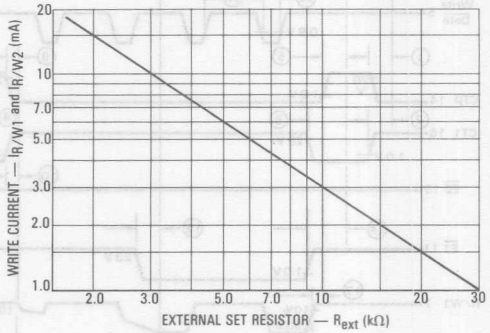


FIGURE 5 — WRITE CURRENT versus R_{ext}



DEGAUSS PERIOD

Degauss of the read/write head can be accomplished at the end of each write operation by attaching a capacitor from pin 1 to ground. The timing relationship that results is shown in Figure 7. A simplified diagram of this function is shown in Figure 6.

While $\overline{WG}$ is low, the selected write current flows into pin 6 or pin 7 (R/W1 or R/W2) and is mirrored through the external resistor, R_{ext}. The degauss capacitor, C_{DG}, will be charged to approximately 5.7 volts. After $\overline{WG}$ goes high, the voltage on C_{DG} begins to decay toward 0.7 V. When the voltage reaches the comparator threshold of 1.7 V, the comparator output triggers the internal logic to completely turn off the write current. At this point, the pulse amplitude on the R/W1 and R/W2 pins has returned to 10% of its maximum value.

Figure 7, Degauss Period shows the relationship between C_{DG} and Degauss Period for R_{ext} = 10 kΩ. This period is equal to the exponential delay time for the voltage as mentioned plus some internal delay times.

POWER-UP WRITE CURRENT CONTROL

During power-up, under certain conditions (V_{BB} comes up first while $\overline{WG}$ is low), there can be a write current transient on Pins 6 and 7 (R/W1 and R/W2) of sufficient magnitude to cause writing to occur if the head is loaded.

This transient can be eliminated by placing a capacitor from Pin 2 to ground. This also delays the write current when $\overline{WG}$ goes low and this delay must be accounted for when the capacitor on Pin 2 is used. The delay is 3.0 μs for a 2700 pF capacitor, and R_{ext} = 10 kΩ. Values up to 7000 pF may be used.

FIGURE 6 — SIMPLIFIED DEGAUSS CIRCUIT

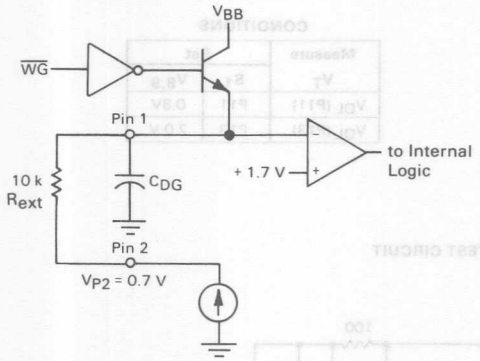


FIGURE 7 — DEGAUSS PERIOD versus CAPACITANCE (C_{DG})

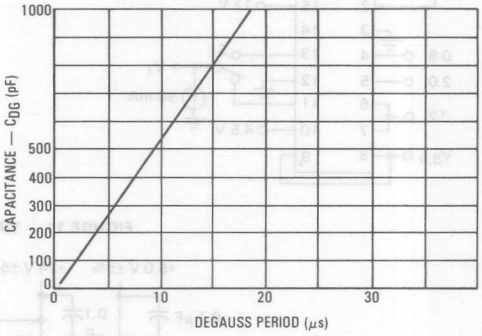
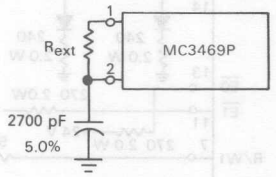


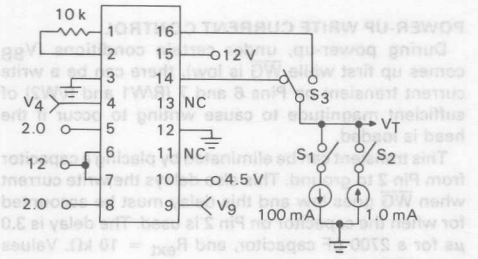
FIGURE 8 — TURN-ON WRITE PROTECTION



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TEST FIGURES

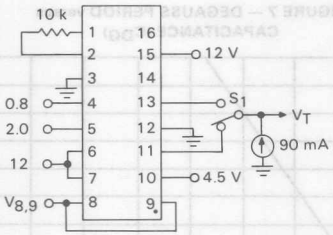
FIGURE 9 — CENTER TAP OUTPUT VOLTAGE (PINS 14 AND 16)



Measure V_T	CONDITIONS Set S_1	S_2	S_3	V_4*	V_9*
V_{OH} (P14)	On	Off	P14	0.8	2.0
				2.0	0.8
V_{OH} (P16)	On	Off	P16	2.0	2.0
				0.8	0.8
V_{OL} (P14)	Off	On	P14	0.8	0.8
				2.0	2.0
V_{OL} (P16)	Off	On	P16	2.0	0.8
				0.8	2.0

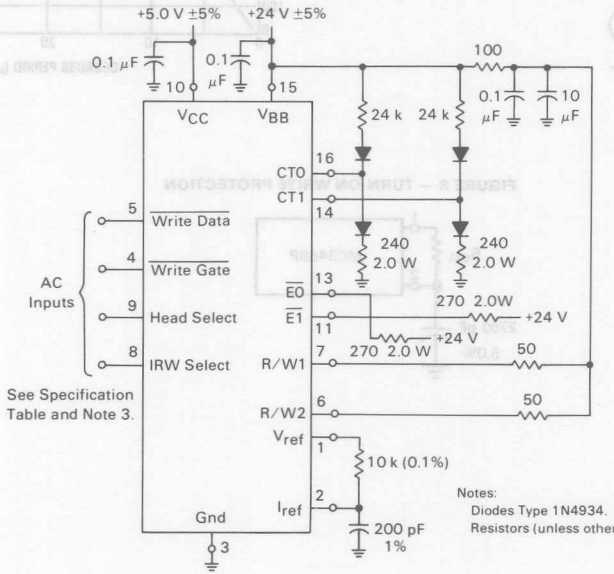
*Volts

FIGURE 10 — ERASE OUTPUT LOW VOLTAGE (PINS 11 AND 13)



Measure V_T	CONDITIONS Set S_1	$V_{8,9}$
V_{OL} (P11)	P11	0.8V
V_{OL} (P13)	P13	2.0 V

FIGURE 11 — TIMING TEST CIRCUIT



Notes:
Diodes Type 1N4934.
Resistors (unless otherwise noted) are 1/4 W, 5%.

ERASE CURRENT

The value of R_E, the erase current set resistor, is found by referring to Figure 12 and selecting the desired erase current.

Looking at the simplified erase current path in Figure 12, when writing, CT0 will be high ($V_{OH(min)}$ = 21 V) and E0 will be low ($V_{OL(max)}$ = 0.6 V). If the erase coil resistance is 10 Ω and 40 mA of erase current is desired, then:

$$(R_E + 10\ \Omega) \times 40\ mA = (21 - 0.6)\ V$$

or

$$R_E = \frac{20.4\ V}{0.04\ A} = 10\ \Omega = 500\ \Omega$$

$$P_D = (0.04)(20.4) = 0.816\ W \text{ or } 1.0\ W$$

This gives the minimum value R_E for worst case V_{OH}/V_{OL} conditions. It is also recommended that a diode be used as required for inductive back emf suppression.

Erase timing is provided internally and is active during Write Gate low for the selected head.

FIGURE 12 — ERASE CURRENT (R_E Selection)

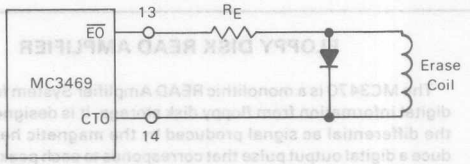
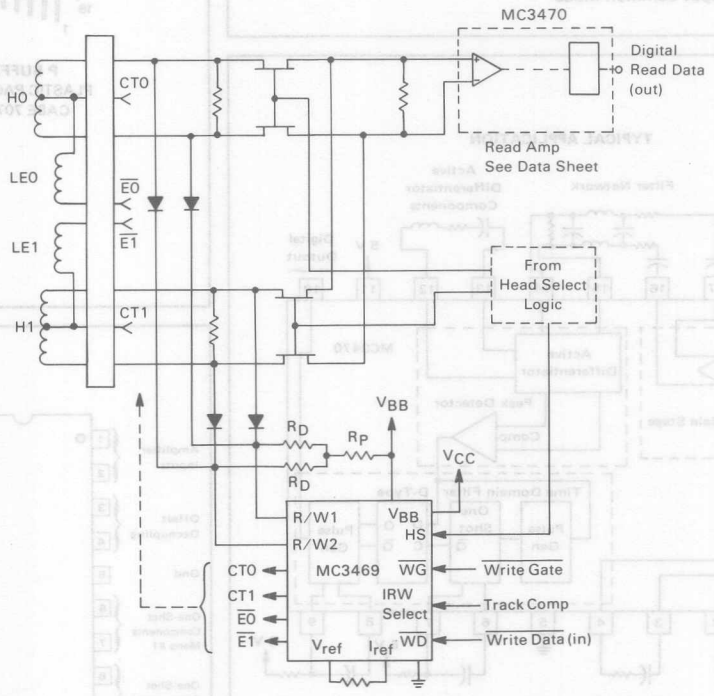


FIGURE 13 — TYPICAL DUAL HEAD FLOPPY DISK SYSTEM USING FET GATE READ CHANNEL SELECTION AND MC3469/MC3470



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MOTOROLA

MC3470P
MC3470AP

Specifications and Applications Information

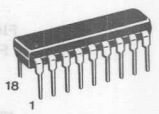
FLOPPY DISK READ AMPLIFIER SYSTEM

SILICON MONOLITHIC INTEGRATED CIRCUIT

FLOPPY DISK READ AMPLIFIER

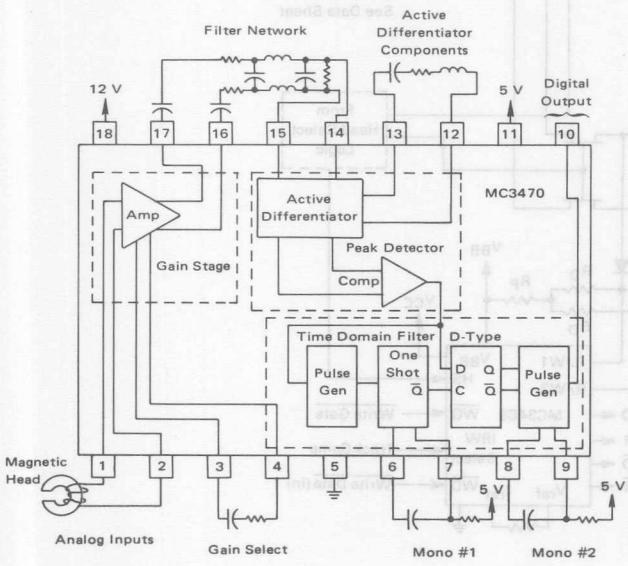
The MC3470 is a monolithic READ Amplifier System for obtaining digital information from floppy disk storage. It is designed to accept the differential ac signal produced by the magnetic head and produce a digital output pulse that corresponds to each peak of the input signal. The gain stage amplifies the input waveform and applies it to an external filter network, enabling the active differentiator and time domain filter to produce the desired output.

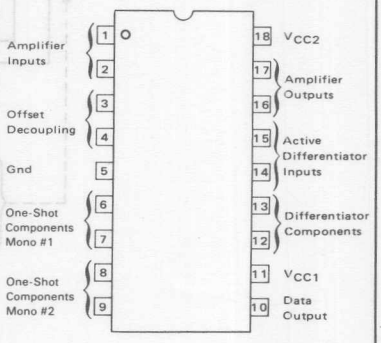
- Combines All the Active Circuitry To Perform the Floppy Disk Read Amplifier Function in One Circuit
- Guaranteed Maximum Peak Shift of 2.0% — MC3470A
- Improved (Positive) Gain T_C and Tolerance
- Improved Input Common Mode



P SUFFIX
PLASTIC PACKAGE
CASE 707-02

TYPICAL APPLICATION





7

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 11)	V_{CC1}	7.0	Vdc
Power Supply Voltage (Pin 18)	V_{CC2}	16	Vdc
Input Voltage (Pins 1 and 2)	V_I	−0.2 to +7.0	Vdc
Output Voltage (Pin 10)	V_O	−0.2 to +7.0	Vdc
Operating Ambient Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−65 to +150	°C
Operating Junction Temperature Plastic Package	T_J	150	°C

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	V_{CC1} + 4.75 to +5.25 V_{CC2} +10 to +14	Vdc
Operating Ambient Temperature Range	T_A	0 to +70	°C

ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C, V_{CC1} = 4.75 to 5.25 V, V_{CC2} = 10 to 14 V unless otherwise noted)

Characteristic		Figure	Symbol	Min	Typ	Max	Unit
Differential Voltage Gain (f = 200 kHz, V_{iD} = 5.0 mV(RMS)	MC3470	2	A_{VD}	80	100	130	V/V
	MC3470A			100	110	130	
Input Bias Current		3	I_{IB}	—	−10	−25	μA
Input Common Mode Range Linear Operation (5% max THD)			v_{iCM}	−0.1	—	1.5	V
Differential Input Voltage Linear Operation (5% max THD)			v_{iD}	—	—	25	mVp-p
Output Voltage Swing Differential		2	v_{oD}	3.0	4.0	—	Vp-p
Output Source Current, Toggled			I_O	—	8.0	—	mA
Output Sink Current, Pins 16 and 17		4	I_{OS}	2.8	4.0	—	mA
Small Signal Input Resistance (T_A = 25°C)			r_i	100	250	—	kΩ
Small Signal Output Resistance, Single-Ended (T_A = 25°C, V_{CC1} = 5.0 V, V_{CC2} = 12 V)			r_o	—	15	—	Ω
Bandwidth, −3.0 dB (v_{iD} = 2.0 mV(RMS), T_A = 25°C V_{CC1} = 5.0 V, V_{CC2} = 12 V)		2, 17	BW	10	—	—	MHz
Common Mode Rejection Ratio (T_A = 25°C, f = 100 kHz, A_{VD} = 40 dB, v_{in} = 200 mVp-p, V_{CC1} = 5.0 V, V_{CC2} = 12 V)		5	CMRR	50	—	—	dB
V_{CC1} Supply Rejection Ratio (T_A = 25°C, V_{CC2} = 12 V, 4.75 ≤ V_{CC1} ≤ 5.25 V, A_{VD} = 40 dB)			—	50	—	—	dB
V_{CC2} Supply Rejection Ratio (T_A = 25°C, V_{CC1} = 5.0 V, 10 V ≤ V_{CC2} ≤ 14 V, A_{VD} = 40 dB)			—	60	—	—	dB
Differential Output Offset (T_A = 25°C, v_{iD} = v_{in} = 0 V)			V_{DO}	—	—	0.4	V
Common Mode Output Offset (v_{iD} = V_{in} = 0 V, Differential and Common Mode)			V_{CO}	—	3.0	—	V
Differential Noise Voltage Referred to Input (BW = 10 Hz to 1.0 MHz, T_A = 25°C)		22	e_n	—	15	—	μV(RMS)
Supply Currents (V_{CC1} = 5.25 V, S_1 to Pin 12 or Pin 13) (V_{CC2} = 14 V)		1	I_{CC1} I_{CC2}	— —	40 4.8	— —	mA

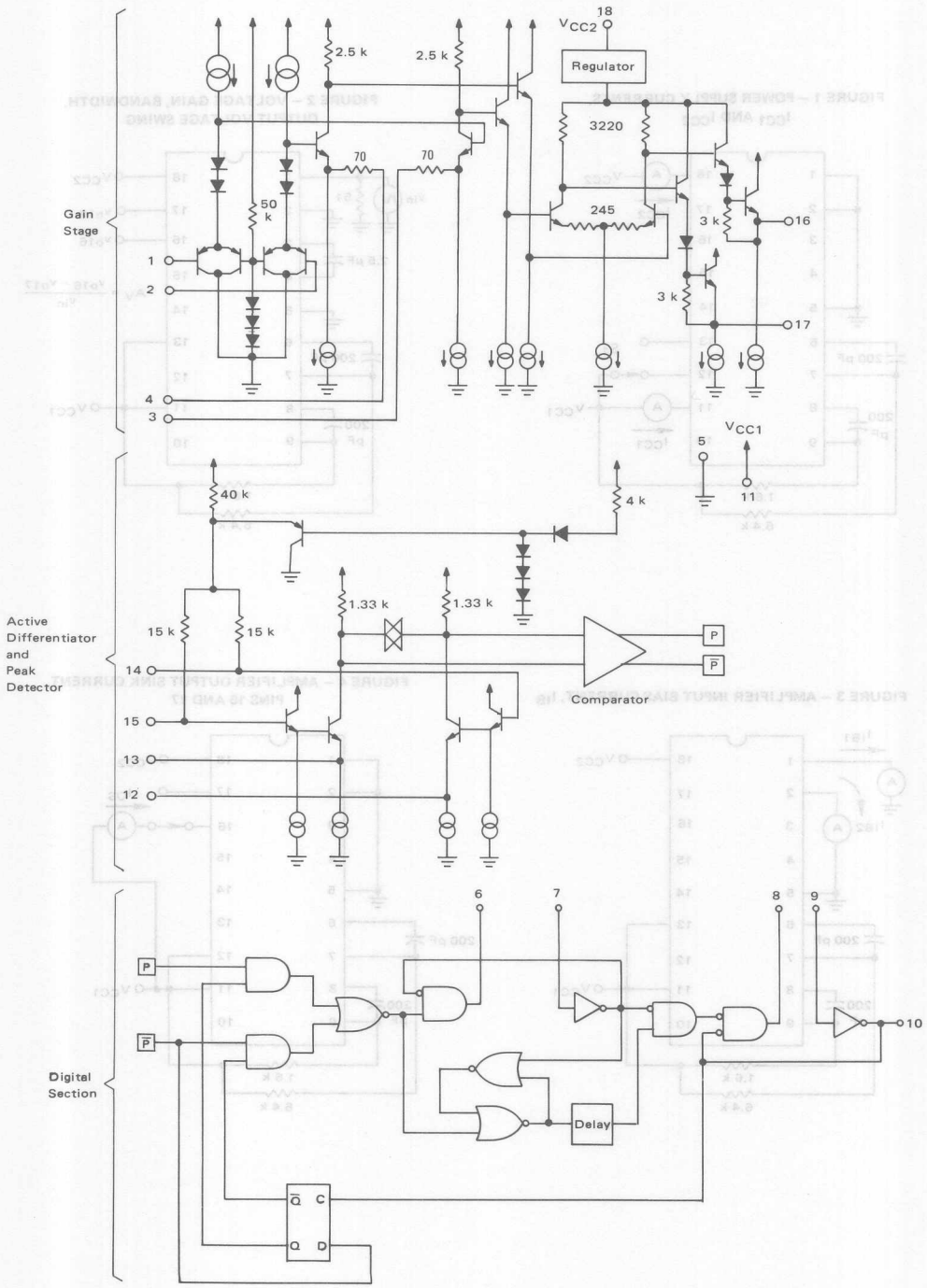
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ELECTRICAL CHARACTERISTICS (continued) (T_A = 0 to +70°C, V_{CC1} = 4.75 to 5.25 V, V_{CC2} = 10 to 14 V unless otherwise noted)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
ACTIVE DIFFERENTIATOR SECTION						
Differentiator Output Sink Current, Pins 12 and 13 (V_{OD} = V_{CC1})	6	I_{OD}	1.0	1.4	—	mA
Peak Shift (f = 250 kHz, v_{iD} = 1.0 Vp-p, i_{cap} = 500 μA, where PS = $1/2 \frac{t_{PS1}-t_{PS2}}{t_{PS1}+t_{PS2}} \times 100\%$, V_{CC1} = 5.0 V, V_{CC2} = 12 V) MC3470	7, 8	PS	—	—	5.0	%
MC3470A			—	—	2.0	
Differentiator Input Resistance, Differential		r_{iD}	—	30	—	kΩ
Differentiator Output Resistance, Differential (T_A = 25°C)		r_{oD}	—	40	—	Ω
DIGITAL SECTION						
Output Voltage High Logic Level, Pin 10 (V_{CC1} = 4.75 V, V_{CC2} = 12 V, I_{OH} = −0.4 mA)	9	V_{OH}	2.7	—	—	V
Output Voltage Low Logic Level, Pin 10 (V_{CC1} = 4.75 V, V_{CC2} = 12 V, I_{OL} = 8.0 mA)	10	V_{OL}	—	—	0.5	V
Output Rise Time, Pin 10	11, 12	t_{TLH}	—	—	20	ns
Output Fall Time, Pin 10	11, 12	t_{THL}	—	—	25	ns
Timing Range Mono #1 (t_{1A} and t_{1B})	13	$t_{1A, B}$	500	—	4000	ns
Timing Accuracy Mono #1 (t1 = 1.0 μs = 0.625 R1C1 + 200 ns) (R1 = 6.4 kΩ, C1 = 200 pF) Accuracy guaranteed for R1 in the range 1.5 kΩ ≤ R1 ≤ 10 kΩ and C1 in the range 150 pF ≤ C1 ≤ 680 pF. Note: To minimize current transients, C1 should be kept as small as is convenient.	12, 13	E_{t1}	85	—	115	%
Timing Range Mono #2	11, 12	t2	150	—	1000	ns
Timing Accuracy Mono #2 (t2 = 200 ns = 0.625 R2C2) (R2 = 1.6 kΩ, C2 = 200 pF) Accuracy guaranteed for 1.5 kΩ ≤ R2 ≤ 10 kΩ, 100 pF ≤ C2 ≤ 800 pF	12, 13	E_{t2}	85	—	115	%

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MC3470 CIRCUIT SCHEMATIC



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FIGURE 1 – POWER SUPPLY CURRENTS, I_{CC1} AND I_{CC2}

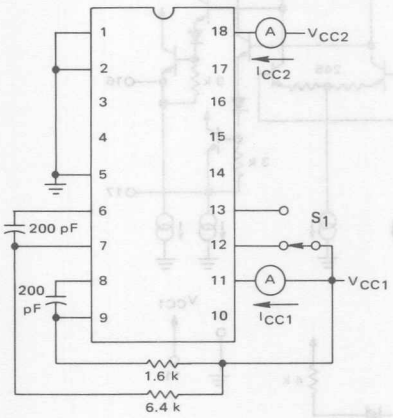


FIGURE 2 – VOLTAGE GAIN, BANDWIDTH, OUTPUT VOLTAGE SWING

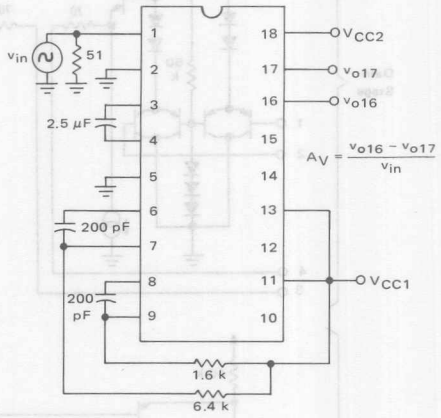


FIGURE 3 – AMPLIFIER INPUT BIAS CURRENT, I_{IB}

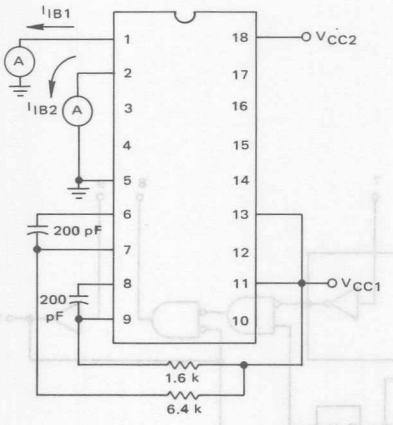
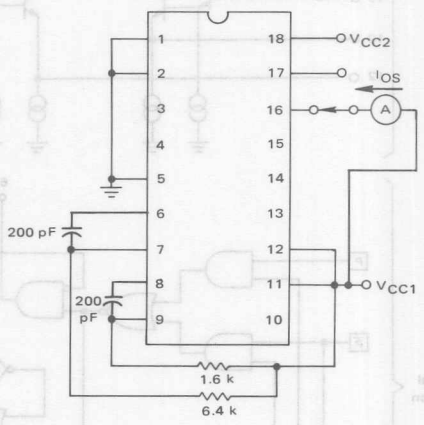
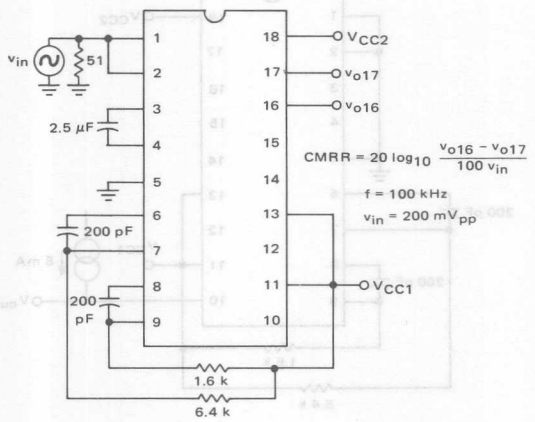


FIGURE 4 – AMPLIFIER OUTPUT SINK CURRENT, PINS 16 AND 17



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FIGURE 5 – AMPLIFIER COMMON MODE REJECTION RATIO, CMRR



NOTE: Measurements may be made with vector voltmeter hp 8405A or equivalent at 1.0 MHz to guarantee 100 kHz performance.

FIGURE 6 – DIFFERENTIATOR OUTPUT SINK CURRENT, PINS 12 AND 13

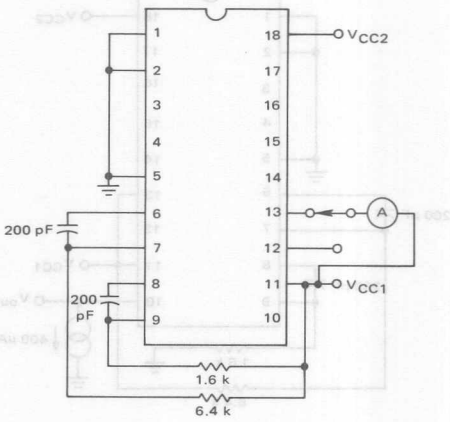


FIGURE 7 – PEAK SHIFT, PS

See Figure 8 for Output Waveform

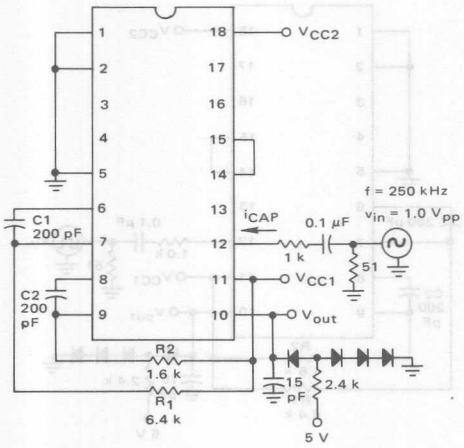
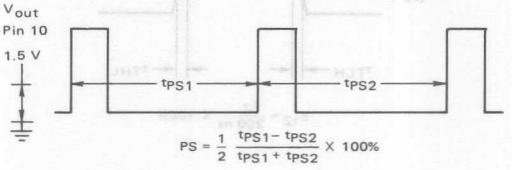


FIGURE 8 – PEAK SHIFT, PS

V_{in} = 1.0 V_{pp} f = 250 kHz

Test schematic on Figure 7



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FIGURE 9 – DATA OUTPUT VOLTAGE HIGH, PIN 10

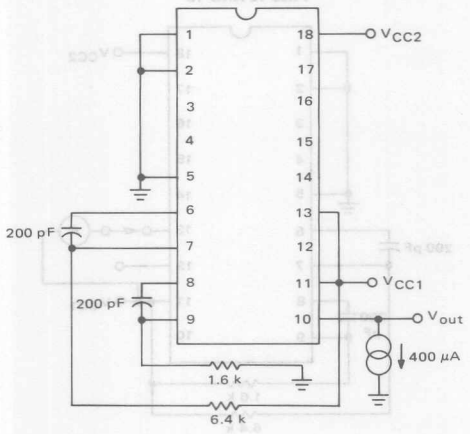
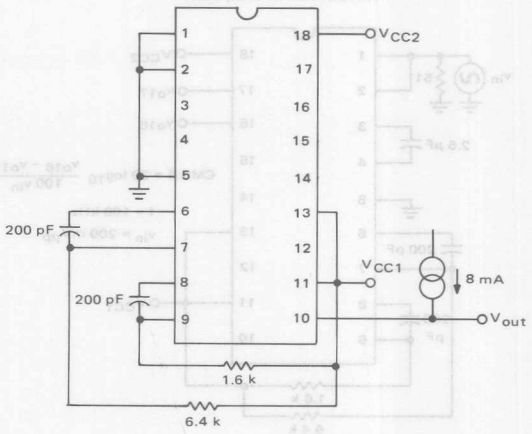


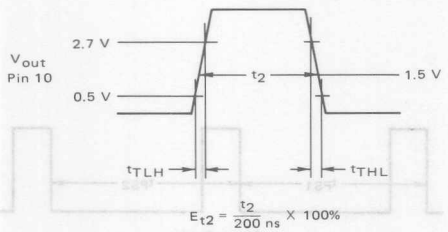
FIGURE 10 – DATA OUTPUT VOLTAGE LOW, PIN 10



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FIGURE 11 – DATA OUTPUT RISE TIME, t_{TLH}
DATA OUTPUT FALL TIME, t_{THL}
TIMING ACCURACY MONO #2, E_{t2}

V_{in} is same as shown on Figure 13, test schematic on Figure 12



$$E_{t2} = \frac{t_2}{200\ ns} \times 100\%$$

FIGURE 12 – TIMING ACCURACY, E_{t1} AND E_{t2}
DATA OUTPUT RISE AND FALL TIMES, t_{TLH} AND t_{THL}

V_{in} shown on Figure 13

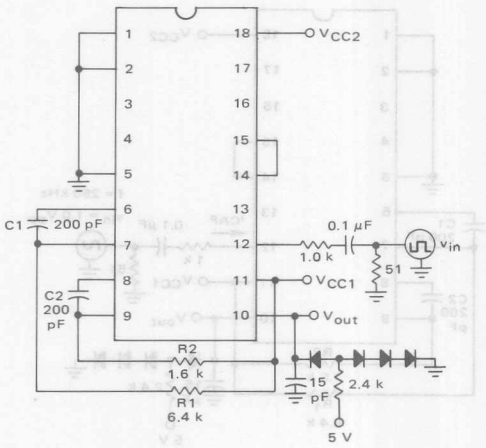
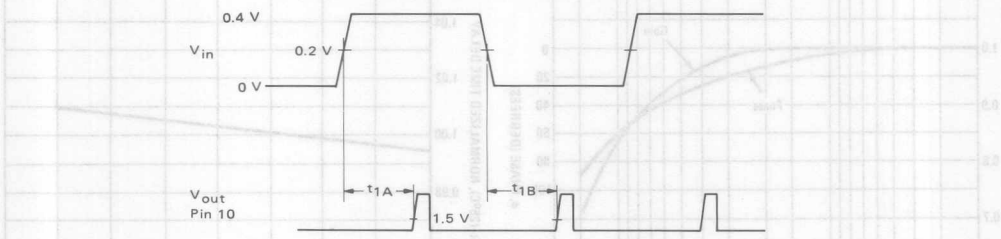


FIGURE 13 – TIMING ACCURACY MONO #1, E_{t1}

$t_{TLH} = t_{THL} < 10$ ns f = 250 kHz 50% Duty Cycle

Test Schematic on Figure 12

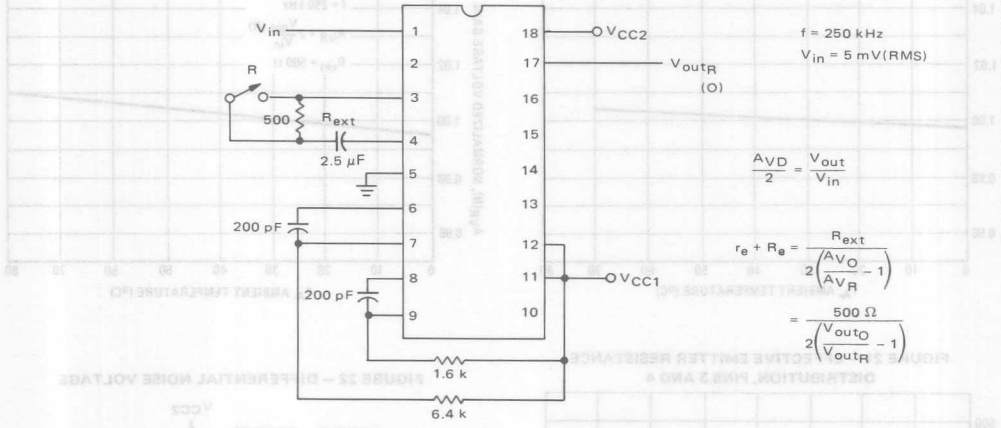


$$E_{t1A} = \frac{t_{1A}}{1000\ ns} \times 100\%$$

$$E_{t1B} = \frac{t_{1B}}{1000\ ns} \times 100\%$$

FIGURE 14 – AMPLIFIER OFFSET DECOUPLING IMPEDANCE, PINS 3 AND 4

$R_e + r_e$ and A_V with $R_{ext} = 500\ \Omega$



f = 250 kHz

V_{in} = 5 mV(RMS)

$$\frac{A_{VD}}{2} = \frac{V_{out}}{V_{in}}$$

$$r_e + R_e = \frac{R_{ext}}{2\left(\frac{A_{V_O}}{A_{V_R}} - 1\right)} = \frac{500\ \Omega}{2\left(\frac{V_{out_O}}{V_{out_R}} - 1\right)}$$

FIGURE 15 – NORMALIZED POWER SUPPLY CURRENT (I_{CC}/I_{CC} 25°C) versus TEMPERATURE

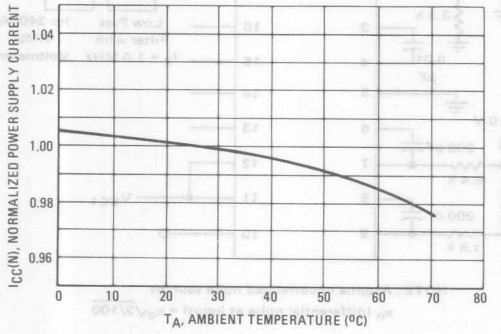
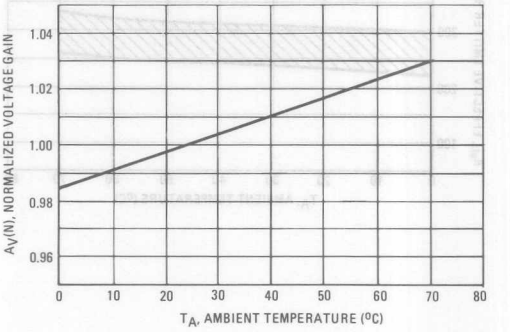


FIGURE 16 – NORMALIZED VOLTAGE GAIN (A_V/A_V 25°C) versus TEMPERATURE



7

FIGURE 17 – PHASE AND NORMALIZED VOLTAGE GAIN versus FREQUENCY

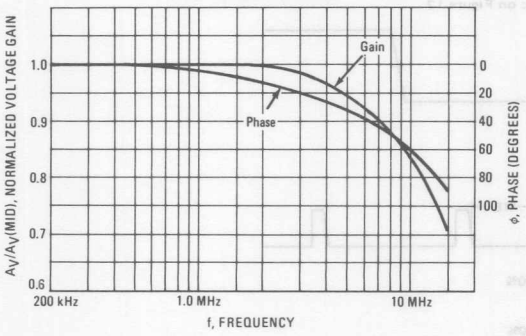


FIGURE 18 – NORMALIZED TIME DELAY t_1 versus TEMPERATURE

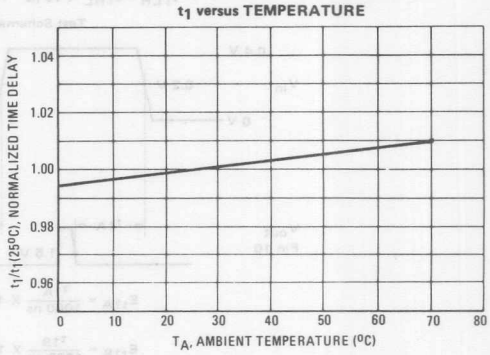


FIGURE 19 – NORMALIZED OUTPUT PULSE WIDTH, t_2/t_2 25°C

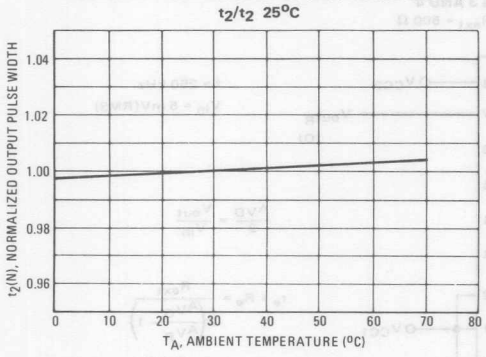


FIGURE 20 – NORMALIZED VOLTAGE GAIN, A_{VR}/A_{VR} 25°C

See Figure 14, Switch Position R

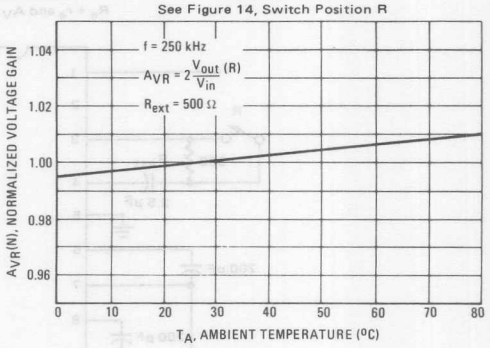


FIGURE 21 – EFFECTIVE EMITTER RESISTANCE DISTRIBUTION, PINS 3 AND 4

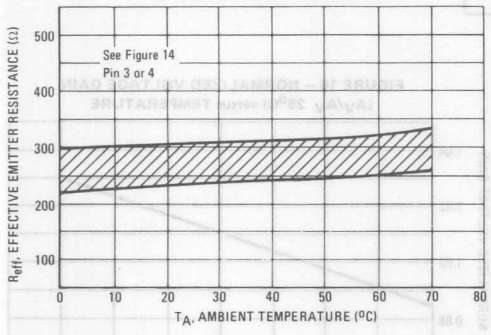
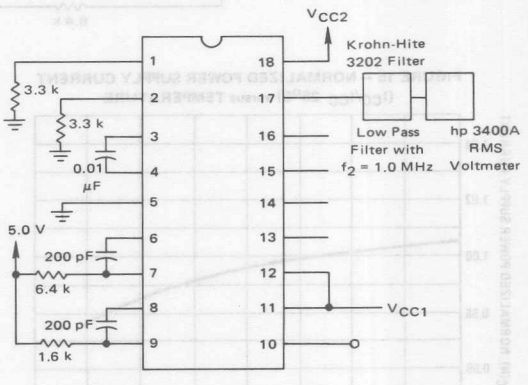


FIGURE 22 – DIFFERENTIAL NOISE VOLTAGE



NOTE: Assume uncorrelated noise sources

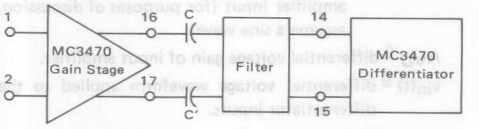
e_n (differential noise at input) = $e_o\sqrt{2/100}$

7

APPLICATION INFORMATION

The MC3470 is designed to accept a differential ac input from the magnetic head of a floppy disk drive and produce a digital output pulse that corresponds to each peak of the ac input. The gain stage amplifies the input waveform and applies it to a filter network (Figure 23a),

FIGURE 23a – BLOCKING CAPACITORS USED TO ISOLATE THE DIFFERENTIATOR



enabling the active differentiator and time domain filter to produce the desired output.

FILTER CONSIDERATIONS

The filter is used to reduce any high frequency noise present on the desired signal. Its characteristics are dictated by the floppy disk system parameters as well as the coupling requirements of the MC3470. The filter design parameters are affected by the read head characteristics, maximum and minimum slew rates, system transient response, system delay distortion, filter center frequency, and other system parameters. This design criteria varies between manufacturers; consequently, the filter configuration also varies. The coupling requirements of the MC3470 are a result of the output structure of the gain stage and the input structure of the differentiator, and must be adhered to regardless of the filter configuration.

The differentiator has an internal biasing network on each input. Therefore, any dc voltage applied to these inputs will perturbate the bias level. Disturbing the bias level does not affect the waveform at the differentiator inputs, but it does cause peak shifting in the digital output (Pin 10). Since the output of the gain stage has an associated dc voltage level, it, as well as any biasing introduced in the filter, must be isolated from the differentiator via series blocking capacitors. The transient response is minimized if the blocking capacitors C and C' are placed before the filter as shown in Figure 23a. The charging and discharging of C and C' is controlled by the filter termination resistor instead of the high input impedance of the differentiator.

The filter design must also include the current-sinking capacity of the amplifier output. The current source in the output structure (see circuit schematic – Pins 16 and 17) is guaranteed to sink a current of 2.8 mA. If the current requirement of the filter exceeds 2.8 mA, the current source will saturate, the output waveform will be distorted, and inaccurate peak detection will occur in the differentiator. Therefore, the total impedance of the filter must be greater than Z_{min} as calculated from

$$Z_{min} = \frac{(E_p A_{VD})\ max}{2.8\ mA}$$

where E_p is the peak differential input voltage to the MC3470.

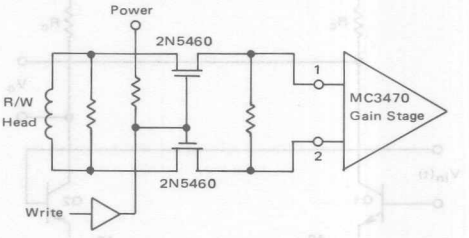
See Application Note AN917 for further information.

TRANSIENT RESPONSE

The worst-case transient response of the read channel occurs when dc switching at the amplifier input causes its output to be toggled. The dc voltage changes are a consequence of diode switching that takes place when control is transferred from the write channel to the read channel.

If the diode network is balanced, the dc change is a common mode input voltage to the amplifier. The switching of an unbalanced diode network creates a differential input voltage and a corresponding amplified swing in the outputs. The output swing will charge the blocking capacitor resulting in peak shifting in the digital output until the transient has decayed. Eliminating the differential dc changes at the amplifier input by matching the diode network or by coupling the read head to the amplifier via FET switches, as shown in Figure 23b, will minimize the filter transient response.

FIGURE 23b – FET SWITCHES USED TO COUPLE THE R/W HEAD TO THE MC3470



Two of the advantages FET switches have over diode switching are:

1. They isolate the read channel from dc voltage changes in the system; therefore, the transient response of the filter does not influence the system transient response.
2. The low voltage drop across the FETs keeps the input signal below the amplifier's internal clamp voltage; whereas, the voltage dropped across a diode switching network adds a dc bias to the input signal which may exceed the clamp voltage.

AMPLIFIER GAIN

For some floppy systems, it may become necessary to either reduce the gain of the amplifier or reduce the

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signal at the input to avoid exceeding the output swing capability of the amplifier. The voltage gain of the amplifier can be reduced by putting a resistor in series with the capacitor between Pins 3 and 4 (Figure 14). The relationship between the gain and the external resistor is given by

$$A_{VR} = A_{VO} \cdot \frac{2(r_e + R_e)}{2(r_e + R_e) + R_{ext}}$$

where A_{VO} ≙ voltage gain with the external resistor = 0,
A_{VR} ≙ voltage gain with the external resistor in,
R_{ext} ≙ the external resistor, and
$r_e + R_e$ ≙ the resistance looking into Pin 3 or Pin 4.

Thus,

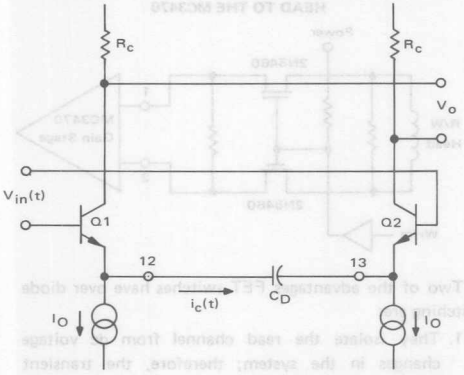
$$R_{ext} = 2\left(\frac{A_{VO}}{A_{VR}} - 1\right)(r_e + R_e).$$

A plot of $(r_e + R_e)$ versus temperature is shown in Figure 21. Figure 20 shows the normalized voltage gain versus temperature with the external resistor equal to 500 ohms.

ACTIVE DIFFERENTIATOR

The active differentiator in the MC3470 (simplified circuit shown in Figure 24), is implemented by coupling

FIGURE 24 – ACTIVE DIFFERENTIATOR NETWORK



the emitters of a differential amplifier with a capacitor resulting in a collector current that will be the derivative of the input voltage,

$$I = C\,dv/dt$$

If the output voltage is taken across a resistor through which the collector current is flowing, the resulting voltage will be the derivative of the input voltage.

$$V_o = 2Ri_c = 2RC\frac{dv_{in}(t)}{dt}$$

V_o is applied to a comparator which will provide zero crossing detection of the current waveform. Since the capacitor shifts the current 90° from the input voltage, the comparator performs peak detection of the input voltage.

The following terms will be used in determining the value of C to be used in the differentiator:

E_p ≙ peak differential voltage applied to MC3470 amplifier input.

$E_p \sin \omega t$ ≙ voltage waveform applied to MC3470 amplifier input (for purposes of discussion, assume a sine wave).

A_{VD} ≙ differential voltage gain of input amplifier.

$v_{in}(t)$ ≙ differential voltage waveform applied to the differentiator inputs.

$= E_p A_{VD} \sin \omega t$ (Note: The filter is assumed to be lossless.)

$i_c(t)$ ≙ current through capacitor C_D.

R_O ≙ output resistance of Q1 (Q2) at Pin 12 (13).

If $v_{in}(t) = E_p A_{VD} \sin \omega t$, then the current through the capacitor C_D is given by

$$i_c(t) = C_D A_{VD} E_p \omega \cos \omega t$$

and $V_O(t) = 2R_C C_D A_{VD} E_p \omega \cos \omega t$.

Accurate zero crossing detection of $V_O(t)$ [peak detection of $v_{in}(t)$] occurs when the current waveform $i_c(t)$ crosses through zero in a minimum amount of time. This condition is satisfied by maximizing current slew rate. For a given value of ω, the maximum slew rate occurs for the maximum value of i_c or $\cos \omega t = 1$. Therefore,

$$i_c = C_D A_{VD} E_p \omega$$

The MC3470 current-sourcing capacity will determine the maximum value i_c; therefore, C_D must be chosen such that the maximum i_c occurs at the maximum $A_{VD} E_p \omega$ product.

$$C_D = \frac{i_{c\,max}}{(A_{VD} E_p \omega)_{max}} = \frac{1\ mA}{(120)(E_p \omega)_{max}}$$

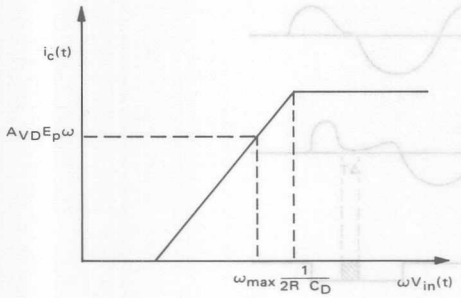
If the peak value specified for i_c is exceeded, the current source (I_O in Figure 24) will saturate and distort the waveform at Pins 12 and 13. Consequently, the differentiator will not accurately locate the peaks and peak shifting will occur in the digital output.

The effective output resistance R_O of Q1 (Q2) will create a pole (as shown in Figure 25) at $1/2\,R_O C_D$. If this pole is ten times greater than the maximum operating frequency (ω_{max}), the phase shift approaches 84°. Locating the pole at a frequency much greater than 10 ω_{max} needlessly extends the noise bandwidth thus:

$$2R_O = \frac{1}{C_D\,10\,\omega_{max}}$$

If R_O is not large enough to satisfy this condition, a series

FIGURE 25 – RESPONSE OF DIFFERENTIATOR USING ONLY C_D

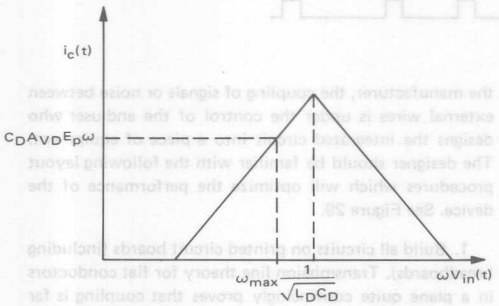


resistor can be added so that

$$R = 2R_O + R_D = \frac{1}{C_D\, 10\, \omega_{max}}.$$

To further reduce the noise bandwidth, a second pole can be added (as shown in Figure 26) by putting an

FIGURE 26 – COMPLETE RESPONSE OF DIFFERENTIATOR



inductor in series with the resistor and the capacitor. The values of R and L are determined by choosing the center frequency (ω_o) and the damping ratio (δ) to meet the systems requirements where

$$\omega_o = \frac{1}{\sqrt{LC_D}}$$

$$\delta = \frac{RC_D}{2\sqrt{LC_D}}$$

$$\omega_o = 10\ \omega_{max} = \frac{1}{\sqrt{LC_D}}$$

where C_D is chosen for maximum i_c as shown previously.

Solving for L gives:

$$L = \frac{1}{100\ C_D(\omega_{max})^2}$$

Using this value for L gives:

$$\delta = \frac{RC_D}{\frac{2}{10}\sqrt{\frac{C_D}{C_D(\omega_{max})^2}}}$$

Solving for R gives:

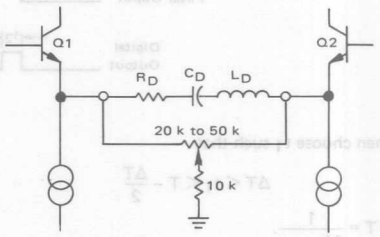
$$R = \frac{\delta}{5\ C_D\omega_{max}}$$

The total resistance (R) is the effective output resistance (R_O) plus the resistor added in the differentiator (R_D). Values of δ from 0.3 to 1 produce satisfactory results.

PEAK SHIFT CONSIDERATIONS

Peak shift, resulting from current imbalance in the differentiator, offset voltage in the comparator, etc., can be eliminated by nulling the current in the emitters of the differentiator with a potentiometer as shown in Figure 27.

FIGURE 27 – PEAK SHIFT COMPENSATION



The potentiometer across the differentiator components is adjusted until a symmetrical digital output cycle is obtained at Pin 10 for a sinusoidal input with the minimum anticipated $E_p\omega$ product.

DESIGN EQUATIONS FOR ONE-SHOTS

As shown in Figure 28, the MC3470 input waveform may have distortion at zero crossing, which can result in false triggering of the digital output. The time domain filter in the MC3470 can be used to eliminate the distortion by properly setting the period (t_1) of the one-shot timing elements on Pins 6 and 7. The following equation will optimize immunity to this signal distortion at zero crossing of the read head signal.

The timing equation for the time domain filter's one-shot is:

$$t_1 = R_1C_1K_1 + T_o$$

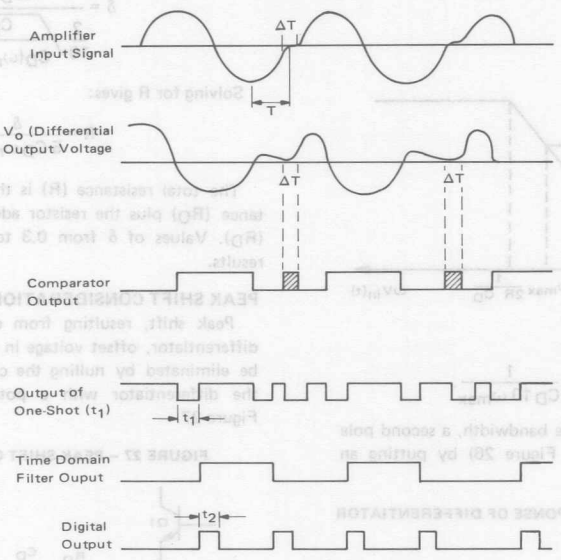
where $K_1 = 0.625$, $T_o = 200$ ns.

Actual time will be within ±15% of t_1 due to variations in the MC3470.

If ΔT is the maximum period of distortion (see Figure

7

FIGURE 28 – WAVEFORMS THROUGH THE READ CIRCUIT



28), then choose t_1 such that

$$\Delta T < t_1 < T - \frac{\Delta T}{2}$$

where $T = \frac{1}{4f_{(max)}}$.

The width of the digital output pulse t_2 (Pin 10) is determined by

$$t_2 = R_2C_2K_2$$

where $K_2 = 0.625$.

Actual pulse width will be within ±15% of t_2 due to variations in the MC3470.

To preserve the specified accuracy of the MC3470, R_1, R_2, C_1, and C_2 should remain in the ranges shown in the Electrical Characteristics. Also, to minimize current transients, it is important to keep the values of C_1 and C_2 as small as is convenient. For t_1 = 1 μs and t_2 = 200 ns, suggested good values for the capacitors are

$$C_1 = 250 \text{ pF}$$
$$C_2 = 160 \text{ pF}$$

BOARD LAYOUT AND TESTING CONSIDERATIONS

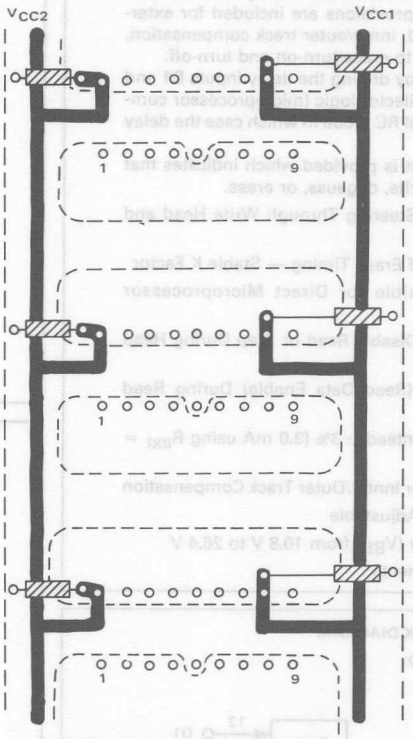
An LSI package has many input/output pins in close proximity, some carrying high level signals and others low level signals. As carefully as the on-chip isolation of the devices connected to these pins is implemented by the manufacturer, the coupling of signals or noise between external wires is under the control of the end-user who designs the integrated circuit into a piece of equipment. The designer should be familiar with the following layout procedures which will optimize the performance of the device. See Figure 29.

1. Build all circuits on printed circuit boards (including breadboards). Transmission line theory for flat conductors in a plane quite convincingly proves that coupling is far less than for round conductors in three dimensions.
2. Use a ground plane under the IC and over as much of the printed circuit board surface as possible without exceeding practical limits.
3. Avoid signal runs under the IC. Also avoid parallel runs of 1 inch or greater on the opposite or same side of board.
4. Use monolithic ceramic 0.1 μF capacitors for decoupling power supply transients: one from V_{CC1} to ground and one from V_{CC2} to ground for each IC package. Keep lead lengths to 1/4 inch or less and place in close proximity to the IC.
5. Keep all signal runs as short as possible.

When evaluating the device for phase jitter and frequency response, a special test jig should be designed to reduce ground loops and coupling caused by instrumentation. Instrumentation test setups must be calibrated

at each test frequency and differential equipment utilized where required. A valid evaluation of the performance of any read amplifier chain requires considerable care and thought.

FIGURE 29 – POWER AND GROUND DISTRIBUTION FOR MC3470 PRINTED CIRCUIT BOARD LAYOUT



NOTE: Dotted lines outline ground plane on back side of printed circuit board.

Specifications and Applications Information

FLOPPY DISK WRITE CONTROLLER/HEAD DRIVER

The MC3471 is a monolithic integrated Write Controller/Head Driver designed to provide the entire interface between the write data and head control signals and the heads (write and erase) for either Tunnel or straddle-erase floppy disk systems.

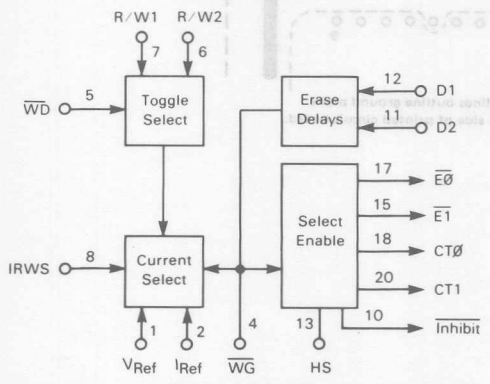
Provisions are made for selecting a range of accurately controlled write currents and for head selection during both read and write operation. Additionally, provisions are included for externally adjusting degauss period, inner/outer track compensation, and the delay from write gate to erase turn-on and turn-off.

Erase Delays are controlled by driving the delay inputs D1 and D2 with standard TTL open-collector logic (microprocessor compatible) or by using the external RC mode in which case the delay is one τ (K factor = 1.0).

In addition, an $\overline{\text{Inhibit}}$ output is provided which indicates that the heads are active during write, degauss, or erase.

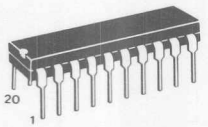
- Head Selection — Current Steering Through Write Head and Erase Coil in Write Mode
- Adjustable On-Chip Delay of Erase Timing — Stable K Factor
- Delay Pins Logic Compatible for Direct Microprocessor Compatibility
- $\overline{\text{Inhibit}}$ Output Provided to Disable Read or Step During Head Active Time
- Provides High Impedance (Read Data Enable) During Read Mode
- Head Current (Write) Guaranteed ±3% (3.0 mA using R_{ext} = 10 kΩ)
- IRW Select Input Provides for Innter/Outer Track Compensation
- Degauss Period Externally Adjustable
- Specified With Head Supply (V_{BB}) from 10.8 V to 26.4 V
- Minimizes External Components

BLOCK DIAGRAM



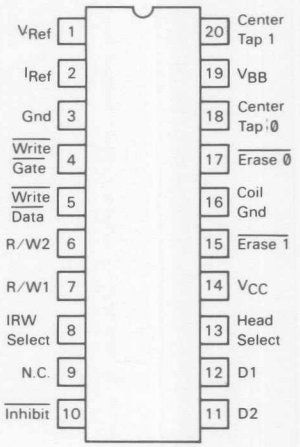
FLOPPY DISK WRITE CONTROLLER (WITH ERASE DELAY)

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 738-03

PIN CONNECTIONS



(Top View)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 14)	V_{CC}	7.0	Vdc
Power Supply Voltage (Pin 19)	V_{BB}	30	Vdc
Input Voltage (Pins 4, 5, 8, 13)	V_I	5.75	Vdc
Output Applied Voltage (Pin 10)	V_O	7.0	Vdc
Open-Collector Sink Current (Pin 10)	I_O	25	mA
Storage Temperature	T_{stg}	-55 to +150	°C
Operating Junction Temperature	T_J	150	°C

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 14)	V_{CC}	+4.75 to +5.25	Vdc
Power Supply Voltage (Pin 19)	V_{BB}	+10.8 to +26.4	Vdc
Operating Ambient Temperature Range	T_A	0 to +70	°C

ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = 4.75 to 5.25 V, V_{BB} = 10.8 to 26.4 V unless otherwise noted. Typicals given for V_{CC} = 5.0 V, V_{BB} = 12 V and T_A = 25°C unless otherwise noted.)

Characteristics	Pins	Symbol	Min	Typ	Max	Unit
DIGITAL INPUT VOLTAGES						
Power Supply Current — V_{CC}		I_{CC}	—	22	60	mA
V_{BB}		I_{BB}	—	15	30	
High Level Input Voltage (V_{CC} = 4.75 V)	4, 8, 13	V_{IH}	2.0	—	—	V
Low Level Input Voltage (V_{CC} = 5.25 V)	4, 8, 13	V_{IL}	—	—	0.8	V
Input Clamp Voltage (I_{IK} = -12 mA)	4, 5, 8, 13	V_{IK}	—	-0.87	-1.5	V
Positive Threshold (V_{CC} = 5.0)	5	$V_{T(+)}$	1.5	1.75	2.0	V
Negative Threshold (V_{CC} = 5.0)	5	$V_{T(-)}$	0.7	0.98	1.3	V
Hysteresis ($V_{T(+)} - V_{T(-)}$)	5	V_{HTS}				V
T_A = 0°C to +70°C			0.2	—	—	
T_A = 25°C			0.4	0.76	—	
DIGITAL INPUT CURRENTS						
High Level Input Current (V_{CC} = 5.25 V, V_{BB} = 26.4 V, V_I = 2.4 V)	4, 5, 8, 13	I_{IH}	—	0.1	40	μA
Low Level Input Current (V_{CC} = 5.25 V, V_{BB} = 26.4 V, T_A = 25°C unless noted below)	4, 5, 8, 13	I_{IL}	—	—	-1.6	mA
V_{BB} = 12 V	4		—	0.36	—	
V_{BB} = 24 V	4		—	0.76	—	
V_{CC} = 5.0 V	5		—	0.46	—	
V_{CC} = 5.0 V	8, 13		—	0.39	—	

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ELECTRICAL CHARACTERISTICS (continued) (T_A = 0 to +70°C, V_{CC} = 4.75 to 5.25 V, V_{BB} = 10.8 to 26.4 V unless otherwise noted. Typicals given for V_{CC} = 5.0 V, V_{BB} = 12 V and T_A = 25°C unless otherwise noted.)

Characteristics	Pins	Symbol	Min	Typ	Max	Unit
CENTER-TAP and ERASE OUTPUTS						
Output High Voltage (See Figure 14) (I_{OH} = −100 mA, V_{CC} = 4.75 V) V_{BB} = 10.8 to 26.4 V	19, 20	V_{OH}	V_{BB}-1.5	V_{BB}-1.0	—	V
Output Low Voltage (See Figure 14) (I_{OL} = 1.0 mA) V_{BB} = 12 V V_{BB} = 24 V	18, 20	V_{OL}	— —	70 70	150 150	mV
Output High Leakage Current (V_{OH} = 24 V, V_{CC} = 4.75 V, V_{BB} = 24 V)	15, 17	I_{OH}	—	0.01	100	μA
Output Low Voltage (See Figure 15) (I_{OL} = 90 mA, V_{CC} = 4.75 V) V_{BB} = 12 V V_{BB} = 24 V	15, 17	V_{OL}		 0.27 0.27	 0.60 0.60	V
DIGITAL OUTPUT LEVEL ($\overline{\text{Inhibit}}$)						
High Level Output Current (V_{OH} = 7.0 V, V_{CC} = 4.75 V)	10	I_{OH}	—	—	100	μA
Low Level Output Voltage (I_{OL} = 4.0 mA, V_{CC} = 4.75 V)	10	V_{OL}	—	—	0.5	V
CURRENT SOURCE						
Reference Voltage	1	V_{Ref}	—	5.7	—	V
Degauss Voltage (See Text) (Voltage Pin 1 - Voltage Pin 2)	1	V_{DEG}	—	1.0	—	V
Bias Voltage	2	V_F	—	0.7	—	V
Write Current Off Leakage (V_{OH} = 30 V)	6, 7	I_{OH}	—	0.03	15	μA
Saturation Voltage (V_{BB} = 12 V)	6, 7	V_{sat}	—	0.85	2.7	V
Current Sink Compliance (For $V_{6,7}$ = 4.0 V to 24 V, $V_{\overline{WG}}$ = 0.8 V)	6, 7	$\Delta I_{RW2,1}$	—	15	40	μA
Average Value Write Current $\left(\frac{I_{Pin\ 6} + I_{Pin\ 7}}{2}\right)$ for V_{BB} = 10.8 to 26.4 V) @ $I_{R/W} = I_{LOW}$, R = 10 k T_A = 25°C T_A = 0 to +70°C @ $I_{R/W} = I_{LOW}$, R = 5.0 k T_A = 25°C T_A = 0 to +70°C @ $I_{R/W} = I_{HI}$, R = 10 k ($I_{HI} = I_{LOW}$ + % I_{LOW}) T_A = 25°C T_A = 0 to +70°C	6, 7	$\overline{I_{R/W(L)}}$ $\overline{\Delta I_{R/W(H)}}$	 2.91 2.84 5.64 5.51 31.3 30.3	 3.0 — 5.89 — 33.3 33.3	 3.09 3.16 6.14 6.28 35.5 36.6	mA %
Difference in Write Current ($\lvert I_{Pin\ 6} - I_{Pin\ 7} \rvert$ @ $I_{R/W} = I_{LOW}$, V_{BB} = 10.8 V to 26.4 V) R = 10 k T_A = 25°C T_A = 0 to +70°C R = 5.0 k T_A = 25°C T_A = 0 to +70°C	6, 7	$I_{R/W\Delta}$	 — — — —	 0.003 — — —	 0.015 0.023 0.030 0.046	mA

ERASE DELAY ACCURACY (V_{CC} = 4.75 to 5.25 V, T_A = 0 to +70°C, V_{BB} = 10.8 to 26.4 V, — refer to Figure 9.)

Characteristics	Test	Min	Typ	Max	Unit
Delay Error, Pin 11, 12 D1, D2 = RC $\pm E_{D1,2}$, 30 kΩ ≤ R ≤ 300 kΩ	$E_{D1,2}$	—	—	15	%

AC SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C, V_{BB} = 24 V, I_{RWS} = 0.4 and $I_{R/W}$ = 3.0 mA unless otherwise noted.)

Characteristics (Note 1)	f_{in} (Note 2)	Min	Typ	Max	Unit
1. Delay from Head Select going low through 0.8 V to CT0 going high through 20 V.	HS, Pin 13	—	1.6	4.0	μs
2. Delay from Head Select going low through 0.8 V to CT1 going low through 1.0 V.	HS, Pin 13	—	2.1	4.0	μs
3. Delay from Head Select going high through 2.0 V to CT0 going low through 1.0 V.	HS, Pin 13	—	1.7	4.0	μs
4. Delay from Head Select going high through 2.0 V to CT1 going high through 20 V.	HS, Pin 13	—	1.4	4.0	μs
5. Delay from $\overline{WG}$ going low through 0.8 V to CT0 going low through 1.0 V.	$\overline{WG}$, Pin 4	—	1.3	4.0	μs
6. Delay from $\overline{WG}$ going low through 0.8 V to CT1 going high through 20 V.	$\overline{WG}$, Pin 4	—	0.8	4.0	μs
7. Delay from $\overline{WG}$ going low through 0.8 V to CT0 going high through 20 V.	$\overline{WG}$, Pin 4	—	0.75	4.0	μs
8. Delay from $\overline{WG}$ going low through 0.8 V to CT1 going low through 1.0 V.	$\overline{WG}$, Pin 4	—	1.2	4.0	μs
9. After $\overline{WG}$ goes high, delay from R/W1 turning off through 10% to CT0 going high through 20 V.	$\overline{WG}$, Pin 4	20	750	—	ns
10. After $\overline{WG}$ goes high, delay from R/W1 turning off through 10% to CT1 going low through 1.0 V.	$\overline{WG}$, Pin 4	20	1200	—	ns
11. After $\overline{WG}$ goes high, delay from R/W2 turning off through 10% to CT0 going low through 1.0 V.	$\overline{WG}$, Pin 4	20	1200	—	ns
12. After $\overline{WG}$ goes high, delay from R/W2 turning off through 10% to CT1 going high through 20 V.	$\overline{WG}$, Pin 4	20	600	—	ns
13. After $\overline{WG}$ goes low, delay from CT0 going low through 1.0 V to R/W1 turning on through 10%.	$\overline{WG}$, Pin 4	20	750	—	ns
14. After $\overline{WG}$ goes low, delay from CT1 going low through 1.0 V to R/W2 turning on through 10%.	$\overline{WG}$, Pin 4	20	750	—	ns
15. After $\overline{WG}$ goes low, fall time (10% to 90%) of R/W1.	$\overline{WG}$, Pin 4	—	5.0	200	ns
16. After $\overline{WG}$ goes low, fall time (10% to 90%) of R/W2.	$\overline{WG}$, Pin 4	—	5.0	200	ns
17. Setup time, Head Select going low before $\overline{WG}$ going low.	$\overline{WG}$, Pin 4	4.0	—	—	μs
18. $\overline{\text{Write Data}}$ low Hold Time	$\overline{WD}$, Pin 5	200	—	—	ns
19. $\overline{\text{Write Data}}$ high Hold Time	$\overline{WD}$, Pin 5	500	—	—	ns
20. Delay from $\overline{WG}$ going high through 2.0 V to R/W 1 turning off through 10% of on value.	$\overline{WG}$, Pin 4	—	3.9	—	μs
21. Delay from $\overline{WG}$ going low thru 0.8 V to $\overline{Inhibit}$ going low thru 0.5 V	$\overline{WG}$, Pin 4	—	0.08	4.0	μs
22. After $\overline{WG}$ goes high, delay from R/W1 turning off thru 10% to $\overline{Inhibit}$ going high thru 1.5 V (10 k pullup on Inhibit, Note 3)	$\overline{WG}$, Pin 4	20	750	—	ns
23. After $\overline{WG}$ goes high, delay from $\overline{E1}$ going high thru 23 V to $\overline{Inhibit}$ going high thru 1.5 V (10 k pullup on Inhibit, Note 3)	$\overline{WG}$	20	750	—	ns

Notes:
1. Test numbers refer to encircled numbers in Figures 3 & 16.
2. AC test waveforms applied to the designated pins as follows:

Pin	f_{in}	Amplitude	Duty Cycle
$\overline{HS}$, Pin 13	50 kHz	0.4 to 2.4 V	50%
$\overline{WG}$, Pin 4	50 kHz	0.4 to 2.4 V	50%
$\overline{WD}$, Pin 5	1.0 MHz	0.2 to 2.4 V	50%

3. Test Conditions 22, or 23, whichever produces the longer delay, will control Inhibit.

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AC SWITCHING CHARACTERISTICS (continued)

(V_{CC} = 5.0 V, T_A = 25°C, V_{BB} = 24 V, $\overline{WG}$ = 0.4 unless otherwise noted)

Characteristics (Note 4)	Min	Typ	Max	Unit
1. Delay from $\overline{\text{Write Data}}$ going low through 0.9 V to R/W1 turning on through 50%.	—	85	—	ns
2. Delay skew, difference of R/W1 turning off and R/W2 turning on through 50% after $\overline{\text{Write Data}}$ going low through 0.9 V.	—	1.0	±40	ns
3. Delay from $\overline{\text{Write Data}}$ going low through 0.9 V to R/W1 turning off through 50%.	—	80	—	ns
4. Delay skew, difference of R/W1 turning on and R/W2 turning off 50% after $\overline{\text{Write Data}}$ going low through 0.9 V.	—	1.0	±40	ns
5. Fall time, 10% to 90%, of R/W1	—	1.7	200	ns
6. Fall time, 10% to 90%, of R/W2	—	1.7	200	ns
7. Rise time, 90% to 10%, of R/W1	—	12	200	ns
8. Rise time, 90% to 10%, of R/W2	—	12	200	ns

Note 4. Test numbers refer to encircled numbers in Figures 2 & 15.
f_{in} = 1.0 MHz, 50% Duty Cycle and Amplitude of 0.2 V to 2.4 V.

PIN DESCRIPTION TABLE

Name	Symbol	Pin	Description
Head Select	HS	13	Head Select input selects between the head I/O pins; center-tap, erase, and read/write. A HIGH selects Head 0 and a LOW selects Head 1.
$\overline{\text{Write Gate}}$	$\overline{WG}$	4	$\overline{\text{Write Gate}}$ input selects the mode of operation. HIGH selects the read mode, while LOW selects the Write Control mode and forces the write current.
$\overline{\text{Write Data}}$	$\overline{WD}$	5	$\overline{\text{Write Data}}$ input controls the turn on/off of the write current. The internal divide-by-two flip-flop toggles on the negative going edge of this input to direct the current alternately to the two halves of the head coils.
IRW Select	IRWS	8	IRW Select input selects the amount of write current to be used. When LOW, the current equals the value found in Figure 5, according to the external resistor. When HIGH, the current equals the low current + 33%.
V_{Ref} I_{Ref}	V_{Ref} I_{Ref}	1 2	A resistor between these pins sets the write current. (Refer to Figure 4.) A capacitor from V_{Ref} to Gnd will adjust the Degauss period.
Center-Tap 0	CT0	18	Center-Tap 0 output is connected to the center tap of Head 0. It will be pulled to Gnd or V_{BB} (+12 or +24) depending on mode and head selection.
$\overline{\text{Erase 0}}$	$\overline{E0}$	17	$\overline{\text{Erase 0}}$ will be LOW for writing on Head 0, and floating for other conditions.
Center-Tap 1	CT1	20	Center-Tap 1 output is connected to the center tap of Head 1. It will be pulled to Gnd or V_{BB} (+12 or +24) depending on mode and head selection.
$\overline{\text{Erase 1}}$	$\overline{E1}$	15	$\overline{\text{Erase 1}}$ will be LOW for writing on Head 1, and floating for other conditions.
R/W2	R/W2	6	R/W2 input is one of the differential inputs that sinks current during writing, being the opposite phase of R/W1. It will be connected to one side of the heads.
R/W1	R/W1	7	R/W1 input is one of the differential inputs that sinks current during writing, being the opposite phase of R/W2. It will be connected to one side of the heads.
	V_{CC}	14	+5.0 V Power
	V_{BB}	19	+12 V or + 24 V Power
	Gnd	16	Coil grounds
	Gnd	3	Reference and logic ground
Delay 1	D1	12	Erase Turn-On Delay adjust (RC or Logic)
Delay 2	D2	11	Erase Turn-Off Delay adjust (RC or Logic)
Inhibit	$\overline{\text{Inhibit}}$	10	Active low open-collector output provided to indicate heads are active in the write, degauss or erase mode. (Used for step or read inhibit.)

FIGURE 1 — LOGIC DIAGRAM

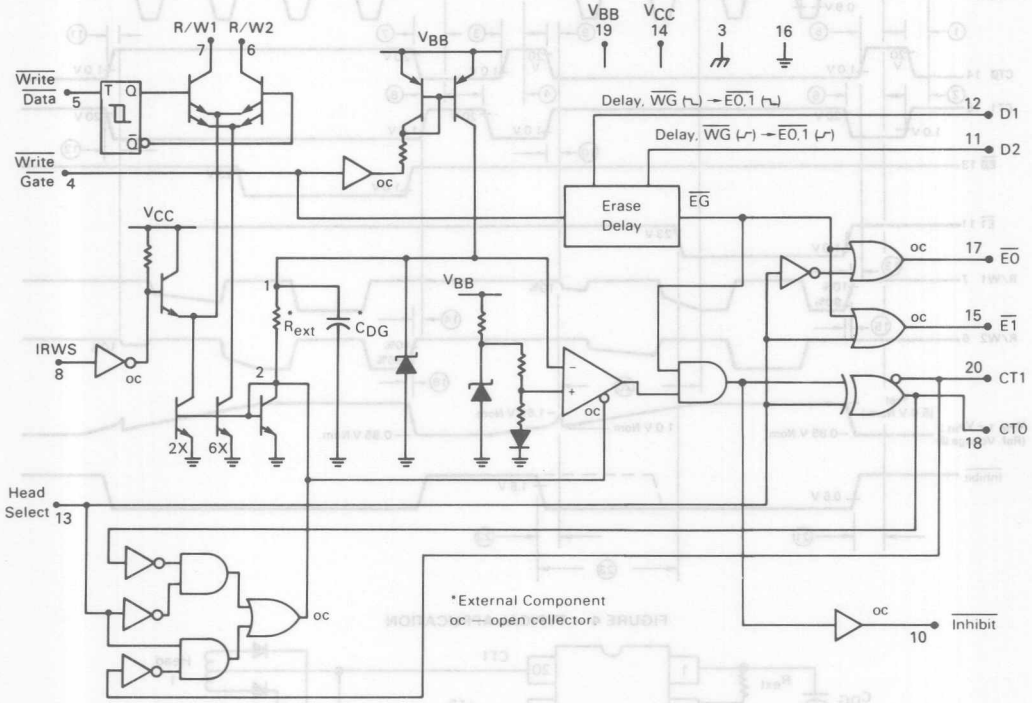
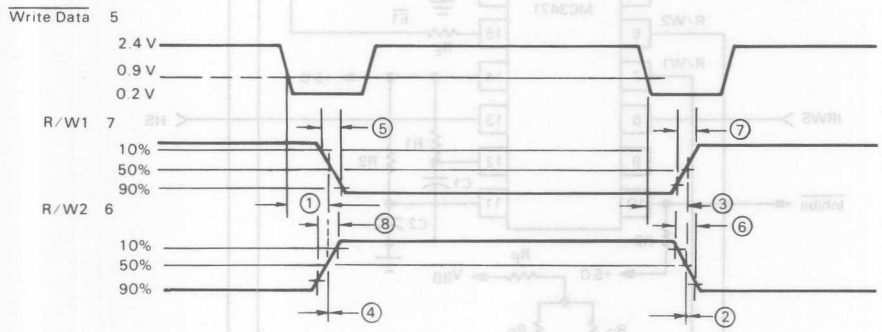


FIGURE 2 — R/W1 AND R/W2 RELATIONSHIP



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FIGURE 3 — AC TIMING DIAGRAM

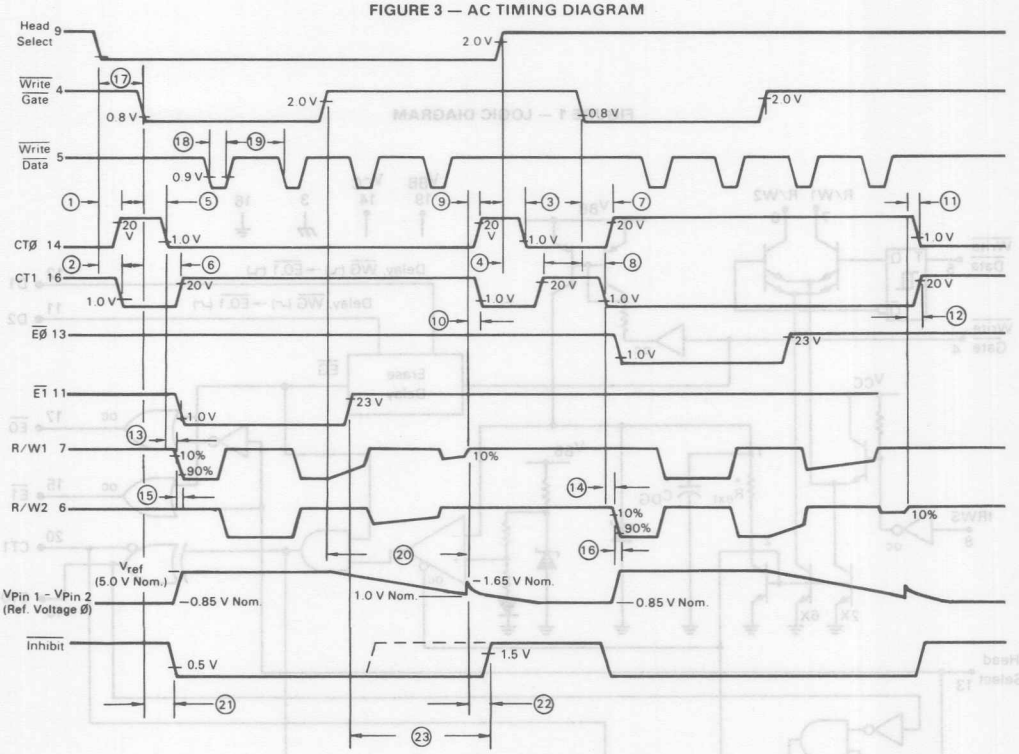
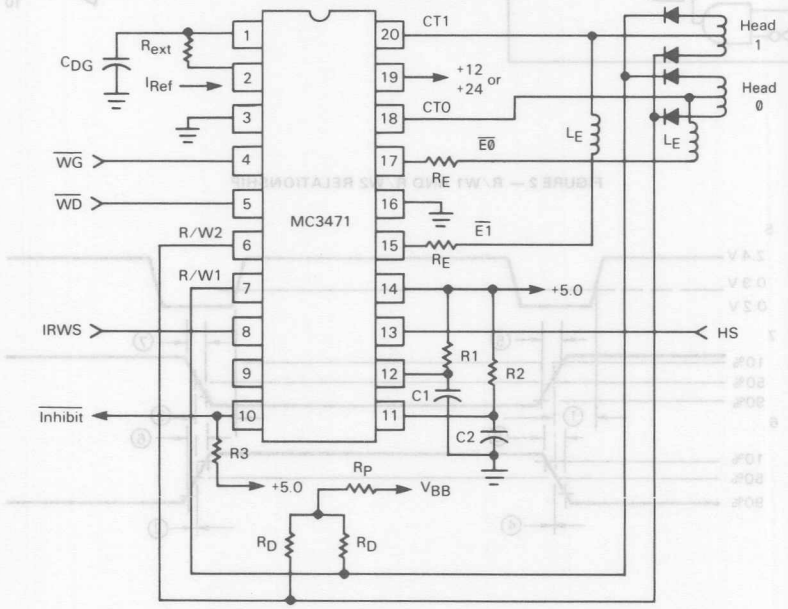


FIGURE 4 — TYPICAL APPLICATION



APPLICATION INFORMATION

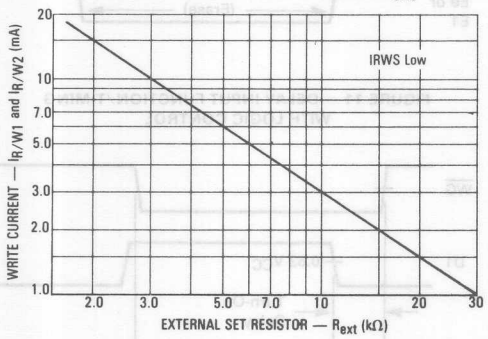
The MC3471P serves as a complete interface between the Write Control functional signals (Head Select, Write Data, Write Gate and inner track compensation, IRWS) and the head itself. A typical configuration is shown in Figure 4. L_E's are erase coils.

WRITE CURRENT SELECTION

Although the MC3471P has been specified for 3.0 mA write current (with a 10 kΩ external resistor), a range of write current values can be chosen by varying R_{ext} using the plot in Figure 5. This current can also be derived using the relationship $I_{Write}\,(mA) = \frac{30}{R_{ext}(k\Omega)}$

I_{Ref}, the current flowing in R_{ext} (required only for dissipation calculations) can be worst case using the fact that the differential voltage between Pins 1 and 2 (V_{Ref}) shown in Figure 3 never exceeds 5.0 volts. With a low value of R_{ext} = 1.0 kΩ, P_D = 25 mW.

FIGURE 5 — WRITE CURRENT versus R_{ext}



WRITE CURRENT DAMPING

Referring to Figure 4, resistors R_D are used to dampen any ringing that results from applying the relatively fast risetime write current pulse to the inductive head load. Values chosen will be a funciton of head characteristics and the desired damping. Rp serves as a common pullup resistor to the head supply V_{BB}.

DEGAUSS PERIOD

Degauss of the read/write head can be accomplished at the end of each write operation by attaching a capacitor from Pin 1 to ground. The time relationship that results is shown in Figure 7. A simplified diagram of this function is shown in Figure 6.

While $\overline{WG}$ is low, the selected write current flows into Pin 6 or Pin 7 (R/W1 or R/W2) and is mirrored through the external resistor, R_{ext}. The degauss capacitor, C_{DG}, will be charged to approximately 5.7 volts. After $\overline{WG}$ goes high, the voltage on C_{DG} begins to decay toward 0.7 V. When the voltage reaches the comparator threshold of 1.7 V, the comparator output triggers the internal logic to completely turn off the write current. At this point, the pulse amplitude on the R/W1 and R/W2 pins has returned to 10% of its maximum value.

See Application Note AN917 for further information.

Figure 7, Degauss Period shows the relationship between C_{DG} and Degauss Period for R_{ext} = 10 kΩ. This period is equal to the exponential delay time for the voltage as mentioned plus internal delay times.

FIGURE 6 — SIMPLIFIED DEGAUSS CIRCUIT

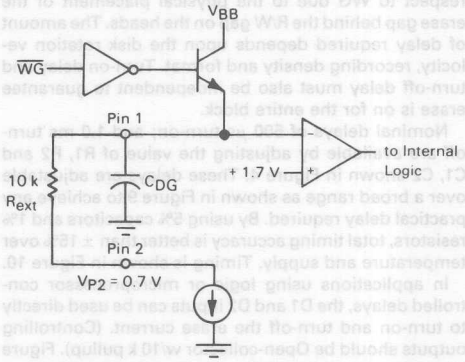
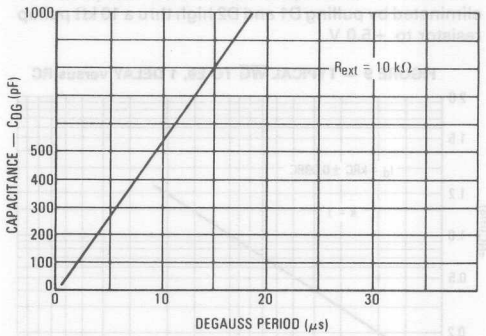


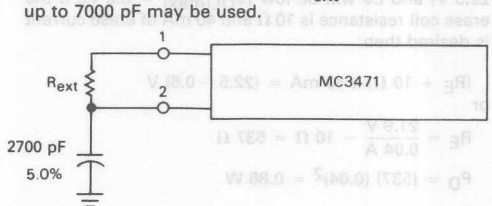
FIGURE 7 — DEGAUSS PERIOD versus CAPACITANCE (C_{DG})



POWER-UP WRITE CURRENT CONTROL

During power-up, under certain conditions (V_{BB} comes up first while $\overline{WG}$ is low), there can be a write current transient on Pins 6 and 7 (R/W1 and R/W2) of sufficient magnitude to cause writing to occur if the head is loaded.

This transient can be eliminated by placing a capacitor from Pin 2 to ground. This also delays the write current when $\overline{WG}$ goes low and this delay must be accounted for when the capacitor on Pin 2 is used. The delay is 3.0 μs for a 2700 pF capacitor, and R_{ext} = 10 kΩ. Values up to 7000 pF may be used.



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ERASE DELAY

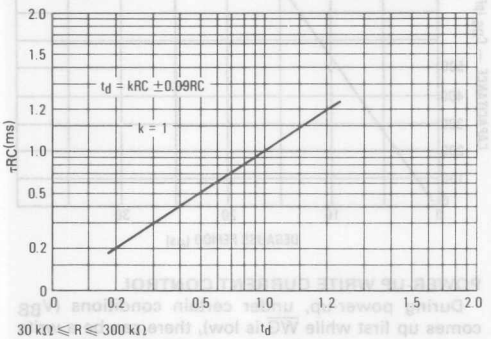
The MC3471P can be used with both straddle and tunnel erase heads. When using the tunnel erase heads, it is necessary to delay the erase current in time with respect to $\overline{WG}$ due to the physical placement of the erase gap behind the R/W gap on the heads. The amount of delay required depends upon the disk rotation velocity, recording density and format. Turn-on delay and turn-off delay must also be independent to guarantee erase is on for the entire block.

Nominal delays of 500 μs turn-on; and 1.0 ms turn-off are available by adjusting the value of R1, R2 and C1, C2 shown in Figure 4. These delays are adjustable over a broad range as shown in Figure 9 to achieve any practical delay required. By using 5% capacitors and 1% resistors, total timing accuracy is better than ±15% over temperature and supply. Timing is shown in Figure 10.

In applications using logic or microprocessor controlled delays, the D1 and D2 inputs can be used directly to turn-on and turn-off the erase current. (Controlling outputs should be Open-collector w/10 k pullup). Figure 11 shows the relative timing involved for the microprocessor and logic controlled applications.

In straddle erase systems, the erase delays can be eliminated by pulling D1 and D2 high thru a 10 kΩ pullup resistor to +5.0 V.

FIGURE 9 — TYPICAL $\overline{WG}$ TO E0, 1 DELAY versus RC



ERASE CURRENT

The value of R_E, the erase current set resistor, is found by referring to Figure 12 and selecting the desired erase current.

Looking at the simplified erase current path in Figure 12, when writing, CT0 will be high ($V_{OH(min)}$ = 22.5 V) and E0 will be low ($V_{OL(max)}$ = 0.6 V). If the erase coil resistance is 10 Ω and 40 mA of erase current is desired then:

$$(R_E + 10\ \Omega) \times 40\ mA = (22.5 - 0.6)\ V$$

or

$$R_E = \frac{21.9\ V}{0.04\ A} - 10\ \Omega = 537\ \Omega$$

$$P_D = (537)\ (0.04)^2 = 0.86\ W$$

This gives the minimum value R_E for worst case V_{OH}/V_{OL} conditions. It is also recommended that a diode be used as indicated for inductive back emf suppression.

FIGURE 10 — DELAY INPUT FUNCTION/TIMING WITH RC ELEMENTS

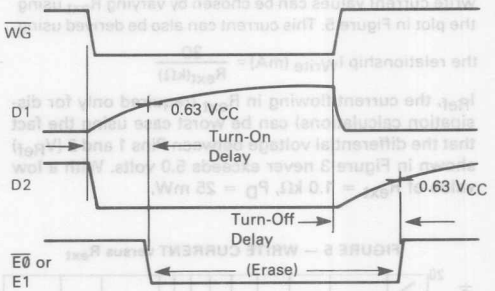


FIGURE 11 — DELAY INPUT FUNCTION/TIMING WITH LOGIC CONTROL

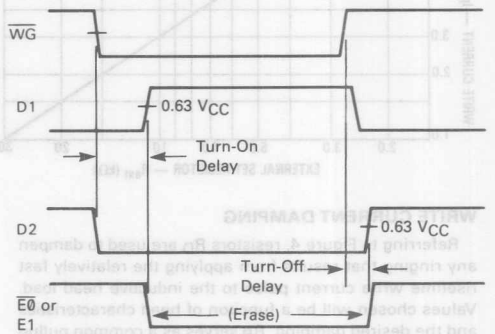


FIGURE 12 — ERASE CURRENT (R_E Selection)

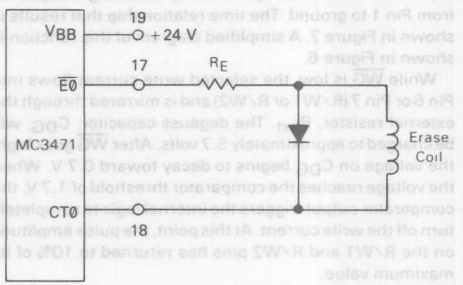
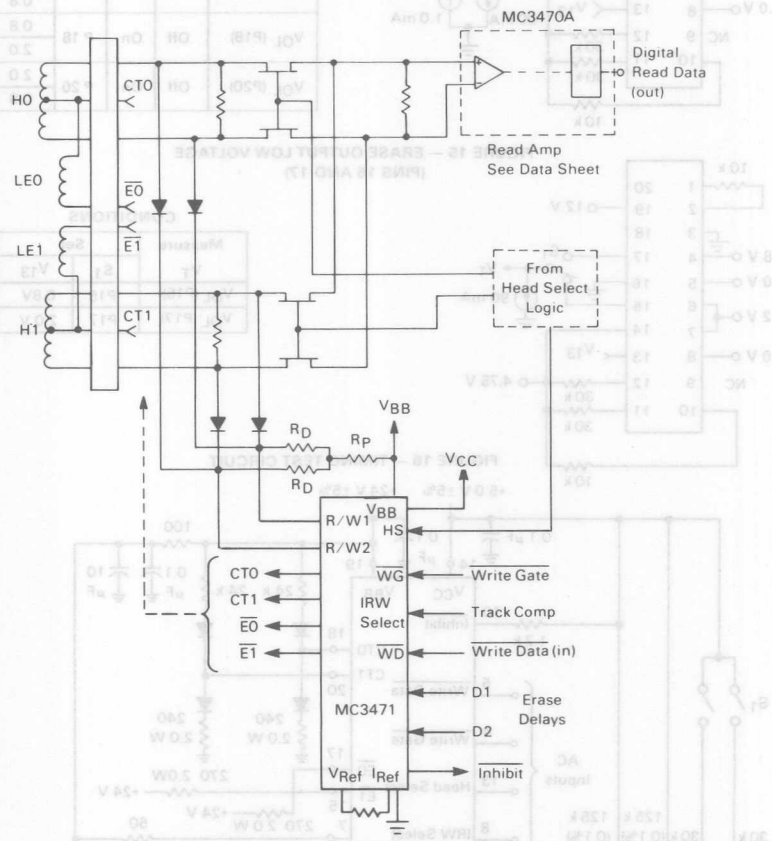


FIGURE 13 — TYPICAL DUAL HEAD FLOPPY DISK SYSTEM USING FET GATE READ CHANNEL SELECTION AND MC3471/MC3470A

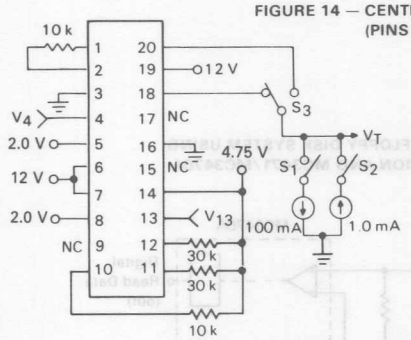


Function	CT0	CT1	E0	E1
Write 0	V_{BB}	0 V	On	Off
Write 1	0 V	V_{BB}	Off	On
Read 0	0 V	V_{BB}	Off	Off
Read 1	V_{BB}	0 V	Off	Off

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TEST FIGURES

FIGURE 14 — CENTER TAP OUTPUT VOLTAGE
(PINS 18 AND 20)

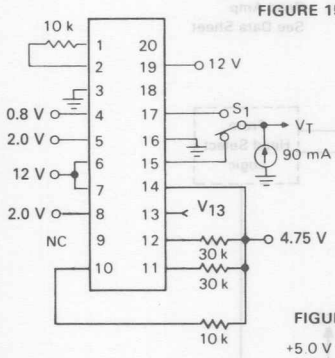


CONDITIONS

Measure V_T	Set S_1	S_2	S_3	V_4*	V_{13}*
V_{OH} (P18)	On	Off	P 18	0.8	2.0
				2.0	0.8
V_{OH} (P20)	On	Off	P 20	2.0	2.0
				0.8	0.8
V_{OL} (P18)	Off	On	P 18	0.8	0.8
				2.0	2.0
V_{OL} (P20)	Off	On	P 20	2.0	0.8
				0.8	2.0

*Volts

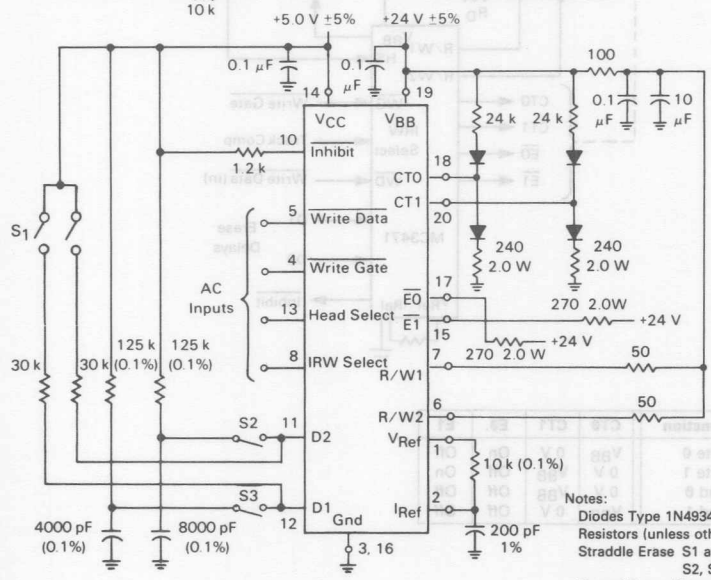
FIGURE 15 — ERASE OUTPUT LOW VOLTAGE
(PINS 15 AND 17)



CONDITIONS

Measure V_T	Set S_1	V_{13}
V_{OL} (P15)	P15	0.8V
V_{OL} (P17)	P17	2.0 V

FIGURE 16 — TIMING TEST CIRCUIT



Notes:
Diodes Type 1N4934
Resistors (unless otherwise noted) are 1/4 W 5%
Straddle Erase S1 and S_4 Closed
S2, S3 Open
Tunnel Erase S1 and S_4 Open
S2, S3 Closed

MC3480

Specifications and Applications Information

MEMORY CONTROLLER FOR 16 PIN 4K, 16K AND 64K DYNAMIC RAMs

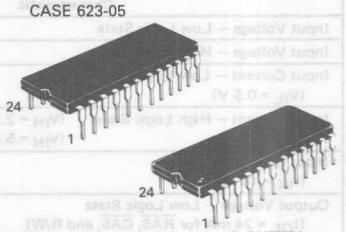
The memory controller chip is designed to greatly simplify the interface logic required to control the popular 16 pin multiplexed dynamic NMOS RAMs in a microprocessor system such as the M6800. The controller will generate, on command from the microprocessor, the proper timing signals required to successfully transfer data between the microprocessor and the NMOS memories. The controller, in conjunction with an oscillator, will also generate the necessary signals required to insure that the dynamic memories are refreshed for the retention of data.

- Greatly Simplify the MPU-Dynamic Memory Interface
- Reduce Package Count and System Access/Cycle Times 30%
- Chip Enable for Expansion to Larger Word Capacity
- Generate 1 of 4 $\overline{RAS}$ Signals for an Optimum 16K/64K Memory System
- High Input Impedance for Minimum Loading of MPU Bus
- Schottky TTL Technology for High Performance
- Useful with 4K and 16K and Future Expanded Dynamic RAMs

DYNAMIC MEMORY CONTROLLER

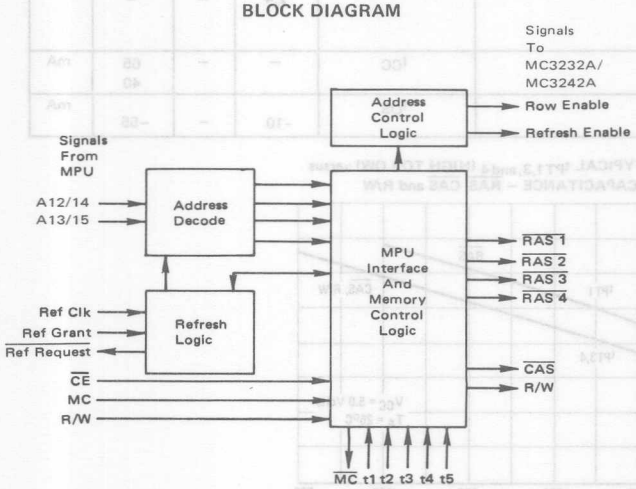
SCHOTTKY MONOLITHIC INTEGRATED CIRCUIT

L SUFFIX
CERAMIC PACKAGE
CASE 623-05



P SUFFIX
PLASTIC PACKAGE
CASE 649-03

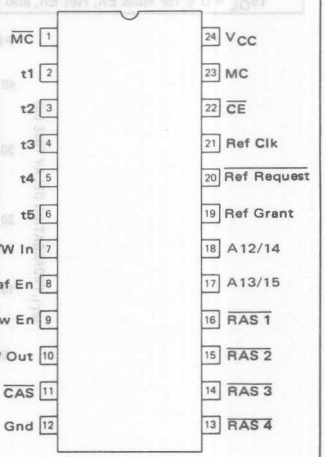
BLOCK DIAGRAM



Several methods may be employed to generate the required time delay:

1. One shots
2. High frequency counters
3. High frequency shift registers
4. Delay lines
5. Signals from MPU Clock

PIN CONNECTIONS



See Pin Descriptions

7

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Input Voltage	V_I	−0.5 to +7.0	Vdc
Output Voltage	V_O	−0.5 to +7.0	Vdc
Operating Ambient Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−65 to +150	°C
Operating Junction Temperature Ceramic Package Plastic Package	T_J	 175 150	°C

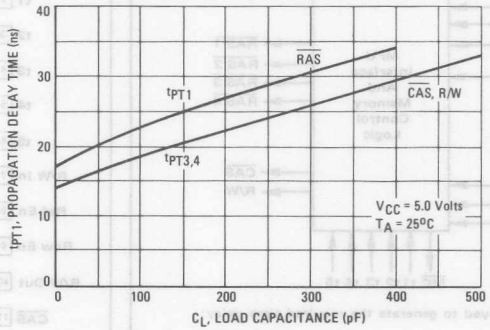
RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+4.50 to +5.50	Vdc
Operating Ambient Temperature Range	T_A	0 to +70	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted specifications apply over recommended power supply and temperature ranges.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage — Low Logic State	V_{IL}	–	–	0.8	V
Input Voltage — High Logic State	V_{IH}	2.0	–	–	V
Input Current — Low Logic State (V_{IL} = 0.5 V)	I_{IL}	–	–	-250	µA
Input Current — High Logic State (V_{IH} = 2.7 V) (V_{IH} = 5.5 V)	I_{IH}	–	–	40 100	µA
Input Clamp Voltages (I_{IK} = 18 mA)	V_{IK}	–	–	-1.5	V
Output Voltage — Low Logic State (I_{OL} = 24 mA for $\overline{RAS}$, $\overline{CAS}$, and R/W) (I_{OL} = 8.0 mA for Row En, Ref En, $\overline{MC}$, $\overline{Ref\ Req}$)	V_{OL}	 – –	 – –	 0.5 0.5	V
Output Voltage — High Logic State (I_{OH} = -1.0 mA for $\overline{RAS}$, $\overline{CAS}$, and R/W) (I_{OH} = -0.4 mA for Row En, Ref En, and $\overline{MC}$) I_{OH} = -0.2 mA for $\overline{Ref\ Req}$ (Note: $\overline{Ref\ Req}$ output has internal 5.0 k resistive pullup to V_{CC}.)	V_{OH}	 3.0 2.4 2.4	 – – –	 – – –	V
Power Supply Current — During R/W or Refresh — During Idle	I_{CC}	–	–	65 40	mA
Output Short-Circuit Current (V_{OL} = 0 V for Row En, Ref En, and $\overline{MC}$)	I_{OS}	-10	–	-55	mA

FIGURE 1 — TYPICAL $t_{PT1,3,and4}$ (HIGH TO LOW) versus LOAD CAPACITANCE — $\overline{RAS}$, $\overline{CAS}$ and R/W



SWITCHING CHARACTERISTICS (Unless otherwise noted, V_{CC} = 5.0 V, T_A = 25°C

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Times (Full AC Load — All Outputs)					ns
MC to $\overline{MC}$ — Low to High	$t_{PLH(\overline{MC})}$	—	7.0	14	
MC to $\overline{MC}$ — High to Low	$t_{PHL(\overline{MC})}$	—	9.0	17	
t1 to $\overline{RAS}$	t_{PT1}	18	26	40	
t2 to Row En	t_{PT2}	16	21	35	
t3 to $\overline{CAS}$	t_{PT3}	17	26	45	
t4 to R/$\overline{W}$	t_{PT4}	16	22	45	
t5 to $\overline{CAS}$	t_{PT5C}	22	30	42	
to $\overline{RAS}$	t_{PT5R}	19	26	40	
to R/$\overline{W}$	t_{PT5W}	30	42	58	
to Row En (Refresh)	t_{PT5ER}	30	50	65	
to Row En (R/$\overline{W}$)	t_{PT5E}	25	32	48	
to Refresh En	t_{PT5F}	22	46	55	
Ref Clk to $\overline{Ref\ Req}$	t_{PCQ}	10	17	27	
Ref Grant to Row En, to Ref En	t_{PGS}	20	30	43	
t1 to $\overline{Ref\ Req}$ (Ref only) Note 1	t_{PTQ}	22	60	75	
Setup Times (Full AC Load — All Pins)					ns
Ref Clk before Ref Grant	$t_{su(RC)}$	35	—	—	
A12, A13 before t1	$t_{su(A)}$	10	—	—	
R/$\overline{W}$ Input before t4	$t_{su(R/W)}$	33	—	—	
$\overline{CE}$ before t1	$t_{su(\overline{CE})}$	20	—	—	
Ref Grant before t1	$t_{su(RG)}$	50	—	—	
Hold Times (Full AC Load — All Pins)					ns
A12, A13 after t5	$t_{h(A)}$	15	—	—	
$\overline{CE}$ after t1	$t_{h(\overline{CE})}$	0	—	—	
R/$\overline{W}$ after t4	$t_{h(R/W)}$	0	—	—	
MC Rising after t1 Rising	$t_{h(MC)}$	30	—	—	
Minimum Delay Times (Note 1 — Full AC Load — All Pins)					ns
t1 Low to High to t2 Low to High	$t_{d(1-2)}$	30	—	—	
t1 Low to High to t4 Low to High	$t_{d(1-4)}$	33	—	—	
t2 Low to High to t3 Low to High	$t_{d(2-3)}$	30	—	—	
t3 Low to High to t5 Low to High	$t_{d(3-5)}$	30	—	—	
Minimum Pulse Widths					ns
t1 through t5 Low	$t_{WL(t)}$	30	—	—	
t1 through t5 High	$t_{WH(t)}$	30	—	—	
MC	$t_{W(MC)}$	30	—	—	
Ref Grant	$t_{W(RG)}$	25	—	—	

Notes: 1. $\overline{Ref.\ Req.}$ has an internal 5.0 kΩ pullup to V_{CC}. If faster propagation delay is required (t_{PTQ}), then an external register can be added in parallel to the internal one to decrease the propagation delay. The value of resistance needed is a function of the capacitive loaded connection to Ref. Reg. The minimum value of R that can be used is 5.0 V/8.0 mA = 625 Ω, assuming there are no other dc loads connected to that pin.

2. If delays between t1–t5 are less than the minimum specified, the succeeding outputs may not switch.

3. All outputs can drive larger capacitive loads than those shown with a small decrease in speed. See Figure 1.

AC LOADS (Note 3)

R/$\overline{W}$ and $\overline{CAS}$ Outputs	450 pF to Gnd*
$\overline{RAS}$ Outputs	150 pF to Gnd*
MC, Row En, Ref En, and $\overline{Ref\ Req}$ Outputs	15 pF to Gnd*

*Includes probe and jig capacitance.

7

PIN DESCRIPTION TABLE

Name	No.	Function
$\overline{RAS1}$ *	16	$\overline{Row\ Address\ Strobe}$ pins which connect to each of the dynamic RAMs to latch in row address on memory chips. Decoded to 1 of 4 during R/W cycle. All 4 go low during refresh cycle.
$\overline{RAS2}$	15	
$\overline{RAS3}$	14	
$\overline{RAS4}$	13	
$\overline{CAS}$ *	11	$\overline{Column\ Address\ Strobe}$ pin which connects to each dynamic RAM to latch in column address.
R/W Out *	10	This pin signals the dynamic RAM whether the RAM is to be read from or written into.
Row En	9	Row Enable output which goes to the MC3232A (MC3242A). It signals the Address Multiplexer that the lower half (Row Addresses) or the upper half (Column Addresses) of the address lines are to be multiplexed into the dynamic RAM address inputs. A Logic 1 on this output indicates the Row Addresses, and a Logic 0 indicates Column Addresses.
Ref En	8	Refresh Enable output. A Logic 1 signals the Address Multiplexer that a refresh cycle is to be done, and a Logic 0 indicates that address multiplexing should be done.
$\overline{CE}$	22	$\overline{Chip\ Enable}$ Input. A Logic 1 on this pin disables all chip functions, except that of Refresh and the $\overline{MC}$ output. $\overline{CE}$ must be low during t1 low to high transition to initiate R/W cycle. Once t1 is initiated, the cycle is independent of $\overline{CE}$.
R/W In	7	The Read/Write input pin receives information from the M6800 MPU as to the direction of data exchange in the dynamic RAM. It transmits a Logic 0 to the R/W output for a Write Cycle and a Logic 1 for a Read Cycle.
A13 (A15)	17	Upper Order Address lines from the M6800. These two inputs decode to four signals controlling the four $\overline{RAS}$ outputs. A14 and A15 apply to 16K RAMs.
A12 (A14)	18	
MC	23	Memory Clock input from MC6875 clock or other signal source. The rising edge of MC must occur after the rising edge of t1 to avoid aborting the refresh cycle. When MC rises, it resets an internal flag that will terminate refresh at the end of the current cycle. Failure to reset the flag forces the 3480 to refresh every cycle thereafter. MC can be connected to t2 or t3 in noncritical applications.
$\overline{MC}$	1	The buffered complement output of MC. It is a buffered output which may be used to drive the circuitry creating the time delays used on inputs t1 through t5.
t1	2	These pins use external timing inputs to sequentially select the outputs to be enabled. They are positive-edge triggered inputs. Assuming a Read/Write cycle is to be executed, a positive edge on t1 forces a logic 0 on one of the four $\overline{RAS}$ outputs as determined by the A12/14, A13/15 inputs. After a delay, a positive edge on t2 causes Row En to go to a Logic 0, providing address-multiplexing information to the MC3232A or MC3242A. t3 enables the $\overline{CAS}$ output and it goes low. t4 enables the R/W output and it goes low, assuming the R/W input was low. t5 resets all the outputs to a Logic 1 (with the exception of $\overline{MC}$, Ref En, and $\overline{Ref\ Req}$). The inputs t1, t2, t3, and t5 are daisy-chained, so they must be sequentially driven to obtain the desired output signals. t4 can be driven at any time after t1.
t2	3	
t3	4	
t4	5	
t5	6	
Ref Clk	21	The 32 kHz (64 kHz) Refresh Clock signals this pin that another refresh cycle is required. It is a positive-edge triggered input, and upon triggering, the $\overline{Ref\ Req}$ pin goes to a Logic 0.
$\overline{Ref\ Req}$	20	The $\overline{Refresh\ Request}$ output acts as an input to the MPU system, requesting a refresh cycle. This output has a 5 kΩ pullup resistor to the V_{CC} supply to allow wire-ORing if desired.
Ref Grant	19	Through the Refresh Grant input, the MC6875 initiates a refresh cycle. This input is positive-edge triggered and is enabled only after the $\overline{Ref\ Req}$ pin has gone low. This allows the MC3480 to discern between a Refresh Grant or a DMA Grant even though they appear on the same line. When employing both dynamic memory (refresh) and DMA in a microprocessor-based system with a combined Refresh/DMA Request control on the clock, provision must be made for holding off a DMA request during a refresh period (and visa versa). If this provision is not made, clock stretching (cycle stealing) will continue indefinitely and dynamic microprocessor data will be lost. The positive edge on Ref Grant causes Row En output to go low and Ref En output to go high. This signals the MC3232A (MC3242A) that a refresh address is required. The refresh cycle occurs with the succeeding pulses on t1-t5. A positive edge on t1 causes $\overline{Ref\ Req}$ to go high and all the $\overline{RAS}$ outputs to go low. A positive going edge on t2 causes no change in the outputs, since it controls the address multiplexing (Row En) during the Read/Write cycles. There is no output change when t3 and t4 go high because no $\overline{CAS}$ or R/W signal is needed during refresh. A positive edge on t5 resets the $\overline{RAS}$ and Row En to a Logic 1 state, and Ref En to a Logic 0 state, ready for the next Read/Write cycle.
V_{CC}	24	+5.0 V supply. A 0.1 μF capacitor is recommended to bypass pin 24 to ground.
Gnd	12	System Ground.

*These outputs are designed to drive the highly capacitive inputs of multiple dynamic RAMs/(150 pF for $\overline{RAS}$ outputs, and 450 pF for $\overline{CAS}$ and R/W outputs). Consequently, these outputs have no short-circuit limit and must be handled accordingly. Good high capacitance load driving techniques usually include a 10 Ω or greater series damping resistor. It is highly recommended that this be done on $\overline{RAS}$, $\overline{CAS}$ and R/W outputs of the MC3480. The effect of these series damping resistors on rise and fall times must be included in timing considerations.

NOTE: All other outputs are LS/TTL totem-pole configuration unless otherwise noted.

TIME DELAY INFORMATION

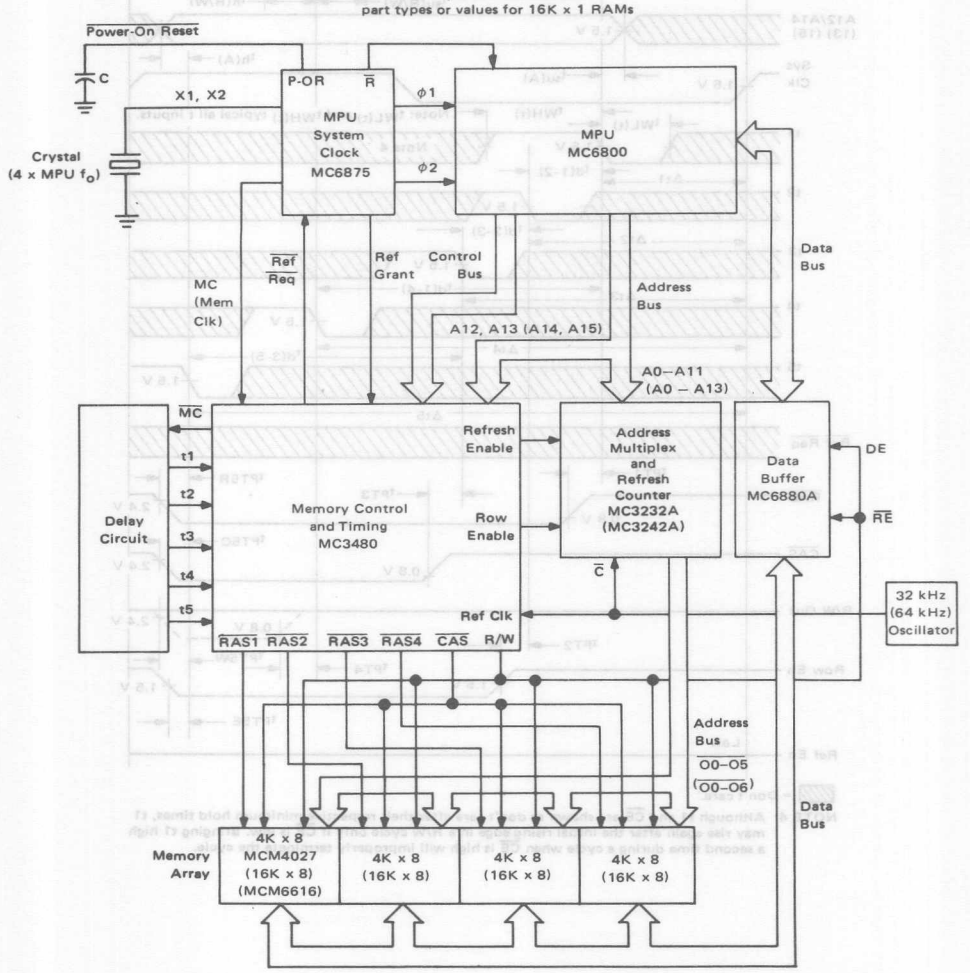
TIMING REQUIREMENT CONSTRAINTS

$\Delta t1$	Minimum is determined by MPU Address Delay (t_{AD}), plus RAM Row Address Set-Up Time (t_{ASR}), minus MC3480 Propagation Delay (t_{PT1}).
$\Delta t2 - \Delta t1$	Minimum is determined by RAM Row Address Hold Time (t_{RAH}) minus the minimum MC3232A/3242A Row Enable to Output Delay (t_{00MIN}).
$\Delta t3 - \Delta t2$	Minimum is determined by RAM Column Address Set-Up Time ($t_{ASC\ minimum}$) plus maximum MC3232A/3242A Row Enable to Output Delay (t_{001MAX}).
$\Delta t4 - \Delta t3$	No Minimum
$\Delta t5 - \Delta t3$	Minimum is determined by RAM minimum $\overline{CAS}$ Pulse Width (t_{CAS}) or Access Time from $\overline{CAS}$ (t_{CAC}) plus Data Set-Up Time of MPU (t_{DSR}).
$\Delta t5 - \Delta t4$	Minimum is determined by the RAM minimum Write Pulse Width (t_{WP}).

Note: Also required in computing time delays are the various delays incurred by the particular delay scheme used; i.e., delays between $4 \times f_o$, $2 \times f_o$, and f_o from the MC6875 which are used as inputs or the gate delays of the gates used in Figures 5A through 5C.

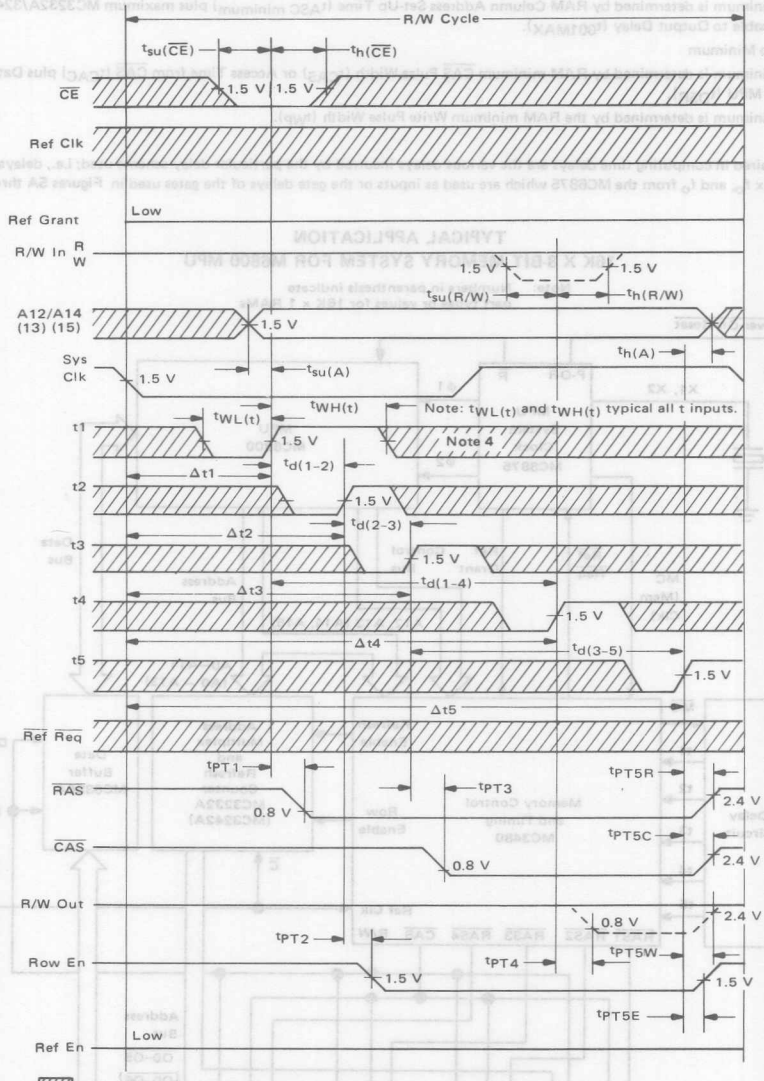
TYPICAL APPLICATION
16K X 8-BIT MEMORY SYSTEM FOR M6800 MPU

Note: Numbers in parenthesis indicate part types or values for 16K x 1 RAMs



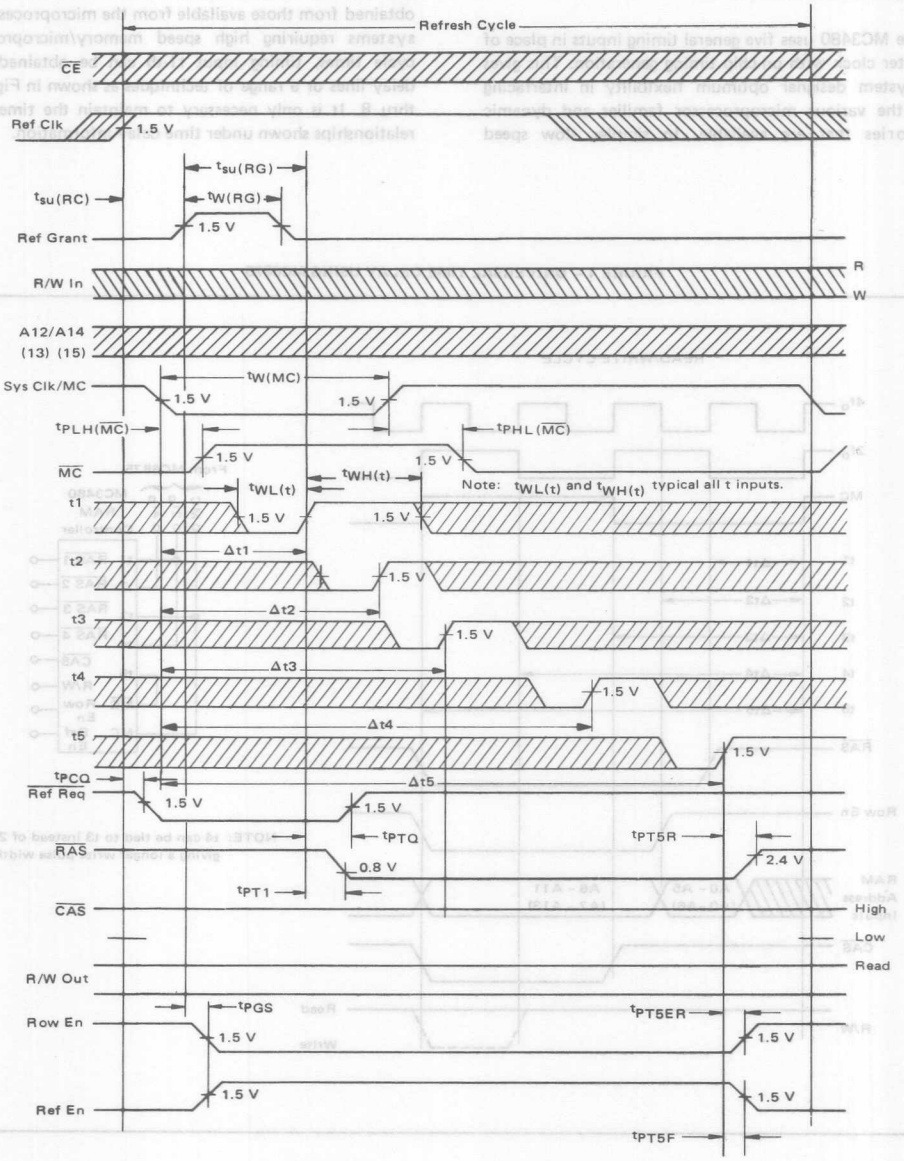
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FIGURE 2 – READ/WRITE TIMING CYCLE



NOTE 4: Although t1 and $\overline{CE}$ are shown as don't care after their respective minimum hold times, t1 may rise again after the initial rising edge in a R/W cycle only if $\overline{CE}$ is low. Bringing t1 high a second time during a cycle when $\overline{CE}$ is high will improperly terminate the cycle.

FIGURE 3 – REFRESH TIMING CYCLE



APPLICATIONS INFORMATION

GENERAL DESCRIPTION

The MC3480 uses five general timing inputs in place of a master clock with on-chip timing generation. This gives the system designer optimum flexibility in interfacing with the various microprocessor families and dynamic memories that are available. In simpler slow speed systems, the timing signals required can be directly obtained from those available from the microprocessor. In systems requiring high speed memory/microprocessor cycle times, timing input t1-t5 can be obtained using delay lines or a range of techniques as shown in Figures 4 thru 8. It is only necessary to maintain the time delay relationships shown under time delay information.

FIGURE 4 – UNIVERSAL TIME DELAY USING MC6875

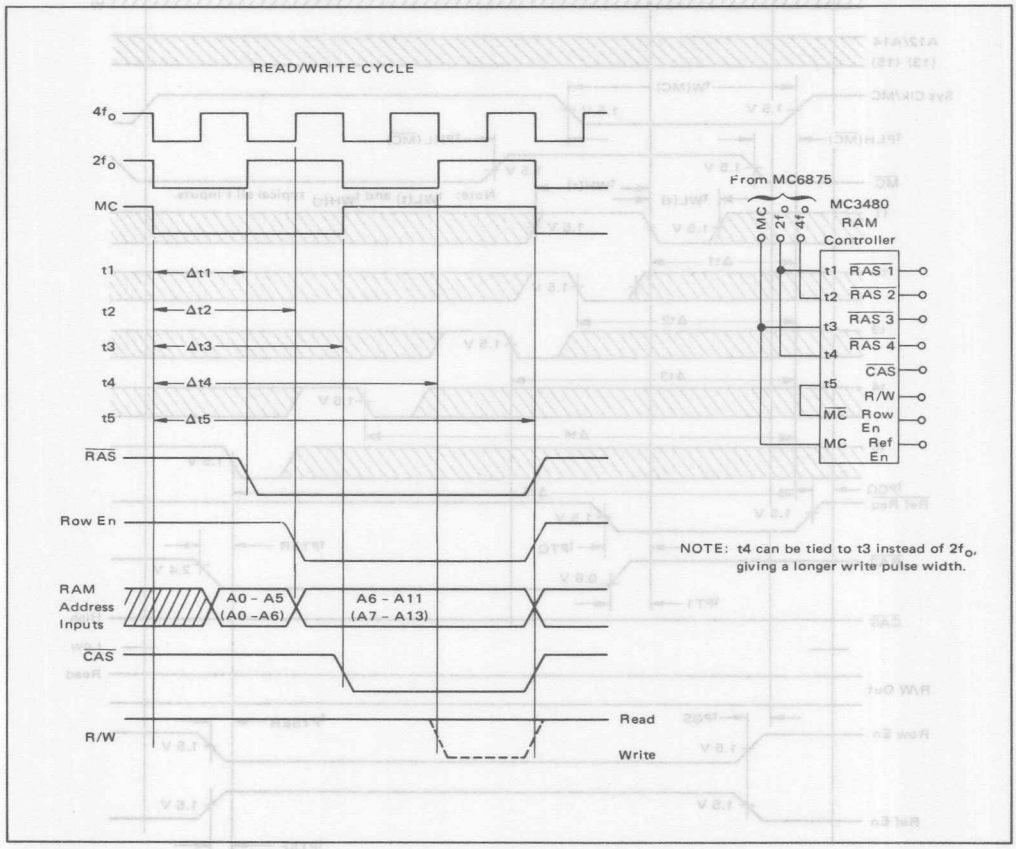
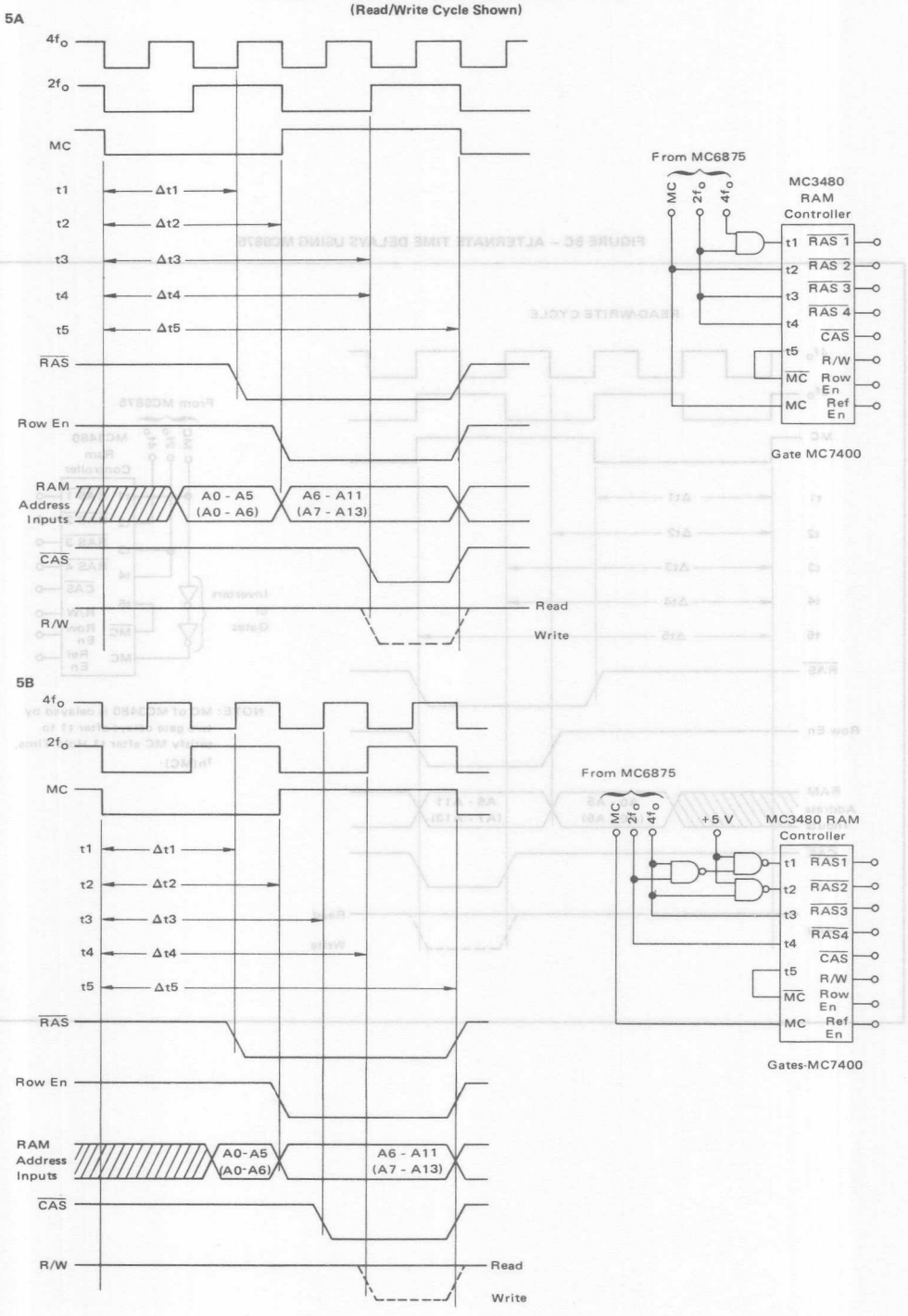
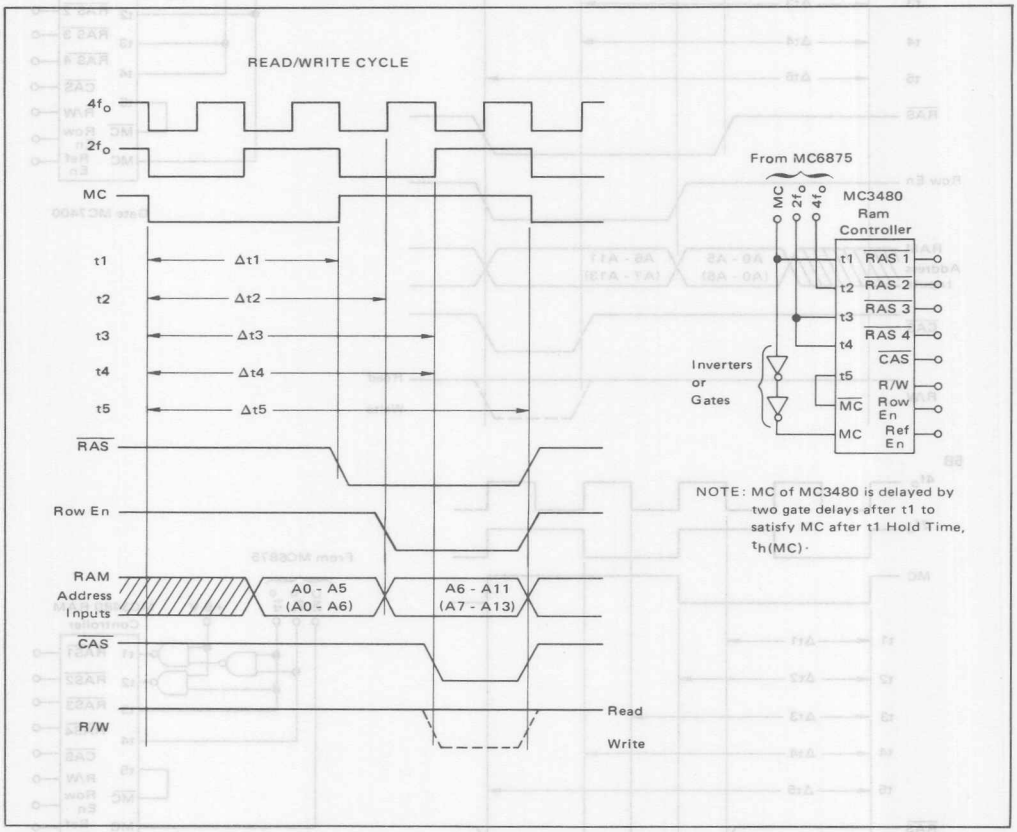


FIGURE 5 – ALTERNATE TIME DELAYS USING MC6875
(Read/Write Cycle Shown)



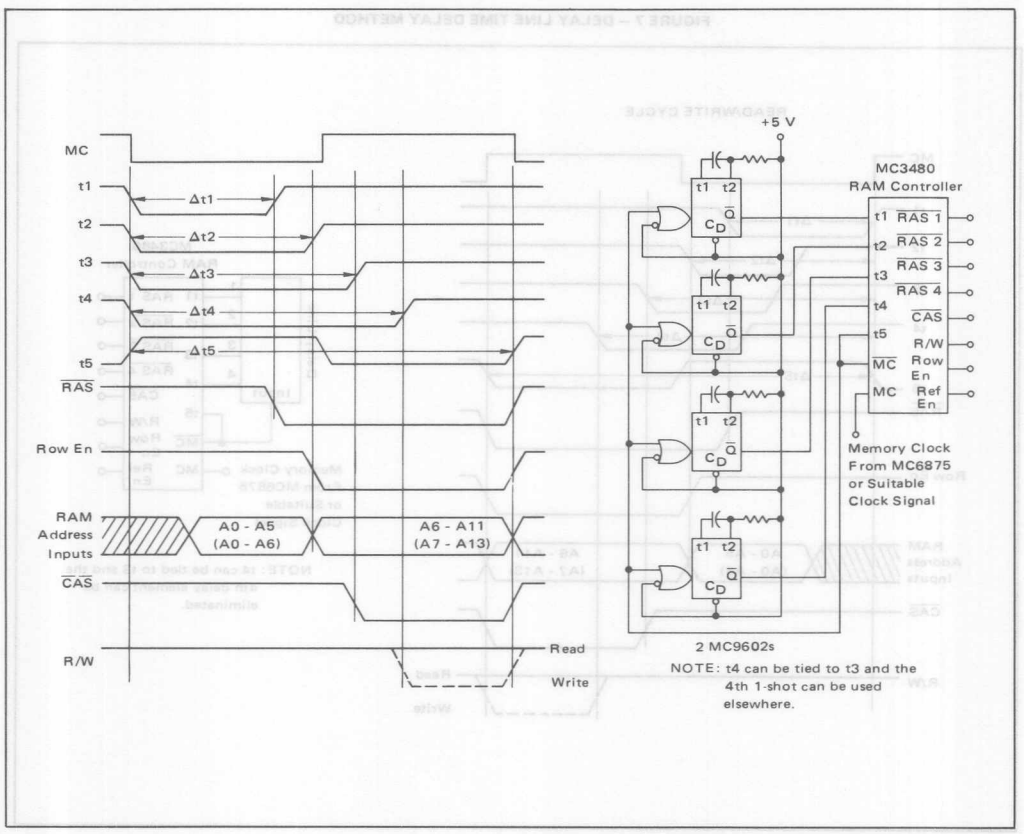
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FIGURE 5C – ALTERNATE TIME DELAYS USING MC6875



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FIGURE 6 – ONE SHOT TIME DELAY METHOD



7

FIGURE 7 – DELAY LINE TIME DELAY METHOD

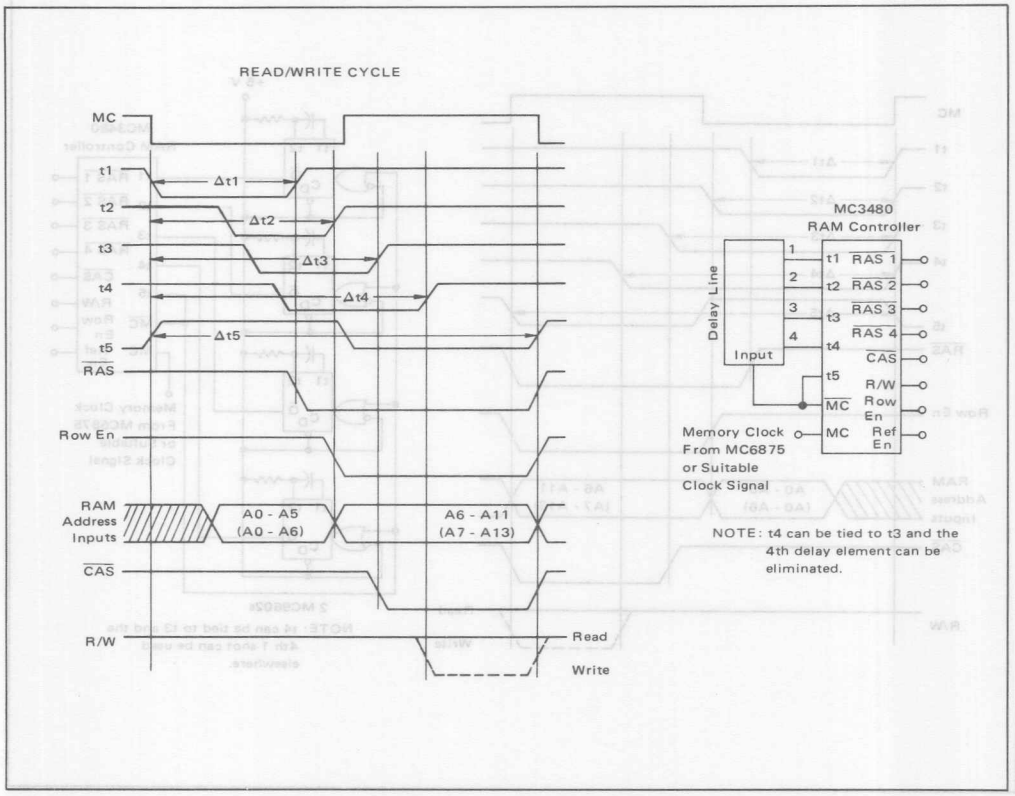
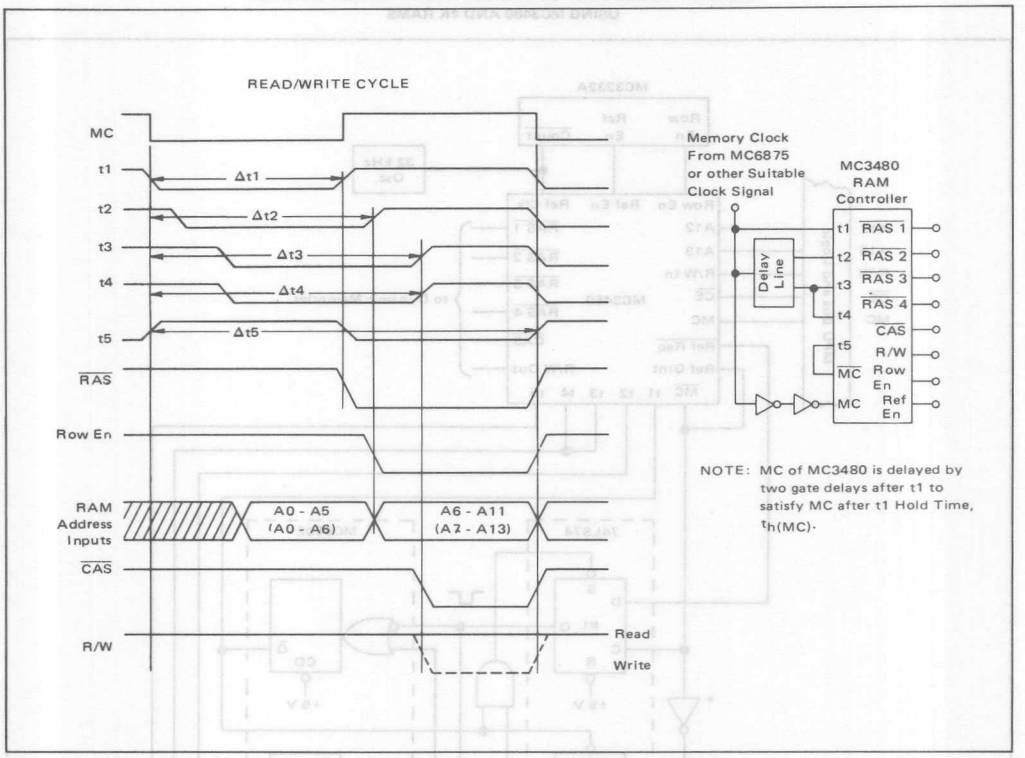


FIGURE 8 – DELAY LINE TIME DELAY (ALTERNATE METHOD)



REFRESH CONSIDERATIONS

The MC3480/MC3232A (MC3242A) memory control system can be used with either cycle steal or transparent refresh methods. Figure 9 shows one transparent technique employing refresh during $\phi 2$ low in an M6800 microprocessor-based system. Using this technique requires that the memory be capable of completing a Read/Write Cycle and a Refresh Cycle sequentially during the M6800 cycle. The minimum cycle time at the time of printing for dynamic multiplexed RAMs is 320 ns, therefore limiting the microprocessor to 1.56 MHz operation. The D flip-flops of Figure 9 produce a trigger at the beginning of both $\phi 1$ and $\phi 2$. For a 1.0 MHz system, the t1 – t5 inputs should be adjusted for the following delays:

$\overline{RAS}$ falls at 150 ns (triggered by t1)
Row En falls at 250 ns (triggered by t2)
$\overline{CAS}$, R/W falls at 300 ns (triggered by t3)
t5 rises at 500 ns.

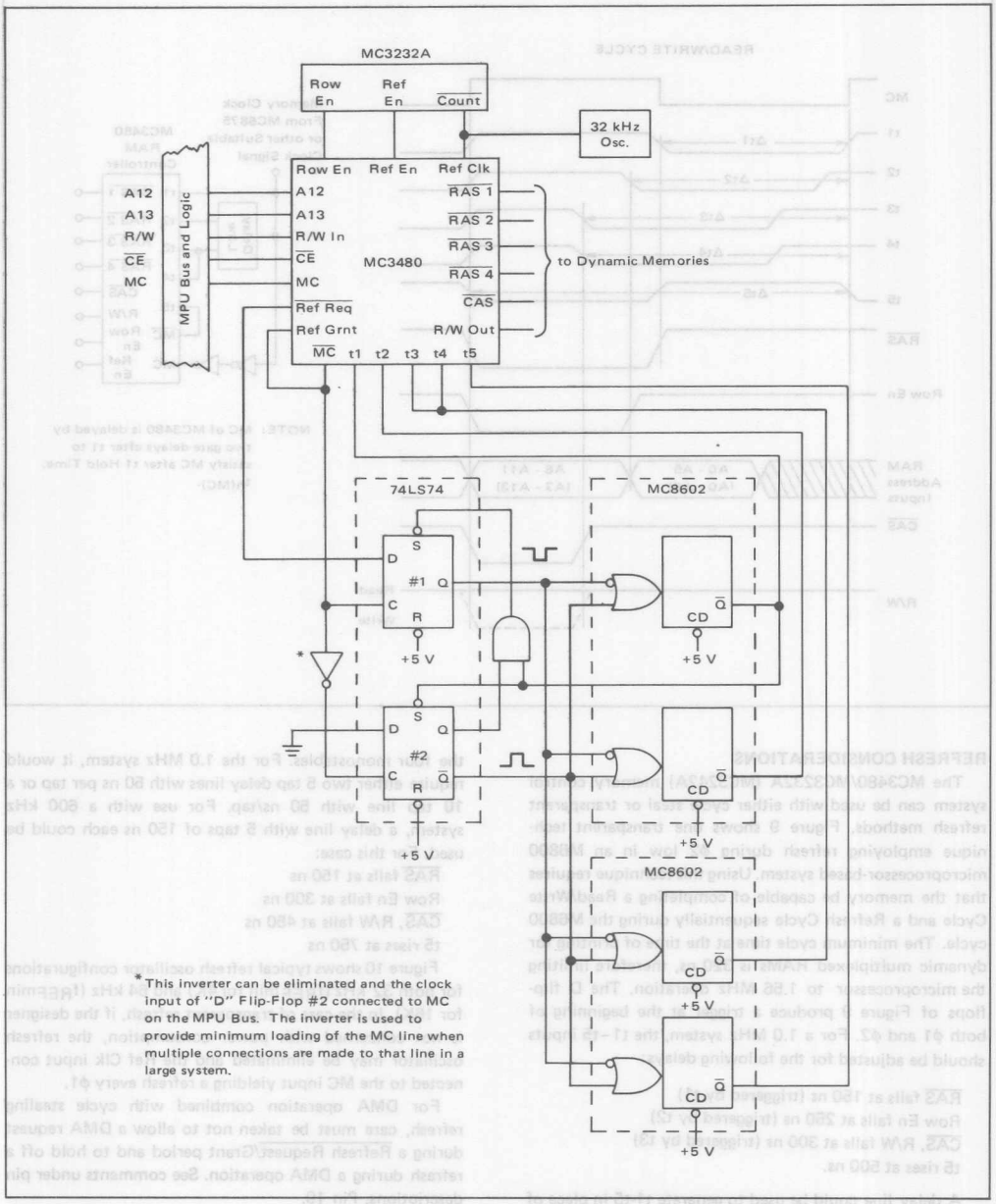
A delay line could be used to generate t1-t5 in place of the four monostables. For the 1.0 MHz system, it would require either two 5 tap delay lines with 50 ns per tap or a 10 tap line with 50 ns/tap. For use with a 600 kHz system, a delay line with 5 taps of 150 ns each could be used. For this case:

$\overline{RAS}$ falls at 150 ns
Row En falls at 300 ns
$\overline{CAS}$, R/W falls at 450 ns
t5 rises at 750 ns

Figure 10 shows typical refresh oscillator configurations for both 32 kHz (f_{REF} min for 4K) and 64 kHz (f_{REF} min for 16K). In the case of transparent refresh, if the designer is not concerned with power consumption, the refresh oscillator may be eliminated and the Ref Clk input connected to the MC input yielding a refresh every $\phi 1$.

For DMA operation combined with cycle stealing refresh, care must be taken not to allow a DMA request during a $\overline{\text{Refresh Request}}$/Grant period and to hold off a refresh during a DMA operation. See comments under pin descriptions, Pin 19.

FIGURE 9 – EXAMPLE OF $\phi 2$ LOW METHOD OF HIDDEN REFRESH USING MC3480 AND 4K RAMS



MOTOROLA

MC3481
MC3485

IBM 360/370 QUAD LINE DRIVER

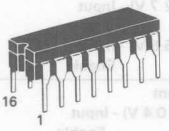
SILICON MONOLITHIC
INTEGRATED CIRCUIT

QUAD SINGLE-ENDED LINE DRIVER

The MC3481 and MC3485 are quad single-ended line drivers specifically designed to meet the IBM 360/370 I/O specification (GA22-6974-3).

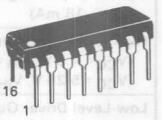
Output levels are guaranteed over the full range of output load and fault conditions. Compliance with the IBM requirements for fault protection, flagging, and power up/power down protection for the bus make this an ideal line driver for party line operations.

- Separate Enable and Fault Flags — MC3481
- Common Enable and Fault Flag — MC3485
- Power Up/Down Does Not Disturb Bus
- Schottky Circuitry for High-Speed — PNP Inputs
- Internal Bootstraps for Faster Rise Times
- Driver Output Current Foldback Protection
- MC3485 has LS Totem Pole Driver Output



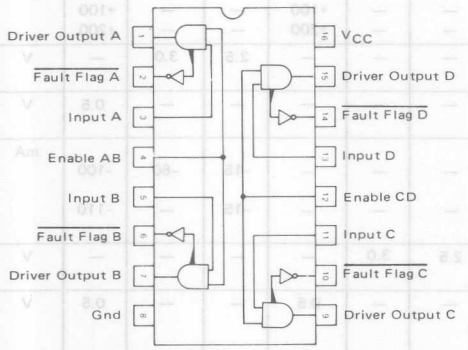
L SUFFIX
CERAMIC PACKAGE
CASE 620-10

P SUFFIX
PLASTIC PACKAGE
CASE 648-06

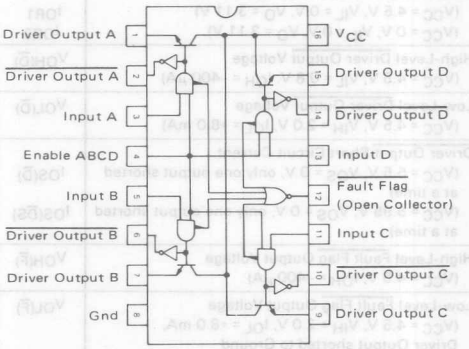


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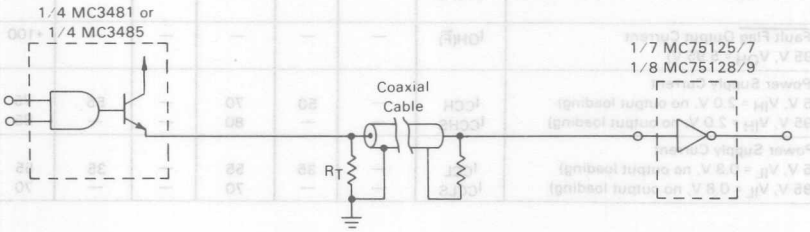
MC3481
DUAL ENABLE
INDIVIDUAL FAULT FLAG



MC3485
COMMON ENABLE
COMMON FAULT FLAG



TYPICAL APPLICATION



RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.95	Vdc
High Level Output Current	I_{OH}	—	—	-59.3	mA
Operating Ambient Temperature Range	T_A	0	—	+70	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, these specifications apply over recommended power supply and temperature ratings. Typical values measured at T_A = 25°C and V_{CC} = +5.0 V)

Characteristic	Symbol	MC3481 Min	MC3481 Typ	MC3481 Max	MC3485 Min	MC3485 Typ	MC3485 Max	Unit
High-Level Input Voltage Note 2	V_{IH}	2.0	—	—	2.0	—	—	V
Low-Level Input Voltage Note 2	V_{IL}	—	—	0.8	—	—	0.8	V
High-Level Input Current	I_{IH}							μA
(V_{CC} = 4.5 V, V_{IH} = 2.7 V) - Input		—	—	20	—	—	20	
Enable		—	—	40	—	—	80	
(V_{CC} = 4.5 V, V_{IH} = 5.5 V) - Input		—	—	100	—	—	100	
Enable		—	—	200	—	—	400	
Low-Level Input Current	I_{IL}							μA
(V_{CC} = 5.95 V, V_{IL} = 0.4 V) - Input		—	—	-250	—	—	-250	
Enable		—	—	-500	—	—	-1000	
Input Clamp Voltage (I_{IC} = -18 mA)	V_{IC}	—	—	-1.5	—	—	-1.5	V
High-Level Driver Output Voltage								V
(V_{CC} = 4.5 V, V_{IH} = 2.0 V, I_{OH} = -59.3 mA)	$V_{OH(D)}$	3.11	3.6	—	3.11	3.6	—	
(V_{CC} = 5.25 V, V_{IH} = 2.0 V, I_{OH} = -41 mA)	$V_{OH(DS)}$	3.9	—	—	3.9	—	—	
Low-Level Driver Output Voltage								V
(V_{CC} = 5.5 V, V_{IL} = 0.8 V, I_{OL} = -240 μA)	$V_{OL(D)}$	—	—	+0.15	—	—	+0.15	
(V_{CC} = 5.95 V, V_{IL} = 0.8 V, I_{OL} = -1.0 mA)	$V_{OL(DS)}$	—	—	+0.15	—	—	+0.15	
Driver Output Short Circuit Current								mA
(V_{CC} = 5.5 V, V_{IH} = 2.0 V, V_{OS} = 0 V)	$I_{OS(D)}$	—	—	-5.0	—	—	-5.0	
(V_{CC} = 5.95 V, V_{IH} = 2.0 V, V_{OS} = 0 V)	$I_{OS(DS)}$	—	—	-5.0	—	—	-5.0	
Driver Output Reverse Leakage Current								μA
(V_{CC} = 4.5 V, V_{IL} = 0 V, V_O = 3.11 V)	I_{OR1}	—	—	+100	—	—	+100	
(V_{CC} = 0 V, V_{IL} = 0 V, V_O = 3.11 V)	I_{OR2}	—	—	+200	—	—	+200	
High-Level $\overline{\text{Driver Output}}$ Voltage (V_{CC} = 4.5 V, V_{IL} = 0.8 V, I_{OH} = -400 μA)	$V_{OH(\overline{D})}$	—	—	—	2.5	3.0	—	V
Low-Level $\overline{\text{Driver Output}}$ Voltage (V_{CC} = 4.5 V, V_{IH} = 2.0 V, I_{OL} = +8.0 mA)	$V_{OL(\overline{D})}$	—	—	—	—	—	0.5	V
$\overline{\text{Driver Output}}$ Short Circuit Current								mA
(V_{CC} = 5.5 V, V_{OS} = 0 V, only one output shorted at a time)	$I_{OS(\overline{D})}$	—	—	—	-15	-60	-100	
(V_{CC} = 5.95 V, V_{OS} = 0 V, only one output shorted at a time)	$I_{OS(\overline{D}S)}$	—	—	—	-15	—	-110	
High-Level $\overline{\text{Fault Flag}}$ Output Voltage (V_{CC} = 4.5 V, I_{OH} = -400 μA)	$V_{OH(\overline{F})}$	2.5	3.0	—	—	—	—	V
Low-Level $\overline{\text{Fault Flag}}$ Output Voltage (V_{CC} = 4.5 V, V_{IH} = 2.0 V, I_{OL} = +8.0 mA, Driver Output shorted to Ground	$V_{OL(\overline{F})}$	—	—	0.5	—	—	0.5	V
$\overline{\text{Fault Flag}}$ Output Short Circuit Current								mA
(V_{CC} = 5.5 V, V_{OS} = 0 V, only one output shorted at a time)	$I_{OS(\overline{F})}$	-15	—	-100	—	—	—	
(V_{CC} = 5.95 V, V_{OS} = 0 V, only one output shorted at a time)	$I_{OS(\overline{F}S)}$	-15	—	-110	—	—	—	
High-Level $\overline{\text{Fault Flag}}$ Output Current (V_{CC} = 5.95 V, V_{OH} = 5.95 V)	$I_{OH(\overline{F})}$	—	—	—	—	—	+100	μA
High-Level Power Supply Current								mA
(V_{CC} = 5.5 V, V_{IH} = 2.0 V, no output loading)	I_{CCH}	—	50	70	—	55	75	
(V_{CC} = 5.95 V, V_{IH} = 2.0 V, no output loading)	I_{CCHS}	—	—	80	—	—	85	
Low-Level Power Supply Current								mA
(V_{CC} = 5.5 V, V_{IL} = 0.8 V, no output loading)	I_{CCL}	—	35	55	—	35	55	
(V_{CC} = 5.95 V, V_{IL} = 0.8 V, no output loading)	I_{CCLS}	—	—	70	—	—	70	

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating		Symbol	Value	Unit
Power Supply Voltage		V_{CC}	+7.0	V
Input Voltage		V_I	10	V
Driver Output Voltage		V_O	5.5	V
Power Dissipation (Package Limitation)	Ceramic Package Plastic Package	P_D	1150 962	mW
Derate Above T_A = 25°C		$1/R_{\theta JA}$	7.7	mW/°C
Operating Ambient Temperature Range		T_A	0 to +70	°C
Junction Temperature	Ceramic Package Plastic Package	T_J	+175 +150	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

SWITCHING CHARACTERISTICS (See Note 1. Unless otherwise noted, these specifications apply over recommended temperature range. I/O Driver characteristics are guaranteed for V_{CC} = 5.0 V ±10% and Select-Out Driver characteristics are guaranteed for V_{CC} = 5.25 to 5.95 V. Typical values measured at T_A = 25°C and V_{CC} = 5.0 V. See Tables 1 and 2, Figures 1 and 2 for load conditions.)

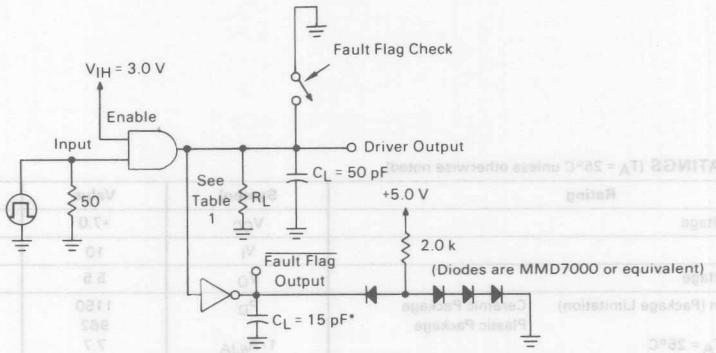
Characteristics	Symbol	Min	Typ	Max	Unit
Propagation Delay Time					ns
High-to-Low-Level, Driver Output					
As I/O Driver	$t_{PHL(D)}$	—	18	—	
As Select-Out Driver	$t_{PHL(DS)}$	—	19	—	
Low-to-High-Level, Driver Output					
As I/O Driver	$t_{PLH(D)}$	—	20	—	
As Select-Out Driver	$t_{PLH(DS)}$	—	21	—	
High-to-Low-Level, $\overline{\text{Driver Output}}$					
As I/O Driver	$t_{PHL(\overline{D})}$	—	25	—	
As Select-Out Driver	$t_{PHL(\overline{D}S)}$	—	26	—	
Low-to-High-Level, $\overline{\text{Driver Output}}$					
As I/O Driver	$t_{PLH(\overline{D})}$	—	25	—	
As Select-Out Driver	$t_{PLH(\overline{D}S)}$	—	26	—	
High-to-Low-Level, $\overline{\text{Fault Flag}}$ — MC3481					
As I/O Driver	$t_{PHL(\overline{F})}$	—	45	—	
As Select-Out Driver	$t_{PHL(\overline{F}S)}$	—	47	—	
Low-to-High-Level, $\overline{\text{Fault Flag}}$ — MC3481					
As I/O Driver	$t_{PLH(\overline{F})}$	—	40	—	
As Select-Out Driver	$t_{PLH(\overline{F}S)}$	—	42	—	
Ratio of Propagation Delay Times As I/O Driver	$\frac{t_{PLH(D)}}{t_{PHL(D)}}$	—	1.0	—	

Note 1. Reference IBM specification GA22-6974-3 for test terminology.

2. The fault protection circuitry of the MC3481/85 requires relatively clean input voltage waveforms for current operation. Noise pulses which enter the threshold region (0.8 to 2.0 V) may cause the output to enter the fault protect mode. To exit the protect mode, it is necessary to gate an input of the effected driver to the low logic state.

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FIGURE 1 — MC3481 AC TEST CIRCUIT AND WAVEFORMS



* Load Capacitance shown includes Fixture and Probe Capacitance

Table 1	Driver Application	
	I/O	Select-Out
V_{OH}	3.11 V	3.9 V
Input Frequency	5 MHz	1 MHz
Input Pulse Width	100 ns	500 ns
Input Amplitude	0 V to 4 V	0 V to 4 V
Input t_{TLH}	≤6 ns	≤ 6 ns
Input t_{THL}	≤6 ns	≤6 ns
Load Resistance (R_L)	50	90

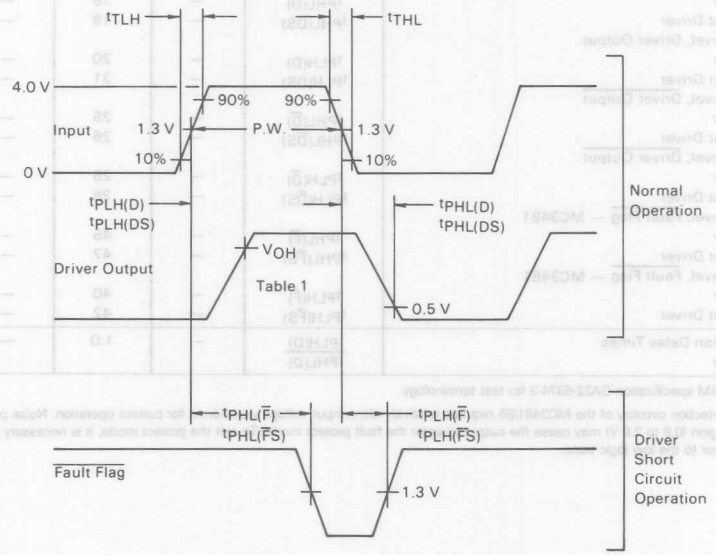


FIGURE 2 — MC3485 AC TEST CIRCUIT AND WAVEFORMS

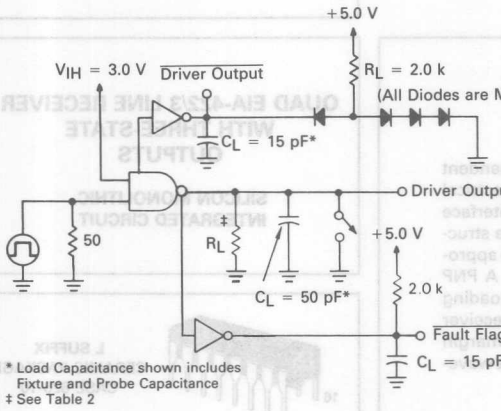
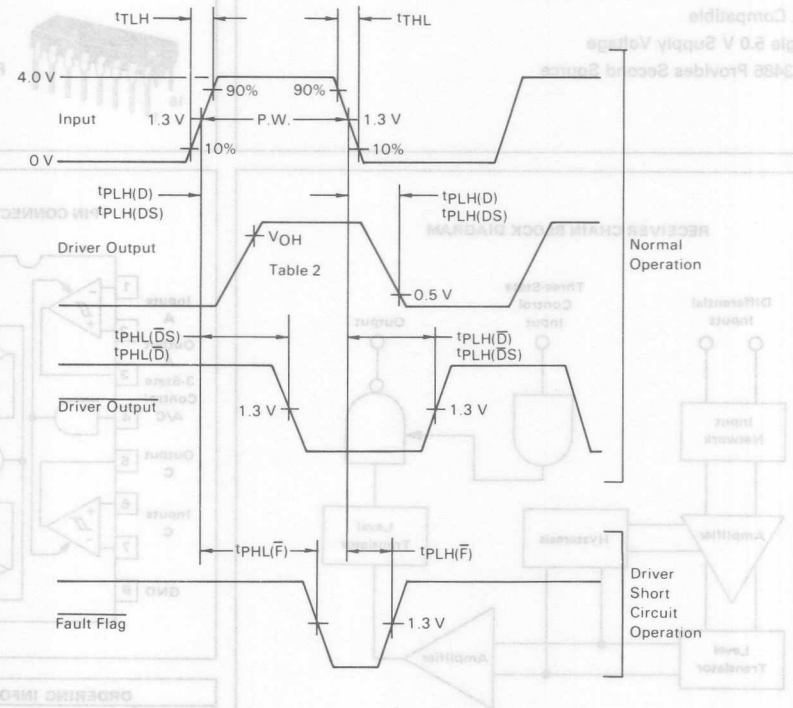


Table 2	Driver Application	
	I/O	Select-Out
V_{OH}	3.11 V	3.9 V
Input Frequency	5 MHz	1 MHz
Input Pulse Width	100 ns	500 ns
Input Amplitude	0 V to 4 V	0 V to 4 V
Input t_{TLH}	≤6 ns	≤6 ns
Input t_{THL}	≤6 ns	≤6 ns
Load Resistance (R_L)	50	90



MOTOROLA

MC3486

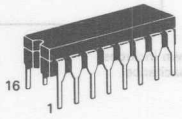
QUAD EIA-422/423 LINE RECEIVER

Motorola's Quad EIA-422/3 Receiver features four independent receiver chains which comply with EIA Standards for the Electrical Characteristics of Balanced/Unbalanced Voltage Digital Interface Circuits. Receiver outputs are 74LS compatible, three-state structures which are forced to a high impedance state when the appropriate output control pin reaches a logic zero condition. A PNP device buffers each output control pin to assure minimum loading for either logic one or logic zero inputs. In addition, each receiver chain has internal hysteresis circuitry to improve noise margin and discourage output instability for slowly changing input waveforms. A summary of MC3486 features include:

- Four Independent Receiver Chains
- Three-State Outputs
- High Impedance Output Control Inputs (PIA Compatible)
- Internal Hysteresis – 30 mV (Typ) @ Zero Volts Common Mode
- Fast Propagation Times – 25 ns (Typ)
- TTL Compatible
- Single 5.0 V Supply Voltage
- DS 3486 Provides Second Source

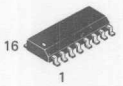
QUAD EIA-422/3 LINE RECEIVER WITH THREE-STATE OUTPUTS

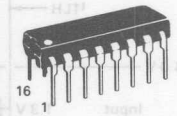
SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 620-10

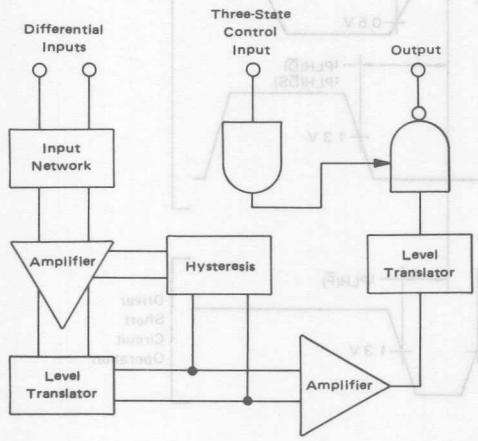
D SUFFIX
PLASTIC PACKAGE
CASE 751B-03
SO-16



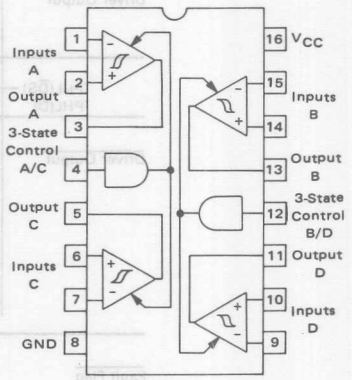


P SUFFIX
PLASTIC PACKAGE
CASE 648-06

RECEIVER CHAIN BLOCK DIAGRAM



PIN CONNECTIONS



ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE
MC3486L	0 to +70°C	Ceramic DIP
MC3486P	0 to +70°C	Plastic DIP

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.0	Vdc
Input Common Mode Voltage	V_{ICM}	±15	Vdc
Input Differential Voltage	V_{ID}	±25	Vdc
Three-State Control Input Voltage	V_I	8.0	Vdc
Output Sink Current	I_O	50	mA
Storage Temperature	T_{stg}	-65 to +150	°C
Operating Junction Temperature Ceramic Package Plastic Package	T_J	 +175 +150	°C

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	4.75 to 5.25	Vdc
Operating Ambient Temperature	T_A	0 to +70	°C
Input Common Mode Voltage Range	V_{ICR}	-7.0 to +7.0	Vdc
Input Differential Voltage Range	V_{IDR}	6.0	Vdc

ELECTRICAL CHARACTERISTICS (Unless otherwise noted minimum and maximum limits apply over recommended temperature and power supply voltage ranges. Typical values are for T_A = 25°C, V_{CC} = 5.0 V and V_{IK} = 0 V. See Note 1.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage — High Logic State (Three-State Control)	V_{IH}	2.0	—	—	V
Input Voltage — Low Logic State (Three-State Control)	V_{IL}	—	—	0.8	V
Differential Input Threshold Voltage, Note 2 (−7.0 V ≤ V_{IC} ≤ 7.0 V, V_{IH} = 2.0 V) (I_O = −0.4 mA, V_{OH} ≥ 2.7 V) (I_O = 8.0 mA, V_{OL} ≥ 0.5 V)	$V_{TH(D)}$	 — —	 — —	 0.2 −0.2	V
Input Bias Current (V_{CC} = 0 V or 5.25) (Other Inputs at 0 V) (V_I = −10 V) (V_I = −3.0 V) (V_I = +3.0 V) (V_I = +10 V)	$I_{IB(D)}$	 — — — —	 — — — —	 −3.25 −1.50 +1.50 +3.25	mA
Input Balance and Output Level (−7.0 V ≤ V_{IC} ≤ 7.0 V, V_{IH} = 2.0 V, Note 3) (I_O = −0.4 mA, V_{ID} = 0.4 V) (I_O = 8.0 mA, V_{ID} = −0.4 V)	 V_{OH} V_{OL}	 2.7 —	 — —	 — 0.5	V
Output Third State Leakage Current ($V_{I(D)}$ = +3.0 V, V_{IL} = 0.8 V, V_{OL} = 0.5 V) ($V_{I(D)}$ = −3.0 V, V_{IL} = 0.8 V, V_{OH} = 2.7 V)	I_{OZ}	 — —	 — —	 −40 40	μA
Output Short-Circuit Current ($V_{I(D)}$ = 3.0 V, V_{IH} = 2.0 V, V_O = 0 V, Note 4)	I_{OS}	−15	—	−100	mA
Input Current — Low Logic State (Three-State Control) (V_{IL} = 0.5 V)	I_{IL}	—	—	−100	μA
Input Current — High Logic State (Three-State Control) (V_{IH} = 2.7 V) (V_{IH} = 5.25 V)	I_{IH}	 — —	 — —	 20 100	μA
Input Clamp Diode Voltage (Three-State Control) (I_{IK} = −10 mA)	V_{IK}	—	—	−1.5	V
Power Supply Current (V_{IL} = 2.0 V)	I_{CC}	—	—	85	mA

NOTES:
1. All currents into device pins are shown as positive, out of device pins are negative. All voltages referenced to ground unless otherwise noted.
2. Differential input threshold voltage and guaranteed output levels are done simultaneously for worst case.
3. Refer to EIA-422/3 for exact conditions. Input balance and guaranteed output levels are done simultaneously for worst case.
4. Only one output at a time should be shorted.

7

Propagation Delay Time — Differential Inputs to Output					ns
(Output High to Low)	$t_{PHL(D)}$	–	–	35	
(Output Low to High)	$t_{PLH(D)}$	–	–	30	
Propagation Delay time — Three-State Control to Output					ns
(Output Low to Third State)	t_{PLZ}	–	–	35	
(Output High to Third State)	t_{PHZ}	–	–	35	
(Output Third State to High)	t_{PZH}	–	–	30	
(Output Third State to Low)	t_{PZL}	–	–	30	

FIGURE 1 — SWITCHING TEST CIRCUIT AND WAVEFORMS

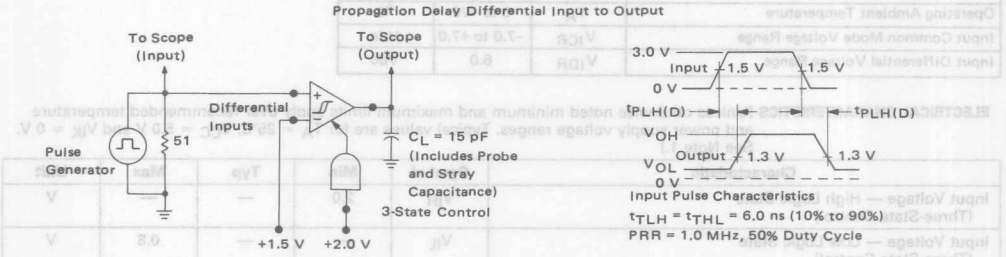
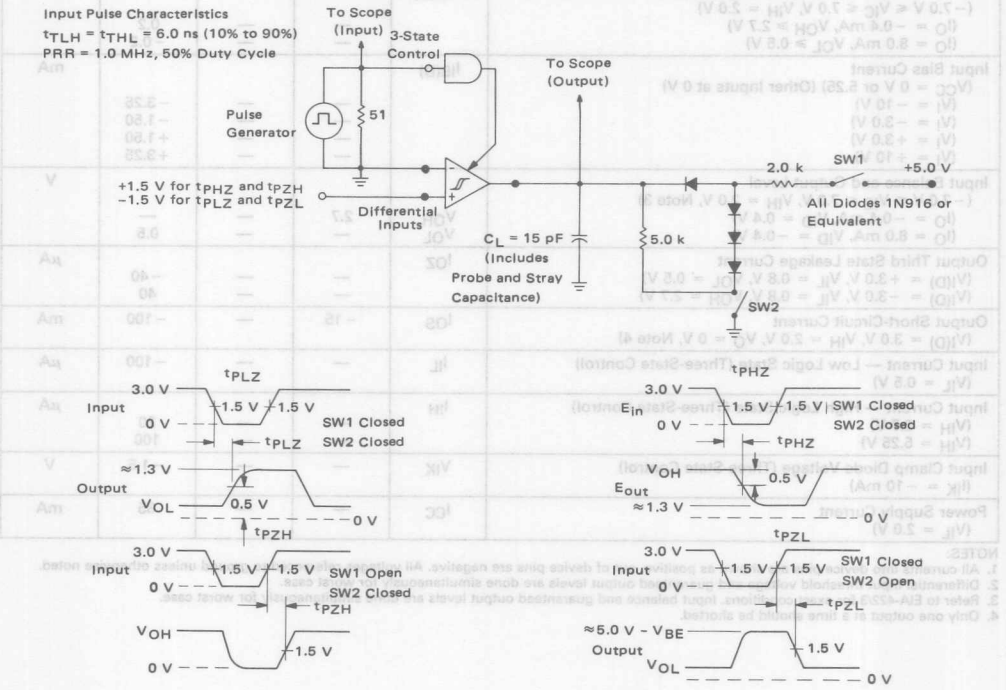


FIGURE 2 — PROPAGATION DELAY THREE-STATE CONTROL INPUT TO OUTPUT



MOTOROLA

MC3487

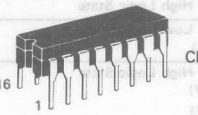
QUAD EIA-422 LINE DRIVER WITH THREE-STATE OUTPUTS

SILICON MONOLITHIC INTEGRATED CIRCUIT

QUAD LINE DRIVER WITH THREE-STATE OUTPUTS

Motorola's Quad EIA-422 Driver features four independent driver chains which comply with EIA Standards for the Electrical Characteristics of Balanced Voltage Digital Interface Circuits. The outputs are three-state structures which are forced to a high impedance state when the appropriate output control pin reaches a logic zero condition. All input pins are PNP buffered to minimize input loading for either logic one or logic zero inputs. In addition, internal circuitry assures a high impedance output state during the transition between power up and power down. A summary of MC3487 features include:

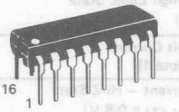
- Four Independent Driver Chains
- Three-State Outputs
- PNP High Impedance Inputs (PIA Compatible)
- Fast Propagation Times (Typ 15 ns)
- TTL Compatible
- Single 5 V Supply Voltage
- Output Rise and Fall Times Less Than 20 ns
- DS 3487 Provides Second Source



L SUFFIX
CERAMIC PACKAGE
CASE 620-10

D SUFFIX
PLASTIC PACKAGE
CASE 751B-03
SO-16

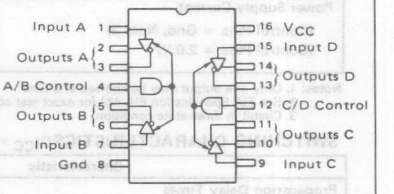




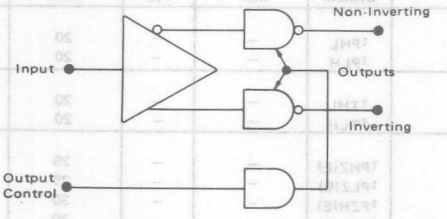
P SUFFIX
PLASTIC PACKAGE
CASE 648-06

7

PIN CONNECTIONS



DRIVER BLOCK DIAGRAM



TRUTH TABLE

Input	Control Input	Non-Inverting Output	Inverting Output
H	H	H	L
L	H	L	H
X	L	Z	Z

L = Low Logic State
H = High Logic State
X = Irrelevant
Z = Third-State (High Impedance)

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.0	Vdc
Input Voltage	V_I	5.5	Vdc
Operating Ambient Temperature Range	T_A	0 to +70	°C
Operating Junction Temperature Range Ceramic Package Plastic Package	T_J	 175 150	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted specifications apply 4.75 V ≤ V_{CC} ≤ 5.25 V and 0°C ≤ T_A ≤ 70°C. Typical values measured at V_{CC} = 5.0 V, and T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage – Low Logic State	V_{IL}	–	–	0.8	Vdc
Input Voltage – High Logic State	V_{IH}	2.0	–	–	Vdc
Input Current – Low Logic State (V_{IL} = 0.5 V)	I_{IL}	–	–	-400	μA
Input Current – High Logic State (V_{IH} = 2.7 V) (V_{IH} = 5.5 V)	I_{IH}	 – –	 – –	 +50 +100	μA
Input Clamp Voltage (I_{IK} = -18 mA)	V_{IK}	–	–	-1.5	V
Output Voltage – Low Logic State (I_{OL} = 48 mA)	V_{OL}	–	–	0.5	V
Output Voltage – High Logic State (I_{OH} = -20 mA)	V_{OH}	2.5	–	–	V
Output Short-Circuit Current (V_{IH} = 2.0 V, Note 1)	I_{OS}	-40	–	-140	mA
Output Leakage Current – Hi-Z State (V_{IL} = 0.5 V, $V_{IL(Z)}$ = 0.8 V) (V_{IH} = 2.7 V, $V_{IL(Z)}$ = 0.8 V)	$I_{OL(Z)}$	 – –	 – –	 ±100 ±100	μA
Output Leakage Current – Power OFF (V_{OH} = 6.0 V, V_{CC} = 0 V) (V_{OL} = -0.25 V, V_{CC} = 0 V)	$I_{OL(off)}$	 – –	 – –	 +100 -100	μA
Output Offset Voltage Difference (Note 2)	$V_{OS} - \overline{V}_{OS}$	–	–	±0.4	V
Output Differential Voltage (Note 2)	V_{OD}	2.0	–	–	V
Output Differential Voltage Difference (Note 2)	$\lvert\Delta V_{OD}\rvert$	–	–	±0.4	V
Power Supply Current (Control Pins = Gnd, Note 3) (Control Pins = 2.0 V)	 I_{CCX} I_{CC}	 – –	 – –	 105 85	mA

Notes: 1. Only one output may be shorted at a time.
2. See EIA Specification EIA-422 for exact test conditions.
3. Circuit in three-state condition.

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Times High to Low Output Low to High Output	 t_{PHL} t_{PLH}	 – –	 – –	 20 20	ns
Output Transition Times – Differential High to Low Output Low to High Output	 t_{THL} t_{TLH}	 – –	 – –	 20 20	ns
Propagation Delay – Control to Output (R_L = 200 Ω, C_L = 50 pF) (R_L = 200 Ω, C_L = 50 pF) (R_L = ∞, C_L = 50 pF) (R_L = 200 Ω, C_L = 50 pF)	 $t_{PHZ(E)}$ $t_{PLZ(E)}$ $t_{PZH(E)}$ $t_{PZL(E)}$	 – – – –	 – – – –	 25 25 30 30	ns

FIGURE 1 – THREE-STATE ENABLE TEST CIRCUIT AND WAVEFORMS

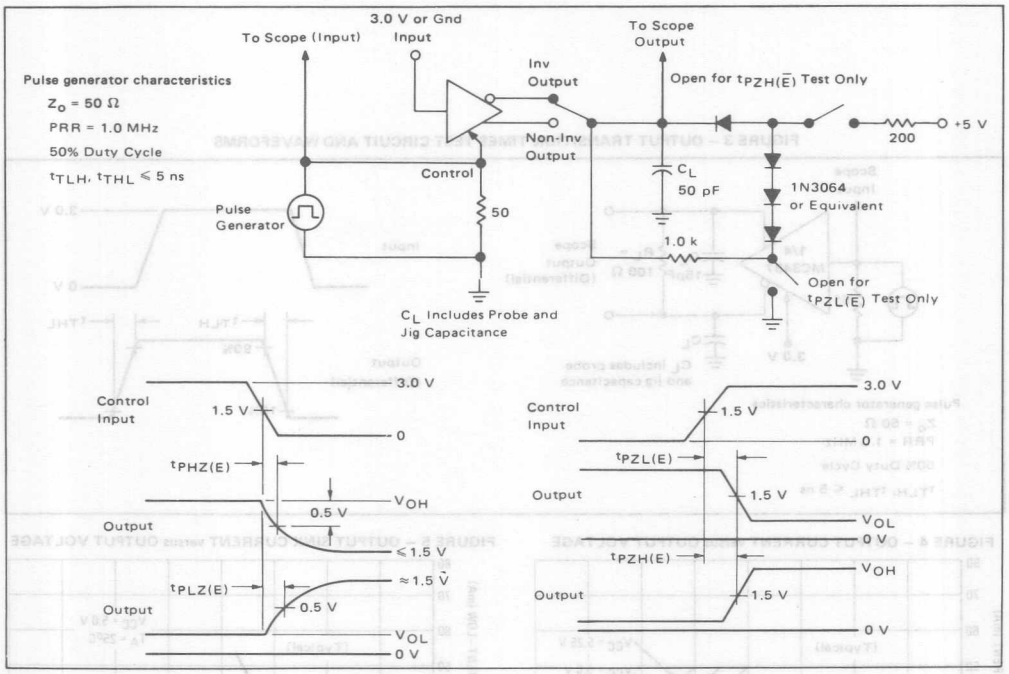
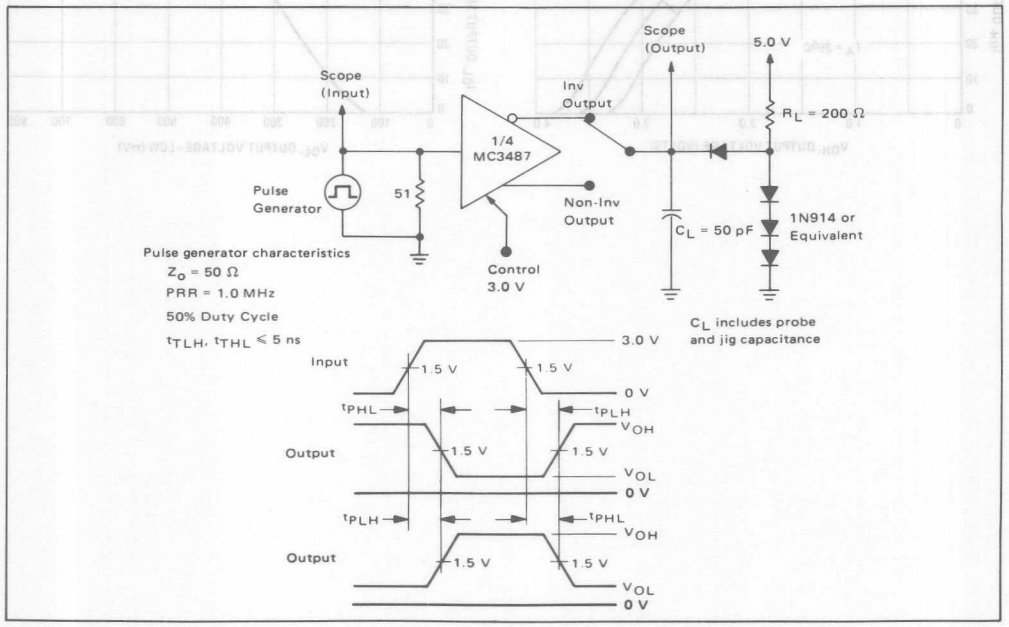


FIGURE 2 – PROPAGATION DELAY TIMES INPUT TO OUTPUT WAVEFORMS AND TEST CIRCUIT



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FIGURE 3 – OUTPUT TRANSITION TIMES TEST CIRCUIT AND WAVEFORMS

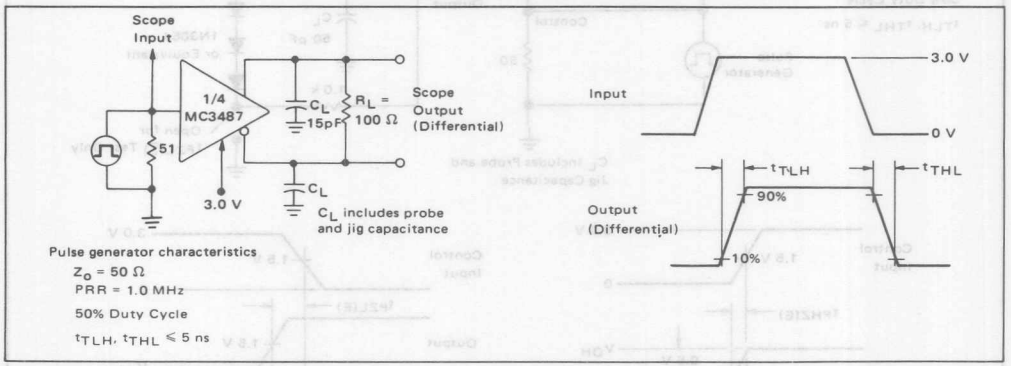


FIGURE 4 – OUTPUT CURRENT versus OUTPUT VOLTAGE

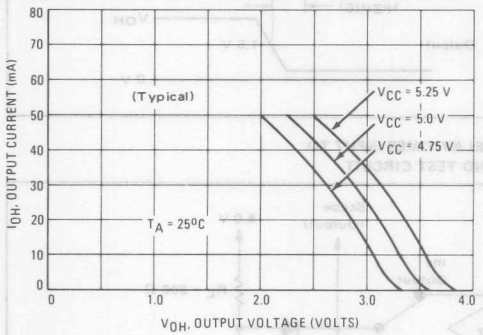
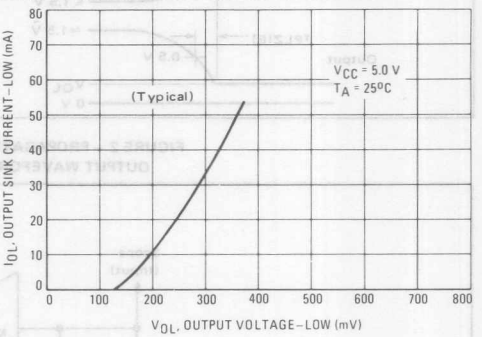


FIGURE 5 – OUTPUT SINK CURRENT versus OUTPUT VOLTAGE



MOTOROLA

MC3488A

DUAL EIA-423/EIA-232C DRIVER

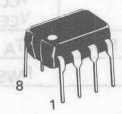
SILICON MONOLITHIC INTEGRATED CIRCUIT

DUAL EIA-423/EIA-232C LINE DRIVER

The MC3488A dual single-ended line driver has been designed to satisfy the requirements of EIA standards EIA-423 and EIA-232C, as well as CCITT X.26, X.28 and Federal Standard FIDS1030. It is suitable for use where signal wave shaping is desired and the output load resistance is greater than 450 ohms. Output slew rates are adjustable from 1.0 μs to 100 μs by a single external resistor. Output level and slew rate are insensitive to power supply variations. Input undershoot diodes limit transients below ground and output current limiting is provided in both output states.

The MC3488A has a standard 1.5 V input logic threshold for TTL or NMOS compatibility.

- PNP Buffered Inputs to Minimize Input Loading
- Short Circuit Protection
- Adjustable Slew Rate Limiting
- MC3488A Equivalent to 9636A
- Output Levels and Slew Rates are Insensitive to Power Supply Voltages
- No External Blocking Diode Required for V_{EE} Supply
- Second Source μA9636A



P1 SUFFIX
PLASTIC PACKAGE
CASE 626-05

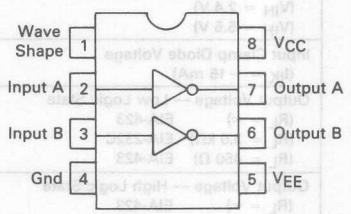


D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SO-8

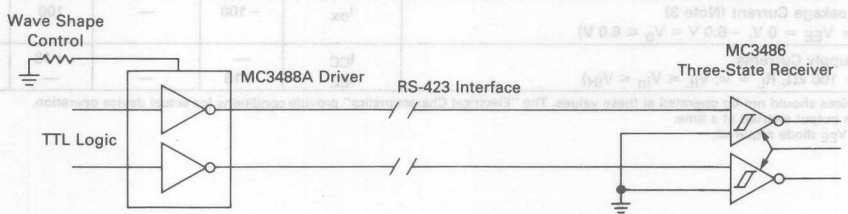


U SUFFIX
CERAMIC PACKAGE
CASE 693-02

PIN CONNECTIONS



TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC} V_{EE}	+15 −15	V
Output Current Source Sink	 I_{O+} I_{O-}	 +150 −150	mA
Operating Ambient Temperature	T_A	0 to +70	°C
Junction Temperature Range Ceramic Package Plastic Package	T_J	 175 150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltages	V_{CC} V_{EE}	10.8 −13.2	12 −12	13.2 −10.8	V
Operating Temperature Range	T_A	0	25	70	°C
Wave Shaping Resistor	R_{WS}	10	—	1000	kΩ

TARGET ELECTRICAL CHARACTERISTICS (Unless otherwise noted specifications apply over recommended operating conditions)

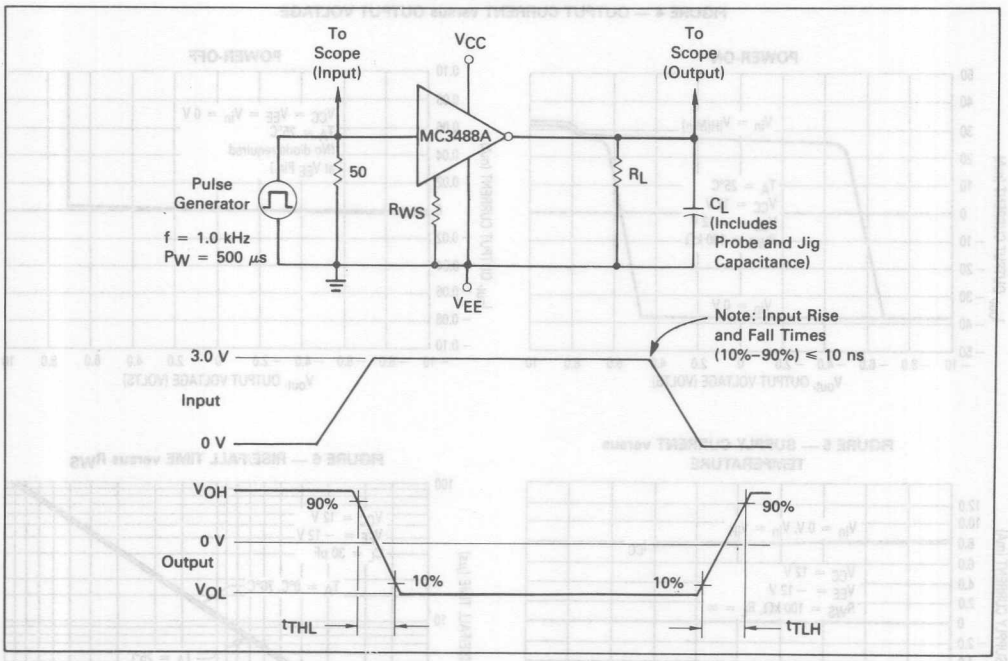
Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage — Low Logic State	V_{IL}	—	—	0.8	V
Input Voltage — High Logic State	V_{IH}	2.0	—	—	V
Input Current — Low Logic State (V_{IL} = 0.4 V)	I_{IL}	−80	—	—	μA
Input Current — High Logic State (V_{IH} = 2.4 V) (V_{IH} = 5.5 V)	 I_{IH1} I_{IH2}	 — —	 — —	 10 100	μA
Input Clamp Diode Voltage (I_{IK} = −15 mA)	V_{IK}	−1.5	—	—	V
Output Voltage — Low Logic State (R_L = ∞) EIA-423 (R_L = 3.0 kΩ) EIA-232C (R_L = 450 Ω) EIA-423	V_{OL}	 −6.0 −6.0 −6.0	 — — —	 −5.0 −5.0 −4.0	V
Output Voltage — High Logic State (R_L = ∞) EIA-423 (R_L = 3.0 kΩ) EIA-232C (R_L = 450 Ω) EIA-423	V_{OH}	 5.0 5.0 4.0	 — — —	 6.0 6.0 6.0	V
Output Resistance (R_L ≥ 450 Ω)	R_O	—	25	50	Ω
Output Short-Circuit Current (Note 2) (V_{in} = V_{out} = 0 V) (V_{in} = $V_{IH(Min)}$, V_{out} = 0 V)	 I_{OSH} I_{OSL}	 −150 +15	 — —	 −15 +150	mA
Output Leakage Current (Note 3) (V_{CC} = V_{EE} = 0 V, −6.0 V ≤ V_o ≤ 6.0 V)	I_{ox}	−100	—	100	μA
Power Supply Currents (R_W = 100 kΩ, R_L = ∞, V_{IL} ≤ V_{in} ≤ V_{IH})	I_{CC} I_{EE}	— −18	— —	+18 —	mA

Note 1: Devices should not be operated at these values. The "Electrical Characteristics" provide conditions for actual device operation.
2: One output shorted at a time.
3: No V_{EE} diode required.

TRANSITION TIMES (Unless otherwise noted, C_L = 30 pF, f = 1.0 kHz, V_{CC} = $-V_{EE}$ = 12.0 V ± 10%, T_A = 25°C, R_L = 450 Ω. Transition times measured 10% to 90% and 90% to 10%)

Characteristic	Symbol	Min	Typ	Max	Unit
Transition Time, Low-to-High State Output	t_{TLH}				μs
(R_W = 10 kΩ)		0.8	—	1.4	
(R_W = 100 kΩ)		8.0	—	14	
(R_W = 500 kΩ)		40	—	70	
(R_W = 1000 kΩ)		80	—	140	
Transition Time, High-to-Low State Output	t_{THL}				μs
(R_W = 10 kΩ)		0.8	—	1.4	
(R_W = 100 kΩ)		8.0	—	14	
(R_W = 500 kΩ)		40	—	70	
(R_W = 1000 kΩ)		80	—	140	

FIGURE 1 — TEST CIRCUIT AND WAVEFORMS FOR TRANSITION TIMES



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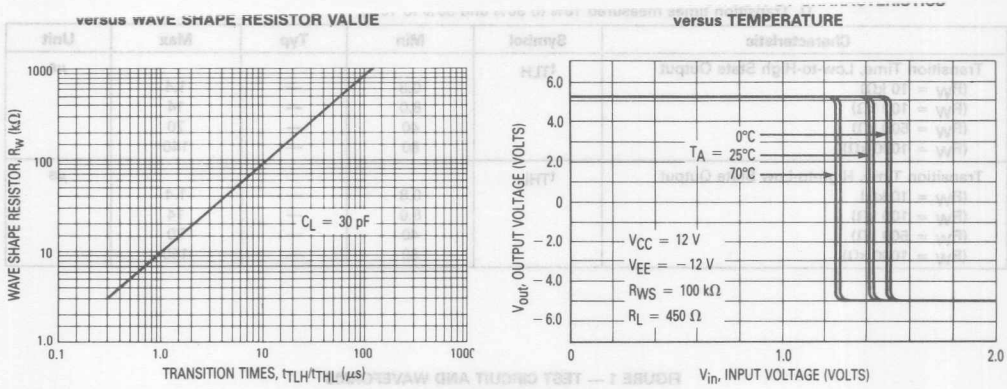


FIGURE 4 — OUTPUT CURRENT versus OUTPUT VOLTAGE

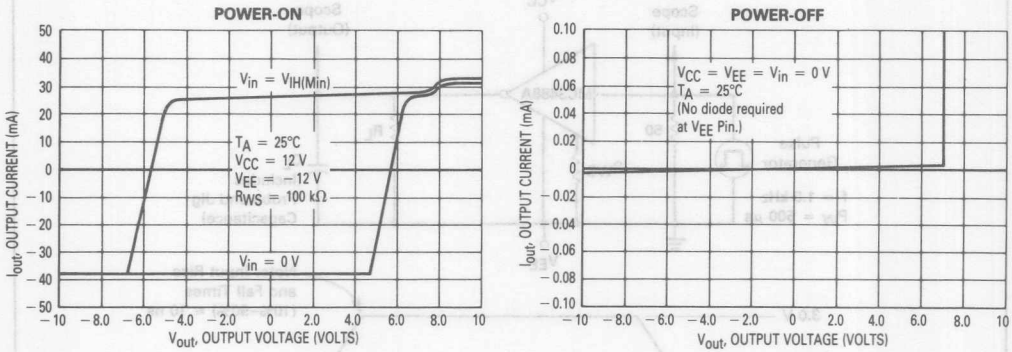


FIGURE 5 — SUPPLY CURRENT versus TEMPERATURE

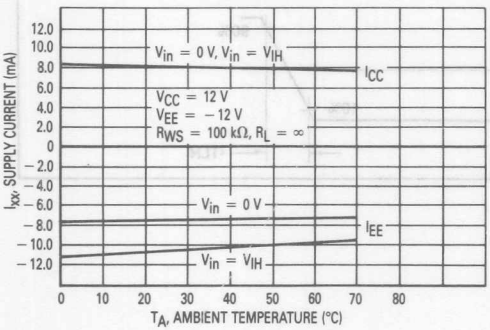
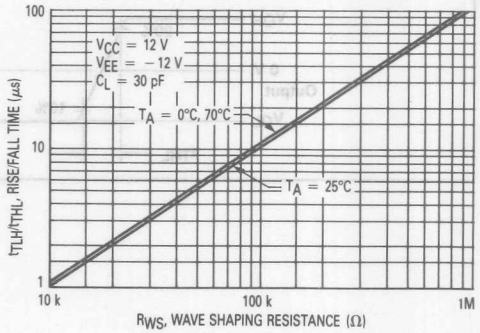


FIGURE 6 — RISE/FALL TIME versus R_{WS}



MOTOROLA

MC6875
MC6875A

Specifications and Applications Information

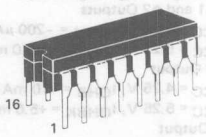
M6800 CLOCK GENERATOR

Intended to supply the non-overlapping $\phi 1$ and $\phi 2$ clock signals required by the microprocessor, this clock generator is compatible with 1.0, 1.5, and 2.0 MHz versions of the MC6800. Both the oscillator and high capacitance driver elements are included along with numerous other logic accessory functions for easy system expansion.

Schottky technology is employed for high speed and PNP-buffered inputs are employed for NMOS compatibility. A single +5 V power supply, and a crystal or RC network for frequency determination are required.

M6800 TWO-PHASE CLOCK GENERATOR/DRIVER

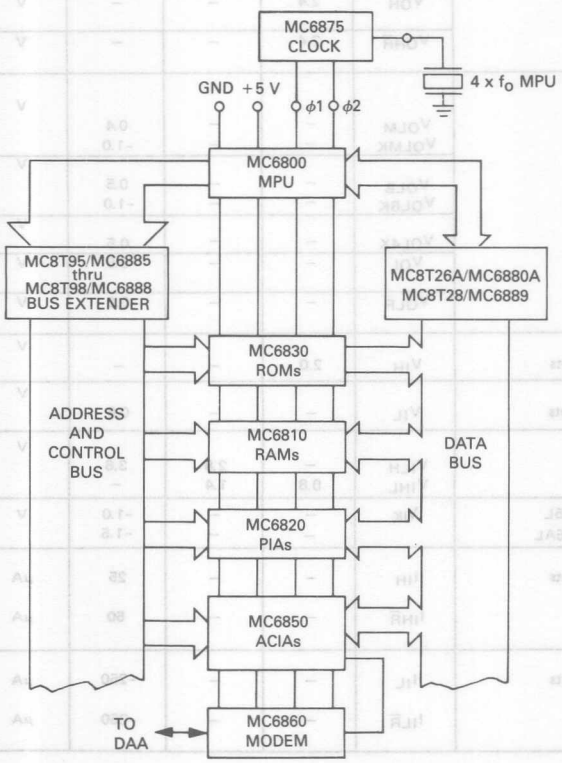
SCHOTTKY MONOLITHIC INTEGRATED CIRCUIT



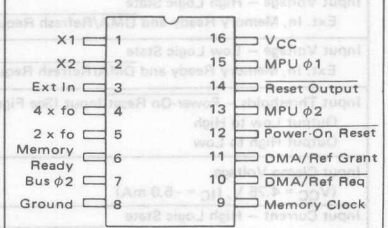
L SUFFIX
CERAMIC PACKAGE
CASE 620-10

7

Typical MPU System with Bus Extenders



PIN CONNECTIONS



ORDERING INFORMATION		
Device	Temperature Range	Package
MC6875L	0 to +70°C	Ceramic
MC6875AL	-55 to +125°C	DIP

ABSOLUTE MAXIMUM RATINGS (Unless otherwise noted $T_A = 25^oC$.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+7.0	Vdc
Input Voltage	V_I	+5.5	Vdc
Operating Ambient Temperature Range MC6875L MC6875AL	T_A	0 to +70 -55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Operating Junction Temperature	T_J	175	°C

NOTE:
Operation of the MC6875AL over the full military temperature range (to maximum T_A) will result in excessive operating junction temperature.

The use of a clip on 16 pin heat sink similar to AAVID Engineering, Inc., Model 5007 ($R_{\theta CA}$ = 18°C/W) is recommended above $T_A \approx 95°C$.

Contact AAVID Engineering, Inc.
30 Cook Court
Laconia, New Hampshire 03246
Tel. (603) 524-4443

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+4.75 to +5.25	Vdc
Operating Ambient Temperature Range	T_A	0 to +70	°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted specifications apply over recommended power supply and temperature ranges.
Typical values measured at V_{CC} = 5.0 V and $T_A = 25^oC$.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage — High Logic State					
MPU $\phi1$ and $\phi2$ Outputs					V
(V_{CC} = 4.75 V, I_{OHM} = -200 μA)	V_{OHM}	V_{CC} - 0.6	–	–	
(V_{CC} = 5.25 V, I_{OHMK} = +5.0 mA)	V_{OHMK}	–	–	V_{CC} + 1.0	
Bus $\phi2$ Output					V
(V_{CC} = 4.75 V, I_{OHB} = -10 mA)	V_{OHB}	2.4	–	–	
(V_{CC} = 5.25 V, I_{OHBK} = +5.0 mA)	V_{OHBK}	–	–	V_{CC} + 1.0	
4 x fo Output					V
(V_{CC} = 4.75 V, V_{IH} = 2.0 V, I_{OH4X} = -500 μA)	V_{OH4X}	2.4	–	–	
2 x fo, DMA/Refresh Grant and Memory Clock Outputs					
(V_{CC} = 4.75 V, I_{OH} = -500 μA)	V_{OH}	2.4	–	–	V
$\overline{\text{Reset}}$ Output					
(V_{CC} = 4.75 V, V_{IH} = 3.3 V, $I_{OH\overline{R}}$ = -100 μA)	$V_{OH\overline{R}}$	2.4	–	–	V
Output Voltage — Low Logic State					
MPU $\phi1$ and $\phi2$ Outputs					V
(V_{CC} = 4.75 V, I_{OLM} = +200 μA)	V_{OLM}	–	–	0.4	
(V_{CC} = 4.75 V, I_{OLMK} = -5.0 mA)	V_{OLMK}	–	–	-1.0	
Bus $\phi2$ Output					V
(V_{CC} = 4.75 V, I_{OLB} = +48 mA)	V_{OLB}	–	–	0.5	
(V_{CC} = 4.75 V, I_{OLBK} = -5.0 mA)	V_{OLBK}	–	–	-1.0	
4 x fo Output					V
(V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OL4X} = 16 mA)	V_{OL4X}	–	–	0.5	
2 x fo, DMA/Refresh Grant and Memory Clock Outputs					
(V_{CC} = 4.75 V, I_{OL} = 16 mA)	V_{OL}	–	–	0.5	V
$\overline{\text{Reset}}$ Output					
(V_{CC} = 4.75 V, V_{IL} = 0.8 V, $I_{OL\overline{R}}$ = 3.2 mA)	$V_{OL\overline{R}}$	–	–	0.5	V
Input Voltage — High Logic State					V
Ext. In, Memory Ready and $\overline{\text{DMA/Refresh Request}}$ Inputs	V_{IH}	2.0	–	–	
Input Voltage — Low Logic State					V
Ext. In, Memory Ready and $\overline{\text{DMA/Refresh Request}}$ Inputs	V_{IL}	–	–	0.8	
Input Thresholds — $\overline{\text{Power-On Reset}}$ Input (See Figure 2)					V
Output Low to High	V_{ILH}	–	2.8	3.6	
Output High to Low	V_{IHL}	0.8	1.4	–	
Input Clamp Voltage MC6875L	V_{IK}	–	–	-1.0	V
(V_{CC} = 4.75 V, I_{IC} = -5.0 mA) MC6875AL		–	–	-1.5	
Input Current — High Logic State					
Ext. In, Memory Ready and $\overline{\text{DMA/Refresh Request}}$ Inputs	I_{IH}	–	–	25	μA
(V_{CC} = 4.75 V, V_{IH} = 5.0 V)					
$\overline{\text{Power-On Reset}}$	$I_{IH\overline{R}}$	–	–	50	μA
(V_{CC} = 5.0 V, $V_{IH\overline{R}}$ = 5.0 V)					
Input Current — Low Logic State					
Ext. In, Memory Ready and $\overline{\text{DMA/Refresh Request}}$ Inputs	I_{IL}	–	–	-250	μA
(V_{CC} = 5.25 V, V_{IL} = 0.5 V)					
$\overline{\text{Power-On Reset}}$ Input	$I_{IL\overline{R}}$	–	–	-250	μA
(V_{CC} = 5.25 V, V_{IL} = 0.5 V)					

OPERATING DYNAMIC POWER SUPPLY CURRENT

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Currents (V_{CC} = 5.25 V, f_{osc} = 8.0 MHz, V_{IL} = 0 V, V_{IH} = 3.0 V)					
Normal Operation (Memory Ready and $\overline{\text{DMA/Refresh Request}}$ Inputs at High Logic State)	I_{CCN}	–	–	150	mA
Memory Ready Stretch Operation (Memory Ready Input at Low Logic State; $\overline{\text{DMA/Refresh Request}}$ Input at High Logic State)	I_{CCMR}	–	–	135	mA
$\overline{\text{DMA/Refresh Request}}$ Stretch Operation (Memory Ready Input at High Logic State; $\overline{\text{DMA/Refresh Request}}$ Input at Low Logic State)	I_{CCDR}	–	–	135	mA

SWITCHING CHARACTERISTICS

(These specifications apply whether the Internal Oscillator (see Figure 9) or an External Oscillator is used (see Figure 10). Typical values measured at V_{CC} = 5.0 V, T_A = 25°C, fo = 1.0 MHz (see Figure 8).

Characteristic	Symbol	Min	Typ	Max	Unit
MPU ϕ1 AND ϕ2 CHARACTERISTICS					
Output Period (Figure 3)	t_o	500	–	–	ns
Pulse Width (Figure 3)	t_{PWM}				ns
(fo = 1.0 MHz)		400	–	–	
(fo = 1.5 MHz)		230	–	–	
(fo = 2.0 MHz)		180	–	–	
Total Up Time (Figure 3)	t_{UPM}				ns
(fo = 1.0 MHz)		900	–	–	
(fo = 1.5 MHz)		600	–	–	
(fo = 2.0 MHz)		440	–	–	
Delay Time Referenced to Output Complement (Figure 3)					
Output High to Low State (Clock Overlap at 1.0 V)	t_{PLHM}	0	–	–	ns
Delay Times Referenced to 2 x fo (Figure 4 MPU ϕ2 only)					
Output Low to High Logic State	t_{PLHM2X}	–	–	85	ns
Output High to Low Logic State	t_{PHLM2X}	–	–	70	ns
Transition Times (Figure 3)					
Output Low to High Logic State	t_{TLHM}	–	–	25	ns
Output High to Low Logic State	t_{THLM}	–	–	25	ns
BUS ϕ2 CHARACTERISTICS					
Pulse Width – Low Logic State (Figure 4)	t_{PWLB}				ns
(fo = 1.0 MHz)		430	–	–	
(fo = 1.5 MHz)		280	–	–	
(fo = 2.0 MHz)		210	–	–	
Pulse Width – High Logic State	t_{PWHB}				ns
(fo = 1.0 MHz)		450	–	–	
(fo = 1.5 MHz)		295	–	–	
(fo = 2.0 MHz)		235	–	–	
Delay Times – (Referenced to MPU ϕ1) (Figure 4)					
Output Low to High Logic State	t_{PLHBM1}				ns
(fo = 1.0 MHz)		480	–	–	
(fo = 1.5 MHz)		320	–	–	
(fo = 2.0 MHz)		240	–	–	
Output High to Low Logic State	t_{PHLBM1}				
(C_L = 300 pF)		–	–	25	
(C_L = 100 pF)		–	–	20	
Delay Times (Referenced to MPU ϕ2) (Figure 4)					
Output Low to High Logic State	t_{PLHBM2}	-30	–	+25	ns
Output High to Low Logic State	t_{PHLBM2}	0	–	+40	ns
Transition Times (Figure 4)					
Output Low to High Logic State	t_{TLHB}	–	–	20	ns
Output High to Low Logic State	t_{THLB}	–	–	20	ns

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Delay Times (Referenced to MPU φ2) (Figure 4)					
Output Low to High Logic State	t_{PLHCM}	-50	–	+25	ns
Output High to Low Logic State	t_{PHLCM}	0	–	+40	ns
Delay Times (Referenced to 2 x fo) (Figure 4)					
Output Low to High Logic State	t_{PLHC2X}	–	–	65	ns
Output High to Low Logic State	t_{PHLC2X}	–	–	85	ns
Transition Times (Figure 4)					
Output Low to High State	t_{TLHC}	–	–	25	ns
Output High to Low State	t_{THLC}	–	–	25	ns

2 x fo CHARACTERISTICS

Delay Times (Referenced to 4 x fo) (Figure 4)					
Output Low to High Logic State	t_{PLH2X}	–	–	50	ns
Output High to Low Logic State	t_{PHL2X}	–	–	65	ns
Delay Time (Referenced to MPU φ1) (Figure 4)					
Output High to Low Logic State	$t_{PHL2XM1}$				ns
(fo = 1.0 MHz)		365	–	–	
(fo = 1.5 MHz)		220	–	–	
Transition Times (Figure 4)					
Output Low to High Logic State	t_{TLH2X}	–	–	25	ns
Output High to Low Logic State	t_{THL2X}	–	–	25	ns

4 x fo CHARACTERISTICS

Delay Times (Referenced to Ext. In) (Figure 4)					
Output Low to High Logic State	t_{PLH4X}	–	–	50	ns
Output High to Low Logic State	t_{PHL4X}	–	–	30	ns
Transition Time (Figure 4)					
Output Low to High Logic State	t_{TLH4X}	–	–	25	ns
Output High to Low Logic State	t_{THL4X}	–	–	25	ns

MEMORY READY CHARACTERISTICS

Set-Up Times (Figure 5)					
Low Input Logic State	t_{SMRL}	55	–	–	ns
High Input Logic State	t_{SMRH}	75	–	–	ns
Hold Time (Figure 5)					
Low Input Logic State	t_{HMRL}	10	–	–	ns

$\overline{\text{DMA/REFRESH REQUEST}}$ CHARACTERISTICS

Set-Up Times (Figure 6)					
Low Input Logic State	t_{SDRL}	65	–	–	ns
High Input Logic State	t_{SDRH}	75	–	–	ns
Hold Time (Figure 6)					
Low Input Logic State	t_{HDRL}	10	–	–	ns

DMA/REFRESH GRANT CHARACTERISTICS

Delay Time Referenced to Memory Clock (Figure 6)					
Output Low to High Logic State	t_{PLHG}	-15	–	+25	ns
Output High to Low Logic State	t_{PHLG}	-25	–	+15	ns
Transition Times (Figure 6)					
Output Low to High Logic State	t_{TLHG}	–	–	25	ns
Output High to Low Logic State	t_{THLG}	–	–	25	ns

$\overline{\text{RESET}}$ CHARACTERISTICS

Delay Time Referenced to Power-On Reset (Figure 7)					
Output Low to High Logic State	$t_{PLH\overline{R}}$	–	–	1000	ns
Output High to Low Logic State	$t_{PHL\overline{R}}$	–	–	250	ns
Transition Times (Figure 7)					
Output Low to High Logic State	$t_{TLH\overline{R}}$	–	–	100	ns
Output High to Low Logic State	$t_{THL\overline{R}}$	–	–	50	ns

DESCRIPTION OF PIN FUNCTIONS

- 4 x fo – A free running oscillator at four times the MPU clock rate useful for a system sync signal.
- 2 x fo – A free running oscillator at two times the MPU clock rate.
- $\overline{\text{DMA/REF REQ}}$ – An asynchronous input used to freeze the MPU clocks in the φ1 high, φ2 low state for dynamic memory refresh or cycle steal DMA (Direct Memory Access).
- REF GRANT – A synchronous output used to synchronize the refresh or DMA operation to the MPU.
- MEMORY READY – An asynchronous input used to freeze the MPU clocks in the φ1 low, φ2 high state for slow memory interface.
- MPU φ1, MPU φ2 – Capable of driving the φ1 and φ2 inputs on two MC6800s.
- BUS φ2 – An output nominally in phase with MPU φ2 having MC8T26A type drive capability.
- MEMORY CLOCK – An output nominally in phase with MPU φ2 which free runs during a refresh request cycle.
- $\overline{\text{POWER-ON RESET}}$ – A Schmitt trigger input which controls $\overline{\text{Reset}}$. A capacitor to ground is required to set the desired time constant. Internal 50 k resistor to V_{CC}. See General Design Suggestions for Manual Reset Operation.
- $\overline{\text{RESET}}$ – An output to the MPU and I/O devices.
- X1, X2 – Provision to attach a series resonant crystal or RC network.
- EXT IN – Allows driving by an external TTL signal to synchronize the MPU to an external system.

FIGURE 1 – BLOCK DIAGRAM

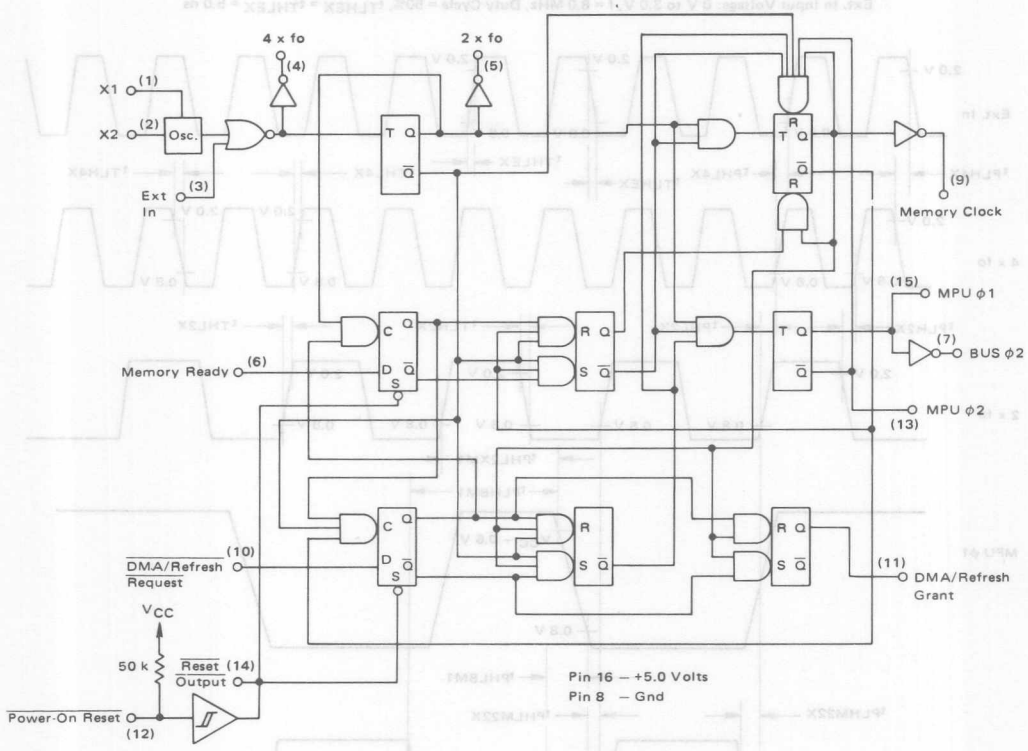


FIGURE 2 – TYPICAL HYSTERESIS CHARACTERISTIC OF $\overline{\text{RESET}}$ FUNCTION

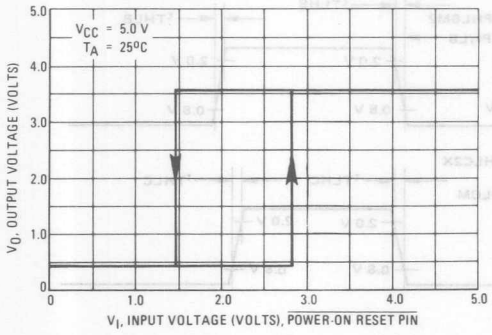


FIGURE 3 – TIMING DIAGRAM FOR MPU ϕ1 AND ϕ2

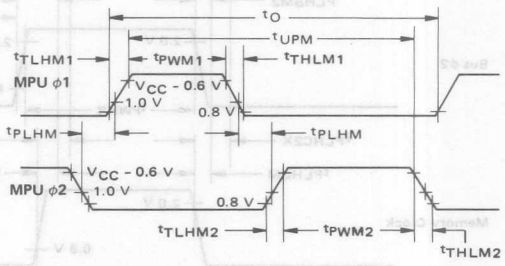


FIGURE 4 – TIMING DIAGRAM FOR NON-STRETCHED OPERATION
(Memory Ready and $\overline{\text{DMA/Refresh Request}}$ held high continuously)
Ext. In Input Voltage: 0 V to 3.0 V, f = 8.0 MHz, Duty Cycle = 50%, $t_{TLHEX} = t_{THLEX} = 5.0$ ns

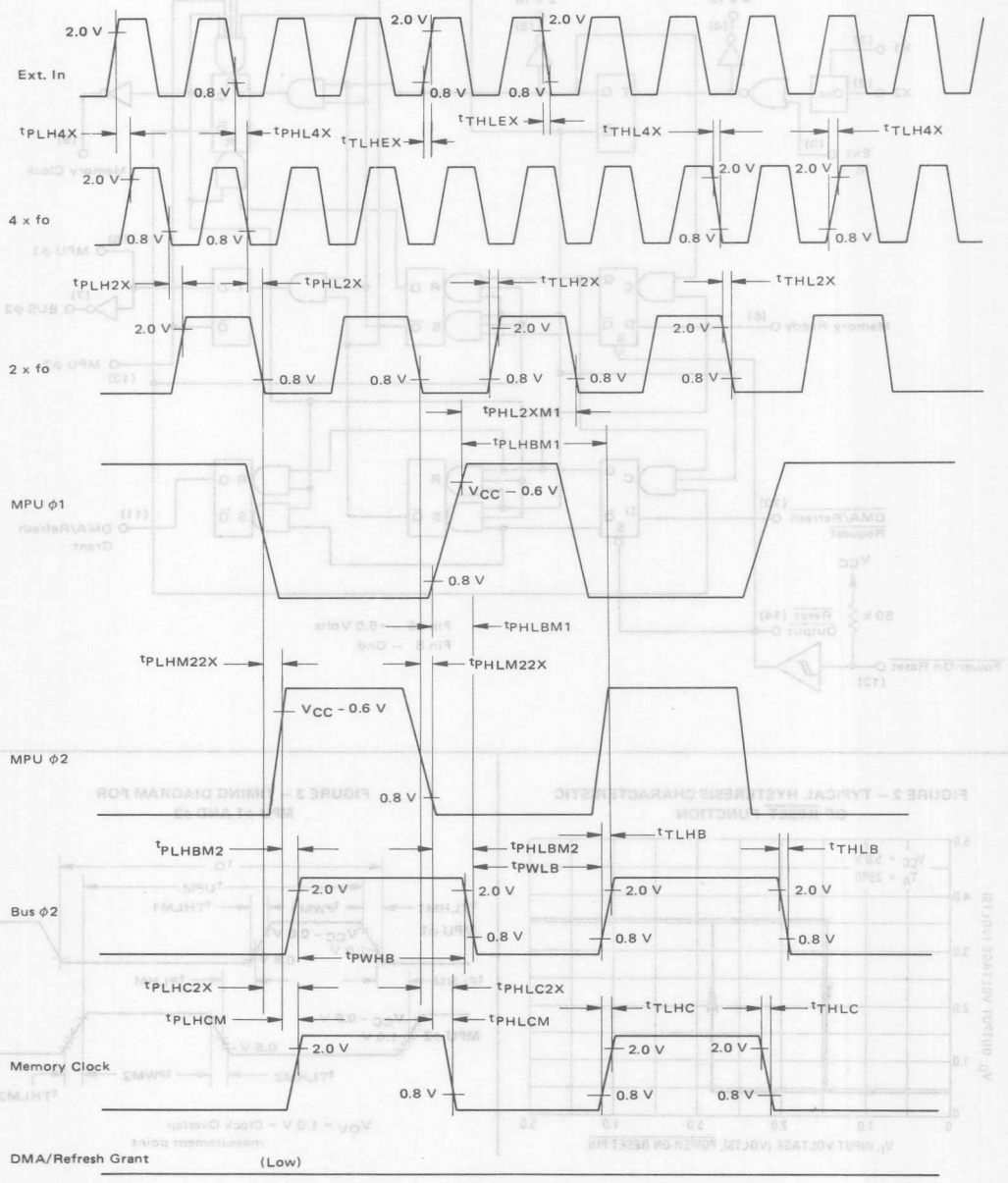
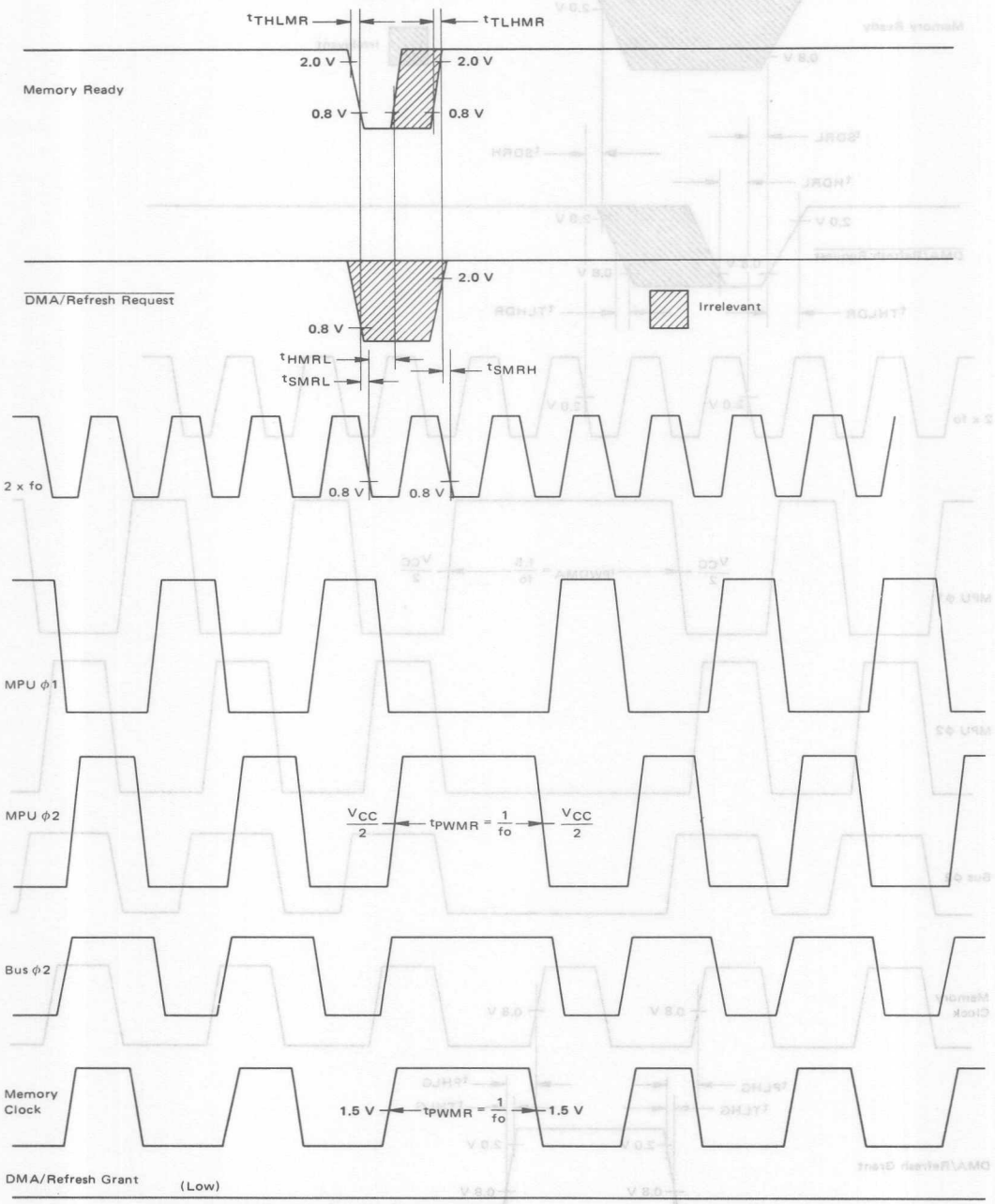
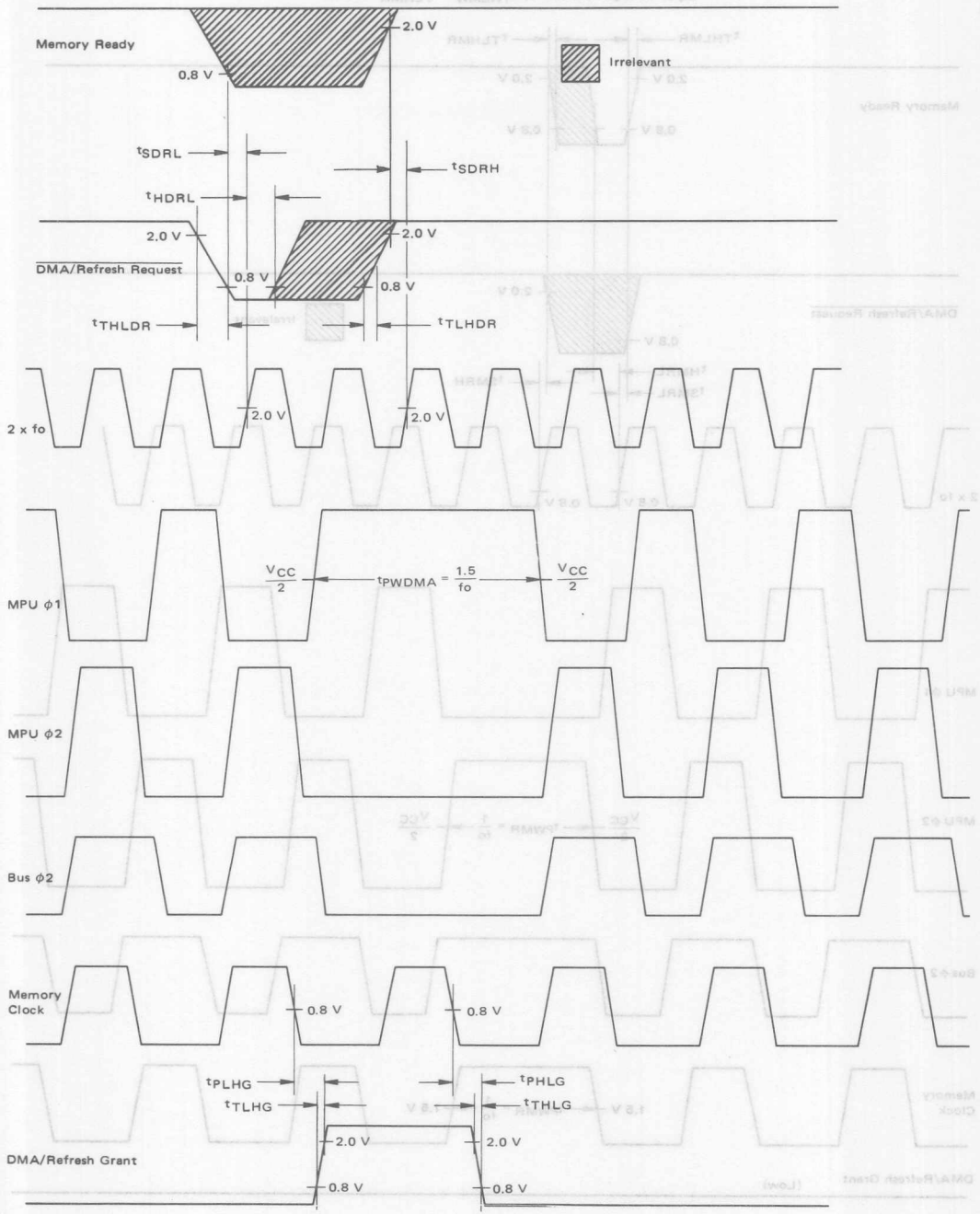


FIGURE 5 – TIMING DIAGRAM FOR MEMORY READY STRETCH OPERATION
(Minimum Stretch Shown)
Input Voltage: 3.0 to 0 V, $t_{THLMR} = t_{TLHMR} = 5.0$ ns



Input Voltage: 3.0 to 0 V, $t_{THLDR} = t_{TLHDR} = 5.0$ ns



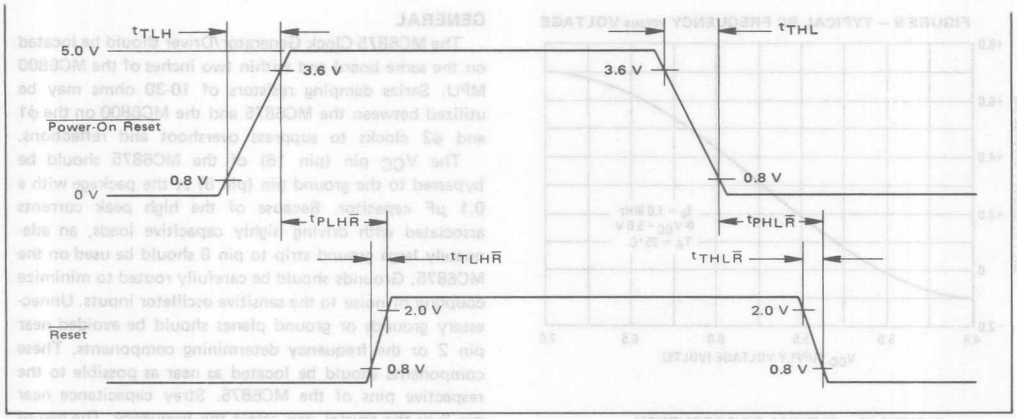
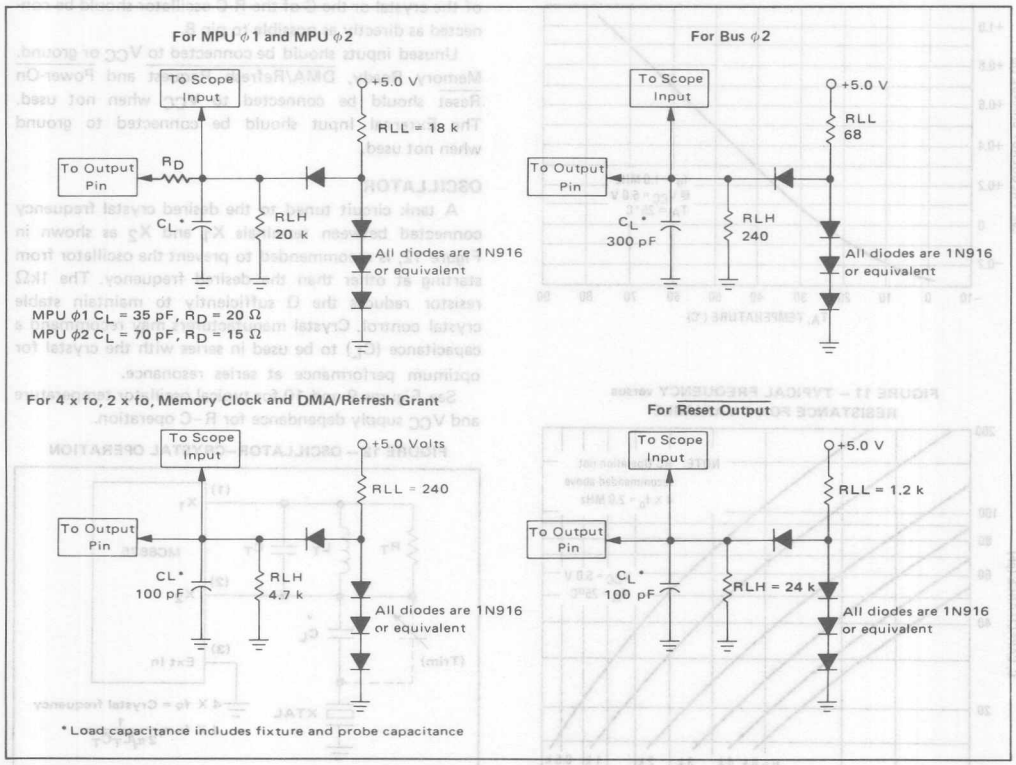


FIGURE 8 – LOAD CIRCUITS



*Load capacitance includes fixture and probe capacitance

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APPLICATIONS INFORMATION

FIGURE 9 – TYPICAL RC FREQUENCY versus VOLTAGE

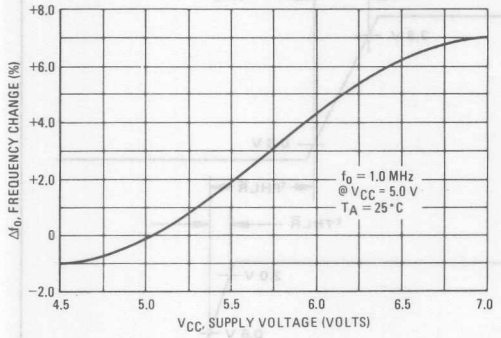


FIGURE 10 – TYPICAL RC FREQUENCY versus TEMPERATURE

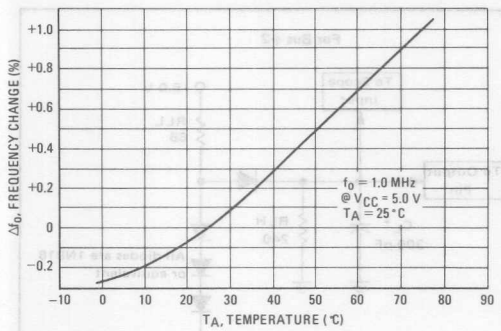
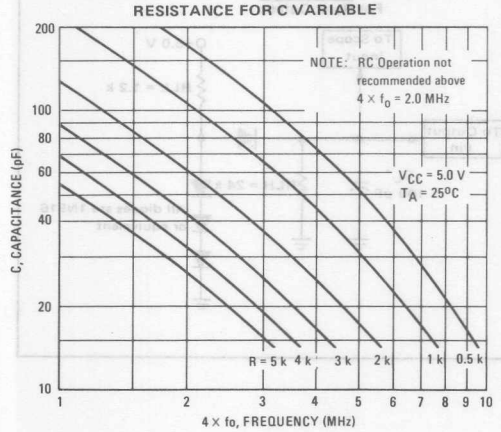


FIGURE 11 – TYPICAL FREQUENCY versus RESISTANCE FOR C VARIABLE



GENERAL

The MC6875 Clock Generator/Driver should be located on the same board and within two inches of the MC6800 MPU. Series damping resistors of 10-30 ohms may be utilized between the MC6875 and the MC6800 on the $\phi 1$ and $\phi 2$ clocks to suppress overshoot and reflections.

The V_{CC} pin (pin 16) of the MC6875 should be bypassed to the ground pin (pin 8) at the package with a 0.1 μF capacitor. Because of the high peak currents associated with driving highly capacitive loads, an adequately large ground strip to pin 8 should be used on the MC6875. Grounds should be carefully routed to minimize coupling of noise to the sensitive oscillator inputs. Unnecessary grounds or ground planes should be avoided near pin 2 or the frequency determining components. These components should be located as near as possible to the respective pins of the MC6875. Stray capacitance near pin 2 or the crystal, can affect the frequency. The can of the crystal should not be grounded. The ground side of the crystal or the C of the R-C oscillator should be connected as directly as possible to pin 8.

Unused inputs should be connected to V_{CC} or ground. Memory Ready, $\overline{\text{DMA/Refresh Request}}$ and $\overline{\text{Power-On Reset}}$ should be connected to V_{CC} when not used. The External Input should be connected to ground when not used.

OSCILLATOR

A tank circuit tuned to the desired crystal frequency connected between terminals X_1 and X_2 as shown in Figure 12, is recommended to prevent the oscillator from starting at other than the desired frequency. The 1kΩ resistor reduces the Q sufficiently to maintain stable crystal control. Crystal manufacturers may recommend a capacitance (C_L) to be used in series with the crystal for optimum performance at series resonance.

See Figures 9 and 10 for typical oscillator temperature and V_{CC} supply dependence for R-C operation.

FIGURE 12 – OSCILLATOR–CRYSTAL OPERATION

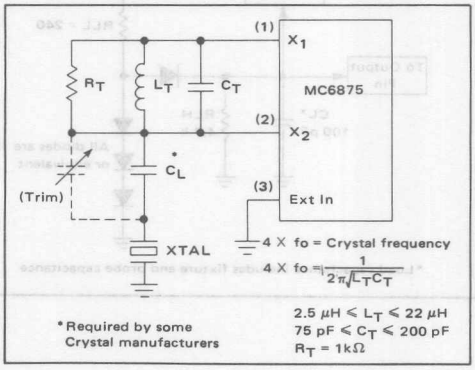
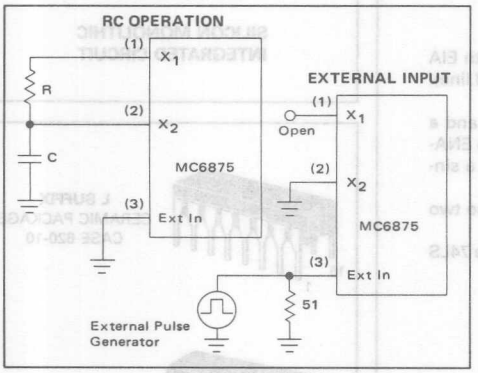


TABLE 1 – OSCILLATOR COMPONENTS

TANK CIRCUIT PARAMETERS		APPROXIMATE CRYSTAL PARAMETERS				CTS KNIGHTS 400 REIMANN AVE. SANDWICH, IL 60548 (815) 786-8411	McCOY ELECT. CO. WATTS & CHESTNUTS STS. MT. HOLLY SPRING, PA 17065 (717) 486-3411	TYCO CRYSTAL PRODUCTS 3940 W. MONTECITO PHOENIX, AZ 85019 (602) 272-7945
L_T μH	C_T pF	R_S Ohms	Co pF	C_1 mpF	fo MHz			
10	150	15-75	3-6	12	4.0	MP-04A * 390 pF	113-31	150-3260
4.7	82	8-45	4-7	23	8.0	MP-080 * 47 pF	113-32	150-3270

Inductors may be obtained from: Coilcraft, Cary, IL 60013 (312) 639-2361

FIGURE 13



To precisely time a crystal to desired frequency, a variable trimmer capacitor in the range of 7 to 40 pF would typically be used. Note it is not a recommended practice to tune the crystal with a parallel load capacitance.

The table above shows typical values for C_T and L_T, typical crystal characteristics, and manufacturers' part numbers for 4.0 and 8.0 megahertz operation.

The MC6875 will function as an R-C oscillator when connected as shown in Figure 13. The desired output frequency (Mϕ1) is approximately:

Formula

$$4 \times fo \approx \frac{320}{C\,(R + .27) + 23}$$

C in picofarads
R in K ohms
4 x fo in Megahertz

(See Figure 11)

It would be desirable to select a capacitor greater than 15 pF to minimize the effects of stray capacitance. It is also desirable to keep the resistor in the 1 to 5 k Ω range. There is a nominal 270 Ω resistor internally at X_1 which is in series with the external R. By keeping the external R as large as possible, the effects due to process variations of the internal resistor on the frequency will be reduced. There will, however, still be some variation in frequency in a production lot both from the resistance variations, external and internal, and process variations of the input switching thresholds. Therefore, in a production system, it is recommended a potentiometer be placed in series with a fixed R between X_1 and X_2.

POWER-ON RESET

As the power to the MC6875 comes up, the Reset Output will be in a high impedance state and will not give a solid V_{OL} output level until V_{CC} has reached 3.5 to 4.0 V. During this time transients may appear on the clock outputs as the oscillator begins to start. This happens at approximately V_{CC} = 3 V. At some V_{CC} level above that, where Reset Output goes low, all the clock outputs will begin functioning normally. This phenomenon of the start-up sequence should not cause any problems except possibly in systems with battery back-up memory. The transients on the clock lines during the time the Reset Output is high impedance could initiate the system in some unknown mode and possibly write into the backup memory system. Therefore in battery backup systems, more elaborate reset circuitry will be required.

Please note that the Power-On Reset input pin of the MC6875 is not suitable for use with a manual MPU reset switch if the DMA/Ref Req or Memory Ready inputs are going to be used. The power on reset circuitry is used to initialize the internal control logic and whenever the input is switched low, the MC6875 is irresponsive to the DMA/Ref Req or Memory Ready inputs. This may result in the loss of dynamic memory and/or possibly a byte of slow static memory. The circuit of Figure 14 is recommended for applications which do not utilize the DMA/Ref Req or Memory Ready inputs. The circuit of Figure 15 is recommended for those applications that do.

FIGURE 14 – MANUAL RESET FOR APPLICATIONS NOT USING DMA/REFRESH REQUEST OR MEMORY READY INPUTS

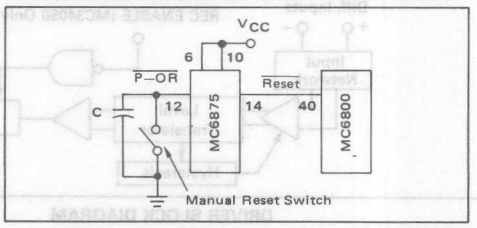
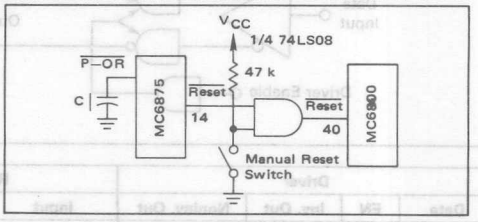


FIGURE 15 – MANUAL RESET FOR SYSTEMS USING DYNAMIC RAM OR SLOW STATIC RAM IN CONJUNCTION WITH MEMORY READY OR DMA/REFRESH REQUEST INPUTS



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MC34051

Advance Information

DUAL EIA-422/423 TRANSCEIVER

The MC34050/51 are dual transceivers which comply with EIA Standards EIA-422 (Balanced line) and EIA-423 (Unbalanced line). Each device contains two drivers and two receivers.

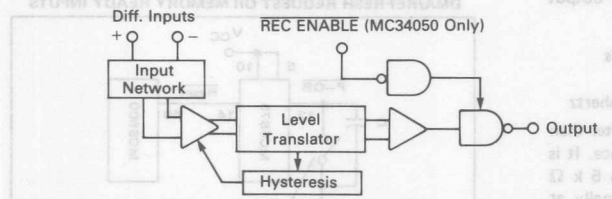
The MC34050 has a DRIVER ENABLE (for both drivers) and a $\overline{\text{RECEIVER ENABLE}}$ (for both receivers). Connecting the two ENABLES together provides Driver-to-Receiver switching from a single line.

The MC34051 has a DRIVER ENABLE for each driver. The two receivers are permanently enabled.

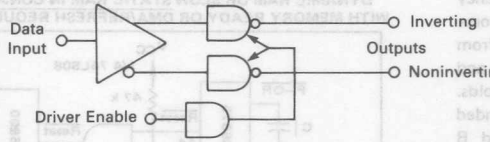
The Driver inputs, Receiver outputs, and Enable inputs are 74LS TTL compatible.

- Two Independent Drivers and Receivers Per Package
- 3-State Outputs
- Single 5 Volt Supply
- Internal Hysteresis (50 mV Typical) on Receivers
- Receivers Provide Fail-Safe Function. Output Stays High if Inputs are Open, Shorted (floating), or Terminated (floating)
- Receivers May Be Used in EIA-422 or 423 Systems
- Drivers Meet Full EIA-422 Standards
- Drivers' Outputs are Short Circuit Protected

RECEIVER BLOCK DIAGRAM



DRIVER BLOCK DIAGRAM

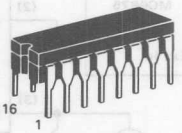


Driver				Receiver		
Data	EN	Inv. Out	Noninv. Out	Input	$\overline{\text{EN}}$	Output
L	H	H	L	> +0.2 V Diff.	L	H
H	H	L	H	< –0.2 V Diff.	L	L
X	L	Z	Z	X	H	Z

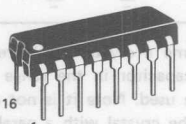
This document contains information on a new product. Specifications and information herein are subject to change without notice.

DUAL EIA-422/423 TRANSCEIVER

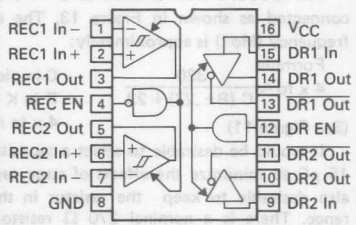
SILICON MONOLITHIC INTEGRATED CIRCUIT



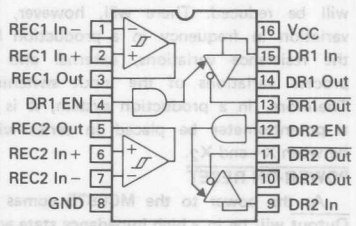
L SUFFIX
CERAMIC PACKAGE
CASE 620-10



P SUFFIX
PLASTIC PACKAGE
CASE 648-06



MC34050



MC34051

ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Units
Power Supply Voltage (V_{CC})	7.0	Vdc
Input Common Mode Voltage (Receivers)	±25	Vdc
Input Differential Voltage (Receivers)	±25	Vdc
Output Sink Current (Receivers)	50	mA
Enable Input Voltage (Drivers and Receivers)	5.5	Vdc
Input Voltage (Drivers)	5.5	Vdc
Applied Output Voltage (3-State mode) — Receivers	−1.0 to +7.0	Vdc
Applied Output Voltage (3-State mode) — Drivers	−1.0 to +7.0	Vdc
Junction Temperature	−65 to +150	°C
Storage Temperature	−65 to +150	°C

Devices should not be operated at these values. The "Recommended Operating Limits" provide for actual device operation.

RECOMMENDED OPERATING LIMITS

Parameter	Min	Typ	Max	Units
Power Supply Voltage	+4.75	+5.0	+5.25	Vdc
Input Common Mode Voltage (Receivers)	−7.0	—	+7.0	Vdc
Input Differential Voltage (Receivers)	−6.0	—	+6.0	Vdc
Enable Input Voltage (Drivers and Receivers)	0	—	+5.25	Vdc
Input Voltage (Drivers)	0	—	+5.25	Vdc
Ambient Temperature Range	0	—	+70	°C

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ELECTRICAL CHARACTERISTICS (Unless otherwise noted specifications apply for $4.75 < V_{CC} < 5.25$ volts, and $0° < T_A < 70°C$).

Parameter	Symbol	Min	Typ	Max	Units
DRIVERS					
Input Voltage — Low	V_{ILD}	—	—	0.8	Vdc
Input Voltage — High	V_{IHD}	2.0	—	—	Vdc
Input Current @ V_{IL} = 0.4 V	I_{ILD}	−360	—	—	μA
Input Current @ V_{IH} = 2.7 V V_{IH} = 5.25 V	I_{IHD}	— —	— —	+20 +100	μA
Input Clamp Voltage (I_{IK} = −18 mA)	V_{IKD}	−1.5	—	—	Vdc
Output Voltage — Low (I_{OL} = 20 mA)	V_{OLD}	—	—	0.5	Vdc
Output Voltage — High (I_{OH} = −20 mA)	V_{OHD}	2.5	—	—	Vdc
Output Offset Voltage Difference (Note 1)	V_{OSD}	−0.4	—	+0.4	Vdc
Output Differential Voltage (Note 1)	V_T	2.0	—	—	Vdc
Output Differential Voltage Difference (Note 1)	V_{TD}	−0.4	—	+0.4	Vdc
Short Circuit Current (V_{CC} = 5.25 V) (From High Output, Note 2)	I_{OSD}	−150	—	−30	mA
Output Leakage Current — Hi-Z State (V_{out} = 0.5 V, DR EN = 0.8 V) (V_{out} = 2.7 V, DR EN = 0.8 V)	I_{OZD}	 −100 −100	 — —	 +100 +100	μA
Output Leakage — Power Off (V_{out} = −0.25 V, V_{CC} = 0 V) (V_{out} = 6.0 V, V_{CC} = 0 V)	$I_{O(off)}$	 −100 —	 — —	 — +100	μA

Notes: 1) See EIA Standard EIA-422 and Figure 1 for exact test conditions.
2) Only one output in a package should be shorted at a time, for no longer than 1 second.

ELECTRICAL CHARACTERISTICS (Unless otherwise noted specifications apply for $4.75 < V_{CC} < 5.25$ volts, and $0° < T_A < 70°C$).

Parameter	Symbol	Min	Typ	Max	Units
RECEIVERS					
Differential Input Threshold Voltage (Note 3)	V_{THR}				Vdc
($-7.0\ V < V_{ICM} < +7.0$, $V_{out} \geq 2.7$ V)		—	—	+0.2	
($-7.0\ V < V_{ICM} < +7.0$, $V_{out} \leq 0.45$ V)		−0.2	—	—	
Input Bias Current	I_{IBR}				mA
($0 \leq V_{CC} \leq 5.25$ V, $V_{in} = +15$ V)		—	—	+2.3	
($0 \leq V_{CC} \leq 5.25$ V, $V_{in} = -15$ V)		−2.8	—	—	
Input Balance and Output Level					Vdc
($-7.0 \leq V_{ICM} \leq +7.0$ V)					
($V_{ID} = +0.4$ V, $I_O = -400\ \mu A$)	V_{OHR}	2.7	—	—	
($V_{ID} = -0.4$ V, $I_O = 8.0$ mA)	V_{OLR}	—	—	0.45	
Output Leakage Current — 3-State (Pin 4 = 2.0 V, MC34050 only)	I_{OZR}				μA
($V_{ID} = +3.0$ V, $V_O = 0.4$ V)		−100	—	+100	
($V_{ID} = -3.0$ V, $V_O = 2.4$ V)		−100	—	+100	
Output Short Circuit Current (Note 2, $V_{CC} = 5.25$ V)	I_{OSR}	−85	—	−15	mA
($V_{ID} = +3.0$ V, MC34050 Pin 4 = 0.4 V, $V_O = 0$ V)					
ENABLES					
Input Voltage — Low	V_{ILE}	—	—	0.8	Vdc
Input Voltage — High	V_{IHE}	2.0	—	—	Vdc
Input Current @ $V_{IL} = 0.4$ V (Receiver EN)	I_{ILER}	−100	—	—	μA
(Driver EN)	I_{ILED}	−360	—	—	
Input Current @ $V_{IH} = 2.7$ V	I_{IHE}	—	—	+20	μA
$V_{IH} = 5.25$ V		—	—	+100	
Input Clamp Voltage ($I_{IK} = -18$ mA)	V_{IKE}	−1.5	—	—	Vdc
POWER SUPPLY					
Power Supply Current @ $V_{CC} = 5.25$ V	I_{CC}	—	55	80	mA

Notes: 1) See EIA Standard EIA-422 and Figure 1 for exact test conditions.
2) Only one output in a package should be shorted at a time, for no longer than 1 second.
3) Differential input threshold voltage and guaranteed output levels are done simultaneously for worst case.
4) All currents into a device pin are positive, those out of a pin are negative. Voltages are referenced to ground. Algebraic convention rather than magnitude is used to define limits.

DRIVER SWITCHING CHARACTERISTICS ($V_{CC} = 5.0$ V, $T_A = 25°C$, See Figure 2)

Parameter	Symbol	Min	Typ	Max	Units
Propagation Delay					ns
Data Input to Output High-to-Low	t_{PHLD}	—	—	20	
Data Input to Output Low-to-High	t_{PLHD}	—	—	20	
Output Skew ($\lvert t_{PHL} - t_{PLH} \rvert$ each driver)	t_{SKD}	—	—	8	
Enable Input to Output					
$C_L = 10$ pF, $R_L = 75\ \Omega$ to Gnd	t_{PHZD}	—	—	30	
$C_L = 10$ pF, $R_L = 180\ \Omega$ to V_{CC}	t_{PLZD}	—	—	35	
$C_L = 30$ pF, $R_L = 75\ \Omega$ to Gnd	t_{PZHD}	—	—	40	
$C_L = 30$ pF, $R_L = 180\ \Omega$ to V_{CC}	t_{PZLD}	—	—	45	
Maximum Data Input Transition Time (10–90%)	t_{TRD}	—	50	—	ns

RECEIVER SWITCHING CHARACTERISTICS ($V_{CC} = 5.0$ V, $T_A = 25°C$, Figure 3)

Parameter	Symbol	Min	Typ	Max	Units
Propagation Delay					ns
Differential Input to Output — High-to-Low	t_{PHLR}	—	—	30	
Differential Input to Output — Low-to-High	t_{PLHR}	—	—	30	
Enable Input — Output Low to 3-State*	t_{PLZR}	—	—	35	
Enable Input — Output High to 3-State*	t_{PHZR}	—	—	35	
Enable Input — Output 3-State to High*	t_{PZHR}	—	—	30	
Enable Input — Output 3-State to Low*	t_{PZLR}	—	—	30	

*MC34050 Only.

FIGURE 1 — DRIVER OUTPUT TEST CIRCUIT

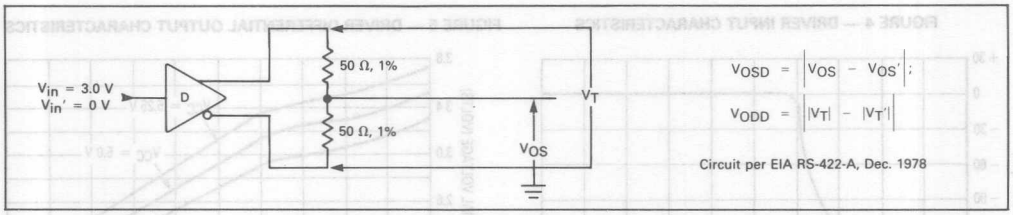
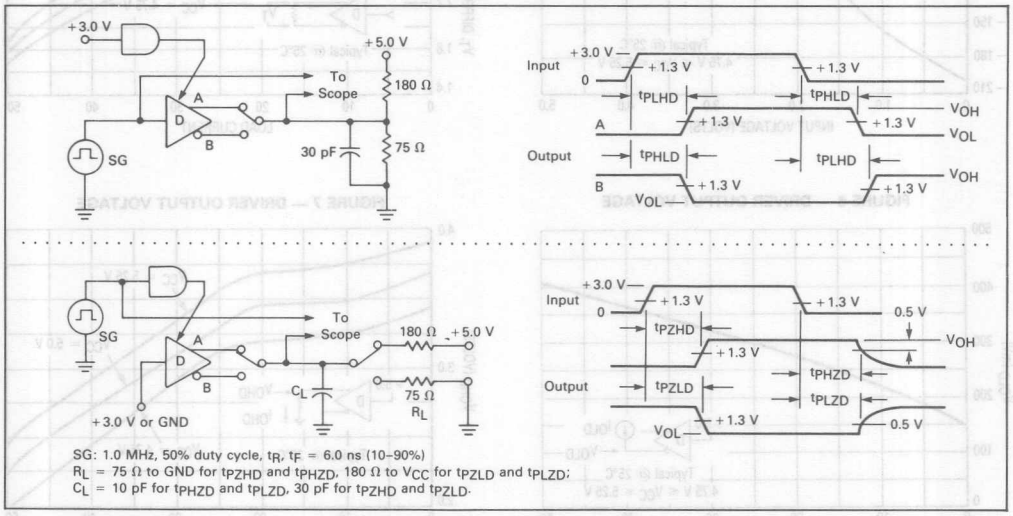
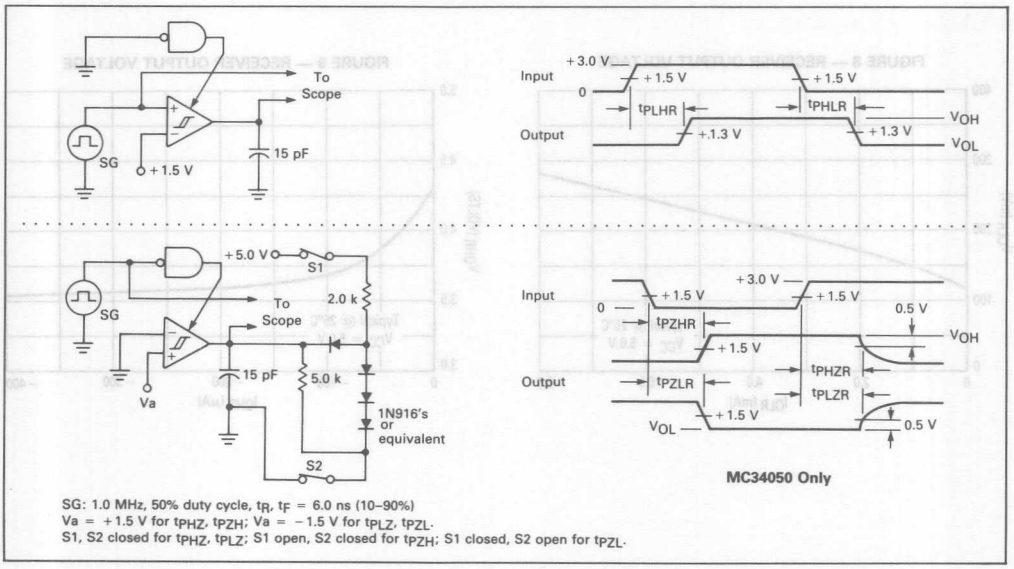


FIGURE 2 — DRIVER SWITCHING TEST CIRCUITS



SG: 1.0 MHz, 50% duty cycle, t_R, t_F = 6.0 ns (10–90%)
R_L = 75 Ω to GND for t_{PZHD} and t_{PHZD}, 180 Ω to V_{CC} for t_{PZLD} and t_{PLZD};
C_L = 10 pF for t_{PHZD} and t_{PLZD}, 30 pF for t_{PZHD} and t_{PZLD}.

FIGURE 3 — RECEIVER SWITCHING TEST CIRCUITS



MC34050 Only

SG: 1.0 MHz, 50% duty cycle, t_R, t_F = 6.0 ns (10–90%)
Va = +1.5 V for t_{PHZ}, t_{PZH}; Va = −1.5 V for t_{PLZ}, t_{PZL}.
S1, S2 closed for t_{PHZ}, t_{PLZ}; S1 open, S2 closed for t_{PZH}; S1 closed, S2 open for t_{PZL}.

7

FIGURE 4 — DRIVER INPUT CHARACTERISTICS

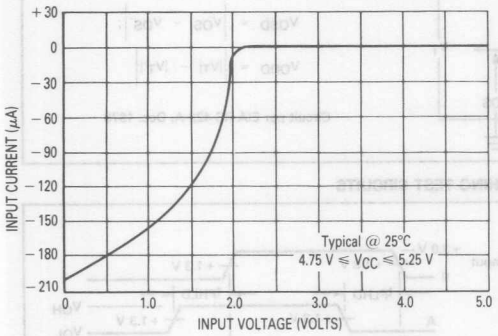


FIGURE 5 — DRIVER DIFFERENTIAL OUTPUT CHARACTERISTICS

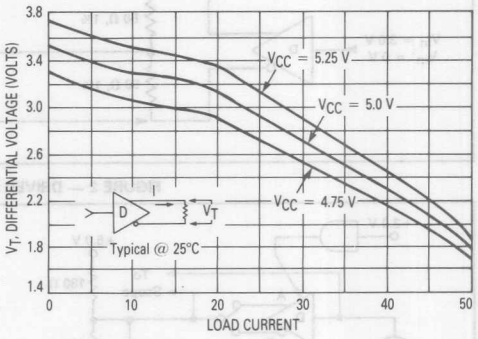


FIGURE 6 — DRIVER OUTPUT VOLTAGE

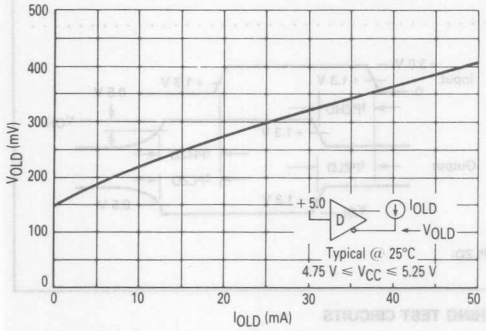


FIGURE 7 — DRIVER OUTPUT VOLTAGE

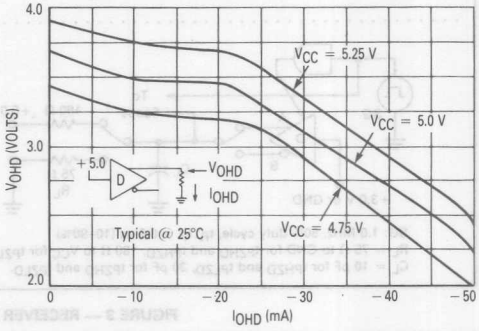


FIGURE 8 — RECEIVER OUTPUT VOLTAGE

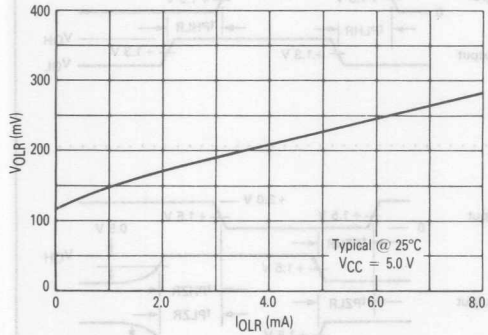
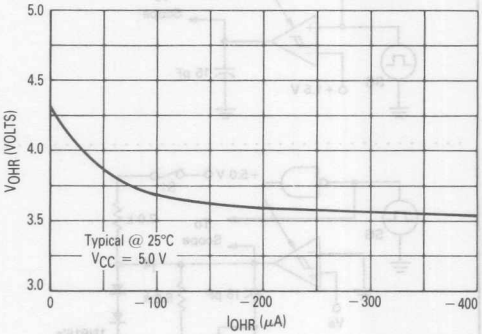


FIGURE 9 — RECEIVER OUTPUT VOLTAGE



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FIGURE 10 — RECEIVER INPUT CHARACTERISTICS

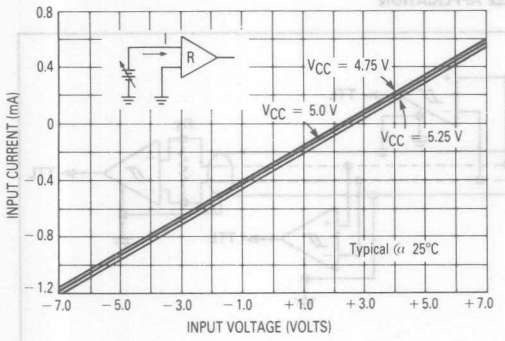


FIGURE 11 — ENABLE INPUT CHARACTERISTICS

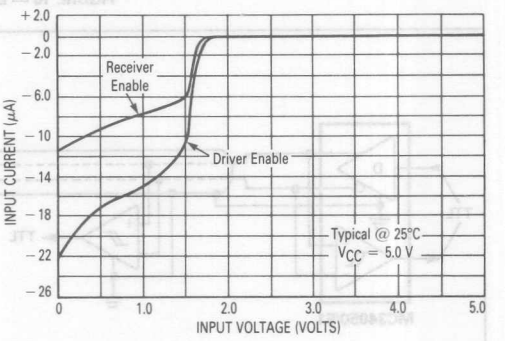


FIGURE 12 — RECEIVER INPUT CHARACTERISTICS

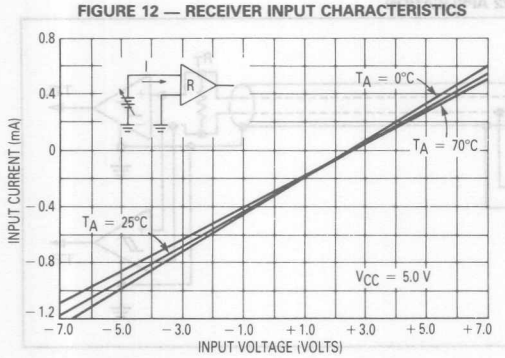


FIGURE 13 — RECEIVER OUTPUT LEAKAGE

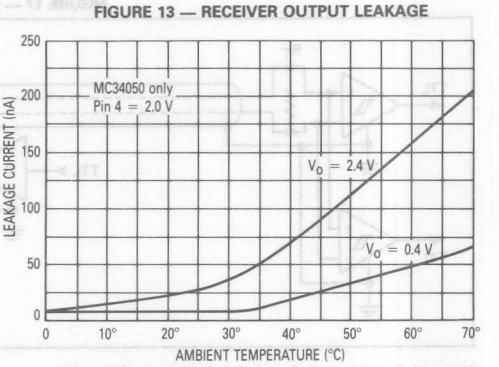


FIGURE 14 — DRIVER OUTPUT VOLTAGE

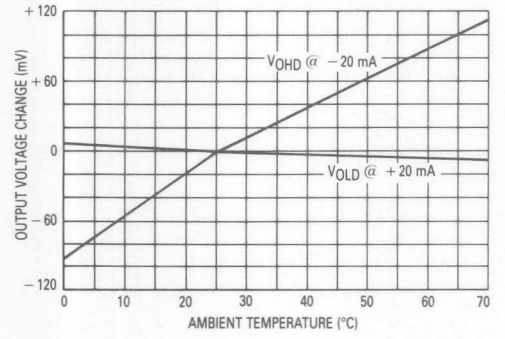
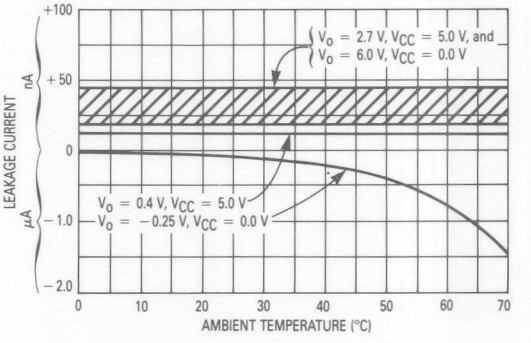


FIGURE 15 — DRIVER OUTPUT LEAKAGE



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FIGURE 16 — EIA-422 APPLICATION

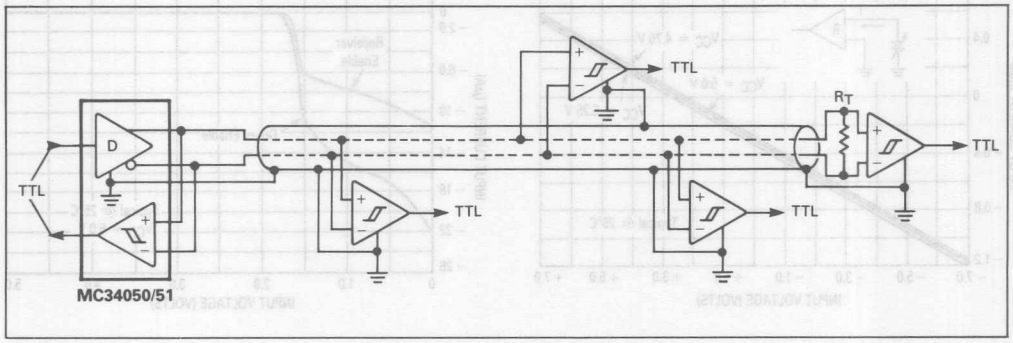
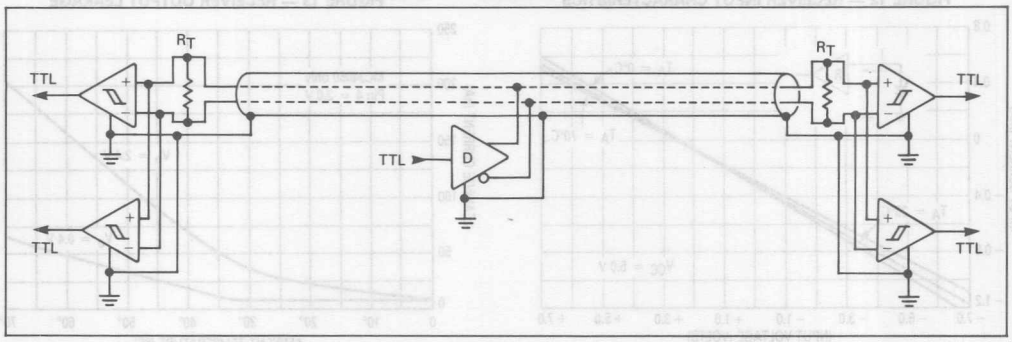


FIGURE 17 — EIA-422 APPLICATION



Notes: 1) R_T must equal characteristic impedance of the cable.
2) Individual receivers may be MC34050, MC34051, MC3486, or AM26LS32.
3) System ground may be made through cable shield as shown, or through chassis ground. Common mode differences and signal quality must be considered when choosing a ground path.

7

MOTOROLA

MC75107
MC75108

DUAL LINE RECEIVERS

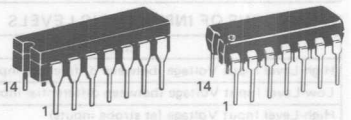
The MC75107 and MC75108 are MTTL compatible dual line receivers featuring independent channels with common voltage supply and ground terminals. The MC75107 circuit features an active pull-up (totem-pole) output. The MC75108 circuit features an open-collector output configuration that permits the Wired-OR logic connection with similar outputs (such as the MC5401/MC7401 MTTL gate or additional MC75108 receivers). Thus a level of logic is implemented without extra delay.

The MC75107 and MC75108 circuits are designed to detect input signals of greater than 25 millivolts amplitude and convert the polarity of the signal into appropriate MTTL compatible output logic levels.

- High Common-Mode Rejection Ratio
- High Input Impedance
- High Input Sensitivity
- Differential Input Common-Mode Voltage Range of ±3.0 V
- Differential Input Common-Mode Voltage of More Than ± 15 V Using External Attenuator
- Strobe Inputs for Receiver Selection
- Gate Inputs for Logic Versatility
- MTTL or MDTL Drive Capability
- High DC Noise Margins
- MC55107 Available as JM38510/10401

DUAL LINE RECEIVERS

SILICON MONOLITHIC
INTEGRATED CIRCUITS

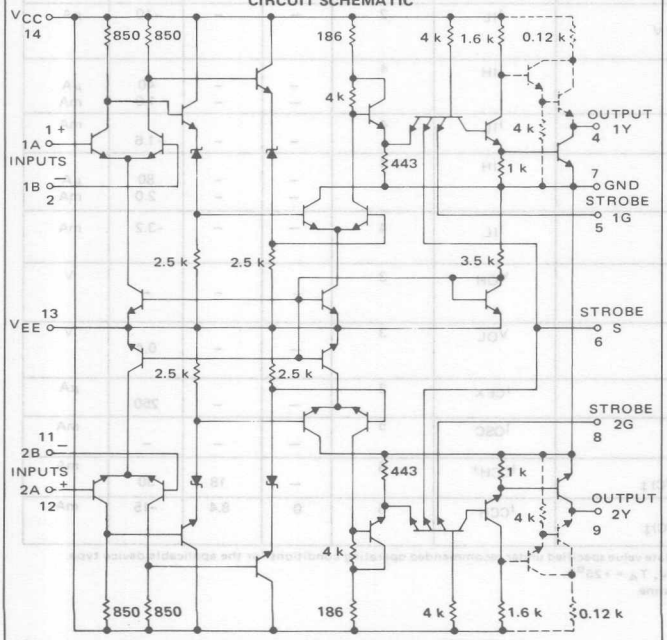


L SUFFIX
CERAMIC PACKAGE
CASE 632-08

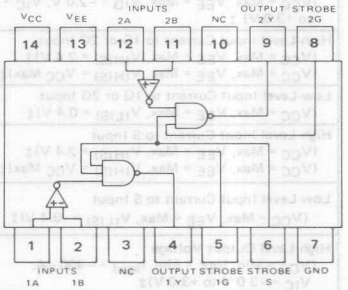
P SUFFIX
PLASTIC PACKAGE
CASE 646-06

7

CIRCUIT SCHEMATIC



Components shown with dashed lines are applicable to the MC75107 only.



TRUTH TABLE

DIFFERENTIAL INPUTS A-B	STROBES G	STROBES S	OUTPUT Y
$V_{ID} > 25$ mV	L or H	L or H	H
	L or H	L	H
-25 mV $< V_{ID} < 25$ mV	L	L or H	H
	H	H	INDETERMINATE
$V_{ID} < -25$ mV	L or H	L	H
	L	L or H	H
	H	H	L

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC} V_{EE}	+7.0 -7.0	Vdc
Differential-Mode Input Signal Voltage Range	V_{ID}	±6.0	Vdc
Common-Mode Input Voltage Range	V_{ICR}	±5.0	Vdc
Strobe Input Voltage	$V_{I(S)}$	5.5	Vdc
Power Dissipation (Package Limitation) Plastic and Ceramic Dual-In-Line Packages Derate above T_A = +25°C	P_D	 625 3.85	 mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltages	V_{CC} V_{EE}	+4.75 -4.75	+5.0 -5.0	+5.25 -5.25	Vdc
Output Sink Current	I_{OS}	–	–	-16	mA
Differential-Mode Input Voltage Range	V_{IDR}	-5.0	–	+5.0	Vdc
Common-Mode Input Voltage Range	V_{ICR}	-3.0	–	+3.0	Vdc
Input Voltage Range, any differential input to ground	V_{IR}	-5.0	–	+3.0	Vdc
Operating Temperature Range	T_A	0	–	+70	°C

DEFINITIONS OF INPUT LOGIC LEVELS

Characteristic	Symbol	Test Fig.	Min	Max	Unit
High-Level Input Voltage (between differential inputs)	V_{IDH}	1	0.025	5.0	Vdc
Low-Level Input Voltage (between differential inputs)	V_{IDL}	1	-5.0†	-0.025	Vdc
High-Level Input Voltage (at strobe inputs)	$V_{IH(S)}$	3	2.0	5.5	Vdc
Low-Level Input Voltage (at strobe inputs)	$V_{IL(S)}$	3	0	0.8	Vdc

†The algebraic convention, where the most positive limit is designated maximum, is used with Low-Level Input Voltage Level (V_{IDL})

ELECTRICAL CHARACTERISTICS (T_A = 0°C to +70°C unless otherwise noted)

Characteristic	Symbol	Test Fig.	Min	Typ #	Max	Unit
High-Level Input Current to 1A or 2A Input (V_{CC} = Max, V_{EE} = Max, V_{ID} = 0.5 V, V_{IC} = -3.0 V to +3.0 V) ‡	I_{IH}	2	–	30	75	μA
Low-Level Input Current to 1A or 2A Input (V_{CC} = Max, V_{EE} = Max, V_{ID} = -2.0 V, V_{IC} = -3.0 V to +3.0 V) ‡	I_{IL}	2	–	–	-10	μA
High-Level Input Current to 1G or 2G Input (V_{CC} = Max, V_{EE} = Max, $V_{IH(S)}$ = 2.4 V)‡ (V_{CC} = Max, V_{EE} = Max, $V_{IH(S)}$ = V_{CC} Max)‡	I_{IH}	4	– –	– –	40 1.0	μA mA
Low-Level Input Current to 1G or 2G Input (V_{CC} = Max, V_{EE} = Max, $V_{IL(S)}$ = 0.4 V)‡	I_{IL}	4	–	–	-1.6	mA
High-Level Input Current to S Input (V_{CC} = Max, V_{EE} = Max, $V_{IH(S)}$ = 2.4 V)‡ (V_{CC} = Max, V_{EE} = Max, $V_{IH(S)}$ = V_{CC} Max)‡	I_{IH}	4	– –	– –	80 2.0	μA mA
Low-Level Input Current to S Input (V_{CC} = Max, V_{EE} = Max, $V_{IL(S)}$ = 0.4 V)‡	I_{IL}	4	–	–	-3.2	mA
High-Level Output Voltage (V_{CC} = Min, V_{EE} = Min, I_{load} = -400 μA, V_{IC} = -3.0 V to +3.0 V)‡	V_{OH}	3	–	–	–	V
Low-Level Output Voltage (V_{CC} = Min, V_{EE} = Min, I_{sink} = 16 mA V_{IC} = -3.0 V to +3.0 V)‡	V_{OL}	3	–	–	0.4	V
High-Level Leakage Current (V_{CC} = Min, V_{EE} = Min, V_{OH} = V_{CC} Max)‡	I_{CEX}	3	–	–	250	μA
Short-Circuit Output Current # # (V_{CC} = Max, V_{EE} = Max)‡	I_{OSC}	5	–	–	–	mA
High Logic Level Supply Current from V_{CC} (V_{CC} = Max, V_{EE} = Max, V_{ID} = 25 mV, T_A = +25°C) ‡	I_{CCH^+}	6	–	18	30	mA
High Logic Level Supply Current from V_{EE} (V_{CC} = Max, V_{EE} = Max, V_{ID} = 25 mV, T_A = +25°C)‡	I_{CCH^-}	6	0	8.4	-15	mA

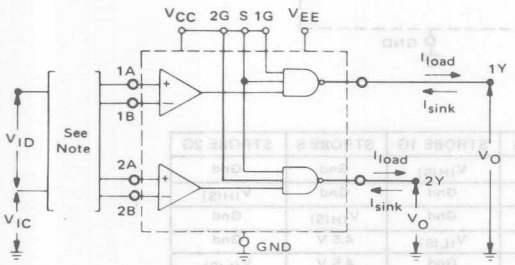
‡For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable device type.
#All typical values are at V_{CC} = +5.0 V, V_{EE} = -5.0 V, T_A = +25°C.
#Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC} = +5.0 V, V_{EE} = -5.0 V, T_A = +25°C)

Characteristic	Symbol	Test Fig.	Min	Typ	Max	Unit
Propagation Delay Time, low-to-high level from differential inputs A and B to output (R_L = 390 Ω, C_L = 50 pF) (R_L = 390 Ω, C_L = 15 pF)	$t_{PLH(D)}$	7	– –	– 19	– 25	ns
Propagation Delay Time, high-to-low level from differential inputs A and B to output (R_L = 390 Ω, C_L = 50 pF) (R_L = 390 Ω, C_L = 15 pF)	$t_{PHL(D)}$	7	– –	– 19	– 25	ns
Propagation Delay Time, low-to-high level, from strobe input G or S to output (R_L = 390 Ω, C_L = 50 pF) (R_L = 390 Ω, C_L = 15 pF)	$t_{PLH(S)}$	7	– –	– 13	– 15	ns
Propagation Delay Time, high-to-low level, from strobe input G or S to output (R_L = 390 Ω, C_L = 50 pF) (R_L = 390 Ω, C_L = 15 pF)	$t_{PHL(S)}$	7	– –	– 13	– 20	ns

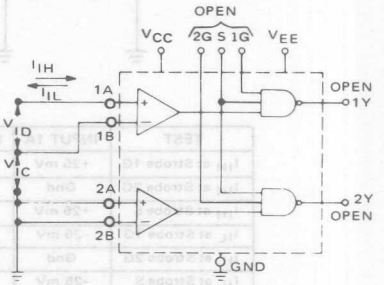
TEST CIRCUITS

FIGURE 1 – V_{IDH} and V_{IDL}



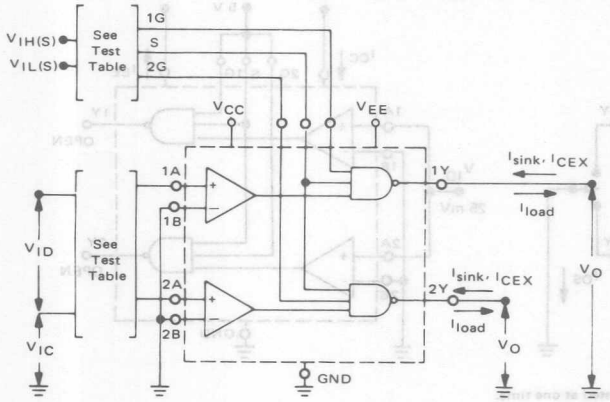
NOTE: When testing one channel, the inputs of the other channel are grounded.

FIGURE 2 – I_{IH} and I_{IL}



NOTE: Each pair of differential inputs is tested separately. The inputs of the other pair are grounded

FIGURE 3 – $V_{IH(S)}$, $V_{IL(S)}$, V_{OH}, V_{OL}, and I_{OH}



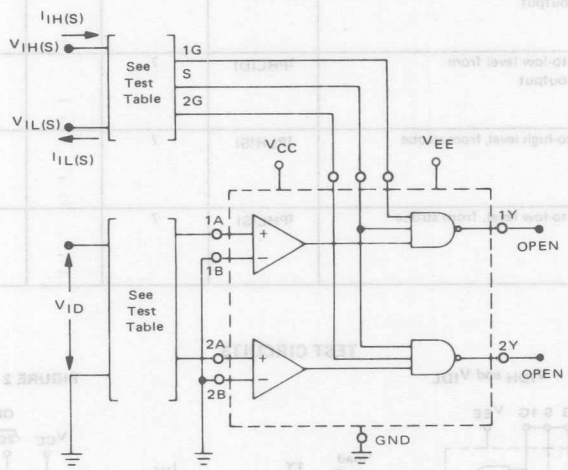
TEST TABLE

MC75107	MC75108	V_{ID}	STROBE 1G or 2G	STROBE S
TEST		APPLY		
V_{OH}	I_{CEX}	+25 mV	$V_{IH(S)}$	$V_{IH(S)}$
V_{OH}	I_{CEX}	-25 mV	$V_{IH(S)}$	$V_{IH(S)}$
V_{OH}	I_{CEX}	-25 mV	$V_{IH(S)}$	$V_{IL(S)}$
V_{OL}	V_{OL}	-25 mV	$V_{IH(S)}$	$V_{IH(S)}$

NOTES: 1. V_{IC} = -3.0 V to +3.0 V.
2. When testing one channel, the inputs of the other channel should be grounded.

TEST CIRCUITS (continued)

FIGURE 4 – $I_{IH(G)}$, $I_{IL(G)}$, $I_{IH(S)}$, and $I_{IL(S)}$



TEST	INPUT 1A	INPUT 2A	STROBE 1G	STROBE S	STROBE 2G
I_{IH} at Strobe 1G	+25 mV	Gnd	$V_{IH(S)}$	Gnd	Gnd
I_{IH} at Strobe 2G	Gnd	+25 mV	Gnd	Gnd	$V_{IH(S)}$
I_{IH} at Strobe S	+25 mV	+25 mV	Gnd	$V_{IH(S)}$	Gnd
I_{IL} at Strobe 1G	-25 mV	Gnd	$V_{IL(S)}$	4.5 V	Gnd
I_{IL} at Strobe 2G	Gnd	-25 mV	Gnd	4.5 V	$V_{IL(S)}$
I_{IL} at Strobe S	-25 mV	-25 mV	4.5 V	$V_{IL(S)}$	4.5 V

FIGURE 5 – I_{OS}

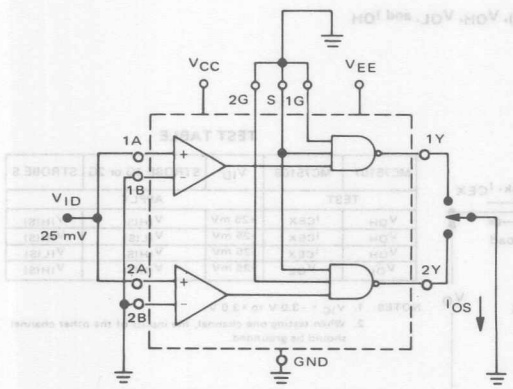
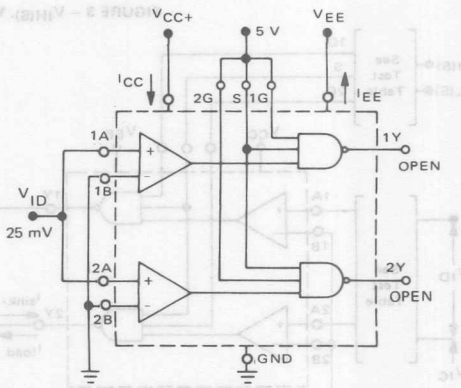


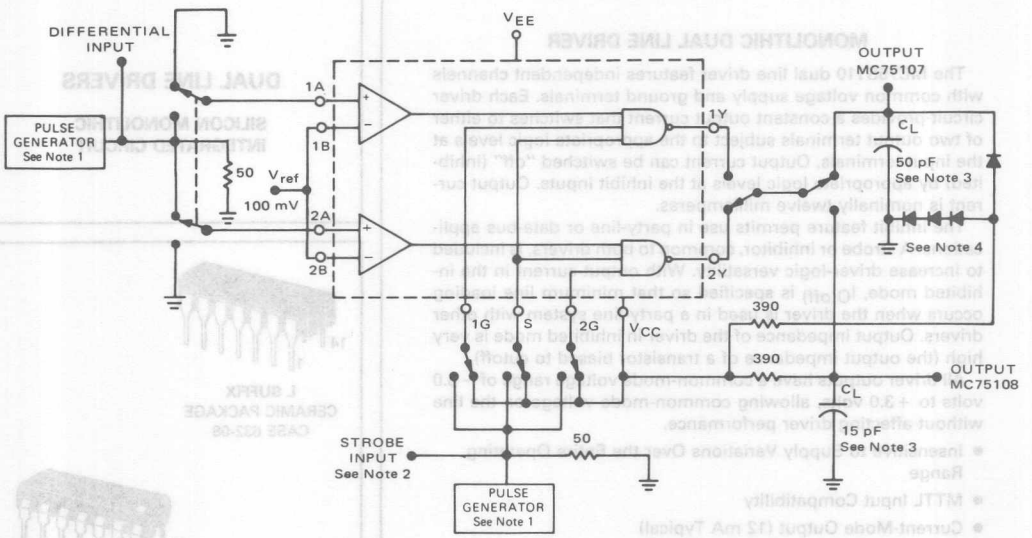
FIGURE 6 – I_{CC} and I_{EE}

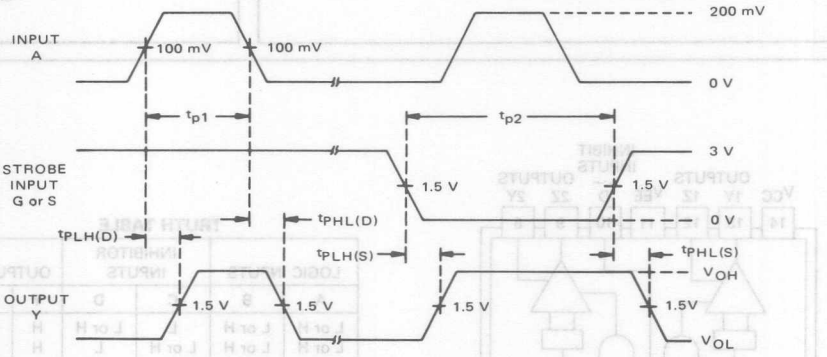


NOTES: 1. Each channel is tested separately.
2. Not more than one output should be tested at one time.

TEST CIRCUITS (continued)

FIGURE 7 – PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS





NOTES: 1. The pulse generators have the following characteristics: $z_o = 50\ \Omega$, $t_r = t_f = 10 \pm 5$ ns, $t_{p1} = 500$ ns, PRR = 1 MHz
$t_{p2} = 1\ \mu s$, PRR = 500 kHz.
2. Strobe input pulse is applied to Strobe 1G when Inputs 1A-1B are being tested, to Strobe S when Inputs 1A-1B or 2A-2B are being tested, and to Strobe 2G when inputs 2A-2B are being tested.
3. C_L includes probe and jig capacitance.
4. All diodes are 1N916 or equivalent.

7

MONOLITHIC DUAL LINE DRIVER

The MC75S110 dual line driver features independent channels with common voltage supply and ground terminals. Each driver circuit provides a constant output current that switches to either of two output terminals subject to the appropriate logic levels at the input terminals. Output current can be switched "off" (inhibited) by appropriate logic levels at the inhibit inputs. Output current is nominally twelve milliamperes.

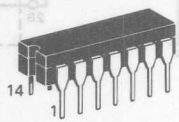
The inhibit feature permits use in party-line or data-bus applications. A strobe or inhibitor, common to both drivers, is included to increase driver-logic versatility. With output current in the inhibited mode, $I_{O(off)}$ is specified so that minimum line loading occurs when the driver is used in a party-line system with other drivers. Output impedance of the driver in inhibited mode is very high (the output impedance of a transistor biased to cutoff).

All driver outputs have a common-mode voltage range of −3.0 volts to +3.0 volts, allowing common-mode voltage on the line without affecting driver performance.

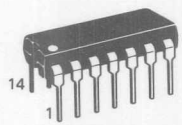
- Insensitive to Supply Variations Over the Entire Operating Range
- MTTL Input Compatibility
- Current-Mode Output (12 mA Typical)
- High Output Impedance
- Common-Mode Output Voltage Range (−3.0 V to +3.0 V)
- Inhibitor Available for Driver Selection

DUAL LINE DRIVERS

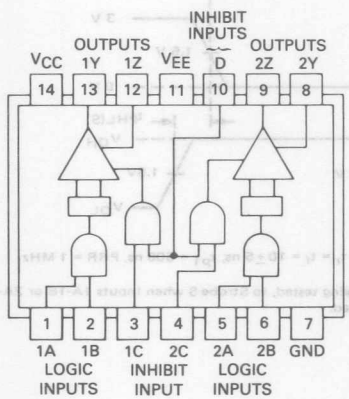
SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 632-08



P SUFFIX
PLASTIC PACKAGE
CASE 646-06



TRUTH TABLE

LOGIC INPUTS		INHIBITOR INPUTS		OUTPUTS	
A	B	C	D	Y	Z
L or H	L or H	L	L or H	H	H
L or H	L or H	L or H	L	H	H
L	L or H	H	H	L	H
L or H	L	H	H	L	H
H	H	H	H	H	L

Low output represents the "on" state.
High output represents the "off" state.

MAXIMUM RATINGS (T_A = 0 to +70°C unless otherwise noted.)

Ratings	Symbol	Value	Unit
Power Supply Voltages (See Note 1)	V_{CC} V_{EE}	+7.0 −7.0	Volts
Logic and Inhibitor Input Voltages (See Note 1)	V_{in}	5.5	Volts
Common-Mode Output Voltage Range (See Note 1)	V_{OCR}	−5.0 to +7.0	Volts
Power Dissipation (Package Limitation) Plastic and Ceramic Dual In-Line Packages Derate above T_A = +25°C	P_D	 1000 3.85	 mW mW/°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

NOTE 1. These voltage values are with respect to the ground terminal.

RECOMMENDED OPERATING CONDITIONS (See Notes 1 and 2.)

Characteristic	Symbol	Min	Nom	Max	Unit
Power Supply Voltages	V_{CC} V_{EE}	+4.75 −4.75	+5.0 −5.0	+5.25 −5.25	Volts
Common-Mode Output Voltage Range	V_{OCR}	−3.0	—	+3.0	Volts

NOTE 2. When using only one channel of the line drivers, the other channel should be inhibited and/or its outputs grounded.

DEFINITIONS OF INPUT LOGIC LEVELS*

Characteristic	Symbol	Test Figure	Min	Max	Unit
High-Level Input Voltage (at any input)	V_{IH}	1,2	2.0	5.25	Volts
Low-Level Input Voltage (at any input)	V_{IL}	1,2	0	0.8	Volts

* The algebraic convention, where the most positive limit is designated maximum, is used with Logic Level Input Voltage Levels only.

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA}\,(Typ)}$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA}\,(Typ)$ = Typical Thermal Resistance Junction to Ambient

ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C unless otherwise noted.)

Characteristic**	Symbol	Test Figure	Min	Typ*	Max	Unit
High-Level Input Current to 1A, 1B, 2A or 2B (V_{CC} = Max, V_{EE} = Max, V_{IH_L} = 2.4 V)* (V_{CC} = Max, V_{EE} = Max, V_{IH_L} = V_{CC} Max)	I_{IH_L}	1	— —	— —	40 1.0	μA mA
Low-Level Input Current to 1A, 1B, 2A or 2B (V_{CC} = Max, V_{EE} = Max, V_{IL_L} = 0.4 V)	I_{IL_L}	1	—	—	−3.0	mA
High-Level Input Current into 1C or 2C (V_{CC} = Max, V_{EE} = Max, V_{IH_I} = 2.4 V) (V_{CC} = Max, V_{EE} = Max, V_{IH_I} = V_{CC} Max)	I_{IH_I}	1	— —	— —	40 1.0	μA mA
Low-Level Input Current into 1C or 2C (V_{CC} = Max, V_{EE} = Max, V_{IL_I} = 0.4 V)	I_{IL_I}	1	—	—	−3.0	mA
High-Level Input Current into D (V_{CC} = Max, V_{EE} = Max, V_{IH_I} = 2.4 V) (V_{CC} = Max, V_{EE} = Max, V_{IH_I} = V_{CC} Max)	I_{IH_I}	1	— —	— —	80 2.0	μA mA
Low-Level Input Current into D (V_{CC} = Max, V_{EE} = Max, V_{IL_I} = 0.4 V)	I_{IL_I}	1	—	—	−6.0	mA
Output Current ("on" state) (V_{CC} = Max, V_{EE} = Max) (V_{CC} = Min, V_{EE} = Min)	$I_{O(on)}$	2	— 6.5	12 —	15 —	mA
Output Current ("off" state) (V_{CC} = Max, V_{EE} = Max) (V_{CC} = Min, V_{EE} = Min)	$I_{O(off)}$	2	— —	— —	100 100	μA
Supply Current from V_{CC} (with driver enabled) (V_{IL_L} = 0.4 V, V_{IH_I} = 2.0 V)	$I_{CC(on)}$	3	—	—	35	mA
Supply Current from V_{EE} (with driver enabled) (V_{IL_L} = 0.4 V, V_{IH_I} = 2.0 V)	$I_{EE(on)}$	3	—	—	−50	mA
Supply Current from V_{CC} (with driver inhibited) (V_{IL_L} = 0.4 V, V_{IL_I} = 0.4 V)	$I_{CC(off)}$	3	—	—	35	mA
Supply Current from V_{EE} (with driver inhibited) (V_{IL_L} = 0.4 V, V_{IL_I} = 0.4 V)	$I_{EE(off)}$	3	—	—	−50	mA

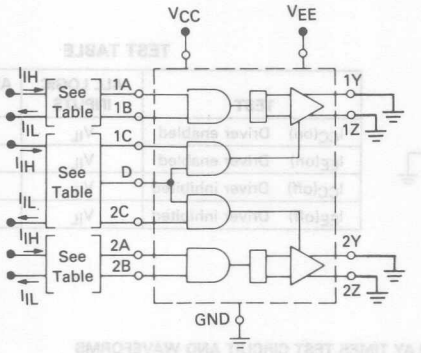
*All typical values are at V_{CC} = +5.0 V, V_{EE} = −5.0 V.
**For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.

SWITCHING CHARACTERISTICS (V_{CC} = +5.0 V, V_{EE} = −5.0 V, T_A = +25°C.)

Characteristic	Symbol	Test Figure	Min	Typ	Max	Unit
Propagation Delay Time from Logic Input A or B to Output Y or Z (R_L = 50 ohms, C_L = 40 pF)	t_{PLH_L} t_{PHL_L}	4	— —	9.0 9.0	15 15	ns
Propagation Delay Time from Inhibitor Input C or D to Output Y or Z (R_L = 50 ohms, C_L = 40 pF)	t_{PLH_I} t_{PHL_I}	4	— —	16 13	25 25	ns

TEST CIRCUITS

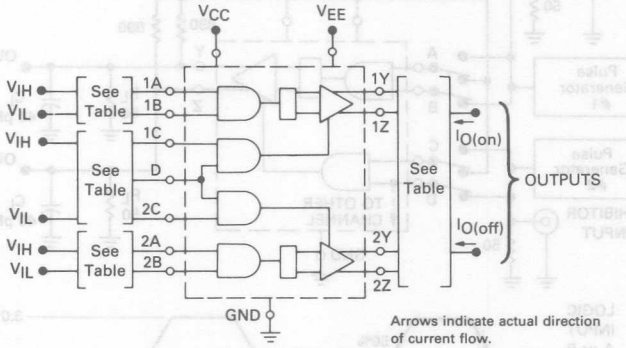
FIGURE 1 — I_{IH}, I_{IL}



TEST TABLE

TEST AT ANY INPUT	ADJACENT INPUTS NOT UNDER TEST
I_{IH}	GND
I_{IL}	4.5 V

FIGURE 2 — $I_{O(on)}$ and $I_{O(off)}$



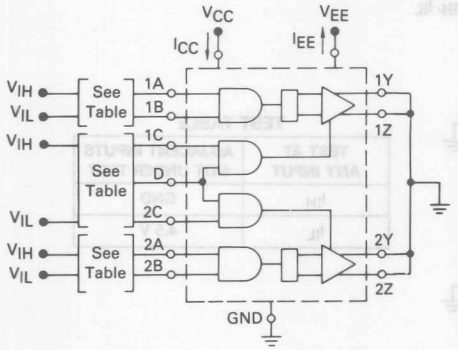
Arrows indicate actual direction of current flow.

TEST TABLE

TEST — Ground all output pins not under test.		LOGIC INPUTS		INHIBITOR INPUTS	
		1A or 2A	1B or 2B	1C or 2C	D
$I_{O(on)}$	at output 1Y or 2Y	V_{IL}	V_{IL}	V_{IH}	V_{IH}
		V_{IL}	V_{IH}		
		V_{IH}	V_{IL}		
$I_{O(on)}$	at output 1Z or 2Z	V_{IH}	V_{IH}	V_{IH}	V_{IH}
$I_{O(off)}$	at output 1Y or 2Y	V_{IH}	V_{IH}	V_{IH}	V_{IH}
$I_{O(off)}$	at output 1Z or 2Z	V_{IL}	V_{IL}	V_{IH}	V_{IH}
		V_{IL}	V_{IH}		
		V_{IH}	V_{IL}		
$I_{O(off)}$	at output 1Y, 2Y, 1Z, or 2Z	Either state	Either state	V_{IL}	V_{IL}
				V_{IL}	V_{IH}
				V_{IH}	V_{IL}

7

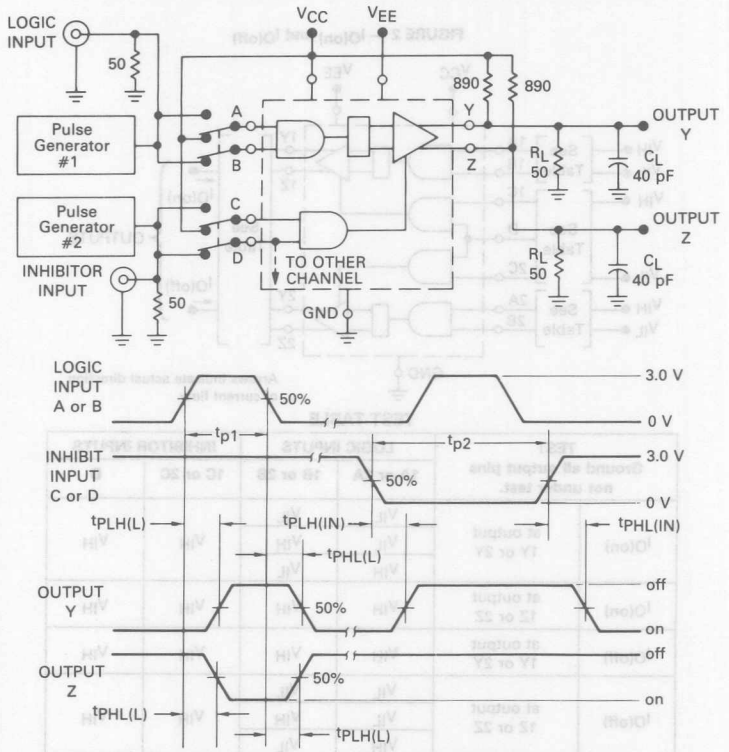
FIGURE 3 — I_{CC} and I_{EE}



TEST TABLE

TEST		ALL LOGIC INPUTS	ALL INHIBITOR INPUTS
I_{CC}(on)	Driver enabled	V_{IL}	V_{IH}
I_{EE}(on)	Driver enabled	V_{IL}	V_{IH}
I_{CC}(off)	Driver inhibited	V_{IL}	V_{IL}
I_{EE}(off)	Driver inhibited	V_{IL}	V_{IL}

FIGURE 4 — PROPAGATION DELAY TIMES TEST CIRCUIT AND WAVEFORMS



NOTES: 1. The pulse generators have the following characteristics: z_o = 50 Ω, t_r = t_f = 10 ± 5.0 ns t_{p1} = 500 ns, PRR = 1.0 MHz, t_{p2} = 1.0 ms, PRR = 500 kHz.
2. C_L includes probe and jig capacitance.
3. For simplicity, only one channel and the inhibitor connections are shown.

MOTOROLA

MC75125
MC75127

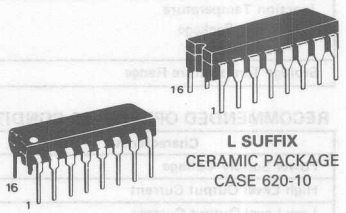
SEVEN CHANNEL LINE RECEIVERS

SEVEN CHANNEL LINE RECEIVERS

The MC75125 and MC75127 are seven-channel line receivers designed to satisfy the requirements of the input/output interface specification for IBM 360/370.

Special low-power design and Schottky-diode-clamped transistors allow low supply-current requirements while maintaining fast switching speeds and high-current TTL outputs. The MC75125 and MC75127 are characterized for operation from 0 to 70°C.

- Meets IBM 360/370 I/O Specification
- Input Resistance — 7 kΩ to 20 kΩ
- Output Compatible with DTL or TTL
- Schottky-Clamped Transistors
- Operates from a Single 5 Volt Supply
- High-Speed — Low Propagation Delay
- Ratio Specification — t_{PLH}/t_{PHL}
- Seven Channels in One 16-Pin Package
- Standard V_{CC} and Ground Positioning on MC75127



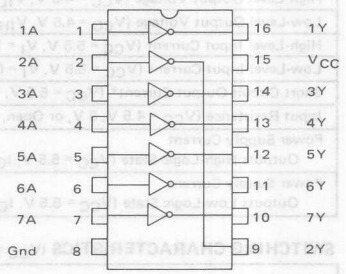
L SUFFIX
CERAMIC PACKAGE
CASE 620-10

P SUFFIX
PLASTIC PACKAGE
CASE 648-06

7

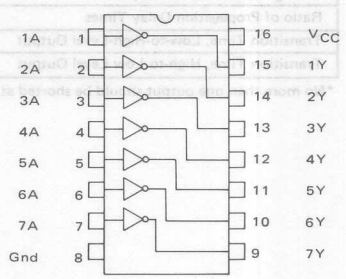
PIN CONNECTIONS

MC75125



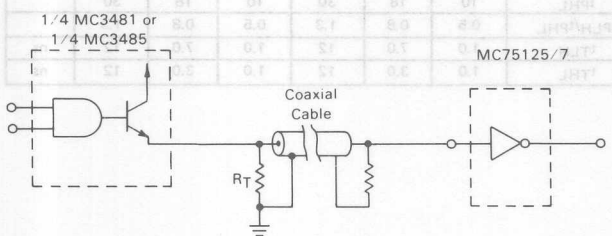
Logic: $Y = \overline{A}$

MC75127



Logic: $Y = \overline{A}$

TYPICAL APPLICATIONS



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+7.0	V
Input Voltage	V_I	−2.0 to +7.0	V
Power Dissipation (Package Limitation) Ceramic Package Plastic Package Derate Above T_A = 25°C	P_D $1/R_{\theta JA}$	 1150 960 7.7	 mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Junction Temperature Ceramic Package Plastic Package	T_J	 +175 +150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	Vdc
High Level Output Current	I_{OH}	–	–	−0.4	mA
Low Level Output Current	I_{OL}	–	–	16	mA
Operating Ambient Temperature Range	T_A	0	–	+70	°C

7

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, these specifications apply over recommended power supply and temperature ratings. Typical values measured at T_A = 25°C and V_{CC} = +5.0 V)

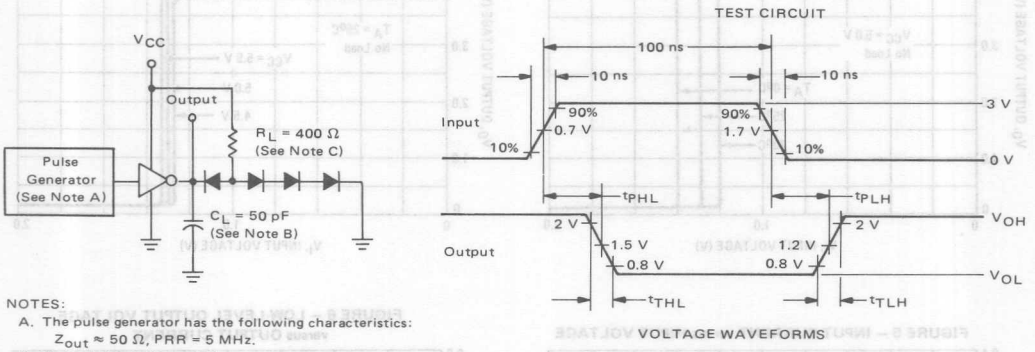
Characteristic	Symbol	Min	Typ	Max	Unit
High-Level Input Voltage	V_{IH}	1.7	–	–	V
Low-Level Input Voltage	V_{IL}	–	–	0.7	V
High-Level Output Voltage (V_{CC} = 4.5 V, V_{IL} = 0.7 V, I_{OH} = −0.4 mA)	V_{OH}	2.4	3.1	–	V
Low-Level Output Voltage (V_{CC} = 4.5 V, V_{IH} = 1.7 V, I_{OL} = 16 mA)	V_{OL}	–	0.4	0.5	V
High-Level Input Current (V_{CC} = 5.5 V, V_I = 3.11 V)	I_{IH}	0.2	0.3	0.42	mA
Low-Level Input Current (V_{CC} = 5.5 V, V_I = 0.15 V)	I_{IL}	–	–	−0.24	mA
Short Circuit Output Current* (V_{CC} = 5.5 V, V_O = 0)	I_{OS}	−18	–	−60	mA
Input Resistance (V_{CC} = 4.5 V, 0 V, or Open, ΔV_I = 0.15 V to 4.15 V)	r_i	7.4	–	20	kΩ
Power Supply Current Outputs High-Logic State (V_{CC} = 5.5 V, I_{OH} = −0.4 mA, all inputs at 0.7 V)	I_{CCH}	–	15	25	mA
Power Supply Current Outputs Low-Logic State (V_{CC} = 5.5 V, I_{OL} = 16 mA, all inputs at 4.0 V)	I_{CCL}	–	28	47	mA

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C, R_L = 400 Ω, C_L = 50 pF, unless otherwise noted. See Figure 1)

Characteristic	Symbol	MC75125			MC75127			Unit
		Min	Typ	Max	Min	Typ	Max	
Propagation Delay Time Low-to-High-Level Output High-to-Low-Level Output	 t_{PLH} t_{PHL}	 7.0 10	 14 18	 25 30	 7.0 10	 14 18	 25 30	ns
Ratio of Propagation Delay Times	t_{PLH}/t_{PHL}	0.5	0.8	1.3	0.5	0.8	1.3	
Transition Time, Low-to-High-Level Output	t_{TLH}	1.0	7.0	12	1.0	7.0	12	ns
Transition Time, High-to-Low Level Output	t_{THL}	1.0	3.0	12	1.0	3.0	12	ns

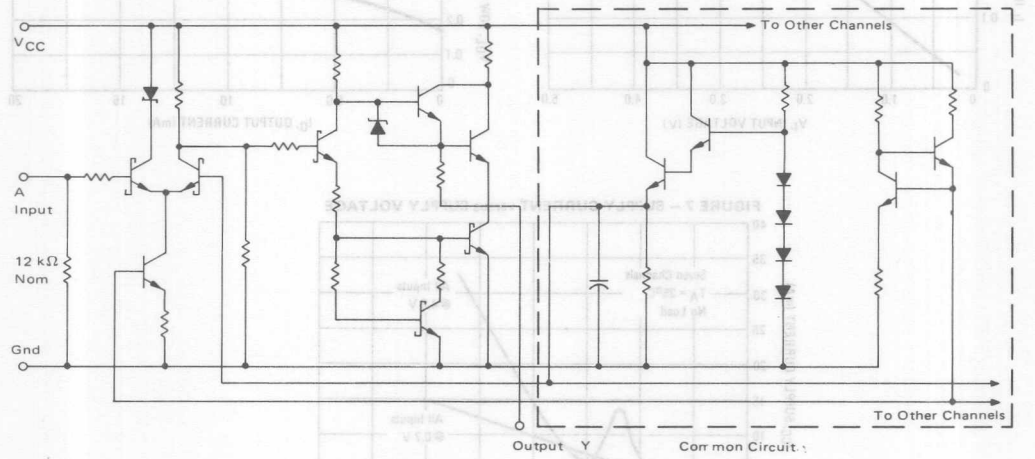
*No more than one output should be shorted at a time.

FIGURE 1 – PARAMETER MEASUREMENT INFORMATION



NOTES:
A. The pulse generator has the following characteristics: $Z_{out} \approx 50\ \Omega$, PRR = 5 MHz.
B. C_L includes probe and jig capacitance.
C. All diodes are MMD7000 or equivalent.

FIGURE 2 – SCHEMATIC (EACH RECEIVER)



7

TYPICAL CHARACTERISTICS

FIGURE 3 – VOLTAGE TRANSFER CHARACTERISTICS versus AMBIENT TEMPERATURE

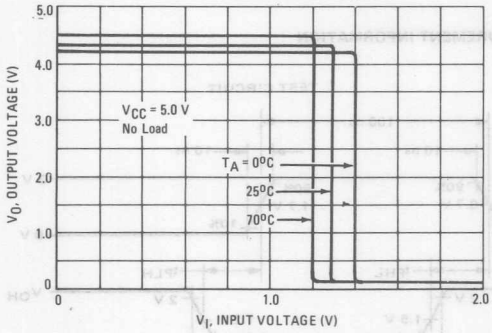


FIGURE 4 – VOLTAGE TRANSFER CHARACTERISTIC versus SUPPLY VOLTAGE

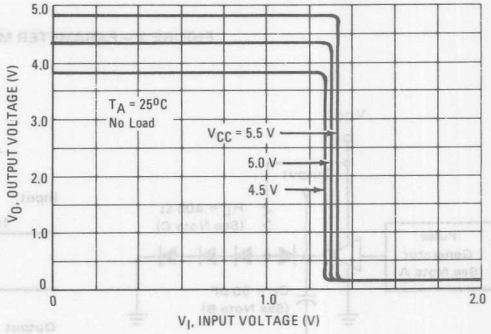


FIGURE 5 – INPUT CURRENT versus INPUT VOLTAGE

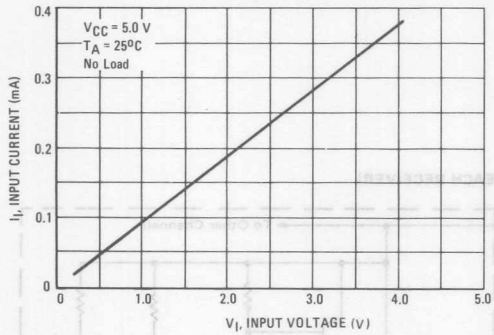


FIGURE 6 – LOW-LEVEL OUTPUT VOLTAGE versus OUTPUT CURRENT

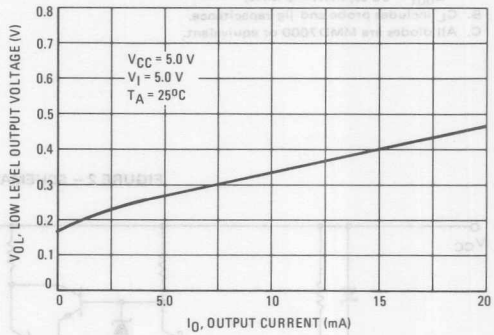
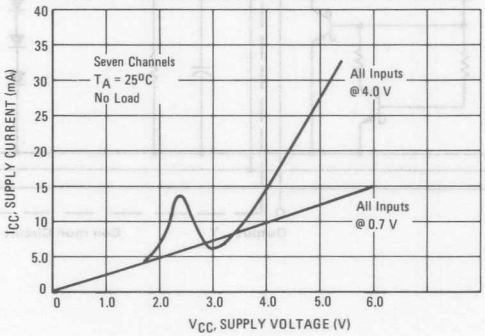


FIGURE 7 – SUPPLY CURRENT versus SUPPLY VOLTAGE



MOTOROLA

MC75128
MC75129

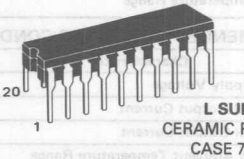
EIGHT-CHANNEL LINE RECEIVERS

EIGHT-CHANNEL LINE RECEIVERS

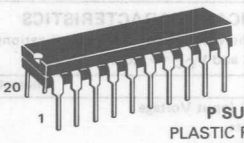
The MC75128 and MC75129 are eight-channel line receivers designed to satisfy the requirements of the input/output interface specification for IBM 360/370. Both devices feature common strobes for each group of four receivers. The MC75128 has an active high strobe; the MC75129 has an active low strobe.

Special low-power design and Schottky-diode-clamped transistors allow low supply current requirements while maintaining fast switching speeds and high-current TTL outputs. Both devices are characterized for operation from 0 to 70°C.

- Meets IBM 360/370 I/O Specification
- Input Resistance – 7 kΩ to 20 kΩ
- Output Compatible with DTL or TTL
- Schottky-Clamped Transistors
- Operates from a Single 5 Volt Supply
- High-Speed – Low Propagation Delay
- Ratio Specification – t_{PLH}/t_{PHL}
- Common Strobe for Each Group of Four Receivers
- MC75128 Strobe – Active-High
  MC75129 Strobe – Active-Low



L SUFFIX
CERAMIC PACKAGE
CASE 732-03

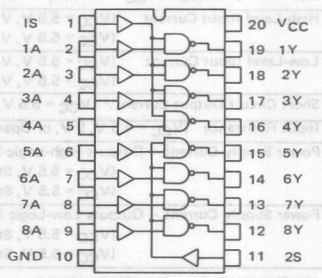


P SUFFIX
PLASTIC PACKAGE
CASE 738-03

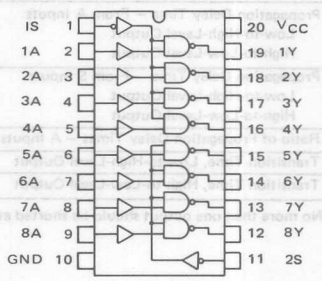
7

PIN CONNECTIONS

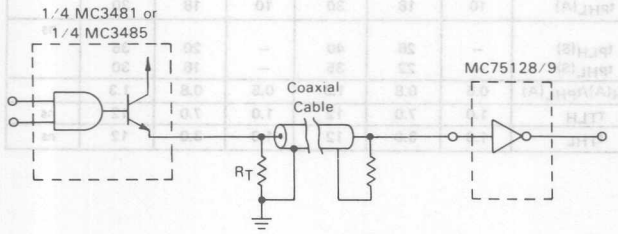
MC75128



MC75129



TYPICAL APPLICATION



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+7.0	V
A Input Voltage	V_{IA}	−0.15 to +7.0	V
Strobe Input Voltage	V_{IS}	+7.0	V
Power Dissipation (Package Limitation)			
Ceramic Package	P_D	1150	mW
Plastic Package		960	
Derate Above T_A = 25°C	$1/R_{\theta JA}$	−7.7	mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Junction Temperature	T_J		°C
Ceramic Package		+175	
Plastic Package		+150	
Storage Temperature Range	T_{stg}	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	Vdc
High Level Output Current	I_{OH}	–	–	−0.4	mA
Low Level Output Current	I_{OL}	–	–	16	mA
Operating Ambient Temperature Range	T_A	0	–	+70	°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, these specifications apply over recommended power supply and temperature ratings. Typical values measured at T_A = 25°C and V_{CC} = +5.0 V)

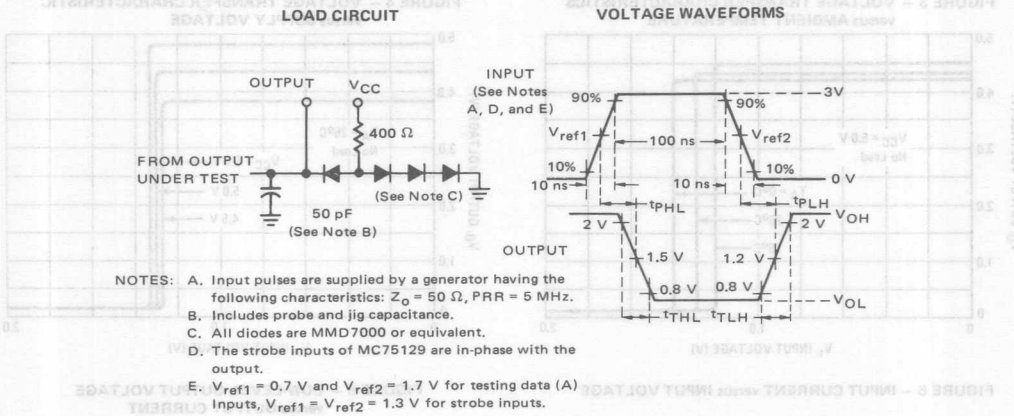
Characteristic	Symbol	Min	Typ	Max	Unit
High-Level Input Voltage	V_{IH}				V
A Inputs		1.7	–	–	
S Inputs		2.0	–	–	
Low-Level Input Voltage	V_{IL}				V
A Inputs		–	–	0.7	
S Inputs		–	–	0.7	
High-Level Output Voltage (V_{CC} = 4.5 V, V_{IL} = 0.7 V, I_{OH} = −0.4 mA)	V_{OH}	2.4	3.1	–	V
Low-Level Output Voltage (V_{CC} = 4.5 V, V_{IH} = 1.7 V, I_{OL} = 16 mA)	V_{OL}	–	0.4	0.5	V
Input Clamp Voltage (V_{CC} = 4.5 V, I_I = −18 mA, S Inputs)	V_{IK}	–	–	−1.5	V
High-Level Input Current (V_{CC} = 5.5 V, V_I = 3.11 V, A Inputs)	I_{IH}	–	0.3	0.42	mA
(V_{CC} = 5.5 V, V_I = 2.7 V, S Inputs)		–	–	20	μA
Low-Level Input Current (V_{CC} = 5.5 V, V_I = 0.15 V, A Inputs)	I_{IL}	–	–	−0.24	mA
(V_{CC} = 5.5 V, V_I = 0.4 V, S Inputs)		–	–	−0.4	
Short Circuit Output Current * (V_{CC} = 5.5 V, V_O = 0)	I_{OS}	−18	–	−60	mA
Input Resistance (V_{CC} = 4.5 V, 0 V, or Open, ΔV_I = 0.15 V to 4.15 V)	r_i	7.0	–	20	kΩ
Power Supply Current — Outputs High-Logic State, all inputs at 0.7 V	I_{CCH}				mA
(V_{CC} = 5.5 V, Strobe at 2.4 V — MC75128)		–	19	31	
(V_{CC} = 5.5 V, Strobe at 0.4 V — MC75129)		–	19	31	
Power Supply Current — Outputs Low-Logic State, all inputs at 4.0 V	I_{CCL}				mA
(V_{CC} = 5.5 V, Strobe at 2.4 V — MC75128)		–	32	53	
(V_{CC} = 5.5 V, Strobe at 0.4 V — MC75129)		–	32	53	

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C, R_L = 400 Ω, C_L = 50 pF, unless otherwise noted, See Figures 1 and 2)

Characteristic	Symbol	MC75128			MC75129			Unit
		Min	Typ	Max	Min	Typ	Max	
Propagation Delay Time — From A Inputs								ns
Low-to-High-Level Output	t_{PLH}(A)	7.0	14	25	7.0	14	25	
High-to-Low-Level Output	t_{PHL}(A)	10	18	30	10	18	30	
Propagation Delay Time — From S Inputs								ns
Low-to-High-Level Output	t_{PLH}(S)	–	26	40	–	20	35	
High-to-Low-Level Output	t_{PHL}(S)	–	22	35	–	16	30	
Ratio of Propagation Delay Times — A Inputs	t_{PLH}(A)/t_{PHL}(A)	0.5	0.8	1.3	0.5	0.8	1.3	
Transition Time, Low-to-High-Level Output	t_{TLH}	1.0	7.0	12	1.0	7.0	12	ns
Transition Time, High-to-Low-Level Output	t_{THL}	1.0	3.0	12	1.0	3.0	12	ns

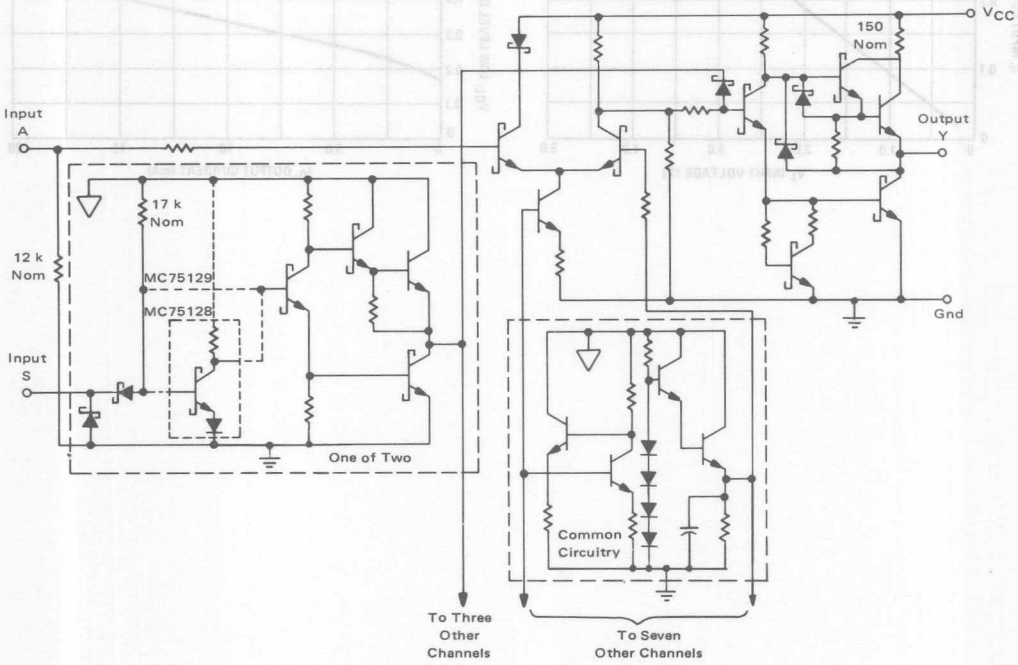
*No more than one output should be shorted at a time.

FIGURE 1 – PARAMETER MEASUREMENT INFORMATION



NOTES: A. Input pulses are supplied by a generator having the following characteristics: Z_o = 50 Ω, PRR = 5 MHz.
B. Includes probe and jig capacitance.
C. All diodes are MMD7000 or equivalent.
D. The strobe inputs of MC75129 are in-phase with the output.
E. V_{ref1} = 0.7 V and V_{ref2} = 1.7 V for testing data (A) inputs, V_{ref1} = V_{ref2} = 1.3 V for strobe inputs.

FIGURE 2 – SCHEMATIC (EACH RECEIVER)



7

TYPICAL CHARACTERISTICS

FIGURE 3 – VOLTAGE TRANSFER CHARACTERISTICS versus AMBIENT TEMPERATURE

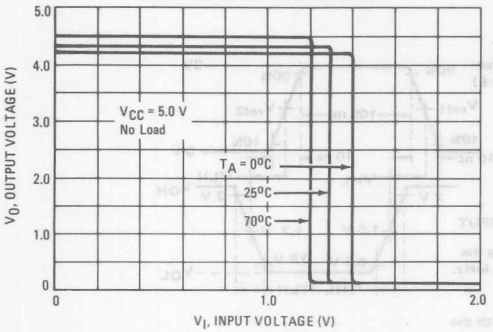


FIGURE 4 – VOLTAGE TRANSFER CHARACTERISTIC versus SUPPLY VOLTAGE

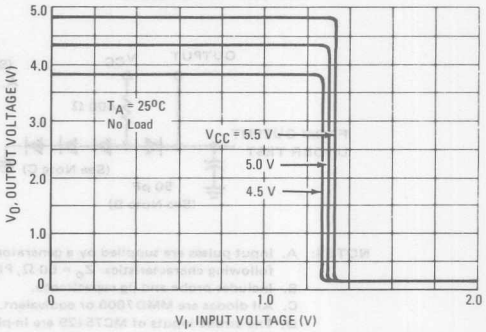


FIGURE 5 – INPUT CURRENT versus INPUT VOLTAGE

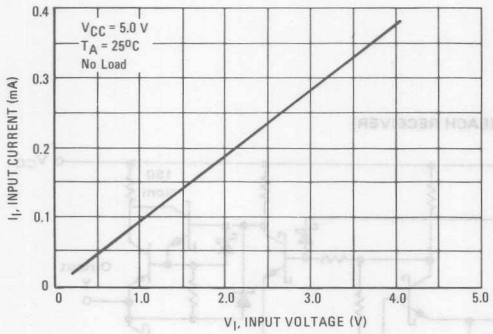
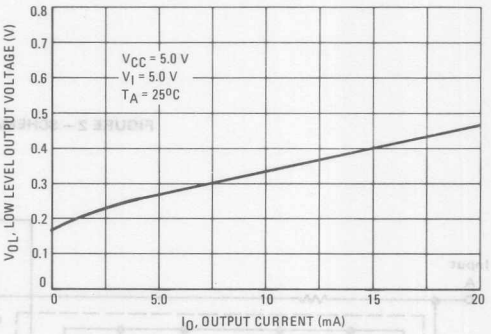


FIGURE 6 – LOW-LEVEL OUTPUT VOLTAGE versus OUTPUT CURRENT



7

MOTOROLA

SN75172
SN75174

Product Preview

QUAD LINE DRIVERS WITH NAND ENABLED THREE-STATE OUTPUTS

The Motorola SN75172/174 are monolithic quad differential line drivers with three-state outputs. They are designed specifically to meet the requirements of EIA-485, EIA-422A Standards and CCITT recommendations V.11 and X.27.

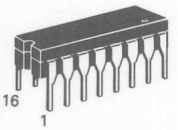
The device is optimized for balanced multipoint bus transmission at rates up to 4 megabits per second. Each driver features wide positive and negative common-mode output voltage ranges making it suitable for party-line applications in noisy environments.

The SN75172/174 provides positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. Shutdown occurs at a junction temperature of approximately 150°C. These devices offer optimum performance when used with the SN75173 or SN75175 quadruple differential line receivers.

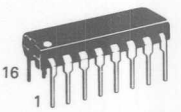
- Meets EIA-485 Standard for Party-Line Operation
- Meets EIA Standard EIA-422A and CCITT Recommendations V.11 and X.27
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Outputs
- Common Mode Output Voltage Range . . . −7.0 V to 12 V
- Active High and Active Low Enables
- Thermal Shutdown Protection
- Positive and Negative Current Limiting
- Operates from Single 5.0 Volt Supply
- Low Power Requirements
- Functionally Interchangeable With
  AM26LS31 (SN75172)
  MC3487 (SN75174)

QUAD EIA-485 LINE DRIVERS WITH THREE-STATE OUTPUTS

SILICON MONOLITHIC INTEGRATED CIRCUIT



J SUFFIX
CERAMIC PACKAGE
CASE 620-10

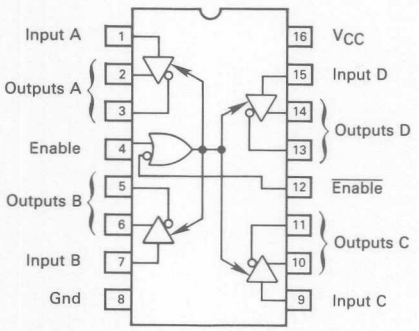


N SUFFIX
PLASTIC PACKAGE
CASE 648-06

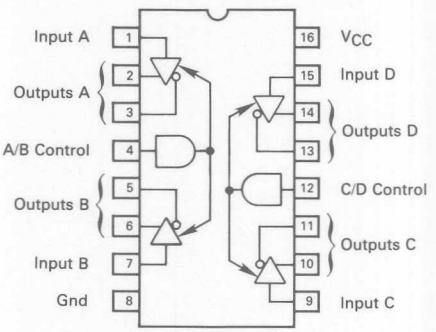
7

PIN CONNECTIONS

SN75172



SN75174



This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

SN75172

TRUTH TABLE			
Input	Control Inputs (E/$\overline{E}$)	Noninverting Output	Inverting Output
H	H/L	H	L
L	H/L	L	H
X	L/H	Z	Z

L = Low Logic State
H = High Logic State
X = Irrelevant
Z = Third-State (High Impedance)

SN75174

TRUTH TABLE			
Input	Control Input	Noninverting Output	Inverting Output
H	H	H	L
L	H	L	H
X	L	Z	Z

L = Low Logic State
H = High Logic State
X = Irrelevant
Z = Third-State (High Impedance)

MOTOROLA

SN75173
SN75175

Advance Information

QUAD EIA-485 LINE RECEIVERS

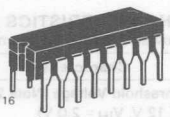
The Motorola SN75173/175 are monolithic quad differential line receivers with three-state outputs. They are designed specifically to meet the requirements of EIA-485, EIA-422A/23A Standards and CCITT recommendations.

The devices are optimized for balanced multipoint bus transmission at rates up to 10 megabits per second. They also feature high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 millivolts over a common mode input voltage range of −12 volts to 12 volts. The SN75173/175 are designed for optimum performance when used with the SN75172 or SN75174 quad differential line drivers.

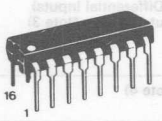
- Meets EIA Standards EIA-422A and EIA-423A, EIA-485
- Meets CCITT Recommendations V.10, V.11, X.26, and X.27
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Outputs
- Common-Mode Input Voltage Range . . . −12 V to 12 V
- Input Sensitivity . . . ±200 mV
- Input Hysteresis . . . 50 mV Typ
- High Input Impedance . . . 1 EIA-485 Unit Load
- Operates from Single 5.0 V Supply
- Low Power Requirements
- Plug-In Replacement for MC3486 (SN75175)
  AM26LS32 (SN75173)

QUAD EIA-485 LINE RECEIVERS WITH THREE-STATE OUTPUTS

SILICON MONOLITHIC INTEGRATED CIRCUITS



J SUFFIX
CERAMIC PACKAGE
CASE 620-10

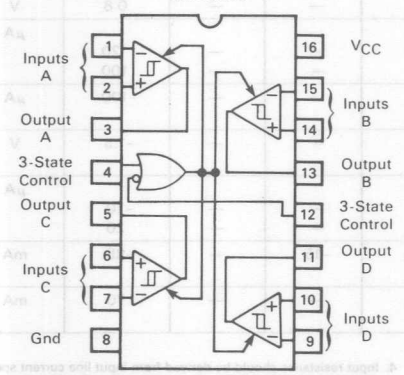


N SUFFIX
PLASTIC PACKAGE
CASE 648-06

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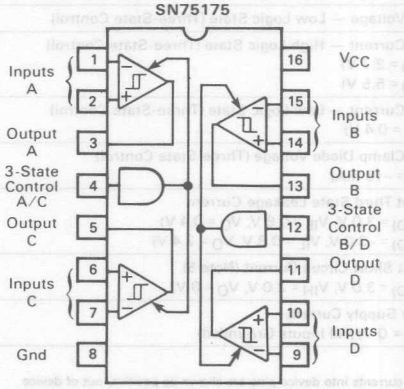
PIN CONNECTIONS

SN75173



ORDERING INFORMATION		
Device	Temperature	Package
SN75173J	0 to +70°C	Ceramic DIP
SN75173N	0 to +70°C	Plastic DIP

SN75175



ORDERING INFORMATION		
Device	Temperature	Package
SN75175J	0 to +70°C	Ceramic DIP
SN75175N	0 to +70°C	Plastic DIP

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Power Supply Voltage	V_{CC}	7.0	Vdc
Input Common Mode Voltage	V_{ICM}	±25	Vdc
Input Differential Voltage	V_{ID}	±25	Vdc
Three-State Control Input Voltage	V_I	7.0	Vdc
Output Sink Current	I_O	50	mA
Storage Temperature	T_{stg}	-65 to +150	°C
Operating Junction Temperature — Ceramic Package — Plastic Package	T_J	+175 +150	°C

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	4.75 to 5.25	Vdc
Operating Ambient Temperature	T_A	0 to +70	°C
Input Common Mode Voltage Range	V_{ICM}	-12 to +12	Vdc
Input Differential Voltage Range	V_{IDR}	-12 to +12	Vdc

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, minimum and maximum limits apply over recommended temperature and power supply voltage ranges. Typical values are for T_A =25°C, V_{CC} = 5.0 V and V_{ICM} = 0 V) (Note 1)

Characteristic	Symbol	Min	Typ	Max	Unit
Differential Input Threshold Voltage (Note 2) (-12 V ≤ V_{ICM} ≤ 12 V, V_{IH} = 2.0 V) (I_O = -0.4 mA, V_{OH} ≥ 2.7 V) (I_O = 16 mA, V_{OL} ≤ 0.5 V)	$V_{TH(D)}$	 — —	 — —	 0.2 -0.2	V
Input Hysteresis	$V_{T+} - V_{T-}$	—	50	—	mV
Input Line Current (Differential Inputs) (Unmeasured Input at 0 V — Note 3) (V_I = +12 V) (V_I = -7.0 V)	I_I	 — —	 — —	 1.0 -0.8	mA
Input Resistance (Note 4)	r_i	1 Unit Load	—	—	
Input Balance and Output Level (Note 3) (-12 V ≤ V_{ICM} ≤ 12 V, V_{IH} = 2.0 V) (I_O = -0.4 mA, V_{ID} = 0.2 V) (I_O = 8.0 mA, V_{ID} = -0.2 V) (I_O = 16 mA, V_{ID} = -0.2 V)	 V_{OH} V_{OL} V_{OL}	 2.7 — —	 — — —	 — 0.45 0.5	V
Input Voltage — High Logic State (Three-State Control)	V_{IH}	2.0	—	—	V
Input Voltage — Low Logic State (Three-State Control)	V_{IL}	—	—	0.8	V
Input Current — High Logic State (Three-State Control) (V_{IH} = 2.7 V) (V_{IH} = 5.5 V)	I_{IH}	 — —	 — —	 20 100	μA
Input Current — Low Logic State (Three-State Control) (V_{IL} = 0.4 V)	I_{IL}	—	—	-100	μA
Input Clamp Diode Voltage (Three-State Control) (I_{IK} = -18 mA)	V_{IK}	—	—	-1.5	V
Output Third State Leakage Current ($V_{I(D)}$ = 3.0 V, V_{IL} = 0.8 V, V_O = 0.4 V) ($V_{I(D)}$ = -3.0 V, V_{IL} = 0.8 V, V_O = 2.4 V)	I_{OZ}	 — —	 — —	 -20 20	μA
Output Short-Circuit Current (Note 5) ($V_{I(D)}$ = 3.0 V, V_{IH} = 2.0 V, V_O = 0 V)	I_{OS}	-15	—	-85	mA
Power Supply Current (V_{IL} = 0 V) (All Inputs Grounded)	I_{CC}	—	—	70	mA

NOTES:
1. All currents into device pins are shown as positive, out of device pins are negative. All voltages referenced to ground unless otherwise noted.
2. Differential input threshold voltage and guaranteed output levels are done simultaneously for worst case.
3. Refer to EIA-485 for exact conditions. Input balance and guaranteed output levels are done simultaneously for worst case.
4. Input resistance should be derived from input line current specifications and is shown for reference only. See EIA-485 and input line current specifications for more specific input resistance information.
5. Only one output at a time should be shorted.

SWITCHING CHARACTERISTICS (Unless otherwise noted, V_{CC} = 5.0 V and T_A = 25°C)

Characteristic	Symbol	SN75173			SN75175			Unit
		Min	Typ	Max	Min	Typ	Max	
Propagation Delay Time — Differential Inputs to Output								ns
(Output High to Low)	$t_{PHL(D)}$	—	25	35	—	25	35	
(Output Low to High)	$t_{PLH(D)}$	—	25	35	—	25	35	
Propagation Delay Time — Three-State Control to Output								ns
(Output Low to Third State)	t_{PLZ}	—	20	40	—	16	35	
(Output High to Third State)	t_{PHZ}	—	20	30	—	19	35	
(Output Third State to High)	t_{PZH}	—	16	22	—	11	30	
(Output Third State to Low)	t_{PZL}	—	16	25	—	11	30	

SN75173

FUNCTION TABLE (EACH RECEIVER)

Differential Inputs	3-State Control		Output Y
	4	12	
$V_{ID} \geq 0.2$ V	H	X	H
	X	L	H
$-0.2\ V < V_{ID} < 0.2$ V	H	X	?
	X	L	?
$V_{ID} \leq -0.2$ V	H	X	L
	X	L	L
X	L	H	Z

SN75175

FUNCTION TABLE (EACH RECEIVER)

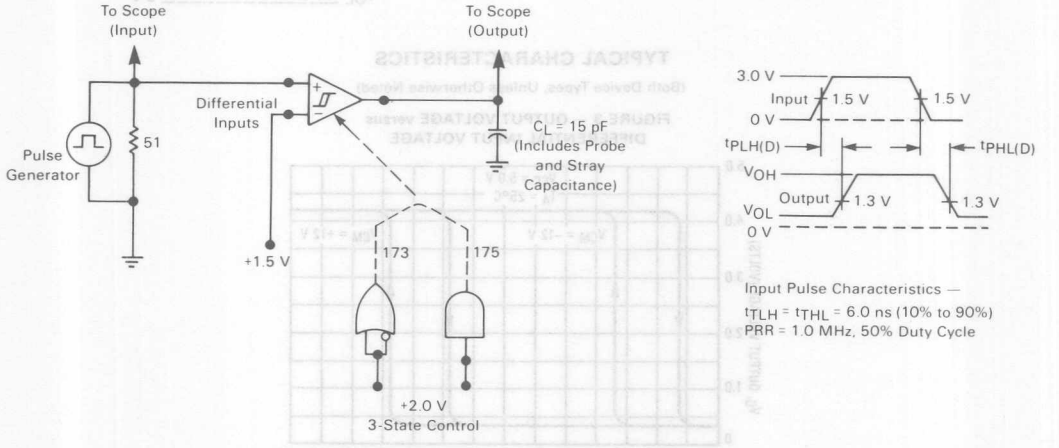
Differential Inputs	3-State Control	Output Y
$V_{ID} \geq 0.2$ V	H	H
$-0.2\ V < V_{ID} < 0.2$ V	H	?
$V_{ID} \leq -0.2$ V	H	L
X	L	Z

H = high level
L = low level
X = irrelevant
? = indeterminate
Z = high-impedance (off)

7

SWITCHING TEST CIRCUIT AND WAVEFORMS

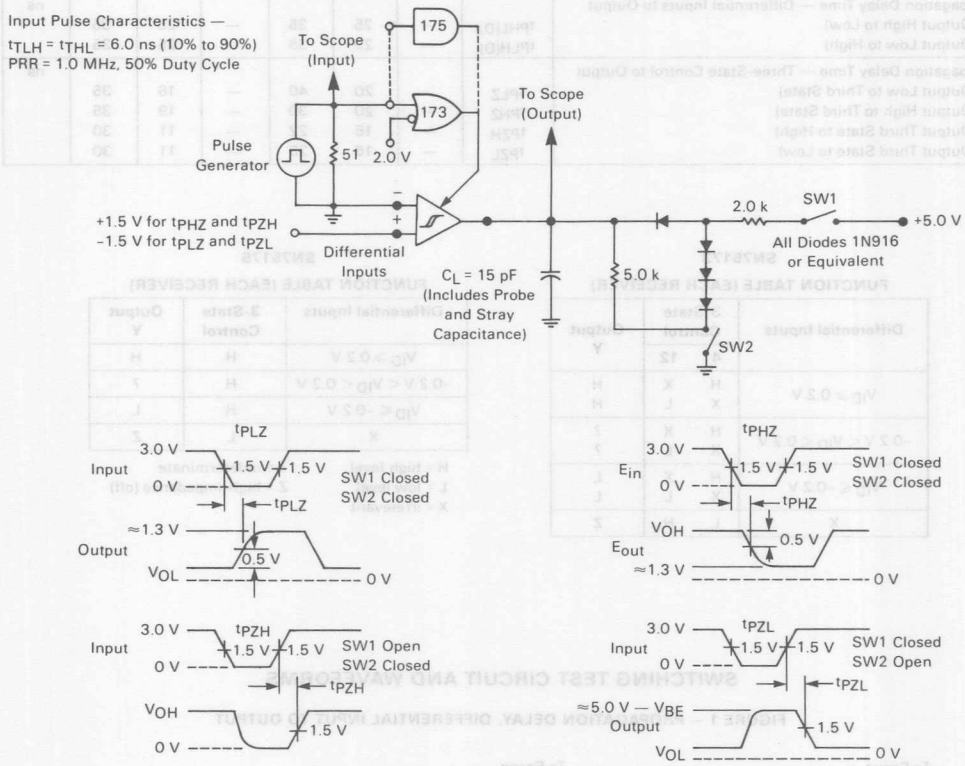
FIGURE 1 — PROPAGATION DELAY, DIFFERENTIAL INPUT TO OUTPUT



Input Pulse Characteristics —
$t_{TLH} = t_{THL}$ = 6.0 ns (10% to 90%)
PRR = 1.0 MHz, 50% Duty Cycle

SWITCHING TEST CIRCUIT AND WAVEFORMS (continued)

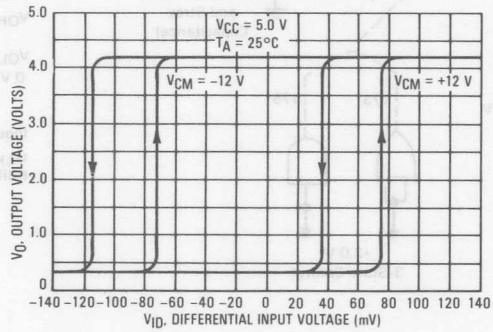
FIGURE 2 — PROPAGATION DELAY, THREE-STATE CONTROL INPUT TO OUTPUT



TYPICAL CHARACTERISTICS

(Both Device Types, Unless Otherwise Noted)

FIGURE 3 — OUTPUT VOLTAGE versus DIFFERENTIAL INPUT VOLTAGE



TYPICAL CHARACTERISTICS (continued)

FIGURE 4 — OUTPUT VOLTAGE versus 3-STATE CONTROL VOLTAGE

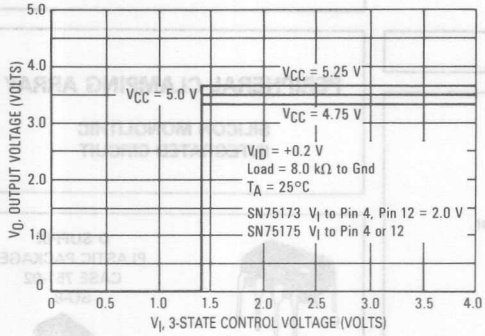


FIGURE 5 — OUTPUT VOLTAGE versus (INVERTED) 3-STATE CONTROL VOLTAGE — SN75173

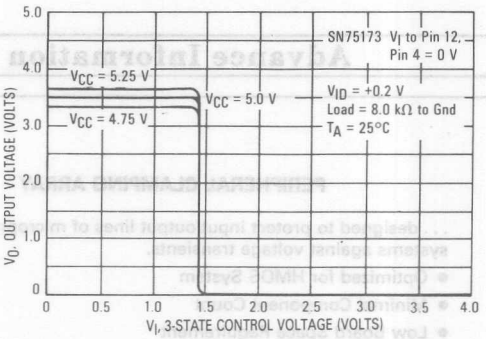


FIGURE 6 — HIGH LEVEL OUTPUT VOLTAGE versus OUTPUT CURRENT

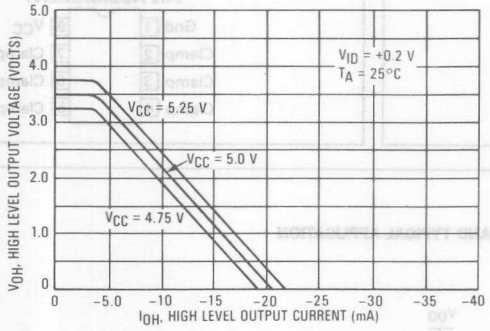


FIGURE 7 — LOW LEVEL OUTPUT VOLTAGE versus OUTPUT CURRENT

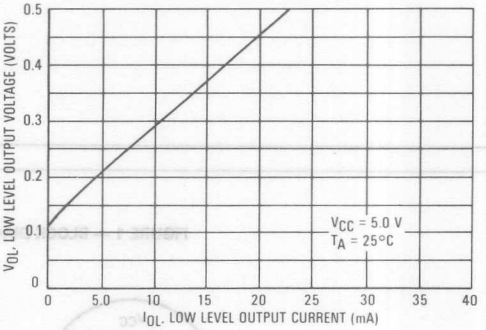


FIGURE 8 — HIGH LEVEL OUTPUT VOLTAGE versus TEMPERATURE

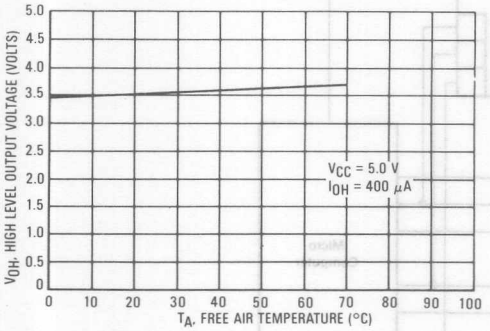
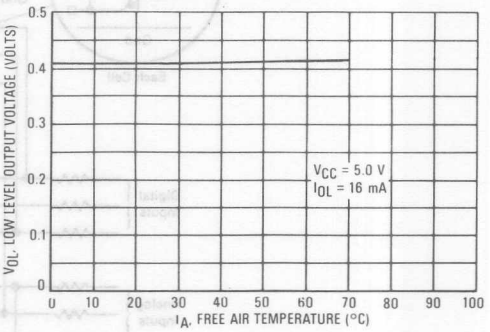


FIGURE 9 — LOW LEVEL OUTPUT VOLTAGE versus TEMPERATURE



7

Advance Information

PERIPHERAL CLAMPING ARRAY

SILICON MONOLITHIC INTEGRATED CIRCUIT

PERIPHERAL CLAMPING ARRAY

. . . designed to protect input/output lines of microprocessor systems against voltage transients.

- Optimized for HMOS System
- Minimal Component Count
- Low Board Space Requirement
- No P.C.B. Track Crossovers Required
- Applications Areas Include Automotive, Industrial, Telecommunications and Consumer Goods



PLASTIC PACKAGE
CASE 626-05

D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SO-8



PIN ASSIGNMENT

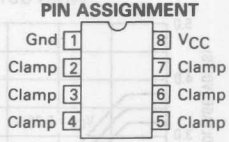
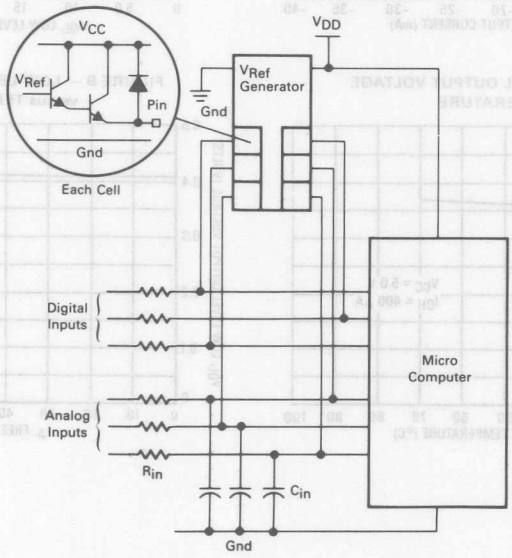


FIGURE 1 — BLOCK DIAGRAM AND TYPICAL APPLICATION



This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted, Note 1.)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	6.0	V
Supply Current	I_i	300	mA
Clamping Current	I_{IK}	±50	mA
Junction Temperature	T_J	125	°C
Power Dissipation (T_A = +85°C)	P_D	400	mW
Thermal Resistance (Junction-Ambient)	θ_{JA}	100	°C/W
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

Note 1: Values beyond which damage may occur.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, 4.5 ≤ V_{CC} ≤ 5.5 V; if not otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
Positive Clamping Voltage (Note 2) (I_{IK} = 10 mA, −40°C ≤ T_A ≤ +85°C)	$V_{(IK)}$	—	V_{CC} + 1.0	V
Positive Peak Clamping Current	$I_{IK(P)}$	—	20	mA
Negative Peak Clamping Voltage (I_{IK} = −10 mA, −40°C ≤ T_A ≤ +85°C)	$V_{(IK)}$	−0.3	—	V
Negative Peak Clamping Current	$I_{IK(P)}$	−20	—	mA
Output Leakage Current (0 V ≤ V_{in} ≤ V_{CC}) (0 V ≤ V_{in} ≤ V_{CC}, −40°C ≤ T_A ≤ +85°C)	 I_L I_{LT}	 — —	 1.0 5.0	μA
Channel Crosstalk (A_{CT} = 20 log I_L/I_{IK})	A_{CT}	100	—	dB
Quiescent Current (Package)	I_B	—	2.0	mA

Note 2: The device might not give 100% protection in CMOS applications.

7

CIRCUIT DESCRIPTION

To ensure the reliable operation of any integrated circuit based electronics system, care has to be taken that voltage transients do not reach the device I/O pins. Most NMOS, HMOS and Bipolar integrated circuits are particularly sensitive to negative voltage peaks which can provoke latch-up or otherwise disturb the normal functioning of the circuit, and in extreme cases may destroy the device.

Generally the maximum rating for a negative voltage transients on integral circuits is −0.3 V over the whole temperature range. Classical protection units have consisted of diode/resistor networks as shown in Figures 2a and 2b.

The arrangement in Figure 2a does not, in general, meet the specification and is therefore inadequate.

The problem with the solution shown in Figure 2b lies mainly with the high current drain through the biassing devices R_1 and D_3. A second problem exists if the input line carries an analog signal. When V_{in} is close to the ground potential, currents arising from leakage and mismatch between D_3 and D_2 can be sourced into the input line, thus disturbing the reading.

FIGURE 2 — CLASSICAL PROTECTION CIRCUITS

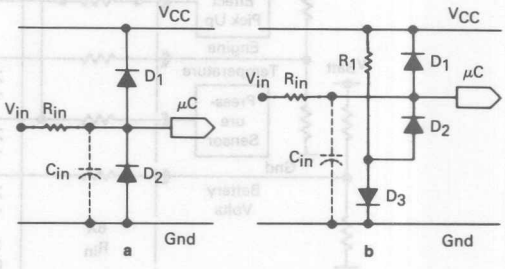
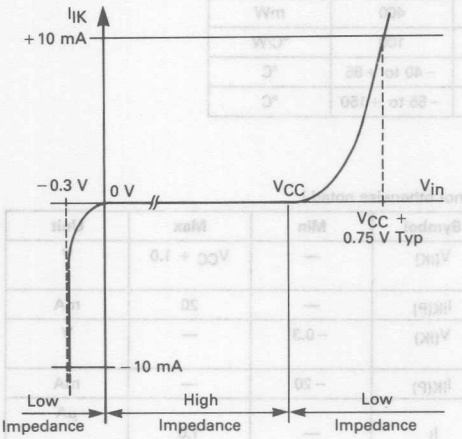


Figure 3 shows the clamping characteristics which are common to each of the six cells in the Peripheral Clamping Array.

As with the classical protection circuits, positive voltage transients are clamped by means of a fast diode to the V_{CC} supply line.

FIGURE 3 — CLAMPING CHARACTERISTICS



APPLICATIONS INFORMATION

Figure 4 depicts a typical application in a microcomputer based automotive ignition system.

The TCF6000 is being used not only to protect the system's normal inputs but also the (bidirectional) serial diagnostics port.

The value of the input resistors, R_{in}, is determined by the clamping current and the anticipated value of the spikes.

Thus:

$$R_{in} = \frac{V}{I_{IK}} \text{ Ohms}$$

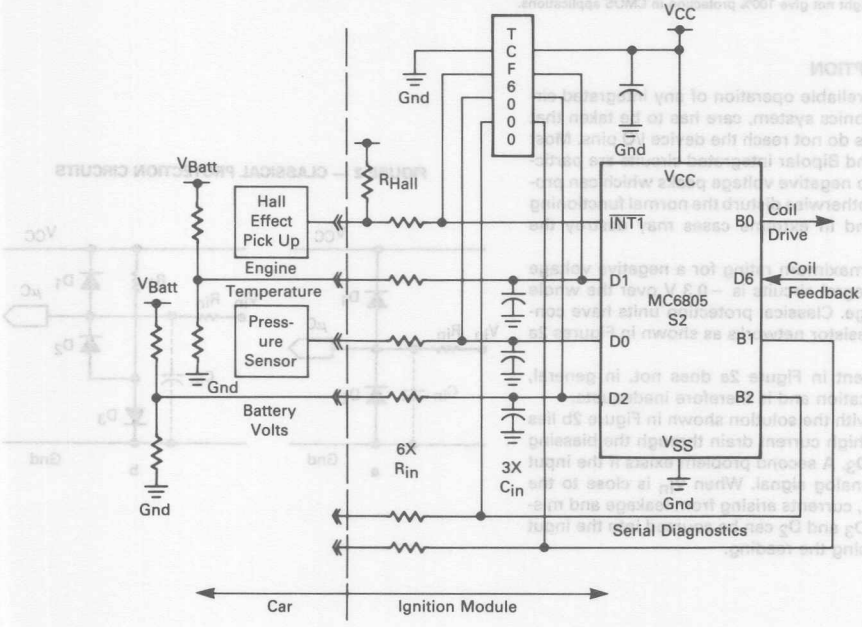
where V = Peak volts (Volts)
I_{IK} = Clamping current (Amps)

So, taking
V = 300 V typically (SAE J1211)
I_{IK} = 10 mA (recommended)

gives
R_{in} = 30 k

Resistors of this value will not usually cause any problems in MOS systems, but their presence needs to be taken into account by the designer. Their effect will normally need to be compensated for in Bipolar systems.

FIGURE 4 — TYPICAL AUTOMOTIVE APPLICATION



The use of C_{in} is not mandatory, and is not recommended where the lines to be protected are used for output or for both input and output. For digital input lines, the use of a small capacitor in the range of 50 to 220 pF is recommended as this will reduce the rate of rise of voltage seen by the TCF6000 and hence the possibility of overshoot.

In the case of the analog inputs, such as that from the pressure sensor, the capacitor C_{in} is necessary for devices, such as the MC6805S2 shown, which present a low impedance during the sampling period. The maximum value for C_{in} is determined by the accuracy required, the time taken to sample the input and the input impedance during that time, while the maximum value is determined by the required frequency response and the value of R_{in}.

Thus for a resistive input A/D connector where:

T_S = Sample time (Seconds)
R_D = Device input resistance (Ohms)
V_{in} = Input voltage (Volts)
k = Required accuracy (%)
Q_1 = Charge on capacitor before sampling
Q_2 = Charge on capacitor after sampling
I_D = Device input current (Amps)

Thus:

$$Q_1 - Q_2 = \frac{k.Q_1}{100}$$

but $Q_1 = C_{in}\, V_{in}$

and $Q_1 - Q_2 = I_D.T_S$

so that $I_D\, T_S = \frac{k.C_{in}.V_{in}}{100}$

and $C_{in}\,(min) = \frac{I_D.T_S}{V_{in}.k}$ Farad

so $C_{in}\,(min) = \frac{100.T_S}{k.R_D}$ Farad

The calculation for a sample and hold type converter is even simpler:

k = Required accuracy (%)
C_H = Hold capacitor (Farad)

$$C_{in}\,(min) = \frac{100.C_H}{k}\ \text{Farad}$$

For the MC6805S2 this comes out at:

$$C_{in}\,(min) = \frac{100.25\ pF}{0.25} = 10\ nF \text{ for } 1/4\% \text{ accuracy}$$

7

QUAD 1.5 A SINKING HIGH CURRENT SWITCH

The ULN2068B is a high-voltage, high-current quad Darlington switch array designed for high current loads, both resistive and reactive, up to 300 watts.

It is intended for interfacing between low level (TTL, DTL, LS and 5.0 V CMOS) logic families and peripheral loads such as relays, solenoids, dc and stepping motors, multiplexer LED and incandescent displays, heaters, or other high voltage, high current loads.

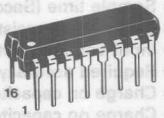
The Motorola ULN2068B is specified with minimum guaranteed breakdown of 50 V and is 100% tested for safe area using an inductive load. It includes integral transient suppression diodes. Use of a predriver stage reduces input current while still allowing the device to switch 1.5 Amps.

It is supplied in an improved 16-Pin plastic DIP package with heat sink contact tabs (Pins 4, 5 and 12, 13). A copper alloy lead frame allows maximum power dissipation using standard cooling techniques. The use of the contact tab lead frame facilitates attachment of a DIP heat sink while permitting the use of standard layout and mounting practices.

- TTL, DTL, LS, CMOS Compatible Inputs
- 1.5 Amp Maximum Output Current
- Low Input Current
- Internal Freewheeling Clamp Diodes
- 100% Inductive Load Tested
- Heat Tab Copper Alloy Lead Frame for Increased Dissipation

QUAD 1.5 A DARLINGTON SWITCH

SILICON MONOLITHIC INTEGRATED CIRCUIT



B SUFFIX
PLASTIC PACKAGE
CASE 648C-02

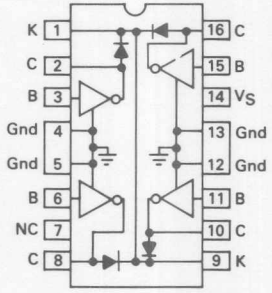
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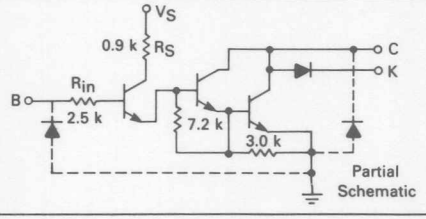
MAXIMUM RATINGS (T_A = 25°C and ratings apply to any one device in the package unless otherwise noted.)

Rating	Symbol	Value	Unit
Output Voltage	V_O	50	V
Input Voltage (Note 1)	V_I	15	V
Supply Voltage	V_S	10	V
Collector Current (Note 2)	I_C	1.75	A
Input Current (Note 3)	I_I	25	mA
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Junction Temperature	T_J	150	°C

Notes:
1. Input voltage referenced to ground.
2. Allowable output conditions shown in Figures 11 and 12.
3. May be limited by max input voltage.

PIN CONNECTIONS





ORDERING INFORMATION*

Device	Temperature Range	Package
ULN2068B	0°C to +70°C	Plastic DIP

* Other options of this ULN2060/2070 series are available for volume applications. Contact your local Motorola Sales Representative.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Fig.	Symbol	Min	Typ	Max	Unit
Output Leakage Current (V_{CE} = 50 V) (V_{CE} = 50 V, T_A = 70°C)	1	I_{CEX}	— —	— —	100 500	μA
Collector-Emitter Saturation Voltage (I_C = 500 mA (I_C = 750 mA (I_C = 1.0 A (I_C = 1.25 A } V_{in} = 2.4 V)	2	$V_{CE(sat)}$	— — — —	— — — —	1.13 1.25 1.40 1.60	V
Input Current — On Condition (V_I = 2.4 V) (V_I = 3.75 V)	4	$I_{I(on)}$	— —	— —	0.25 1.0	mA
Input Voltage — On Condition (V_{CE} = 2.0 V, I_C = 1.5 A)	5	$V_{I(on)}$	—	—	2.4	V
Inductive Load Test (V_S = 5.5 V, V_{CC} = 24.5 V, t_{PW} = 4.0 ms)	3	ΔV_{out}	—	—	100	mV
Supply Current (I_C = 500 mA, V_{in} = 2.4 V, V_S = 5.5 V)	8	I_S	—	—	6.0	mA
Turn-On Delay Time (50% E_I to 50% E_O)	—	t_{PHL}	—	—	1.0	μs
Turn-Off Delay Time (50% E_I to 50% E_O)	—	t_{PLH}	—	—	4.0	μs
Clamp Diode Leakage Current (V_R = 50 V) (V_R = 50 V, T_A = 70°C)	6	I_R	— —	— —	50 100	μA
Clamp Diode Forward Voltage (I_F = 1.0 A) (I_F = 1.5 A)	7	V_F	— —	— —	1.75 2.0	V

TEST FIGURES

FIGURE 1

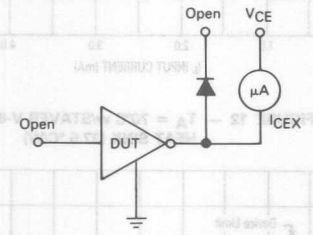


FIGURE 2

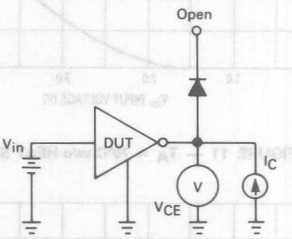


FIGURE 3

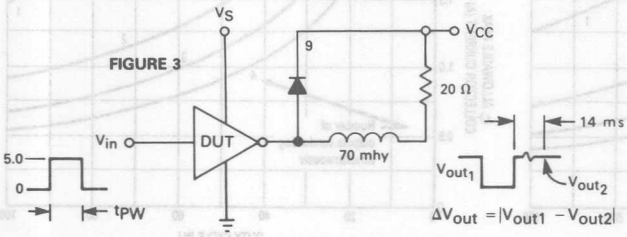
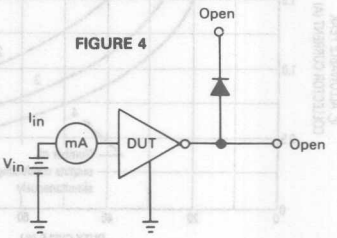


FIGURE 4



TEST FIGURES (CONTINUED)

FIGURE 5

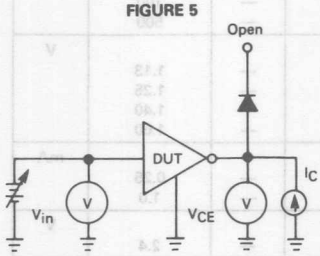


FIGURE 6

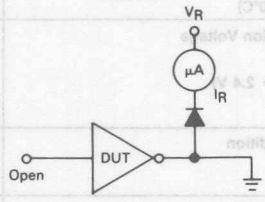


FIGURE 7

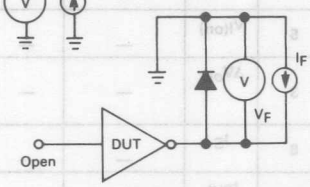
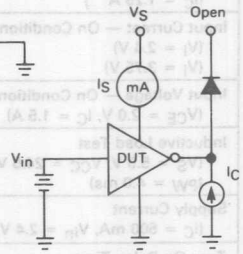


FIGURE 8



TYPICAL CHARACTERISTIC CURVES — T_A = 25°C

FIGURE 9 — INPUT CURRENT versus INPUT VOLTAGE

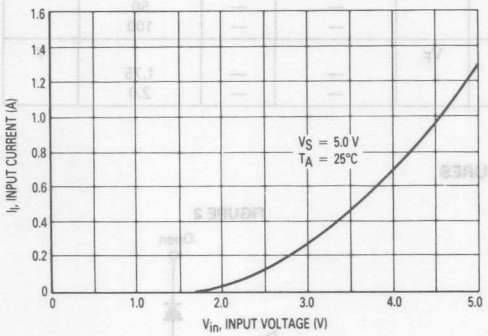


FIGURE 10 — COLLECTOR CURRENT versus INPUT CURRENT

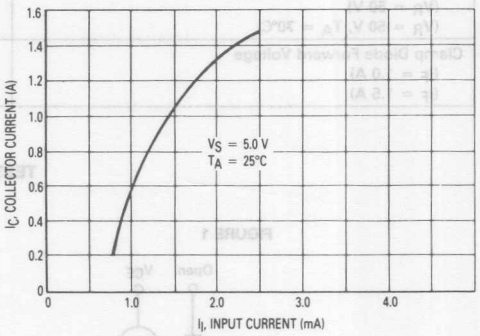


FIGURE 11 — T_A = 70°C w/o HEAT SINK

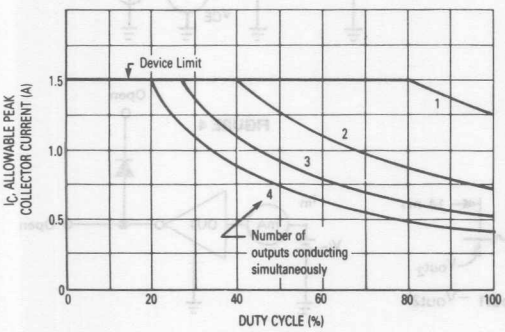


FIGURE 12 — T_A = 70°C w/STAVER V-8 HEAT SINK (37.5 °C/W)

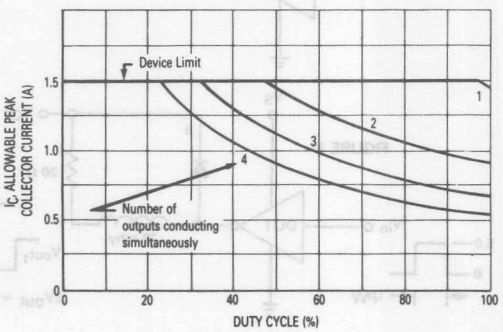


FIGURE 13 — T_A = 70°C w/STAVER V-7 HEAT SINK (27.5 °C/W)

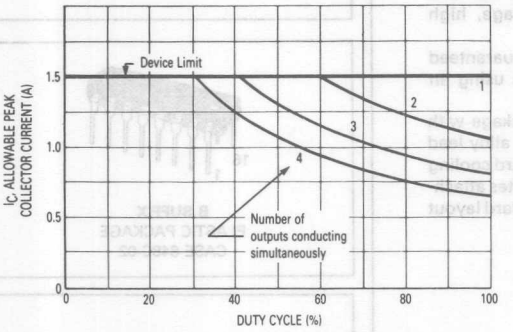


FIGURE 14 — T_A = 50°C w/o HEAT SINK

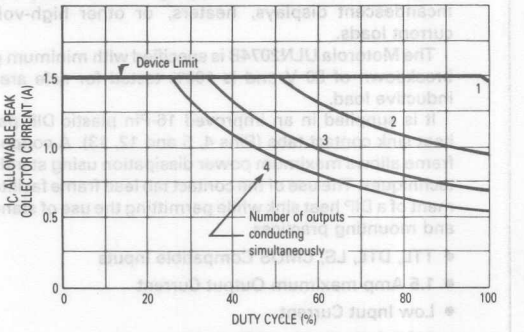


FIGURE 15 — T_A = 50°C w/STAVER V-8 HEAT SINK (37.5 °C/W)

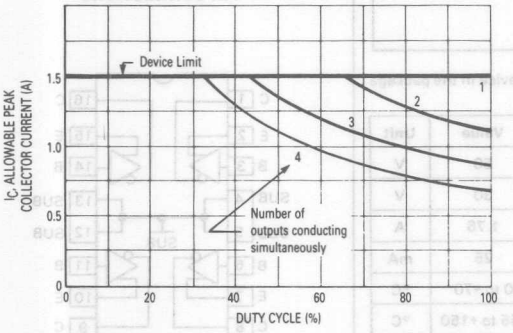
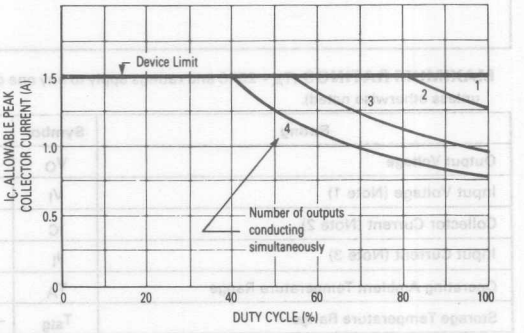


FIGURE 16 — T_A = 50°C w/ STAVER V-7 HEAT SINK (27.5 °C/W)



7

ULN2074B

QUAD 1.5 A SINKING HIGH CURRENT SWITCH

The ULN2074B is a high voltage, high current quad Darlington switch array designed for high current loads, both resistive and reactive, up to 300 watts.

It is intended for interfacing between low level (TTL, DTL, LS and 5.0 V CMOS) logic families and peripheral loads such as relays, solenoids, dc and stepping motors, multiplexer LED and incandescent displays, heaters, or other high-voltage, high current loads.

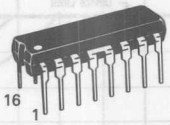
The Motorola ULN2074B is specified with minimum guaranteed breakdown of 50 V and is 100% tested for safe area using an inductive load.

It is supplied in an improved 16-Pin plastic DIP package with heat sink contact tabs (Pins 4, 5 and 12, 13). A copper alloy lead frame allows maximum power dissipation using standard cooling techniques. The use of the contact tab lead frame facilitates attachment of a DIP heat sink while permitting the use of standard layout and mounting practices.

- TTL, DTL, LS, CMOS Compatible Inputs
- 1.5 Amp maximum Output Current
- Low Input Current
- 100% Inductive Load Tested
- Heat Tab Copper Alloy Lead Frame for Increased Dissipation

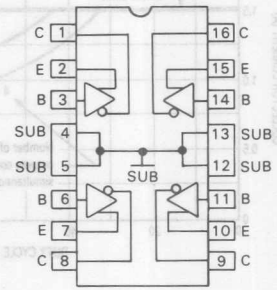
QUAD 1.5 A DARLINGTON SWITCH

SILICON MONOLITHIC INTEGRATED CIRCUIT



B SUFFIX
PLASTIC PACKAGE
CASE 648C-02

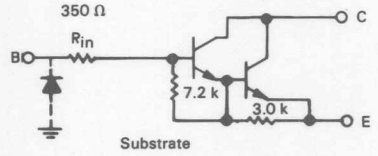
PIN CONNECTIONS



MAXIMUM RATINGS (T_A = 25°C and ratings apply to any one device in the package unless otherwise noted).

Rating	Symbol	Value	Unit
Output Voltage	V_O	50	V
Input Voltage (Note 1)	V_I	30	V
Collector Current (Note 2)	I_C	1.75	A
Input Current (Note 3)	I_I	25	mA
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Junction Temperature	T_J	150	°C

Notes:
1. Input voltage referenced to ground (substrate).
2. Allowable output conditions shown in Figures 8 and 9.
3. May be limited by max input voltage.



Partial Schematic

ORDERING INFORMATION*

Device	Temperature Range	Package
ULN2074B	0°C to +70°C	Plastic DIP

* Other options of this ULN2060/2070 series are available for volume applications. Contact your local Motorola Sales Representative.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Fig.	Symbol	Min	Typ	Max	Unit
Output Leakage Current (V_{CE} = 50 V) (V_{CE} = 50 V, T_A = 70°C)	1	I_{CEX}	 — —	 — —	 100 500	μA
Collector-Emitter Saturation Voltage (I_C = 500 mA, I_I = 625 μA) (I_C = 750 mA, I_I = 935 μA) (I_C = 1.0 A, I_I = 1.25 mA) (I_C = 1.25 A, I_I = 2.0 mA)	2	$V_{CE(sat)}$	 — — — —	 — — — —	 1.13 1.25 1.40 1.60	V
Input Current — On Condition (V_I = 2.4 V) (V_I = 3.75 V)	4	$I_{I(on)}$	 2.0 4.5	 — —	 4.3 9.6	mA
Input Voltage — On Condition (V_{CE} = 2.0 V, I_C = 1.0 A) (V_{CE} = 2.0 V, I_C = 1.5 A)	5	$V_{I(on)}$	 — —	 — —	 2.0 2.5	V
Inductive Load Test (V_{CC} = 24.5 V, t_{PW} = 4.0 μs)	3	ΔV_{out}	—	—	100	mV
Turn-On Delay Time (50% E_I to 50% E_O)	—	t_{PHL}	—	—	1.0	μs
Turn-Off Delay Time (50% E_I to 50% E_O)	—	t_{PLH}	—	—	1.5	μs

7

TEST FIGURES

FIGURE 1

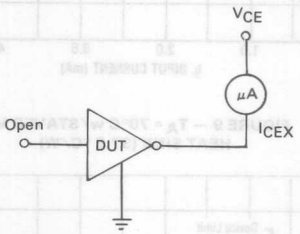


FIGURE 2

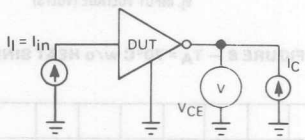


FIGURE 3

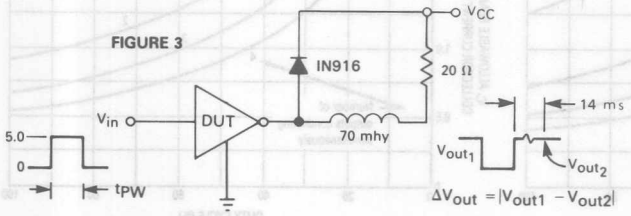


FIGURE 4

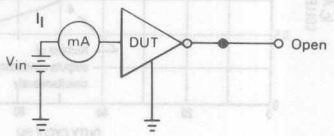
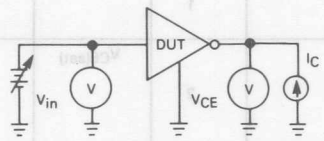


FIGURE 5



TYPICAL CHARACTERISTIC CURVES

FIGURE 6 — INPUT CURRENT versus INPUT VOLTAGE

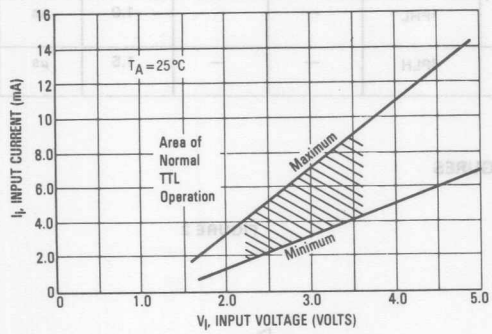


FIGURE 7 — COLLECTOR CURRENT versus INPUT CURRENT

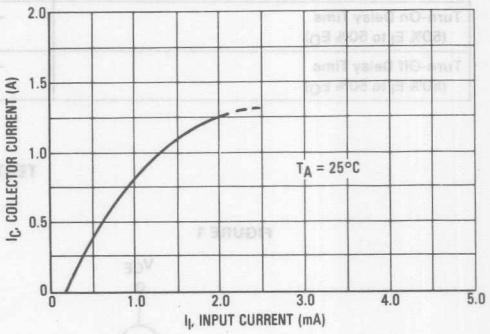


FIGURE 8 — T_A = 70°C w/o HEAT SINK

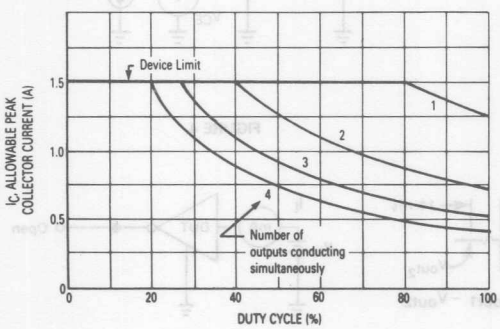


FIGURE 9 — T_A = 70°C w/STAVER V-8 HEAT SINK (37.5 °C/W)

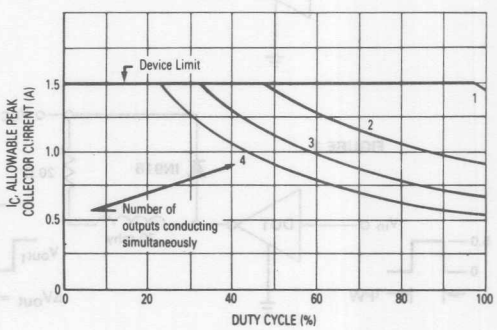


FIGURE 10 — T_A = 70°C w/STAVER V-7 HEAT SINK (27.5 °C/W)

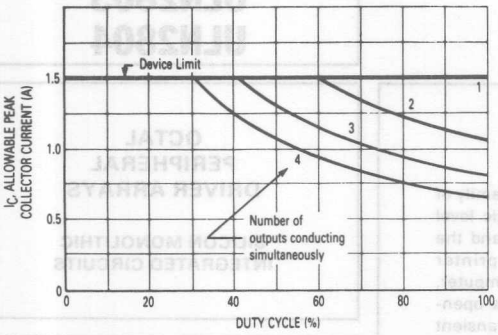


FIGURE 11 — T_A = 50°C w/o HEAT SINK

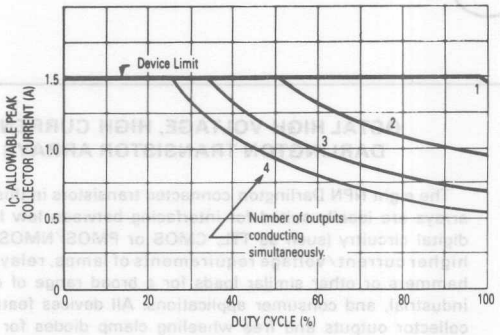


FIGURE 12 — T_A = 50°C w/STAVER V-8 HEAT SINK (37.5 °C/W)

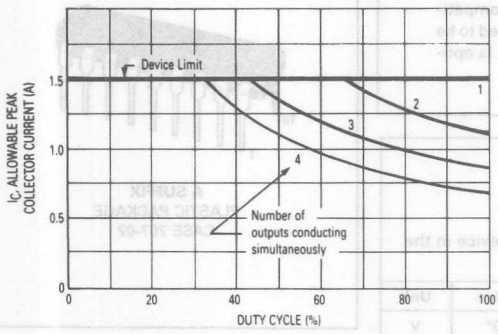
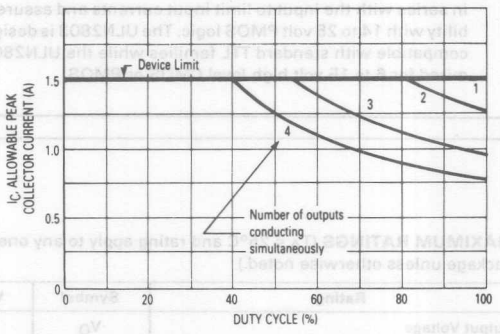


FIGURE 13 — T_A = 50°C w/STAVER V-7 HEAT SINK (27.5 °C/W)



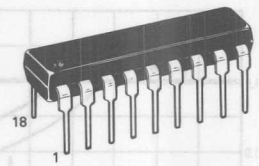
OCTAL HIGH VOLTAGE, HIGH CURRENT DARLINGTON TRANSISTOR ARRAYS

The eight NPN Darlington connected transistors in this family of arrays are ideally suited for interfacing between low logic level digital circuitry (such as TTL, CMOS or PMOS/NMOS) and the higher current/voltage requirements of lamps, relays, printer hammers or other similar loads for a broad range of computer, industrial, and consumer applications. All devices feature open-collector outputs and free wheeling clamp diodes for transient suppression.

The ULN2801 is a general purpose device for use with CMOS, PMOS or TTL logic. The ULN2802 contains a zener diode and resistor in series with the input to limit input currents and assure compatibility with 14 to 25 volt PMOS logic. The ULN2803 is designed to be compatible with standard TTL families while the ULN2804 is optimized for 6 to 15 volt high level CMOS or PMOS.

OCTAL PERIPHERAL DRIVER ARRAYS

SILICON MONOLITHIC INTEGRATED CIRCUITS



A SUFFIX
PLASTIC PACKAGE
CASE 707-02

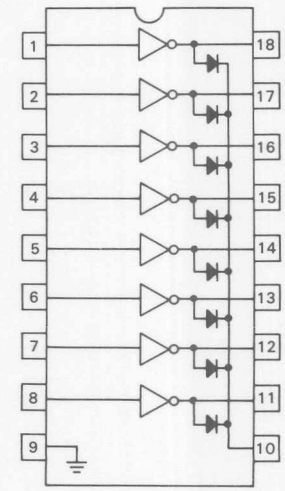
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MAXIMUM RATINGS (T_A = 25°C and rating apply to any one device in the package unless otherwise noted.)

Rating	Symbol	Value	Unit
Output Voltage	V_O	50*	V
Input Voltage (Except ULN2801)	V_I	30	V
Collector Current — Continuous	I_C	500	mA
Base Current — Continuous	I_B	25	mA
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Junction Temperature	T_J	125	°C

$R_{\theta JA}$ = 55°C/W
Do not exceed maximum current limit per driver.
*Higher voltage selection available. See your local representative.

PIN CONNECTIONS



ORDERING INFORMATION

DEVICE	CHARACTERISTICS		
	INPUT COMPATIBILITY	V_{CE}(MAX)/I_C(MAX)	T_A
ULN2801A	General Purpose CMOS, PMOS	50 V/500 mA	0 to +70°C
ULN2802A	14–25 Volt PMOS	50 V/500 mA	0 to +70°C
ULN2803A	TTL, 5.0 V CMOS	50 V/500 mA	0 to +70°C
ULN2804A	6–15 V CMOS, PMOS	50 V/500 mA	0 to +70°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Fig.	Symbol	Min	Typ	Max	Unit
Output Leakage Current		1	I_{CEX}				μA
(*V_O = 50 V, T_A = +70°C)	All Types			—	—	100	
(*V_O = 50 V, T_A = +25°C)	All Types			—	—	50	
(*V_O = 50 V, T_A = +70°C, V_I = 6.0 V)	ULN2802			—	—	500	
(*V_O = 50 V, T_A = +70°C, V_I = 1.0 V)	ULN2804			—	—	500	
Collector-Emitter Saturation Voltage		2	$V_{CE(sat)}$				V
(I_C = 350 mA, I_B = 500 μA)	All Types			—	1.1	1.6	
(I_C = 200 mA, I_B = 350 μA)	All Types			—	0.95	1.3	
(I_C = 100 mA, I_B = 250 μA)	All Types			—	0.85	1.1	
Input Current — On Condition		4	$I_{I(on)}$				mA
(V_I = 17 V)	ULN2802			—	0.82	1.25	
(V_I = 3.85 V)	ULN2803			—	0.93	1.35	
(V_I = 5.0 V)	ULN2804			—	0.35	0.5	
(V_I = 12 V)	ULN2804			—	1.0	1.45	
Input Voltage — On Condition		5	$V_{I(on)}$				V
(V_{CE} = 2.0 V, I_C = 300 mA)	ULN2802			—	—	13	
(V_{CE} = 2.0 V, I_C = 200 mA)	ULN2803			—	—	2.4	
(V_{CE} = 2.0 V, I_C = 250 mA)	ULN2803			—	—	2.7	
(V_{CE} = 2.0 V, I_C = 300 mA)	ULN2803			—	—	3.0	
(V_{CE} = 2.0 V, I_C = 125 mA)	ULN2804			—	—	5.0	
(V_{CE} = 2.0 V, I_C = 200 mA)	ULN2804			—	—	6.0	
(V_{CE} = 2.0 V, I_C = 275 mA)	ULN2804			—	—	7.0	
(V_{CE} = 2.0 V, I_C = 350 mA)	ULN2804			—	—	8.0	
Input Current — Off Condition (I_C = 500 μA, T_A = +70°C)	All Types	3	$I_{I(off)}$	50	100	—	μA
DC Current Gain (V_{CE} = 2.0 V, I_C = 350 mA)	ULN2801	2	h_{FE}	1000	—	—	—
Input Capacitance			C_I	—	15	25	pF
Turn-On Delay Time (50% E_I to 50% E_O)			t_{on}	—	0.25	1.0	μs
Turn-Off Delay Time (50% E_I to 50% E_O)			t_{off}	—	0.25	1.0	μs
Clamp Diode Leakage Current (V_R = 50 V)	T_A = +25°C T_A = +70°C	6	I_R	—	—	50 100	μA
Clamp Diode Forward Voltage (I_F = 350 mA)		7	V_F	—	1.5	2.0	V

*Higher voltage selections available, contact your local representative.

7

TEST FIGURES

(SEE FIGURE NUMBERS IN ELECTRICAL CHARACTERISTICS TABLES)

FIGURE 1

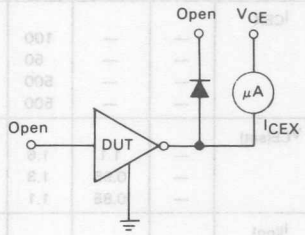


FIGURE 2

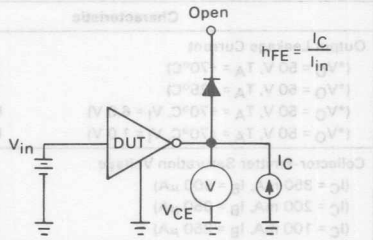


FIGURE 3

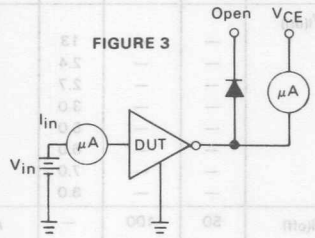


FIGURE 4

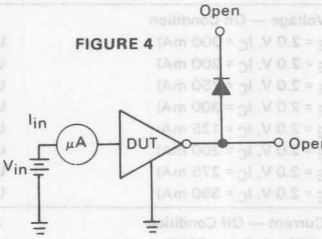


FIGURE 5

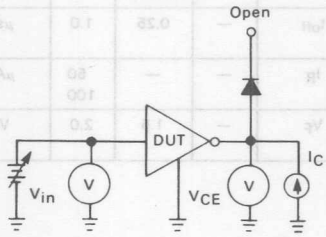


FIGURE 6

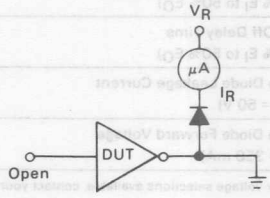
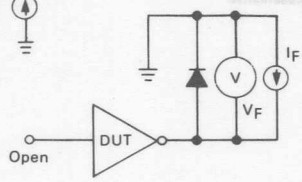


FIGURE 7



TYPICAL CHARACTERISTIC CURVES — T_A = 25°C
(unless otherwise noted)

OUTPUT CHARACTERISTICS

FIGURE 8 — OUTPUT CURRENT versus SATURATION VOLTAGE

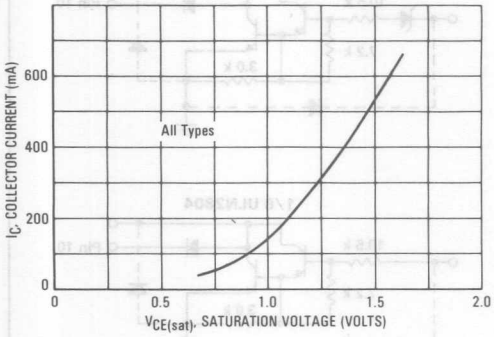
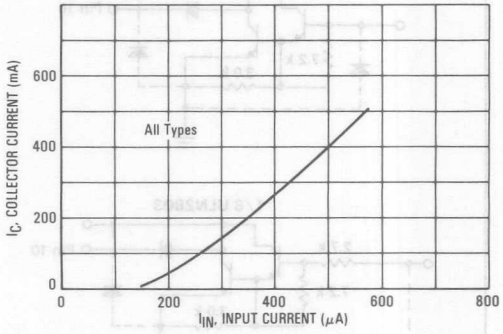


FIGURE 9 — OUTPUT CURRENT versus INPUT CURRENT



INPUT CHARACTERISTICS

FIGURE 10 — ULN2802 INPUT CURRENT versus INPUT VOLTAGE

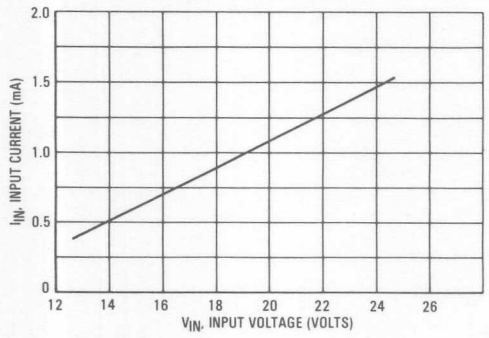


FIGURE 11 — ULN2803 INPUT CURRENT versus INPUT VOLTAGE

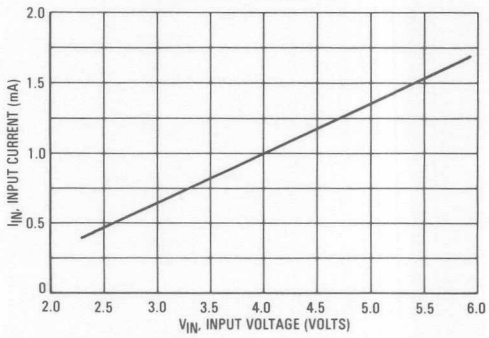
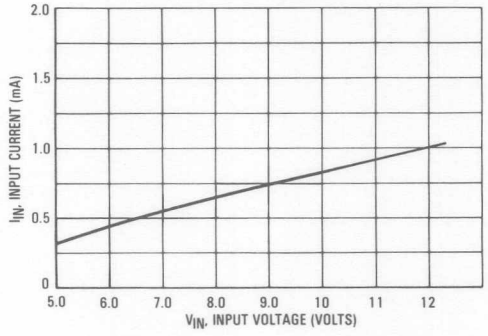
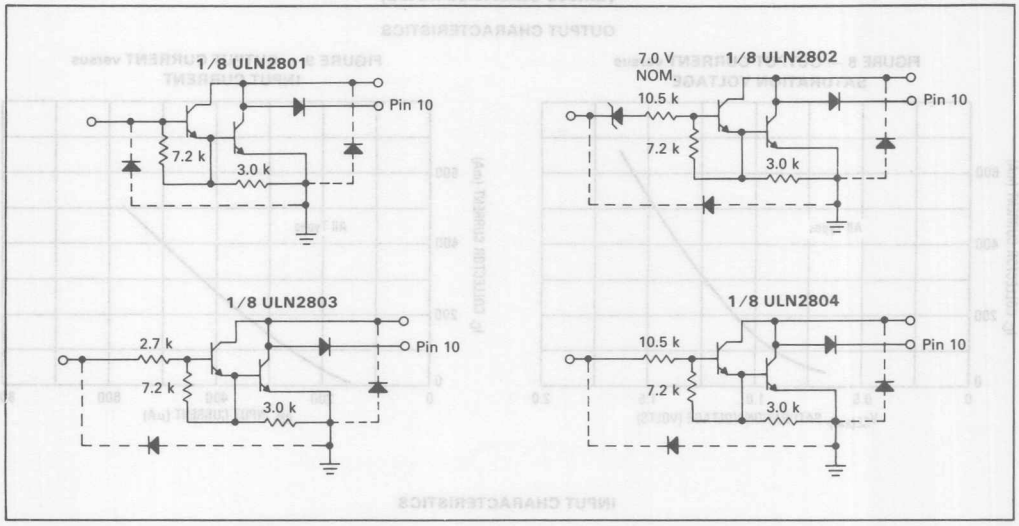


FIGURE 12 — ULN2804 INPUT CURRENT versus INPUT VOLTAGE

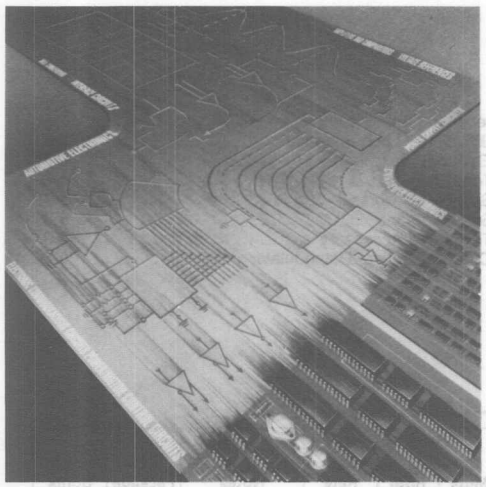


7

REPRESENTATIVE CIRCUIT SCHEMATICS



7



In Brief . . .

RF

Radio communication has greatly expanded its scope in the past several years. Once dominated by public safety radio, the 30 to 1000 MHz spectrum is now packed with personal and low cost business radio systems. The vast majority of this equipment uses FM or FSK modulation and is targeted at short range applications. From mobile phones and VHF marine radios to garage door openers and radio controlled toys, these new systems have become a part of our lifestyle. Motorola linear products has focused on this technology adding a wide array of new products including complete receivers processed in our exclusive 3 GHz MOSAIC 1.5 process. New surface mount packages, for high density assembly, are available for all of these products, as is a growing family of supporting applications notes and development kits.

Telephone & Voice/Data

Traditionally, an office environment has utilized two distinctly separate wired communications systems — Telecommunications and Datacommunications. Each had its individual hardware components complement and each required its own independent transmission line system: twisted wire pairs for Telecom and relatively high priced coax cable for Datacom. But times have changed. Today, Telecom and Datacom coexist comfortably on inexpensive twisted wire pairs and utilize a significant number of components in common. This has led to the development and enhancement of PBX (Private Branch Exchanges) to the point where the long heralded "office of the future," with simultaneous voice and data communications capability at each station, is no longer of the future at all. The capability is here today!

Motorola semiconductor components serve a wide range of requirements for the voice/data marketplace. They encompass both CMOS and linear technologies, each to its best advantage, and upgrade the conventional analog voice systems and establish new capabilities in digital communications. Early products, such as the solid-state single-chip crosspoint switch, the more recent monolithic Subscriber-Loop-Interface Circuit (SLIC), a single-chip Codec/Filter (Monocircuit) the latest Universal Digital Loop Transceivers (UDLT), and single-chip telephone circuits are just a few examples of Motorola leadership in the voice/data area.

Selector Guide
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Communication Circuits

8

Communication Circuits

RF Communications
- Narrowband Dual Conversion Receivers 8-2
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- Narrowband IFs 8-2
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Telecommunications
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RF Communications

Narrowband Dual Conversion Receivers — FM/FSK — VHF

Type	V_{CC}	I_{CC}	Sensitivity	RF Input (Max)	IF1 (Max)	IF2 (limiter in)	Mute	RSSI	Max Data Rate	Notes	Package	Case Suffix
MC3362	2–7 V	3 mA	<1 μV	180 MHz	10.7 MHz	455 kHz	—	√	1.2 kb	Includes buffered VCO output	24 Pin DIP, SOIC	P/724 DW/751E
MC3363	2–7 V	4 mA	<1 μV	180 MHz	10.7 MHz	455 kHz	√	√	1.2 kb	Includes RF amp, mute	28 Pin SOIC	DW/751F

AM Receiver Medium/Short Wave

MC13041	6.5–16.5 V	25 mA	6 μV	10 MHz	455 kHz	—	—	√	—	Includes scan stop	20 Pin DIP	P/738 DW/751D

Wideband Data (FM/FSK) Receiver — VHF

Type	V_{CC}	I_{CC}	Sensitivity	IF1 (Max)	IF2 (limiter in)	Mute	RSSI	Max Data Rate	Notes	Package	Case Suffix
MC3356	3–9 V	25 mA	30 μV	200 MHz	10.7 MHz	√	√	500 kb	Includes front end mixer/L.O.	20 Pin DIP/PLCC	P/738 FN/775

Narrowband IF's — Wideband (FM/FSK) IF

MC3357	4–8 V	5 mA	5 μV	45 MHz	455 kHz	√	—	—		16 Pin DIP/SOIC	P/648 D/751B
MC3359	4–9 V	7 mA	2 μV	45 MHz	455 kHz	√	—	—		18 Pin DIP/SOIC	P/707 DW/751C
MC3361	2–8 V	6 mA	2 μV	60 MHz	455 kHz	√	—	—		16 Pin DIP/SOIC	P/648 D/751B
MC3367	1–5 V	1 mA	<1 μV	75 MHz	455 kHz	√	—	1.2 kb	1 Cell Operation	28 Pin SOIC	DW/751F
MC3371	2–8 V	6 mA	2 μV	60 MHz	455 kHz	√	√	—	(3Q88 Intro)	16 Pin DIP/SOIC	P/648 D/751B
MC13055	3–12 V	25 mA	20 μV	—	40 MHz	√	√	2 Mb	Wideband Data IF	16 Pin DIP/SOIC	P/648 D/751B

Transmitters — FM/FSK

Type	V_{CC}	I_{CC}	P_{out}	Max RF Freq. Out	Battery Check	Tone OSC	Max Mod. Freq.	Notes	Package	Case Suffix
MC2831A	3–8 Vdc	5 mA	−30 dBm	50 MHz	√	√	5.0 kHz (xtal ctl)	Includes low battery checker, tone osc.	16 Pin DIP/SOIC	P/648 D/751B
MC2833	3–8 Vdc	3 mA	−30 dBm to +10 dBm	150 MHz	—	—	5.0 kHz (xtal ctl)	Includes two frequency multiplier/amplifier transistors	16 Pin DIP/SOIC	P/648 D/751B

Balanced Modulator/Demodulator

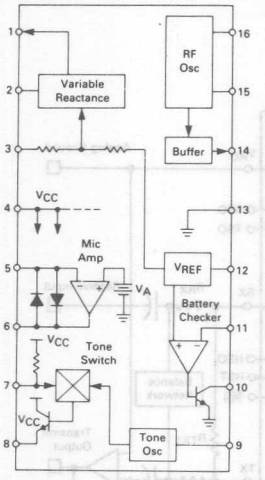
Type	V_{CC}	I_{CC}	Function	Package	Case Suffix
MC1596	5–30 V	10 mA	Carrier Balance >50 dB General purpose balanced modulator/ demodulator for AM, SSB, FM Detection	10 Pin Metal	G/603
MC1496	5–30 V	10 mA		14 Pin Ceramic DIL, DIP, SOIC	L/632 P/646 D/751A

Low Power FM Transmitter System

MC2831A — T_A = −30° to +75°C, Case 648, 751B

- Complete VHF FM Transmitter/Exciter
- Mike Preamp with Limiting
- Tone Generator for CTSS or AFSK
- Crystal or L-C VCO Operation
- Buffer/Multiplier Output Stage
- Low Voltage (internal reference) Warning Circuit
- Easily Partitioned for Semicustom Applications

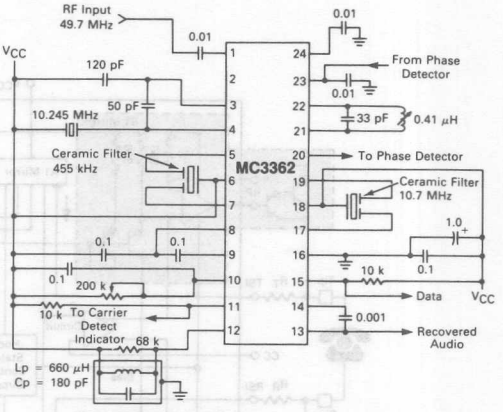
MC2831A



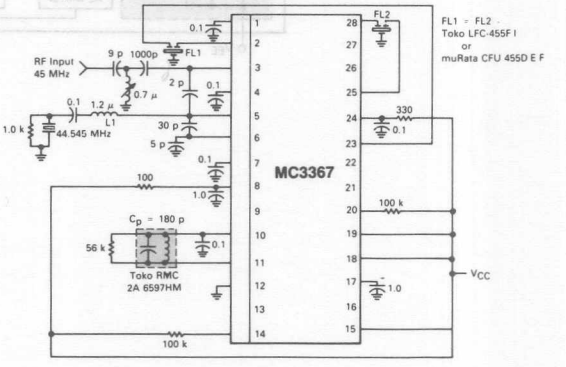
MOSAIC® 1.5 VHF Narrowband Dual-Conversion Receivers

MC3362/MC3363 — T_A = −40°C to +85°C, Case 724, 751A

- Operation to 180 MHz
- 2–8 V dc Supply
- >1 μV for 20 dB Quieting Sensitivity
- Analog and Data Modulation Recovery
- >60 dB Dynamic Range RSSI
- Crystal or VCO First L.O. Operation
- On-Chip RF Amp/MC3363



(All capacitors in μF unless otherwise stated. Resistors in ohms. Inductors in Henries.)



Low Voltage FM Narrowband Receiver

MC3367 — T_A = 0°C to +70°C, Case 751F

- Single Cell Operation to 0.9 V_{CC}
- Single Conversion Operation to 75 MHz
- Current Drain of 1 mA
- Split I.F. Amplifier for Single or Dual Filters
- Analog and Data Outputs
- Sensitivity of 0.7 μV Typ for 20 dB Quieting
- Low Battery Voltage Indicator

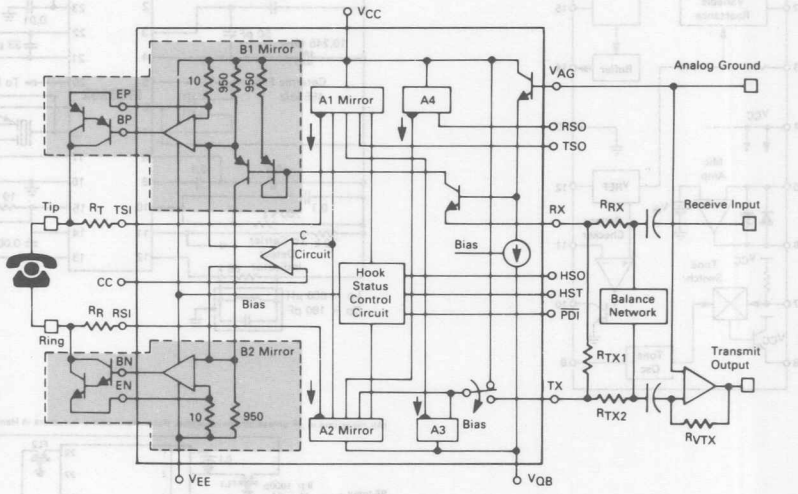
8

Subscriber Loop Interface Circuit (SLIC)

MC3419-1L — Case 726

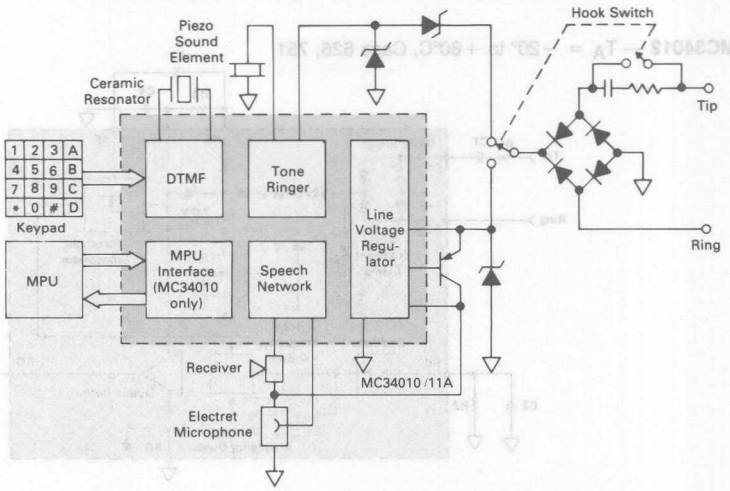
The replacement of two-to-four wire conversion hybrid transformers in Central Office, PBX, and Subscriber Carrier equipment with the SLIC has resulted in major improvement in telephony equipment. The SLIC family performs this task, along with all the other BORSHT functions required by signal transmission. These include the provision of dc power to the telephone (*B*attery); *O*vervoltage protection; *R*ing trip detection; *S*upervisory features such as hook status and dial pulsing; 2-to-4 wire conversion, suppression of longitudinal signals (*H*ybrid); and *T*esting.

- All Key Parameters Externally Programmable
- Current Sensing Outputs Monitor Status of Both Tip and Ring Leads
- On-Hook Power Below 5.0 mW
- Digital Hook Status Output
- Power Down Input
- Ground Fault Protection
- Size and Weight Reduction Over Conventional Approaches
- The sale of this product is licensed under patent No. 4,004,109. All royalties related to this patent are included in the unit price.



The Complete Electronic Telephone Circuit

MC34010/11A — T_A = −20° to +60°C, Case 711, 777



The conventional transformer-driven telephone handset is undergoing major innovations. The bulky transformer is disappearing. So are many of its discrete components, including the familiar telephone bell. They are being replaced with integrated circuits that perform all the major handset functions simply, reliably and inexpensively . . . functions such as 2-to-4 wire conversion, DTMF dialing, tone ringing, and a variety of related activities.

The culmination of these capabilities is the Electronic Telephone Circuit, the MC34010/11A. These IC's place all of the above mentioned functions on a single monolithic chip.

These telephone circuits utilize advanced bipolar linear (I^2L) technology and provide all the necessary elements of a modern tone-dialing telephone. The MC34010 even incorporates an MPU interface circuit for the inclusion of automatic dialing in the final system.

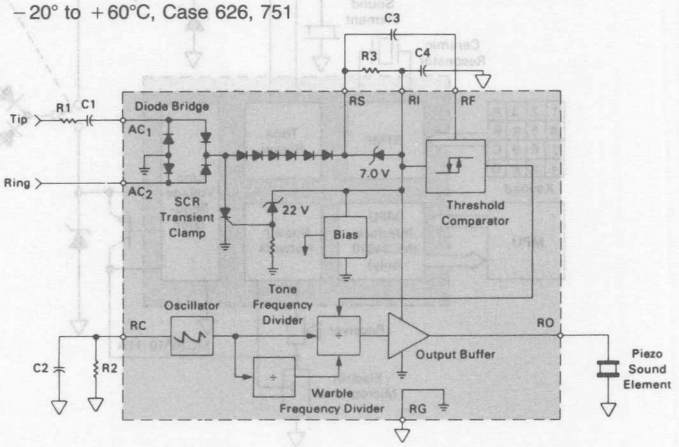
Features

- Provides All Basic Telephone Functions, Including DTMF Dialer, Tone Ringer, Speech Network and Line Voltage Regulator
- DTMF Generator Uses Low-Cost Ceramic Resonator with Accurate Frequency Synthesis Technique
- Tone Ringer Drives Piezoelectric Transducer and Satisfies EIA-470 Requirements
- Speech Network Provides Two–Four Wire Conversion with Adjustable Sidetone Utilizing an Electret Transmitter
- On-Chip Regulator Insures Stable Operation Over Wide Range of Loop Lengths
- I^2L Technology Provides Low 1.4 Volt Operation and High Static Discharge Immunity
- MC34010P Provides Microprocessor Interface Port for Automatic Dialing Features

Tone Ringers

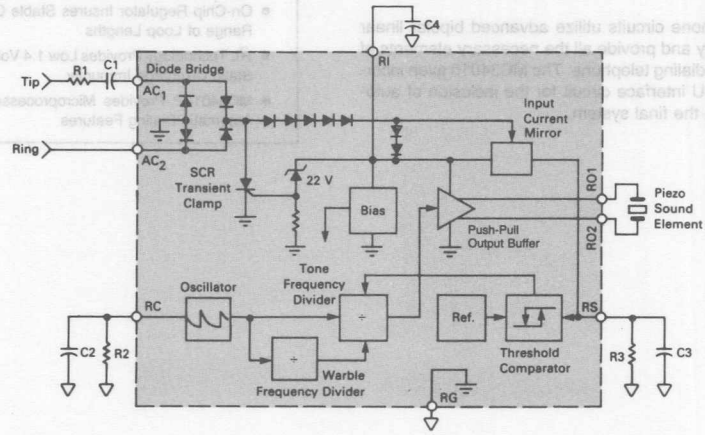
The MC34012 and MC34017 Tone Ringers are designed to replace the bulky bell assembly of a telephone, while providing the same function and performance under a variety of conditions. The operational requirements spelled out by the FCC and the EIA, simply stated, are that a ringer circuit MUST function when a ringing signal is provided, and MUST NOT ring when other signals (speech, dialing signals, noise) are on the line. The MC34012 series and the MC34017 series were designed to meet those requirements.

MC34012 — T_A = −20° to +60°C, Case 626, 751



- Complete Telephone Bell Replacement Circuit with Minimum External Components
- On-Chip Diode Bridge and Transient Protection
- Direct Drive for Piezoelectric Transducers
- Base Frequency Options — MC34012-1: 1.0 kHz
  MC34012-2: 2.0 kHz
  MC34012-3: 500 Hz
- Push-Pull Output Stage for Greater Output Power Capability (MC34017)
- Base Frequency Options — MC34017-1: 1.0 kHz
  MC34017-2: 2.0 kHz
  MC34017-3: 500 Hz
- Input Impedance Signature Meets Bell and EIA Standards
- Rejects Rotary Dial Transients

MC34017 — T_A = −20° to +60°C, Case 626, 751



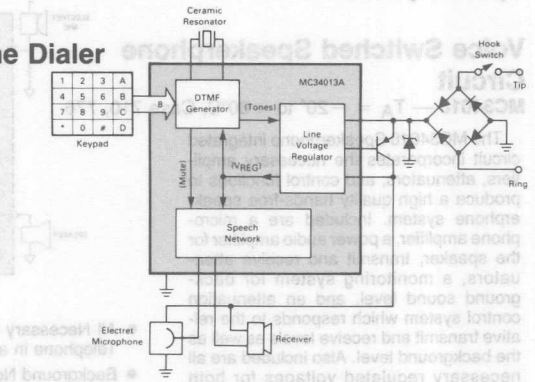
8

Speech Networks

Telephone Speech Network and Tone Dialer

MC34013A — T_A = −20° to +60°C, Case 710,776

- Linear/I^2L Technology Provides Low 1.4 Volt Operation in Both Speech and Dialing Modes
- Speech Network Provides 2–4 Wire Conversion with Adjustable Sidetone Utilizing an Electret Microphone
- DTMF Generator Uses Low-Cost Ceramic Resonator with Accurate Frequency Synthesis Technique
- On-Chip Regulator Insures Stable Operation Over Wide Range of Loop Lengths
- Dialer Mutes Speech Network with Internal Delay for Click Suppression on DTMF Key Release

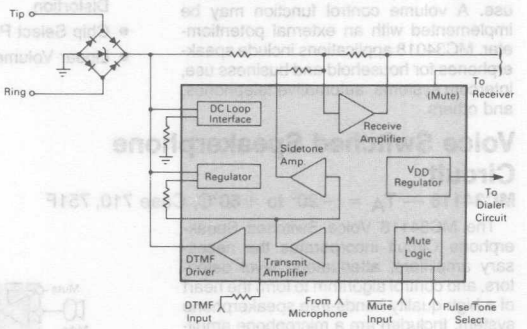


Speech Network with Dialer Interface

MC34014 — T_A = −20° to +60°C, Case 707, 775

The MC34014 is a Telephone Speech Network integrated circuit which incorporates adjustable transmit, receive, and sidetone functions, line interface circuit, dialer interface, and a regulated output voltage for a dialer circuit. It includes an equalization circuit to compensate for various line lengths and the conversion from 2-to-4 wire is accomplished with supply voltages as low as 1.5 volts.

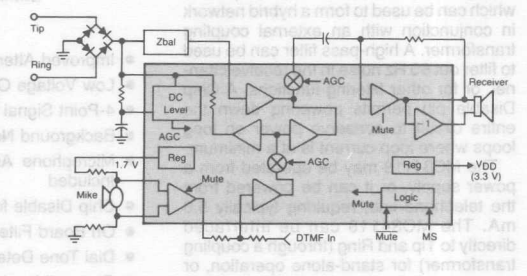
- Transmit, Receive, and Sidetone Gains Set By External Resistors
- Loop Length Equalization for Transmit, Receive, and Sidetone Functions
- Operates Down to 1.5 Volts (V+) in Speech Mode
- Provides Regulated Voltage for CMOS Dialer
- Speech Amplifiers Muted During Pulse and Tone Dialing
- DTMF Output Level Adjustable with a Single Resistor
- Compatible with 2-Terminal Electret Microphones
- Compatible with Receiver Impedances of 150 Ω and Higher



Telephone Speech Network with Dialer Interface

MC34114 — T_A = −20° to +70°C, Case 707, 751D

- Operation Down to 1.2 Volts
- Externally Adjustable Transmit, Receive, and Sidetone Gains
- Differential Microphone Amplifier Input Minimizes RFI
- Transmit, Receive, and Sidetone Equalization on both Voice and DTMF Signals
- Regulated 1.7 Volts Output for Biasing Microphone
- Regulated 3.3 Volts Output for Powering External Dialer
- Microphone and Receive Amplifiers Muted During Dialing
- Differential Receive Amplifier Output Eliminates Coupling Capacitor
- Operates with Receiver Impedances of 150 Ω and Higher
- MC34114 Complies with Bell Telephone and BT Standards

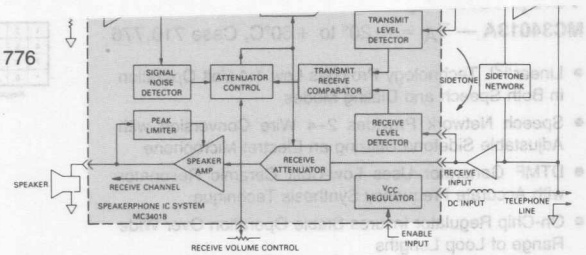


8

Circuit

MC34018 — T_A = −20° to +60°C, Case 710, 776

The MC34018 Speakerphone integrated circuit incorporates the necessary amplifiers, attenuators, and control functions to produce a high quality hands-free speakerphone system. Included are a microphone amplifier, a power audio amplifier for the speaker, transmit and receive attenuators, a monitoring system for background sound level, and an attenuation control system which responds to the relative transmit and receive levels as well as the background level. Also included are all necessary regulated voltages for both internal and external circuitry, allowing line-powered operation (no additional power supplies required). A Chip Select pin allows the chip to be powered down when not in use. A volume control function may be implemented with an external potentiometer. MC34018 applications include speakerphones for household and business use, intercom systems, automotive telephones, and others.



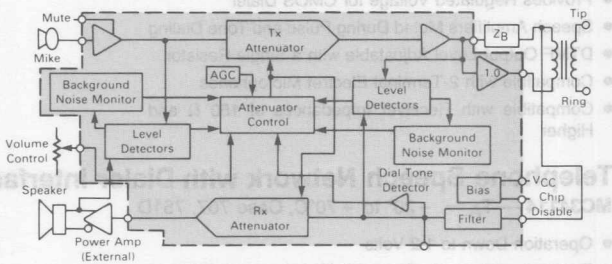
- All Necessary Level Detection and Attenuation Controls for a Hands-Free Telephone in a Single Integrated Circuit
- Background Noise Level Monitoring with Long Time Constant
- Wide Operating Dynamic Range Through Signal Compression
- On-chip Supply and Reference Voltage Regulation
- Typical 100 mW Output Power (into 25 Ω) with Peak Limiting to Minimize Distortion
- Chip Select Pin for Active/Standby Operation
- Linear Volume Control Function

Voice Switched Speakerphone Circuit

MC34118 — T_A = −20° to +60°C, Case 710, 751F

The MC34118 Voice Switched Speakerphone Circuit incorporates the necessary amplifiers, attenuators, level detectors, and control algorithm to form the heart of a high quality hands-free speakerphone system. Included are a microphone amplifier with adjustable gain and MUTE control, Transmit and Receive attenuators which operate in a complementary manner, level detectors at both input and output of both attenuators, and background noise monitors for both the transmit and receive channels. A Dial Tone Detector prevents the dial tone from being attenuated by the Receive background noise monitor circuit. Also included are two line driver amplifiers which can be used to form a hybrid network in conjunction with an external coupling transformer. A high-pass filter can be used to filter out 60 Hz noise in the receive channel, or for other filtering functions. A Chip Disable pin permits powering down the entire circuit to conserve power on long loops where loop current is at a minimum.

The MC34118 may be operated from a power supply, or it can be powered from the telephone line, requiring typically 5.0 mA. The MC34118 can be interfaced directly to Tip and Ring (through a coupling transformer) for stand-alone operation, or it can be used in conjunction with a handset speech network and/or other features of a featurephone.



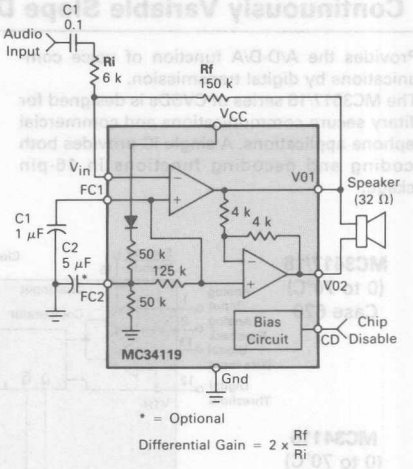
- Improved Attenuator Gain Range: 52 dB Between Transmit and Receive
- Low Voltage Operation for Line-Powered Applications (3.0–6.5 V)
- 4-Point Signal Sensing for Improved Sensitivity
- Background Noise Monitors for Both Transmit and Receive Paths
- Microphone Amplifier Gain Set by External Resistors — Mute Function Included
- Chip Disable for Active/Standby Operation
- On Board Filter Pinned-Out for User Defined Function
- Dial Tone Detector to Inhibit Receive Idle Mode During Dial Tone Presence
- Compatible with MC34119 Speaker Amplifier

Audio Amplifier

MC34119 — T_A = 0° to +70°C, Case 626, 751

A low power audio amplifier circuit intended (primarily) for telephone applications, such as speakerphones. Provides differential speaker outputs to maximize output swing at low supply voltages (2 volt min.). Coupling capacitors to the speaker, and snubbers, are not required. Overall gain is externally adjustable from 0 to 46 dB. A Chip Disable pin permits powering-down to mute the audio signal and reduce power consumption.

- Drives a Wide Range of Speaker Loads (16–100 Ω)
- Output Power Exceeds 250 mW with 32 Ω Speaker
- Low Distortion (THD = 0.4% Typical)
- Wide Operating Supply Voltage (2–16 Volts) — Allows Telephone Line Powered Applications.
- Low Quiescent Supply Current (2.5 mA Typical)
- Low Power-Down Quiescent Current (60 μA Typical)



Current Mode Switching Regulator

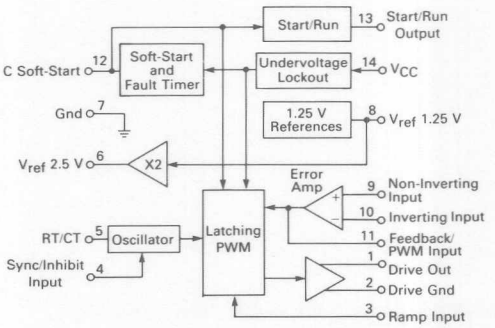
MC34129 — T_A = 0° to +70°C, Case 646, 751A

High performance current mode switching regulator for low-power digital telephones. Unique internal fault timer provides automatic restart for overload recovery. A start/run comparator is included to implement bootstrapped operation of V_{CC}.

Although primarily intended for digital telephone systems, these devices can be used cost effectively in many other applications.

On-chip functions and features include:

- Current Mode Operation to 300 kHz
- Automatic Feed Forward Compensation
- Latching PWM for Cycle-By-Cycle Current Limiting
- Latched-Off or Continuous Retry after Fault Timeout
- Soft-Start with Maximum Peak Switch Current Clamp
- Internally Trimmed 2% Bandgap Reference
- Input Undervoltage Lockout



8

Continuously Variable Slope Delta (CVSD) Modulator/Demodulator

Provides the A/D-D/A function of voice communications by digital transmission.

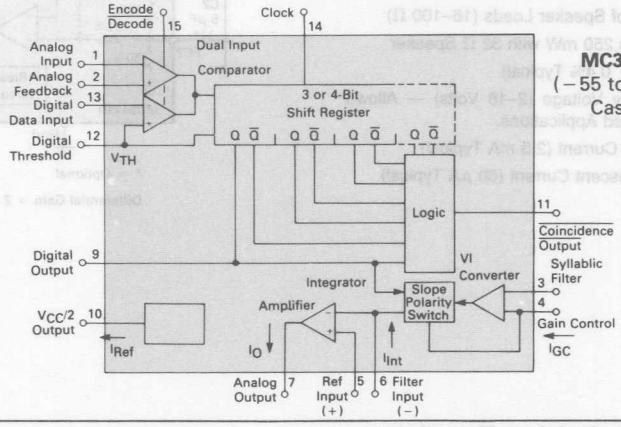
The MC3517/18 series of CVSDs is designed for military secure communications and commercial telephone applications. A single IC provides both encoding and decoding functions in 16-pin package.

- Encode and Decode functions on the Same Chip with a Digital Input for Selection
- CMOS Compatible Digital Output
- Digital Input Threshold Selectable ($V_{CC}/2$ reference provided on chip)
- MC3417/MC3517/MC34115 has a 3-Bit Algorithm (General Communications)
- MC3418/MC3518 has a 4-Bit Algorithm (Commercial Telephone)

MC3417/18
(0 to 70°C)
Case 620

MC34115
(0 to 70°C)
Case 648

MC3517/18
(−55 to +125°C)
Case 620



8

COMMUNICATION CIRCUITS

RF Communications

Device	Function	Page
MC1496	Balanced Modulator/Demodulator	8-13
MC1596	Balanced Modulator/Demodulator	8-13
MC2831A	Low Power FM Transmitter System	8-23
MC2833	Low Power FM Transmitter System	8-26
MC3356	Wideband FSK Receiver	8-29
MC3357	Low Power FM IF	8-35
MC3359	Low Power Narrowband FM IF	8-39
MC3361	Low Voltage Narrowband FM IF	8-45
MC3362	Low Power Dual Conversion FM Receiver	8-47
MC3363	Low Power Dual Conversion FM Receiver	8-52
MC3367	Low Voltage FM Narrowband Receiver	8-59
MC13041	AM Receiver Subsystem	See Chapter 9
MC13055	Wideband FSK Receiver	8-65

Telecommunications

Device	Function	Page
MC3417	Continuously Variable Slope Delta Modulator/Demodulator	*
MC3418	Continuously Variable Slope Delta Modulator/Demodulator	*
MC3419-1L	Telephone Line-Feed Circuit	*
MC3517	Continuously Variable Slope Delta Modulator/Demodulator	*
MC3518	Continuously Variable Slope Delta Modulator/Demodulator	*
MC33129	High Performance Current Mode Controller	See Chapter 3, *
MC34010	Electronic Telephone Circuit	*
MC34011A	Electronic Telephone Circuit	*
MC34012-1,-2,-3	Telephone Tone Ringer	*
MC34013A	Speech Network and Tone Ringer	*
MC34014	Telephone Speech Network with Dialer Interface	*
MC34017	Telephone Tone Ringer	*
MC34018	Voice Switched Speakerphone Circuit	*
MC34114	Telephone Speech Network with Dialer Interface	*
MC34115	Continuously Variable Slope Delta Modulator/Demodulator	*
MC34118	Voice Switched Speakerphone Circuit	*
MC34119	Low Power Audio Amplifier	See Chapter 9
MC34120	Subscriber Loop Interface Circuit	*
MC34129	High Performance Current Mode Controller	See Chapter 3, *

*See Telecommunications Device Data (DL136/R1)

RELATED APPLICATION NOTES

Application Note	Title	Related Device
AN531	MC1596 Balanced Modulator	MC1596
AN933	A Variety of Uses for the MC34012/MC34017 Tone Ringers	MC34012-1,-2,-3, MC34017
AN937	A Telephone Ringer which Complies with FCC and EIA Impedance Standards	MC34012, MC34017
AN957	Interfacing the Speakerphone to the MC34010/11/13 Speech Networks	MC34010, MC34011A, MC34013A
AN959	A Speakerphone with Receive Idle Mode	MC34018
AN960	Equalization of DTMF Signals Using the MC34014	MC34014
AN976	A New High Performance Current Mode Controller Teams Up with Current Sensing Power MOSFETs	MC34129
AN980	Low Power FM Dual Conversion Receivers	MC3362, MC3363
AN1002	A Handsfree Featurephone Design Using the MC34114 Speech Network and the MC34018 Speakerphone ICs	MC34018, MC34114
ANHK07	A High Performance, Manual-Tuned AM Stereo Receiver for Automotive Application Using Motorola ICs: MC13021, MC13020 & MC13041	MC13041

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ORDERING INFORMATION

Device	Temperature Range	Package
MC1496D	0°C to +70°C	SO-14
MC1496G		Metal Can
MC1496L		Ceramic DIP
MC1496P		Plastic DIP
MC1596G	−55°C to +125°C	Metal Can
MC1596L		Ceramic DIP

MC1496
MC1596

Specifications and Applications Information

BALANCED MODULATOR/DEMODULATOR

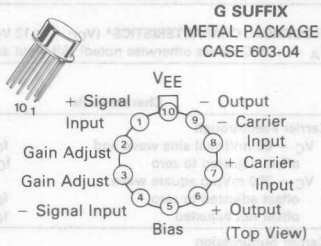
SILICON MONOLITHIC INTEGRATED CIRCUIT

BALANCED MODULATOR/ DEMODULATOR

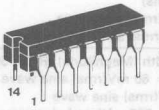
. . . designed for use where the output voltage is a product of an input voltage (signal) and a switching function (carrier). Typical applications include suppressed carrier and amplitude modulation, synchronous detection, FM detection, phase detection, and chopper applications. See Motorola Application Note AN-531 for additional design information.

- Excellent Carrier Suppression — 65 dB typ @ 0.5 MHz
  — 50 dB typ @ 10 MHz
- Adjustable Gain and Signal Handling
- Balanced Inputs and Outputs
- High Common Mode Rejection — 85 dB typ

G SUFFIX
METAL PACKAGE
CASE 603-04



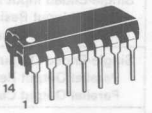
L SUFFIX
CERAMIC PACKAGE
CASE 632-08

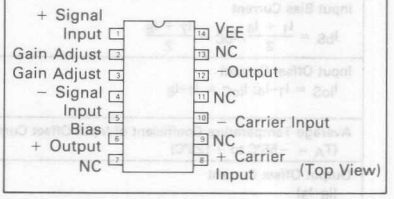


D SUFFIX
PLASTIC PACKAGE
CASE 751A-02
SO-14



P SUFFIX
PLASTIC PACKAGE
CASE 646-06





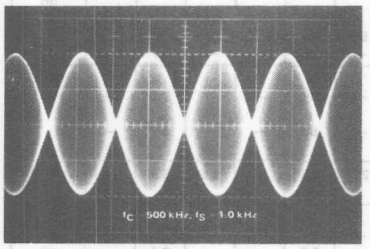


FIGURE 1 — SUPPRESSED-CARRIER OUTPUT WAVEFORM

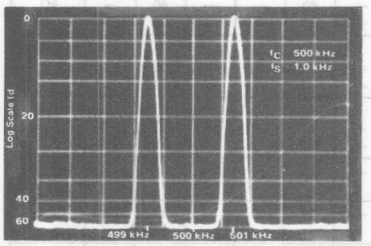


FIGURE 2 — SUPPRESSED-CARRIER SPECTRUM

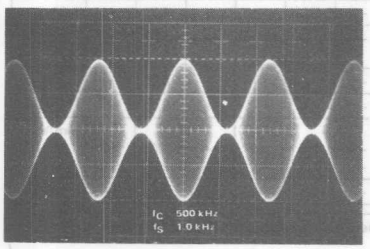
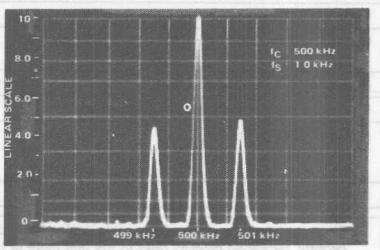


FIGURE 3 — AMPLITUDE-MODULATION OUTPUT WAVEFORM

FIGURE 4 — AMPLITUDE-MODULATION SPECTRUM



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MAXIMUM RATINGS* (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Applied Voltage ($V_6 - V_7$, $V_8 - V_1$, $V_9 - V_7$, $V_9 - V_8$, $V_7 - V_4$, $V_7 - V_1$, $V_8 - V_4$, $V_6 - V_8$, $V_2 - V_5$, $V_3 - V_5$)	ΔV	30	Vdc
Differential Input Signal	$V_7 - V_8$ $V_4 - V_1$	+5.0 $\pm(5 + I_5R_e)$	Vdc
Maximum Bias Current	I_5	10	mA
Thermal Resistance, Junction to Air Ceramic Dual In-Line Package Plastic Dual In-Line Package Metal Package	$R_{\theta JA}$	 100 100 160	°C/W
Operating Temperature Range MC1496 MC1596	T_A	 0 to +70 −55 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS* (V_{CC} = +12 Vdc, V_{EE} = −8.0 Vdc, I_5 = 1.0 mAdc, R_L = 3.9 kΩ, R_e = 1.0 kΩ, T_A = +25°C unless otherwise noted) (All input and output characteristics are single-ended unless otherwise noted.)

Characteristic	Fig.	Note	Symbol	MC1596 Min	MC1596 Typ	MC1596 Max	MC1496 Min	MC1496 Typ	MC1496 Max	Unit
Carrier Feedthrough	5	1	V_{CFT}							μV(rms)
V_C = 60 mV(rms) sine wave and offset adjusted to zero, f_C = 1.0 kHz				—	40	—	—	40	—	
f_C = 10 MHz				—	140	—	—	140	—	mV(rms)
V_C = 300 mVp-p square wave: offset adjusted to zero, f_C = 1.0 kHz				—	0.04	0.2	—	0.04	0.4	
offset not adjusted, f_C = 1.0 kHz				—	20	100	—	20	200	
Carrier Suppression	5	2	V_{CS}							dB
f_S = 10 kHz, 300 mV(rms)										
f_C = 500 kHz, 60 mV(rms) sine wave				50	65	—	40	65	—	
f_C = 10 MHz, 60 mV(rms) sine wave				—	50	—	—	50	—	k
Transadmittance Bandwidth (Magnitude) (R_L = 50 ohms)	8	8	BW_{3dB}							MHz
Carrier Input Port, V_C = 60 mV(rms) sine wave f_S = 1.0 kHz, 300 mV(rms) sine wave				—	300	—	—	300	—	
Signal Input Port, V_S = 300 mV(rms) sine wave $\lvert V_C\rvert$ = 0.5 Vdc				—	80	—	—	80	—	
Signal Gain V_S = 100 mV(rms), f = 1.0 kHz; $\lvert V_C\rvert$ = 0.5 Vdc	10	3	A_{VS}	2.5	3.5	—	2.5	3.5	—	V/V
Single-Ended Input Impedance, Signal Port, f = 5.0 MHz	6	—								
Parallel Input Resistance			r_{ip}	—	200	—	—	200	—	kΩ
Parallel Input Capacitance			c_{ip}	—	2.0	—	—	2.0	—	pF
Single-Ended Output Impedance, f = 10 MHz	6	—								
Parallel Output Resistance			r_{op}	—	40	—	—	40	—	kΩ
Parallel Output Capacitance			c_{oo}	—	5.0	—	—	5.0	—	pF
Input Bias Current $I_{bS} = \frac{I_1 + I_4}{2}$; $I_{bC} = \frac{I_7 + I_8}{2}$	7	—								μA
			I_{bS}	—	12	25	—	12	30	
			I_{bC}	—	12	25	—	12	30	
Input Offset Current $I_{ioS} = I_1 - I_4$; $I_{ioC} = I_7 - I_8$	7	—								μA
			$\lvert I_{ioS}\rvert$	—	0.7	5.0	—	0.7	7.0	
			$\lvert I_{ioC}\rvert$	—	0.7	5.0	—	0.7	7.0	
Average Temperature Coefficient of Input Offset Current (T_A = −55°C to +125°C)	7	—	$\lvert TC_{Iio}\rvert$	—	2.0	—	—	2.0	—	nA/°C
Output Offset Current $(I_6 - I_9)$	7	—	$\lvert I_{oo}\rvert$	—	14	50	—	14	80	μA
Average Temperature Coefficient of Output Offset Current (T_A = −55°C to +125°C)	7	—	$\lvert TC_{Ioo}\rvert$	—	90	—	—	90	—	nA/°C
Common-Mode Input Swing, Signal Port, f_S = 1.0 kHz	9	4	CMV	—	5.0	—	—	5.0	—	Vp-p
Common-Mode Gain, Signal Port, f_S = 1.0 kHz, $\lvert V_C\rvert$ = 0.5 Vdc	9	—	ACM	—	−85	—	—	−85	—	dB
Common-Mode Quiescent Output Voltage (Pin 6 or Pin 9)	10	—	V_{out}	—	8.0	—	—	8.0	—	Vp-p
Differential Output Voltage Swing Capability	10	—	V_{out}	—	8.0	—	—	8.0	—	Vp-p
Power Supply Current	7	6								mAdc
$I_6 + I_9$			I_{CC}	—	2.0	3.0	—	2.0	4.0	
I_{10}			I_{EE}	—	3.0	4.0	—	3.0	5.0	
DC Power Dissipation	7	5	P_D	—	33	—	—	33	—	mW

* Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.

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GENERAL OPERATING INFORMATION *

Note 1 – Carrier Feedthrough

Carrier feedthrough is defined as the output voltage at carrier frequency with only the carrier applied (signal voltage = 0).

Carrier null is achieved by balancing the currents in the differential amplifier by means of a bias trim potentiometer (R_1 of Figure 5).

Note 2 – Carrier Suppression

Carrier suppression is defined as the ratio of each sideband output to carrier output for the carrier and signal voltage levels specified.

Carrier suppression is very dependent on carrier input level, as shown in Figure 22. A low value of the carrier does not fully switch the upper switching devices, and results in lower signal gain, hence lower carrier suppression. A higher than optimum carrier level results in unnecessary device and circuit carrier feedthrough, which again degenerates the suppression figure. The MC1596 has been characterized with a 60 mV(rms) sinewave carrier input signal. This level provides optimum carrier suppression at carrier frequencies in the vicinity of 500 kHz, and is generally recommended for balanced modulator applications.

Carrier feedthrough is independent of signal level, V_S. Thus carrier suppression can be maximized by operating with large signal levels. However, a linear operating mode must be maintained in the signal-input transistor pair – or harmonics of the modulating signal will be generated and appear in the device output as spurious sidebands of the suppressed carrier. This requirement places an upper limit on input-signal amplitude (see Note 3 and Figure 20). Note also that an optimum carrier level is recommended in Figure 22 for good carrier suppression and minimum spurious sideband generation.

At higher frequencies circuit layout is very important in order to minimize carrier feedthrough. Shielding may be necessary in order to prevent capacitive coupling between the carrier input leads and the output leads.

Note 3 – Signal Gain and Maximum Input Level

Signal gain (single-ended) at low frequencies is defined as the voltage gain,

$$A_{VS} = \frac{V_o}{V_S} = \frac{R_L}{R_e + 2r_e} \text{ where } r_e = \frac{26\text{ mV}}{I_5\text{ (mA)}}$$

A constant dc potential is applied to the carrier input terminals to fully switch two of the upper transistors "on" and two transistors "off" (V_C = 0.5 Vdc). This in effect forms a cascode differential amplifier.

Linear operation requires that the signal input be below a critical value determined by R_E and the bias current I_5

$$V_S \leq I_5 R_E \text{ (Volts peak)}$$

Note that in the test circuit of Figure 10, V_S corresponds to a maximum value of 1 volt peak.

Note 4 – Common-Mode Swing

The common-mode swing is the voltage which may be applied to both bases of the signal differential amplifier, without saturating the current sources or without saturating the differential amplifier itself by swinging it into the upper switching devices. This swing is variable depending on the particular circuit and biasing conditions chosen (see Note 6).

Note 5 – Power Dissipation

Power dissipation, P_D, within the integrated circuit package should be calculated as the summation of the voltage-current products at each port, i.e. assuming $V_9 = V_6$, $I_5 = I_6 = I_9$ and ignoring base current, $P_D = 2\ I_5\ (V_6 - V_{10}) + I_5\ (V_5 - V_{10})$ where subscripts refer to pin numbers.

Note 6 – Design Equations

The following is a partial list of design equations needed to operate the circuit with other supply voltages and input conditions. See Note 3 for R_e equation.

A. Operating Current

The internal bias currents are set by the conditions at pin 5. Assume:

$$I_5 = I_6 = I_9$$

$$I_B \ll I_C \text{ for all transistors}$$

then:

$$R_5 = \frac{V^- - \phi}{I_5} - 500\ \Omega \quad \text{where: } R_5 \text{ is the resistor between pin 5 and ground}$$

$\phi = 0.75$ V at $T_A = +25^oC$

The MC1596 has been characterized for the condition I_5 = 1.0 mA and is the generally recommended value.

B. Common-Mode Quiescent Output Voltage

$$V_6 = V_9 = V^+ - I_5 R_L$$

Note 7 – Biasing

The MC1596 requires three dc bias voltage levels which must be set externally. Guidelines for setting up these three levels include maintaining at least 2 volts collector-base bias on all transistors while not exceeding the voltages given in the absolute maximum rating table;

$$30 \text{ Vdc} \geq [(V_6, V_9) - (V_7, V_8)] \geq 2 \text{ Vdc}$$

$$30 \text{ Vdc} \geq [(V_7, V_8) - (V_1, V_4)] \geq 2.7 \text{ Vdc}$$

$$30 \text{ Vdc} \geq [(V_1, V_4) - (V_5)] \geq 2.7 \text{ Vdc}$$

The foregoing conditions are based on the following approximations:

$$V_6 = V_9, \quad V_7 = V_8, \quad V_1 = V_4$$

Bias currents flowing into pins 1, 4, 7, and 8 are transistor base currents and can normally be neglected if external bias dividers are designed to carry 1.0 mA or more.

Note 8 – Transadmittance Bandwidth

Carrier transadmittance bandwidth is the 3-dB bandwidth of the device forward transadmittance as defined by:

$$Y_{21C} = \left.\frac{i_o \text{ (each sideband)}}{v_s \text{ (signal)}}\right| V_o = 0$$

Signal transadmittance bandwidth is the 3-dB bandwidth of the device forward transadmittance as defined by:

$$Y_{21S} = \left.\frac{i_o \text{ (signal)}}{v_s \text{ (signal)}}\right| V_c = 0.5 \text{ Vdc}, V_o = 0$$

*Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.

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Note 9 – Coupling and Bypass Capacitors C_1 and C_2

Capacitors C_1 and C_2 (Figure 5) should be selected for a reactance of less than 5.0 ohms at the carrier frequency.

Note 10 – Output Signal, V_o

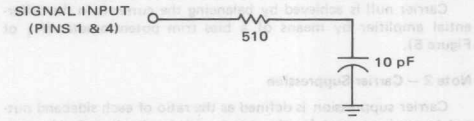
The output signal is taken from pins 6 and 9, either balanced or single-ended. Figure 12 shows the output levels of each of the two output sidebands resulting from variations in both the carrier and modulating signal inputs with a single-ended output connection.

Note 11 – Negative Supply, V_{EE}

V_{EE} should be dc only. The insertion of an RF choke in series with V_{EE} can enhance the stability of the internal current sources.

Note 12 – Signal Port Stability

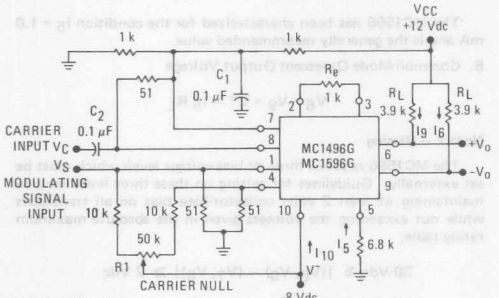
Under certain values of driving source impedance, oscillation may occur. In this event, an RC suppression network should be connected directly to each input using short leads. This will reduce the Q of the source-tuned circuits that cause the oscillation.



An alternate method for low-frequency applications is to insert a 1 k-ohm resistor in series with the inputs, pins 1 and 4. In this case input current drift may cause serious degradation of carrier suppression.

TEST CIRCUITS

FIGURE 5 – CARRIER REJECTION AND SUPPRESSION



NOTE: Shielding of input and output leads may be needed to properly perform these tests.

FIGURE 6 – INPUT-OUTPUT IMPEDANCE

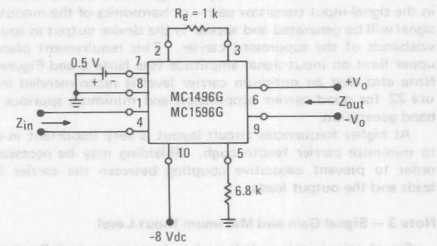


FIGURE 7 – BIAS AND OFFSET CURRENTS

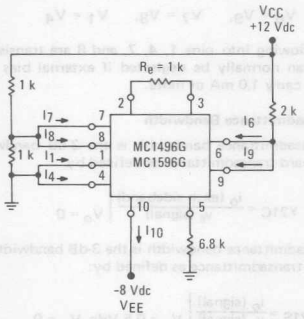
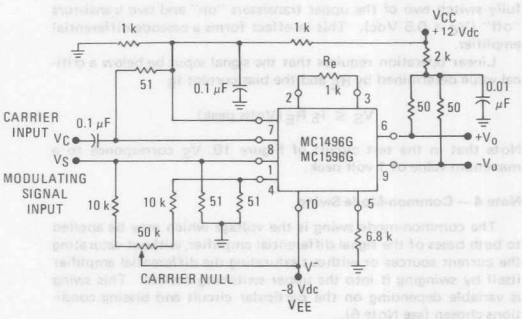


FIGURE 8 – TRANSCONDUCTANCE BANDWIDTH



NOTE: Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.

TEST CIRCUITS (continued)

FIGURE 9 – COMMON-MODE GAIN

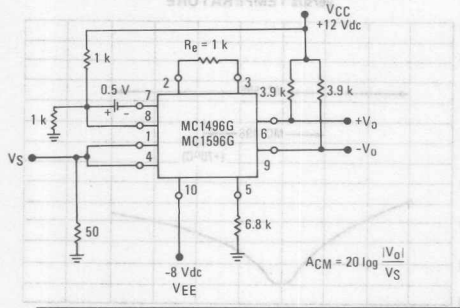
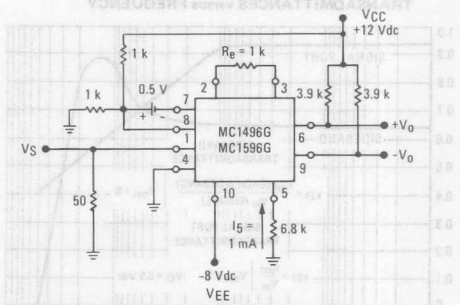


FIGURE 10 – SIGNAL GAIN AND OUTPUT SWING



NOTE: Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.

TYPICAL CHARACTERISTICS (continued)

Typical characteristics were obtained with circuit shown in Figure 5, f_C = 500 kHz (sine wave), V_C = 60 mV(rms), f_S = 1 kHz, V_S = 300 mV(rms), T_A = +25°C unless otherwise noted.

FIGURE 11 – SIDEBAND OUTPUT versus CARRIER LEVELS

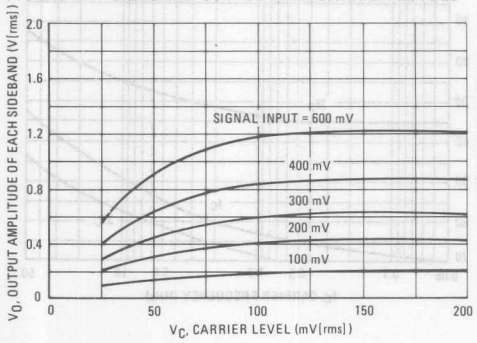


FIGURE 12 – SIGNAL-PORT PARALLEL-EQUIVALENT INPUT RESISTANCE versus FREQUENCY

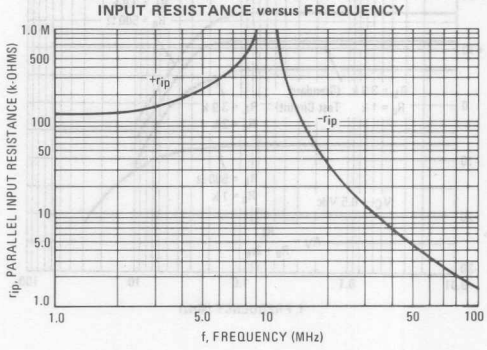


FIGURE 13 – SIGNAL-PORT PARALLEL-EQUIVALENT INPUT CAPACITANCE versus FREQUENCY

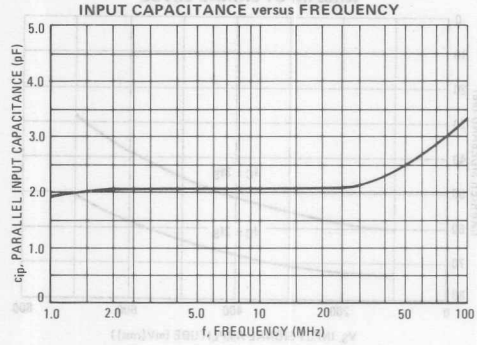
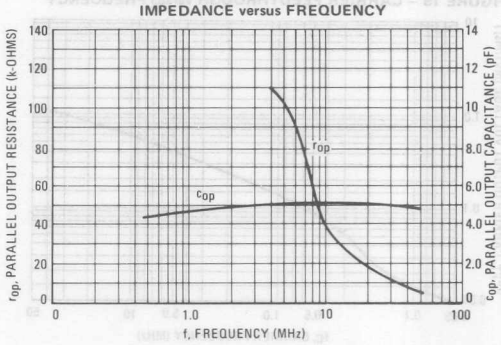


FIGURE 14 – SINGLE-ENDED OUTPUT IMPEDANCE versus FREQUENCY



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TYPICAL CHARACTERISTICS (continued)

Typical characteristics were obtained with circuit shown in Figure 5, f_C = 500 kHz (sine wave), V_C = 60 mV(rms), f_S = 1 kHz, V_S = 300 mV(rms), T_A = +25°C unless otherwise noted.

FIGURE 15 – SIDEBAND AND SIGNAL PORT TRANSADMITTANCES versus FREQUENCY

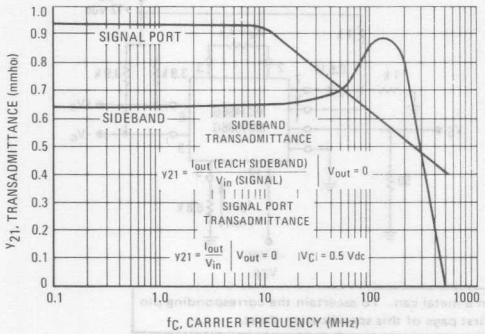


FIGURE 16 – CARRIER SUPPRESSION versus TEMPERATURE

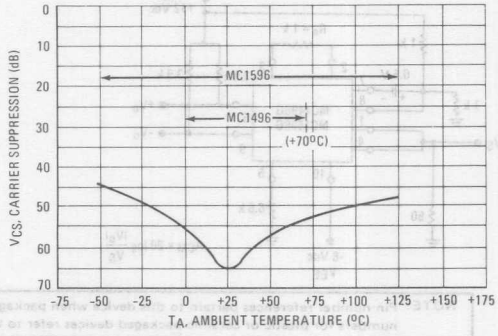


FIGURE 17 – SIGNAL-PORT FREQUENCY RESPONSE

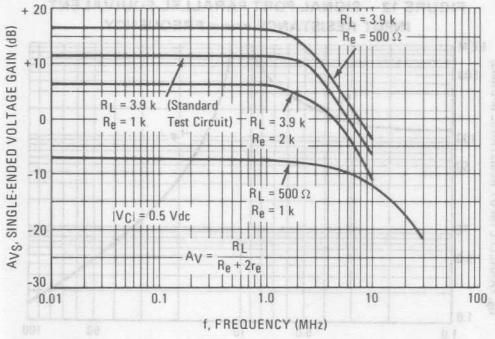


FIGURE 18 – CARRIER SUPPRESSION versus FREQUENCY

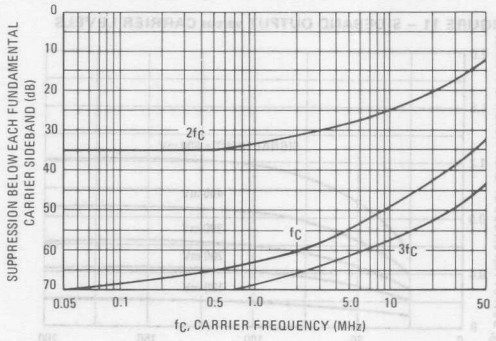


FIGURE 19 – CARRIER FEEDTHROUGH versus FREQUENCY

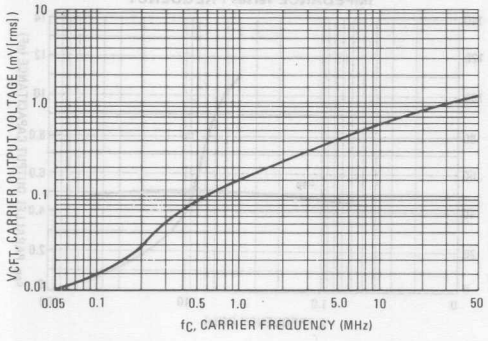
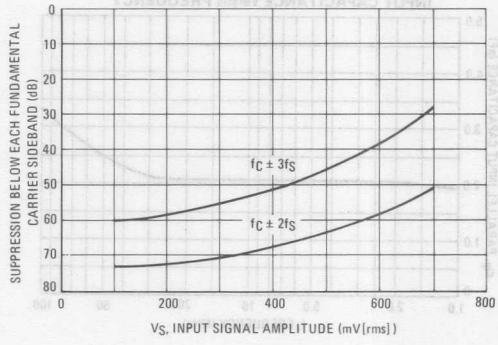


FIGURE 20 – SIDEBAND HARMONIC SUPPRESSION versus INPUT SIGNAL LEVEL



TYPICAL CHARACTERISTICS (continued)

FIGURE 21 – SUPPRESSION OF CARRIER HARMONIC SIDEBANDS versus CARRIER FREQUENCY

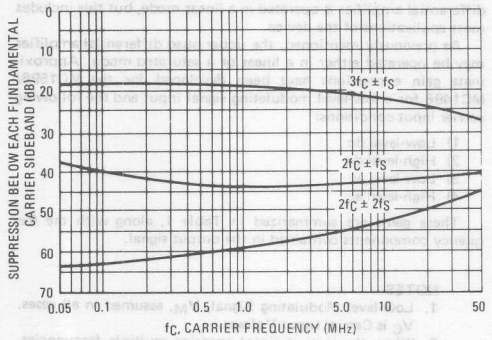
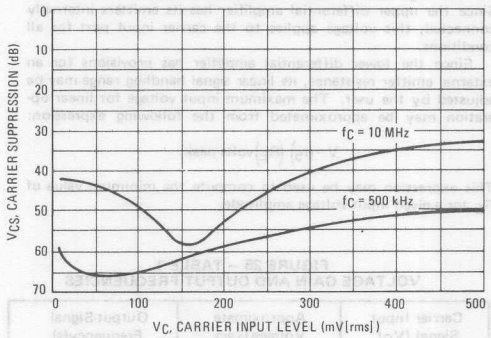


FIGURE 22 – CARRIER SUPPRESSION versus CARRIER INPUT LEVEL



OPERATIONS INFORMATION

The MC1596/MC1496, a monolithic balanced modulator circuit, is shown in Figure 23.

This circuit consists of an upper quad differential amplifier driven by a standard differential amplifier with dual current sources. The output collectors are cross-coupled so that full-wave balanced multiplication of the two input voltages occurs. That is, the output signal is a constant times the product of the two input signals.

Mathematical analysis of linear ac signal multiplication indicates that the output spectrum will consist of only the sum and difference of the two input frequencies. Thus, the device may be used as a balanced modulator, doubly balanced mixer, product detector, frequency doubler, and other applications requiring these particular output signal characteristics.

The lower differential amplifier has its emitters connected to the package pins so that an external emitter resistance may be used. Also, external load resistors are employed at the device output.

FIGURE 23 – CIRCUIT SCHEMATIC

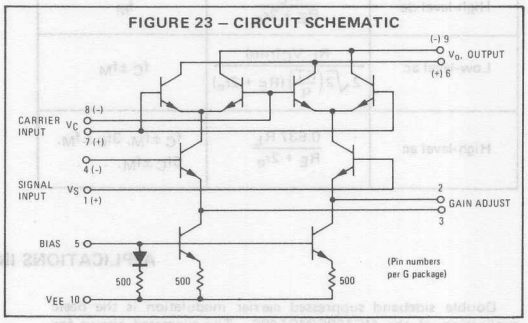
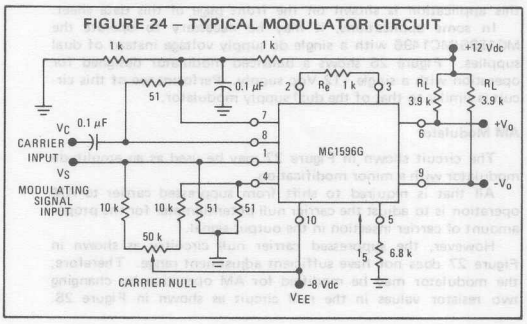


FIGURE 24 – TYPICAL MODULATOR CIRCUIT



Signal Levels

The upper quad differential amplifier may be operated either in a linear or a saturated mode. The lower differential amplifier is operated in a linear mode for most applications.

For low-level operation at both input ports, the output signal will contain sum and difference frequency components and have an amplitude which is a function of the product of the input signal amplitudes.

For high-level operation at the carrier input port and linear operation at the modulating signal port, the output signal will contain sum and difference frequency components of the modulating signal frequency and the fundamental and odd harmonics of the carrier frequency. The output amplitude will be a constant times the modulating signal amplitude. Any amplitude variations in the carrier signal will not appear in the output.

NOTE: Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.

OPERATIONS INFORMATION (continued)

The linear signal handling capabilities of a differential amplifier are well defined. With no emitter degeneration, the maximum input voltage for linear operation is approximately 25 mV peak. Since the upper differential amplifier has its emitters internally connected, this voltage applies to the carrier input port for all conditions.

Since the lower differential amplifier has provisions for an external emitter resistance, its linear signal handling range may be adjusted by the user. The maximum input voltage for linear operation may be approximated from the following expression:

$$V = (I_5)(R_E) \text{ volts peak.}$$

This expression may be used to compute the minimum value of R_E for a given input voltage amplitude.

FIGURE 25 – TABLE 1
VOLTAGE GAIN AND OUTPUT FREQUENCIES

Carrier Input Signal (V_C)	Approximate Voltage Gain	Output Signal Frequency(s)
Low-level dc	$\frac{R_L V_C}{2(R_E + 2r_e)\left(\frac{KT}{q}\right)}$	f_M
High-level dc	$\frac{R_L}{R_E + 2r_e}$	f_M
Low-level ac	$\frac{R_L V_C(rms)}{2\sqrt{2}\left(\frac{KT}{q}\right)(R_E + 2r_e)}$	$f_C \pm f_M$
High-level ac	$\frac{0.637\, R_L}{R_E + 2r_e}$	$f_C \pm f_M$, $3f_C \pm f_M$, $5f_C \pm f_M$, . . .

The gain from the modulating signal input port to the output is the MC1596/MC1496 gain parameter which is most often of interest to the designer. This gain has significance only when the lower differential amplifier is operated in a linear mode, but this includes most applications of the device.

As previously mentioned, the upper quad differential amplifier may be operated either in a linear or a saturated mode. Approximate gain expressions have been developed for the MC1596/MC1496 for a low-level modulating signal input and the following carrier input conditions:

1) Low-level dc
2) High-level dc
3) Low-level ac
4) High-level ac

These gains are summarized in Table 1, along with the frequency components contained in the output signal.

NOTES:
1. Low-level Modulating Signal, V_M, assumed in all cases. V_C is Carrier Input Voltage.
2. When the output signal contains multiple frequencies, the gain expression given is for the output amplitude of each of the two desired outputs, $f_C + f_M$ and $f_C - f_M$.
3. All gain expressions are for a single-ended output. For a differential output connection, multiply each expression by two.
4. R_L = Load resistance.
5. R_E = Emitter resistance between pins 2 and 3.
6. r_e = Transistor dynamic emitter resistance, at +25°C; $r_e \approx \frac{26 \text{ mV}}{I_5 \text{ (mA)}}$
7. K = Boltzmann's Constant, T = temperature in degrees Kelvin, q = the charge on an electron. $\frac{KT}{q} \approx 26$ mV at room temperature

APPLICATIONS INFORMATION

Double sideband suppressed carrier modulation is the basic application of the MC1596/MC1496. The suggested circuit for this application is shown on the front page of this data sheet.

In some applications, it may be necessary to operate the MC1596/MC1496 with a single dc supply voltage instead of dual supplies. Figure 26 shows a balanced modulator designed for operation with a single +12 Vdc supply. Performance of this circuit is similar to that of the dual supply modulator.

AM Modulator

The circuit shown in Figure 27 may be used as an amplitude modulator with a minor modification.

All that is required to shift from suppressed carrier to AM operation is to adjust the carrier null potentiometer for the proper amount of carrier insertion in the output signal.

However, the suppressed carrier null circuitry as shown in Figure 27 does not have sufficient adjustment range. Therefore, the modulator may be modified for AM operation by changing two resistor values in the null circuit as shown in Figure 28.

Product Detector

The MC1596/MC1496 makes an excellent SSB product detector (see Figure 29).

This product detector has a sensitivity of 3.0 microvolts and a dynamic range of 90 dB when operating at an intermediate frequency of 9 MHz.

The detector is broadband for the entire high frequency range. For operation at very low intermediate frequencies down to 50 kHz the 0.1 μF capacitors on pins 7 and 8 should be increased to 1.0 μF. Also, the output filter at pin 9 can be tailored to a specific intermediate frequency and audio amplifier input impedance.

As in all applications of the MC1596/MC1496, the emitter resistance between pins 2 and 3 may be increased or decreased to adjust circuit gain, sensitivity, and dynamic range.

This circuit may also be used as an AM detector by introducing carrier signal at the carrier input and an AM signal at the SSB input.

The carrier signal may be derived from the intermediate frequency signal or generated locally. The carrier signal may be introduced with or without modulation, provided its level is sufficiently high to saturate the upper quad differential amplifier. If the carrier signal is modulated, a 300 mV(rms) input level is recommended.

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Doubly Balanced Mixer

The MC1596/MC1496 may be used as a doubly balanced mixer with either broadband or tuned narrow band input and output networks.

The local oscillator signal is introduced at the carrier input port with a recommended amplitude of 100 mV(rms).

Figure 30 shows a mixer with a broadband input and a tuned output.

Frequency Doubler

The MC1596/MC1496 will operate as a frequency doubler by introducing the same frequency at both input ports.

Figures 31 and 32 show a broadband frequency doubler and a tuned output very high frequency (VHF) doubler, respectively.

Phase Detection and FM Detection

The MC1596/MC1496 will function as a phase detector. High-level input signals are introduced at both inputs. When both inputs are at the same frequency the MC1596/MC1496 will deliver an output which is a function of the phase difference between the two input signals.

An FM detector may be constructed by using the phase detector principle. A tuned circuit is added at one of the inputs to cause the two input signals to vary in phase as a function of frequency. The MC1596/MC1496 will then provide an output which is a function of the input signal frequency.

NOTE: Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.

TYPICAL APPLICATIONS

FIGURE 26 – BALANCED MODULATOR
(+12 Vdc SINGLE SUPPLY)

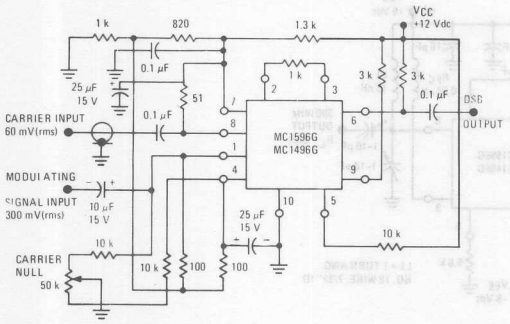


FIGURE 27 – BALANCED MODULATOR-DEMODULATOR

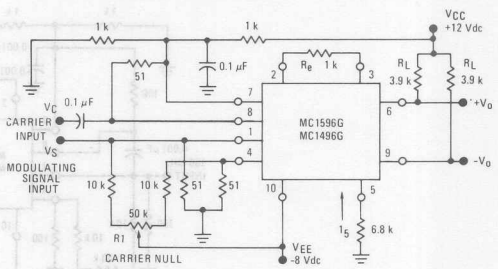


FIGURE 28 – AM MODULATOR CIRCUIT

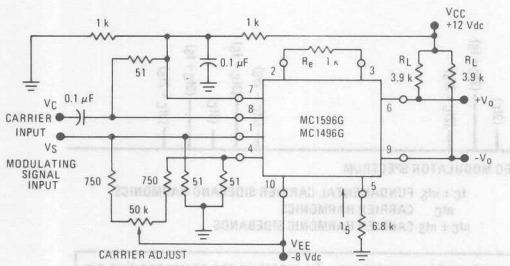
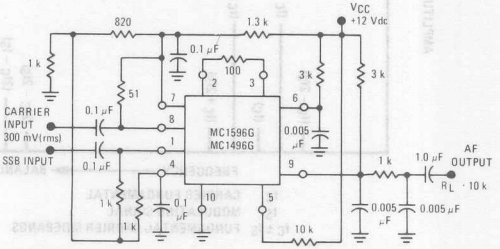


FIGURE 29 – PRODUCT DETECTOR
(+12 Vdc SINGLE SUPPLY)



TYPICAL APPLICATIONS (continued)

FIGURE 30 – DOUBLY BALANCED MIXER
(BROADBAND INPUTS, 9.0 MHz TUNED OUTPUT)

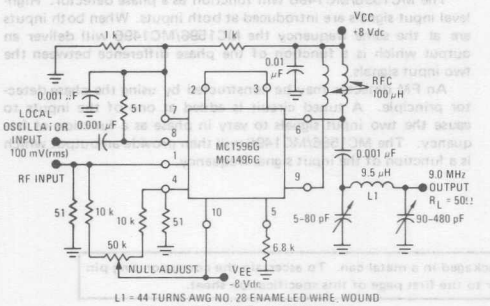


FIGURE 31 – LOW-FREQUENCY DOUBLER

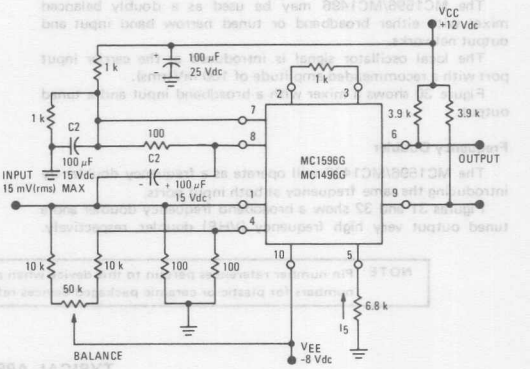
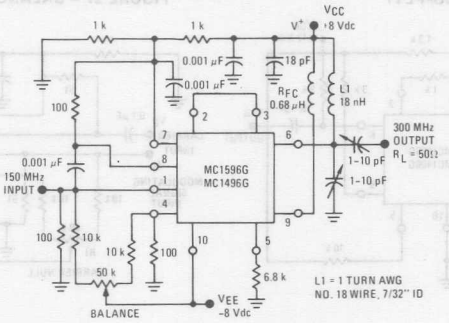
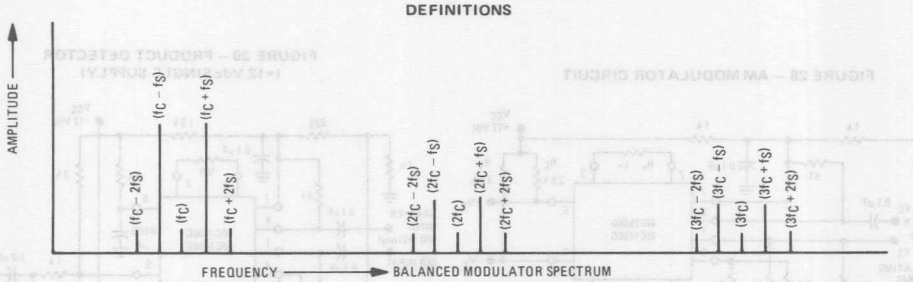


FIGURE 32 – 150 to 300 MHz DOUBLER



DEFINITIONS



f_C	CARRIER FUNDAMENTAL	$f_C \pm nf_S$	FUNDAMENTAL CARRIER SIDEBAND HARMONICS
f_S	MODULATING SIGNAL	nf_C	CARRIER HARMONICS
$f_C \pm f_S$	FUNDAMENTAL CARRIER SIDEBANDS	$nf_C \pm nf_S$	CARRIER HARMONIC SIDEBANDS

NOTE: Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.

MOTOROLA

MC2831A

LOW POWER FM TRANSMITTER SYSTEM

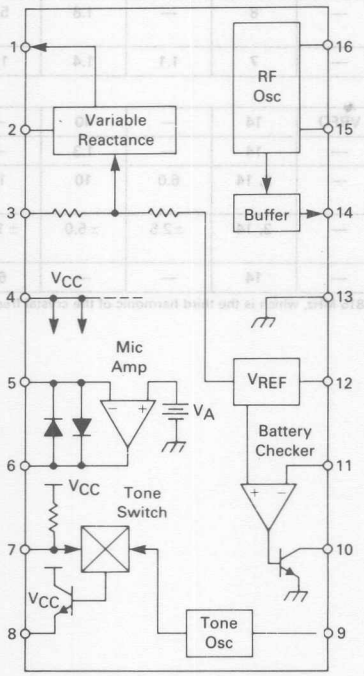
The MC2831A is a one-chip FM transmitter subsystem designed for cordless telephone and FM communication equipment. It includes a Microphone Amplifier, Pilot Tone Oscillator, Voltage Controlled Oscillator and Battery Monitor.

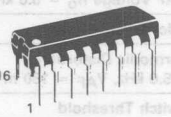
- Wide Range of Operating Supply Voltage (3.0 V–8.0 V)
- Low Drain Current (4.0 mA Typ Full Operation at V_{CC} = 4.0 V)
- Battery Checker (290 μA Typ at V_{CC} = 4.0 V)
- Low Number of External Parts Required

LOW POWER FM TRANSMITTER SYSTEM

SILICON MONOLITHIC INTEGRATED CIRCUIT

FIGURE 1 — FUNCTIONAL BLOCK DIAGRAM



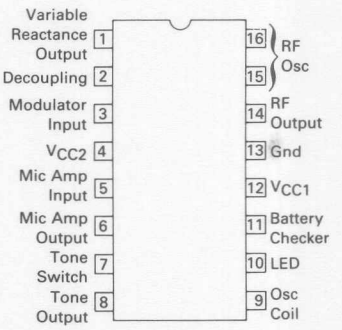


P SUFFIX
PLASTIC PACKAGE
CASE 648-06



D SUFFIX
PLASTIC PACKAGE
CASE 751B-03
SO-16

PIN ASSIGNMENTS



MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4, 12	V_{CC}	10	Vdc
Operating Supply Voltage Range	4, 12	V_{CC}	3.0 to 8.0	Vdc
Battery Checker Output Sink Current	10	I_{LED}	25	mA
Junction Temperature	—	T_J	+150	°C
Operating Ambient Temperature Range	—	T_A	−30 to +75	°C
Storage Temperature Range	—	T_{stg}	−65 to +150	°C

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Drain Current	I_{CC1}	12	150	290	420	μA
Drain Current	I_{CC2}	4	2.2	3.6	6.5	mA

BATTERY CHECKER

Threshold Voltage (LED Off → On)	V_{TB}	11	1.0	1.2	1.4	Vdc
Output Saturation Voltage (Pin 11 = 0 V, Pin 10 Sink Current = 5.0 mA)	V_{OSAT}	10	—	0.15	0.5	Vdc

MIC AMPLIFIER

Voltage Gain, Closed Loop (V_{in} = 1.0 mV_{rms}, f_{in} = 1.0 kHz)	—	5, 6	27	30	33	dB
Output dc Voltage	—	6	1.1	1.4	1.7	Vdc
Output Swing (V_{in} = 30 mV_{rms}, f_{in} = 1.0 kHz)	—	6	0.8	1.2	1.6	Vp-p
Total Harmonic Distortion (V_0 = 31 mV_{rms}, f_{in} = 1.0 kHz)	THD	6	—	0.7	—	%

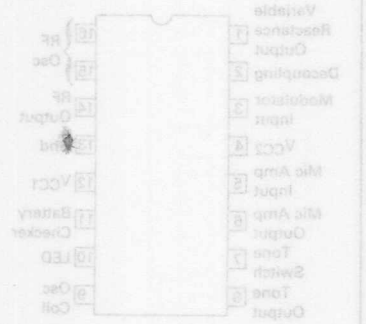
PILOT TONE OSCILLATOR (250 Ω LOADING)

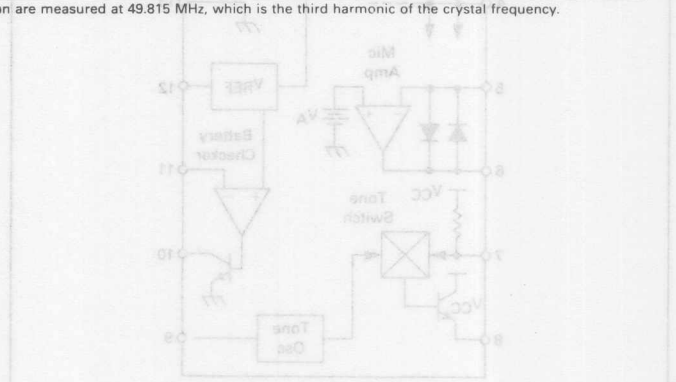
Output AF Voltage (f_o = 5.0 kHz)	—	8	—	50	—	mV_{rms}
Output dc Voltage	—	8	—	1.4	—	Vdc
Total Harmonic Distortion (f_o = 5.0 kHz, V_{AF} = 150 mV_{rms})	—	8	—	1.8	5.0	%
Tone Switch Threshold	—	7	1.1	1.4	1.7	Vdc

FM MODULATOR (120 Ω LOADING)

Output RF Voltage (f_o = 16.6 MHz)	VRFO	14	—	40	—	mV_{rms}
Output dc Voltage	—	14	—	1.3	—	Vdc
Modulation Sensitivity (Note 1) (V_{in} = 1.0 V ± 0.2 V)	—	3, 14	6.0	10	18	Hz/mVdc
Maximum Deviation (Note 1) (V_{in} = 0 V to +2.0 V)	—	3, 14	±2.5	±5.0	±12.5	kHz
RF Frequency Range	—	14	—	—	60	MHz

Note 1. Modulation sensitivity and maximum deviation are measured at 49.815 MHz, which is the third harmonic of the crystal frequency.





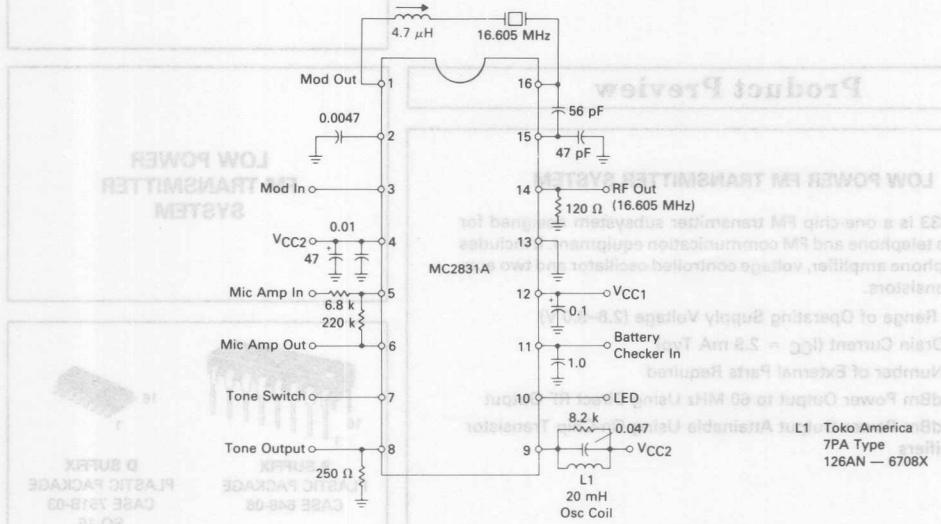
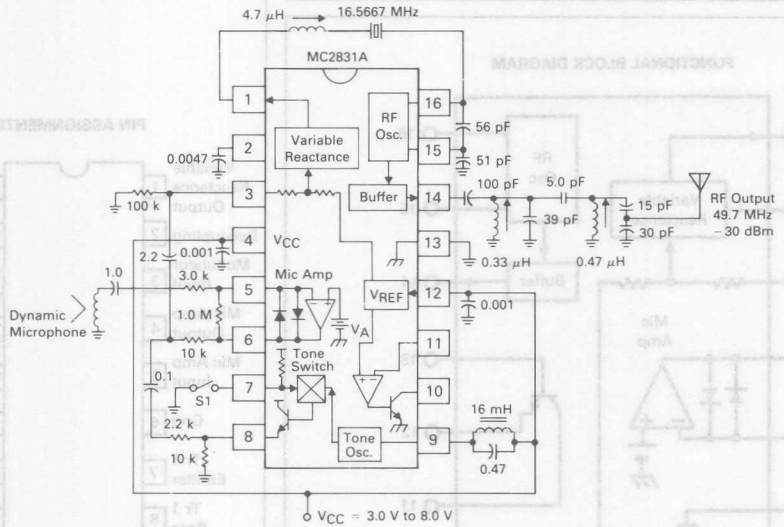


FIGURE 3 — SINGLE CHIP FM VHF TRANSMITTER AT 49.7 MHz



NOTES:

S1 is a normally closed push button type switch.

The crystal used is fundamental mode, calibrated for parallel resonance with a 32 pF load. The 49.7 MHz output is generated in the output buffer, which generates useful harmonics to 60 MHz.

The network on the output at Pin 14 provides output tuning and impedance matching to 50 Ω at 49.7 MHz. Harmonics are suppressed by more than 25 dB.

Battery checker circuit (Pins 10, 11) is not used in this application.

All capacitors in microfarads, inductors in Henries and resistors in Ohms, unless otherwise specified.

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MOTOROLA

MC2833

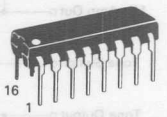
Product Preview

LOW POWER FM TRANSMITTER SYSTEM

MC2833 is a one-chip FM transmitter subsystem designed for cordless telephone and FM communication equipment. It includes a microphone amplifier, voltage controlled oscillator and two auxiliary transistors.

- Wide Range of Operating Supply Voltage (2.8–9.0 V)
- Low Drain Current (I_{CC} = 2.9 mA Typ)
- Low Number of External Parts Required
- −30 dBm Power Output to 60 MHz Using Direct RF Output
- +10 dBm Power Output Attainable Using On-Chip Transistor Amplifiers

LOW POWER FM TRANSMITTER SYSTEM



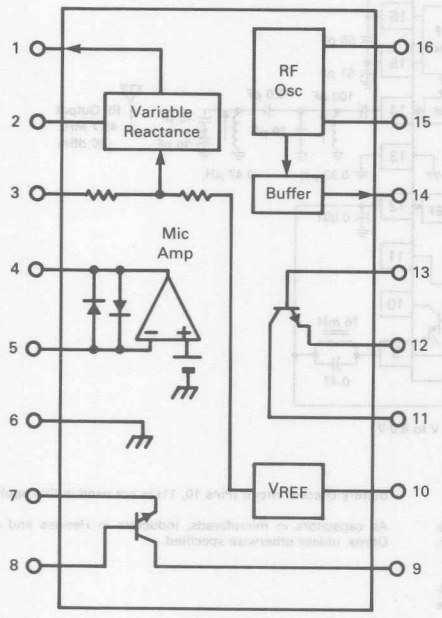
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CASE 648-06



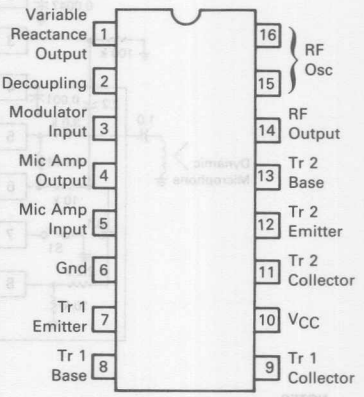
D SUFFIX
PLASTIC PACKAGE
CASE 751B-03
SO-16

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FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENTS



This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MAXIMUM RATINGS

Ratings	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	10 (max)	V
Operating Supply Voltage Range	V_{CC}	2.8–9.0	V
Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_A	−30 to +75	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0 V, T_A = 25°C, unless otherwise noted)

Characteristics	Symbol	Pin	Min	Typ	Max	Unit
Drain Current (No input signal)	I_{CC}	10	1.7	2.9	4.3	mA
FM MODULATOR						
Output RF Voltage (f_o = 16.6 MHz)	V_{out} RF	14	60	90	130	mVrms
Output DC Voltage (No input signal)	Vdc	14	2.2	2.5	2.8	V
Modulation Sensitivity (f_o = 16.6 MHz) (V_{in} = 0.8 V to 1.2 V)	SEN	3.0 14	7.0 —	10 —	15 —	Hz/mVdc
Maximum Deviation (f_o = 16.6 MHz) (V_{in} = 0 V to 2.0 V)	Fdev	3.0 14	3.0 —	5.0 —	10 —	kHz
MIC AMPLIFIER						
Closed Loop Voltage Gain (V_{in} = 3.0 mVrms) (f_{in} = 1.0 kHz)	A_v	4.0 5.0	27 —	30 —	33 —	dB
Output DC Voltage (No input signal)	V_{out} dc	4.0	1.1	1.4	1.7	V
Output Swing Voltage (V_{in} = 30 mVrms) (f_{in} = 1.0 kHz)	V_{out} p-p	4.0	0.8	1.2	1.6	Vp-p
Total Harmonic Distortion (V_{in} = 3.0 mVrms) (f_{in} = 1.0 kHz)	THD	4.0	—	0.15	2.0	%

AUXILIARY TRANSISTOR STATIC CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
Collector Base Breakdown Voltage (I_C = 5.0 μA)	$V_{(BR)CBO}$	15	45	—	V
Collector Emitter Breakdown Voltage (I_C = 200 μA)	$V_{(BR)CEO}$	10	15	—	V
Collector Substrate Breakdown Voltage (I_C = 50 μA)	$V_{(BR)CSO}$	—	70	—	V
Emitter Base Breakdown Voltage (I_E = 50 μA)	$V_{(BR)EBO}$	—	6.2	—	V
Collector Base Cut Off Current (V_{CB} = 10 V) (I_E = 0)	I_{CBO}	—	—	200	nA
DC Current Gain (I_C = 3.0 mA) (V_{CE} = 3.0 V)	h_{FE}	40	150	—	—

AUXILIARY TRANSISTOR DYNAMIC CHARACTERISTICS

Current Gain Bandwidth Product (V_{CE} = 3.0 V) (I_C = 3.0 mA)	f_T	—	500	—	MHz
Collector Base Capacitance (V_{CE} = 3.0 V) (I_C = 0)	C_{CB}	—	2.0	—	pF
Collector Substrate Capacitance (V_{CS} = 3.0 V) (I_C = 0)	C_{CS}	—	3.3	—	pF

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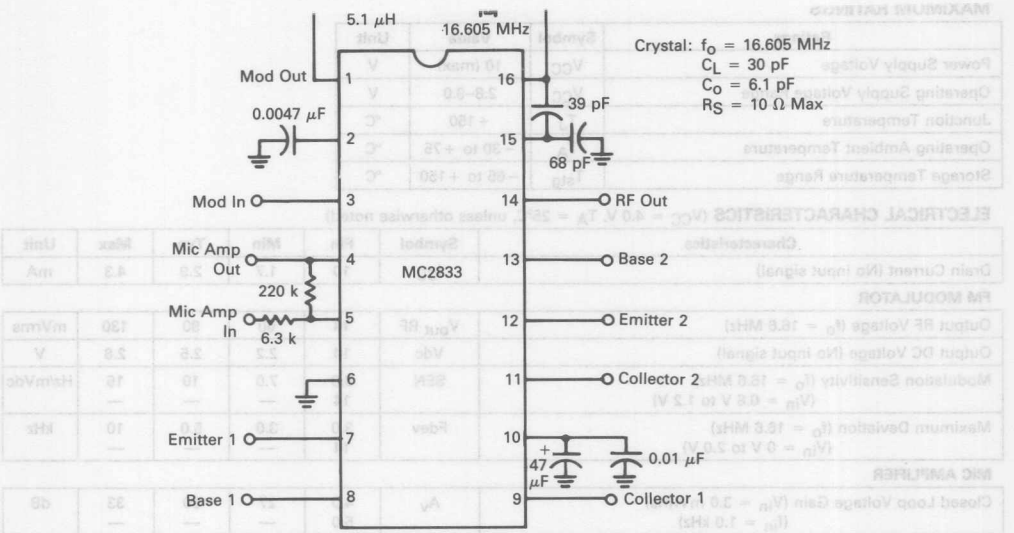
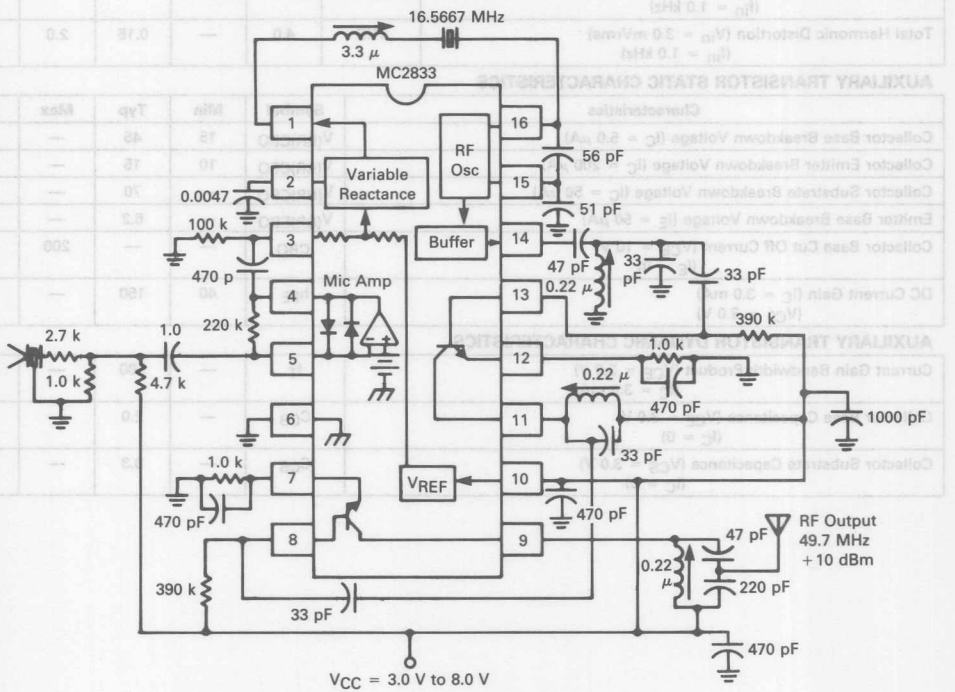


FIGURE 2 — SINGLE CHIP FM VHF TRANSMITTER AT 49.7 MHz



NOTES: The crystal used is fundamental mode, calibrated for parallel resonance with a 32 pF load. The 49.7 MHz output is generated in the output buffer, which is being used as a frequency tripler in this application.
The networks in the output stages provide frequency selectivity and impedance matching at 49.7 MHz.
The RF output is +10 dBm (10 mW into 50 Ω load) at 49.7 MHz, with all harmonics reduced by more than 50 dB.
All capacitors in microfarads, inductors in Henries and resistors in Ohms unless otherwise specified.
0.22 μH inductors are Toko B199SN-T1048Z
3.3 μH inductor is Toko B199KN-T1055Z

MOTOROLA

MC3356

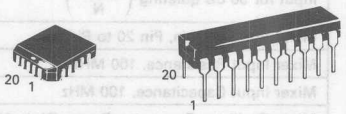
WIDEBAND FSK RECEIVER

. . . includes Oscillator, Mixer, Limiting IF Amplifier, Quadrature Detector, Audio Buffer, Squelch, Meter Drive, Squelch Status output, and Data Shaper comparator. The MC3356 is designed for use in digital data communications equipment.

- Data Rates up to 500 kilobaud
- Excellent Sensitivity: −3 dB Limiting Sensitivity
  30 μVrms @ 100 MHz
- Highly versatile, full-function device, yet few external parts are required

WIDEBAND FSK RECEIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT



FN SUFFIX
PLASTIC PACKAGE
CASE 775-02

P SUFFIX
PLASTIC PACKAGE
CASE 738-03

FIGURE 1 — FUNCTIONAL BLOCK DIAGRAM

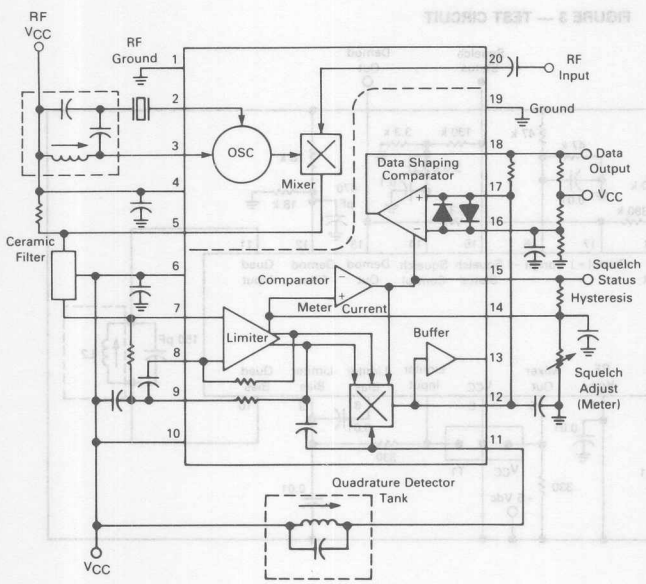
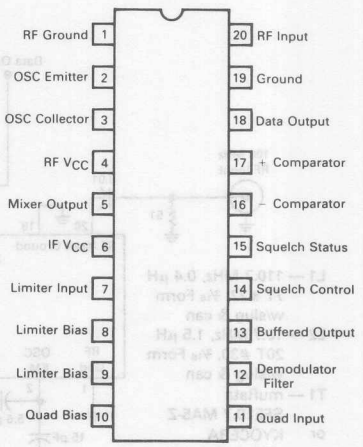


FIGURE 2 — PIN CONNECTIONS



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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC(max)}$	15	Vdc
Operating Power Supply Voltage Range (Pins 6, 10)	V_{CC}	3.0 to 9.0	Vdc
Operating R.F. Supply Voltage Range (Pin 4)	R.F. V_{CC}	3.0 to 12.0	Vdc
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Power Dissipation, Package Rating	P_D	1.25	W

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, f_o = 100 MHz, f_{osc} = 110.7 MHz, Δf = ±75 kHz, f_{mod} = 1.0 kHz, 50 Ω source, T_A = 25°C, test circuit of Figure 3, unless otherwise noted.)

Characteristics	Min	Typ	Max	Unit
Drain Current Total, RF V_{CC} and V_{CC}	—	20	25	mAdc
Input for −3 dB limiting	—	30	—	μVrms
Input for 50 dB quieting $\left(\frac{S+N}{N}\right)$	—	60	—	μVrms
Mixer Voltage Gain, Pin 20 to Pin 5	2.5	—	—	
Mixer Input Resistance, 100 MHz	—	260	—	Ω
Mixer Input Capacitance, 100 MHz	—	5.0	—	pF
Mixer/Oscillator Frequency Range (Note 1)	—	0.2 to 150	—	MHz
IF/Quadrature Detector Frequency Range (Note 1)	—	0.2 to 50	—	MHz
AM Rejection (30% AM, RF V_{in} = 1.0 mVrms)	—	50	—	dB
Demodulator Output, Pin 13	—	0.5	—	Vrms
Meter Drive	—	7.0	—	μA/dB
Squelch Threshold	—	0.8	—	Vdc

Note 1: Not taken in Test Circuit of Figure 3; new component values required.

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FIGURE 3 — TEST CIRCUIT

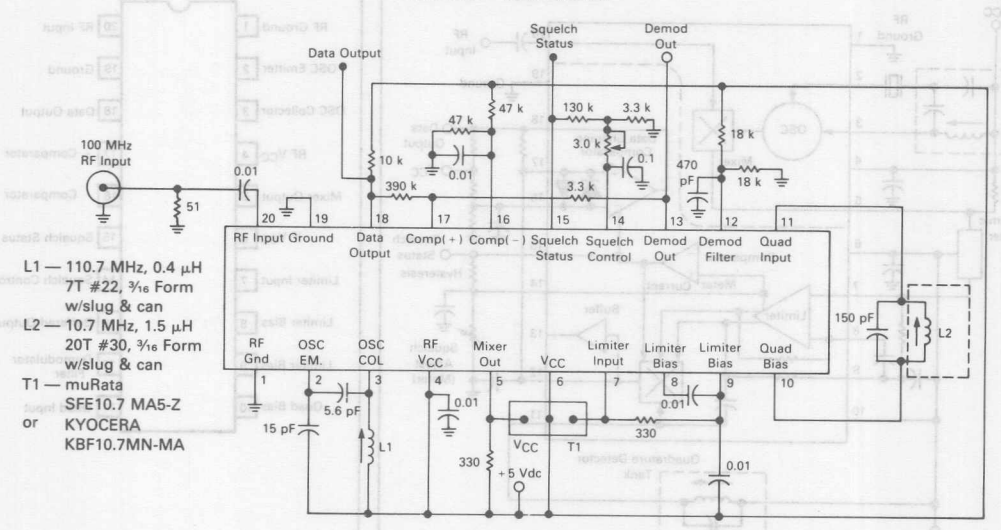


FIGURE 4 — OUTPUT COMPONENTS OF SIGNAL, NOISE, AND DISTORTION

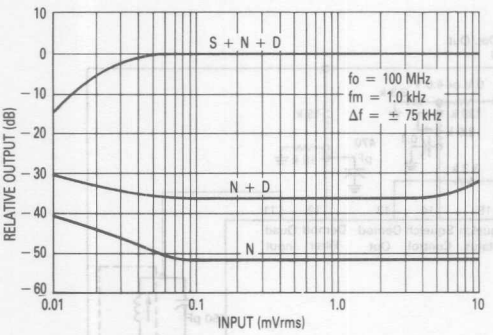
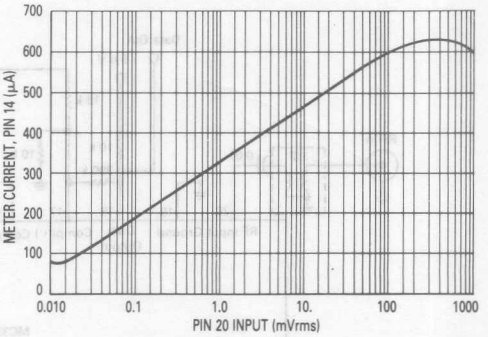


FIGURE 5 — METER CURRENT versus SIGNAL INPUT



GENERAL DESCRIPTION

This device is intended for single and double conversion VHF receiver systems, primarily for FSK data transmission up to 500 K baud (250 kHz). It contains an oscillator, mixer, limiting IF, quadrature detector, signal strength meter drive, and data shaping amplifier.

The oscillator is a common base Colpitts type which can be crystal controlled, as shown in Figure 1, or L-C controlled as shown in the other figures. At higher V_{CC}, it has been operated as high as 200 MHz. A mixer/oscillator voltage gain of 2 up to approximately 150 MHz, is readily achievable.

The mixer functions well from an input signal of 10 μVrms, below which the squelch is unpredictable, up to about 10 mVrms, before any evidence of overload. Operation up to 1.0 Vrms input is permitted, but nonlinearity of the meter output is incurred, and some oscillator pulling is suspected. The AM rejection above 10 mVrms is degraded.

The limiting IF is a high frequency type, capable of being operated up to 50 MHz. It is expected to be used at 10.7 MHz in most cases, due to the availability of standard ceramic resonators. The quadrature detector is internally coupled to the IF, and a 5.0 pF quadrature capacitor is internally provided. The −3dB limiting sensitivity of the IF itself is approximately 50 μV (at Pin 7), and the IF can accept signals up to 1.0 Vrms without distortion or change of detector quiescent dc level.

The IF is unusual in that each of the last 5 stages of the 6 state limiter contains a signal strength sensitive, current sinking device. These are parallel connected and buffered to produce a signal strength meter drive which is fairly linear for IF input signals of 10 μV to 100 mVrms. (See Figure 5.)

A simple squelch arrangement is provided whereby the meter current flowing through the meter load resistance flips a comparator at about 0.8 Vdc above ground. The signal strength at which this occurs can be adjusted by changing the meter load resistor. The comparator(+) input and output are available to permit control of hysteresis. Good positive action can be obtained for IF input signals of above 30 μVrms. The 130 kΩ resistor shown in the test circuit provides a small amount of hysteresis. Its connection between the 3.3 k resistor to ground and the 3.0 k pot, permits adjustment of squelch level without changing the amount of hysteresis.

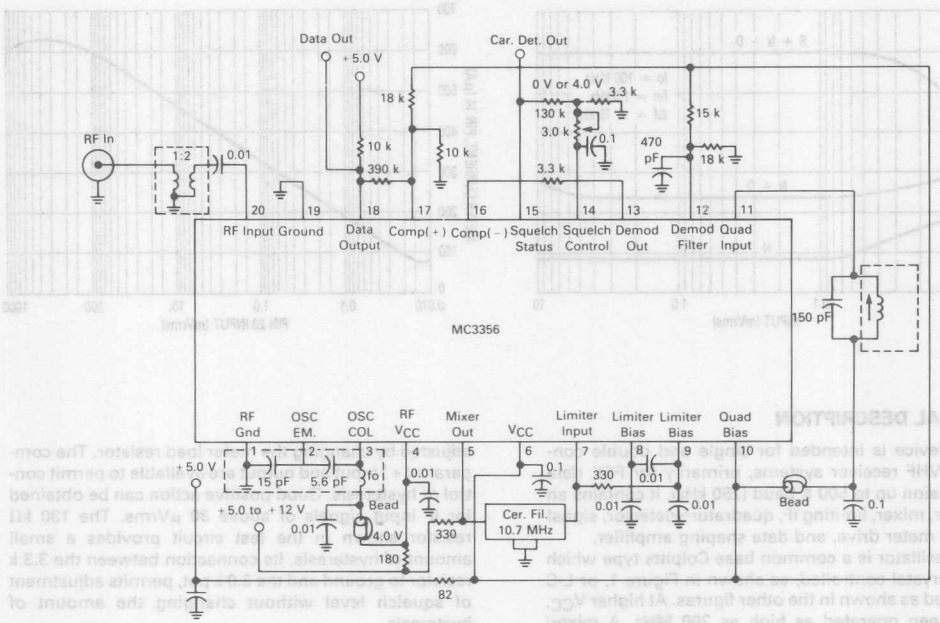
The squelch is internally connected to both the quadrature detector and the data shaper. The quadrature detector output, when squelched, goes to a dc level approximately equal to the zero signal level, unsquelched. The squelch causes the data shaper to produce a high (V_{CC}) output.

The data shaper is a complete "floating" comparator, with back to back diodes across its inputs. The output of the quadrature detector can be fed directly to either input of this amplifier to produce an output that is either at V_{CC} or V_{EE}, depending upon the received frequency. The impedance of the biasing can be varied to produce an amplifier which "follows" frequency detuning to some degree, to prevent data pulse width changes.

When the data shaper is driven directly from the demodulator output, Pin 13, there may be distortion at Pin 13 due to the diodes, but this is not important in the data application. A useful note in relating high/low input frequency to logic state: low IF frequency corresponds to low demodulator output. If the oscillator is above the incoming RF frequency, then high RF frequency will produce a logic low. (Input to (+)input of Data Shaper as shown in figures 1 and 3.)

8

FIGURE 6 — APPLICATION WITH FIXED BIAS ON DATA SHAPER



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APPLICATION NOTES

The MC3356 is a high frequency/high gain receiver that requires following certain layout techniques in designing a stable circuit configuration. The objective is to minimize or eliminate, if possible, any unwanted feedback.

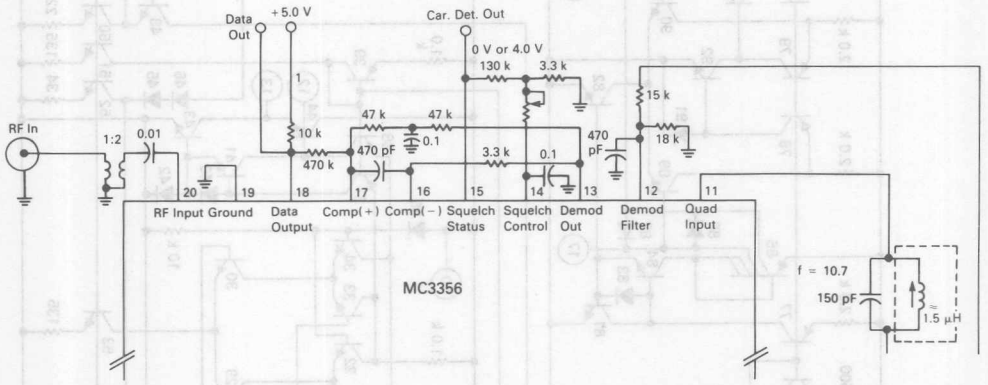
Shielding, which includes the placement of input and output components, is important in minimizing electrostatic or electromagnetic coupling. The MC3356 has its pin connections such that the circuit designer can place the critical input and output circuits on opposite ends of the chip. Shielding is normally required for inductors in tuned circuits.

The MC3356 has separate V_{CC}'s and grounds for the RF and IF sections which allows good external circuit isolation by minimizing common ground paths.

Note that the circuits of figures 1 and 3 have RF, oscillator, and IF circuits predominantly referenced to the plus supply rails. Figure 6, on the other hand, shows a suitable means of ground referencing. The two methods produce identical results when carefully executed. It is important to treat Pin 19 as a ground node for either approach. The RF input should be "grounded" to Pin 1 and then the input and the mixer/oscillator grounds (or RF V_{CC} bypasses) should be connected by a low inductance path to Pin 19. IF and detector sections should also have their bypasses returned by a *separate* path to Pin 19. V_{CC} and RF V_{CC} can be decoupled to minimize feedback, although the configuration of Figure 3 shows a successful implementation on a common 5.0 supply. Once again, the message is: define a supply node and a ground node and return each section to those nodes by separate, low impedance paths.

The test circuit of Figure 3 has a 3 db limiting level of 30 μV which can be lowered 6 db by a 1:2 untuned transformer at the input as shown in figures 6 and 7. For applications that require additional sensitivity, an RF amplifier can be added, but with no greater than 20 db gain. This will give a 2.0 to 2.5 μV sensitivity and any additional gain will reduce receiver dynamic range without improving its sensitivity. Although the test circuit operates at +5.0 V, the mixer/oscillator optimum performance is at +8.0 V to 12 V. A minimum of +8.0 V is recommended in high frequency applications (above 150 MHz), or in PLL applications where the oscillator drives a prescaler.

FIGURE 7 — APPLICATION WITH SELF-ADJUSTING BIAS ON DATA SHAPER



APPLICATION NOTES (continued)

Depending on the external circuit, inverted or non-inverted data is available at Pin 18. Inverted data makes the higher frequency in the FSK signal a 'one' when the local oscillator is above the incoming RF. Figure 6 schematic shows the comparator with hysteresis. In this circuit the dc reference voltage at Pin 17 is about the same as the demodulated output voltage (Pin 13) when no signal is present. This type circuit is preferred for systems where the data rates can drop to zero. Some systems have a low frequency limit on the data rate, such as systems using the MC3850 ACIA that has a start or stop bit. This defines the low frequency limit that can appear in the data stream. Figure 6 circuit can then be changed to a circuit configuration as shown in Figure 7. In Figure 7 the reference voltage for the comparator is derived from the demodulator output through a low pass circuit where τ is much lower than the lowest frequency data rate. This and similar circuits will compensate for small tuning changes (or drift) in the quadrature detector.

Squelch status (Pin 15) goes high (squelch off) when the input signal becomes greater than some preset level set by the resistance between Pin 14 and ground. Hysteresis is added to the circuit externally by the resistance from Pin 14 to Pin 15.

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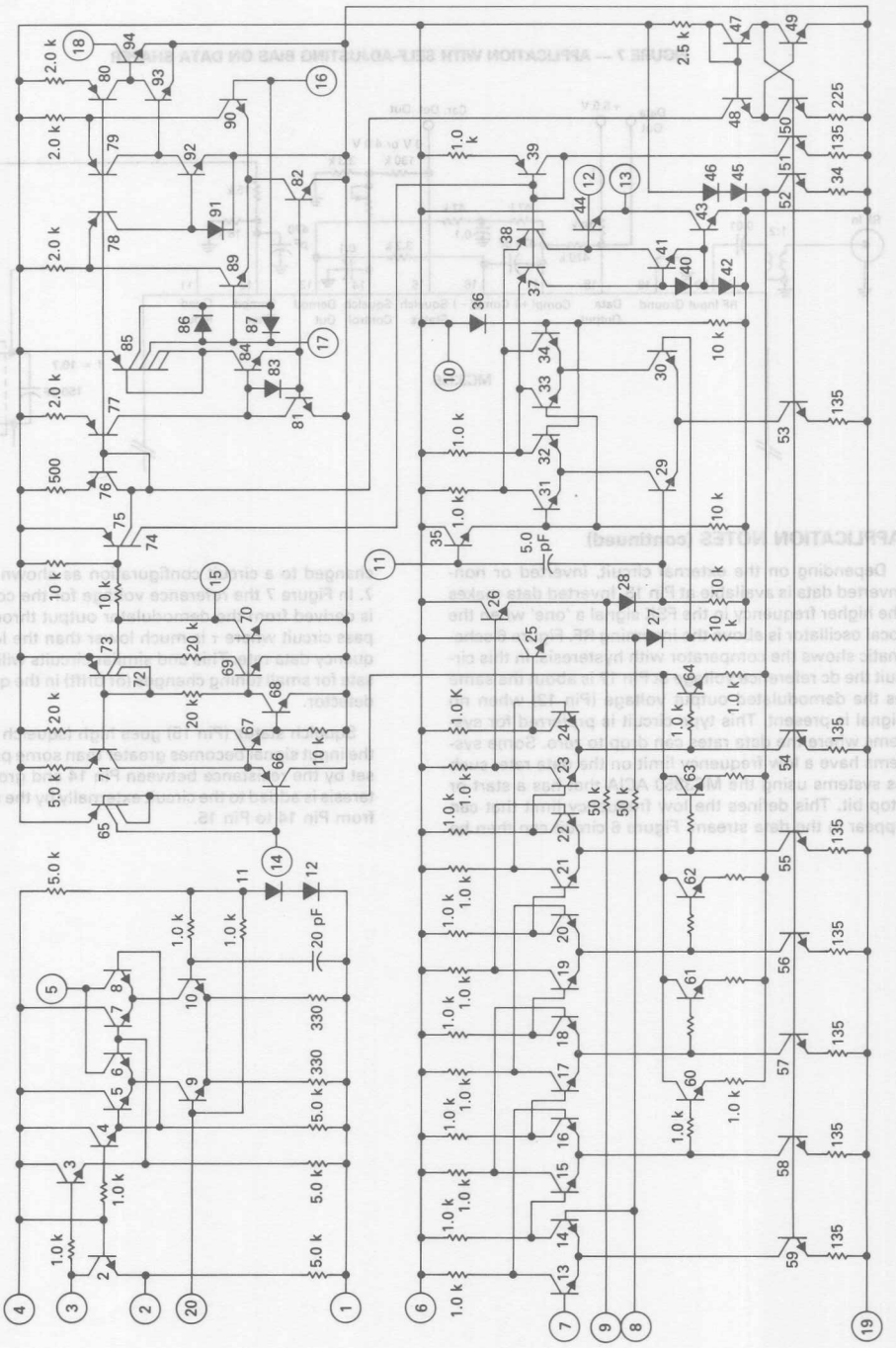


FIGURE 8— INTERNAL SCHEMATIC

MOTOROLA

MC3357

Advance Information

LOW POWER NARROWBAND FM IF

. . . includes Oscillator, Mixer, Limiting Amplifier, Quadrature Discriminator, Active Filter, Squelch, Scan Control, and Mute Switch. The MC3357 is designed for use in FM dual conversion communications equipment.

- Low Drain Current (3.0 mA (Typ) @ V_{CC} = 6.0 Vdc)
- Excellent Sensitivity: Input Limiting Voltage — (-3.0 dB) = 5.0 μV (Typ)
- Low Number of External Parts Required

LOW POWER FM IF

SILICON MONOLITHIC INTEGRATED CIRCUIT



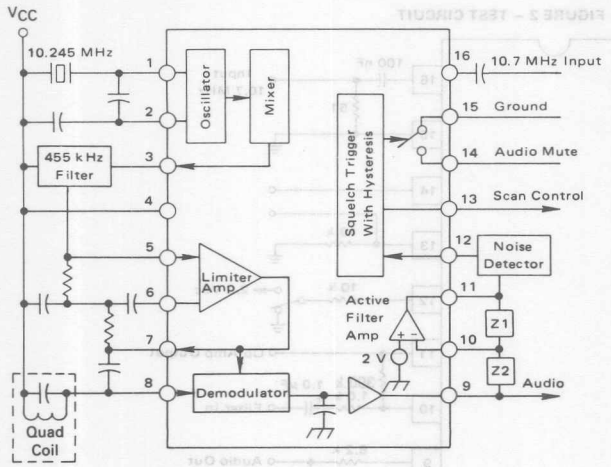
P SUFFIX
PLASTIC PACKAGE
CASE 648-06



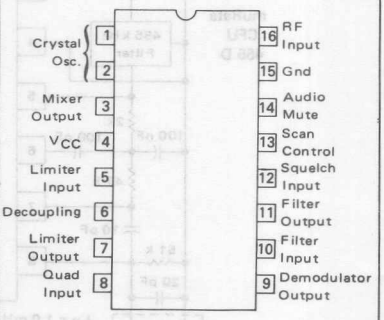
D SUFFIX
PLASTIC PACKAGE
CASE 751B-03
SO-16

8

FIGURE 1 — FUNCTIONAL BLOCK DIAGRAM



PIN CONNECTIONS



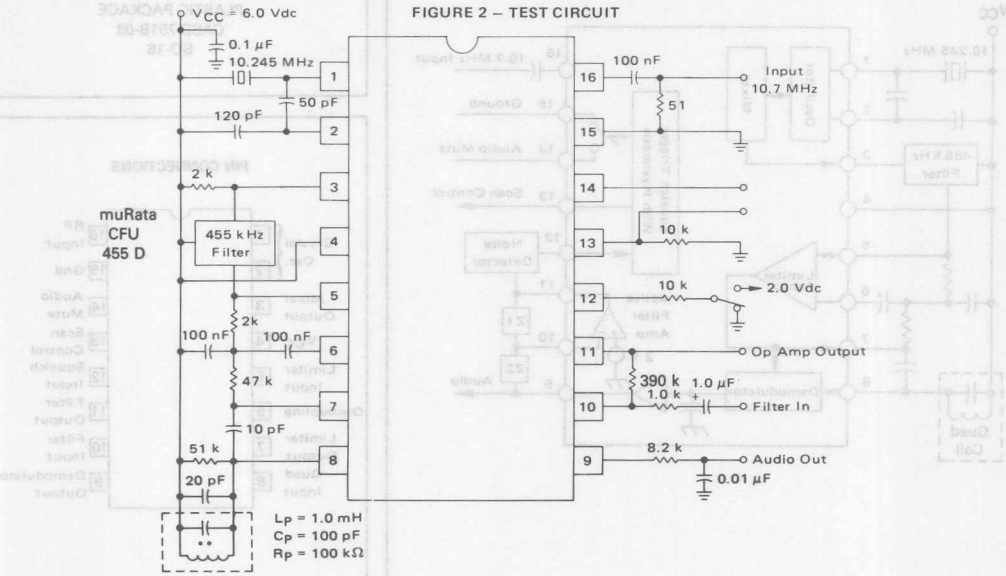
This document contains information on a new product. Specifications and information herein are subject to change without notice.

Power Supply Voltage	4	V_{CC}(max)	12	Vdc
Operating Supply Voltage Range	4	V_{CC}	4 to 8	Vdc
Detector Input Voltage	8	–	1.0	Vp-p
Input Voltage ($V_{CC} \geq$ 6.0 Volts)	16	V_{16}	1.0	V_{RMS}
Mute Function	14	V_{14}	-0.5 to 5.0	V_{pk}
Junction Temperature	–	T_J	150	°C
Operating Ambient Temperature Range	–	T_A	-30 to +70	°C
Storage Temperature Range	–	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 6.0 Vdc, fo = 10.7 MHz, Δf = ± 3.0 kHz, f_{mod} = 1.0 kHz, T_A = 25°C unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
Drain Current Squelch Off Squelch On	4	– –	2.0 3.0	– 5.0	mA
Input Limiting Voltage (-3 dB Limiting)	16	–	5.0	10	μV
Detector Output Voltage	9	–	3.0	–	Vdc
Detector Output Impedance	–	–	400	–	Ω
Recovered Audio Output Voltage (V_{in} = 10 mV)	9	200	350	–	mVrms
Filter Gain (10 kHz) (V_{in} = 5 mV)	–	40	46	–	dB
Filter Output Voltage	11	1.8	2.0	2.5	Vdc
Trigger Hysteresis	–	–	100	–	mV
Mute Function Low	14	–	15	50	Ω
Mute Function High	14	1.0	10	–	MΩ
Scan Function Low (Mute Off) (V_{12} = 2 Vdc)	13	–	0	0.5	Vdc
Scan Function High (Mute On) (V_{12} = Gnd)	13	5.0	–	–	Vdc
Mixer Conversion Gain	3	–	20	–	dB
Mixer Input Resistance	16	–	3.3	–	kΩ
Mixer Input Capacitance	16	–	2.2	–	pF

FIGURE 2 – TEST CIRCUIT



CIRCUIT DESCRIPTION

The MC3357 is a low power FM IF circuit designed primarily for use in voice communication scanning receivers.

The mixer-oscillator combination converts the input frequency (e.g., 10.7 MHz) down to 455 kHz, where, after external bandpass filtering, most of the amplification is done. The audio is recovered using a conventional quadrature FM detector. The absence of an input signal is indicated by the presence of noise above the desired audio frequencies. This "noise band" is monitored by an active filter and a detector. A squelch trigger circuit indicates the presence of noise (or a tone) by an output which can be used to control scanning. At the same time, an internal switch is operated which can be used to mute the audio.

The oscillator is an internally-biased Colpitts type with the collector, base, and emitter connections at Pins 4, 1, and 2 respectively. A crystal can be used in place of the usual coil.

The mixer is doubly-balanced to reduce spurious responses. The input impedance at Pin 16 is set by a 3.0 kΩ internal biasing resistor and has low capacitance, allowing the circuit to be preceded by a crystal filter. The collector output at Pin 3 must be dc connected to B+, below which it can swing 0.5 V.

After suitable bandpass filtering (ceramic or LC) the signal goes to the input of a five-stage limiter at Pin 5. The output of the limiter at Pin 7 drives a multiplier, both internally directly, and externally through a quadrature coil, to detect the FM. The output at Pin 7 is also used to supply dc feedback to Pin 5. The other side of the first limiter stage is decoupled at Pin 6.

The recovered audio is partially filtered, then buffered giving an impedance of around 400 Ω at Pin 9. The signal still requires de-emphasis, volume control and further amplification before driving a loudspeaker.

A simple inverting op amp is provided with an output at Pin 11 providing dc bias (externally) to the input at Pin 10 which is referred internally to 2.0 V. A filter can be made with external impedance elements to discriminate between frequencies. With an external AM detector the filtered audio signal can be checked for the presence of noise above the normal audio band, or a tone signal. This information is applied to Pin 12.

An external positive bias to Pin 12 sets up the squelch trigger circuit such that Pin 13 is low at an impedance level of around 60 kΩ, and the audio mute (Pin 14) is open circuit. If Pin 12 is pulled down to 0.7 V by the noise or tone detector, Pin 13 will rise to approximately 0.5 Vdc below supply where it can support a load current of around 500 μA and Pin 14 is internally short-circuited to ground. There is 100 mV of hysteresis at Pin 12 to prevent jitter. Audio muting is accomplished by connecting Pin 14 to a high-impedance ground-reference point in the audio path between Pin 9 and the audio amplifier.

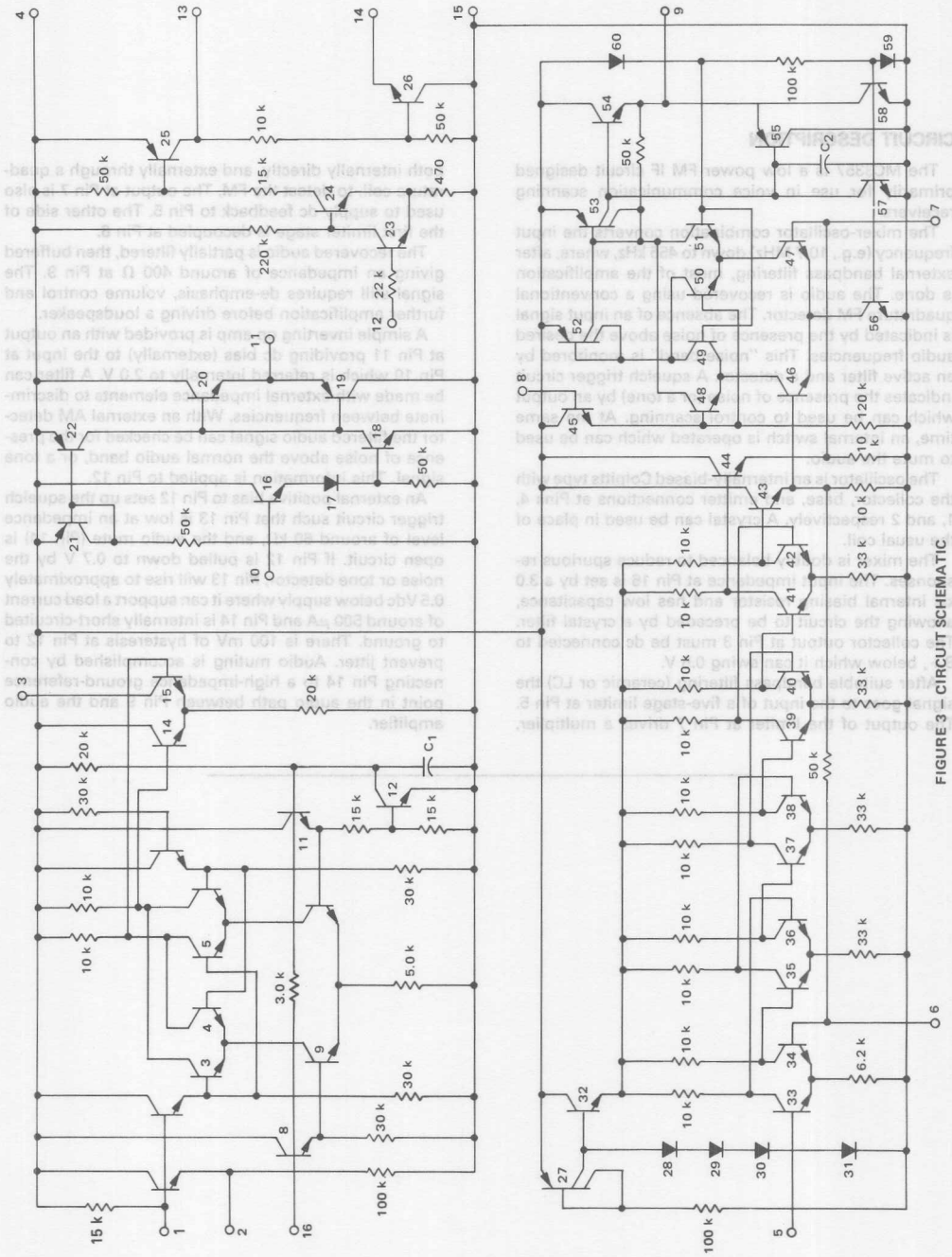


FIGURE 3 – CIRCUIT SCHEMATIC

MOTOROLA

MC3359

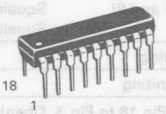
LOW POWER NARROWBAND FM IF

. . . includes oscillator, mixer, limiting amplifier, AFC, quadrature discriminator, op/amp, squelch, scan control, and mute switch. The MC3359 is designed to detect narrowband FM signals using a 455 kHz ceramic filter for use in FM dual conversion communications equipment. The MC3359 is similar to the MC3357 except that the MC3359 has an additional limiting IF stage, an AFC output, and an opposite polarity Broadcast Detector. The MC3359 also requires fewer external parts.

- Low Drain Current: 3.6 mA (Typ) @ V_{CC} = 6.0 Vdc
- Excellent Sensitivity: Input Limiting Voltage — −3.0 dB = 2.0 μV (Typ)
- Low Number of External Parts Required

HIGH GAIN LOW POWER FM IF

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 707-02



DW SUFFIX
PLASTIC PACKAGE
CASE 751D-03
SO-20L

FIGURE 1 — TYPICAL APPLICATION IN A SCANNER RECEIVER

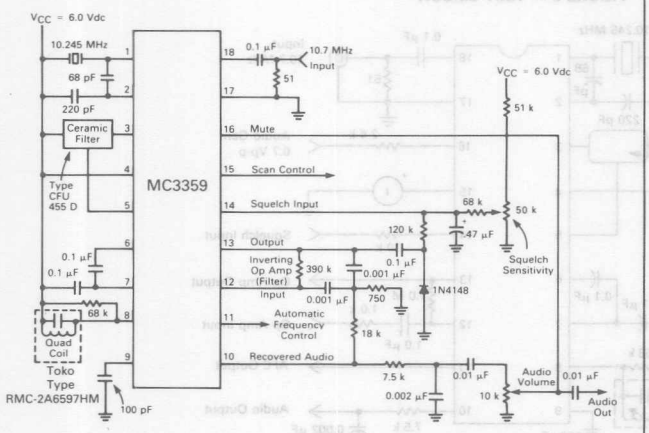
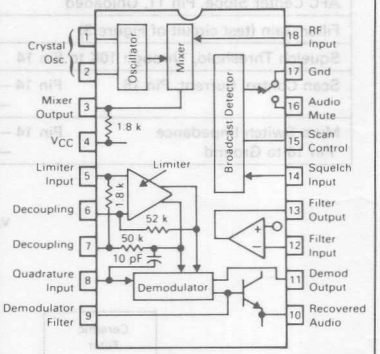
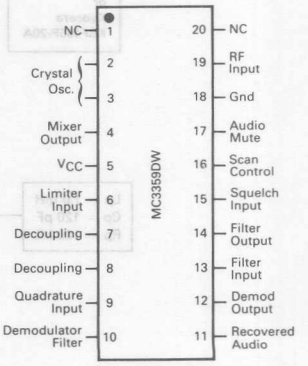


FIGURE 2 — PIN CONNECTIONS AND FUNCTIONAL BLOCK DIAGRAM



CASE 707-02



CASE 751D-03

8

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4	V_{CC}(max)	12	Vdc
Operating Supply Voltage Range	4	V_{CC}	4 to 9	Vdc
Input Voltage ($V_{CC} \geq$ 6.0 Volts)	18	V_{18}	1.0	V_{rms}
Mute Function	16	V_{16}	−0.7 to 12	V_{pk}
Junction Temperature	—	T_J	150	°C
Operating Ambient Temperature Range	—	T_A	−30 to +70	°C
Storage Temperature Range	—	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 6.0 Vdc, f_o = 10.7 MHz, Δf = ±3.0 kHz, f_{mod} = 1.0 kHz, 50 Ω source, T_A = 25°C test circuit of Figure 3, unless otherwise noted)

Characteristics		Min	Typ	Max	Units
Drain Current (Pins 4 and 8)	Squelch Off	—	3.6	6.0	mA
	Squelch On	—	5.4	7.0	
Input for 20 dB Quieting		—	8.0	—	μVrms
Input for −3.0 dB Limiting		—	2.0	—	μVrms
Mixer Voltage Gain (Pin 18 to Pin 3, Open)		—	46	—	
Mixer Third Order Intercept, 50 Ω Input		—	−1.0	—	dBm
Mixer Input Resistance		—	3.6	—	kΩ
Mixer Input Capacitance		—	2.2	—	pF
Recovered Audio, Pin 10 (Input Signal 1.0 mVrms)		450	700	—	mVrms
Detector Center Frequency Slope, Pin 10		—	0.3	—	V/kHz
AFC Center Slope, Pin 11, Unloaded		—	12	—	V/kHz
Filter Gain (test circuit of Figure 3)		40	51	—	dB
Squelch Threshold, Through 10K to Pin 14		—	0.62	—	Vdc
Scan Control Current, Pin 15	Pin 14 — High	—	0.01	1.0	μA
	— Low	2.0	2.4	—	mA
Mute Switch Impedance Pin 16 to Ground	Pin 14 — High	—	5.0	10	Ω
	— Low		1.5	—	MΩ

FIGURE 3 — TEST CIRCUIT

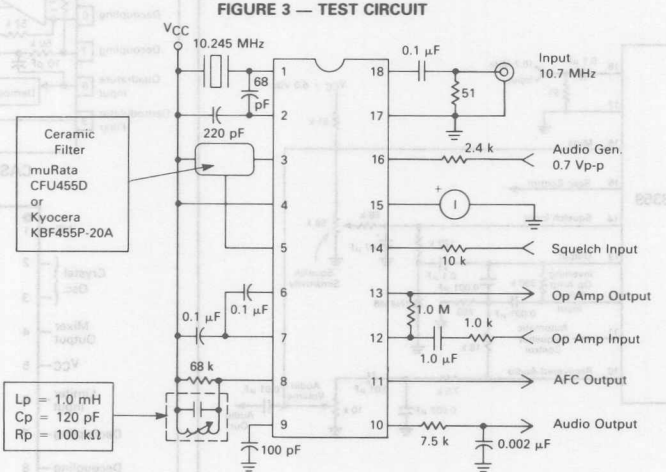


FIGURE 4 — MIXER VOLTAGE GAIN

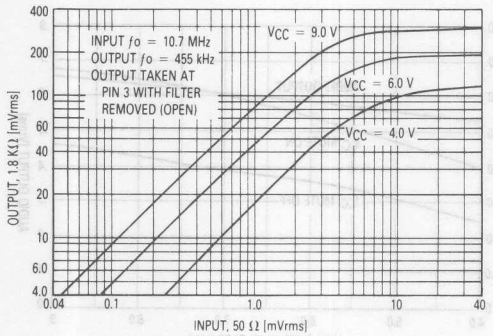


FIGURE 5 — LIMITING I.F. FREQUENCY RESPONSE

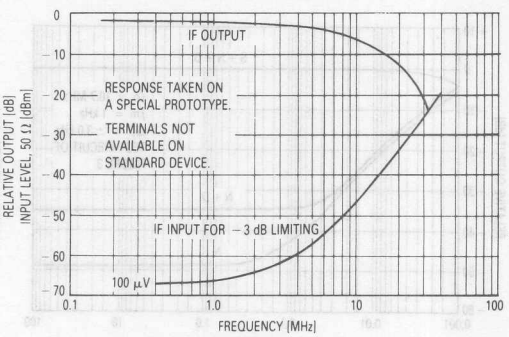


FIGURE 6 — MIXER THIRD ORDER INTERMODULATION PERFORMANCE

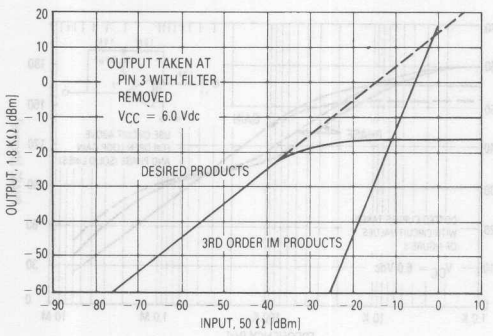


FIGURE 7 — DETECTOR AND AFC RESPONSES

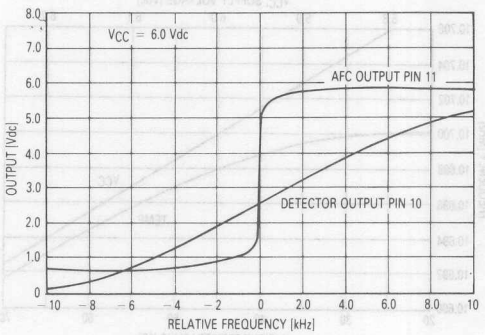


FIGURE 8 — RELATIVE MIXER GAIN

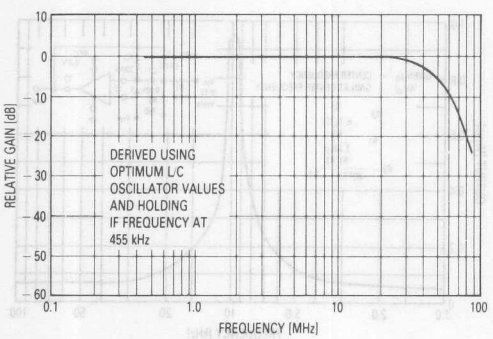
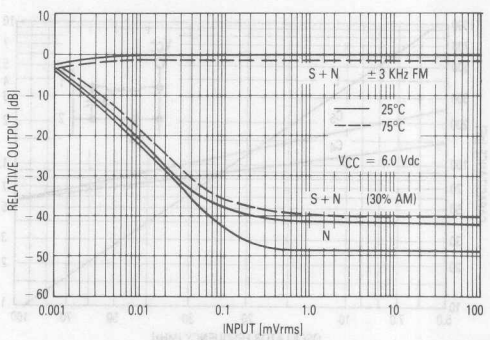


FIGURE 9 — OVERALL GAIN, NOISE, AND A.M. REJECTION



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FIGURE 10 — OUTPUT COMPONENTS OF SIGNAL, NOISE, AND DISTORTION

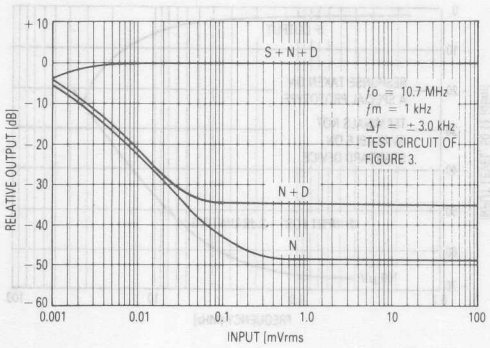


FIGURE 11 — AUDIO OUTPUT AND TOTAL CURRENT DRAIN versus SUPPLY VOLTAGE

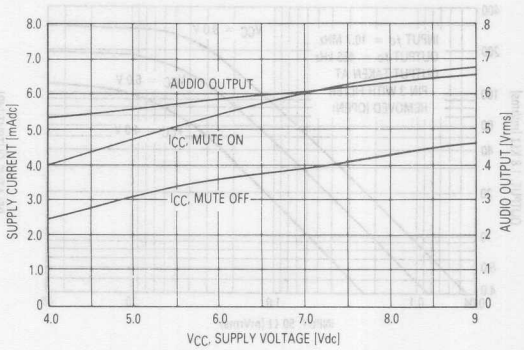


FIGURE 12 — L/C OSCILLATOR, TEMPERATURE AND POWER SUPPLY SENSITIVITY

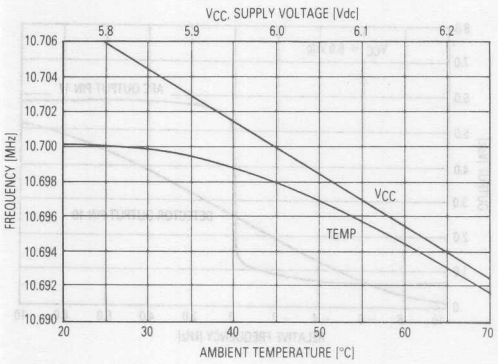


FIGURE 13 — OP AMP GAIN AND PHASE RESPONSE

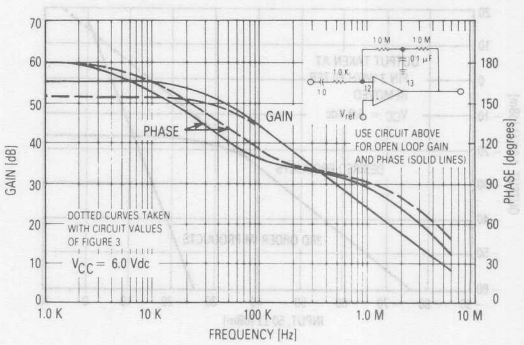


FIGURE 14 — L/C OSCILLATOR RECOMMENDED COMPONENT VALUES

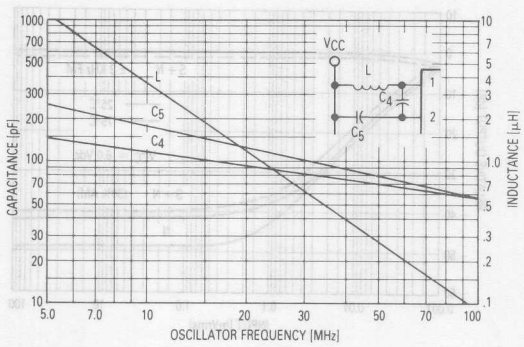
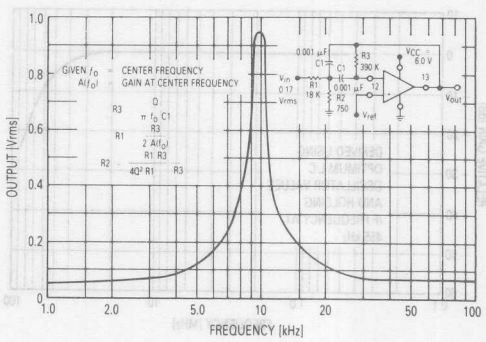


FIGURE 15 — THE OP AMP AS A BANDPASS FILTER



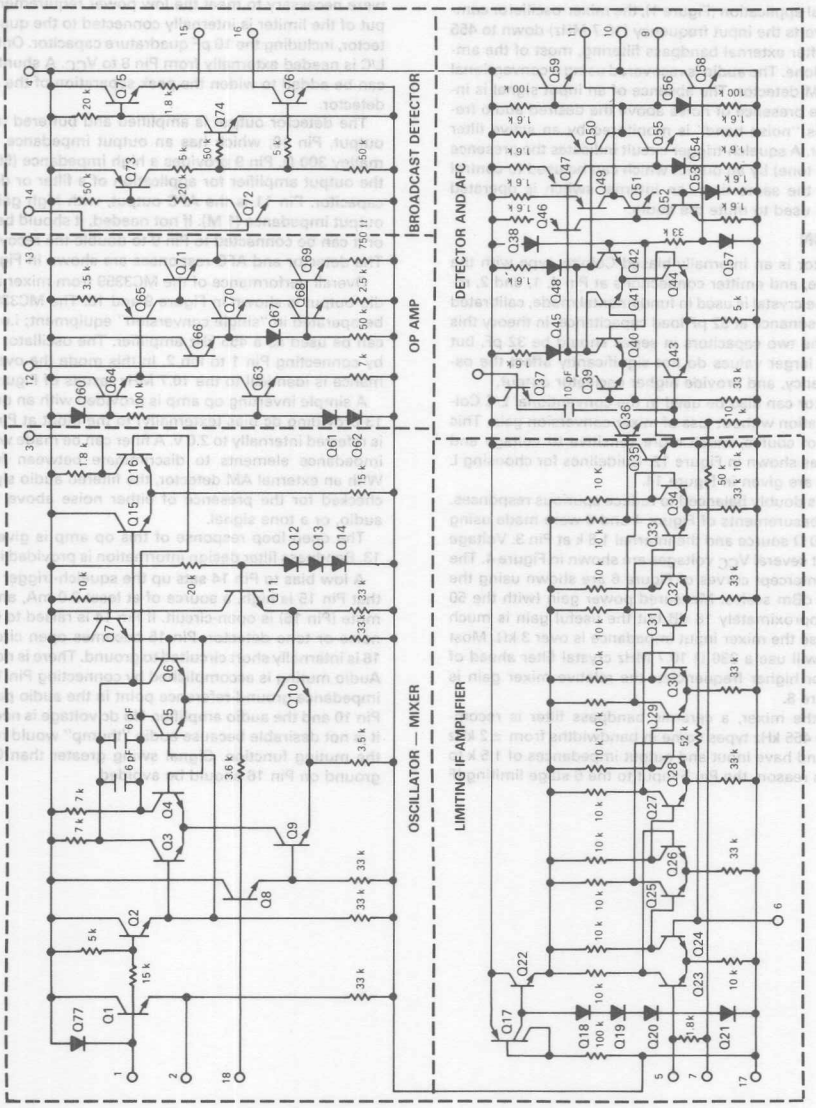


FIGURE 16 — CIRCUIT SCHEMATIC

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CIRCUIT DESCRIPTION

The MC3359 is a low-power FM IF circuit designed primarily for use in voice-communication scanning receivers. It is also finding a place in narrowband data links.

In the typical application (Figure 1), the mixer-oscillator combination converts the input frequency (10.7 MHz) down to 455 kHz, where, after external bandpass filtering, most of the amplification is done. The audio is recovered using a conventional quadrature FM detector. The absence of an input signal is indicated by the presence of noise above the desired audio frequencies. This "noise band" is monitored by an active filter and a detector. A squelch-trigger circuit indicates the presence of noise (or a tone) by an output which can be used to control scanning. At the same time, an internal switch is operated which can be used to mute the audio.

APPLICATION

The oscillator is an internally biased Colpitts type with the collector, base, and emitter connections at Pin 4, 1, and 2, respectively. The crystal is used in fundamental mode, calibrated for parallel resonance at 32 pF load capacitance. In theory this means that the two capacitors in series should be 32 pF, but in fact much larger values do not significantly affect the oscillator frequency, and provide higher oscillator output.

The oscillator can also be used in the conventional L/C Colpitts configuration without loss of mixer conversion gain. This oscillator is, of course, much more sensitive to voltage and temperature as shown in Figure 12. Guidelines for choosing L and C values are given in Figure 14.

The mixer is doubly balanced to reduce spurious responses. The mixer measurements of Figure 4 and 6 were made using an external 50 Ω source and the internal 1.8 k at Pin 3. Voltage gain curves at several V_{CC} voltages are shown in Figure 4. The Third Order Intercept curves of Figure 6 are shown using the conventional dBm scales. Measured power gain (with the 50 Ω input) is approximately 18 dB but the useful gain is much higher because the mixer input impedance is over 3 kΩ. Most applications will use a 330 Ω 10.7 MHz crystal filter ahead of the mixer. For higher frequencies, the relative mixer gain is given in Figure 8.

Following the mixer, a ceramic bandpass filter is recommended. The 455 kHz types come in bandwidths from ±2 kHz to ±15 kHz and have input and output impedances of 1.5 k to 2.0 k. For this reason, the Pin 5 input to the 6 stage limiting IF has an internal 1.8 k resistor. The IF has a 3 dB limiting sensitivity of approximately 100 μV at Pin 5 and a useful frequency range of about 5 MHz as shown in Figure 5. The frequency limitation is due to the high resistance values in the IF, which were necessary to meet the low power requirement. The output of the limiter is internally connected to the quadrature detector, including the 10 pF quadrature capacitor. Only a parallel L/C is needed externally from Pin 8 to V_{CC}. A shunt resistance can be added to widen the peak separation of the quadrature detector.

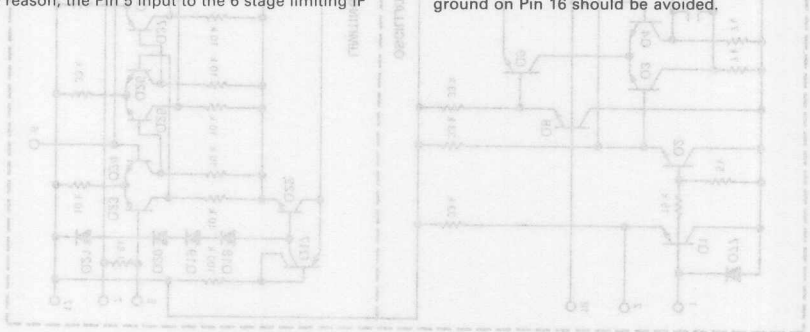
The detector output is amplified and buffered to the audio output, Pin 10, which has an output impedance of approximatley 300 Ω. Pin 9 provides a high impedance (50 k) point in the output amplifier for application of a filter or de-emphasis capacitor. Pin 11 is the AFC output, with high gain and high output impedance (1 M). If not needed, it should be grounded, or it can be connected to Pin 9 to double the recovered audio. The detector and AFC responses are shown in Figure 7.

Overall performance of the MC3359 from mixer input to audio output is shown in Figure 9 and 10. The MC3359 can also be operated in "single conversion" equipment; i.e., the mixer can be used as a 455 kHz amplifier. The oscillator is disabled by connecting Pin 1 to Pin 2. In this mode the overall performance is identical to the 10.7 MHz results of Figure 9.

A simple inverting op amp is provided with an output at Pin 13 providing dc bias (externally) to the input at Pin 12, which is referred internally to 2.0 V. A filter can be made with external impedance elements to discriminate between frequencies. With an external AM detector, the filtered audio signal can be checked for the presence of either noise above the normal audio, or a tone signal.

The open loop response of this op amp is given in Figure 13. Bandpass filter design information is provided in Figure 15.

A low bias to Pin 14 sets up the squelch-trigger circuit such that Pin 15 is high, a source of at least 2.0 mA, and the audio mute (Pin 16) is open-circuit. If Pin 14 is raised to 0.7 V by the noise or tone detector, Pin 15 becomes open circuit and Pin 16 is internally short circuited to ground. There is no hysteresis. Audio muting is accomplished by connecting Pin 16 to a high-impedance ground-reference point in the audio path between Pin 10 and the audio amplifier. No dc voltage is needed, in fact it is not desirable because audio "thump" would result during the muting function. Signal swing greater than 0.7 V below ground on Pin 16 should be avoided.



MOTOROLA

MC3361

Advance Information

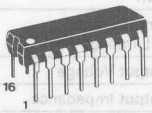
LOW POWER NARROWBAND FM IF

. . . includes Ocillator, Mixer, Limiting Amplifier, Quadrature Discriminator, Active Filter, Squelch, Scan Control, and Mute Switch. The MC3361 is designed for use in FM dual conversion communications equipment.

- Operates From 1.8 V to 7.0 V
- Low Drain Current 4.0 mA Typ @ V_{CC} = 4.0 Vdc
- Excellent Sensitivity: Input Limiting Voltage — −3.0 dB = 2.0 μV Typ
- Low Number of External Parts Required

LOW POWER FM IF

SILICON MONOLITHIC INTEGRATED CIRCUIT



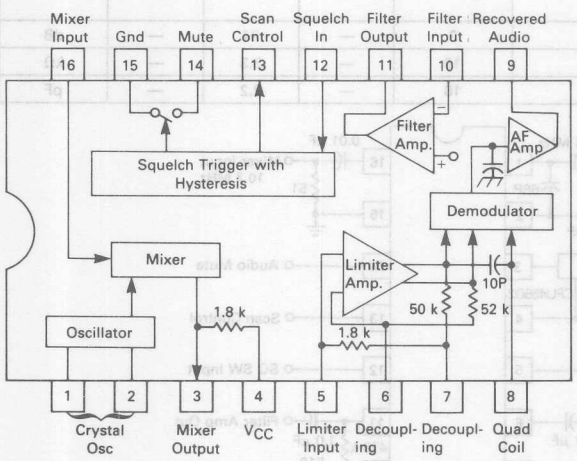
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PLASTIC PACKAGE
CASE 648-06



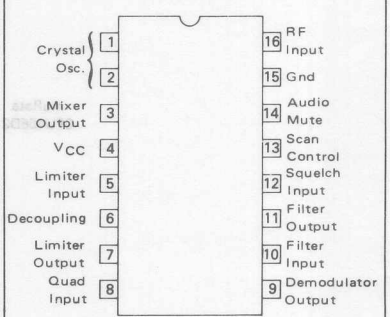
D SUFFIX
PLASTIC PACKAGE
CASE 751B-03
SO-16

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FIGURE 1 — FUNCTIONAL BLOCK DIAGRAM



PIN CONNECTIONS



This document contains information on a new product. Specifications and information herein are subject to change without notice.

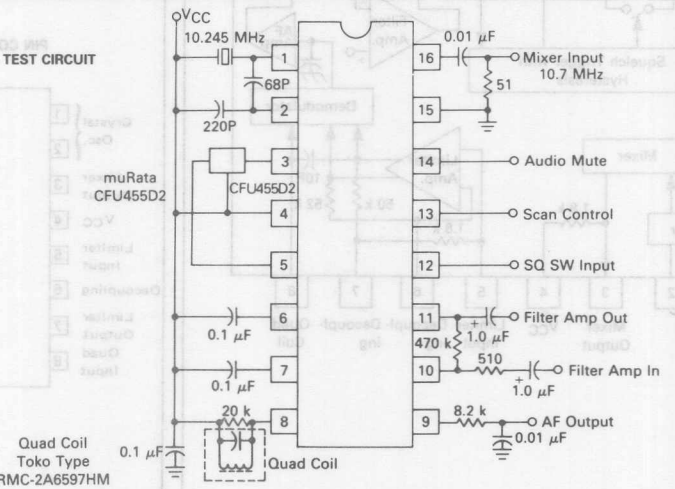
MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4	V_{CC}(max)	8.0	Vdc
Operating Supply Voltage Range	4	V_{CC}	1.8 to 7.0	Vdc
Detector Input Voltage	8	—	1.0	Vp-p
Input Voltage (V_{CC} ≥ 4.0 Volts)	16	V_{16}	1.0	V_{RMS}
Mute Function	14	V_{14}	−0.5 to 5.0	V_{pk}
Junction Temperature	—	T_J	150	°C
Operating Ambient Temperature Range	—	T_A	−30 to +70	°C
Storage Temperature Range	—	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0 Vdc, fo = 10.7 MHz, Δf = ±3.0 kHz, f_{mod} = 1.0 kHz, T_A = 25°C unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
Drain Current	4				mA
Squelch Off		—	4.0	—	
Squelch On		—	6.0	—	
Input Limiting Voltage (−3.0 dB Limiting)	16	—	2.0	—	μV
Detector Output Voltage	9	—	2.0	—	Vdc
Detector Output Impedance	—	—	400	—	Ω
Recovered Audio Output Voltage (V_{in} = 10 mV)	9	100	150	—	mVrms
Filter Gain (10 kHz) (V_{in} = 5.0 mV)	—	40	48	—	dB
Filter Output Voltage	11	—	1.5	—	Vdc
Trigger Hysteresis	—	—	50		mV
Mute Function Low	14	—	10	—	Ω
Mute Function High	14	—	10	—	MΩ
Scan Function Low (Mute Off) (V_{12} = 2.0 Vdc)	13	—	—	0.5	Vdc
Scan Function High (Mute On) (V_{12} = Gnd)	13	3.0	—	—	Vdc
Mixer Conversion Gain	3	—	24	—	dB
Mixer Input Resistance	16	—	3.3	—	kΩ
Mixer Input Capacitance	16	—	2.2	—	pF

FIGURE 2 — TEST CIRCUIT



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MOTOROLA

MC3362

Advance Information

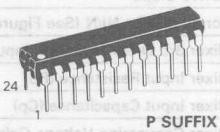
LOW POWER NARROWBAND FM RECEIVER

. . . includes dual FM conversion with oscillators, mixers, quadrature detector, and meter drive/carrier detect circuitry. The MC3362 also has buffered first and second local oscillator outputs and a comparator circuit for FSK detection.

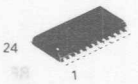
- Wide Input Bandwidth:
  - — 200 MHz using Internal Local Oscillator
  - — 450 MHz using External Local Oscillator
- Complete Dual Conversion Circuitry
- Low Voltage: V_{CC} = 2.0 to 7.0 Vdc
- Low Drain Current (3.6 mA (Typ) @ V_{CC} = 3.0 Vdc)
- Excellent Sensitivity: Input 0.7 μV (Typ) for 12 dB SINAD
- Data Shaping Comparator
- Received Signal Strength Indicator (RSSI) with 60 dB Dynamic Range
- Low Number of External Parts Required
- Manufactured in Motorola's MOSAIC Process Technology

LOW POWER DUAL CONVERSION FM RECEIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 724-02



DW SUFFIX
PLASTIC PACKAGE
CASE 751E-02
SO-24

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FIGURE 1 — TYPICAL APPLICATION IN A PLL FREQUENCY SYNTHESIZED RECEIVER

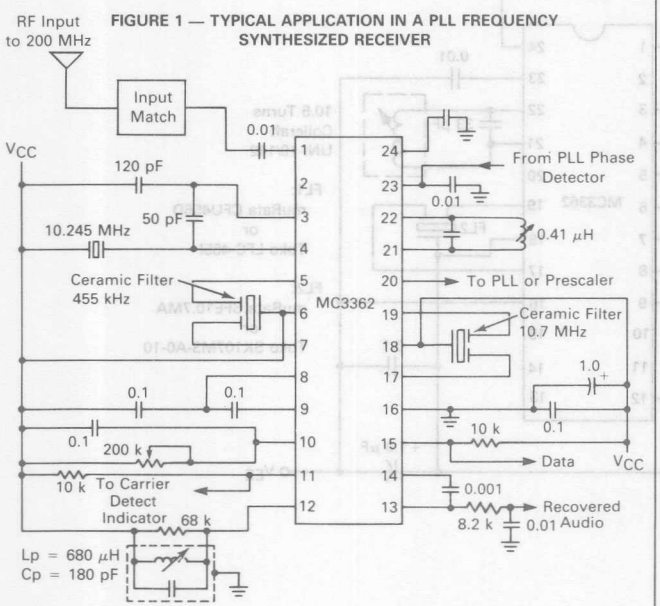
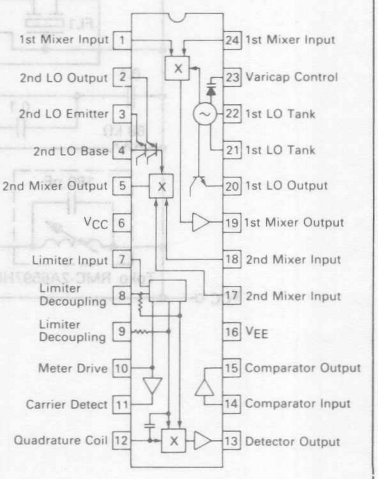


FIGURE 2 — PIN CONNECTIONS AND FUNCTIONAL BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	6	$V_{CC(max)}$	8.0	Vdc
Operating Supply Voltage Range (Recommended)	6	V_{CC}	2.0 to 7.0	Vdc
Input Voltage ($V_{CC} \geq$ 5.0 Vdc)	1, 24	V_{1-24}	1.0	Vrms
Junction Temperature	—	T_J	150	°C
Operating Ambient Temperature Range	—	T_A	−40 to +85	°C
Storage Temperature Range	—	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, f_o = 49.7 MHz, Deviation = 3.0 kHz, T_A = 25°C, Test Circuit of Figure 3 unless otherwise noted)

Characteristic	Pin	Min	Typ	Max	Units
Drain Current (Carrier Detect Low — See Figure 5)	6	—	4.5	7.0	mA
Input for −3.0 dB Limiting	—	—	0.7	2.0	μVrms
Recovered Audio (RF signal level = 10 mV)	13	—	350	—	mVrms
Noise Output (RF signal level = 0 mV)	13	—	250	—	mVrms
Carrier Detect Threshold (below V_{CC})	10	—	0.64	—	Vdc
Meter Drive Slope	10	—	100	—	nA/dB
Input for 20 dB (S+N)/N (See Figure 7)	—	—	0.7	—	μVrms
First Mixer 3rd Order Intercept (Input)	—	—	−22	—	dBm
First Mixer Input Resistance (Rp)	—	—	690	—	Ω
First Mixer Input Capacitance (Cp)	—	—	7.2	—	pF
First Mixer Conversion Voltage Gain	—	—	18	—	dB
Second Mixer Conversion Voltage Gain	—	—	21	—	dB
Detector Output Resistance	13	—	1.4	—	kΩ

8

FIGURE 3 — TEST CIRCUIT

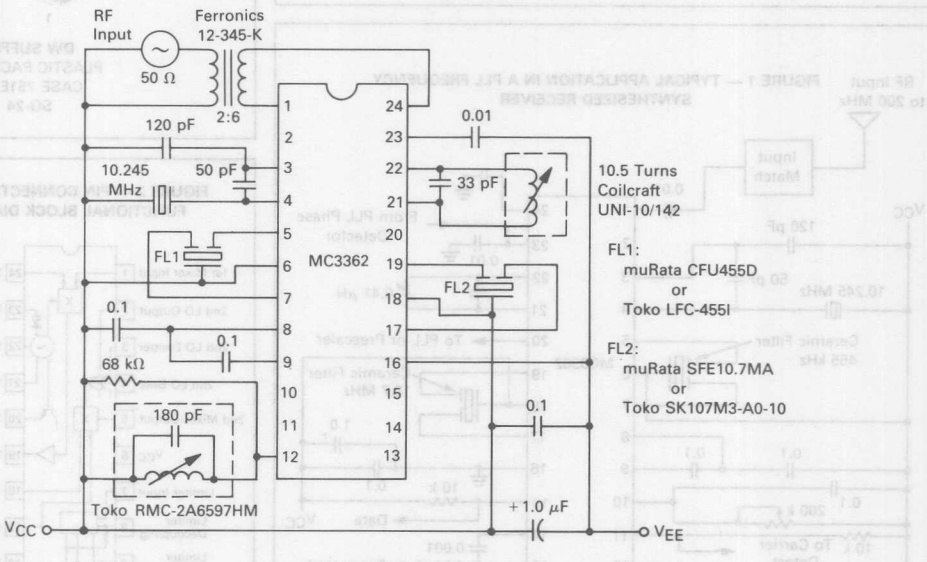


FIGURE 4 — I_{METER} versus INPUT

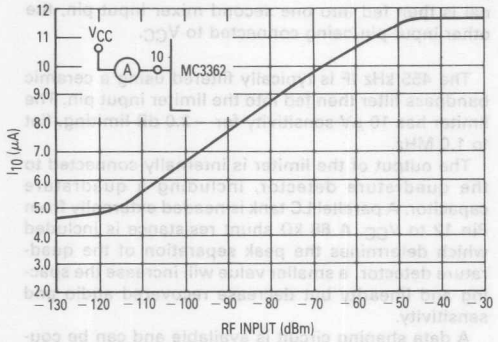


FIGURE 5 — DRAIN CURRENT, RECOVERED AUDIO versus SUPPLY

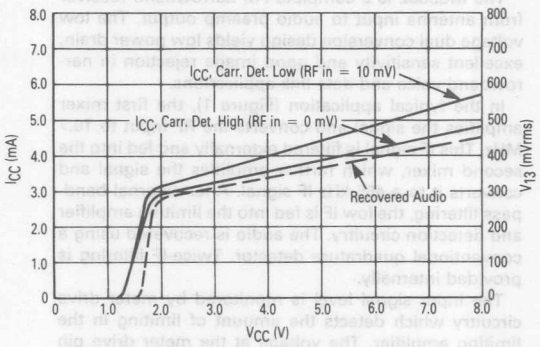


FIGURE 6 — SIGNAL LEVELS

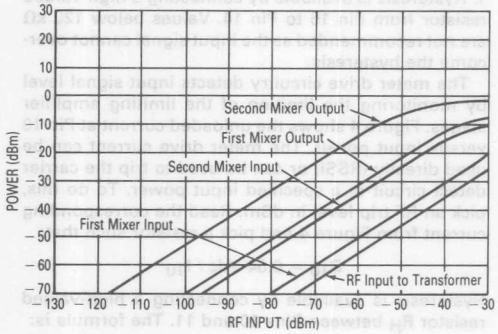


FIGURE 7 — S+N, N, AMR versus INPUT

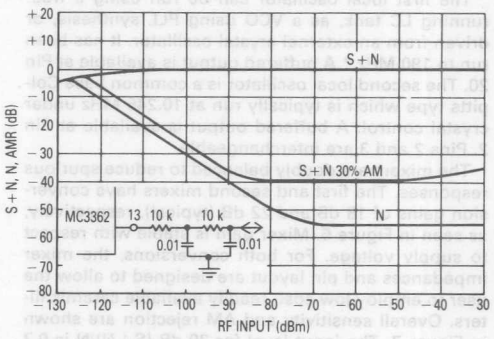


FIGURE 8 — 1ST MIXER 3RD ORDER INTERMODULATION

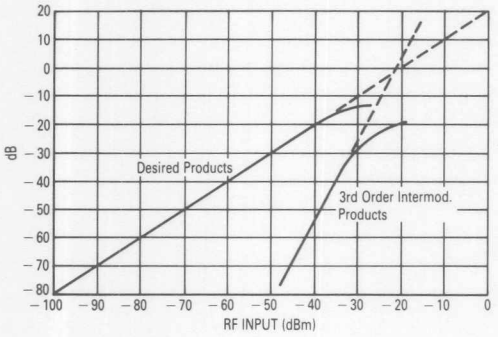
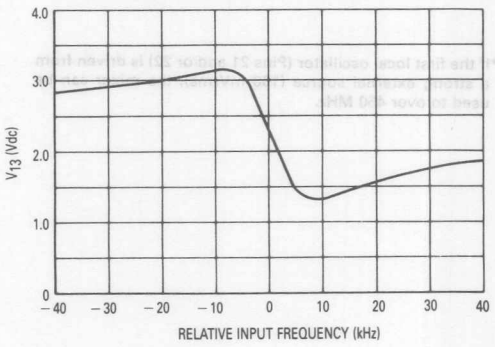


FIGURE 9 — DETECTOR OUTPUT versus FREQUENCY



8

CIRCUIT DESCRIPTION

The MC3362 is a complete FM narrowband receiver from antenna input to audio preamp output. The low voltage dual conversion design yields low power drain, excellent sensitivity and good image rejection in narrowband voice and data link applications.

In the typical application (Figure 1), the first mixer amplifies the signal and converts the RF input to 10.7 MHz. This IF signal is filtered externally and fed into the second mixer, which further amplifies the signal and converts it to a 455 kHz IF signal. After external bandpass filtering, the low IF is fed into the limiting amplifier and detection circuitry. The audio is recovered using a conventional quadrature detector. Twice-IF filtering is provided internally.

The input signal level is monitored by meter drive circuitry which detects the amount of limiting in the limiting amplifier. The voltage at the meter drive pin determines the state of the carrier detect output, which is active low.

APPLICATION

The first local oscillator can be run using a free-running LC tank, as a VCO using PLL synthesis, or driven from an external crystal oscillator. It has been run to 190 MHz.* A buffered output is available at Pin 20. The second local oscillator is a common base Colpitts type which is typically run at 10.245 MHz under crystal control. A buffered output is available at Pin 2. Pins 2 and 3 are interchangeable.

The mixers are doubly balanced to reduce spurious responses. The first and second mixers have conversion gains of 18 dB and 22 dB (typical), respectively, as seen in Figure 6. Mixer gain is stable with respect to supply voltage. For both conversions, the mixer impedances and pin layout are designed to allow the user to employ low cost, readily available ceramic filters. Overall sensitivity and AM rejection are shown in Figure 7. The input level for 20 dB (S+N)/N is 0.7 μV using the two-pole post-detection filter pictured.

Following the first mixer, a 10.7 MHz ceramic bandpass filter is recommended. The 10.7 MHz filtered signal is then fed into one second mixer input pin, the other input pin being connected to V_{CC}.

The 455 kHz IF is typically filtered using a ceramic bandpass filter then fed into the limiter input pin. The limiter has 10 μV sensitivity for −3.0 dB limiting, flat to 1.0 MHz.

The output of the limiter is internally connected to the quadrature detector, including a quadrature capacitor. A parallel LC tank is needed externally from Pin 12 to V_{CC}. A 68 kΩ shunt resistance is included which determines the peak separation of the quadrature detector; a smaller value will increase the spacing and linearity but decrease recovered audio and sensitivity.

A data shaping circuit is available and can be coupled to the recovered audio output of Pin 13. The circuit is a comparator which is designed to detect zero crossings of FSK modulation. Data rates of 2000 to 35000 baud are detectable using the circuit of Figure 1. Hysteresis is available by connecting a high-valued resistor from Pin 15 to Pin 14. Values below 120 kΩ are not recommended as the input signal cannot overcome the hysteresis.

The meter drive circuitry detects input signal level by monitoring the limiting of the limiting amplifier stages. Figure 4 shows the unloaded current at Pin 10 versus input power. The meter drive current can be used directly (RSSI) or can be used to trip the carrier detect circuit at a specified input power. To do this, pick an RF trip level in dBm. Read the corresponding current from Figure 4 and pick a resistor such that:

$$R_{10} \simeq 0.64\ Vdc / I_{10}$$

Hysteresis is available by connecting a high-valued resistor R_H between Pins 10 and 11. The formula is:

$$Hyst. = V_{CC}/(R_H \times 10^{-7})\ dB$$

*If the first local oscillator (Pins 21 and/or 22) is driven from a strong external source (100 mVrms), the mixer can be used to over 450 MHz.

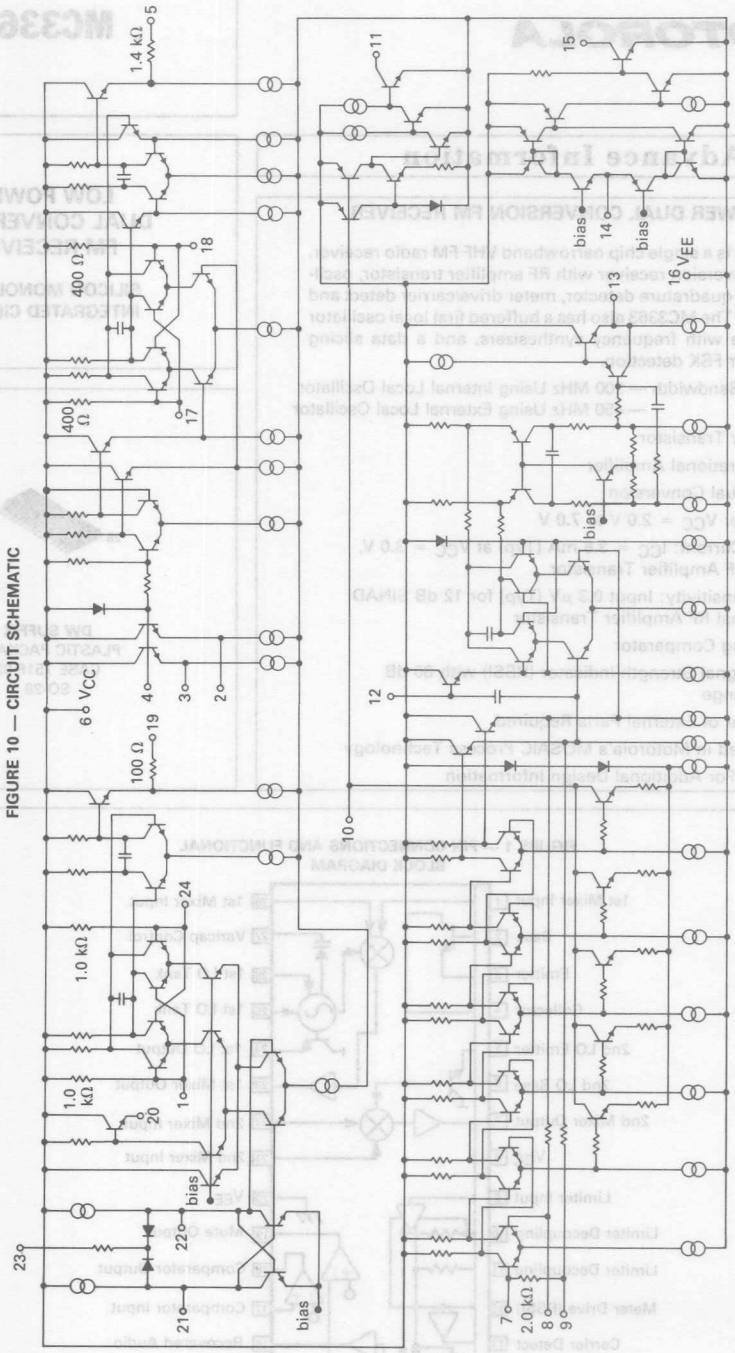


FIGURE 10 — CIRCUIT SCHEMATIC

8

MOTOROLA

MC3363

Advance Information

LOW POWER DUAL CONVERSION FM RECEIVER

The MC3363 is a single chip narrowband VHF FM radio receiver. It is a dual conversion receiver with RF amplifier transistor, oscillators, mixers, quadrature detector, meter drive/carrier detect and mute circuitry. The MC3363 also has a buffered first local oscillator output for use with frequency synthesizers, and a data slicing comparator for FSK detection.

- Wide Input Bandwidth — 200 MHz Using Internal Local Oscillator
  — 450 MHz Using External Local Oscillator
- RF Amplifier Transistor
- Muting Operational Amplifier
- Complete Dual Conversion
- Low Voltage: V_{CC} = 2.0 V to 7.0 V
- Low Drain Current: I_{CC} = 3.6 mA (Typ) at V_{CC} = 3.0 V, Excluding RF Amplifier Transistor
- Excellent Sensitivity: Input 0.3 μV (Typ) for 12 dB SINAD Using Internal RF Amplifier Transistor
- Data Shaping Comparator
- Received Signal Strength Indicator (RSSI) with 60 dB Dynamic Range
- Low Number of External Parts Required
- Manufactured in Motorola's MOSAIC Process Technology
- See AN980 For Additional Design Information

LOW POWER DUAL CONVERSION FM RECEIVER

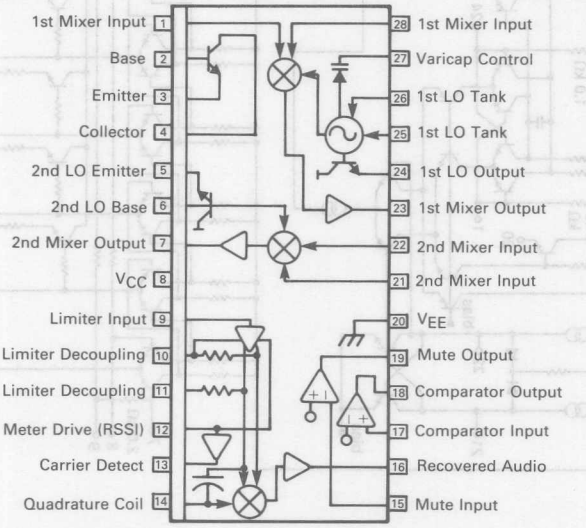
SILICON MONOLITHIC INTEGRATED CIRCUIT



DW SUFFIX
PLASTIC PACKAGE
CASE 751F-02
SO-28

8

FIGURE 1 — PIN CONNECTIONS AND FUNCTIONAL BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

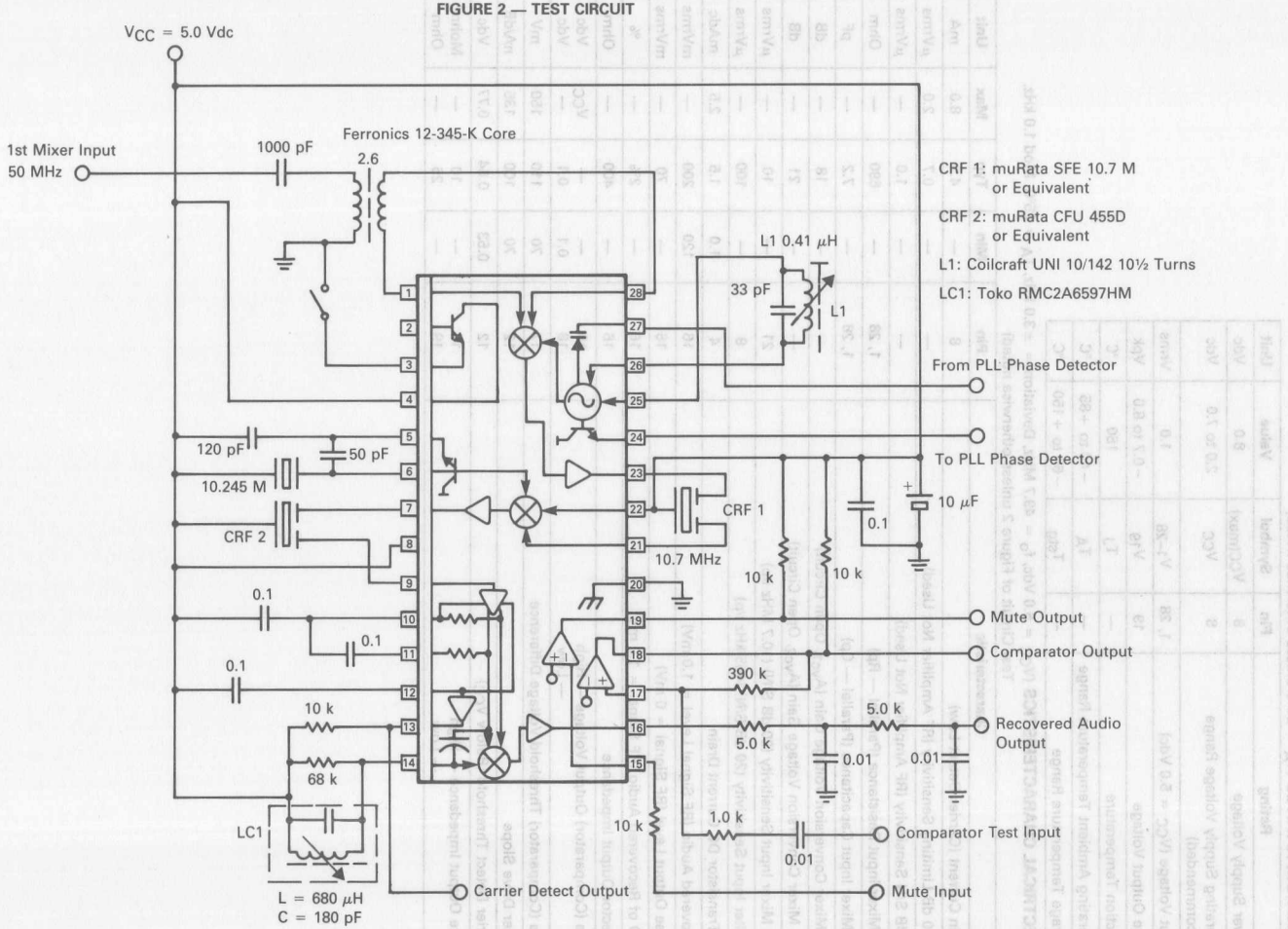
Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	8	$V_{CC(max)}$	8.0	Vdc
Operating Supply Voltage Range (Recommended)	8	V_{CC}	2.0 to 7.0	Vdc
Input Voltage (V_{CC} = 5.0 Vdc)	1, 28	V_{1-28}	1.0	Vrms
Mute Output Voltage	19	V_{19}	−0.7 to 8.0	Vpk
Junction Temperature	—	T_J	150	°C
Operating Ambient Temperature Range	—	T_A	−40 to +85	°C
Storage Temperature Range	—	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, f_o = 49.7 MHz, Deviation = ±3.0 kHz, T_A = 25°C, Mod 1.0 kHz, Test Circuit of Figure 2 unless otherwise noted)

Characteristic	Pin	Min	Typ	Max	Unit
Drain Current (Carrier Detect Low)	8	—	4.5	8.0	mA
−3.0 dB Limiting Sensitivity (RF Amplifier Not Used)	—	—	0.7	2.0	μVrms
20 dB S/N Sensitivity (RF Amplifier Not Used)	—	—	1.0	—	μVrms
1st Mixer Input Resistance (Parallel — Rp)	1, 28	—	690	—	Ohm
1st Mixer Input Capacitance (Parallel — Cp)	1, 28	—	7.2	—	pF
1st Mixer Conversion Voltage Gain (A_{vc1}, Open Circuit)	—	—	18	—	dB
2nd Mixer Conversion Voltage Gain (A_{vc2}, Open Circuit)	—	—	21	—	dB
2nd Mixer Input Sensitivity (20 dB S/N) (10.7 MHz i/p)	21	—	10	—	μVrms
Limiter Input Sensitivity (20 dB S/N) (455 kHz i/p)	9	—	100	—	μVrms
RF Transistor DC Current Drain	4	1.0	1.5	2.5	mAdc
Recovered Audio (RF Signal Level = 1.0 mV)	16	120	200	—	mVrms
Noise Output Level (RF Signal = 0 mV)	16	—	70	—	mVrms
THD of Recovered Audio (RF Signal = 1.0 mV)	16	—	2%	—	%
Detector Output Impedance	16	—	400	—	Ohm
Data (Comparator) Output Voltage — High — Low	18 18	— 0.1	— 0.1	V_{CC} —	Vdc Vdc
Data (Comparator) Threshold Voltage Difference	17	70	110	150	mV
Meter Drive Slope	12	70	100	135	nA/dB
Carrier Detect Threshold (Below V_{CC})	12	0.53	0.64	0.77	Vdc
Mute Output Impedance — High — Low	19 19	— —	10 25	— —	Mohm Ohm

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FIGURE 2 — TEST CIRCUIT



CIRCUIT DESCRIPTION

The MC3363 is a complete FM narrowband receiver from RF amplifier to audio preamp output. The low voltage dual conversion design yields low power drain, excellent sensitivity and good image rejection in narrowband voice and data link applications.

In the typical application, the input RF signal is amplified by the RF transistor and then the first mixer amplifies the signal and converts the RF input to 10.7 MHz. This IF signal is filtered externally and fed into the second mixer, which further amplifies the signal and converts it to a 455 kHz IF signal. After external bandpass filtering, the low IF is fed into the limiting amplifier and detection circuitry. The audio is recovered using a conventional quadrature detector. Twice-IF filtering is provided internally.

The input signal level is monitored by meter drive circuitry which detects the amount of limiting in the limiting amplifier. The voltage at the meter drive pin determines the state of the carrier detect output, which is active low.

APPLICATION

The first local oscillator is designed to serve as the VCO in a PLL frequency synthesized receiver. The MC3363 can operate together with the MC145166/7 to provide a two-chip ten channel frequency synthesized receiver in the 46/49 cordless telephone band. The MC3363 can also be used with the MC14515X series of CMOS PLL synthesizers and MC120XX series of ECL prescalers in VHF frequency synthesized applications to 200 MHz.

For single channel applications the first local oscillator can be crystal controlled. The circuit of Figure 4 has been used successfully up to 60 MHz. For higher frequencies an external oscillator signal can be injected into Pins 25 and/or 26 — a level of approximately 100 mVrms is recommended. The first mixer's transfer characteristic is essentially flat to 450 MHz when this approach is used (keeping a constant 10.7 MHz IF frequency). The second local oscillator is a Colpitts type which is typically run at 10.245 MHz under crystal control.

The mixers are doubly balanced to reduce spurious responses. The first and second mixers have conversion gains of 18 dB and 21 dB (typical), respectively. Mixer gain is stable with respect to supply voltage. For both conversions, the mixer impedances and pin layout are designed to allow the user to employ low cost, readily available ceramic filters.

Following the first mixer, a 10.7 MHz ceramic bandpass filter is recommended. The 10.7 MHz filtered signal is then fed into the second mixer input Pin 21, the other input Pin 22 being connected to V_{CC}.

The 455 kHz IF is filtered by a ceramic narrow bandpass filter then fed into the limiter input Pin 9. The limiter has 10 μV sensitivity for −3.0 dB limiting, flat to 1.0 MHz.

The output of the limiter is internally connected to the quadrature detector, including a quadrature capacitor. A parallel LC tank is needed externally from Pin 14 to V_{CC}. A 68 kOhm shunt resistance is included which determines the peak separation of the quadrature detector; a smaller value will lower the Q and expand the deviation range and linearity, but decrease recovered audio and sensitivity.

A data shaping circuit is available and can be coupled to the recovered audio output of Pin 16. The circuit is a comparator which is designed to detect zero crossings of FSK modulation. Data rates of 2000 to 35000 baud are detectable using the comparator. Best sensitivity is obtained when data rates are limited to 1200 baud maximum. Hysteresis is available by connecting a high-valued resistor from Pin 17 to Pin 18. Values below 120 kOhm are not recommended as the input signal cannot overcome the hysteresis.

The meter drive circuitry detects input signal level by monitoring the limiting of the limiting amplifier stages. Figure 5 shows the unloaded current at Pin 12 versus input power. The meter drive current can be used directly (RSSI) or can be used to trip the carrier detect circuit at a specified input power.

A muting op amp is provided and can be triggered by the carrier detect output (Pin 13). This provides a carrier level triggered squelch circuit which is activated when the RF input at the desired input frequency falls below a preset level. The level at which this occurs is determined by the resistor placed between the meter drive output (Pin 12) and V_{CC}. Values between 80–130 kOhms are recommended. This type of squelch is pictured in Figures 3 and 4.

Hysteresis is available by connecting a high-valued resistor Rh between Pins 12 and 13. The formula is:

$$\text{Hyst} = V_{CC}/(\text{Rh} \times 10^{-7})\ \text{dB}$$

The meter drive can also be used directly to drive a meter or to provide AGC. A current to voltage converter or other linear buffer will be needed for this application.

A second possible application of the op amp would be in a noise triggered squelch circuit, similar to that used with the MC3357/MC3359/MC3361 FM I.F.'s. In this case the op amp would serve as an active noise filter, the output of which would be rectified and compared to a reference on a squelch gate. The MC3363 does not have a dedicated squelch gate, but the NPN RF input stage or data shaping comparator might be used to provide this function if available. The op amp is a basic type with the inverting input and the output available. This application frees the meter drive to allow it to be used as a linear signal strength monitor.

The circuit of Figure 4 is a complete 50 MHz receiver from antenna input to audio preamp output. It uses few components and has good performance. The receiver operates on a single channel and has input sensitivity of <0.3 μV for 12 dB SINAD.

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FIGURE 3 — TYPICAL APPLICATION IN A PLL FREQUENCY SYNTHESIZED RECEIVER

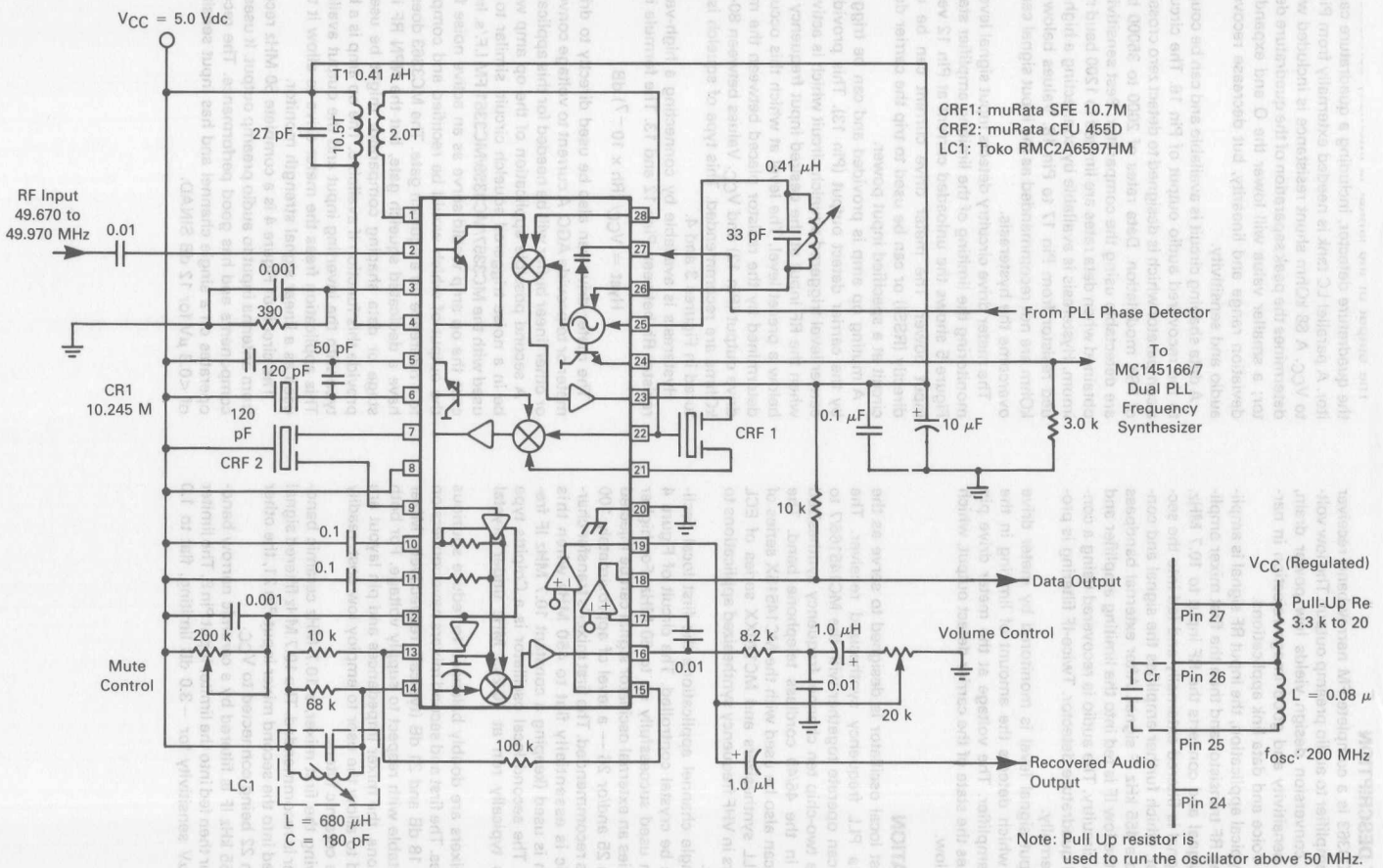
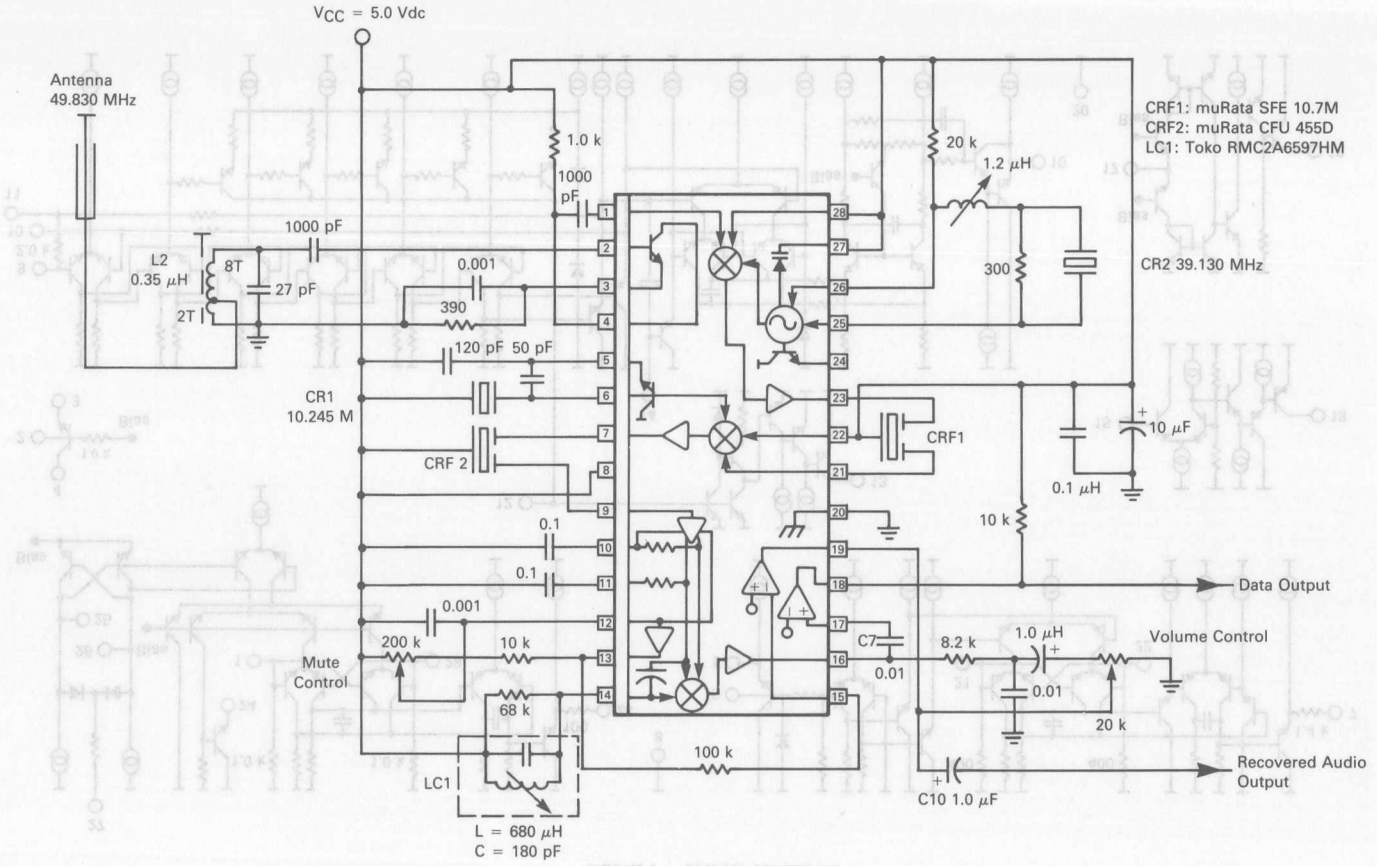


FIGURE 4 — SINGLE CHANNEL CRYSTAL CONTROLLED FM RECEIVER



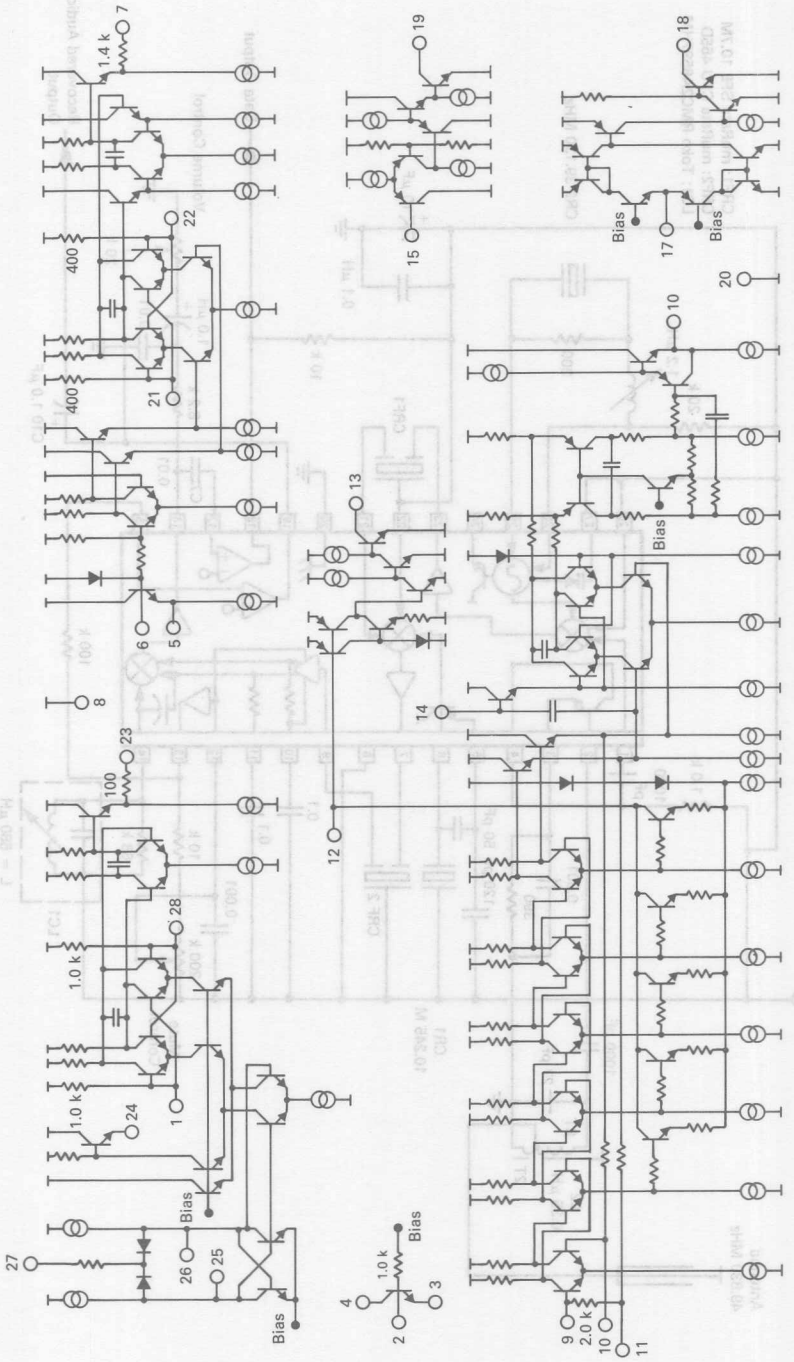


FIGURE 5 — CIRCUIT SCHEMATIC

MOTOROLA

MC3367

Product Preview

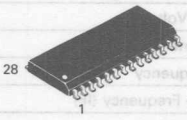
LOW VOLTAGE FM NARROWBAND RECEIVER

. . . with single conversion circuitry including oscillator, mixer, IF amplifiers, limiting IF circuitry, and quadrature discriminator. The MC3367 is perfect for narrowband audio and data applications up to 75 MHz which require extremely low power consumption. Battery powered applications down to V_{CC} = 1.1 V are possible. The MC3367 also includes an on-board voltage regulator, low battery detection circuitry, a receiver enable allowing a power down "sleep mode," two undedicated buffer amplifiers to allow simultaneous audio and data reception, and a comparator for enhancing FSK (Frequency Shift Keyed) data reception.

- Low Supply Voltage: V_{CC} = 1.1 to 3.0 Vdc
- Low Power Consumption: P_D = 1.5 to 5.0 mW
- Input Bandwidth 75 MHz
- Excellent Sensitivity: Input Limiting Voltage (−3.0 dB) = 0.2 μVrms
- Voltage Regulator Available (Source Capability 3.0 mA)
- Receiver Enable to Allow Active/Standby Operation
- Low Battery Detection Circuitry
- Self Biasing Audio Buffer with Nominal Gain A_V = 4.0
- Data Buffer with Nominal Gain A_V = 3.2
- Comparator with > 25 kHz (50 kbaud) Capability
- Standard 28-Lead Surface Mount (SOIC) Package

LOW VOLTAGE SINGLE CONVERSION FM RECEIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT



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CASE 751F-02
SO-28

PIN CONNECTIONS

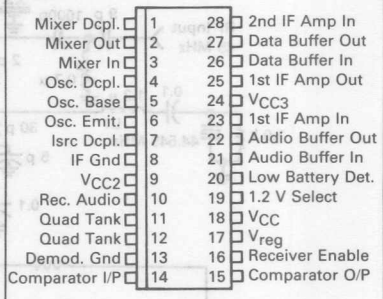
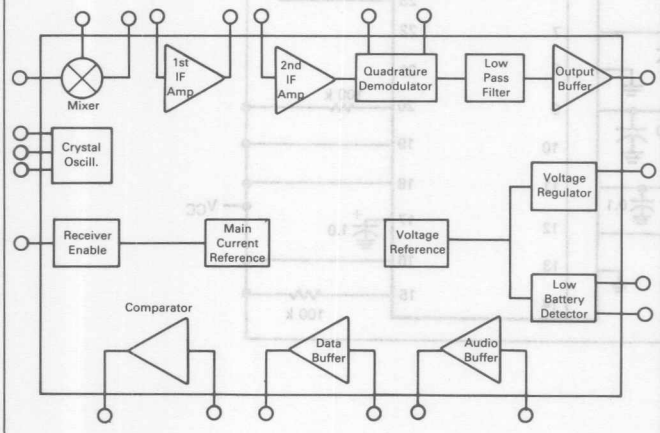


FIGURE 1 — BLOCK DIAGRAM



This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

Parameter	Pin	Value	Units
Supply Voltage	18	5.0	Vdc
RF Input Signal	3	1.0	Vrms
Audio Buffer Input	21	1.0	Vrms
Data Buffer Input	26	1.0	Vrms
Comparator Input	14	1.0	Vrms
Junction Temperature	—	150	°C
Storage Temperature	—	−65 to +150	°C

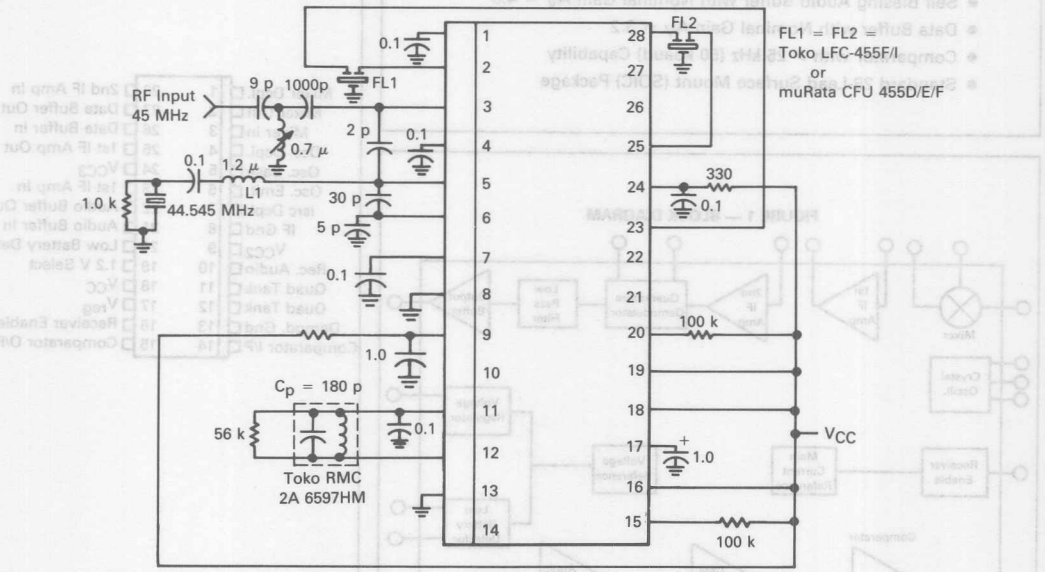
Devices should not be operated at or outside these values. The "Recommended Operating Limits" provide for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Parameter	Pin	Value	Units
Supply Voltage	18	1.1 to 3.0	Vdc
Receiver Enable Voltage	16	0 or V_{CC}	Vdc
1.2 V Select Voltage	19	V_{CC}	Vdc
RF Input Signal	3	0.001 to 100	mVrms
RF Input Frequency	3	0 to 75	MHz
Intermediate Frequency (IF)	—	455	kHz
Audio Buffer Input	21	0 to 75	mVrms
Data Buffer Input	26	0 to 75	mVrms
Comparator Input	14	10 to 300	mVrms
Ambient Temperature	—	0 to 70	°C

FIGURE 2 — TEST CIRCUIT

(All capacitors in μF unless otherwise stated. Resistors in ohms. Inductors in Henries.)



ELECTRICAL CHARACTERISTICS (V_{CC} = 1.3 V, f_o = 45 MHz, f_{mod} = 1.0 kHz, Deviation = 3.0 kHz, T_A = 25°C, Test Circuit of Figure 2 unless otherwise noted)

Characteristic	Pin	Min	Typ	Max	Units
OVERALL MC3367 PERFORMANCE					
Drain Current — Pin 15 = V_{CC}	—	—	1.4	3.0	mA
— Pin 15 = 0 Vdc	—	—	0.5	—	μA
Recovered Audio (RF Input = 10 mV)	10	—	13	—	mVrms
Noise Output (RF Input = 0 mV)	10	—	4.5	—	mVrms
Input for −3.0 dB Limiting	3	—	0.2	—	μVrms
MIXER					
Mixer Input Resistance (Rp)	3	—	3.0	—	kΩ
Mixer Input Capacitance (Cp)	3	—	9.0	—	pF
FIRST IF AMPLIFIER					
First IF Amp Voltage Gain	—	—	25	—	dB
AUDIO BUFFER					
Voltage Gain	—	—	4.0	—	V/V
Input Resistance	21	—	125	—	kΩ
Maximum Input for Undistorted Output	21	—	70	—	mVrms
Maximum Output Swing	22	—	800	—	mVpp
Output Resistance	22	—	680	—	Ω
DATA BUFFER					
Voltage Gain	—	—	3.2	—	V/V
Input Resistance	26	—	8.0	—	MΩ
Maximum Input for Undistorted Output	26	—	70	—	mVrms
Maximum Output Swing	27	—	600	—	mVpp
Output Resistance	27	—	1.5	—	kΩ
COMPARATOR					
Minimum Input for Triggering	14	—	7.0	—	mVrms
Maximum Input Frequency (R_L = 100 kΩ)	14	—	25	—	kHZ
Rise Time (10–90%; R_L = 100 kΩ)	15	—	5.0	—	μs
Fall Time (90–10%; R_L = 100 kΩ)	15	—	0.4	—	μs
LOW BATTERY DETECTOR					
Low Battery Trip Point	18	—	1.09	—	Vdc
Low Battery Output — V_{CC} = 0.9 V	20	—	0.2	—	Vdc
— V_{CC} = 1.3 V	20	—	V_{CC}	—	Vdc
VOLTAGE REGULATOR					
Regulated Output (see Figure 6)	17	—	0.95	—	Vdc
Source Capability	17	—	—	3.0	mA

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FIGURE 3 — RECOVERED AUDIO versus SUPPLY

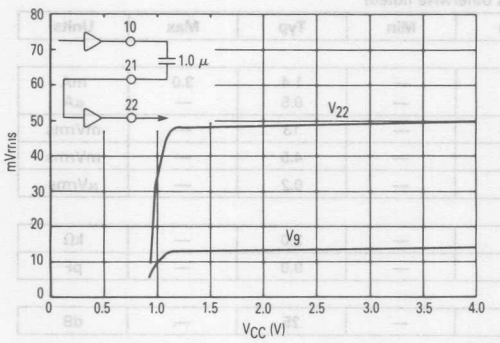


FIGURE 4 — DRAIN versus SUPPLY

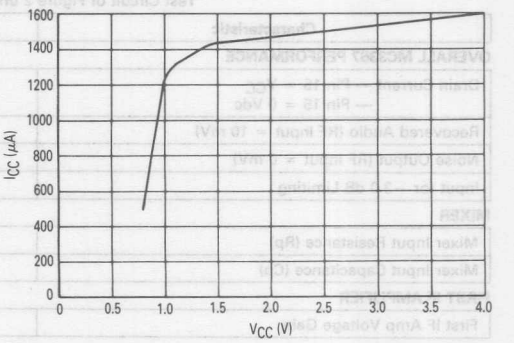


FIGURE 5 — S+N, N versus INPUT

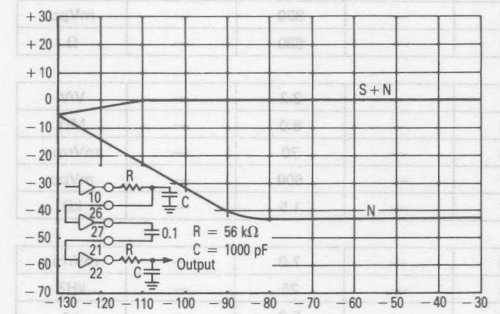
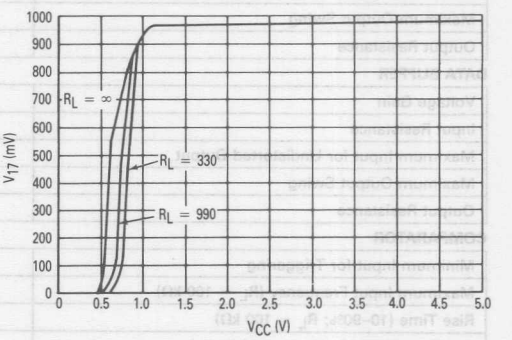


FIGURE 6 — V_{REG} versus SUPPLY



CIRCUIT DESCRIPTION

The MC3367 is an FM narrowband receiver capable of operation to 75 MHz. The low voltage design yields low power drain and excellent sensitivity in narrowband voice and data link applications. In the typical application the mixer amplifies the incoming RF or IF signal and converts the RF or IF frequency to 455 kHz. This signal is then filtered by a 455 ceramic filter and applied to the first intermediate frequency (IF) amplifier input. This amplifier amplifies the 455 kHz IF before it is filtered by a second ceramic filter. The modulated IF signal is then applied to the limiting IF amplifier and detector circuitry. Audio is recovered by a conventional quadrature detector.

Features available include buffers for audio/data amplification and active filtering, on board voltage regulator, low battery detection circuitry with programmable level, and receiver disable circuitry. The MC3367 is an FM utility receiver to be used for voice and/or narrowband data reception, especially suitable where extremely low power consumption and high design flexibility are required.

APPLICATION

The MC3367 can be used as a high performance FM IF for use in low power dual conversion receivers. Because of the MC3367's extremely good sensitivity (0.6 μV for 20 dB (S+N)/N, see Figure 5), it can also be used as a stand alone single conversion narrowband receiver to 75 MHz for applications not sensitive to image frequency interference.

The oscillator is a Colpitts type which can be run as an LC oscillator or under crystal control. The crystal in Figure 2 is a 3rd overtone series mode type, and the 1.2 μH coil (L1) and 1.0 kΩ resistor are needed to ensure proper operation. For fundamental mode crystals, the inductor L1 can be omitted.

The best adjacent channel and sensitivity response occur when two 455 kHz ceramic filters are used, as shown in Figure 2. Either can be replaced by a 0.1 μF coupling capacitor to reduce cost, but some degradation in sensitivity and/or stability is suspected.

The detector is a quadrature type, with the connection from the limiter output to the detector input provided internally as with the MC3359 and the MC3361.

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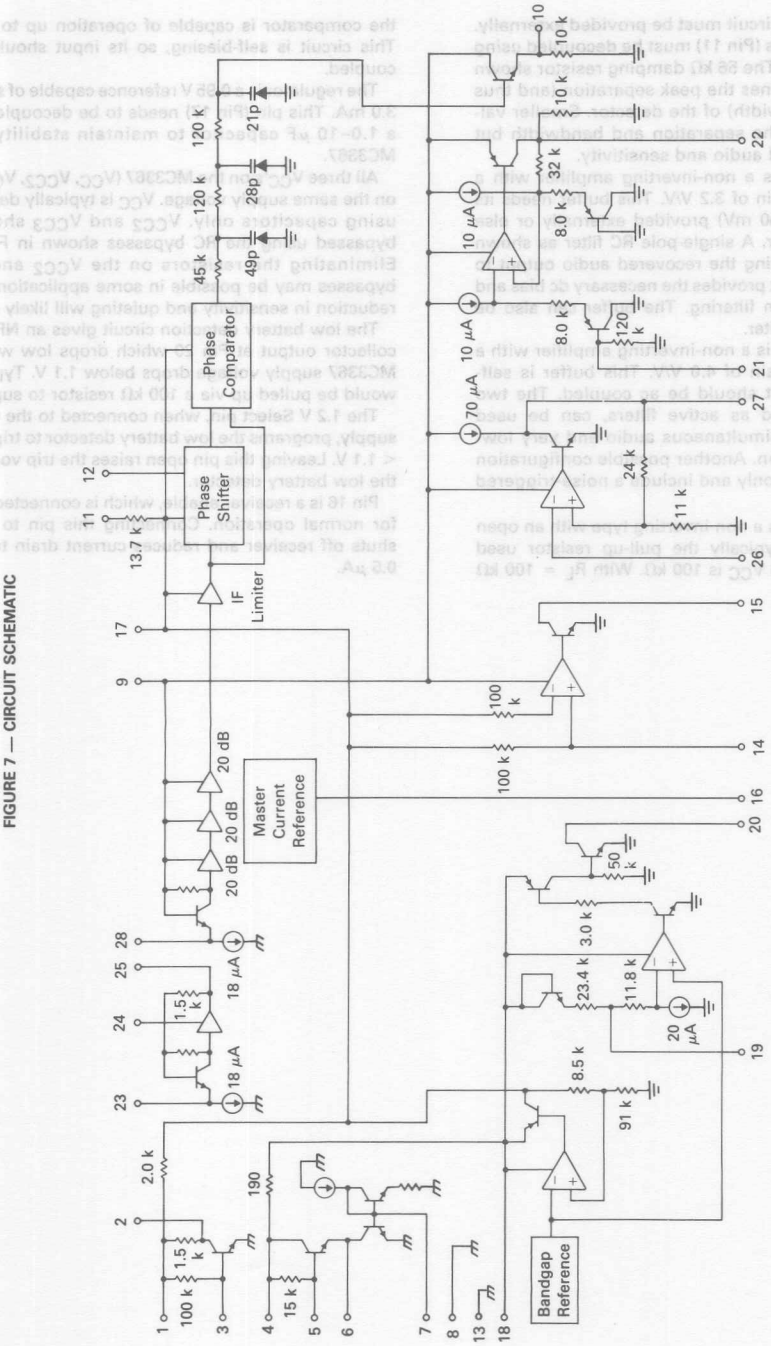


FIGURE 7 — CIRCUIT SCHEMATIC

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One of the tank pins (Pin 11) must be decoupled using a 0.1 μF capacitor. The 56 kΩ damping resistor shown in Figure 2 determines the peak separation (and thus the detector bandwidth) of the detector. Smaller values will increase the separation and bandwidth but decrease recovered audio and sensitivity.

The data buffer is a non-inverting amplifier with a nominal voltage gain of 3.2 V/V. This buffer needs its dc bias (approx. 250 mV) provided externally or else debiasing will occur. A single-pole RC filter as shown in Figure 5 connecting the recovered audio output to the data buffer input provides the necessary dc bias and some post-detection filtering. The buffer can also be used as an active filter.

The audio buffer is a non-inverting amplifier with a nominal voltage gain of 4.0 V/V. This buffer is self-biasing so its input should be ac coupled. The two buffers, when used as active filters, can be used together to allow simultaneous audio and very low-speed data reception. Another possible configuration is to receive audio only and include a noise-triggered squelch.

The comparator is a non-inverting type with an open collector output. Typically the pull-up resistor used between Pin 15 and V_{CC} is 100 kΩ. With R_L = 100 kΩ [illegible] operation up to 25 kHz. This circuit is self-biasing, so its input should be ac coupled.

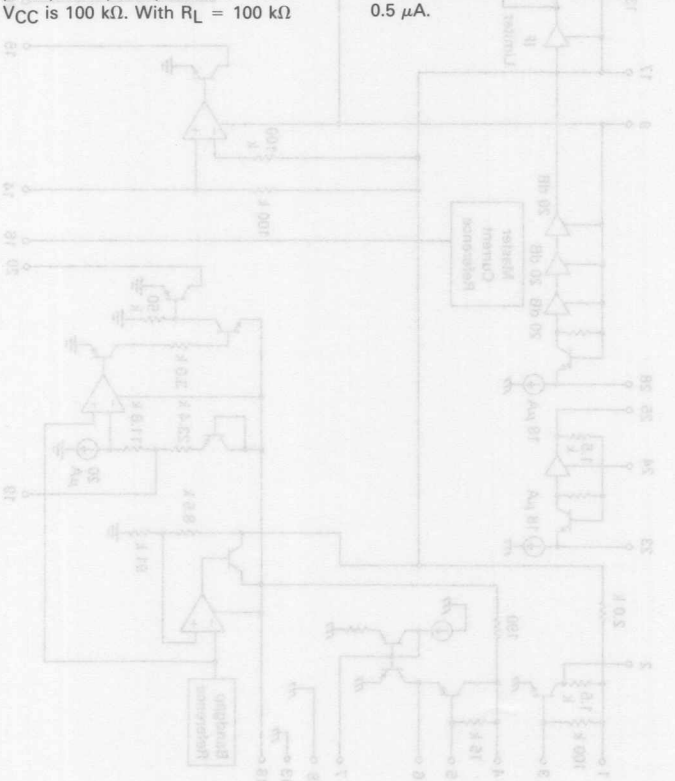
The regulator is a 0.95 V reference capable of sourcing 3.0 mA. This pin (Pin 17) needs to be decoupled using a 1.0–10 μF capacitor to maintain stability of the MC3367.

All three V_{CC}'s on the MC3367 (V_{CC}, V_{CC2}, V_{CC3}) run on the same supply voltage. V_{CC} is typically decoupled using capacitors only. V_{CC2} and V_{CC3} should be bypassed using the RC bypasses shown in Figure 2. Eliminating the resistors on the V_{CC2} and V_{CC3} bypasses may be possible in some applications, but a reduction in sensitivity and quieting will likely occur.

The low battery detection circuit gives an NPN open collector output at Pin 20 which drops low when the MC3367 supply voltage drops below 1.1 V. Typically it would be pulled up via a 100 kΩ resistor to supply.

The 1.2 V Select pin, when connected to the MC3367 supply, programs the low battery detector to trip at $V_{CC} < 1.1$ V. Leaving this pin open raises the trip voltage on the low battery detector.

Pin 16 is a receiver enable, which is connected to V_{CC} for normal operation. Connecting this pin to ground shuts off receiver and reduces current drain to $I_{CC} < 0.5$ μA.



MOTOROLA

MC13055

WIDEBAND FSK RECEIVER

The MC13055 is intended for RF data link systems using carrier frequencies up to 40 MHz and FSK (frequency shift keying) data rates up to 2.0M Baud (1.0 MHz). This design is similar to the MC3356, except that it does not include the oscillator/mixer. The IF bandwidth has been increased and the detector output has been revised to a balanced configuration. The received signal strength metering circuit has been retained, as has the versatile data slicer/comparator.

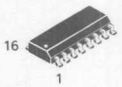
- Input Sensitivity 20 μV @ 40 MHz
- Signal Strength Indicator Linear Over 3 Decades
- Available in Surface Mount Package
- Easy Application, Few Peripheral Components

WIDEBAND FSK RECEIVER

MONOLITHIC SILICON INTEGRATED CIRCUIT

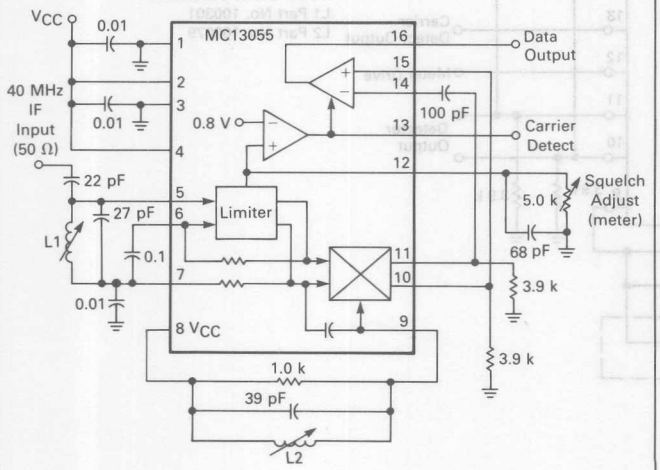


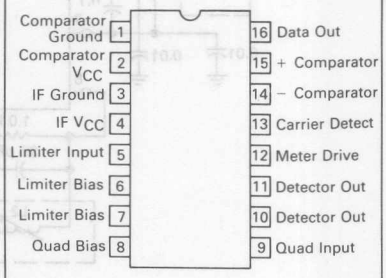
P SUFFIX
PLASTIC PACKAGE
CASE 648-06



D SUFFIX
PLASTIC PACKAGE
CASE 751B-03
SO-16

FIGURE 1 — BLOCK DIAGRAM AND APPLICATION CIRCUIT





8

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC(max)}$	15	Vdc
Operating Supply Voltage Range	V2, V4	3.0 to 12	Vdc
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Power Dissipation, Package Rating	P_D	1.25	W

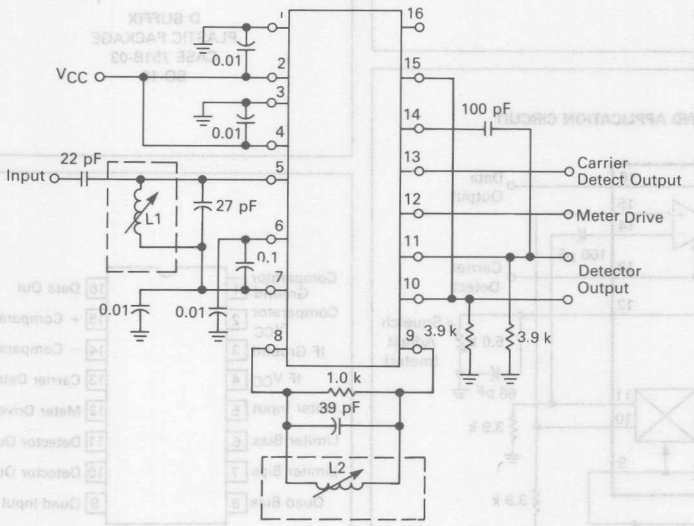
ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0 Vdc, f_o = 40 MHz, f_{mod} = 1.0 MHz, Δf = ±1.0 MHz, T_A = 25°C, Test circuit of Figure 2)

Characteristics		Measure	Min	Typ	Max	Unit
Total Drain Current		I2 + I4	—	20	25	mA
Data Comparator Pull-Down Current		I16	—	10	—	mA
Meter Drive Slope versus Input		I12	4.5	7.0	9.0	μA/dB
Carrier Detect Pull-Down Current		I13	—	1.3	—	mA
Carrier Detect Pull-Up Current		I13	—	500	—	μA
Carrier Detect Threshold Voltage		V12	700	800	900	mV
DC Output Current		I10, I11	—	430	—	μA
Recovered Signal		V10 − V11	—	350	—	mVrms
Sensitivity for 20 dB S+N/N, BW = 5.0 MHz		VIN	—	20	—	μVrms
S+N/N at V_{in} = 50 μV		V10 − V11	—	30	—	dB
Input Impedance @ 40 MHz	R_{in}	Pin 5, Ground	—	4.2	—	kΩ
	C_{in}		—	4.5	—	pF
Quadrature Coil Loading	R_{in}	Pin 9 to 8	—	7.6	—	kΩ
	C_{in}		—	5.2	—	pF

8

FIGURE 2 — TEST CIRCUIT



Coils — Shielded
Coilcraft UNI–10/142
L1 Gray 8-1/2 Turns, nominal 300 μH
L2 Black 10-1/2 Turns, nominal 380 μH

or
TOKO Series E526HNA
L1 Part No. 100301
L2 Part No. 100079

All curves taken with test conditions of ELECTRICAL CHARACTERISTICS, unless otherwise noted

FIGURE 3 — OVERALL GAIN, NOISE, AM REJECTION

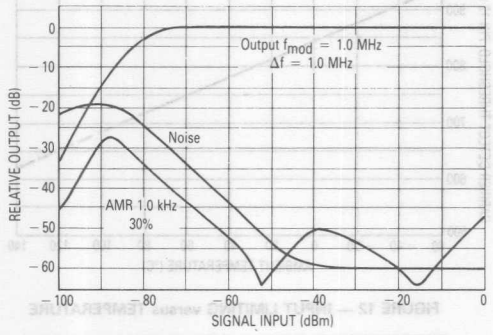


FIGURE 4 — METER CURRENT versus SIGNAL

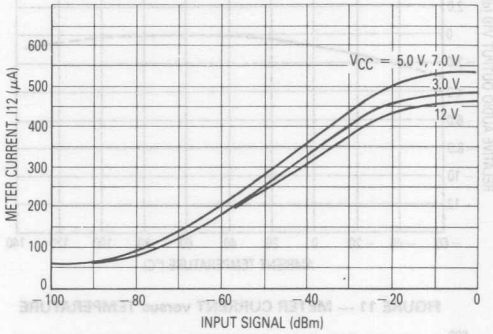


FIGURE 5 — UNTUNED INPUT: LIMITING SENSITIVITY versus FREQUENCY

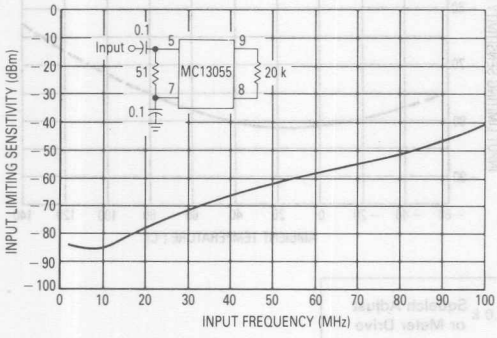


FIGURE 6 — UNTUNED INPUT: METER CURRENT versus FREQUENCY

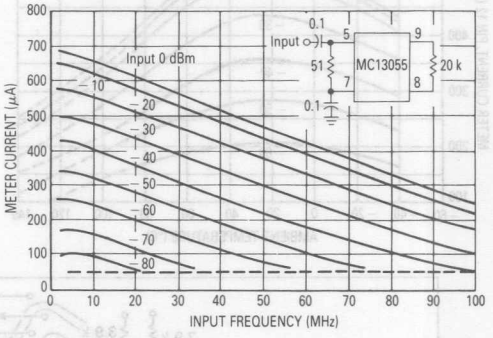


FIGURE 7 — LIMITING SENSITIVITY AND DETUNING versus SUPPLY

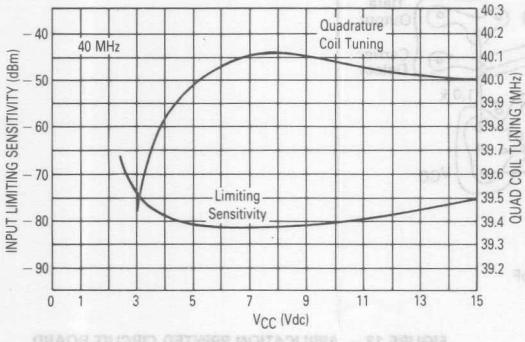
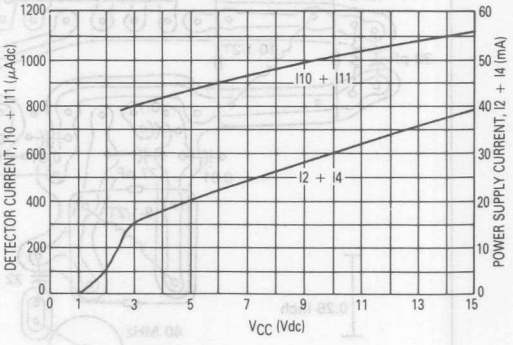


FIGURE 8 — DETECTOR CURRENT AND POWER SUPPLY CURRENT versus SUPPLY VOLTAGE



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FIGURE 9 — RECOVERED AUDIO versus TEMPERATURE

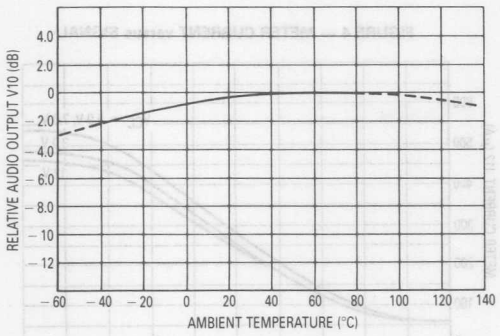


FIGURE 10 — CARRIER DETECT THRESHOLD versus TEMPERATURE

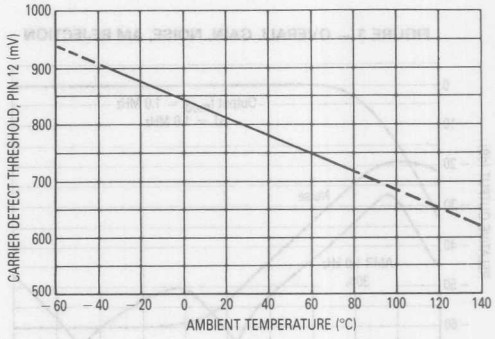


FIGURE 11 — METER CURRENT versus TEMPERATURE

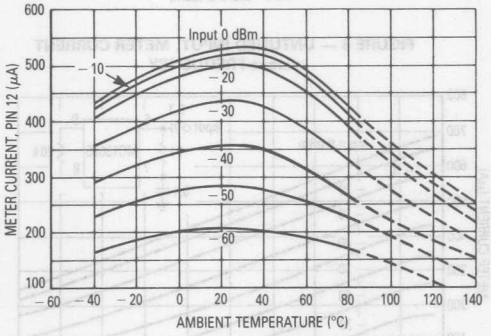
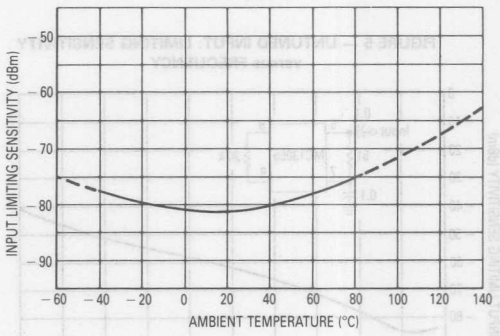


FIGURE 12 — INPUT LIMITING versus TEMPERATURE



8

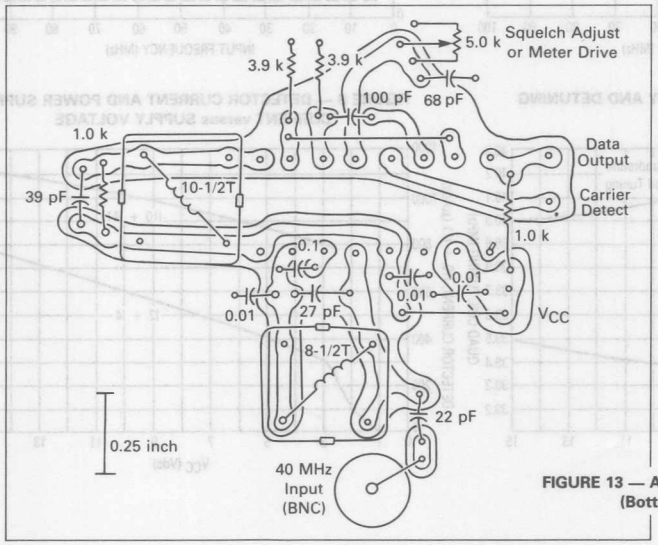


FIGURE 13 — APPLICATION PRINTED CIRCUIT BOARD
(Bottom View, Circuit of Figure 1)

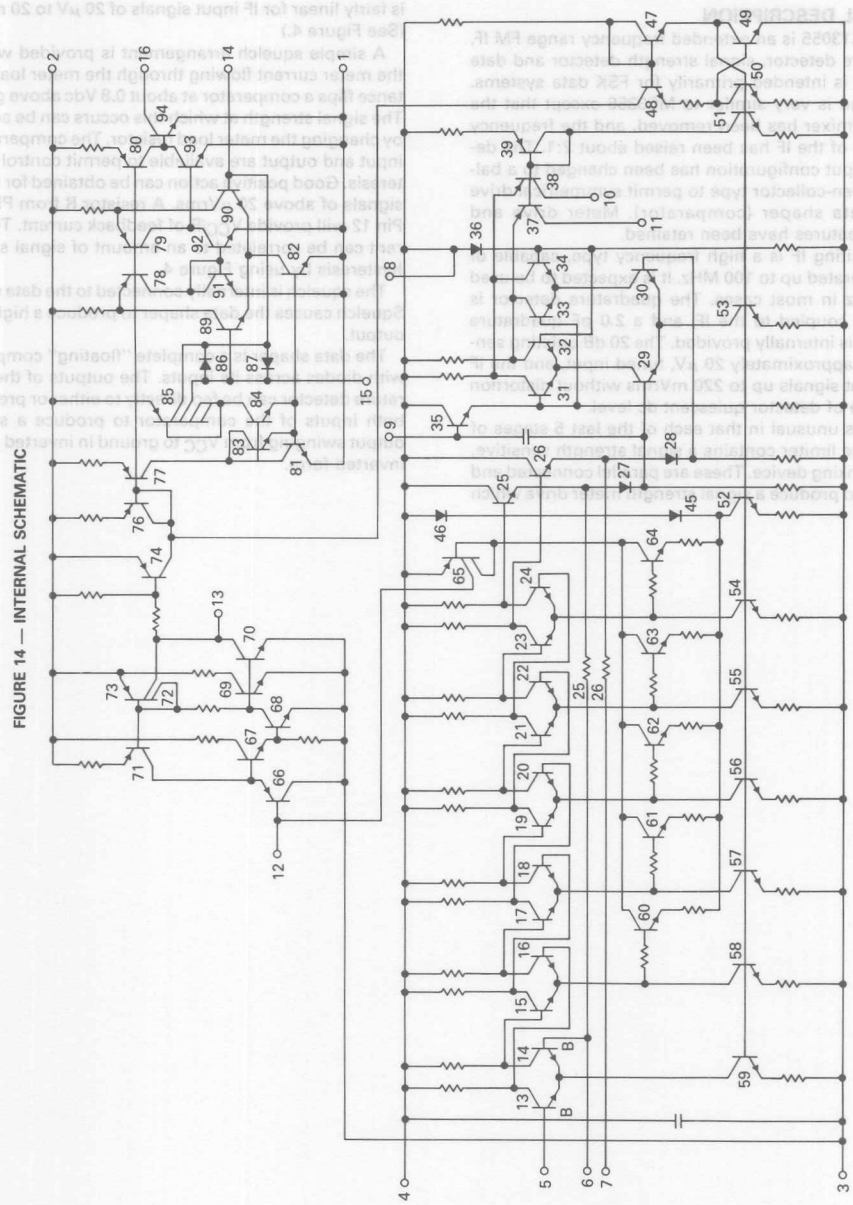


FIGURE 14 — INTERNAL SCHEMATIC

GENERAL DESCRIPTION

The MC13055 is an extended frequency range FM IF, quadrature detector, signal strength detector and data shaper. It is intended primarily for FSK data systems. The design is very similar to MC3356 except that the oscillator/mixer has been removed, and the frequency capability of the IF has been raised about 2:1. The detector output configuration has been changed to a balanced, open-collector type to permit symmetrical drive of the data shaper (comparator). Meter drive and squelch features have been retained.

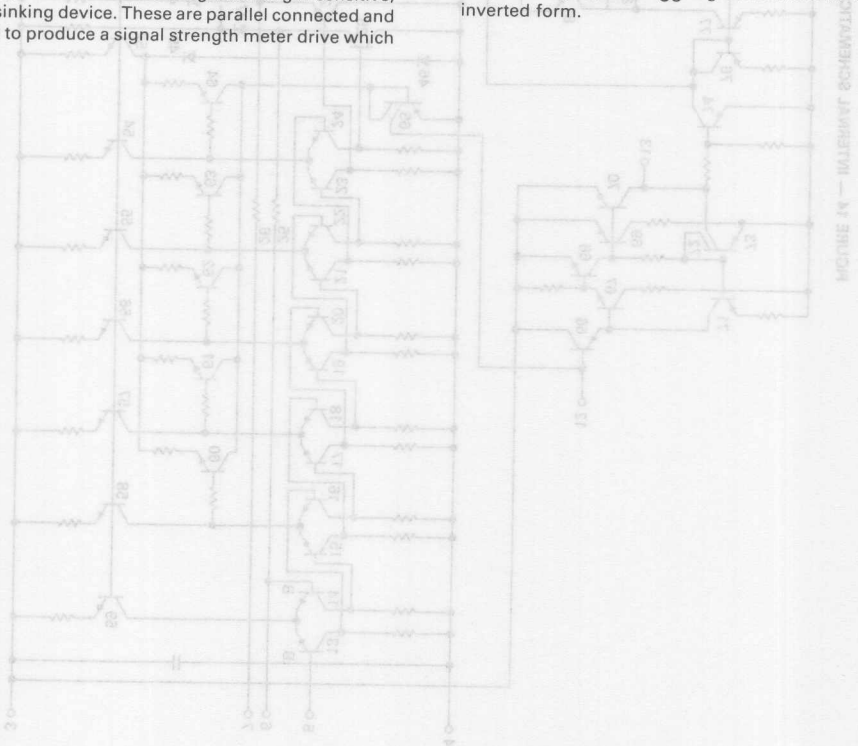
The limiting IF is a high frequency type, capable of being operated up to 100 MHz. It is expected to be used at 40 MHz in most cases. The quadrature detector is internally coupled to the IF, and a 2.0 pF quadrature capacitor is internally provided. The 20 dB quieting sensitivity is approximately 20 μV, tuned input, and the IF can accept signals up to 220 mVrms without distortion or change of detector quiescent dc level.

The IF is unusual in that each of the last 5 stages of the 6 stage limiter contains a signal strength sensitive, current sinking device. These are parallel connected and buffered to produce a signal strength meter drive which is fairly linear for IF input signals of 20 μV to 20 mVrms. (See Figure 4.)

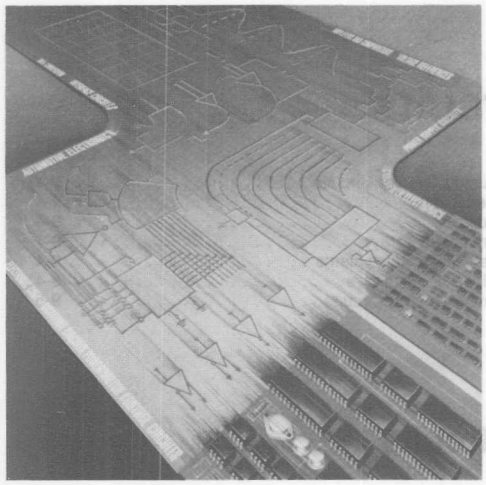
A simple squelch arrangement is provided whereby the meter current flowing through the meter load resistance flips a comparator at about 0.8 Vdc above ground. The signal strength at which this occurs can be adjusted by changing the meter load resistor. The comparator(+) input and output are available to permit control of hysteresis. Good positive action can be obtained for IF input signals of above 20 μVrms. A resistor R from Pin 13 to Pin 12 will provide V_{CC}/R of feedback current. This current can be correlated to an amount of signal strength hysteresis by using Figure 4.

The squelch is internally connected to the data shaper. Squelch causes the data shaper to produce a high (V_{CC}) output.

The data shaper is a complete "floating" comparator, with diodes across its inputs. The outputs of the quadrature detector can be fed directly to either or preferably both inputs of the comparator to produce a squared output swinging from V_{CC} to ground in inverted or non-inverted form.



8



In Brief . . .

. . . reflecting Motorola's continuing commitment to semiconductor products necessary for consumer system designs. This tabulation is arranged to simplify first-order selection of consumer integrated circuit devices that satisfy the primary functions for home entertainment products, including Television, Hi-Fi Audio and AM/FM Radio.

Selector Guide

Entertainment Radio Receiver Circuits 9-2

Video Circuits 9-3

Remote Control Circuits 9-5

Alphanumeric Index 9-6

Related Application Notes 9-6

Data Sheets 9-7

Consumer Electronic Circuits

9

Consumer Electronic Circuits

Entertainment Radio Receiver Circuits
- C-QUAM® AM Stereo Decoders 9-2
- FM Stereo Decoder 9-2
- Audio Amplifiers 9-2
- Audio Attenuators/Controls 9-2

Video Circuits
- Modulators 9-3
- Demodulators 9-3
- Tuning System Circuits 9-4
- Deflection 9-4
- Sound 9-4
- Transistor Arrays 9-4
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- Video IF Amplifiers 9-4

Remote Control Circuits 9-5

Entertainment Radio Receiver Circuits

C-QUAM® AM Stereo Decoders

Function	Features	Suffix/Case	Device
Basic AM Stereo Decoder	Monaural/Stereo AM Detector, Indicator, 6–10 V Operation	P/738	MC13020
Advanced AM Stereo Decoder	Medium Voltage 2–8 V, Decoder and IF Amp	DW/751F	MC13022
AM Front End	Tuning Stabilizer for MC13022	P/738	MC13023
AM Stereo Personal Radio	Complete Low Voltage AM Stereo Receiver	P/724	MC13024
Tuning Stabilizer	Companion for MC13020 for Manual Tuned Receivers	P/648	MC13021
AM Broadcast Receiver	AM Receiver Subsystem — Ideal Companion for MC13020	P/738	MC13041

FM Stereo Decoder

Function	Channel Separation dB Typ	THD % Typ	Stereo/Indicator Lamp Driver mA Max	Features	Suffix/Case	Device
FM Multiplex Stereo Decoder	62	0.1	100	Low Signal Blend for Noise Reduction	—/648	TCA4500A

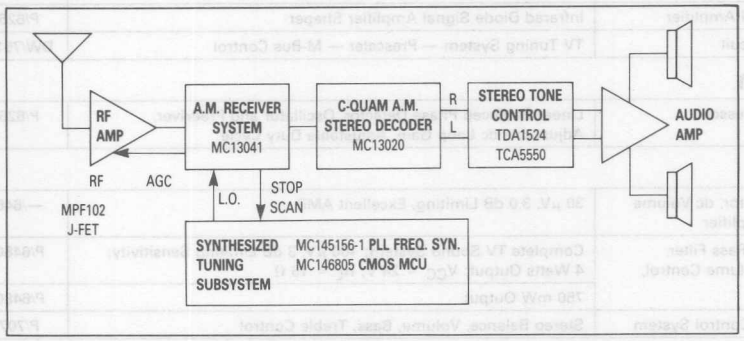
Audio Amplifiers

Function	P_O Watts	V_{CC} Vdc Max	V_{in} @ rated P_O mV Typ	I_D mA Typ	R_L Ohms	Suffix/Case	Type
Mini Watt SOIC Audio Amp	1.0 W	35	80	11	16	D/751	MC13060
Low Power Audio Amp	400 mW	16	—	2.5 mA	8–100	D/751 P/626	MC34119

Audio Attenuators/Controls

Function	V_{CC} Range Vdc	THD %	Tone Control Range dB Typ	Attenuation Range dB Typ	Suffix/Case	Device
Stereo, Volume, Bass, Treble, Balance	8.5–18	0.1 Typ	±14	80	P/707	TCA5550
Stereo, Volume, Bass, Treble, Balance	3–18	0.5 Max	±15	80	P/707	TDA1524

C-QUAM® A.M. Stereo Broadcast Receiver



When AM stereo broadcasting was sanctioned by the F.C.C. in 1982, there were five different systems vying for user approval. Since then C-QUAM® has become the defacto standard in the U.S.A., as the market and broadcasters recognize its performance advantages. It is the legal standard in Canada, Australia and Brazil where A.M. is the dominant radio medium. C-QUAM is available from nearly 50 automobile radio makers and a dozen home receiver builders (for as little as $60 in a basic tuner).

Based on the field-proven C-Quam performance, Motorola has developed a low-cost, high performance C-Quam AM Stereo Decoder chip, with fully compatible, no-compromise mono performance, as the basis for both broadcast and receiving equipment. Additional IC components from Motorola's inventory offer a single supply source for state-of-the-art radio receiver designs. New products cover virtually every type of receiver — home, auto, and personal portable.

Radio Circuits (See Communications Section)

Video Circuits

Modulators

Function	Features	Suffix/Case	Device
TV Modulator (Hi Quality)	RF Oscillator/Modulator, and FM Sound Oscillator/Modulator	P/646	MC1374
Video RGB to PAL/NTSC Encoder	RGB and Sync Inputs, Composite Video Out — PAL/NTSC Switch Selectable	P/738	MC1377
Video Synchronizer	Complete Color TV Video Overlay Synchronizer	P/711	MC1378

Demodulators

Color Processor	PAL/NTSC Input, RGB Output, also RGB Inputs, Plus Fast Blanking Input. Ideal for Text, Graphics, Overlays	P/711	TDA3301 TDA3303
Color Processor	PAL/NTSC Input, RGB Outputs, On-Chip Hue Control	P/724	TDA3330
Color Processor	PAL/NTSC Input, Color Difference Outputs On-Chip Hue Control	P/707	TDA3333

Tuning System

Function	Features	Suffix/Case	Device
Remote Control Amplifier	Infrared Diode Signal Amplifier Shaper	P/626	MC3373
PLL-Tuning Circuit	TV Tuning System — Prescaler — M-Bus Control	DW/751C	MC44802

Deflection

Horizontal Processor	Linear Balanced Phase Detector, Oscillator and Predriver, Adjustable dc Loop Gain, Adjustable Duty Cycle	P/626	MC1391

Sound

Sound IF Detector, dc Volume Control, Preamplifier	30 μV, 3.0 dB Limiting, Excellent AMR	—/646	TBA120C
Sound IF, Low Pass Filter, Detector, dc Volume Control, Preamplifier	Complete TV Sound System; 100 μV, 3 dB Limiting Sensitivity; 4 Watts Output; V_{CC} = 24 V; R_L = 16 Ω	P/648C	TDA3190
	750 mW Output	P/648C	TDA1190
Stereo Sound Control System	Stereo Balance, Volume, Bass, Treble Control	P/707	TCA5550

Transistor Arrays

Function	$I_{C(max)}$ mA	V_{CEO} Volts Max	V_{CBO} Volts Max	V_{EBO} Volts Max	Suffix/Case	Device
One Differentially Connected Pair and Three Isolated Transistors	50	15	20	5.0	P/646 D/751A	MC3346
Dual Independent Differential Amplifiers with Associated Constant Current Transistors	50	15	20	5.0	P/646	CA3054

Television Subsystems

Function	Features	Suffix/Case	Device
MONOMAX — 1-Chip Black and White TV Subsystem	Video IF, Detector, AGC, Video Amplifier, Horizontal Processor, Vertical Processor, and Sync For 525 Line Systems	P/710	MC13001X
	Same as Above Except For 625 Line Systems	P/710	MC13002X
Sound IF, Low Pass Filter, Detector, dc Volume Control, Preamplifier, Power Amplifier	Complete TV Sound System; 100 μV, 3 dB Limiting Sensitivity; 4 Watts Output; V_{CC} = 24 V; R_L = 16 Ω	P/648C	TDA3190
	Same as TDA1190Z Except for 750 mW Output	P/648C	TDA1190
MONOMAX Audio/Vertical Output	High Level 750 mW Audio Output — Vertical Yoke Driver	P/648C	MC13014

Video IF Amplifiers

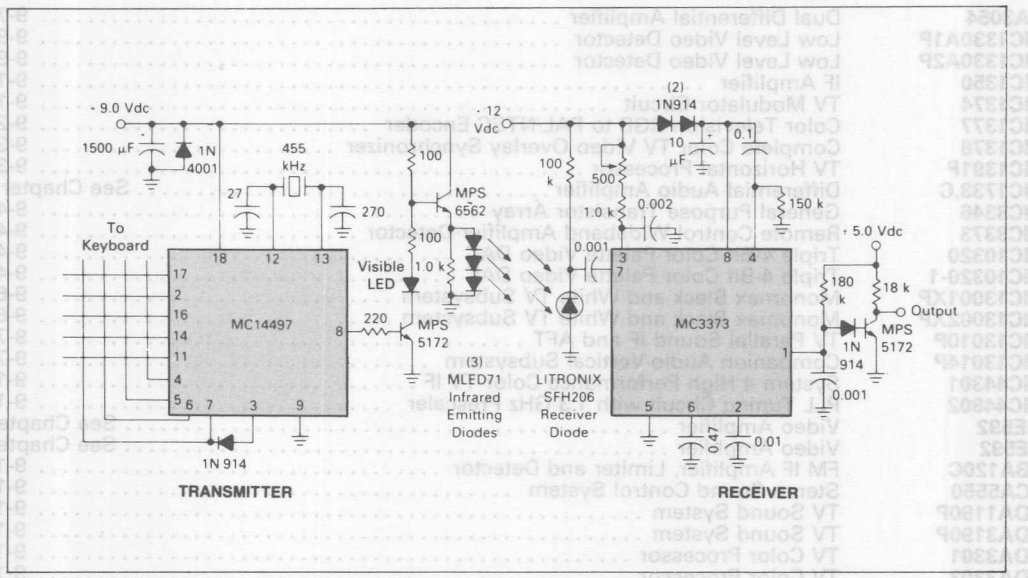
Function	Features	Suffix/Case	Device
1st and 2nd Video IF Amplifier	IF Gain @ 45 MHz = 50 dB typ, AGC Range = 60 dB min	P/626	MC1350
3rd IF, Video Detector, Video Buffer, and AFC Buffer	Low Level Detection, Low Harmonic Generation, Zero Signal dc Output Voltage of 7.0 to 8.2 V	P/626	MC1330A1P
	Same as MC1330A1 Except Zero Signal dc Output Voltage of 7.8 to 9.0 V	P/626	MC1330A2P
SAW Preamp, IF Amplifier, Detector, AGC, AFC	Complete Video IF or Parallel Sound IF System Complete AFT System with Simple Quadrature Detector	P/707	MC13010P
Advanced Video IF	Complete Video/Audio IF System for High Performance Analog TV Receivers	DW/751F	MC44301

Remote Control Circuits

MC3373 Amplifier/Detector (Bipolar), Case 626
MC14497 Transmitter (CMOS), Case 707

The MC3373 remote control receiver is specifically designed for infra-red link systems where high sensitivity and good noise immunity are critical. The MC3373 incorporates a high gain detector diode preamp driving an envelope detector and data wave shaper for accurate data recovery. Provision is also made to use an external L-C tank circuit at the carrier frequency, normally 30 to 60 kHz, for extended range low noise systems. Applications include TV remote control, short range data links (up to several hundred feet), door openers and security systems. The MC14497 is an ideal companion transmitter, where a simple D.T.M.F. like key-pad control is desired. The Motorola discrete opto division also has several high sensitivity detectors and emitters which match up well to the MC1373 system.

Functional Block Diagram of Remote Control System



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ENTERTAINMENT RADIO RECEIVER CIRCUITS

Device	Function	Page
MC13020P	C-QUAM® AM Stereo Decoder	9-84
MC13021	Motorola C-QUAM® AM Stereo Tuning Stabilizer	9-89
MC13022	Advanced Medium Voltage AM Stereo Decoder	9-91
MC13023	C-QUAM® AM Receiver Front End and Tuner Stabilizer	9-95
MC13024	Low Voltage Motorola C-QUAM® AM Stereo Receiver	9-101
MC13041	AM Receiver Subsystem	9-104
MC13055	Wideband FSK Receiver	See Chapter 8
MC13060	Mini-Watt Audio Output	9-110
MC34119	Low Power Audio Amplifier	9-114
TCA4500A	FM Stereo Demodulator	9-142
TCA5550	Stereo Sound Control System	9-149
TDA1524A	Stereo Tone Control System	9-156

VIDEO CIRCUITS

Device	Function	Page
CA3054	Dual Differential Amplifier	9-7
MC1330A1P	Low Level Video Detector	9-9
MC1330A2P	Low Level Video Detector	9-9
MC1350	IF Amplifier	9-15
MC1374	TV Modulator Circuit	9-19
MC1377	Color Television RGB to PAL/NTSC Encoder	9-27
MC1378	Complete Color TV Video Overlay Synchronizer	9-31
MC1391P	TV Horizontal Processor	9-35
MC1733,C	Differential Audio Amplifier	See Chapter 2
MC3346	General Purpose Transistor Array	9-40
MC3373	Remote Control Wideband Amplifier-Detector	9-43
MC10320	Triple 4-Bit Color Palette Video DAC	9-47
MC10320-1	Triple 4-Bit Color Palette Video DAC	9-47
MC13001XP	Monomax Black and White TV Subsystem	9-64
MC13002XP	Monomax Black and White TV Subsystem	9-64
MC13010P	TV Parallel Sound IF and AFT	9-73
MC13014P	Companion Audio/Vertical Subsystem	9-78
MC44301	System 4 High Performance Color TV IF	9-123
MC44802	PLL Tuning Circuit with 1.3 GHz Prescaler	9-129
NE592	Video Amplifier	See Chapter 2
SE592	Video Amplifier	See Chapter 2
TBA120C	FM IF Amplifier, Limiter and Detector	9-137
TCA5550	Stereo Sound Control System	9-149
TDA1190P	TV Sound System	9-153
TDA3190P	TV Sound System	9-153
TDA3301	TV Color Processor	9-161
TDA3303	TV Color Processor	9-161
TDA3330	TV Color Processor	9-175
TDA3333	TV Color Difference Demodulator	9-183

REMOTE CONTROL CIRCUIT

Device	Function	Page
MC3373	Remote Control Wideband Amplifier-Detector	9-43

RELATED APPLICATION NOTES

Application Note	Title	Related Device
AN545A	Television Video IF Amplifier Using Integrated Circuits	MC1350
AN829	Application of the MC1374 TV Modulator	MC1374
AN932	Application of the MC1377 Color Encoder	MC1377
AN879	Monomax-Application of the MC13001 Monochrome TV IC	MC13001
ANHK07	A High Performance, Manual-Tuned AM Stereo Receiver for Automotive Application Using Motorola ICs: MC13020, MC13021 and MC13041	MC13020,21 MC13041

MOTOROLA

CA3054

DUAL INDEPENDENT DIFFERENTIAL AMPLIFIER

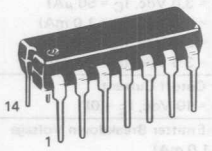
The CA3054 consists of two independent differential amplifiers with associated constant-current transistors on a common monolithic substrate. The six NPN transistors which comprise the amplifiers are general purpose devices useful from dc to 120 MHz.

The monolithic construction of the CA3054 provides close electrical and thermal matching of the amplifiers which makes this device particularly useful in dual channel applications where matched performance of the two channels is required.

- Two differential amplifiers on a common substrate
- Independently accessible inputs and outputs
- Maximum input offset voltage – ±5 mV

GENERAL PURPOSE TRANSISTOR ARRAY

SILICON MONOLITHIC INTEGRATED CIRCUIT



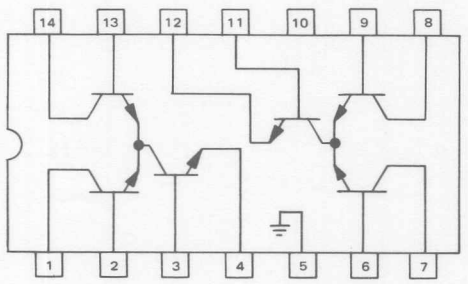
P SUFFIX
PLASTIC PACKAGE
CASE 646-06

9

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	15	Vdc
Collector-Base Voltage	V_{CBO}	20	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector-Substrate Voltage	V_{CIO}	20	Vdc
Collector Current – Continuous	I_C	50	mAdc
Junction Temperature	T_J	150	°C
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

PIN CONNECTIONS



Pin 5 is connected to substrate and must remain at the lowest circuit potential

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
STATIC CHARACTERISTICS FOR EACH DIFFERENTIAL AMPLIFIER					
Input Offset Voltage (V_{CB} = 3.0 Vdc)	V_{IO}	–	–	5.0	mV
Input Offset Current (V_{CB} = 3.0 Vdc)	I_{IO}	–	–	2.0	μA
Input Bias Current (V_{CB} = 3.0 Vdc)	I_{IB}	–	–	24	μA
STATIC CHARACTERISTICS FOR EACH TRANSISTOR					
Base-Emitter Voltage	V_{BE}				Vdc
(V_{CB} = 3.0 Vdc, I_C = 50 μA)		–	–	0.70	
(V_{CB} = 3.0 Vdc, I_C = 1.0 mA)		–	–	0.80	
(V_{CB} = 3.0 Vdc, I_C = 3.0 mA)		–	–	0.85	
(V_{CB} = 3.0 Vdc, I_C = 10 mA)		–	–	0.90	
Collector Cutoff Current (V_{CB} = 10 Vdc, I_E = 0)	I_{CBO}	–	–	100	nA
Collector-Emitter Breakdown Voltage (I_C = 1.0 mA)	$V_{(BR)CEO}$	15	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 10 μA)	$V_{(BR)CBO}$	20	–	–	Vdc
Collector-Substrate Breakdown Voltage (I_C = 10 μA)	$V_{(BR)CIO}$	20	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μA)	$V_{(BR)EBO}$	5.0	–	–	Vdc

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MC1330A1P
MC1330A2P

ORDERING INFORMATION

Device	Temperature Range	Package
MC1330A1P	0°C to +70°C	Plastic DIP
MC1330A2P	0°C to +70°C	Plastic DIP

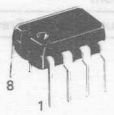
LOW LEVEL VIDEO DETECTOR

. . . an integrated circuit featuring very linear video characteristics and wide bandwidth. Designed for color and monochrome television receivers, replacing the third IF, detector, video buffer and AFC buffer.

- Conversion Gain – 33 dB (Typ)
- Excellent Differential Phase and Gain
- High Rejection of IF Carrier Feedthrough
- High Video Output – 8.0 V(p-p)
- Fully Balanced Detector
- Output Temperature Compensated
- Improved Versions of the MC1330P

LOW LEVEL VIDEO DETECTOR

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 626-05

CIRCUIT DESCRIPTION

The MC1330A video detector is a fully balanced multiplier detector circuit that has linear amplitude and phase characteristics. The signal is divided into two channels, one a linear amplifier and the other a limiting amplifier that provides the switching carrier for the detector.

The switching carrier has a buffered output for use in providing the AFT function.

The video amplifier output is an improved design that reduces the differential gain and phase distortion associated with previous video output systems. The output is wide band, > 8.0 MHz, with normal negative polarity. A separate narrow bandwidth, positive video output is also provided.

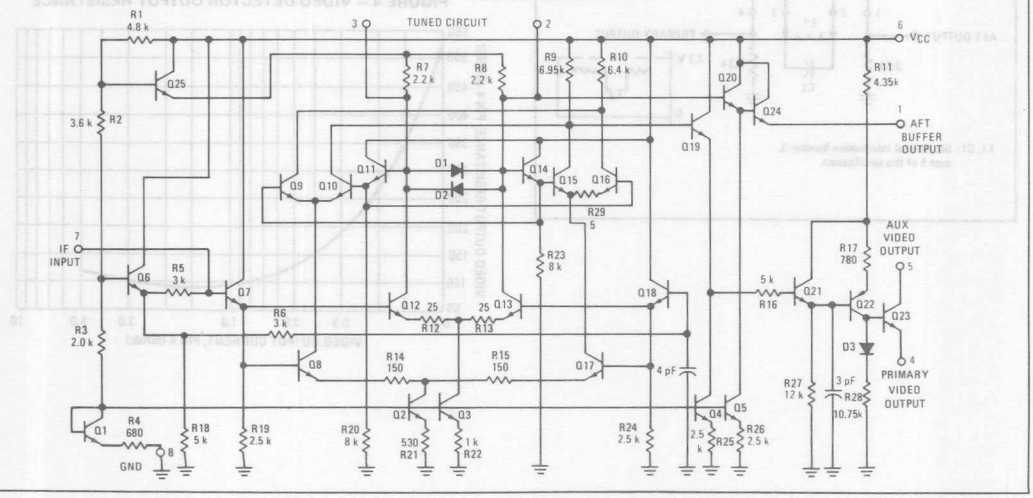
OUTPUT VOLTAGE SELECTION

The MC1330A1P is identical to the MC1330A2P with the following exception:

	ZERO SIGNAL DC OUTPUT VOLTAGE
MC1330A1P	7.0 to 8.2 Vdc
MC1330A2P	7.8 to 9.0 Vdc

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FIGURE 1 – CIRCUIT SCHEMATIC



Rating	Value	Unit
Power Supply Voltage	24	Vdc
DC Video Output Current	5.0	mAdc
DC AFT Output Current	2.0	mAdc
Junction Temperature	+150	°C
Operating Ambient Temperature Range	0 to +70	°C
Storage Temperature Range	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +20 Vdc, Q = 40, fc = 45.75 MHz, T_A = +25°C unless otherwise noted)

Characteristic		Pin	Min	Typ	Max	Unit
Zero Signal dc Output Voltage	MC1330A1P	4	7.0	–	8.2	Vdc
	MC1330A2P	4	7.8	–	9.0	Vdc
Supply Current		5, 6	11	17.5	20	mA
Maximum Signal dc Output Voltage		4	–	0	0.5	Vdc
Conversion Gain for 1.0 Vp-p Output (30% Modulation)		7	25	36	65	mVrms
AFT Buffer Output at Carrier Frequency		1	300	475	650	mVp-p

FIGURE 2 – TEST FIXTURE CIRCUIT

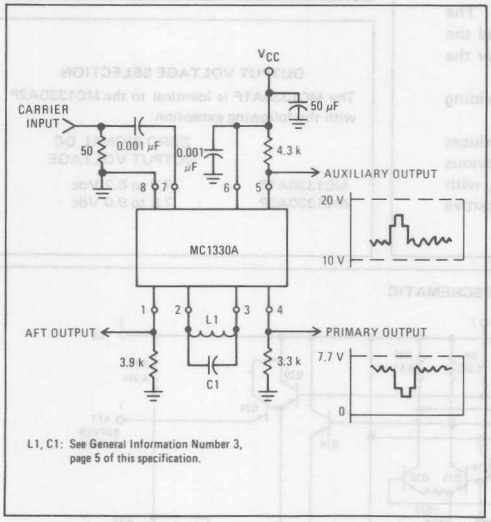


FIGURE 3 – INPUT ADMITTANCE

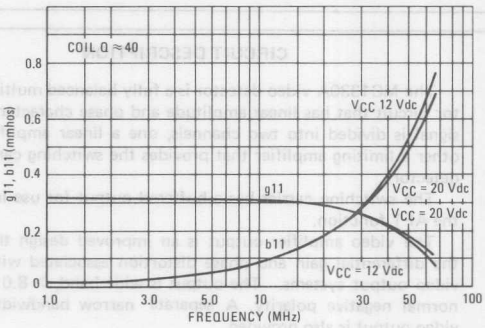
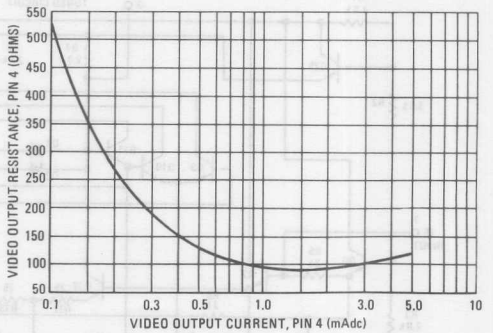


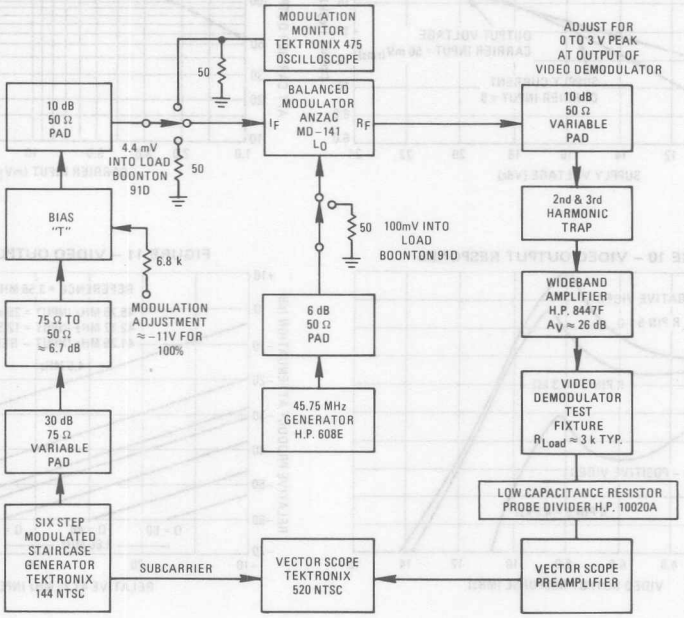
FIGURE 4 – VIDEO DETECTOR OUTPUT RESISTANCE



DESIGN CHARACTERISTICS (V_{CC} = +20 Vdc, Q = 40, f_c = 45.75 MHz, T_A = +25°C unless otherwise noted)

Characteristic		Pin	Typ	Unit
Input Resistance Input Capacitance		7 7	4.9 1.5	kΩ pF
Internal Resistance (Across Tuned Circuit) Internal Capacitance (Across Tuned Circuit)		2, 3 2, 3	4.4 1.0	kΩ pF
Negative Video Output Bandwidth (Figure 10) Positive Video Output Bandwidth (Figure 10)		4 5	10.8 2.2	MHz MHz
Differential Phase @ 3.58 MHz, 100% Modulated Staircase, 3.0 Vp-p Detected Video Pin 5 Tied to Pin 6 Differential Gain @ 3.58 MHz, 100% Modulated Staircase, 3.0 Vp-p Detected Video Pin 5 Tied to Pin 6		4 4	7.0 4.0	Degrees %
Differential Phase @ 3.58 MHz, 100% Modulated Staircase, 3.0 Vp-p Detected Video, R Pin 5 = 4.3 kΩ Differential Gain @ 3.58 MHz, 100% Modulated Staircase, 3.0 Vp-p Detected Video, R Pin 5 = 4.3 kΩ		4 4	8.0 6.0	Degrees %
920 kHz Beat Output (dB Below 100% Modulated Video, See Figure 11) 45.75 MHz = Reference 42.17 MHz = – 6 dB 41.25 MHz = –20 dB		4	–38	dB
Video Output Resistance @ 1 MHz, 2 mA		4	94	Ω
Input Overload (Carrier Level at Input to Caused Detector Output, Pin 4, To Go Positive 0.1 Vdc From Ground.)	V_{CC} = 12 Vdc V_{CC} = 15 Vdc V_{CC} = 20 Vdc V_{CC} = 24 Vdc	7	2.0 2.6 3.6 4.6	Volts
Power Supply Voltage Range		5	10 to 24	Volts

FIGURE 5 –DIFFERENTIAL PHASE AND GAIN TEST SET UP



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TYPICAL CHARACTERISTICS

(V_{CC} = +20 Vdc, T_A = +25°C Unless Otherwise Noted)

FIGURE 6 – OUTPUT VOLTAGE TRANSFER FUNCTION

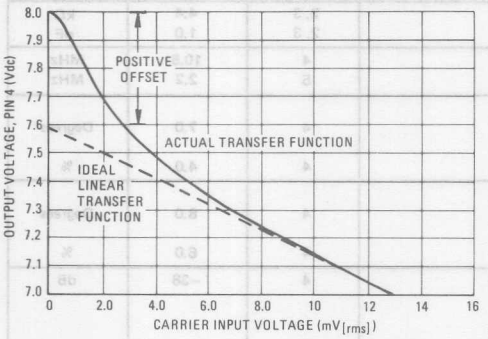


FIGURE 7 – OUTPUT VOLTAGE TRANSFER FUNCTION

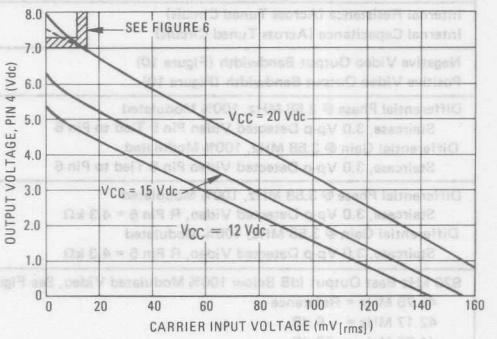


FIGURE 8 – OUTPUT VOLTAGE, SUPPLY CURRENT

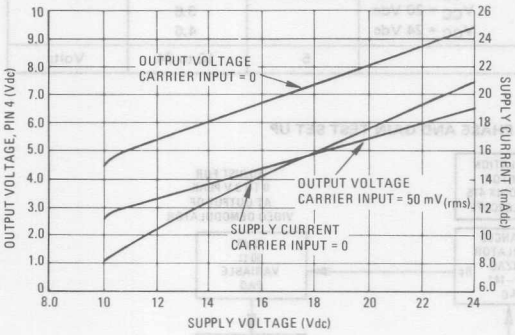


FIGURE 9 – AFT LIMITING

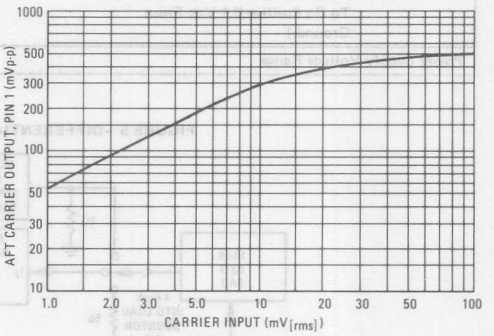


FIGURE 10 – VIDEO OUTPUT RESPONSE

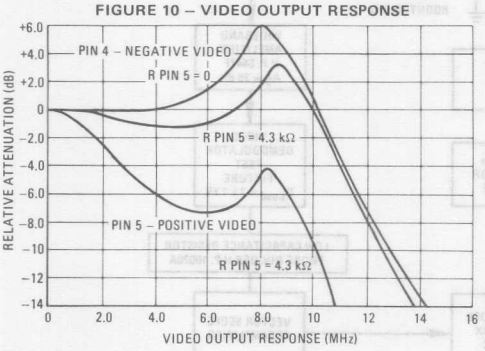
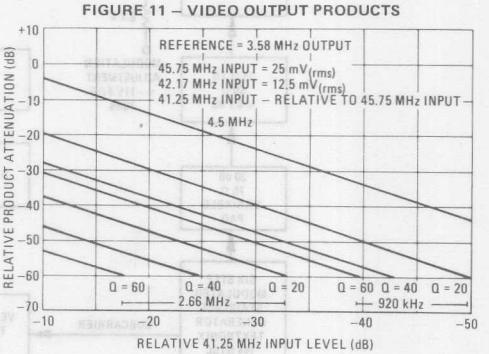


FIGURE 11 – VIDEO OUTPUT PRODUCTS



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TV-IF Amplifier Information

A very compact high performance IF amplifier constructed as shown in Figure 14 minimizes the number of overall components and alignment adjustments. It can be readily combined with normal tuners and input tuning-trapping circuitry to provide the performance demanded of high quality receivers. This configuration will provide approximately 93 dB voltage gain and can accomodate the usual low impedance input network or, if desired, can take advantage of an impedance step-up from tuner to MC1349P input.

The burden of selectivity, formerly found between the third IF and detector, must now be placed at the interstage. The nominal 3 volt peak-to-peak output can be varied from 0 to 7.0 V with excellent linearity and freedom from spurious output products.

Alignment is most easily accomplished with an AM generator, set at a carrier frequency of 45.75 MHz, modulated with a video frequency sweep. This provides the proper realistic conditions necessary to operate to low-level detector (LLD). The detector tank is first adjusted for maximum detected dc (with a CW input), next, the video sweep modulation is applied and the interstage and input circuits aligned, step by step, as in a standard IF amplifier.

Note: A normal IF sweep generator, essentially an FM generator, will not serve properly without modification. The LLD tank attempts to "follow" the sweep input frequency, and results in variations of switching amplitude in the detector. Hence, the apparent overall response becomes modified by the response of the LLD tank, which a real signal doesn't do.

This effect can be prevented by resistively adding a 45.75 MHz CW signal to the output of the sweep generator approximately 3 dB greater than the sweep amplitude. See Figures 12 and 13 below. For a more detailed description of the MC1330AP see application note AN-545.

MC1330A General Information

The MC1330A offers the designer a new approach to an old problem. Now linear detection can be performed at much lower power signal levels than possible with a detector diode.

Offering a number of distinct advantages, its easy implementation should meet with ready acceptance for television designs. Some specific features and information on systems design with this device are given below:

1. The device provides excellent linearity of output versus input, as shown in Figures 6 and 7. These graphs also show that video peak-to-peak amplitude (ac) does not change with supply voltage variation. (Slopes are parallel. Visualize a given variation of input CW and use the figure as a transfer function.)

2. The dc output level does change linearly with supply voltage shown in Figure 8. This can be accommodated by regulating the supply or by referencing the subsequent video amplifier to the same power supply.

3. The choice of Q for the tuned circuit of pins 2 and 3 is not critical. The higher the Q, the better the rejection of 920 kHz products but the more critical the tuning accuracy required. See Figure 11. Values of Q from 20 to 50 are recommended. (Note the internal resistance.)

4. A video output with positive-going sync is available at pin 5 if required. This signal has a higher output impedance than pin 4 so it must be handled with greater care. If not used, pin 5 may be connected directly to the supply voltage (pin 6).The video response will be altered somewhat. See Figure 10.

5. An AFT output (pin1) provides 460 mV of IF carrier output, sufficient voltage to drive an AFT ratio detector, with only one additional stage.

6. AGC lockout can occur if the input signal presented in the MC1330A is greater than that shown in the input overload section of the design characteristics shown on Page 3. If these values are exceeded, the turns ratio between the primary and secondary of T_1 should be increased. Another solution to the problem is to use an input clamp diode D_1 shown in Figure 14.

7. The total I.F. noise figure at high gain reductions can be improved by reflecting $\approx$ 1 k source impedance to the input of the MC1330AP. This will cause some loss in overall IF voltage gain.

FIGURE 12 — BANDPASS DISPLAYED BY CONVENTIONAL SWEEP

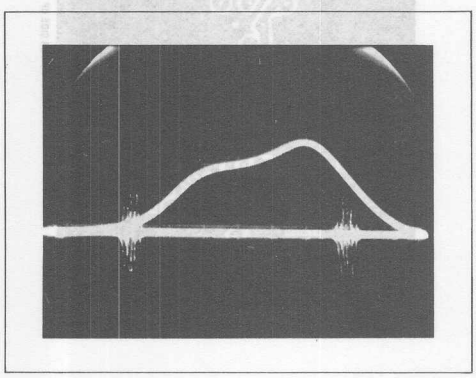
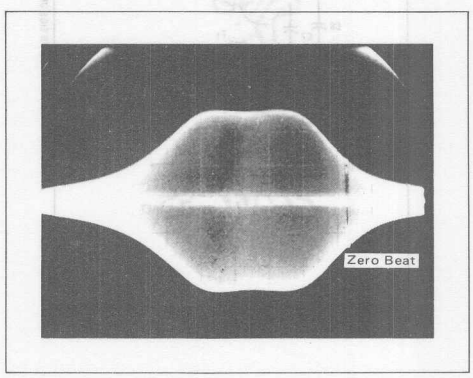
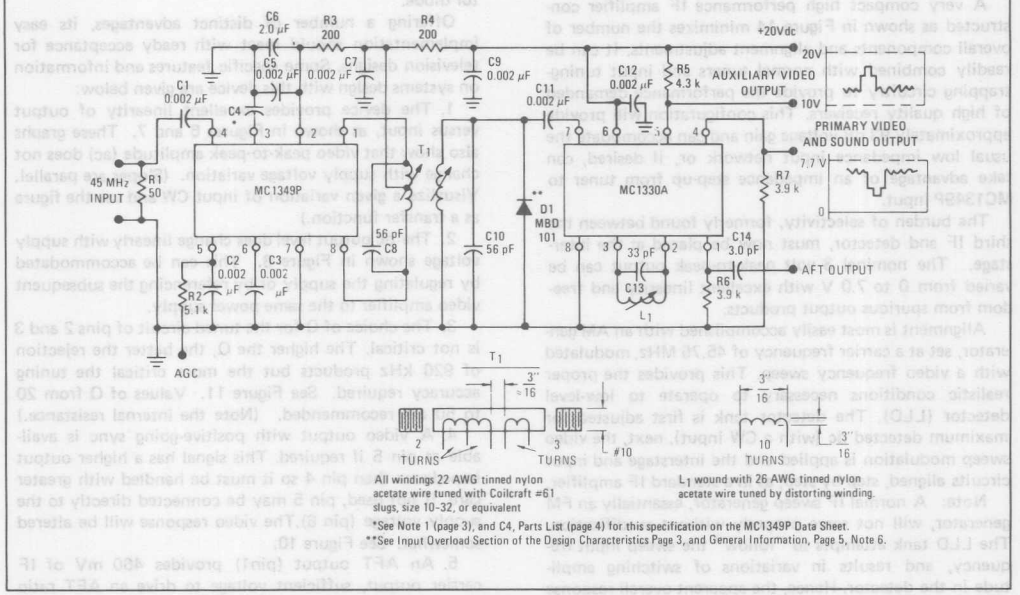


FIGURE 13 — BANDPASS DISPLAY WITH THE ADDITION OF CARRIER INJECTION



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FIGURE 14 – TYPICAL APPLICATION OF MC1349P VIDEO IF AMPLIFIER and MC1330A LOW-LEVEL VIDEO DETECTOR CIRCUIT



All windings 22 AWG tinned nylon acetate wire tuned with Coilcraft #61 slugs, size 10-32, or equivalent

L_1 wound with 26 AWG tinned nylon acetate wire tuned by distorting winding.

*See Note 1 (page 3), and C4, Parts List (page 4) for this specification on the MC1349P Data Sheet.

**See Input Overload Section of the Design Characteristics Page 3, and General Information, Page 5, Note 6.

FIGURE 15 – PRINTED CIRCUIT BOARD PARTS LAYOUT

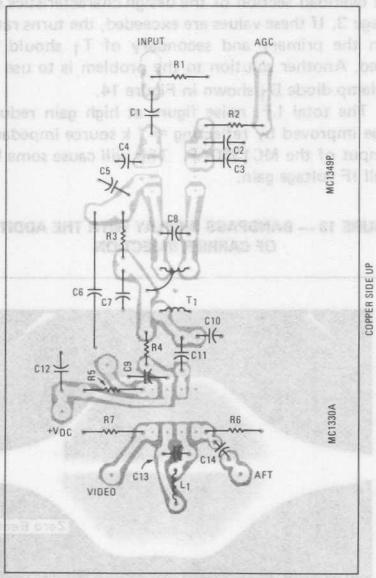
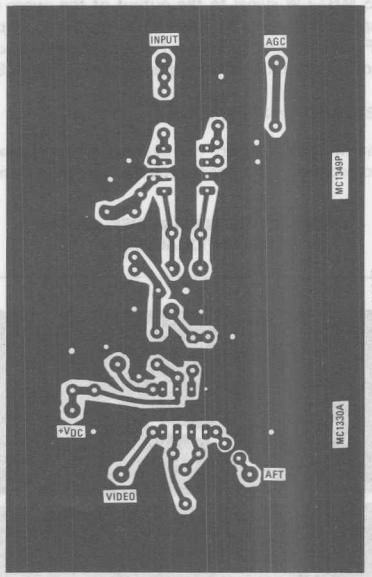


FIGURE 16 – PRINTED CIRCUIT BOARD LAYOUT



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MOTOROLA

MC1350

IF AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

MONOLITHIC IF AMPLIFIER

. . . an integrated circuit featuring wide range AGC for use as an IF amplifier in radio and TV over the temperature range 0 to +75°C. The MC1352 is similar in design but has a keyed-AGC amplifier as an integral part of the same chip.

- Power Gain — 50 dB Typ at 45 MHz
  — 48 dB Typ at 58 MHz
- AGC Range — 60 dB Min, dc to 45 MHz
- Nearly Constant Input and Output Admittance Over the Entire AGC Range
- y_{21} Constant (−3.0 dB) to 90 MHz
- Low Reverse Transfer Admittance — << 1.0 μmho Typ
- 12-Volt Operation, Single-Polarity Power Supply



P SUFFIX
PLASTIC PACKAGE
CASE 626-05



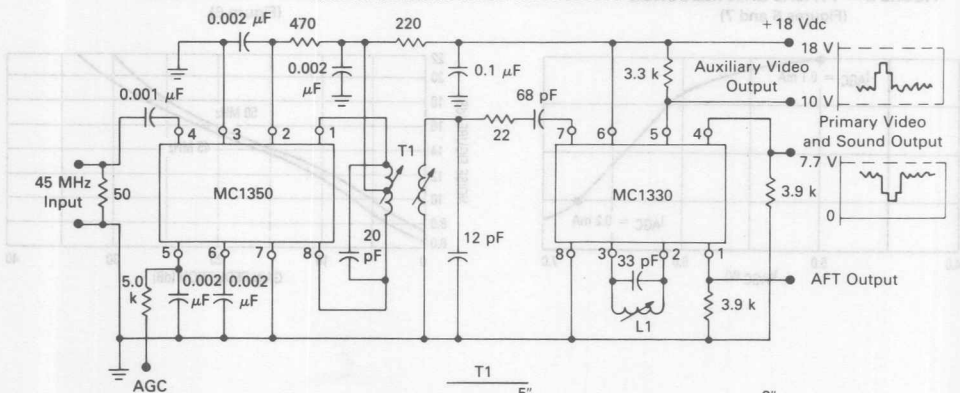
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PLASTIC PACKAGE
CASE 751-02
SO-8

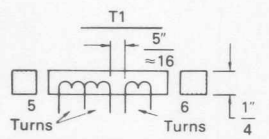
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+	+18	Vdc
Output Supply Voltage	V_1, V_8	+18	Vdc
AGC Supply Voltage	V_{AGC}	V^+	Vdc
Differential Input Voltage	V_{in}	5.0	Vdc
Power Dissipation (Package Limitation) Plastic Package Derate above 25°C	P_D	 625 5.0	 mW mW/°C
Operating Temperature Range	T_A	0 to +75	°C

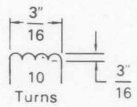
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FIGURE 1 — TYPICAL MC1350 VIDEO IF AMPLIFIER AND MC1330 LOW-LEVEL VIDEO DETECTOR CIRCUIT





All windings #30 AWG tinned nylon acetate wire tuned with Carbonyl E or J slugs.



L1 wound with #26 AWG tinned nylon acetate wire tuned by distorting winding.

ELECTRICAL CHARACTERISTICS (V^+ = +12 Vdc; T_A = +25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
AGC Range, 45 MHz (5.0 V to 7.0 V) (Figure 1)			60	68	—	dB
Power Gain (Pin 5 grounded via a 5.1 kΩ resistor)		A_p				dB
f = 58 MHz, BW = 4.5 MHz	See Figure 6(a)		—	48	—	
f = 45 MHz, BW = 4.5 MHz	See Figure 6(a),(b)		46	50	—	
f = 10.7 MHz, BW = 350 kHz	See Figure 7		—	58	—	
f = 455 kHz, BW = 20 kHz			—	62	—	
Maximum Differential Voltage Swing		V_o				V_{p-p}
0 dB AGC			—	20	—	
−30 dB AGC			—	8.0	—	
Output Stage Current (Pins 1 and 8)		$I_1 + I_8$	—	5.6	—	mA
Total Supply Current (Pins 1, 2 and 8)		I_S	—	14	17	mAdc
Power Dissipation		P_D	—	168	204	mW

DESIGN PARAMETERS, Typical Values (V^+ = +12 Vdc, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Frequency 455 kHz	10.7 MHz	45 MHz	58 MHz	Unit
Single-Ended Input Admittance	g_{11}	0.31	0.36	0.39	0.5	mmhos
	b_{11}	0.022	0.50	2.30	2.75	
Input Admittance Variations with AGC (0 to 60 dB)	Δg_{11}	—	—	60	—	μmhos
	Δb_{11}	—	—	0	—	
Differential Output Admittance	g_{22}	4.0	4.4	30	60	μmhos
	b_{22}	3.0	110	390	510	
Output Admittance Variations with AGC (0 to 60 dB)	Δg_{22}	—	—	4.0	—	μmhos
	Δb_{22}	—	—	90	—	
Reverse Transfer Admittance (Magnitude)	$\lvert y_{12}\rvert$	<<1.0	<<1.0	<<1.0	<<1.0	μmho
Forward Transfer Admittance						
Magnitude	$\lvert y_{21}\rvert$	160	160	200	180	mmhos
Angle (0 dB AGC)	$< y_{21}$	−5.0	−20	−80	−105	degrees
Angle (−30 dB AGC)	$< y_{21}$	−3.0	−18	−69	−90	degrees
Single-Ended Input Capacitance	C_{in}	7.2	7.2	7.4	7.6	pF
Differential Output Capacitance	C_o	1.2	1.2	1.3	1.6	pF

9

FIGURE 2 — TYPICAL GAIN REDUCTION
(Figures 6 and 7)

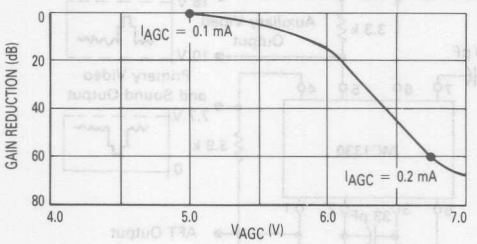
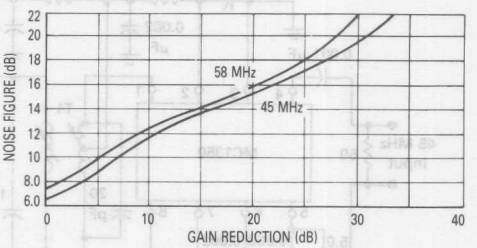


FIGURE 3 — NOISE FIGURE
(Figure 6)



GENERAL OPERATING INFORMATION

The input amplifiers (Q1 and Q2) operate at constant emitter currents so that input impedance remains independent of AGC action. Input signals may be applied single-ended or differentially (for ac) with identical results. Terminals 4 and 6 may be driven from a transformer, but a dc path from either terminal to ground is not permitted.

AGC action occurs as a result of an increasing voltage on the base of Q4 and Q5 causing these transistors to conduct more heavily thereby shunting signal current from the interstage amplifiers Q3 and Q6. The output amplifiers are supplied from an active current source to maintain constant quiescent bias thereby holding output admittance nearly constant. Collector voltage for the output amplifier must be supplied through a center-tapped tuning coil to Pins 1 and 8. The 12-volt supply (V^+) at Pin 2 may be used for this purpose, but output admittance remains more nearly constant if a separate 15-volt supply (V^{++}) is used, because the base voltage on the output amplifier varies with AGC bias.

FIGURE 4 — CIRCUIT SCHEMATIC

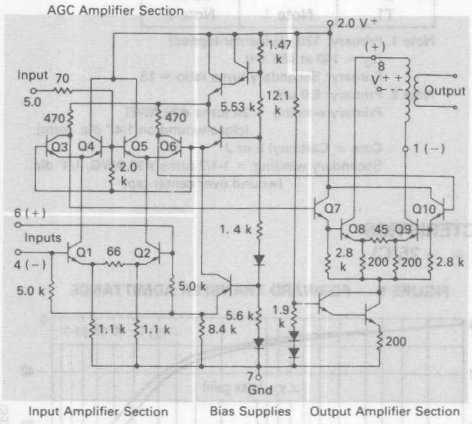


FIGURE 5 — TEST CIRCUIT RESPONSE CURVE (45 and 58 MHz)

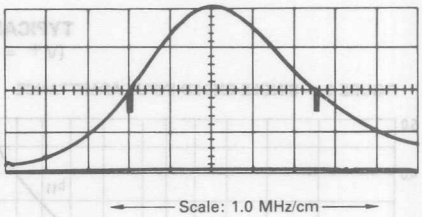
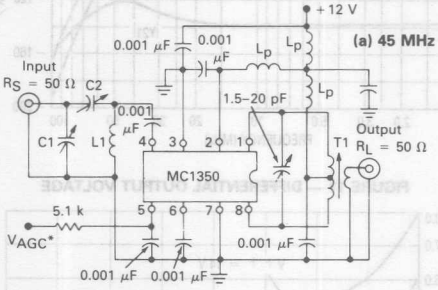


FIGURE 6 — POWER GAIN, AGC AND NOISE FIGURE TEST CIRCUITS

(a) 45 MHz and 58 MHz

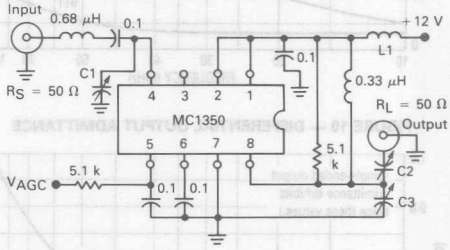


*Connect to ground for maximum power gain test. All power-supply chokes (L_p), are self-resonant at input frequency. $L_p \geq 20$ kΩ
See Figure 5 for frequency response curve.

L1 @ 45 MHz = 7 1/4 Turns on a 1/4" coil form.
@ 58 MHz = 6 Turns on a 1/4" coil form
T1 Primary Winding = 18 Turns on a 1/4" coil form, center-tapped, #26 AWG
Secondary Winding = 2 Turns centered over Primary Winding @ 45 MHz
= 1 Turn @ 58 MHz
Slug = Carbonyl E or J

	45 MHz		58 MHz	
L1	0.4 μH	Q ≥ 100	0.3 μH	Q ≥ 100
T1	1.3–3.4 μH	Q ≥ 100 @ 2.0 μH	1.2–3.8 μH	Q ≥ 100 @ 2.0 μH
C1	50–160 pF		8–60 pF	
C2	8–60 pF		3–35 pF	

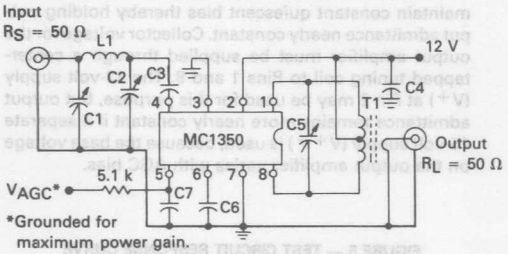
(b) Alternate 45 MHz



L1	Ferrite Core 14 Turns 28 S.W.G
C1	5–25 pF
C2	5–25 pF
C3	5–25 pF

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FIGURE 7 — POWER GAIN AND AGC TEST CIRCUIT (455 kHz and 10.7 MHz)



Component	Frequency 455 kHz	Frequency 10.7 MHz
C1	—	80–450 pF
C2	—	5.0–80 pF
C3	0.05 μF	0.001 μF
C4	0.05 μF	0.05 μF
C5	0.001 μF	36 pF
C6	0.05 μF	0.05 μF
C7	0.05 μF	0.05 μF
L1	—	4.6 μH
T1	Note 1	Note 2

Note 1. Primary: 120 μH (center-tapped)
Q_u = 140 at 455 kHz
Primary: Secondary turns ratio ≈ 13

Note 2. Primary: 6.0 μH
Primary winding = 24 turns #36 AWG (close-wound on 1/4 " dia. form)
Core = Carbonyl E or J
Secondary winding = 1-1/2 turns #36 AWG, 1/4" dia. (wound over center-tap)

TYPICAL CHARACTERISTICS
(V^+ = 12 V, T_A = +25°C)

FIGURE 8 — SINGLE-ENDED INPUT ADMITTANCE

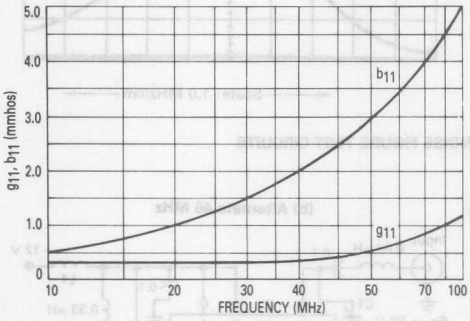


FIGURE 9 — FORWARD TRANSFER ADMITTANCE

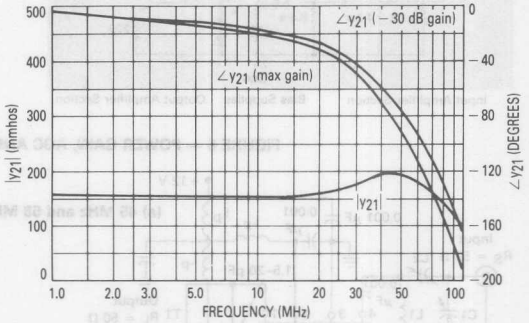


FIGURE 10 — DIFFERENTIAL OUTPUT ADMITTANCE

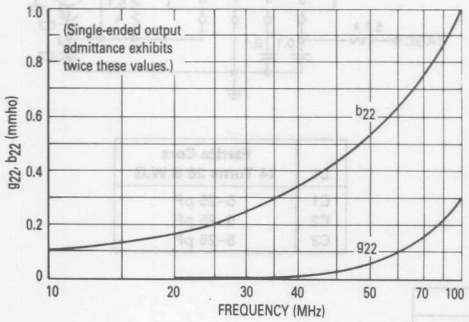
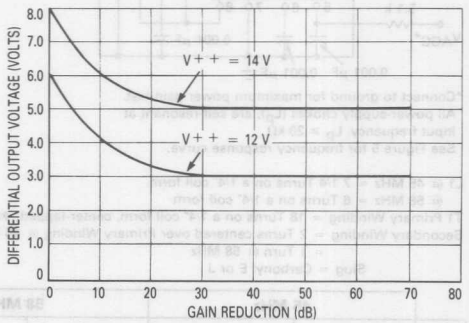


FIGURE 11 — DIFFERENTIAL OUTPUT VOLTAGE



For additional information see "A High-Performance Monolithic IF Amplifier Incorporating Electronic Gain Control," by W. R. Davis and J. E. Solomon, IEEE Journal on Solid State Circuits, December 1968.

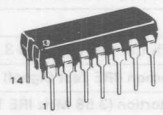
TV MODULATOR CIRCUIT

The MC1374 includes an FM audio modulator, sound carrier oscillator, RF oscillator, and RF dual input modulator. It is designed to generate a TV signal from audio and video inputs. The MC1374's wide dynamic range and low distortion audio make it particularly well suited for applications such as video tape recorders, video disc players, T.V. games and subscription decoders.

- Single Supply, 5 V to 12 V
- Channel 3 or 4 Operation
- Variable Gain RF Modulator
- Wide Dynamic Range
- Low Intermodulation Distortion
- Positive or Negative Sync
- Low Audio Distortion
- Few External Components

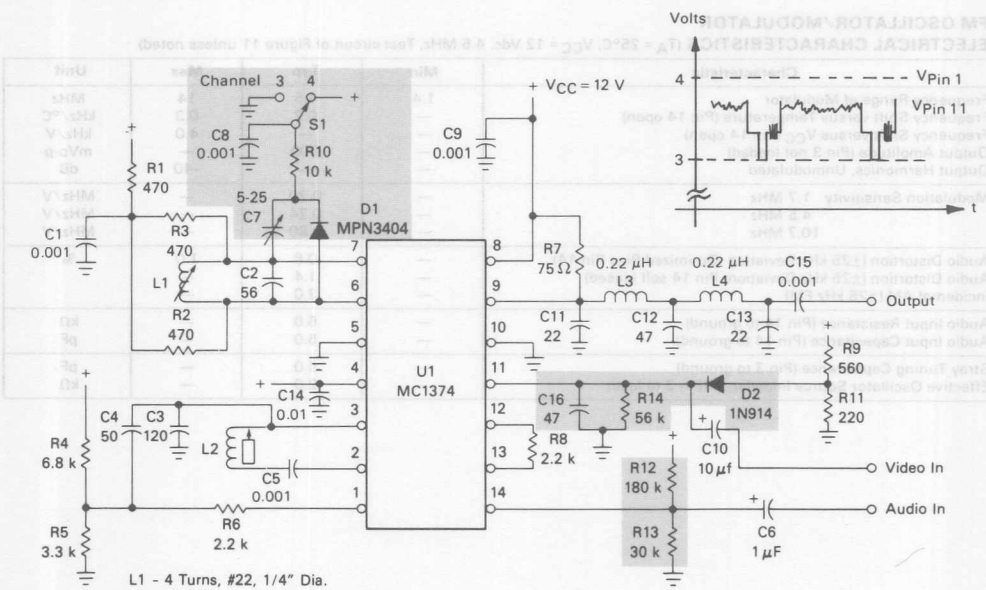
TV MODULATOR CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 646-06

FIGURE 1 — TYPICAL APPLICATION



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MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Value	Unit
Supply Voltage	14	Vdc
Operating Ambient Temperature Range	0 to +70	°C
Storage Temperature Range	-65 to +150	°C
Junction Temperature	150	°C
Power Dissipation, Package Derate above 25°C	1.25 10 mW/°C	Watts

AM OSCILLATOR/MODULATOR
ELECTRICAL CHARACTERISTICS (V_{CC} = 12 Vdc, T_A = 25°C, f_c = 67.25 MHz, Figure 4 circuit, unless noted)

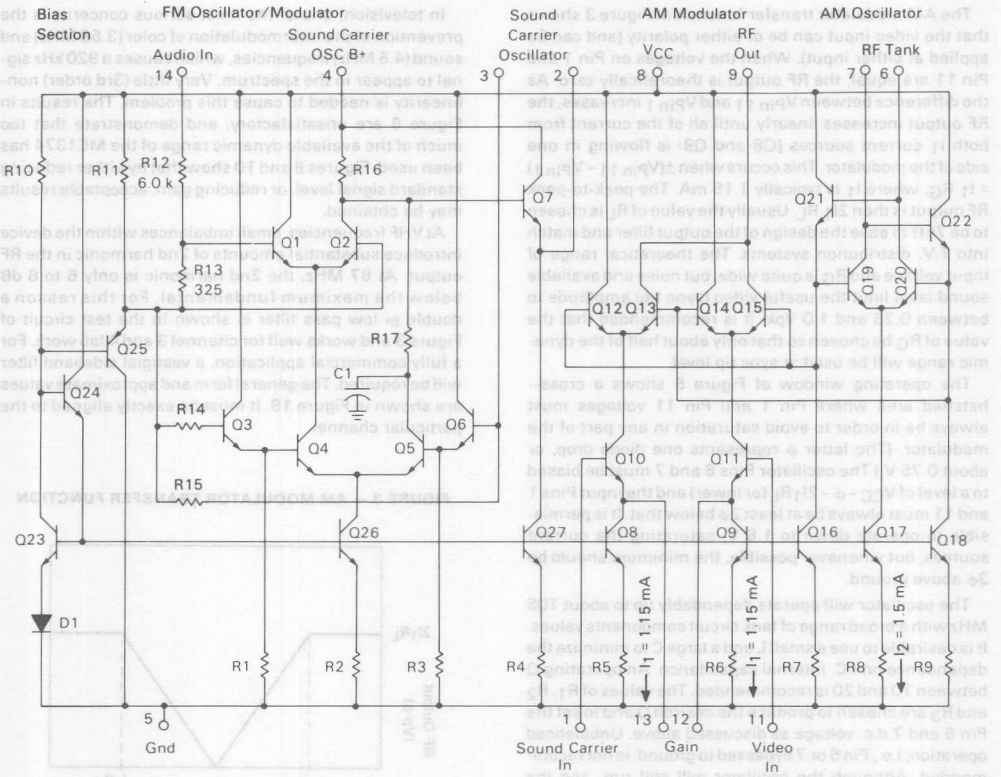
Characteristic	Min	Typ	Max	Unit
Operating Supply Voltage	5.0	12	12	V
Supply Current (Figure 1)	—	13	—	mA
Video Input Dynamic Range (Sync Amplitude)	0.25	1.0	1.0	V Pk
RF Output (Pin 9, R7 = 75 Ω, No External Load)	—	170	—	mV pp
Carrier Suppression	36	40	—	dB
Linearity (75% to 12.5% Carrier, 15 kHz to 3.58 MHz)	—	—	2.0	%
Differential Gain Distortion (IRE Test Signal)	5.0	7.0	10	%
Differential Phase Distortion (3.58 MHz IRE Test Signal)	—	1.5	2.0	Degrees
920 kHz Beat (3.58 MHz @ 30%, 4.5 MHz @ 25%)	—	-57	—	dB
Video Bandwidth (75 Ω Input Source)	30	—	—	MHz
Oscillator Frequency Range	—	105	—	MHz
Internal Resistance across Tank (Pin 6 to Pin 7) Internal Capacitance across Tank (Pin 6 to Pin 7)	— —	1.8 4.0	— —	kΩ pF

FM OSCILLATOR/MODULATOR
ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 12 Vdc, 4.5 MHz, Test circuit of Figure 11 unless noted)

Characteristic	Min	Typ	Max	Unit
Frequency Range of Modulator	1.4	4.5	14	MHz
Frequency Shift versus Temperature (Pin 14 open)	—	0.2	0.3	kHz/°C
Frequency Shift versus V_{CC} (Pin 14 open)	—	—	4.0	kHz/V
Output Amplitude (Pin 3 not loaded)	—	900	—	mVp-p
Output Harmonics, Unmodulated	—	—	-40	dB
Modulation Sensitivity 1.7 MHz	—	0.20	—	MHz/V
4.5 MHz	—	0.24	—	MHz/V
10.7 MHz	—	0.80	—	MHz/V
Audio Distortion (±25 kHz Deviation ,Optimized Bias Pin 14)	—	0.6	1.0	%
Audio Distortion (±25 kHz Deviation, Pin 14 self biased)	—	1.4	—	
Incidental AM (±25 kHz FM)	—	2.0	—	
Audio Input Resistance (Pin 14 to ground)	—	6.0	—	kΩ
Audio Input Capacitance (Pin 14 to ground)	—	5.0	—	pF
Stray Tuning Capacitance (Pin 3 to ground)	—	5.0	—	pF
Effective Oscillator Source Impedance (Pin 3 to load)	—	2.0	—	kΩ

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FIGURE 2 — TV MODULATOR



GENERAL DESCRIPTION

The MC1374 contains an RF oscillator, RF modulator, and a phase-shift type FM modulator, arranged to permit good printed circuit layout of a complete T.V. modulation system. The RF oscillator is similar to the one used in MC1372 and MC1373, and is coupled internally in the same way. It's frequency is controlled by an external tank on Pins 6 and 7, or by a crystal circuit, and will operate to approximately 105 MHz. The video modulator is a balanced type as used in the well known MC1496. Modulated sound carrier and composite video information can be put in separately on pins 1 and 11 to minimize unwanted crosstalk. A single resistor on Pins 12 and 13 is selected to set the modulator gain. The RF output at Pin 9 is a current source which drives a load connected from Pin 9 to V_{CC}.

The FM system was designed specifically for the T.V. intercarrier function. For circuit economy, one phase shift circuit was built into the chip. Still, it will operate from 1.4 MHz to 14 MHz, low enough to be used in a cordless telephone base station (1.76 MHz), and high enough to be used as an FM IF test signal source (10.7 MHz). At 4.5 MHz, a deviation of ±25 kHz can be achieved with 0.6% distortion (typical).

In the circuit above devices Q1 through Q7 are active in the oscillator function. Differential amplifier Q3, Q4, Q5, and Q6 acts as a gain stage, sinking current from input section Q1, Q2 and the phase shift network R17, C1. Input amplifier Q1, Q2 can vary the amount of "in phase" Q4 current to be combined with phase shifter current in load resistor R16. The R16 voltage is applied to emitter follower Q7 which drives an external L-C circuit. Feedback from the center of the L-C circuit back to the base of Q6 closes the loop. As audio input is applied which would offset the stable oscillatory phase, the frequency changes to counteract. The input to Pin 14 can include a dc feedback current for AFC over a limited range.

The modulated FM signal from Pin 3 is coupled to Pin 1 of the RF modulator and is then modulated onto the AM carrier.

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The AM modulator transfer function in Figure 3 shows that the video input can be of either polarity (and can be applied at either input). When the voltages on Pin 1 and Pin 11 are equal, the RF output is theoretically zero. As the difference between $V_{Pin\ 11}$ and $V_{Pin\ 1}$ increases, the RF output increases linearly until all of the current from both I_1 current sources (Q8 and Q9) is flowing in one side of the modulator. This occurs when $\pm(V_{Pin\ 11} - V_{Pin\ 1}) = I_1 R_G$, where I_1 is typically 1.15 mA. The peak-to-peak RF output is then $2I_1 R_L$. Usually the value of R_L is chosen to be 75Ω to ease the design of the output filter and match into T.V. distribution systems. The theoretical range of input voltage and R_G is quite wide, but noise and available sound level limit the useful video (sync tip) amplitude to between 0.25 and 1.0 Vpk. It is recommended that the value of R_G be chosen so that only about half of the dynamic range will be used at sync tip level.

The operating window of Figure 5 shows a cross-hatched area where Pin 1 and Pin 11 voltages must always be in order to avoid saturation in any part of the modulator. (The letter ϕ represents one diode drop, or about 0.75 V.) The oscillator Pins 6 and 7 must be biased to a level of $V_{CC} - \phi - 2I_1 R_L$ (or lower) and the input Pins 1 and 11 must always be at least 2ϕ below that. It is permissible to operate down to 1.6 V, saturating the current sources, but whenever possible, the minimum should be 3ϕ above ground.

The oscillator will operate dependably up to about 105 MHz with a broad range of tank circuit components values. It is desirable to use a small L and a large C to minimize the dependence on I.C. internal capacitance. An operating Q between 10 and 20 is recommended. The values of R_1, R_2 and R_3 are chosen to produce the desired Q and to set the Pin 6 and 7 d.c. voltage as discussed above. Unbalanced operation; i.e., Pin 6 or 7 bypassed to ground, is not recommended. Although the oscillator will still run, and the modulator will produce a useable signal, this mode causes substantial base-band video feedthrough. Bandswitching, as Figure 1 shows, can still be accomplished economically without using the unbalanced method.

The oscillator frequency with respect to temperature in the test circuit shows less than ±20 kHz total shift from 0°C to 50°C as shown in Figure 7. At higher temperatures the slope approaches 2.0 kHz/°C. Improvement in this region would require a temperature compensating tuning capacitor of the N75 family.

Crystal control is feasible using the circuit shown in Figure 21. The crystal is a 3rd overtone series type, used in series resonance. The L1, C2 resonance is adjusted well below the crystal frequency and is sufficiently tolerant to permit fixed values. A frequency shift versus temperature of less than 1.0 Hz/°C can be expected from this approach. The resistors Ra and Rb are to suppress parasitic resonances.

Coupling of output RF to wiring and components on Pins 1 and 11 can cause as much as 300 kHz shift in carrier (at 67 MHz) over the video input range. A careful layout can keep this shift below 10 kHz. Oscillator may also be inadvertently coupled to the RF output, with the undesired effect of preventing a good null when $V_{11} = V_1$. Reasonable care will yield carrier rejection ratios of 36 to 40 dB below sync tip level carrier.

In television, one of the most serious concerns is the prevention of the intermodulation of color (3.58 MHz) and sound (4.5 MHz) frequencies, which causes a 920 kHz signal to appear in the spectrum. Very little (3rd order) nonlinearity is needed to cause this problem. The results in Figure 6 are unsatisfactory, and demonstrate that too much of the available dynamic range of the MC1374 has been used. Figures 8 and 10 show that by either reducing standard signal level, or reducing gain, acceptable results may be obtained.

At VHF frequencies, small imbalances within the device introduce substantial amounts of 2nd harmonic in the RF output. At 67 MHz, the 2nd harmonic is only 6 to 8 dB below the maximum fundamental. For this reason a double pi low pass filter is shown in the test circuit of Figure 3 and works well for channel 3 and 4 lab work. For a fully commercial application, a vestigial sideband filter will be required. The general form and approximate values are shown in Figure 19. It must be exactly aligned to the particular channel.

FIGURE 3 — AM MODULATOR TRANSFER FUNCTION

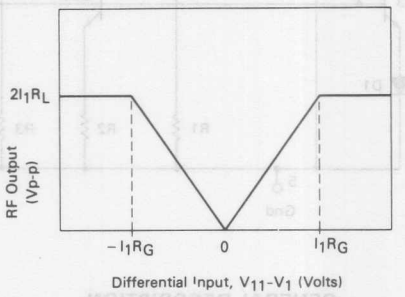


FIGURE 4 — AM TEST CIRCUIT

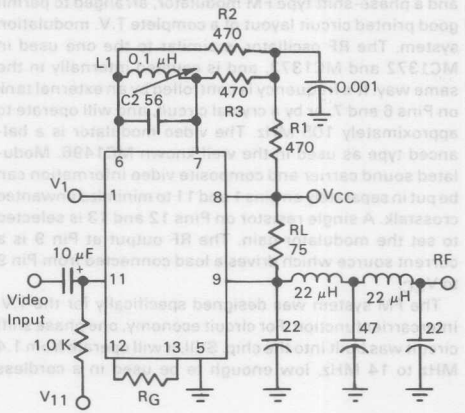


FIGURE 5 — THE OPERATING WINDOW

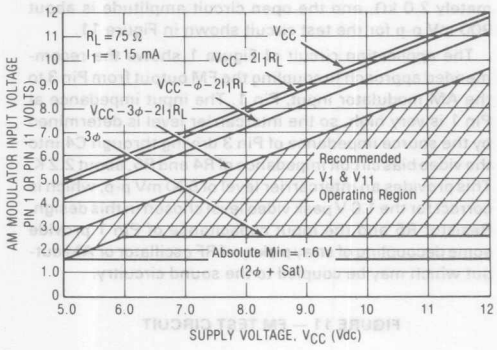


FIGURE 6 — 920 kHz BEAT

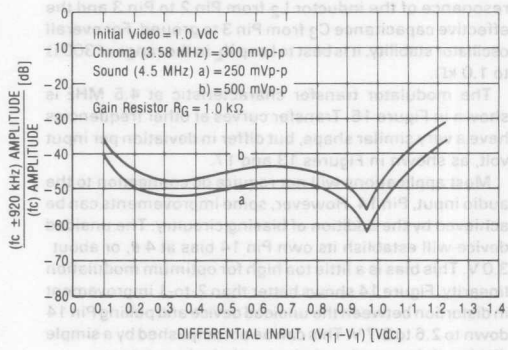


FIGURE 7 — RF OSCILLATOR FREQUENCY versus TEMPERATURE

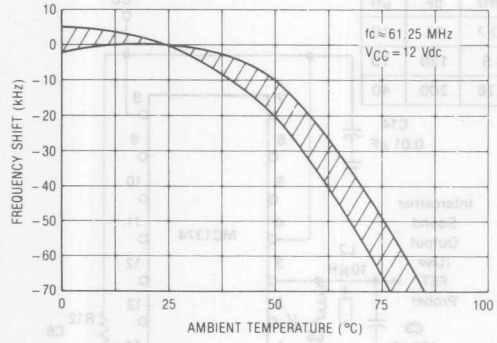


FIGURE 8 — 920 kHz BEAT

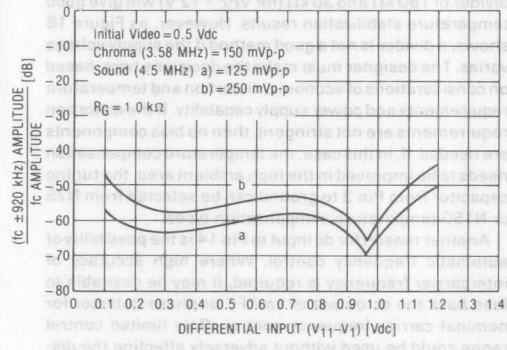


FIGURE 9 — RF OSCILLATOR FREQUENCY versus SUPPLY VOLTAGE

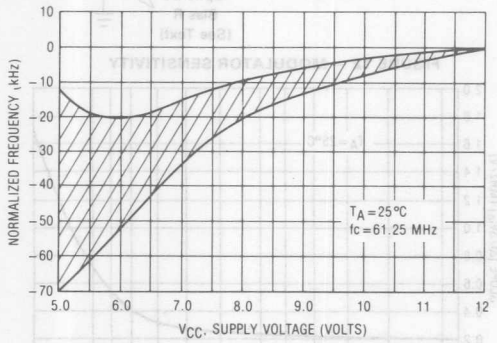
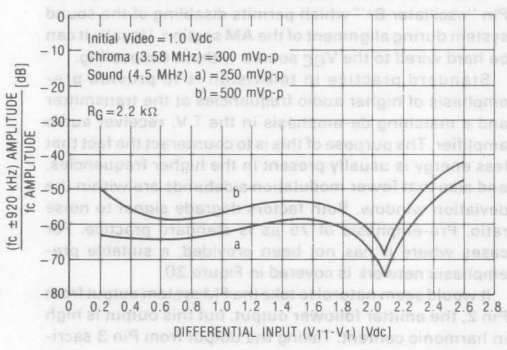


FIGURE 10 — 920 kHz BEAT



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FM SECTION

The oscillator center frequency is approximately the resonance of the inductor L_2 from Pin 2 to Pin 3 and the effective capacitance C_3 from Pin 3 to ground. For overall oscillator stability, it is best to keep X_L in the range of 300 Ω to 1.0 kΩ.

The modulator transfer characteristic at 4.5 MHz is shown in Figure 15. Transfer curves at other frequencies have a very similar shape, but differ in deviation per input volt, as shown in Figures 13 and 17.

Most applications will not require dc connection to the audio input, Pin 14. However, some improvements can be achieved by the addition of biasing circuitry. The unaided device will establish its own Pin 14 bias at 4 θ, or about 3.0 V. This bias is a little too high for optimum modulation linearity. Figure 14 shows better than 2-to-1 improvement in distortion between the unaided device and pulling Pin 14 down to 2.6 to 2.7 V. This can be accomplished by a simple divider, if the supply voltage is relatively constant.

The impedance of the divider has a bearing on the frequency versus temperature stability of the FM system. A divider of 180 kΩ and 30 kΩ (for V_{CC} = 12 V) will give good temperature stabilization results. However, as Figure 18 shows, a divider is not a good method if the supply voltage varies. The designer must make the decisions here, based on considerations of economy, distortion and temperature requirements and power supply capability. If the distortion requirements are not stringent, then no bias components are needed. If, in this case, the temperature compensation needs to be improved in the high ambient area, the tuning capacitor from Pin 3 to ground can be selected from N75 or N150 temperature compensation types.

Another reason for dc input to Pin 14 is the possibility of automatic frequency control. Where high accuracy of intercarrier frequency is required, it may be desirable to feed back the dc output of an AFC or phase detector for nominal carrier frequency control. Only limited control range could be used without adversely affecting the distortion performance, but very little frequency compensation will be needed.

One added convenience in the FM section is the separate Pin "oscillator B+" which permits disabling of the sound system during alignment of the AM section. Usually it can be hard wired to the V_{CC} source without decoupling.

Standard practice in television is to provide pre-emphasis of higher audio frequencies at the transmitter and a matching de-emphasis in the T.V. receiver audio amplifier. The purpose of this is to counteract the fact that less energy is usually present in the higher frequencies, and also that fewer modulation sidebands are within the deviation window. Both factors degrade signal to noise ratio. Pre-emphasis of 75 μs is standard practice. For cases where it has not been provided, a suitable pre-emphasis network is covered in Figure 20.

It would seem natural to take the FM system output from Pin 2, the emitter follower output, but this output is high in harmonic content. Taking the output from Pin 3 sacrifices somewhat in source impedance but results in a clean output fundamental, with all harmonics more than 40 dB down. This choice removes the need for additional filtering components. The source impedance of Pin 3 is approximately 2.0 kΩ, and the open circuit amplitude is about 900 mV p-p for the test circuit shown in Figure 11.

The application circuit of Figure 1 shows the recommended approach to coupling the FM output from Pin 3 to the AM modulator input, Pin 1. The input impedance at Pin 1 is very high, so the intercarrier level is determined by the source impedance of Pin 3 driving through C4 into the video bias circuit impedance of R4 and R5, about 2.2 K. This provides an intercarrier level of 500 mV p-p, which is correct for the 1.0 V peak video level chosen in this design. Resistor R6 and the input capacitance of Pin 1 provide some decoupling of stray pickup of RF oscillator or AM output which may be coupled to the sound circuitry.

FIGURE 11 — FM TEST CIRCUIT

f_o MHz	C3 pF	L2 μH
10.7	12	10
4.5	120	10
1.76	200	40

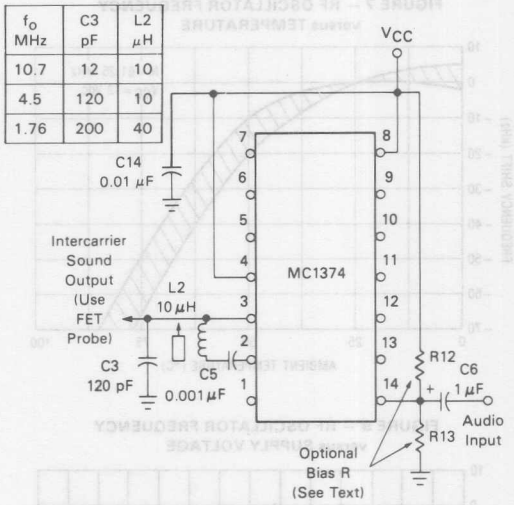


FIGURE 12 — MODULATOR SENSITIVITY

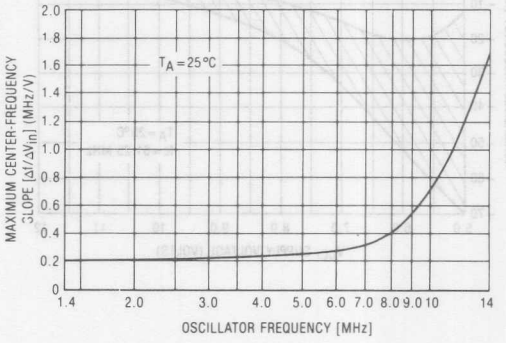


FIGURE 13 — MODULATOR TRANSFER FUNCTION (1.76 MHz)

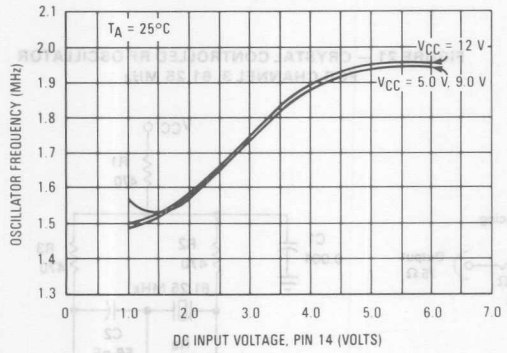


FIGURE 14 — DISTORTION versus MODULATION DEPTH

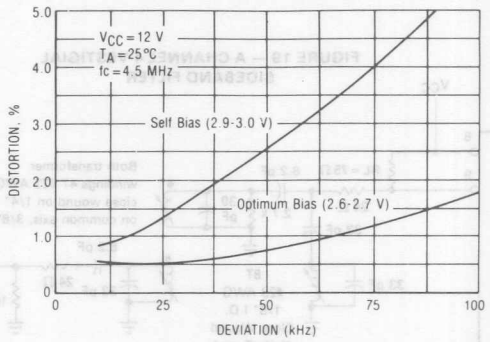


FIGURE 15 — MODULATOR TRANSFER FUNCTION (4.5 MHz)

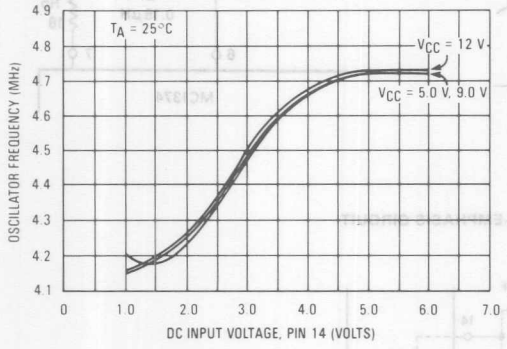


FIGURE 16 — FM SYSTEM FREQUENCY versus TEMPERATURE

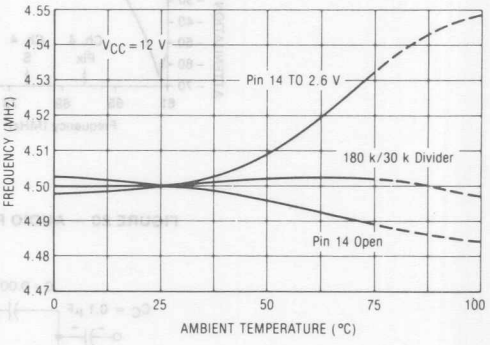


FIGURE 17 — MODULATOR TRANSFER FUNCTION (10.7 MHz)

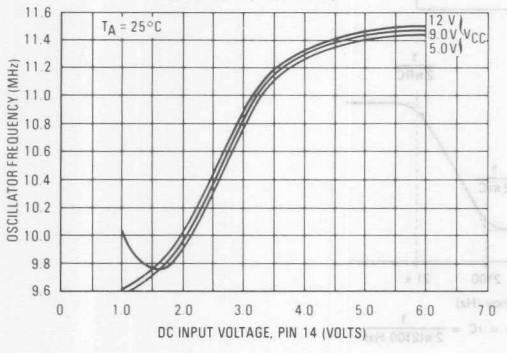
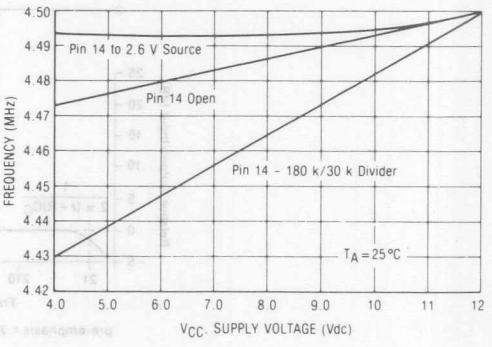


FIGURE 18 — FM SYSTEM FREQUENCY versus V_{CC}



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FIGURE 19 — A CHANNEL 4 VESTIGIAL SIDEBAND FILTER

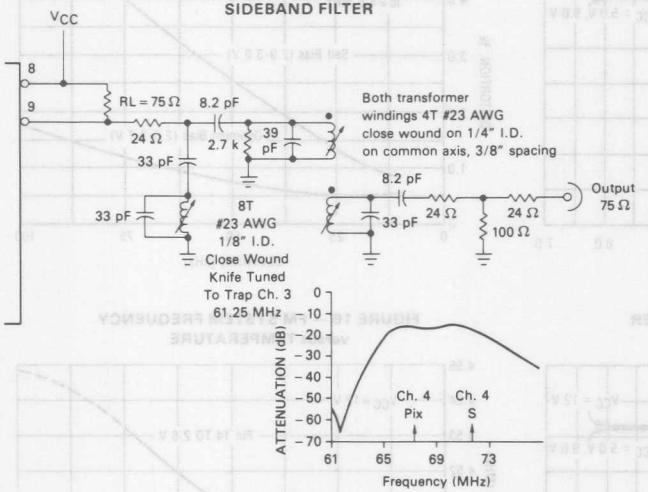


FIGURE 21 — CRYSTAL CONTROLLED RF OSCILLATOR FOR CHANNEL 3, 61.25 MHz

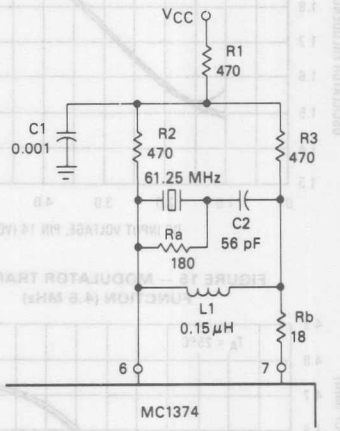
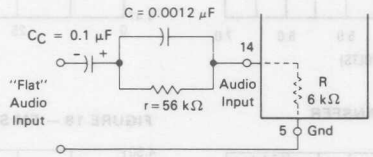
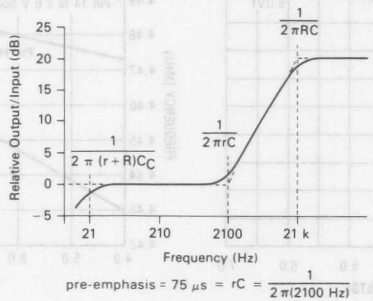


FIGURE 20 — AUDIO PRE-EMPHASIS CIRCUIT





pre-emphasis = 75 μs = $rC = \frac{1}{2\pi(2100\ Hz)}$

See Application Note AN829 for further information.

MOTOROLA

MC1377

Advance Information

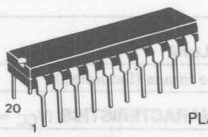
COLOR TELEVISION RGB to PAL/NTSC ENCODER

SILICON MONOLITHIC INTEGRATED CIRCUIT

COLOR TELEVISION RGB to PAL/NTSC ENCODER

. . . an integrated circuit used to generate a composite TV signal from baseband red, blue, green and sync inputs. The MC1377 has color subcarrier oscillator, voltage controlled 90° phase shifter, two DSB suppressed carrier chroma modulators, RGB input matrices and blanking level clamps. It can be operated with very few external parts, but has the pinouts for a fully implemented, top quality composite signal. It is ideal for encoding signals from color cameras and graphics generators.

- Reference Oscillator Self-Contained Or Externally Driven
- Nominal 90° ±3.0° Axes Are Optionally Trimmable
- Simple PAL/NTSC Switch
- Luminance And Chroma Channels Can Accept Delay Line/Bandpass Elements Or Direct Connection
- Provides dc Reference To Permit Direct Drive To RF Modulator



P SUFFIX
PLASTIC PACKAGE
CASE 738-03

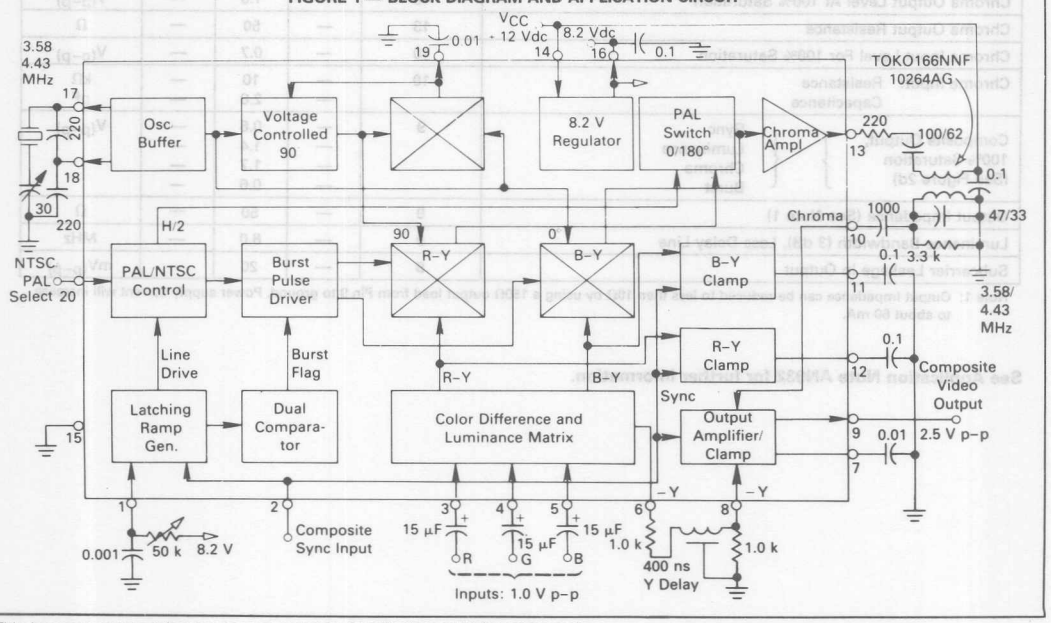


FN SUFFIX
PLASTIC PACKAGE
CASE 775-02
PLCC-20

ORDERING INFORMATION

Device	Temperature Range	Package
MC1377P MC1377FN	0–70°C	Plastic DIP PLCC-20

FIGURE 1 — BLOCK DIAGRAM AND APPLICATION CIRCUIT



This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	15	Vdc
8.2 Vdc Regulator Output Current	I_{REG}	10	mAdc
Operating Temperature	T_{AMB}	0 to +70	°C
Storage Temperature	T_{stg}	−65 to +150	°C
Junction Temperature	$T_{J(max)}$	150	°C
Power Dissipation, package Derate above 25°C	P_D	1.25 10	W mW/°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltage	12 ± 1.2	Vdc
Sync Tip Level Sync, Blanking Level	−0.5 to +1.0 +1.7 to +8.2	Vdc
Red, Green, Blue Inputs (Saturated)	1.0	V_{p-p}

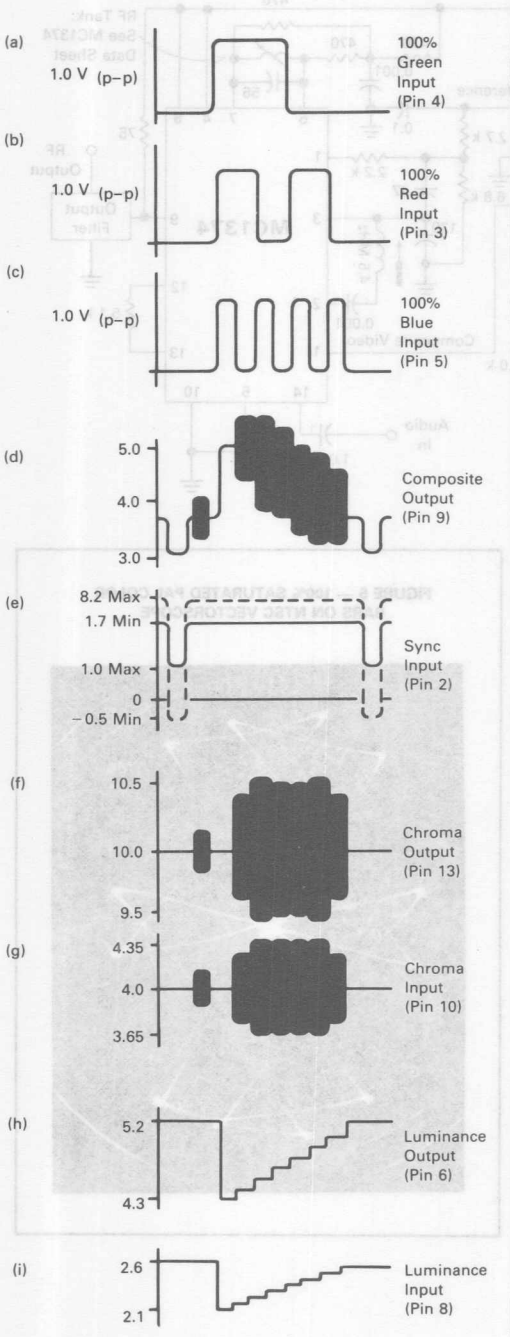
ELECTRICAL CHARACTERISTICS (V_{CC} = 12 Vdc, T_A = 25°C, Circuit Of Figure 1 Unless Otherwise Noted.)

Characteristic	Pin No.	Min	Typ	Max	Unit
Supply Current	14	20	32	40	mAdc
Oscillator Amplitude	18	—	0.5	—	$V_{(p-p)}$
External Subcarrier Input (Oscillator Components Removed)	17	—	0.25	—	V_{RMS}
Subcarrier Input: Resistance Capacitance	17	— —	5.0 2.0	— —	kΩ pF
Modulation Angle (R–Y) to (B–Y)	—	85	90	95	Degrees
(R–Y) Angle Adjustment	19	—	0.25	—	Deg/μA
R, G, B Input For 100% Color Saturation	3, 4, 5	—	1.0	—	$V_{(p-p)}$
R, G, B Input: Resistance Capacitance	3, 4, 5	— —	10 2.0	—	kΩ pF
Sync Threshold (See Figure 2e)	2	—	1.7	—	V
Sync Input Resistance (Input > 1.7 V)	2	—	10	—	kΩ
Chroma Output Level At 100% Saturation	13	—	1.0	—	$V_{(p-p)}$
Chroma Output Resistance	13	—	50	—	Ω
Chroma Input Level For 100% Saturation	10	—	0.7	—	$V_{(p-p)}$
Chroma Input: Resistance Capacitance	10	— —	10 2.0	— —	kΩ pF
Composite Output, 100% Saturation (See Figure 2d): Sync	9	—	0.6	—	$V_{(p-p)}$
Luminance		—	1.4	—	
Chroma		—	1.7	—	
Burst		—	0.6	—	
Output Impedance (See Note 1)	9	—	50	—	Ω
Luminance Bandwidth (3 dB), Less Delay Line	9	—	8.0	—	MHz
Subcarrier Leakage In Output	9	—	20	—	$mV_{(p-p)}$

Note 1: Output Impedance can be reduced to less than 10Ω by using a 150Ω output load from Pin 9 to ground. Power supply current will increase to about 60 mA.

See Application Note AN932 for further information.

FIGURE 2 — SIGNAL VOLTAGES
(CIRCUIT VALUES OF FIGURE 1)



APPLICATION NOTES

R.G.B. Inputs should be set up to be 1.0 V p–p for fully saturated levels. This is not arbitrary, since sync and burst levels are internally fixed. The large (15 μF) input capacitors of Figure 1 are needed for the 50/60 Hz vertical component.

Subcarrier Oscillator. The internal common-collector Colpitts can be free run or it can easily be pulled in by a lightly coupled signal from a "master" into Pin 17. Also, it can be disabled entirely and a 0.25 V_{RMS} signal driven into Pin 17.

Modulator Phase Angles are quite accurately established internally. Taking (B–Y) as 0°, burst is at 180°, and the angle of (R–Y) is 90° ±3.0°. The (R–Y) angle can be "tweaked." For example, 470 kΩ from Pin 19 to ground will increase the (R–Y) to (B–Y) angle about 3.0°. Pulling Pin 19 up will decrease the angle.

Composite Output is dc referenced and can be direct coupled to an RF modulator as shown in Figure 3. In this case, the 8.2 V regulator output of the MC1377 is divided down to 5.8 V to provide the zero carrier reference to Pin 1 of the MC1374.

Burst Generation is provided by a sync triggered ramp on Pin 1 and two internal level sensors. Since the early part of this ramp is used, it is quite accurate. Fixed R–C values are feasible, as shown in Figure 3.

Sync Input can be varied over a wide latitude but neverless must be applied correctly. The typical ac coupled sync signal has very little positive value and will require a pull-up resistor to 8.2 Vdc at the input. The sync input is a 10 kΩ/10 kΩ divider in the base of a common emitter stage. For PAL operation, the correctly serrated vertical sync interval must be used, in order to continuously trigger the PAL flip-flop. "Block" vertical sync can be used for NTSC.

(R–Y)(B–Y)(–Y) signals are generated to NTSC values (±5.0%) in the input matrices. They are dc clamped at black level by a sync driven clamp. Burst amplitude is internally fixed to correspond to sync level, allowing for 3.0 dB loss in the chroma bandpass filter. If the filter is not used, as shown in Figure 3, a resistor divider should be inserted between Pin 13 and Pin 10 to provide the proper chroma level. When the chroma bandpass is not used, the (–Y) delay line should also be removed, but the 1.0 k/1.0 k divider from Pin 6 to Pin 8 should be retained.

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FIGURE 3 — COUPLING THE MC1377 TO THE MC1374 RF MODULATOR

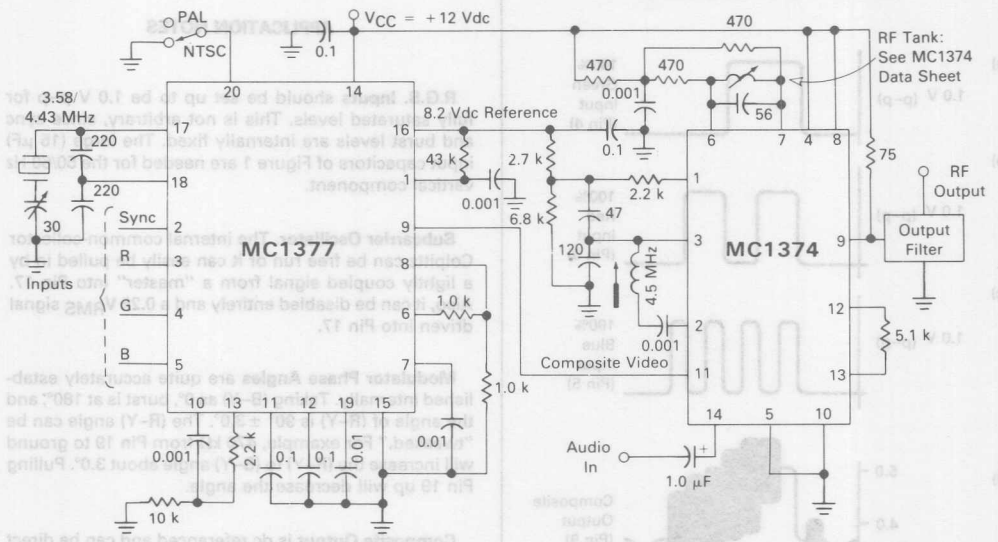


FIGURE 4 — VECTORSCOPE DISPLAY OF 100% SATURATED NTSC COLOR BARS

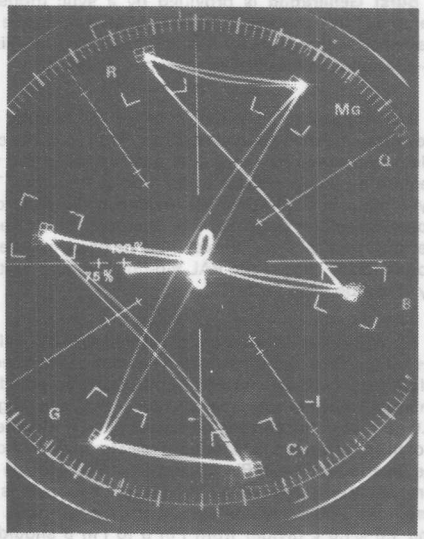
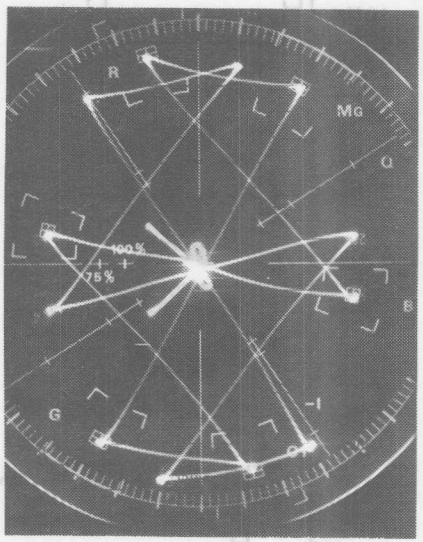


FIGURE 5 — 100% SATURATED PAL COLOR BARS ON NTSC VECTORSCOPE



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MOTOROLA

MC1378

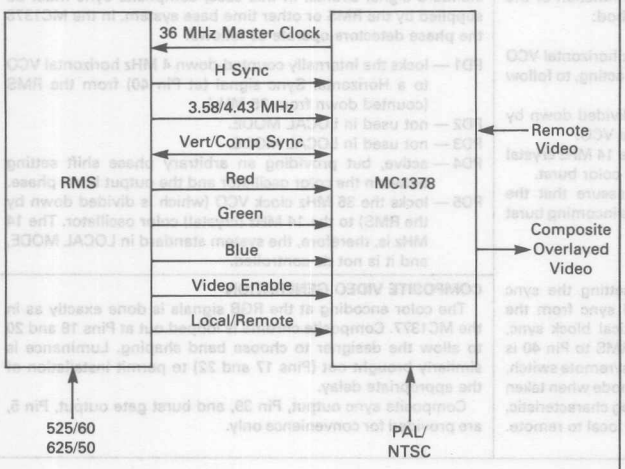
Product Preview

COLOR TELEVISION COMPOSITE VIDEO OVERLAY SYNCHRONIZER

. . . a bipolar composite video overlay encoder and microcomputer synchronizer. The MC1378 contains the complete encoder function of the MC1377, i.e. quadrature color modulators, RGB matrix, and blanking level clamps, plus a complete complement of synchronizers to lock a microcomputer-based video source to any remote video source. The MC1378 is especially tailored to work with the Motorola RMS (Raster Memory System), but it can be applied to other controllable video sources. It can be used as a local system timing and encoding source, but it is most valuable when used to lock the microcomputer source to a remotely originated video signal.

- Contains All Needed Reference Oscillators
- Can Be Operated in PAL or NTSC Mode, 625 or 525 Line
- Wideband, Full-Fidelity Color Encoding
- Local or Remote Modes of Operation
- Minimal External Components
- Designed to Operate from 5.0 V Supply
- Will Work with Non-standard Video

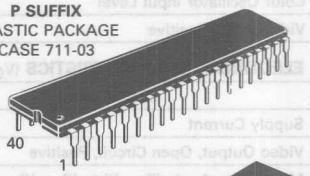
FIGURE 1 — BLOCK DIAGRAM TYPICAL APPLICATION



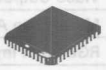
COLOR TELEVISION COMPOSITE VIDEO OVERLAY SYNCHRONIZER

SILICON MONOLITHIC INTEGRATED CIRCUIT

P SUFFIX
PLASTIC PACKAGE
CASE 711-03



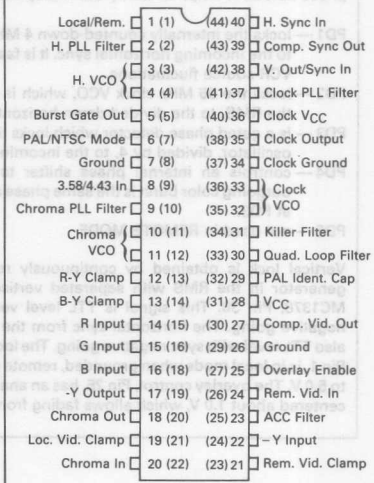
FN SUFFIX
PLASTIC PACKAGE
CASE 777-02
PLCC-44



ORDERING INFORMATION

Device	Temperature Range	Package
MC1378P	0–70°C	Plastic DIP
MC1378FN		PLCC-44

PIN ASSIGNMENTS



*( ) PLCC Pin Assignments

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This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	6.0	Vdc
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−65 to +150	°C
Junction Temperature	$T_{J(max)}$	150	°C
Power Dissipation (Package) Derate above 25°C	P_D	1.25 10	W mW/°C

RECOMMENDED OPERATING CONDITIONS

Condition	Pin No.	Value	Unit
Supply Voltage	28, 36	5.0 ± 0.25	Vdc
RGB Input for 100% Saturation	14, 15, 16	1.0	V_{p-p}
Color Oscillator Input Level	8	0.5	V_{p-p}
Video Input, Positive	24	1.0	V_{p-p}

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C Circuit of Figure 4 or 5)

Characteristic	Pin No.	Min	Typ	Max	Unit
Supply Current	28, 36	—	100	—	mAdc
Video Output, Open Circuit, Positive	27	—	2.0	9.4	V_{p-p}
Modulation Angle (R − Y) to (B − Y)	—	87	90	93	Degrees
RGB Input Impedance	14, 15, 16	—	10	—	kΩ
Local/Remote Switch (TTL) High Low	1	—	Remote Local	—	—
Horizontal Sync Input, Negative Going (TTL)	40	—	4.3	—	V_{p-p}
Vertical Sync Output, Negative Going, Remote Mode (TTL)	38	—	4.3	—	V_{p-p}
Composite Sync Output, Negative Going (TTL)	39	—	4.3	—	V_{p-p}
Burst Gate Output, Positive Going (TTL)	5	—	4.3	—	V_{p-p}

DESCRIPTION OF OPERATION — Refer to Figures 3, 4

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REMOTE MODE

The incoming remote video signal (Pin 24) supplies all synchronizing information. A discussion of the function of the phase detectors helps to clarify the lockup method:

PD1 — locks the internally counted-down 4 MHz horizontal VCO to the incoming horizontal sync. It is fast acting, to follow VCR source fluctuations.
PD2 — locks the 36 MHz clock VCO, which is divided down by the RMS, to the divided down horizontal VCO.
PD3 — is a gated phase detector which locks the 14 MHz crystal oscillator, divided by 4, to the incoming color burst.
PD4 — controls an internal phase shifter to assure that the outgoing color burst is the same phase as incoming burst at PD3.
PD5 — not used in REMOTE MODE

Vertical lock is obtained by continuously resetting the sync generator in the RMS with separated vertical sync from the MC1378, Pin 38. This signal is TTL level vertical block sync, negative going. The horizontal sync from the RMS to Pin 40 is also TTL level with sync negative going. The local/remote switch, Pin 1, is in local mode when grounded, remote mode when taken to 5.0 V. The overlay control, Pin 25, has an analog characteristic, centered about 1.0 V, which allows fading from local to remote.

LOCAL MODE

The MC1378 and RMS combine to provide a fully synchronized standard signal source. In this case, composite sync must be supplied by the RMS or other time base system. In the MC1378 the phase detectors operate as follows:

PD1 — locks the internally counted-down 4 MHz horizontal VCO to a Horizontal Sync signal (at Pin 40) from the RMS (counted down from 36 MHz).
PD2 — not used in LOCAL MODE.
PD3 — not used in LOCAL MODE.
PD4 — active, but providing an arbitrary phase shift setting between the color oscillator and the output burst phase.
PD5 — locks the 36 MHz clock VCO (which is divided down by the RMS) to the 14 MHz (crystal) color oscillator. The 14 MHz is, therefore, the system standard in LOCAL MODE, and it is not dc controlled.

COMPOSITE VIDEO GENERATION

The color encoding at the RGB signals is done exactly as in the MC1377. Composite chroma is looped out at Pins 18 and 20 to allow the designer to choose band shaping. Luminance is similarly brought out (Pins 17 and 22) to permit installation of the appropriate delay.

Composite sync output, Pin 39, and burst gate output, Pin 5, are provided for convenience only.

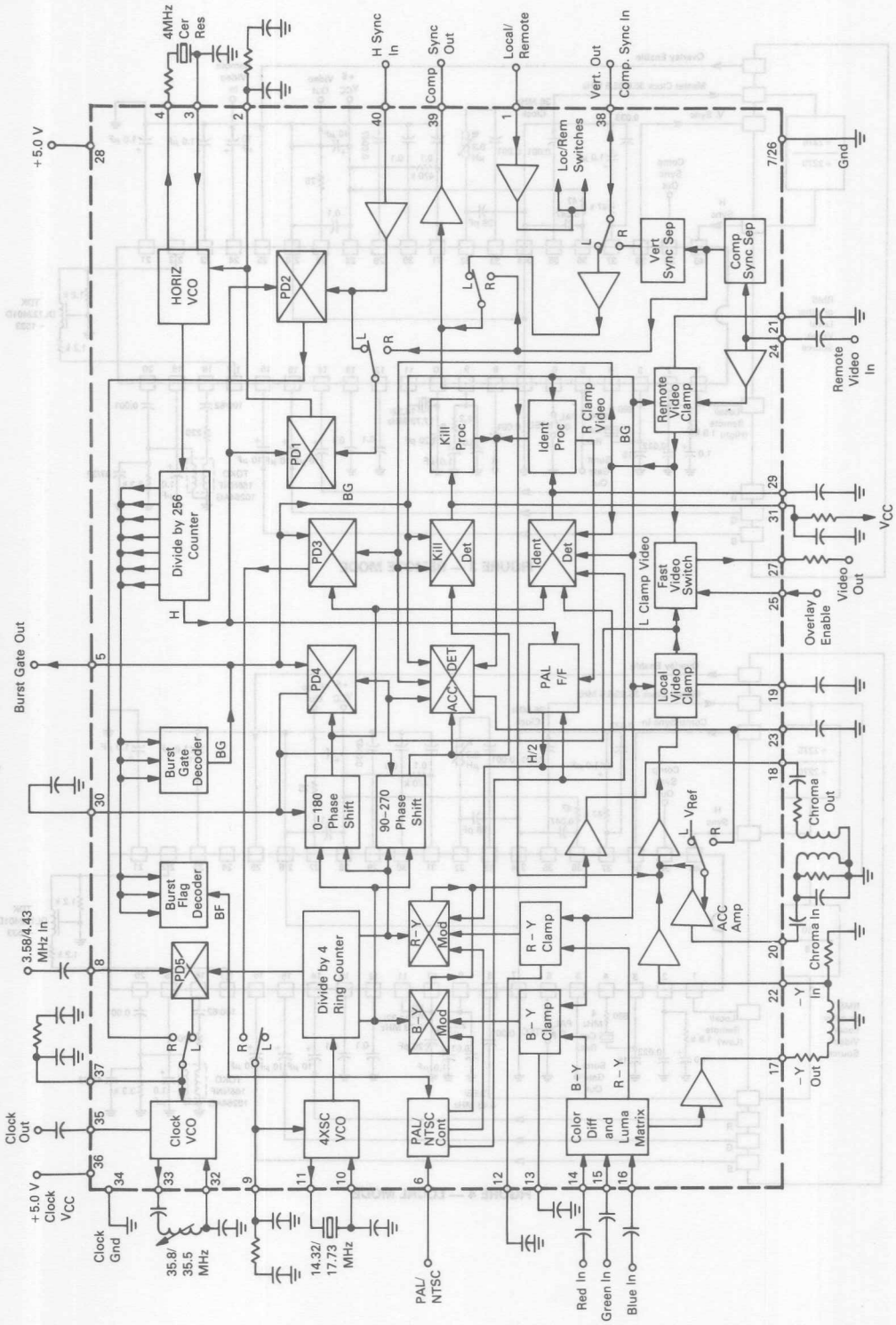


FIGURE 2 — MC1378 INTERNAL BLOCK DIAGRAM

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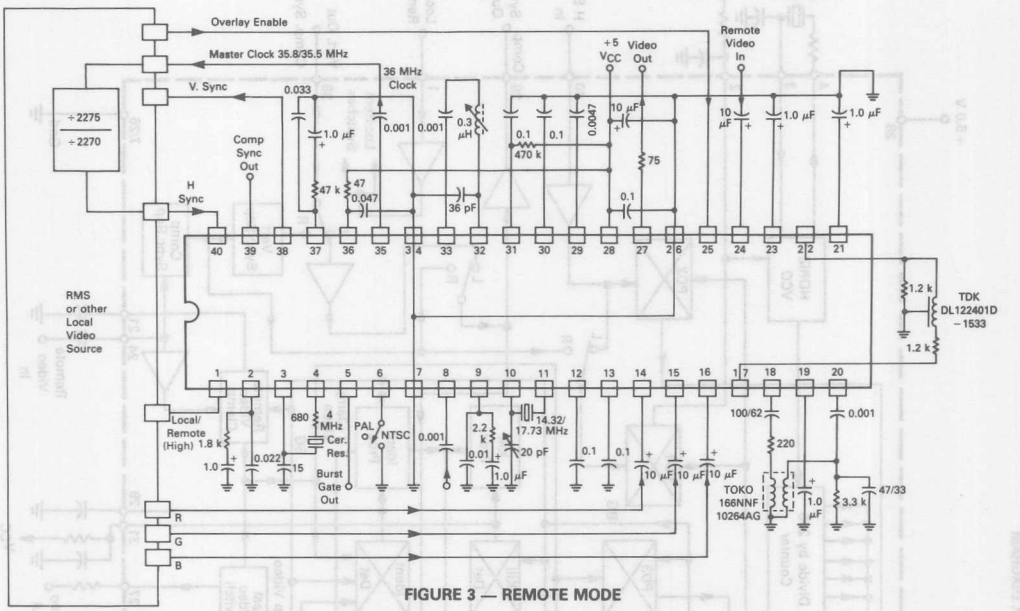


FIGURE 3 — REMOTE MODE

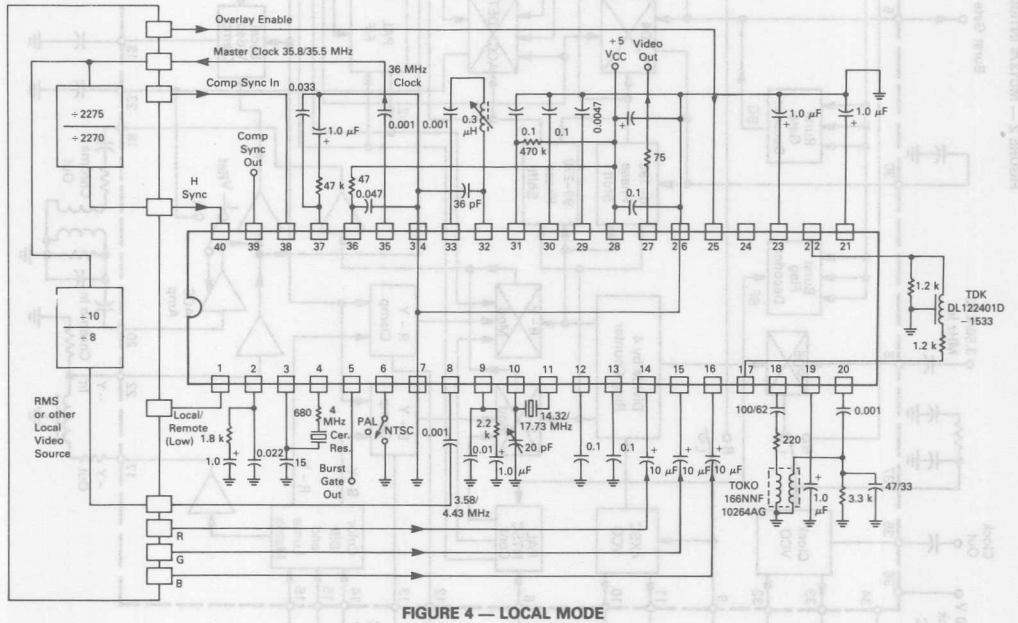


FIGURE 4 — LOCAL MODE

MOTOROLA

MC1391P

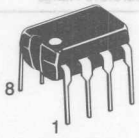
TV HORIZONTAL PROCESSOR

. . . low-level horizontal sections including phase detector, oscillator and pre-driver — a device designed for use in all types of television receivers.

- Internal Shunt Regulator
- Preset Hold Control Capability
- ±300 Hz Typical Pull-In
- Linear Balanced Phase Detector
- Variable Output Duty Cycle for Driving Tube or Transistor
- Low Thermal Frequency Drift
- Small Static Phase Error
- Adjustable dc Loop Gain
- Positive Flyback Inputs

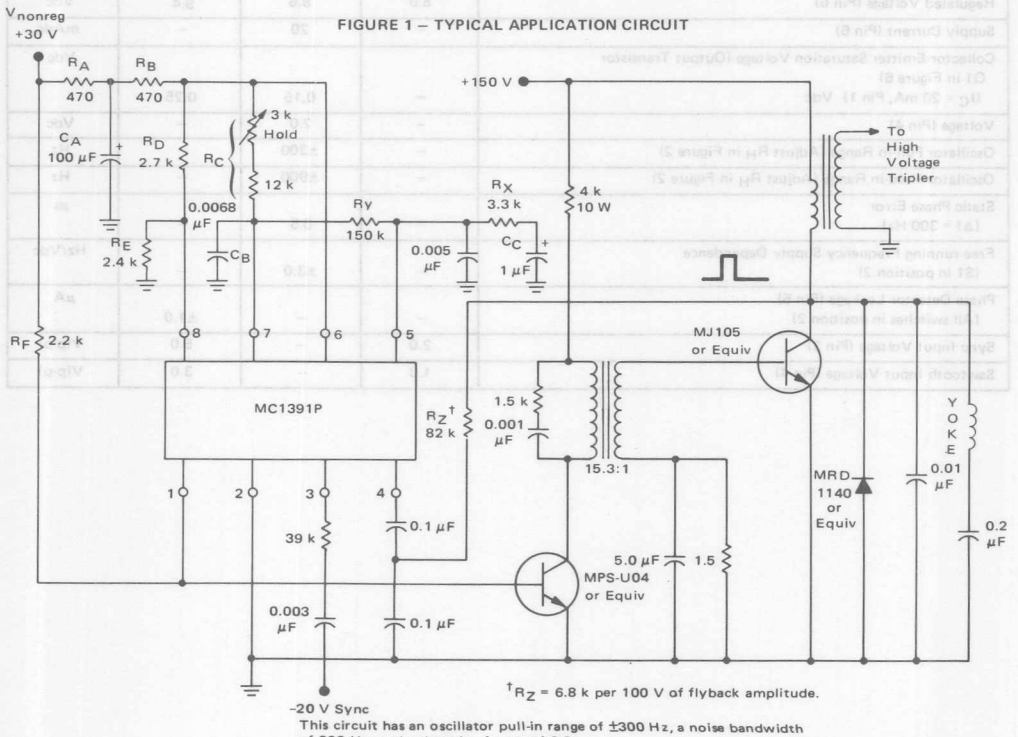
TV HORIZONTAL PROCESSOR

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 626-05

FIGURE 1 – TYPICAL APPLICATION CIRCUIT



This circuit has an oscillator pull-in range of ±300 Hz, a noise bandwidth of 320 Hz, and a damping factor of 0.8.

9

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Value	Unit
Supply Current	40	mAdc
Output Voltage	40	Vdc
Output Current	30	mAdc
Sync Input Voltage (Pin 3)	5.0	$V_{(p-p)}$
Flyback Input Voltage (Pin 4)	5.0	$V_{(p-p)}$
Power Dissipation (Package Limitation) Plastic Package Derate above T_A = +25°C	 625 5.0	 mW mW/°C
Operating Temperature Range (Ambient)	0 to +70°	°C
Storage Temperature Range	-65 to +150	°C



ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted.) (See Test Circuit of Figure 2, all switches in position 1.)

Characteristic	Min	Typ	Max	Unit
Regulated Voltage (Pin 6)	8.0	8.6	9.4	Vdc
Supply Current (Pin 6)	–	20	–	mAdc
Collector-Emitter Saturation Voltage (Output Transistor Q1 in Figure 6) (I_C = 20 mA, Pin 1) Vdc	–	0.15	0.25	Vdc
Voltage (Pin 4)	–	2.0	–	Vdc
Oscillator Pull-in Range (Adjust R_H in Figure 2)	–	±300	–	Hz
Oscillator Hold-in Range (Adjust R_H in Figure 2)	–	±900	–	Hz
Static Phase Error (Δf = 300 Hz)	–	0.5	–	μs
Free-running Frequency Supply Dependance (S1 in position 2)	–	±3.0	–	Hz/Vdc
Phase Detector Leakage (Pin 5) (All switches in position 2)	–	–	±1.0	μA
Sync Input Voltage (Pin 3)	2.0	–	5.0	V(p-p)
Sawtooth Input Voltage (Pin 4)	1.0	–	3.0	V(p-p)

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TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted.)

FIGURE 2 – TEST CIRCUIT

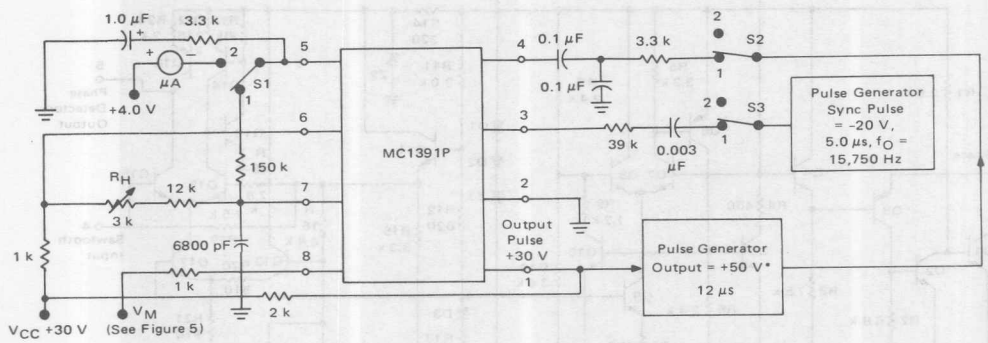


FIGURE 3 – FREQUENCY versus TEMPERATURE

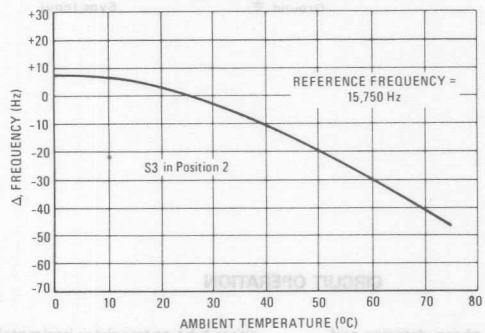


FIGURE 4 – FREQUENCY DRIFT versus WARM-UP TIME

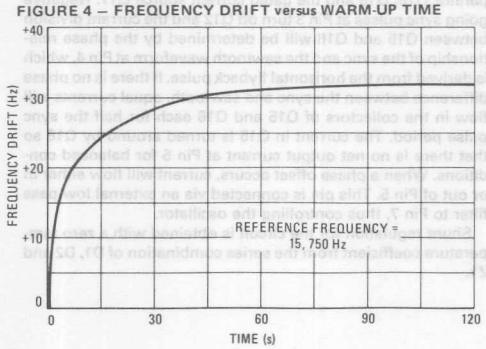
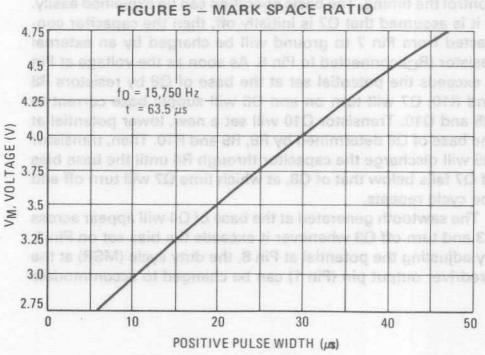
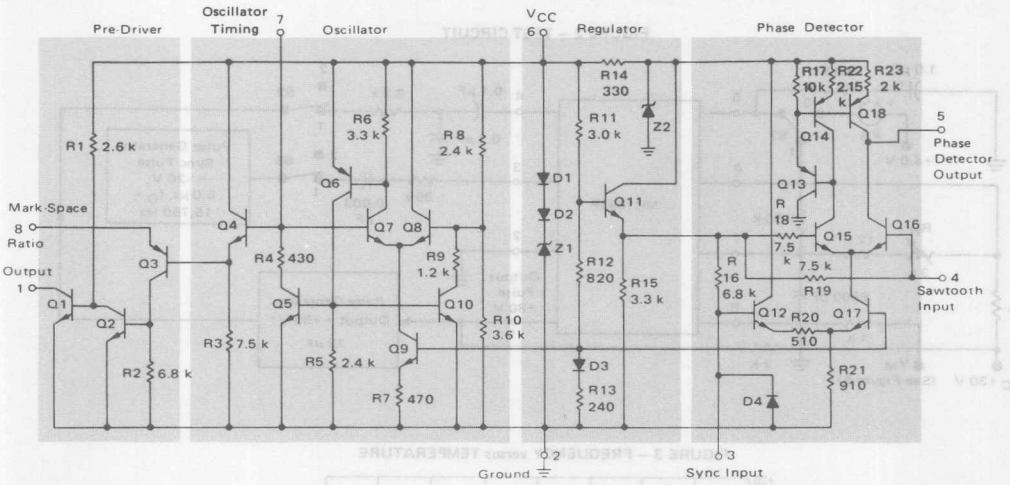


FIGURE 5 – MARK SPACE RATIO



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FIGURE 6 – CIRCUIT SCHEMATIC



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CIRCUIT OPERATION

The MC1391P contains the oscillator, phase detector and predriver sections needed for a television horizontal APC loop.

The oscillator is an RC type with one pin (Pin 7) used to control the timing. The basic operation can be explained easily. If it is assumed that Q7 is initially off, then the capacitor connected from Pin 7 to ground will be charged by an external resistor (R_C) connected to Pin 6. As soon as the voltage at Pin 7 exceeds the potential set at the base of Q8 by resistors R8 and R10, Q7 will turn on and Q6 will supply base current to Q5 and Q10. Transistor Q10 will set a new, lower potential at the base of Q8 determined by R8, R9 and R10. Then, transistor Q5 will discharge the capacitor through R4 until the base bias of Q7 falls below that of Q8, at which time Q7 will turn off and the cycle repeats.

The sawtooth generated at the base of Q4 will appear across R3 and turn off Q3 whenever it exceeds the bias set on Pin 8. By adjusting the potential at Pin 8, the duty cycle (MSR) at the predriver output pin (Pin 1) can be changed to accommodate either tube or transistor horizontal output stages.

The phase detector is isolated from the remainder of the circuit by R14 and Z2. The phase detector consists of the comparator Q15, Q16 and the gated current source Q17. Negative going sync pulses at Pin 3 turn off Q12 and the current division between Q15 and Q16 will be determined by the phase relationship of the sync and the sawtooth waveform at Pin 4, which is derived from the horizontal flyback pulse. If there is no phase difference between the sync and sawtooth, equal currents will flow in the collectors of Q15 and Q16 each for half the sync pulse period. The current in Q15 is turned around by Q18 so that there is no net output current at Pin 5 for balanced conditions. When a phase offset occurs, current will flow either in or out of Pin 5. This pin is connected via an external low-pass filter to Pin 7, thus controlling the oscillator.

Shunt regulation for the circuit is obtained with a zero temperature coefficient from the series combination of D1, D2 and Z1.

APPLICATION INFORMATION

Although it is an integrated circuit, the MC1391P has all the flexibility of a conventional discrete component horizontal APC loop.

The internal temperature compensated voltage regulator allows a wide supply voltage variation to be tolerated, enabling operation from nonregulated power supplies. A minimum value for supply current into Pin 6 to maintain zener regulation is about 18 mA. Allowing 2 mA for the external dividers

$$R_A + R_B = \frac{V_{nonreg(min)} - 8.8}{20 \times 10^{-3}}$$

Components R_A, R_B and C_A are used for ripple rejection. If the supply voltage ripple is expected to be less than 100 mV (for a 30 Volt supply) then R_A and R_B can be combined and C_A omitted.

The output pulse width can be varied from 6 μs to 48 μs by changing the voltage at Pin 8 (see Figure 5). However, care should be taken to keep the lead lengths to Pin 8 as short as possible to prevent ringing which can result in erroneous output pulses at Pin 1. The parallel impedance of R_D and R_E should be close to 1 kΩ to ensure stable pulse widths.

For 15 mA drive at saturation

$$R_F = \frac{V_{nonreg} - 0.3}{15 \times 10^{-3}}$$

The oscillator free-running frequency is set by R_C and C_B connected to Pin 7. For values of $R_C \gg R_{discharge}$ (R4 in Figure 6), a useful approximation for the free-running frequency is

$$f_O = \frac{1}{0.6\ R_C C_B}$$

Proper choice of R_C and C_B will give a wide range of oscillator frequencies — operation at 31.5 kHz for count-down circuits is possible for example. As long as the product $R_C C_B \approx 10^{-4}$ many combinations of values of R_C and C_B will satisfy the free-running frequency requirement of 15.734 kHz. However, the sensitivity of the oscillator (β) to control-current from the phase detector is directly dependent on the magnitude of R_C, and this provides a convenient method of adjusting the dc loop gain (fc).

For a given phase detector sensitivity (μ) = 1.60×10^{-4} A/rad

$$fc = \mu\beta \text{ and } \beta = 3.15 \times R_C \text{ Hz/mA}$$

Increasing R_C will raise the dc loop gain and reduce the static phase error (S.P.E.) for a given frequency offset. Secondary effects are to increase the natural resonant frequency of the loop (ω_n) and give a wider pull-in range from an out-of-lock condition. The loop will also tend to be underdamped with fast pull-in times, producing good airplane flutter performance. However, as the loop becomes more underdamped impulse noise can cause shock excitation of the loop. Unlimited increase in the dc loop gain will also raise the noise bandwidth excessively causing horizontal jitter with thermal noise. Once the dc loop gain has been selected for adequate S.P.E. performance, the loop filter can be used to produce the balance between other desirable characteristics. Damping of the loop is achieved most directly by changing the resistor R_X with respect to R_Y which modifies the ac/dc gain ratio (m) of the loop. Lowering this ratio will reduce the pull-in range and noise bandwidth (fnn). (Note: very large values of R_Y will limit the control capability of the phase detector with a corresponding reduction in hold-in range.)

Static phasing can be adjusted simply by adding a small resistor between the flyback pulse integrating capacitor and ground. The sync coupling capacitor should not be too small or it can charge during the vertical pulse and this may result in picture bends at the top of the CRT.

NOTE:
In adjusting the loop parameters, the following equations may prove useful:

$$f_{nn} = \frac{1 \times \chi^2\ T\omega_c}{4\ \chi\ T}$$

$$\omega_n = \sqrt{\frac{\omega_c}{(1 + \chi)\ T}}$$

$$K = \frac{\chi^2 T\omega_c}{4}$$

$$\chi = \frac{R_X}{R_Y}$$

$$\omega_c = 2\ \pi\ fc$$

$$T = R_Y\ C_C$$

where:
K = loop damping coefficient

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ORDERING INFORMATION

Device	Temperature Range	Package
MC3346D	−40°C to +85°C	SO-14
MC3346P	−40°C to +85°C	Plastic DIP

MC3346

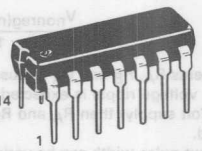
ONE DIFFERENTIALLY CONNECTED PAIR AND THREE ISOLATED TRANSISTOR ARRAY

The MC3346 is designed for general purpose, low power applications for consumer and industrial designs.

- Guaranteed Base-Emitter Voltage Matching
- Operating Current Range Specified — 10 μA to 10 mA
- Five General-Purpose Transistors in One Package

GENERAL PURPOSE TRANSISTOR ARRAY

SILICON MONOLITHIC INTEGRATED CIRCUIT



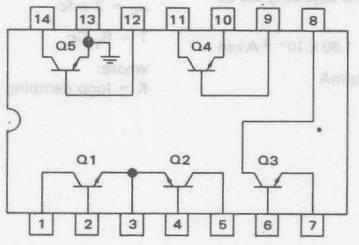
P SUFFIX
PLASTIC PACKAGE
CASE 646-06



D SUFFIX
PLASTIC PACKAGE
CASE 751A-02
SO-14

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	15	Vdc
Collector-Base Voltage	V_{CBO}	20	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector-Substrate Voltage	V_{CIO}	20	Vdc
Collector Current — Continuous	I_C	50	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C Derate Each Transistor @ 25°C	P_D	1.2 10 300	Watts mW/°C mW/°C
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C



Pin 13 is connected to substrate and must remain at the lowest circuit potential.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
STATIC CHARACTERISTICS					
Collector-Base Breakdown Voltage (I_C = 10 μAdc)	$V_{(BR)CBO}$	20	60	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc)	$V_{(BR)CEO}$	15	—	—	Vdc
Collector-Substrate Breakdown Voltage (I_C = 10 μA)	$V_{(BR)CIO}$	20	60	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc)	$V_{(BR)EBO}$	5.0	7.0	—	Vdc
Collector-Base Cutoff Current (V_{CB} = 10 Vdc, I_E = 0)	I_{CBO}	—	—	40	nAdc
DC Current Gain	h_{FE}				—
(I_C = 10 mAdc, V_{CE} = 3.0 Vdc)		—	140	—	
(I_C = 1.0 mAdc, V_{CE} = 3.0 Vdc)		40	130	—	
(I_C = 10 μAdc, V_{CE} = 3.0 Vdc)		—	60	—	
Base-Emitter Voltage	V_{BE}				Vdc
(V_{CE} = 3.0 Vdc, I_E = 1.0 mAdc)		—	0.72	—	
(V_{CE} = 3.0 Vdc, I_E = 10 mAdc)		—	0.8	—	
Input Offset Current for Matched Pair Q1 and Q2 (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc)	$\lvert I_{IO1} - I_{IO2} \rvert$	—	0.3	2.0	μAdc
Magnitude of Input Offset Voltage (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc)	—	—	0.5	5.0	mVdc
Temperature Coefficient of Base-Emitter Voltage (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc)	$\frac{\Delta V_{BE}}{\Delta T}$	—	−1.9	—	mV/°C
Temperature Coefficient	$\frac{\lvert \Delta V_{IO} \rvert}{\Delta T}$	—	1.0	—	μV/°C
Collector-Emitter Cutoff Current (V_{CE} = 10 Vdc, I_B = 0)	I_{CEO}	—	—	0.5	μAdc
DYNAMIC CHARACTERISTICS					
Low Frequency Noise Figure (V_{CE} = 3.0 Vdc, I_C = 100 μAdc, R_S = 1.0 kΩ, f = 1.0 kHz)	NF	—	3.25	—	dB
Forward Current Transfer Ratio (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc, f = 1.0 kHz)	h_{FE}	—	110	—	—
Short-Circuit Input Impedance (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc)	h_{ie}	—	3.5	—	kΩ
Open-Circuit Output Impedance (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc)	h_{oe}	—	15.6	—	μmhos
Reverse Voltage Transfer Ratio (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc)	h_{re}	—	1.8	—	$x10^{-4}$
Forward Transfer Admittance (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc, f = 1.0 MHz)	y_{fe}	—	31 − j1.5	—	—
Input Admittance (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc, f = 1.0 MHz)	y_{ie}	—	0.3 + j0.04	—	—
Output Admittance (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc, f = 1.0 MHz)	y_{oe}	—	0.001 + j0.03	—	—
Current-Gain — Bandwidth Product (V_{CE} = 3.0 Vdc, I_C = 3.0 mAdc)	f_T	300	550	—	MHz
Emitter-Base Capacitance (V_{EB} = 3.0 Vdc, I_E = 0)	C_{eb}	—	0.6	—	pF
Collector-Base Capacitance (V_{CB} = 3.0 Vdc, I_C = 0)	C_{cb}	—	0.58	—	pF
Collector-Substrate Capacitance (V_{CS} = 3.0 Vdc, I_C = 0)	C_{CI}	—	2.8	—	pF

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TYPICAL CHARACTERISTICS

FIGURE 1 – COLLECTOR CUTOFF CURRENT versus TEMPERATURE, (Each Transistor)

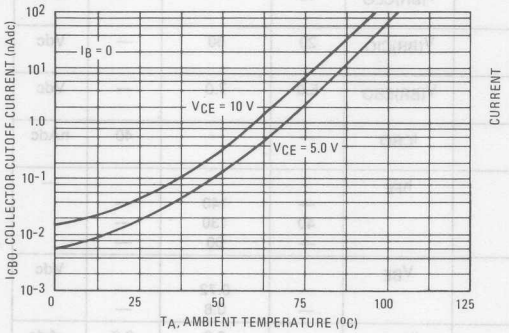


FIGURE 2 – COLLECTOR CUTOFF CURRENT versus TEMPERATURE (Each Transistor)

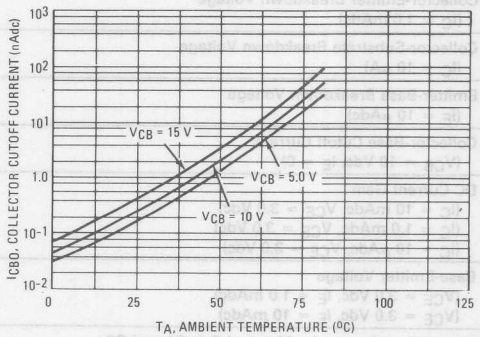


FIGURE 3 – INPUT OFFSET CHARACTERISTICS FOR Q1 and Q2

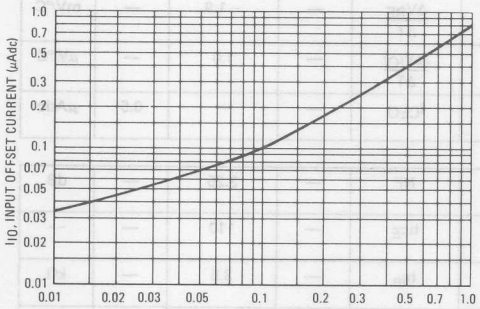


FIGURE 4 – BASE-EMITTER AND INPUT OFFSET VOLTAGE CHARACTERISTICS

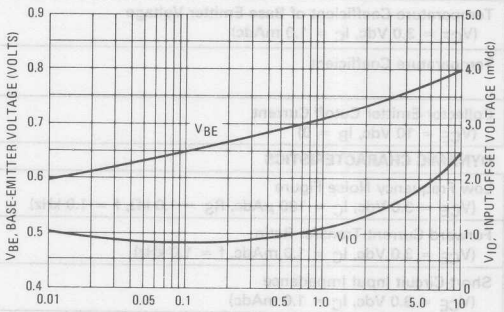
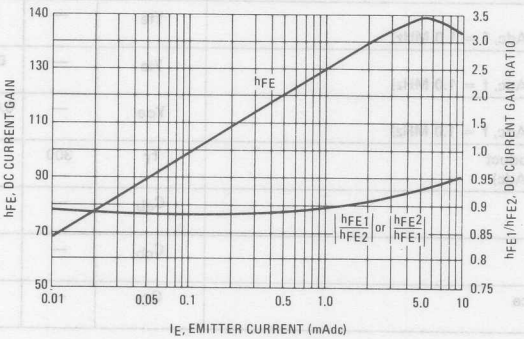


FIGURE 5 – DC CURRENT GAIN



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MOTOROLA

MC3373

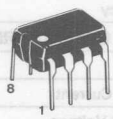
REMOTE CONTROL WIDEBAND AMPLIFIER WITH DETECTOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

REMOTE CONTROL AMPLIFIER-DETECTOR

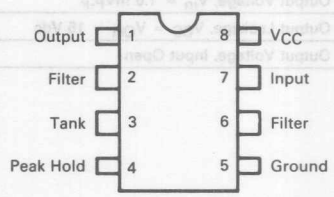
The MC3373 is intended for application in infrared remote controls. It provides the high gain and pulse shaping needed to couple the signal from an IR receiver diode to the tuning control system logic.

- High Gain Pre-Amp
- Envelope Detector for PCM Demodulation
- Simple Interface to Microcomputer Remote Control Decoder
- May Be Used with Tuned Circuit for Narrow Bandwidth, Lower Noise Operation
- Small Package Size
- Minimum External Components
- Wide Operating Supply Voltage Range
- Low Current Drain
- Improved retrofit for NEC part no. μPC1373



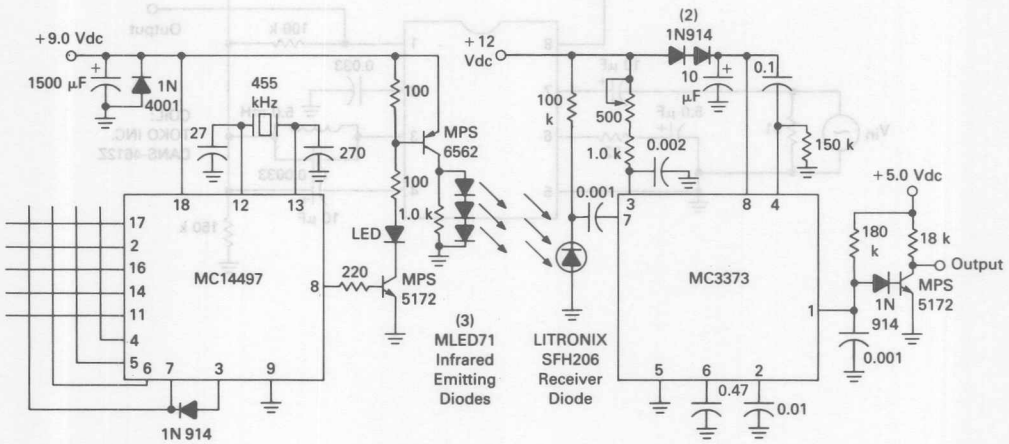
P SUFFIX
PLASTIC PACKAGE
CASE 626-05

Pin Connections



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FIGURE 1 — REMOTE CONTROL APPLICATION



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	15	Vdc
Operating Temperature Range	T_A	0 to 75	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Junction Temperature	T_J	150	°C
Power Dissipation, Package Rating Derate above 25°C	P_D $1/\theta JA$	1.25 10	Watts mW/°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage (25°C)	V_{CC}	4.75	—	15	Vdc
Power Supply Voltage (0°C)	V_{CC}	5.0	—	15	Vdc
Input Frequency	f_{in}	30	40	80	kHz

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V, f_{in} = 40 kHz, Test circuit of Figure 2)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Current	I_{CC}	1.5	2.5	3.5	mAdc
Input Terminal Voltage	V(Pin 7)	2.4	2.8	3.0	Vdc
Input Voltage Threshold	V_{in}	—	50	100	μV_{P-P}
Input Amplifier Voltage Gain (V[Pin 3] = 500 mV_{P-P})	A_V	—	60	—	dB
Input Impedance	r_{in}	40	60	80	kΩ
Output Voltage, V_{in} = 1.0 mV_{P-P}	V_{OL}	—	—	0.5	V
Output Leakage, V_{CC} = V_{OH} = 15 Vdc	I_{OH}	—	—	2.0	μA
Output Voltage, Input Open	V_{OH}	—	—	5.0	Vdc

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FIGURE 2 — TEST CIRCUIT

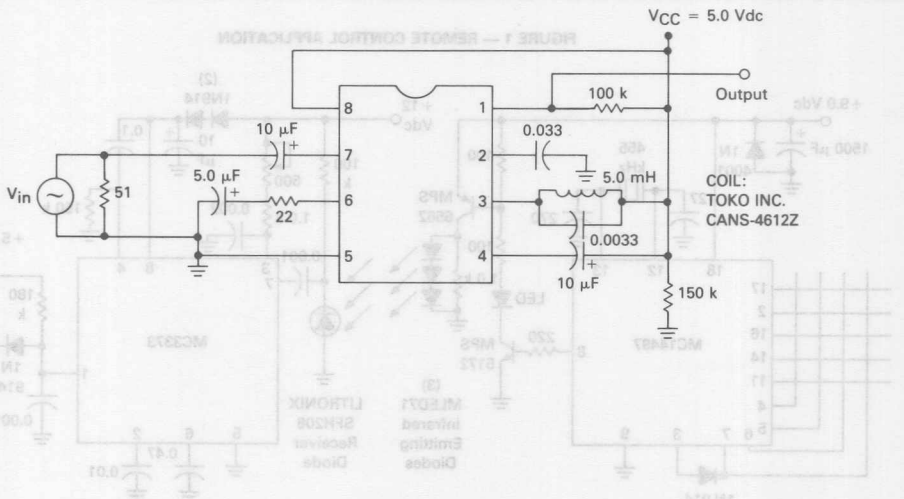


FIGURE 3 — BLOCK DIAGRAM

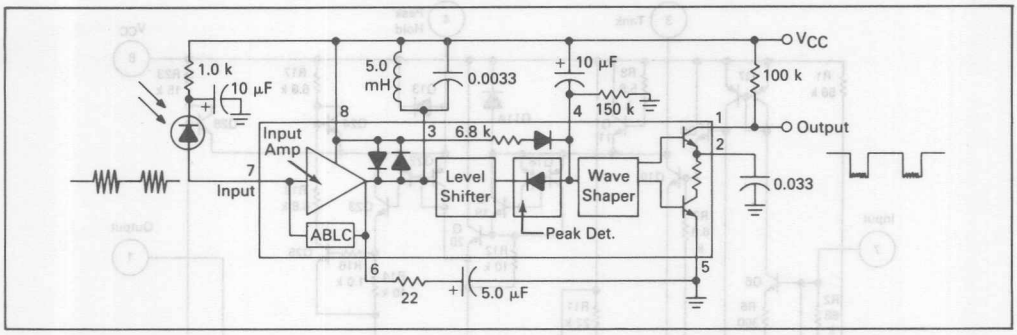


FIGURE 4 — INPUT AMPLIFIER GAIN

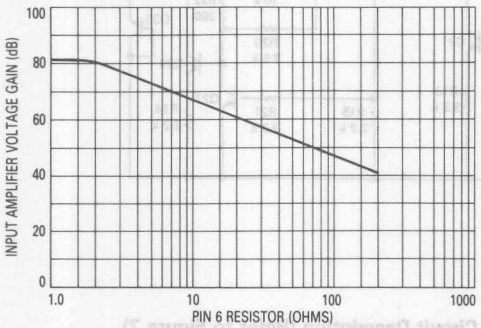


FIGURE 5 — DETECTOR THRESHOLD

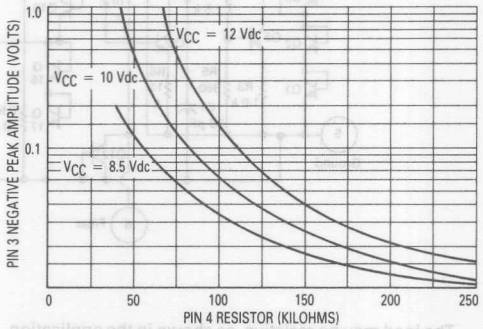
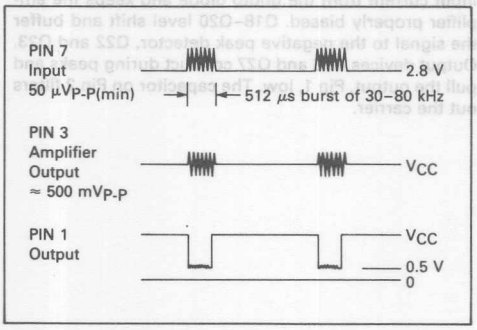


FIGURE 6 — TYPICAL SIGNAL WAVEFORMS

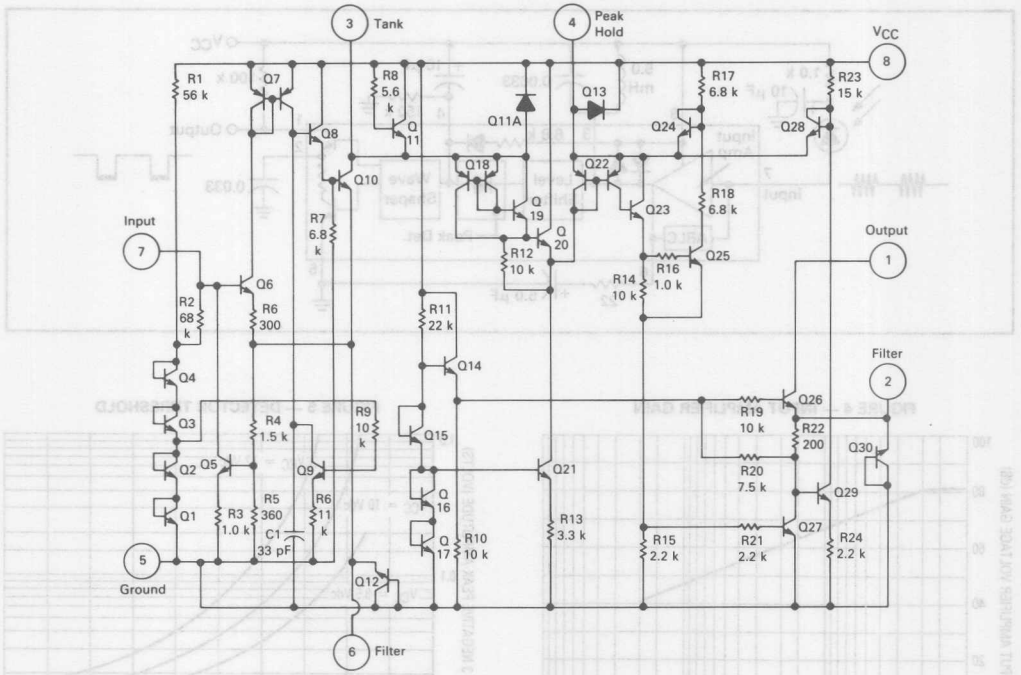


APPLICATIONS INFORMATION

The MC3373 is designed to amplify and detect the signal from an infrared receiver diode in a remote control system. The signal is generally in the form of ultrasonic bursts, ranging in amplitude from 50 μV_{P-P} to several hundred millivolts. The receiver diode may be directly connected to the MC3373 to save parts; the input is internally compensated by an ABLC (automatic bias level control). However, it is advantageous to ac couple the input, as shown in Figure 1, in order to provide attenuation of the power line frequency IR inputs, which are plentiful in most cases.

The input amplifier gain is approximately equal to the load impedance at Pin 3, divided by the resistor from Pin 6 to ground. Again, the low frequency gain can be reduced by using a small coupling capacitor in series with the Pin 6 resistor.

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The load may be resistive, as shown in the application circuit, or tuned, as in the test circuit. The amplifier output is limited by back-to-back clamping diodes, level shifted, buffered and fed to a negative peak detector. The detector threshold is set by the external resistor on Pin 4, and an internal 6.8 kΩ resistor and diode to V_{CC}. The capacitor from V_{CC} to Pin 4 quickly charges during the negative peaks and then settles toward the set-up voltage between signal bursts at a rate roughly determined by the value of the capacitor and the 6.8 k resistor. The external capacitor at Pin 2 filters the ultrasonic carrier from the pulses.

Circuit Description (Refer to Figure 7)

Q1–Q4 set the bias on the amplifier input at approximately 2.8 V. Q6–Q10 form the input amplifier, which has a gain of about 80 dB when R(Pin 6) = 0. Q5 sinks input current from the photo diode and keeps the amplifier properly biased. Q18–Q20 level shift and buffer the signal to the negative peak detector, Q22 and Q23. Output devices Q26 and Q27 conduct during peaks and pull the output, Pin 1, low. The capacitor on Pin 2 filters out the carrier.

MOTOROLA

MC10320
MC10320-1

Specifications and Applications Information

TRIPLE 4-BIT COLOR PALETTE VIDEO DAC

The MC10320 integrates a triple 4-bit digital-to-analog converter and a 16 x 12 color look-up table into a single 28 pin IC for use in a high resolution color graphics display system. The outputs are EIA-343-A compatible red, blue, and green video signals capable of driving single or doubly terminated 50 ohm or 75 ohm cables directly. Complementary outputs are provided for custom displays.

Control inputs include $\overline{\text{BLANK}}$ and $\overline{\text{SYNC}}$ to produce the levels required for vertical and horizontal retrace.

The color look-up table allows up to 16 color combinations (out of a palette of 4096 possible colors) on the screen at any one time. The table can be updated as often as required.

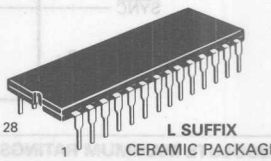
The lower speed digital inputs ($\overline{\text{WRITE}}$, DATA, and $\overline{\text{SYNC}}$) are TTL compatible, whereas the high speed inputs (ADDRESS, PIXEL CLOCK, and $\overline{\text{BLANK}}$) can be user programmed to either ECL or TTL compatability. The address and blank signals are latched into input registers, facilitating the timing requirements for those signals. Additional registers frame the data as it is presented to the three DACs, ensuring low glitch area and matched response.

Innovative level translators permit the MC10320 series to be used in single or dual supply systems, permitting compatability with most any system configuration. The MC10320 series is fabricated with Motorola's MOSAIC process, which provides both low power consumption and high speed.

- Triple 4-Bit Video DAC with 16 x 12 Color Look-Up Table
- 125 MHz Max Pixel Rate (MC10320), 90 MHz Max (MC10320-1)
- User Selectable TTL or ECL Compatability on High Speed Inputs
- Single/Dual Supply Operation (Inputs and/or Outputs May Be Above/Below Ground)
- Supply Sensitivity Typically −34 dB
- EIA-343-A Compatible Output Levels
- Directly Drives 50 or 75 Ohm Cables
- Low Power Dissipation — 684 mW Typical
- Internal Bandgap Reference
- $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ Control Inputs

TRIPLE 4-BIT COLOR PALETTE VIDEO DAC

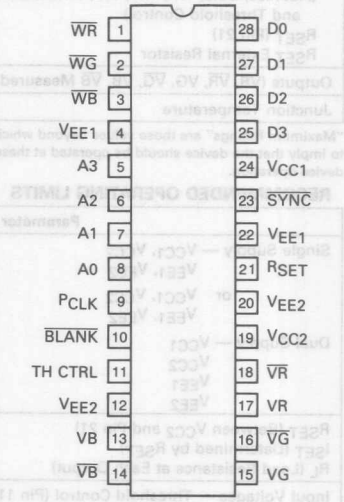
SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 733-04

PIN CONNECTIONS

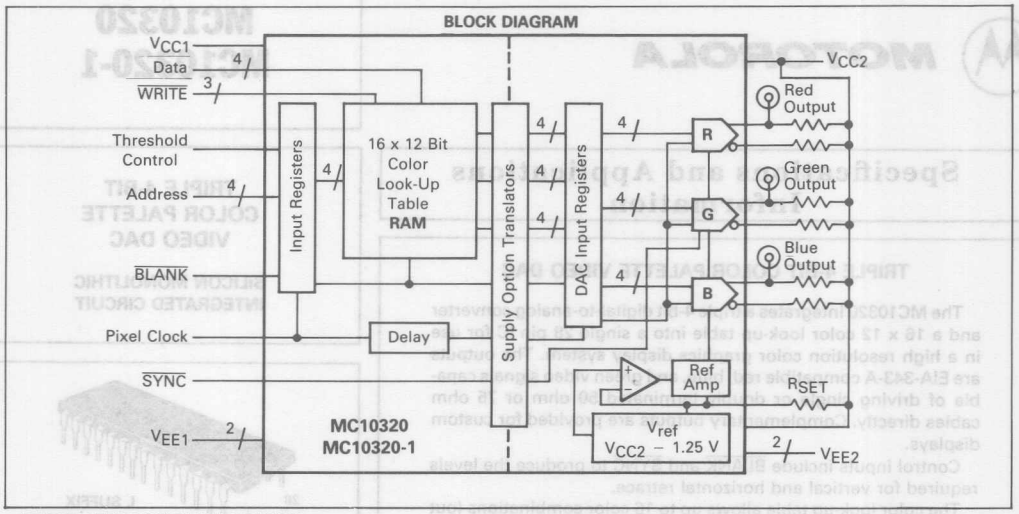
(Top View)



ORDERING INFORMATION

Maximum Pixel Rate	Device
125 MHz	MC10320L
90 MHz	MC10320L-1

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ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Units
Supply Voltages		Vdc
V_{CC1} (Measured to V_{EE1})	−0.5, +7.0	
V_{CC2} (Measured to V_{EE2})	−0.5, +7.0	
V_{EE1} (Measured to V_{EE2})	−0.5, +7.0	
V_{CC2} (Measured to V_{EE1})	−0.5, +7.0	
Input Voltages		
(Address, Data, $\overline{WR}$, $\overline{WG}$, $\overline{WB}$, $\overline{SYNC}$, $\overline{BLANK}$, P_{CLK}, and Threshold Control)	V_{EE1} − 0.5, V_{CC1} + 0.5	Vdc
R_{SET} (Pin 21)	V_{EE2} − 0.5, V_{CC2}	Vdc
R_{SET} External Resistor	0, 3.0 k	Ω
Outputs (VR, $\overline{VR}$, VG, $\overline{VG}$, VB, $\overline{VB}$ Measured to V_{EE2})	+2.5, +8.0	Vdc
Junction Temperature	−55, +150	°C

"Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The "Recommended Operating Limits" provide for actual device operation.

RECOMMENDED OPERATING LIMITS

Parameter	Min	Typ	Max	Units
Single Supply — V_{CC1}, V_{CC2}	4.5	5.0	5.5	Vdc
V_{EE1}, V_{EE2}	—	0	—	
or V_{CC1}, V_{CC2}	—	0	—	
V_{EE1}, V_{EE2}	−4.5	−5.0	−5.72	
Dual Supply — V_{CC1}	4.5	5.0	5.5	
V_{CC2}	—	0	—	
V_{EE1}	—	0	—	
V_{EE2}	−4.5	−5.0	−5.72	
R_{SET} (Between V_{CC2} and Pin 21)	500	1.0 k	2.0 k	Ω
I_{SET} (Determined by R_{SET})	0.55	1.25	2.8	mA
R_L (Load Resistance at Each Output)	0	—	75	Ω
Input Voltages — Threshold Control (Pin 11, See Text)	V_{EE1}	—	V_{CC1}	Vdc
TTL High (Pins 1–3, 5–10, 23, 25–28,	V_{EE1} + 2.0	—	V_{CC1}	
TTL Low Pin 11 connected to V_{EE1})	V_{EE1}	—	V_{EE1} + 0.8	
ECL High (Pins 5–10 only, Pin 11	V_{CC1} − 1.13	—	V_{CC1}	
ECL Low connected to V_{CC1})	V_{EE1}	—	V_{CC1} − 1.48	
Output Compliance (Measured to V_{CC2})	−2.0	0	+2.0	Vdc
Ambient Temperature	0	—	+70	°C

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ELECTRICAL CHARACTERISTICS (See Figure 1, T_A = 25°C)

Parameter	Symbol	Min	Typ	Max	Units
Resolution (Each DAC)	Res	4.0	4.0	4.0	Bits
Palette Colors (Active)	—	—	—	16	Colors
(Total Available)	—	—	—	4096	Colors
Integral Nonlinearity	INL	−1/4	0	+1/4	LSB
Differential Nonlinearity	DNL	−1/4	0	+1/4	LSB
Monotinicity	—		Guaranteed*		
Output Levels @ VR, VG, VB, relative to V_{CC2} unless otherwise noted.					
Ref. White Offset (DAC Input = 1111)	I_{OW}	—	50	400	μA
$\overline{BLANK}$, $\overline{SYNC}$ = 1	V_{OW}	−15	−1.9	—	mV
Ref. Black (DAC Input = 0000) Relative to	I_{OB}	16.1	17.2	18.2	mA
Ref. White, $\overline{BLANK}$, $\overline{SYNC}$ = 1	V_{OB}	−682	−645	−604	mV
Blank Level Relative to Ref. Black	I_{OBK}	1.17	1.33	1.5	mA
$\overline{BLANK}$ = 0, $\overline{SYNC}$ = 1	V_{OBK}	−56.2	−50	−43.9	mV
Sync Level — VG Only, Relative to Blank	I_{OSY}	6.71	7.63	8.54	mA
$\overline{SYNC}$, $\overline{BLANK}$ = 0	V_{OSY}	−320	−286	−251	mV
Total Error (Each DAC, Ref. White to Ref. Black)	G_{ER}	−6.0	0	+6.0	%
Gain Tracking Error (Any two DACs @ Ref. Black)	G_{TR}	−3.0	0	+3.0	%
Output Impedance @ VR, VG, VB	Z_o	10	100	—	kΩ
Reference Voltage (V_{CC2} − V_{RSET}, R_{SET} = 1.0 kΩ)	V_{REF}	−1.4	−1.25	−1.1	Vdc
Pin 21 Output DC Resistance (0 mA < I_{REF} < 3.0 mA)	—	—	3.0	—	Ω
Input Voltage High (Data, $\overline{WR}$, $\overline{WG}$, $\overline{WB}$, $\overline{SYNC}$)	V_{IHA}	V_{EE1} + 2.0	—	V_{CC1}	Vdc
Low (Data, $\overline{WR}$, $\overline{WG}$, $\overline{WB}$, $\overline{SYNC}$)	V_{ILA}	V_{EE1}	—	V_{EE1} + 0.8	
Input Voltage High (Address, P_{CLK}, $\overline{BLANK}$)					
(Threshold Control @ V_{EE1} [TTL Mode])	V_{IHB}	V_{EE1} + 2.0	—	V_{CC1}	
(Threshold Control @ V_{CC1} [ECL Mode])	V_{IHC}	V_{CC1} − 1.13	—	V_{CC1}	
Input Voltage Low (Address, P_{CLK}, $\overline{BLANK}$)					
(Threshold Control @ V_{EE1} [TTL Mode])	V_{ILB}	V_{EE1}	—	V_{EE1} + 0.8	
(Threshold Control @ V_{CC1} [ECL Mode])	V_{ILC}	V_{EE1}	—	V_{CC1} − 1.48	
Input Current @ 2.4 V (TTL Mode) (All Input Pins	I_{IHA}	—	50	150	μA
@ 0.4 V (TTL Mode) Except Pin 11)	I_{ILA}	—	10	100	
Input Current @ V_{CC1} − 0.8 V (ECL Mode)	I_{IHB}	—	100	250	
@ V_{CC1} − 1.8 V (ECL Mode)	I_{ILB}	—	70	200	
Input Current @ Pin 11 (Pin 11 = V_{CC1})	I_{ITH}	−5.0	0	—	mA
@ Pin 11 (Pin 11 = V_{EE1})	I_{ITL}	−1.0	−0.4	—	
Signal Feedthrough to Outputs Due to	SRR				dB
Pixel Clock (@ 125 MHz for MC10320,		—	−50	—	
$\overline{BLANK}$ 90 MHz MC10320-1)		—	−50	—	
Data		—	−60	—	
Power Supply Rejection Ratio (All DACs)	PSRR				dB
V_{CC1} @ 1.0 kHz		—	60	—	
V_{CC1} @ 1.0 MHz		—	45	—	
V_{CC1} @ 50 MHz		—	30	—	
V_{EE2} @ 1.0 kHz		—	50	—	
V_{EE2} @ 1.0 MHz		—	33	—	
V_{EE2} @ 50 MHz		—	12	—	
Power Supply Sensitivity**		—	0.02	0.12	%/%
Power Supply Requirements (See Figure 1)					mA
V_{CC1} Current (V_{CC1} − V_{EE1} = 5.0 V)	I_{CC1}	—	50	70	
V_{EE1} Current (V_{CC1} − V_{EE1} = 5.0 V)	I_{EE1}	—	−50	−70	
V_{CC2} Current (V_{CC2} − V_{EE2} = 5.0 V)	I_{CC2}	—	28	45	
V_{EE2} Current (V_{CC2} − V_{EE2} = 5.0 V, Includes output currents)	I_{EE}	—	−92	−120	
Power Dissipation (@ 5.0 volt supplies)	P_D	—	684	894	mW

*Guaranteed by linearity tests.

**(V_{CC1} − V_{EE1}) and (V_{CC2} − V_{EE2}) are each varied from 4.5 to 5.72 volts, but not simultaneously.

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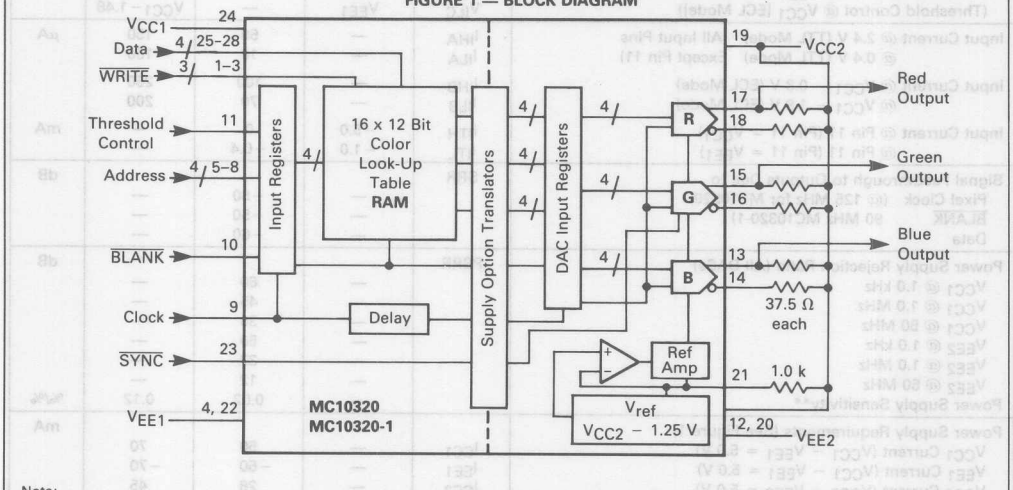
Parameter	Symbol	Min	Typ	Max	Units
READ Cycle (Display Mode)					
Address, $\overline{\text{BLANK}}$ Setup Time	t_{RSA}	—	1.5	—	ns
Address, $\overline{\text{BLANK}}$ Hold Time	t_{RHA}	—	1.5	—	ns
Clock Pulse Width — High	t_{PWH}	—	3.0	—	ns
Clock Pulse Width — Low	t_{PWL}	—	3.0	—	ns
Pipeline Delay	t_{PIPE}	1.0	1.0	1.0	clk cycle
DAC Prop Delay (P_{CLK} to 50% Point)	t_{DPD}	—	9.0	—	ns
DAC Prop Delay Difference (DAC to DAC)	$t_{DPD\Delta}$	—	0.5	—	ns
$\overline{\text{SYNC}}$ Prop Delay	t_{SPD}	—	6.0	—	ns
Output Settling Time (±1/2 LSB to ±1/2 LSB)	t_{DS}	—	3.0	—	ns
Output Slew Rate	SR	—	300	—	V/μs
Glitch Area	A_G	—	20	—	pV-S
WRITE Cycle (RAM Update Mode)					ns
Address Setup Time	t_{WSA}	—	1.5	—	
Address Hold Time	t_{WHA}	—	1.5	—	
Clock Setup Time	t_{WSC}	—	5.0	—	
Clock Hold Time	t_{WHC}	—	10	—	
Data Setup Time	t_{WSD}	—	90	—	
Data Hold Time	t_{WHD}	—	10	—	
Write Pulse Width	t_{WPW}	—	90	—	

TEMPERATURE CHARACTERISTICS (0°C to +70°C)

Parameter	Typ	Units
Offset (at Ref. White)	±20	ppm GS/°C
DAC Gain	±100	ppm GS/°C
Gain Tracking (any 2 DACs @ Ref. Black)	±50	ppm GS/°C
Linearity	±100	ppm GS/°C

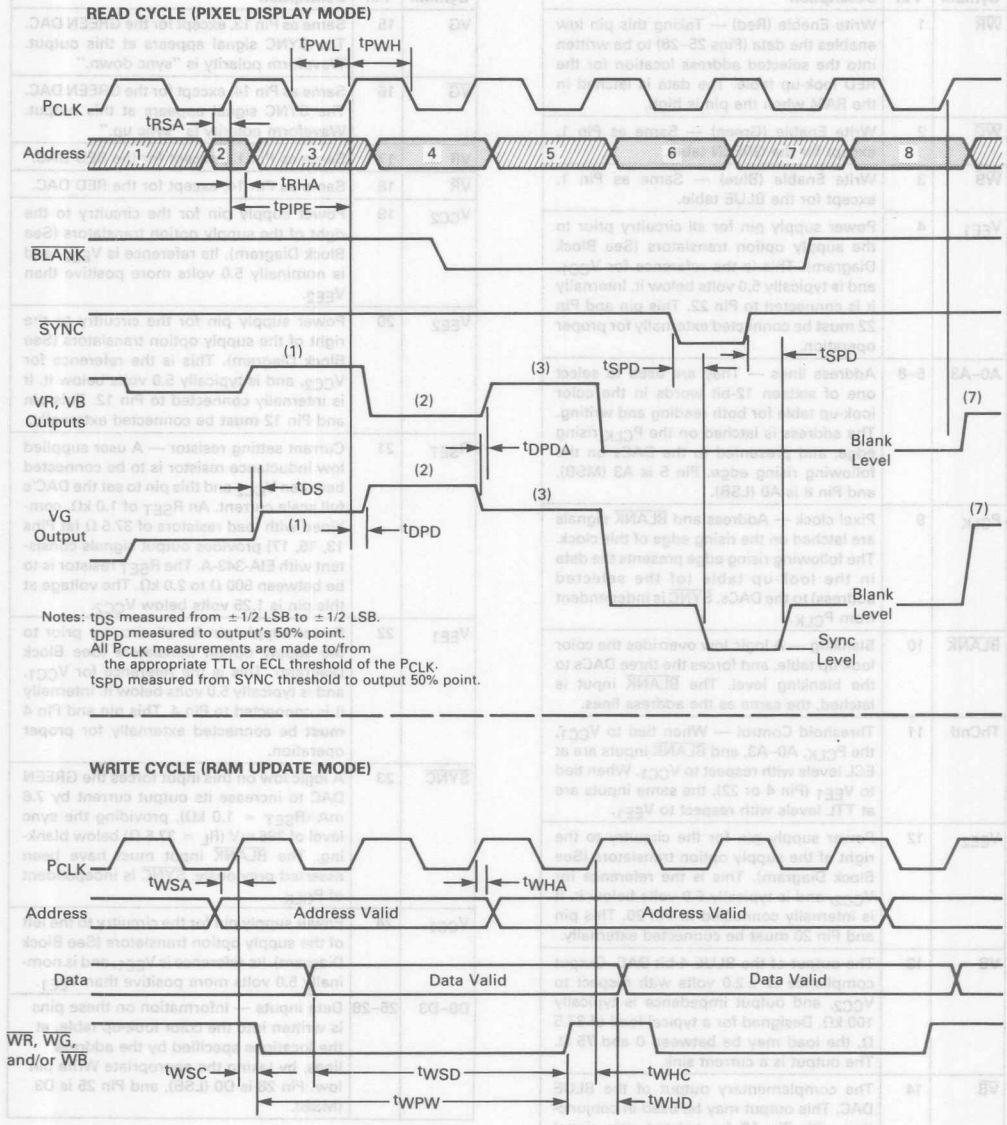
Note: ppm GS/°C = Parts Per Million of Grey Scale/°C.

FIGURE 1 — BLOCK DIAGRAM



Note:
Electrical Characteristics are tested with both single and dual supply configurations at the typical supply voltages listed in the "Recommended Operating Limits." Input levels are TTL or ECL, as appropriate. Threshold control input is set at V_{CC1}, or V_{EE1}, as appropriate. Exceptions to these conditions are noted in the Characteristics.

FIGURE 2 — TIMING DIAGRAM



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PIN DESCRIPTIONS

Symbol	Pin	Description
$\overline{WR}$	1	Write Enable (Red) — Taking this pin low enables the data (Pins 25–28) to be written into the selected address location for the RED look-up table. The data is latched in the RAM when the pin is high.
$\overline{WG}$	2	Write Enable (Green) — Same as Pin 1, except for the GREEN table.
$\overline{WB}$	3	Write Enable (Blue) — Same as Pin 1, except for the BLUE table.
V_{EE1}	4	Power supply pin for all circuitry prior to the supply option translators (See Block Diagram). This is the reference for V_{CC1}, and is typically 5.0 volts below it. Internally it is connected to Pin 22. This pin and Pin 22 **must** be connected externally for proper operation.
A0–A3	5–8	Address lines — They are used to select one of sixteen 12-bit words in the color look-up table for both reading and writing. The address is latched on the P_{CLK} rising edge, and presented to the DACs on the following rising edge. Pin 5 is A3 (MSB), and Pin 8 is A0 (LSB).
P_{CLK}	9	Pixel clock — Address and $\overline{BLANK}$ signals are latched on the rising edge of this clock. The following rising edge presents the data in the look-up table (of the selected address) to the DACs. $\overline{SYNC}$ is independent from P_{CLK}.
$\overline{BLANK}$	10	Blanking — A logic low overrides the color look-up table, and forces the three DACs to the blanking level. The $\overline{BLANK}$ input is latched, the same as the address lines.
ThCntl	11	Threshold Control — When tied to V_{CC1}, the P_{CLK}, A0–A3, and $\overline{BLANK}$ inputs are at ECL levels with respect to V_{CC1}. When tied to V_{EE1} (Pin 4 or 22), the same inputs are at TTL levels with respect to V_{EE1}.
V_{EE2}	12	Power supply pin for the circuitry to the right of the supply option translators (See Block Diagram). This is the reference for V_{CC2}, and is typically 5.0 volts below it. It is internally connected to Pin 20. This pin and Pin 20 **must** be connected externally.
VB	13	The output of the BLUE 4-bit DAC. Output compliance is ±2.0 volts with respect to V_{CC2}, and output impedance is typically 100 kΩ. Designed for a typical load of 37.5 Ω, the load may be between 0 and 75 Ω. The output is a current sink.
$\overline{VB}$	14	The complementary output of the BLUE DAC. This output may be used in conjunction with Pin 13 for twisted pair signal transmission or for custom interface schemes. If unused, it must be tied to V_{CC2}.

PIN DESCRIPTIONS

Symbol	Pin	Description
VG	15	Same as Pin 13, except for the GREEN DAC. The SYNC signal appears at this output. Waveform polarity is "sync down."
$\overline{VG}$	16	Same as Pin 14, except for the GREEN DAC. The SYNC signal appears at this output. Waveform polarity is "sync up."
VR	17	Same as Pin 13, except for the RED DAC.
$\overline{VR}$	18	Same as Pin 14, except for the RED DAC.
V_{CC2}	19	Power supply pin for the circuitry to the right of the supply option translators (See Block Diagram). Its reference is V_{EE2}, and is nominally 5.0 volts more positive than V_{EE2}.
V_{EE2}	20	Power supply pin for the circuitry to the right of the supply option translators (See Block Diagram). This is the reference for V_{CC2}, and is typically 5.0 volts below it. It is internally connected to Pin 12. This pin and Pin 12 **must** be connected externally.
R_{SET}	21	Current setting resistor — A user supplied low inductance resistor is to be connected between V_{CC2} and this pin to set the DAC's full scale current. An R_{SET} of 1.0 kΩ, combined with load resistors of 37.5 Ω (at Pins 13, 15, 17) provides output signals consistent with EIA-343-A. The R_{SET} resistor is to be between 500 Ω to 2.0 kΩ. The voltage at this pin is 1.25 volts below V_{CC2}.
V_{EE1}	22	Power supply pin for all circuitry prior to the supply option translators (See Block Diagram). This is the reference for V_{CC1}, and is typically 5.0 volts below it. Internally it is connected to Pin 4. This pin and Pin 4 **must** be connected externally for proper operation.
$\overline{SYNC}$	23	A logic low on this input forces the GREEN DAC to increase its output current by 7.6 mA (R_{SET} = 1.0 kΩ), providing the sync level of 286 mV (R_L = 37.5 Ω) below blanking. The $\overline{BLANK}$ input must have been asserted previously. $\overline{SYNC}$ is independent of P_{CLK}.
V_{CC1}	24	Power supply pin for the circuitry to the left of the supply option translators (See Block Diagram). Its reference is V_{EE1}, and is nominally 5.0 volts more positive than V_{EE1}.
D0–D3	25–28	Data inputs — Information on these pins is written into the color look-up table, at the locations specified by the address lines, by taking the appropriate Write pin low. Pin 28 is D0 (LSB), and Pin 25 is D3 (MSB).

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FUNCTIONAL DESCRIPTION

GENERAL

The MC10320 is a triple video DAC, with a 16 location color palette RAM, designed for high resolution graphics systems. The maximum pixel speed capability is 125 MHz for the MC10320, and 90 MHz for the MC10320-1. The input configurations are compatible with TTL or ECL systems, and the outputs are directly compatible with monitors having 50 Ω or 75 Ω RGB inputs. Using the external components recommended in this data sheet, the outputs will conform to EIA-343-A levels. The output levels are adjustable by means of the R_{SET} resistor.

The MC10320 contains three 4-bit DACs whose inputs are fed from a color palette RAM (data is loaded by the user). The RAM contains 16 locations (each 12 bits wide). Each 4-bit nibble of each RAM address can be individually loaded, so that every address location can have any one of a possible 4096 codes. The DAC output levels are determined by the contents of the selected RAM address (by means of the address inputs).

The MC10320 contains an input register to accept the address and Blanking information, and a second register located between the RAM and the DAC inputs. This arrangement ensures that the RAM data is presented to the 3 DACs simultaneously, which ensures the DAC outputs will transition simultaneously. The registers are toggled by the P_{CLK} input's rising edge.

The $\overline{BLANK}$ input overrides the RAM data to the DACs, and forces the outputs to the Blanking level. The $\overline{SYNC}$ input goes directly to the Green DAC, bypassing the RAM and the latches, forcing the green DAC output to shift. The combination of $\overline{BLANK}$ and $\overline{SYNC}$ produce the video sync level.

Referring to the Block Diagram, the input stage (circuitry to the left of the Supply Option Translators) and the output stage (to the right of the Translators) can be operated at different supply voltages. The only restriction is that the output stage cannot be more positive than the input stage.

INPUTS

Address, P_{CLK}, $\overline{BLANK}$

The Address, P_{CLK} (pixel clock), and $\overline{BLANK}$ inputs are the "high speed" inputs capable of the maximum pixel clock rates mentioned above. The Address and $\overline{BLANK}$ are latched into the input register on the rising edge of the P_{CLK}, as long as the required setup and hold times are adhered to. The data at that RAM address (or the $\overline{BLANK}$ signal) is then presented to the DAC inputs on the next P_{CLK} rising edge.

The $\overline{BLANK}$ input, when taken to a Logic "0" and clocked in as described above, will override the RAM data presented to the DACs, and force the 3 DAC outputs to the Blanking level (see Figure 2).

These 6 input pins can accept either TTL or ECL signals. With the Threshold Control pin (Pin 11) connected to V_{EE1}, the inputs are TTL compatible with respect to V_{EE1}, having a nominal threshold of 1.5 volts above V_{EE1}, independent of V_{CC1}. With Pin 11 connected to V_{CC1}, the inputs are fully compatible with the 10KH family of ECL devices, having a nominal threshold of 1.3 volts below V_{CC1}, independent of V_{EE1}.

Figure 3 depicts a typical input stage configuration, and Figure 4 indicates the typical input current. Figure 4 applies to both ECL and TTL modes of operation. The inputs should be kept within the range of V_{EE1} to V_{CC1}. If an input is taken more than 0.3 volt below V_{EE1}, or more than 0.5 volts above V_{CC1}, excessive currents will flow through that input, and the DAC output waveforms will be distorted.

$\overline{SYNC}$

The $\overline{SYNC}$ input goes directly to the green DAC, independent of the clock. When taken to a Logic "0", the output current at VG is forced to increase by 6.1 x I_{SET}. For a standard EIA-343-A system, the shift is 7.63 mA, resulting in a 286 mV change in the output voltage. The $\overline{SYNC}$ input does **not** override the RAM data, requiring that the $\overline{BLANK}$ input have been asserted (Logic "0") previously in order to obtain a proper video sync level. The $\overline{SYNC}$ input does not affect the red or blue DACs.

The $\overline{SYNC}$ input is always TTL compatible, with a nominal threshold of 1.5 volts above V_{EE1}, independent of V_{CC1}.

Figure 3 depicts the input stage configuration, and Figure 4 indicates the typical input current. The input should be kept within the range of V_{EE1} to V_{CC1}. If the input is taken more than 0.3 volt below V_{EE1}, or more than 0.5 volts above V_{CC1}, excessive currents will flow through the input, and the DAC output waveforms will be distorted.

DATA (1–4), $\overline{WR}$, $\overline{WB}$, $\overline{WG}$

The data (D0, D1, D2, D3), and $\overline{WRITE}$ inputs are the "low speed" inputs, as they do not have to operate at the same high speed as the above mentioned inputs. These inputs are independent of the P_{CLK}, although they are normally used in conjunction with the clock.

Pins 25–28 are the data inputs to the color palette RAM, and are used for updating the RAM information. The information is written into the RAM at the address which was previously clocked into the input register, while the appropriate $\overline{WRITE}$ input is low, and then latched in when the $\overline{WRITE}$ input is taken high. The required data setup and hold times (mentioned in the Timing Characteristics) are with respect to the rising edge of the $\overline{WRITE}$ input. If the same data is to be loaded into different nibbles (color sections) of the same address, the appropriate $\overline{WRITE}$ inputs may be taken low simultaneously, or sequentially. $\overline{WR}$, $\overline{WB}$, and $\overline{WG}$ control the loading of data into the red, blue and green nibbles respectively.

The data and $\overline{WRITE}$ inputs are always TTL compatible, with a nominal threshold of 1.5 volts above V_{EE1}, independent of V_{CC1}.

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In most applications, it will be advantageous to set the Blanking level while updating the RAM. If Blanking is not set, the DAC outputs will change unpredictably while new data is being written into the RAM.

Figure 3 depicts a typical input stage configuration, and Figure 4 indicates the typical input current. The inputs should be kept within the range of V_{EE1} to V_{CC1}. If an input is taken more than 0.3 volt below V_{EE1}, or more than 0.5 volts above V_{CC1}, excessive currents will flow through the input, and the DAC output waveforms will be distorted.

FIGURE 3 — TYPICAL INPUT STAGE

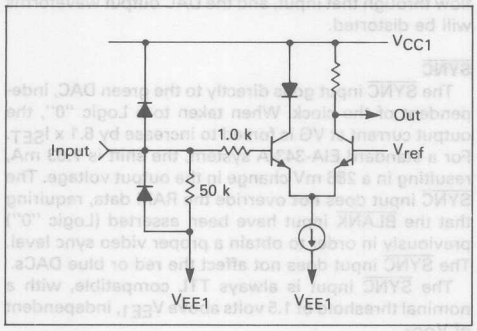
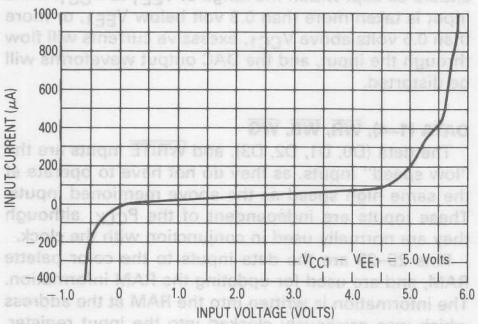


FIGURE 4 — INPUT CURRENT AT PINS 1–3, 5–10, 23, 25–28



THRESHOLD CONTROL

The Threshold Control input (Pin 11) is to be connected directly to V_{CC1} to set Pins 5–10 to ECL compatibility, or directly to V_{EE1} to set the pins to TTL compatibility. A series resistor should not be used with this input, and it should not be connected to any other voltage as an incorrect threshold will result at Pins 5–10. Bias current at Pin 11 is approximately 400 μA out of the pin when at V_{EE1}, and 0 μA when at V_{CC1}. If the pin is taken more than 0.3 volt below V_{EE1}, excessive currents will flow through this input, and the DAC output waveforms will be distorted.

OUTPUTS

The six DAC outputs (VB, $\overline{VB}$, VG, $\overline{VG}$, VR, $\overline{VR}$) at Pins 13–18 are high impedance current sink outputs, with the current flow **into** the pins, never out. VG, VB, and VR provide the conventional video polarity (sync down), while the complementary outputs provide a "sync up" waveform. The output loads must be connected from the outputs to V_{CC2}, or to a pullup voltage, such that the output voltages are within ±2.0 volts of V_{CC2}. Unused outputs **must** be connected to V_{CC2}, and not left open.

The output current (for the gray scale) at Pins 13, 15, and 17 is related to the digital inputs (of the DACs) and the reference current (I_{SET} at Pin 21, equal to 1.25 V/R_{SET}) by the following equation:

$$I_{OUT(GS)} = \frac{(15\text{-}A) \times I_{SET} \times 14.63}{16} \quad \text{(nominal value)}$$

where A = binary value of the digital input (0–15). A digital input of 1111 (15) produces no output current, and therefore the most positive output voltage, referred to as "Reference White." An input code of 0000 (0) results in the maximum current, and therefore the gray scale's most negative output voltage, referred to as "Reference Black."

After the $\overline{BLANK}$ input is asserted and clocked in as described above, the RAM data to the DACs is overriden, and the output current is set at:

$$I_{OUT(BLANK)} = I_{SET} \times 14.864 \quad \text{(nominal value)}$$

When the $\overline{SYNC}$ input is asserted, the output current at VG is increased by:

$$\Delta I_{OUT(SYNC)} = I_{SET} \times 6.1 \quad \text{(nominal value)}$$

The four outputs of the red and blue DACs are not affected by $\overline{SYNC}$. The current increase at VG results regardless of the digital input to the Green DAC. To obtain the correct (EIA-343-A) sync level, the $\overline{BLANK}$ output level must have previously been set. Otherwise the green output will simply shift by the above amount from the grey scale level in effect at the time the $\overline{SYNC}$ input was asserted. If both $\overline{BLANK}$ and $\overline{SYNC}$ are asserted, the output current at VG is:

$$I_{OUT(SYNC)} = I_{SET} \times 20.97 \quad \text{(nominal value)}$$

The sum of the currents into each pair of outputs is a constant equal to [20.93 x I_{SET}] for the VG/$\overline{VG}$ pair, and [14.824 x I_{SET}] for the VR/$\overline{VR}$, and VB/$\overline{VB}$ pairs. Table 1 summarizes the above information.

The voltage levels generated at the outputs depend on the value of I_{SET} and the load impedance. An R_{SET} of 1.0 kΩ (I_{SET} = 1.25 mA), and a load of 37.5 Ω (doubly terminated 75 Ω system) at each output will generate the standard EIA-343-A levels. The output voltages must be kept within the range of +2.0 to −2.0 volts **with respect to V_{CC2}**. If any part of the output's waveform is outside this range, its linearity will be affected.

TABLE 1

Video Level	Output Current (mA) at:			
	VR, VB	VG	$\overline{VR}$, $\overline{VB}$	$\overline{VG}$
Gray Scale	$\left(\frac{(15\text{-}A) \times I_{SET}}{1.09}\right)$	Same as VB, VR	$\left(\frac{(A) \times I_{SET}}{1.09} + 1.06\ I_{SET}\right)$	$\left(\frac{(A) \times I_{SET}}{1.09} + 7.17\ I_{SET}\right)$
Blank	$I_{SET} \times 14.824$	Same as VB, VR	0 mA	$I_{SET} \times 6.1$
Sync + Blank	$I_{SET} \times 14.824$	$I_{SET} \times 20.93$	0 mA	0 mA

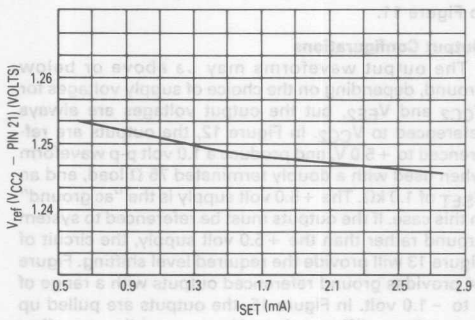
A = DAC digital input (binary value), I_{SET} is the current into Pin 21.

REFERENCE VOLTAGE (R_{SET})

The reference current for the DACs is supplied from an internal band-gap reference with a typical TC of ≈ ±50 ppm/°C. The voltage at R_{SET} (Pin 21) is a constant 1.25 volts below V_{CC2}, and an external resistor R_{SET} is to be connected from V_{CC2} to Pin 21. The current I_{SET} is therefore equal to 1.25 V/R_{SET}. Internally, equal reference currents are supplied to the three DACs such that their outputs are matched within ±3.0%.

R_{SET} should normally be between 500 Ω and 2.0 kΩ. With values less than 500 Ω, the current at Pin 21 approaches an upper limit, resulting in a nonlinear relationship for the MC10320. With values greater than 2.0 kΩ, instability and oscillations of the reference amplifier will result. For this reason, current to Pin 21 should not be supplied from a current source. Additionally, the resistor should be noninductive (non-wirewound). Metal film resistors, available with low TCs, are recommended. The resistor should be physically adjacent to the MC10320 to avoid the inductive effects of long PC board tracks. Figure 5 indicates the voltage/current characteristics at Pin 21.

FIGURE 5 — V_{ref} versus I_{SET}



POWER SUPPLIES

The MC10320 may be used in a single or dual supply system, depending on the system logic levels, and/or the output requirements (See the Applications Section). Table 2 indicates permissable configurations. The only restriction is that the output stage (V_{CC2}/V_{EE2}) cannot be more positive than the input stage. The positive supplies may range from +4.5 to +5.5 volts, and negative supplies may range from −4.5 to −5.72 volts.

TABLE 2

System	V_{CC1}	V_{EE1}	V_{CC2}	V_{EE2}
Single Supply	+5.0 V	Gnd	+5.0 V	Gnd
Single Supply	Gnd	−5.0 V	Gnd	−5.0 V
Dual Supply	+5.0 V	Gnd	Gnd	−5.0 V

The current requirement for the input stage (I_{CC1}) is typically 50 mA, and the majority of that current (+0, −4.0 mA) flows out of V_{EE1}. The current requirement for the output stage (I_{CC2}) is typically 28 mA. Out of V_{EE2} flows that current, plus the current due to the outputs and I_{SET}. In a typical application the output currents total ≈63 mA, and I_{SET} is ≈1.25 mA, giving a total I_{EE2} of ≈92 mA.

The minimum voltage at V_{CC1} for memory retention is ≈1.5 volts.

Proper bypassing of the supplies **at the IC** is critical due to the high frequencies involved. Further information can be found in the Applications section.

TIMING

Timing diagrams for the Read (display) mode and the Write (RAM update) mode are shown in Figure 2.

In the READ mode, the clock may be any frequency up to 125 MHz for the MC10320, and up to 90 MHz for the MC10320-1. Duty cycle is not important as long as the minimum low and high times are observed. On each clock's rising edge, a new address is clocked in, and the previous address' information is supplied to the DACs from the look-up table. If the $\overline{BLANK}$ line is taken to a Logic "0", it will override the information to the DACs on the next clock rising edge, and the 3 DACs will be taken to the blanking level. The $\overline{SYNC}$ input, when taken to a Logic "0", drives the Green DAC directly with only a small internal propagation delay. The output of the Green DAC will then change with respect to the last address input. For this reason, the $\overline{SYNC}$ input should normally be used only after asserting the $\overline{BLANK}$ input.

In the WRITE mode, the clock is used only to enter the address where the new data is to be written. The P_{CLK} input may continue to toggle if the address inputs are stable during the write period, or the clock may be stopped while writing. Data is then entered into each of 3 color sections of that address by taking low the appropriate WRITE lines ($\overline{WR}$, $\overline{WG}$, $\overline{WB}$). If the same four bits are to be stored in different color locations of the same address, the appropriate WRITE lines may be taken low simultaneously. If the $\overline{BLANK}$ input is held low during the Write operation, the DAC outputs will be held in a known state.

9

APPLICATIONS INFORMATION

POWER SUPPLIES, GROUNDING

The PC board layout, and the quality of the power supplies and the ground system **at the IC** are very important in order to obtain proper operation. Noise, from any source, coming into the device can result in an incorrect output due to interaction with the analog portion of the circuit. At the same time, noise generated within the MC10320 can cause incorrect operation if that noise does not have a clear path to ac ground.

The power supply pins at both the input and output sections of the MC10320 must be decoupled to ground **at the IC** (within 1" max) with a 10 μF tantalum and a 0.1 μF ceramic. Tantalum capacitors are recommended since electrolytic capacitors simply have too much inductance at the frequencies of interest. The quality of the V_{CC} and V_{EE} supplies should then be checked at the IC with a high frequency scope. Noise spikes (always present among digital circuits) can easily exceed 400 mV peak, and if they get into the analog portion of the IC, the output waveforms can be disrupted. Noise can be reduced by inserting resistors and/or inductors between the supplies and the IC.

If switching power supplies are used, there will usually be spikes of 0.5 volts or greater at frequencies of 50–200 kHz. These spikes are generally more difficult to reduce because of their greater energy content. In extreme cases, 3-terminal regulators (MC78L05ACP, MC7805.2CT), with appropriate high frequency filtering, should be used and dedicated to the MC10320.

The ripple content of the supplies should not allow their magnitude to exceed the values in the Recommended Operating Limits.

The PC board tracks supplying V_{CC} and V_{EE} to the MC10320 should preferably not be at the tail end of the bus distribution, after passing through a maze of digital circuitry. The MC10320 should be close to the power supply, or the connector where the supply voltages enter the board. If the V_{CC} and V_{EE} lines are supplying considerable current to other parts of the board, then it is preferable to have dedicated lines from the supply or connector directly to the MC10320.

The two V_{EE1} pins (4 and 22) **must** be connected directly together. Likewise, the two V_{EE2} pins (12 and 20) **must** be connected directly together. Any long path between them can cause stability problems due to the inductance (@ 125 MHz) of the PC tracks. The ground return for the analog signals must be noise free.

PC Board Layout

Due to the high frequencies involved, and in particular, the fast edges of the various digital signals, proper PC board layout is imperative. A solid ground plane is necessary in order to have known transmission characteristics, and also to minimize coupling of the digital signals into the analog section. Use of wire wrapped boards should definitely be avoided.

Each PC track should be considered a transmission line, and if they are of any considerable length (more than a few inches), they should be terminated according to transmission line theory. Otherwise reflections back to the signal sources can occur, disrupting their operation. Additionally, the overshoots and undershoots which will occur at the MC10320's input pins can cause its operation to be disrupted, resulting in an incorrect output.

Additional information regarding the transmission characteristics of PC board tracks can be found in Motorola's MECL System Design Handbook (HB205R1).

Input Configurations

The unique configuration of the MC10320's power supply system permits its use in an all TTL, or all ECL, or mixed TTL/ECL environments, with the secondary capability of having the output levels be above or below ground. For standard TTL inputs refer to Figure 7. For systems using "above ground ECL" (ECL circuitry operated between ground and +5.0 volts, rather than −5.2 volts), refer to Figure 8. The MC10H350 translators will change the above ground ECL levels to the TTL levels required by the $\overline{\text{SYNC}}$, Data and $\overline{\text{WRITE}}$ inputs, while the Threshold Control will set the thresholds of the Address, Clock and $\overline{\text{BLANK}}$ inputs to the ECL levels. For standard (below ground) ECL levels, refer to Figure 9. Since V_{CC2} cannot be more positive than V_{CC1}, they are both connected to ground level in this case.

In the case where all inputs are above ground, but the low speed inputs (Data, $\overline{\text{WRITE}}$, and $\overline{\text{SYNC}}$) are connected to TTL circuits, while the high speed inputs are connected to above ground ECL circuits, refer to Figure 10. In the case where the low speed inputs are connected to standard TTL, and the high speed inputs are connected to standard (below ground) ECL, refer to Figure 11.

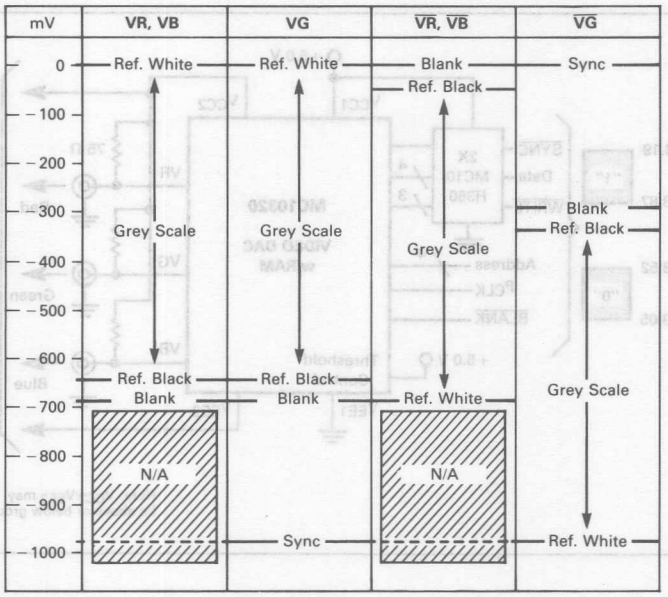
Output Configurations

The output waveforms may be above or below ground, depending on the choice of supply voltages for V_{CC2} and V_{EE2}, but the output voltages are always referenced to V_{CC2}. In Figure 12, the outputs are referenced to +5.0 V, and produce a 1.0 volt p-p waveform when used with a doubly terminated 75 Ω load, and an R_{SET} of 1.0 kΩ. The +5.0 volt supply is the "ac ground" in this case. If the outputs must be referenced to system ground rather than the +5.0 volt supply, the circuit of Figure 13 will provide the required level shifting. Figure 14 provides ground referenced outputs with a range of 0 to −1.0 volt. In Figure 15, the outputs are pulled up to a voltage different from V_{CC2}, providing an offset (+1.0 volt offset in the figure). In Figure 15 the complementary outputs should be connected to the +1.0 volt pullup voltage. The voltage at VR, VG, and VB (and the complementary outputs) must always lie within the range of ±2.0 volts with respect to V_{CC2}.

Figure 6 illustrates the output voltage range, with respect to V_{CC2} or a pullup voltage, of the six outputs (R_L = 37.5 Ω, R_{SET} = 1.0 kΩ):

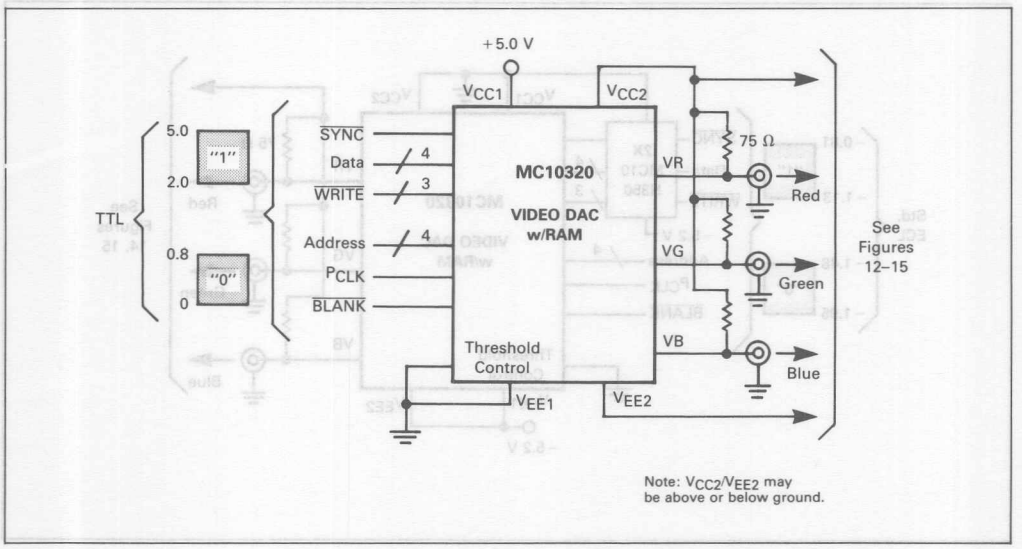
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FIGURE 6 — OUTPUT LEVELS



Note: R_{SET} = 1.0 k, R_L = 37.5 Ω, above values are typical.

FIGURE 7 — TTL INPUTS



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FIGURE 8 — ABOVE GROUND ECL INPUTS

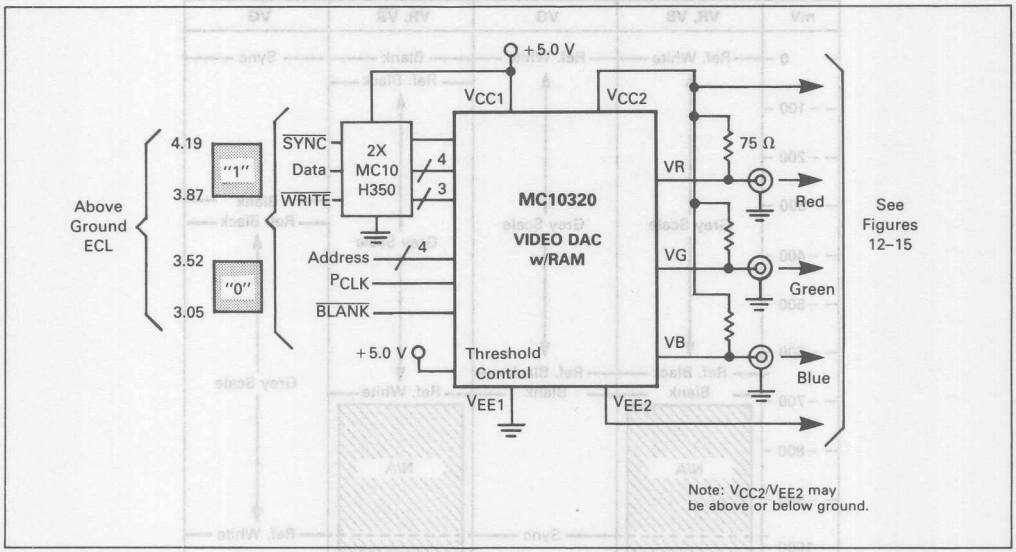
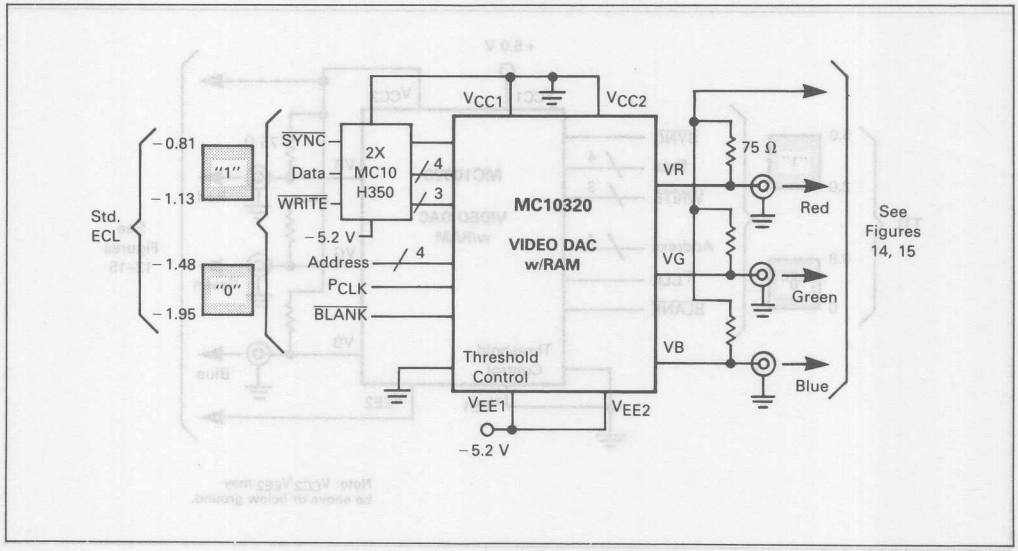


FIGURE 9 — STANDARD ECL INPUTS



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FIGURE 10 — LOW SPEED INPUTS @ TTL,
HIGH SPEED INPUTS @ ABOVE GROUND ECL

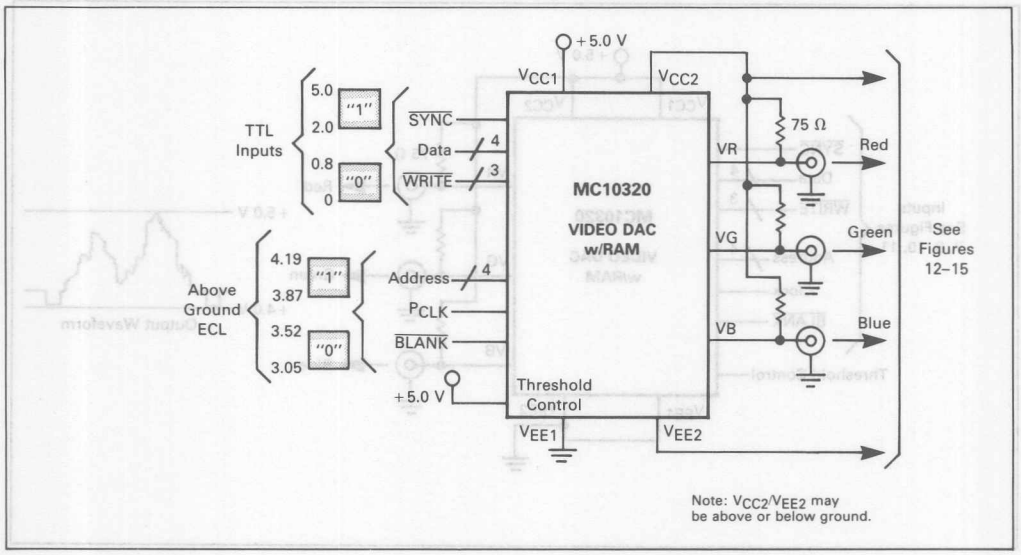
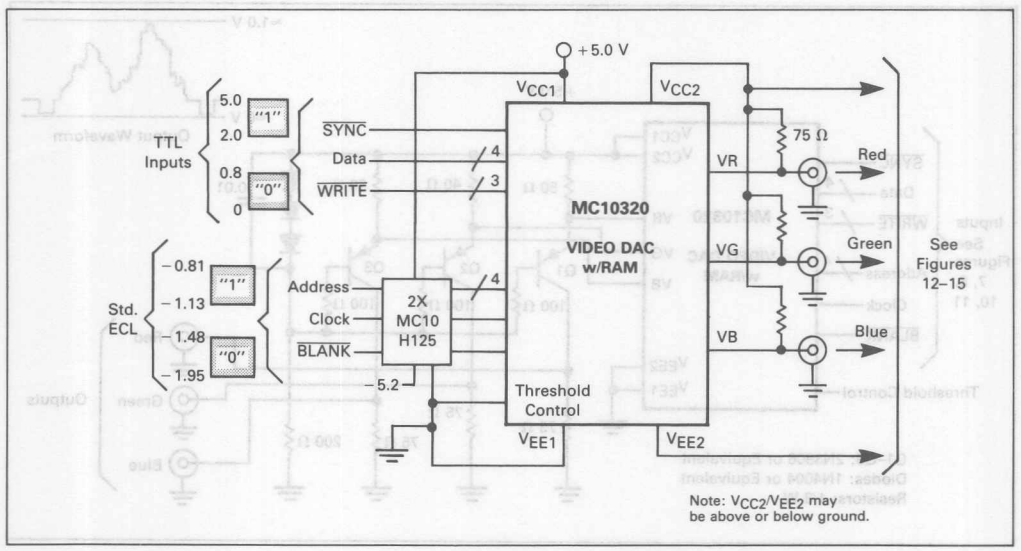


FIGURE 11 — LOW SPEED INPUTS @ TTL,
HIGH SPEED INPUTS @ STANDARD ECL



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FIGURE 12 — SINGLE +5.0 VOLT SUPPLY, OUTPUTS ABOVE GROUND

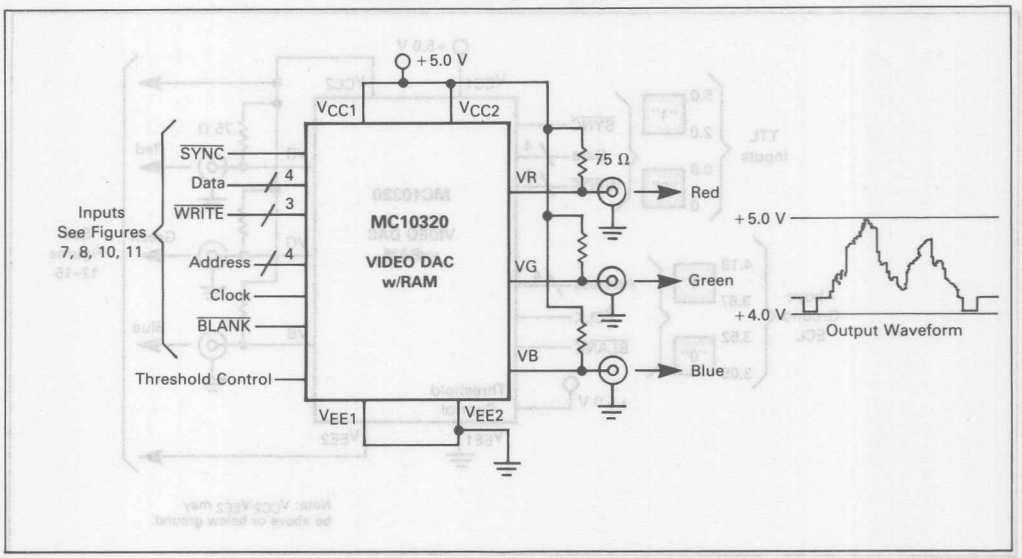
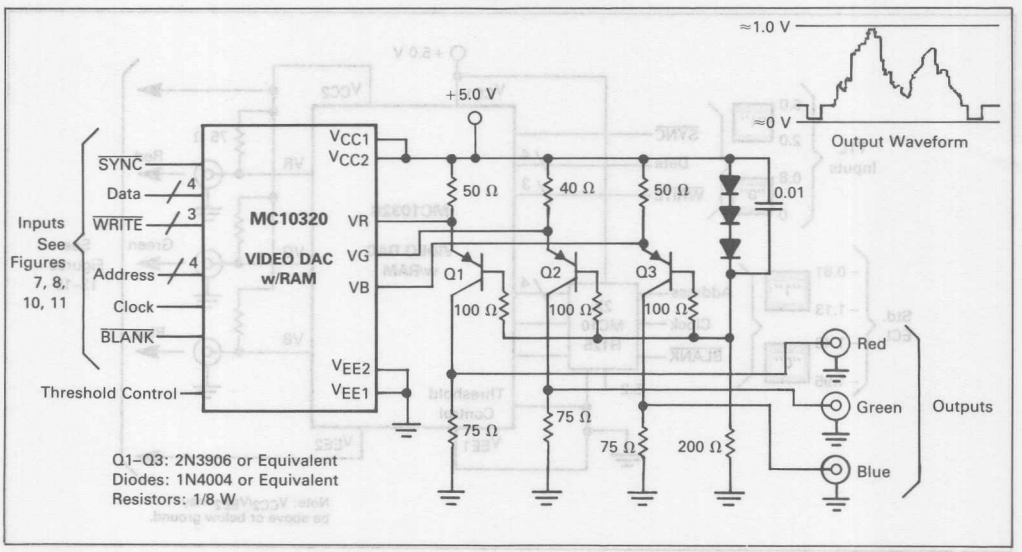


FIGURE 13 — SINGLE +5.0 VOLT SUPPLY, OUTPUTS REFERENCED TO GROUND



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FIGURE 14 — SINGLE OR DUAL SUPPLY, OUTPUTS BELOW GROUND

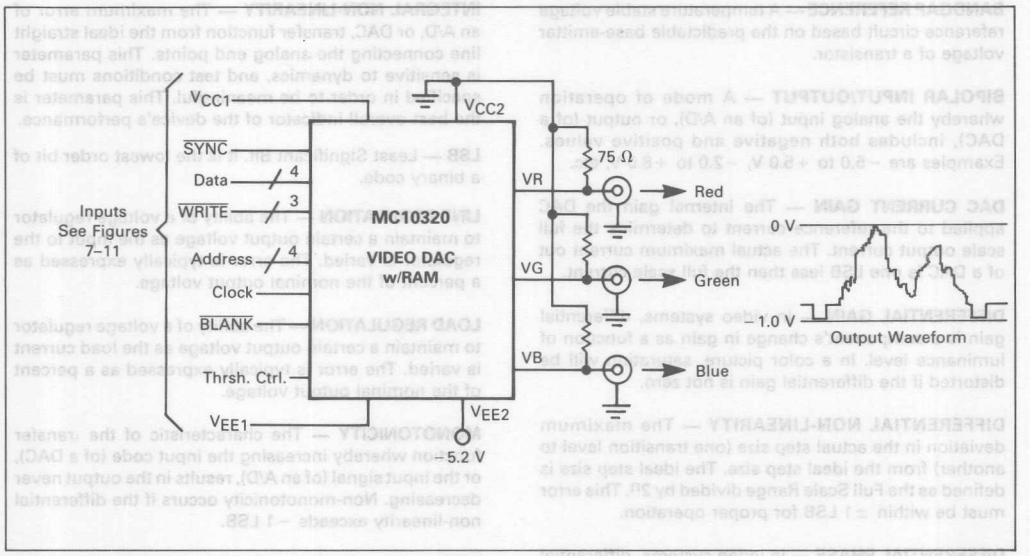
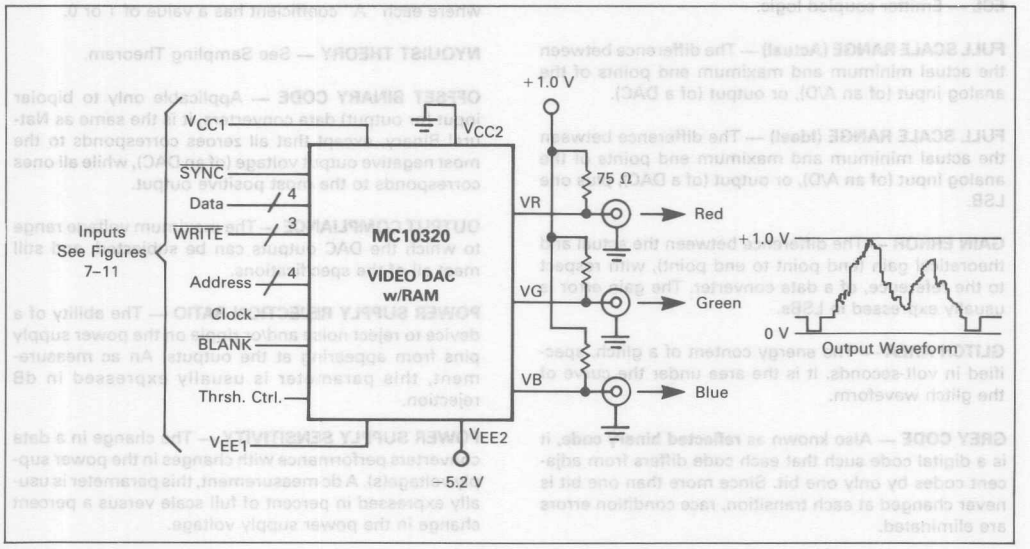


FIGURE 15 — SINGLE OR DUAL SUPPLY, OUTPUTS ABOVE GROUND, REFERENCED TO GROUND



9

GLOSSARY

BANDGAP REFERENCE — A temperature stable voltage reference circuit based on the predictable base-emitter voltage of a transistor.

BIPOLAR INPUT/OUTPUT — A mode of operation whereby the analog input (of an A/D), or output (of a DAC), includes both negative and positive values. Examples are −5.0 to +5.0 V, −2.0 to +8.0 V, etc.

DAC CURRENT GAIN — The internal gain the DAC applied to the reference current to determine the full scale output current. The actual maximum current out of a DAC is one LSB less than the full scale current.

DIFFERENTIAL GAIN — In video systems, differential gain is a component's change in gain as a function of luminance level. In a color picture, saturation will be distorted if the differential gain is not zero.

DIFFERENTIAL NON-LINEARITY — The maximum deviation in the actual step size (one transition level to another) from the ideal step size. The ideal step size is defined as the Full Scale Range divided by 2^n. This error must be within ±1 LSB for proper operation.

DIFFERENTIAL PHASE — In video systems, differential phase is the change in the phase modulation of the chrominance signal as a function of the luminance level. The hue in a color picture will be distorted if the differential phase is not zero.

ECL — Emitter coupled logic.

FULL SCALE RANGE (Actual) — The difference between the actual minimum and maximum end points of the analog input (of an A/D), or output (of a DAC).

FULL SCALE RANGE (Ideal) — The difference between the actual minimum and maximum end points of the analog input (of an A/D), or output (of a DAC), plus one LSB.

GAIN ERROR — The difference between the actual and theoretical gain (end point to end point), with respect to the reference, of a data converter. The gain error is usually expressed in LSBs.

GLITCH AREA — The energy content of a glitch, specified in volt-seconds. It is the area under the curve of the glitch waveform.

GREY CODE — Also known as **reflected binary code**, it is a digital code such that each code differs from adjacent codes by only one bit. Since more than one bit is never changed at each transition, race condition errors are eliminated.

INTEGRAL NON-LINEARITY — The maximum error of an A/D, or DAC, transfer function from the ideal straight line connecting the analog end points. This parameter is sensitive to dynamics, and test conditions must be specified in order to be meaningful. This parameter is the best overall indicator of the device's performance.

LSB — Least Significant Bit. It is the lowest order bit of a binary code.

LINE REGULATION — The ability of a voltage regulator to maintain a certain output voltage as the input to the regulator is varied. The error is typically expressed as a percent of the nominal output voltage.

LOAD REGULATION — The ability of a voltage regulator to maintain a certain output voltage as the load current is varied. The error is typically expressed as a percent of the nominal output voltage.

MONOTONICITY — The characteristic of the transfer function whereby increasing the input code (of a DAC), or the input signal (of an A/D), results in the output never decreasing. Non-monotonicity occurs if the differential non-linearity exceeds −1 LSB.

MSB — Most Significant Bit. It is the highest order bit of a binary code.

NATURAL BINARY CODE — A binary code defined by:

$$N = A_n 2^n + \ldots + A_3 2^3 + A_2 2^2 + A_1 2^1 + A_0 2^0$$

where each "A" coefficient has a value of 1 or 0.

NYQUIST THEORY — See Sampling Theorem.

OFFSET BINARY CODE — Applicable only to bipolar input (or output) data converters, it is the same as Natural Binary, except that all zeroes corresponds to the most negative output voltage (of an DAC), while all ones corresponds to the most positive output.

OUTPUT COMPLIANCE — The maximum voltage range to which the DAC outputs can be subjected, and still meet all of the specifications.

POWER SUPPLY REJECTION RATIO — The ability of a device to reject noise and/or ripple on the power supply pins from appearing at the outputs. An ac measurement, this parameter is usually expressed in dB rejection.

POWER SUPPLY SENSITIVITY — The change in a data converters performance with changes in the power supply voltage(s). A dc measurement, this parameter is usually expressed in percent of full scale versus a percent change in the power supply voltage.

PROPAGATION DELAY — For a video DAC, the time from when the clock input crosses its threshold to when the DAC output(s) reach the 50% point of the transition.

QUANTITIZATION ERROR — Also known as digitization error or uncertainty. It is the inherent error involved in digitizing an analog signal due to the finite number of steps at the digital output versus the infinite number of values at the analog input. This error is a minimum of ±1/2 LSB.

RESOLUTION — The smallest change which can be discerned by an A/D converter, or produced by a DAC. It is usually expressed as the number of bits, n, where the converter has 2^n possible states.

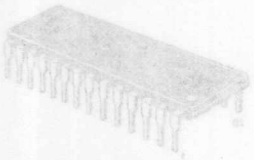
SAMPLING THEOREM — Also known as the Nyquist Theorem. It states that the sampling frequency of an A/D must be no less than 2x the highest frequency (of interest) of the analog signal to be digitized in order to preserve the information of that analog signal.

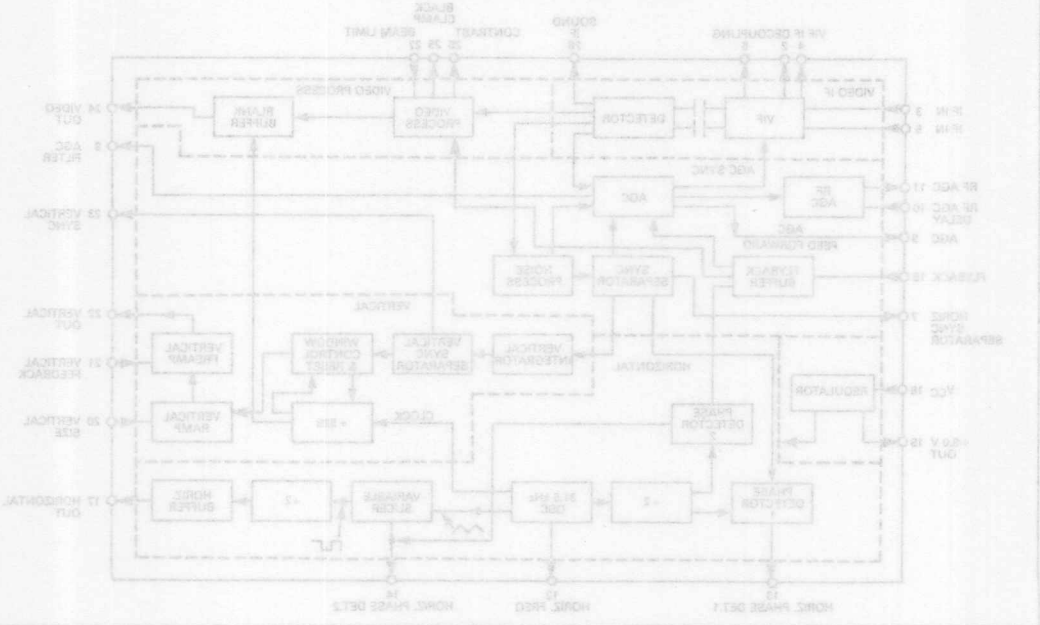
SETTLING TIME — For a video DAC, the time required for the output to change (and settle in) from an initial ±1/2 LSB error band to the final ±1/2 LSB error band.

TTL — Transistor-transistor logic.

TWO'S COMPLEMENT CODE — A binary code applicable to bipolar operation, in which the positive and negative codes of the same analog magnitude sum to all zeroes, plus a carry. It is the same as Offset Binary Code, with the MSB inverted.

UNIPOLAR INPUT — A mode of operation whereby the analog input range (of an A/D), or output range (of a DAC), includes values of a single polarity. Examples are 0 to +10 V, 0 to −5.0 V, +2.0 to +8.0 V, etc.





MOTOROLA

MC13001XP
MC13002XP

Advance Information

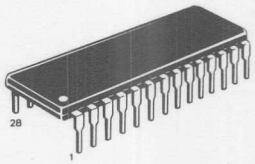
MONOMAX BLACK AND WHITE TV SUBSYSTEM

The MONOMAX is a single-chip IC that will perform the electronic functions of a monochrome TV receiver, with the exception of the tuner, sound channel, and power output stages. The MC13001XP and MC13002XP will function as drop-in replacements for MC13001P and MC13002P, but some external IF components can be removed for maximum benefit. IF AGC range has been increased, video output impedance lowered, and horizontal driver output current capability increased.

- Full Performance Monochrome Receiver with Noise and Video Processing — Black Level Clamp, DC Contrast, Beam Limiter
- Video IF Detection on Chip — No Coils, No Pins, except Inputs
- Noise Filtering on Chip — Minimum Pins and Externals
- Oscillator Components on Chip — No Precision Capacitors Required
- MC13001XP for 525 Line NTSC and MC13002XP for 625 Line CCIR
- Low Dissipation in All Circuit Sections
- High-Performance Vertical Countdown
- 2-Loop Horizontal System with Low Power Start-Up Mode
- Noise Protected Sync and Gated AGC System
- Designed to work with TDA1190P or TDA3190P Sound IF and Audio Output Devices
- Reverse RF AGC Types are Available: MC13008XP, MC13009XP

MONOMAX BLACK AND WHITE TV SUBSYSTEM

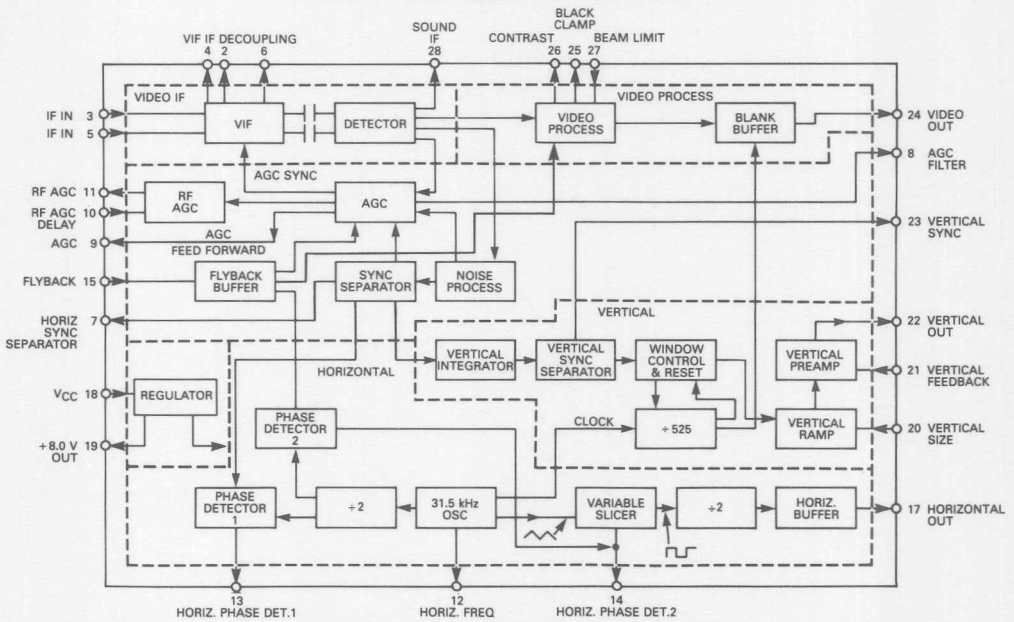
SILICON MONOLITHIC INTEGRATED CIRCUITS



P SUFFIX
PLASTIC PACKAGE
CASE 710-02

9

FIGURE 1 — BASIC ELEMENTS OF THE SYSTEM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage — Pin 18	V_{CC}	+16	Vdc
Power Dissipation	P_D	1.0	Watts
Horizontal Driver Current — Pin 17	I_{HOR}	−20	mA
RF AGC Current — Pin 11	I_{RFAGC}	20	mA
Video Detector Current — Pin 24	I_{VID}	5.0	mA
Vertical Driver Current — Pin 22	I_{VERT}	5.0	mA
Auxiliary Regulator Current — Pin 19	I_{REG}	35	mA
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	60	°C/W
Maximum Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Operating Temperature Range	T_A	0° to +70	°C

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Horizontal Output Drive Current	I_{HOR}	≤10	mA
RF AGC Current	I_{RFAGC}	≤10	mA
Regulator Current	I_{REG}	≤20	mA

ELECTRICAL CHARACTERISTICS (V_{CC} = 11.3 V, T_A = 25°C)

Characteristics		Symbol	Min	Typ	Max	Unit
Power Supply Current	Pins 18 & 19	I_{CC}	44	—	76	mA
Regulator Voltage	Pin 19	V_{REG}	7.2	8.2	8.8	Vdc
HORIZONTAL SPECIFICATIONS						
Oscillator Frequency (Nominal)	Pin 12	$f_{HOR(NOM)}$	13	—	19	kHz
Oscillator Sensitivity			—	230	—	Hz/μA
Start-Up Frequency (I_{18} = 4.0 mA)		f_{HOR}	−10	—	+10	%
Oscillator Temperature Stability (0 ≤ TA ≤ 75°C)		f_{HOR}	—	50	—	Hz
Phase Detector 1 (Charge/Discharge Current) (Non Standard Frame) (Standard Frame)		$I_{\phi 1}$		±900 ±400		μA
Phase Detector 1 (Output Voltage Limits)		$V_{\phi 1}$	—	7.5 (Max) 2.5 (Min)	—	Vdc
Phase Detector 1 (Leakage Current)			—	—	2.0	μA
Phase Detector 2 (Charge/Discharge Current)		$I_{\phi 2}$	—	+1.0 −0.6		mA
Phase Detector 2 (Output Voltage Limits)		$V_{\phi 2}$		7.7 (Max) 1.5 (Min)		Vdc
Phase Detector 2 (Leakage Current)			—	—	3.0	μA
Horizontal Delay Range (Sync to Flyback)				18 (Max) 5.0 (Min)		μs
Horizontal Output Saturation Voltage (I_{17} = 15 mA)		$V_{17(SAT)}$	—	—	0.3	Vdc
Phase Detector 1 (Gain Constant) (Out-of-Lock) (In-Lock)			—	5.0 10	—	μA/μs
Horizontal Pull-In Range			±500	±750		Hz

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Characteristics		Symbol	Min	Typ	Max	Unit
Output Current	Pin 22	I_{22}	−0.6	—	—	mA
Feedback Leakage Current	Pin 21	I_{21}	—	—	6.0	μA
Ramp Retrace Current	Pin 20	I_{20}	500	—	900	μA
Ramp Leakage Current	Pin 20		—	—	0.3	μA
Feedback Maximum Voltage		V_{21}	—	5.1	—	Vdc
IF SPECIFICATIONS						
Regulator Voltage		V_4	—	7.5	—	Vdc
Input Bias Voltage		$V_{2,6}$	—	4.2	—	Vdc
Input Resistance Input Capacitance (V_{AGC} Pin 8 = 4.0 V)		R_{IN} C_{IN}		6.0 2.0		kΩ pF
Sensitivity (V_8 = 0 V, 400 Hz 30% MOD, V_{28} = 0.8 V_{pp})			—	80	—	μV_{RMS}
Bandwidth			—	75	—	MHz
VIDEO SPECIFICATIONS						
Zero Carrier Voltage (See Figure 5)	Pin 28		—	7.0	—	Vdc
Output Voltage (See Figure 6) White to Back Porch	Pin 24		—	1.4	—	V
Differential Gain Differential Phase (IRE Test Method)			—	6 4	—	% Degrees
Contrast Bias Current	Pin 26	I_{26}	—	10	—	μA
Contrast Control Range			—	14:1	—	
Beam Limiting Voltage	Pin 27	V_{27}	—	1.0	—	Vdc
AGC & SYNC						
R.F. (Tuner) AGC Output Current (V_{11} = 5.5 V)		I_{11}	5.0	—	—	mA
AGC Delay Bias Current		I_{10}	—	−10	—	μA
AGC Feedforward Current		I_9	—	1.0	—	mA
AGC Threshold (Sync Tip at Pin 28)		V_{28}	4.7	—	5.1	Vdc
Sync Separator Operating Point		V_7	—	4.2	—	Vdc
Sync Separator Charge Current		I_7	—	5.0	—	mA

FIGURE 2 — MONOMAX AGC CHARACTERISTICS

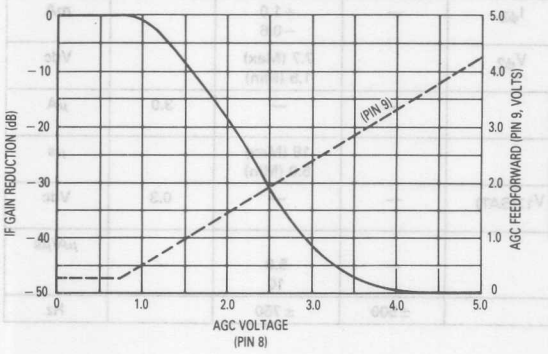


FIGURE 3 — VIDEO OUTPUT RESPONSE

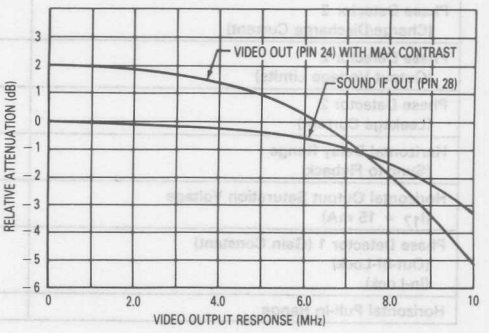
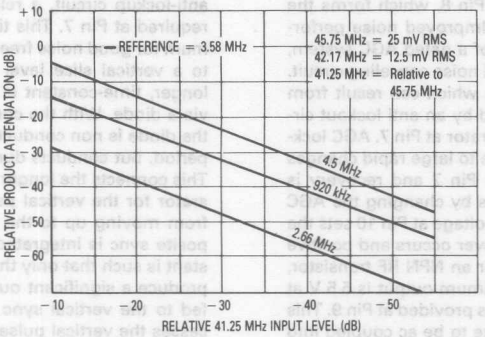


FIGURE 4 — DETECTOR PRODUCTS



GENERAL DESCRIPTION

The Video IF Amplifier is a four-stage design with 80 μV sensitivity. It uses a 6.2 V supply decoupled at Pin 4. The first two stages are gain controlled, and to ensure optimum noise performance, the first stage control is delayed until the second stage has been gain reduced by 15 dB. To bias the amplifier, balanced dc feedback is used which is decoupled at Pins 2 and 6 and then fed to the input Pins 3 and 5 by internal 3.9 k resistors. The nominal bias voltage at these input pins is approximately 4.2 Vdc. The input, because of the high IF gain, should be driven from a balanced differential source. For the same reason, care must be taken with the IF decoupling.

The IF output is rectified in a full wave envelope detector and detector nonlinearity is compensated by using a similar nonlinear element in a feedback output buffer amplifier. The detected 1.9 V_{p-p} video at Pin 28 contains the sound intercarrier signal, and Pin 28 is normally used as the sound takeoff point. The video frequency response, detector to Pin 28, is shown in Figure 3 and the detector intermodulation performance can be seen by reference to Figure 4. Typical Pin 28 video waveforms and voltage levels are shown in Figure 5.

The video processing section of Monomax contains a contrast control, black level clamp, a beam current limiter and composite blanking. The video signal first passes through the contrast control. This has a range of 14:1 for a 0 V to 5.0 V change of voltage on Pin 26, which corresponds to a change of video amplitude at Pin 24 of 1.4 V to 0.1 V (black to white level). The beam current limiter operates on the contrast control, reducing the video signal when the beam current exceeds the limit set by external components. As the beam current increases, the voltage at Pin 27 moves negatively from its normal value of 1.5 V, and at 1.0 V operates the contrast control, thus initiating beam limiting action. After the contrast control, the video is passed through a buffer amplifier and dc restored by the black level clamp circuit before being fed to Pin 24 where it is blanked. The black level clamp, which is gated "on" during the second half of the flyback, maintains the video black level at 2.4 V ± 0.1 V under all conditions, including changes in contrast, temperature and power supply. The loop integrating capacitor is at Pin 25 and is normally at a voltage of 3.3 V. The frequency response of the video at Pin 24 is shown in Figure 3 and it is blanked to within 0.5 V of ground.

The AGC loop is a gated system, and for all normal variations of the IF input signal maintains the sync tip of a noise filtered video signal at a reference voltage

FIGURE 5 — PIN 28 SOUND OUTPUT

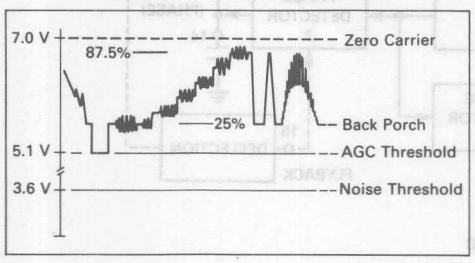
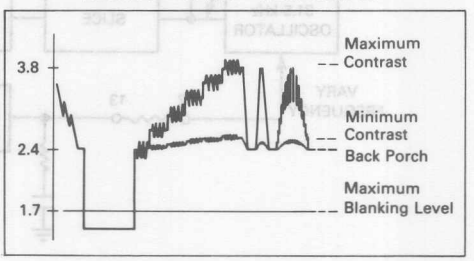


FIGURE 6 — PIN 24 — VIDEO OUTPUT



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(5.1 V Pin 28). The strobe for the AGC error amplifier is formed by gating together the flyback pulse with the separated sync pulse. Integration of the error signal is performed by the capacitor at Pin 8, which forms the dominant AGC time constant. Improved noise performance is obtained by the use of a gated AGC system, noise protected by a dc coupled noise canceling circuit. The false AGC lock conditions, which can result from this combination, are prevented by an anti lockout circuit connected to the sync separator at Pin 7. AGC lockout conditions, which occur due to large rapid changes of signal level are detected at Pin 7 and recovery is ensured under these conditions by changing the AGC into a mean level system. The voltage at Pin 10 sets the point at which tuner AGC takeover occurs and positive going tuner control, suitable for an NPN RF transistor, is available at Pin 11. The maximum output is 5.5 V at 5.0 mA. A feed-forward output is provided at Pin 9. This enables the AGC control voltage to be ac coupled into the tuner takeover control at Pin 10. The coupling allows additional IF gain reduction during signal transient conditions, thus compensating for variations of AGC loop gain at the tuner AGC takeover point. In this way the AGC system stability and response are not degraded.

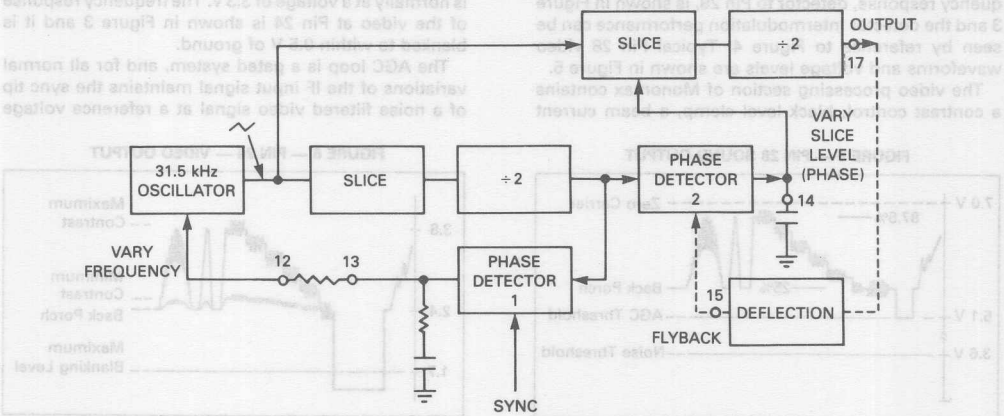
The previously mentioned noise protection is effected by detecting negative-going noise spikes at the video detector output. A dc coupled detector is used which turns on when a noise spike exceeds the video sync tip by 1.4 V. This pulse is then stretched and used to cancel the noise present on the delayed video at the input to the sync separator. Cancellation is performed by blanking the video to ground. Complete cancellation of the noise spike results from the stretching of the blanking pulse and the delay of the noise spike at the input to the sync separator. Protection of both the horizontal PLL and the AGC stems from the fact that both circuits use the noise cancelled sync for gating.

The composite sync is stripped from a delayed and filtered video in a peak detecting type of sync separator. The components connected to Pin 7 determine the slice and tilt levels of the sync separator. For ideal horizontal sync separation and to ensure correct operation of AGC anti-lockup circuit, a relatively short time constant is required at Pin 7. This time constant is less than optimum for good noise free vertical separation, giving rise to a vertical slice level near sync tip. An additional, longer, time-constant is therefore coupled to the first via a diode. With the correct choice of time constants, the diode is non conducting during the horizontal sync period, but conducts during the longer vertical period. This connects the longer time constant to the sync separator for the vertical period and stops the slice level from moving up to the sync tip. The separated composite sync is integrated internally, and the time constant is such that only the longer period vertical pulses produce a significant output pulse. The output is then fed to the vertical sync separator, which further processes the vertical pulse and provides increased noise protection. The selection of the external components connected to the vertical separator at Pin 23 permits a wide range of performance options. A simple resistor divider from the 8.2 V regulated supply gives adequate performance for most conditions. The addition of an RC network will make the slice level adapt to varying sync amplitude and give improved weak signal performance. A resistor to the AGC voltage on Pin 9 enables the sync slice level to be changed as a function of signal level. This further improves the low signal level separation while at the same time giving increased impulse noise protection on strong signals.

HORIZONTAL OSCILLATOR

The horizontal PLL (see Figure 7) is a 2-loop system using a 31.5 kHz oscillator which after a divider stage is locked to the sync pulse using phase detector 1. The control signal derived from this phase detector on Pin 13 is fed via a high-value resistor to the frequency-control point on Pin 12. The same divided oscillator

FIGURE 7 — HORIZONTAL OSCILLATOR SYSTEMS



frequency is also fed to phase detector 2, where the flyback pulse is compared with it and the resulting error used to change a variable slice level on the oscillator ramp waveform. This therefore changes the timing of the output square wave from the slicer and hence the timing of the buffered horizontal output on Pin 17 (see Figure 8). The error on phase detector 2 is reduced until the phasing of the flyback pulse is correct with respect to the divided oscillator waveform, and hence with respect to the sync pulse.

To improve the pull-in and noise characteristics of the first PLL, the phase detector current is increased when the vertical lock indicator signals an unlocked condition and is decreased when locked. This increases the loop bandwidth and pull-in range when out of lock and decreases the loop bandwidth when in lock, thus improving the noise performance. In addition, the phase detector current during the vertical period is reduced in order to minimize the disturbance to the horizontal caused by the longer period vertical phase detector pulses.

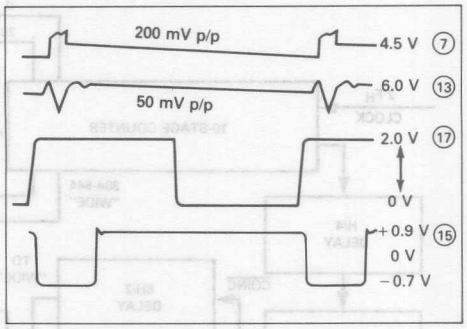
The oscillator itself is a novel design using an on-chip 50 pF silicon nitride capacitor which has a temperature drift of only 70 ppm/°C and negligible long term drift. This, in conjunction with an external resistor, gives a drift of horizontal frequency of less than 1Hz/°C — i.e., less than 100 Hz over the full operating temperature range of the chip. The pull-in range of the PLL is about ± 750 Hz, so normally this would eliminate the need for any customer adjustment of the frequency.

The second significant feature of this design is the use of a virtual ground at the frequency control point which floats at a potential derived from a divider across the power supply and this is the same divider which determines the end-points of the oscillator ramp. The frequency adjustment which is necessary to take up tolerances in the on-chip capacitor is fed in as a current to this virtual ground and when this adjustment current is derived from an external potentiometer across the same supply there is no frequency variation with supply voltage. Moreover, using the voltage from a potentiometer for the adjustment instead of the simple variable resistor normally used in RC oscillators makes the frequency independent of the value of the potentiometer and hence its temperature coefficient. The frequency control current from the first phase detector is fed into this same virtual ground and as the sensitivity of the control is about 230 Hz/μA a high value resistor can be used (680 kΩ) and this can be directly connected to the phase detector filter without significant loading.

This oscillator operates with almost constant frequency to below 4.0 volts and as the total PLL system consumes less than 4.0 mA at this voltage, this gives an ideal start-up characteristic for receivers using deflection-derived power supplies.

The flyback gating input is on Pin 15 which is internally clamped to 0.7 V in both directions and requires a negative input current of 0.6 mA to operate the gate circuit. This input can be a raw flyback pulse simply fed via a suitable resistor.

FIGURE 8 — HORIZONTAL WAVEFORMS



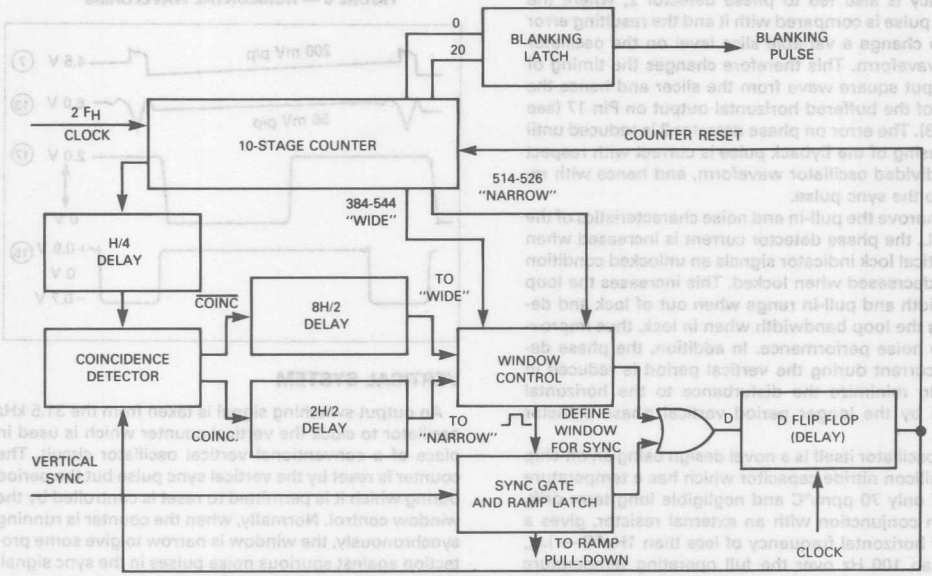
VERTICAL SYSTEM

An output switching signal is taken from the 31.5 kHz oscillator to clock the vertical counter which is used in place of a conventional vertical oscillator circuit. The counter is reset by the vertical sync pulse but the period during which it is permitted to reset is controlled by the window control. Normally, when the counter is running synchronously, the window is narrow to give some protection against spurious noise pulses in the sync signal. If the counter output is not coincident with sync however, after a short period the window opens to give reset over a much wider count range, leading to a fast picture roll towards lock. At weak signal, i.e., less than 200 μV IF input, the vertical system is forced to narrow mode to give a steadier picture for commonly occurring types of noise. The vertical sync, gated by the counter, then resets a ramp generator on Pin 20 and the 1.5 volt p-p ramp is buffered to Pin 22 by the vertical preamplifier. A differential input to the preamp on Pin 21 compares the signal generated across the resistor in series with the deflection coils with the generated ramp and thus controls shape and amplitude of the coil current.

The basic block diagram of the countdown system is shown in Figure 9. The 31.5 kHz (2 F^H) clock from the horizontal oscillator drives a 10-stage counter circuit which is normally reset by the vertical sync pulse via the sync gate, OR gate and D flip-flop. This D input is also used to initiate discharge of the ramp capacitor and hence causes picture flyback.

The period during which sync can reset the counter and cause flyback is determined by the window control which defines a count range during which the gate is open. One of two ranges is selected according to the condition of the signal. The normal "narrow" range is 514 to 526 counts for a 525 line system and is selected after the coincidence detector indicates that the reset is coincident, twice in succession, with the 525 count from the counter. When the detector indicates non-coincidence 8 times in succession, then the window control switches to the "wide" mode (384 to 544 counts) to achieve rapid re-synchronization. For the 625 line version the counts are 614 to 626 for narrow mode and

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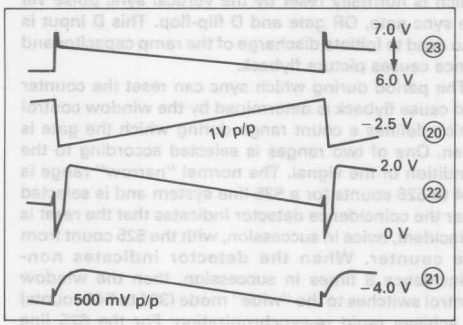


484 to 644 for wide mode. Note that the OR gate after the sync gate is used to terminate the count at the end of the respective window if a sync pulse has not appeared.

This method accepts non-standard signals almost in the same way as a conventional triggered RC oscillator and has a similar fast lock-in time. However, the use of a window control on the counter reset ensures that when locked with a normal standard broadcast signal the counter will reject most spurious noise pulses.

The blanking output is provided from a latch which is set by the counter reset pulse and terminated by count 20 from the counter chain.

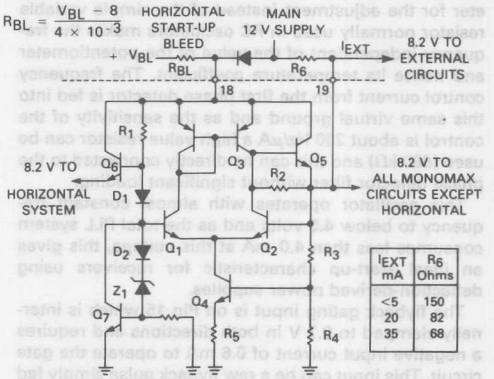
FIGURE 10 — VERTICAL WAVEFORMS



POWER SUPPLY

The power supply regulator, although of simple design, provides two independent power supplies — one for the horizontal PLL section and the other for the remainder of the chip. The supplies share the same reference voltage but the design of the main regulator is such that it can be switched on independently to give minimum loading on the "bleed" voltage source during start-up phase of a deflection-derived supply system.

FIGURE 11 — POWER SUPPLY CIRCUIT



I_{EXT} mA	R_6 Ohms
<5	150
20	82
35	68

FIGURE 12 — TEST CIRCUIT DIAGRAM

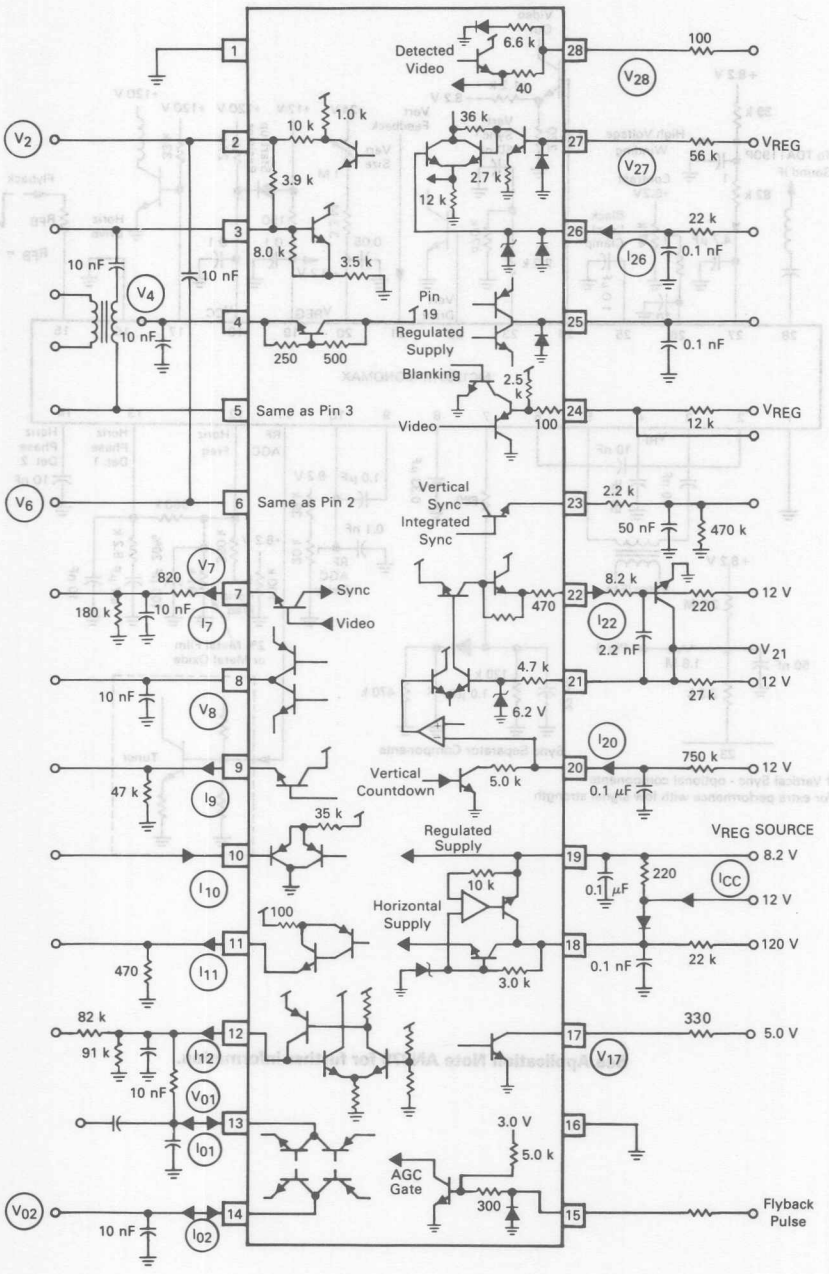
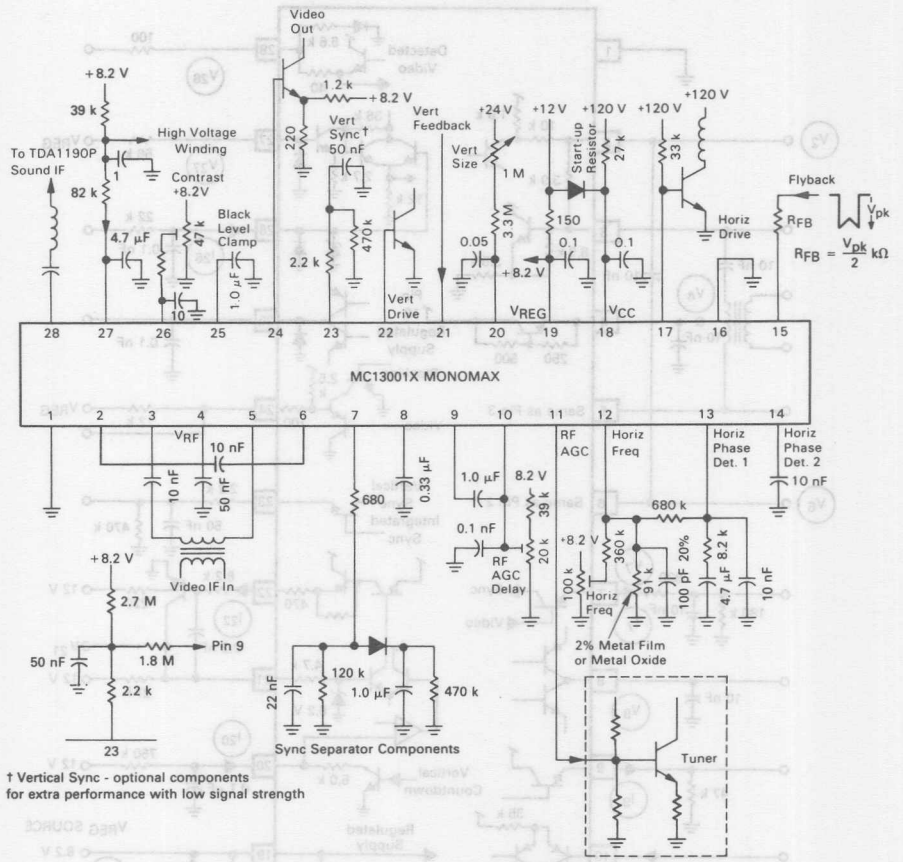


FIGURE 13 — TYPICAL APPLICATION



† Vertical Sync - optional components for extra performance with low signal strength

See Application Note AN879 for further information.

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MOTOROLA

MC13010P

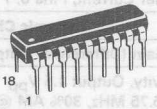
TV PARALLEL SOUND IF/AFT

SILICON MONOLITHIC INTEGRATED CIRCUIT

TV PARALLEL SOUND IF AND AFT

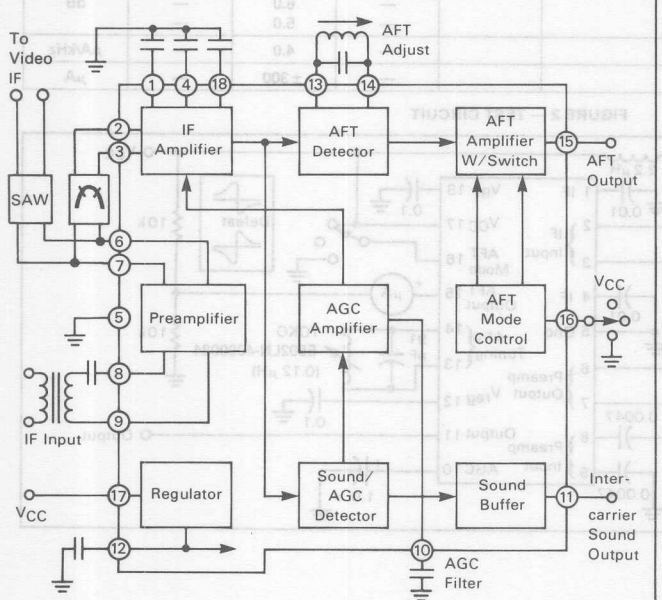
The PSIF is a single-chip IC that enhances the performance of a color TV, audio and video/chroma system. It eliminates band-pass compromises which normally tradeoff 920 kHz video beat with sound performance. The chip also includes a surface wave filter preamplifier and an AFT circuit.

- Low Noise Preamplifier for SAW Filter
- Wideband IF Amplification with Mean Level AGC
- Intercarrier Detector for Sound Carrier Output
- Reduces 920 kHz Beat
- AFT Discriminator with Output Polarity Selection
- Internal Voltage Regulator 8.2 V
- 30 mA Available from 8.2 V Internal Regulator

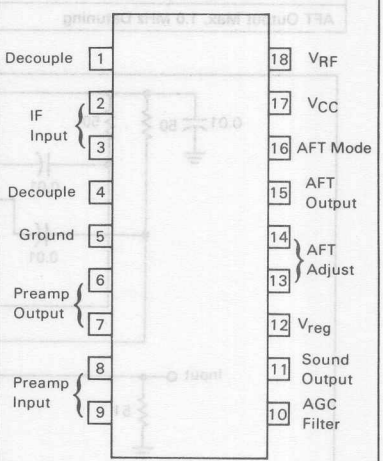


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FIGURE 1 — BLOCK DIAGRAM



PIN CONNECTIONS



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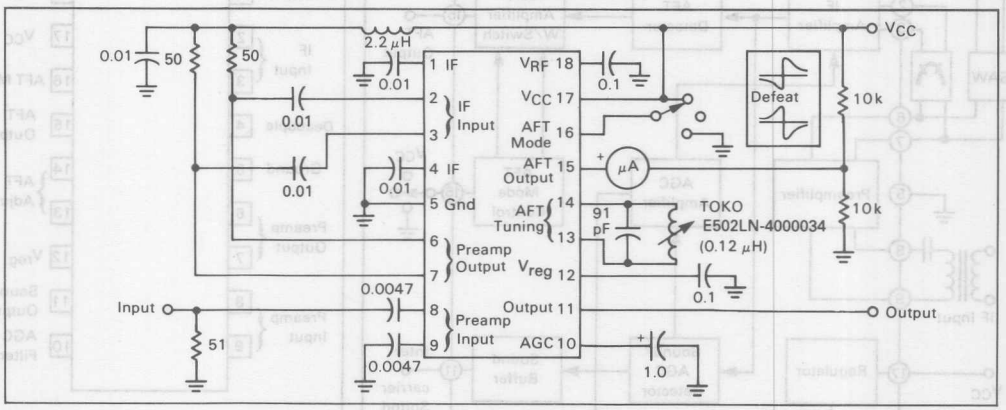
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CCC}	16	Vdc
Regulator Output Current	I_{reg}	30	mAdc
Thermal Resistance	$R_{\theta JA}$	70	°C/W
Power Dissipation (Package Limitation)	P_D	1.1	W
Maximum Junction Temperature	$T_{J(max)}$	150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Operating Temperature Range	T_A	0 to +70	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, T_A = 25°C, Test Circuit of Figure 2, unless otherwise noted)

Static Characteristics	Symbol	Min	Typ	Max	Unit
Supply Current	I_{CC}	30	—	60	mAdc
Regulator Voltage, Pin 12	V_{reg}	7.6	8.2	8.8	Vdc
RF Supply Voltage, Pin 18	V_{RF}	5.8	6.5	7.2	Vdc
Preamplifier Current, Pins 6, 7		4.0	6.6	7.5	mAdc
Dynamic Characteristics					
Preamp Gain (Differential Output, 50 Ω Loads)	Av	—	−3.0	—	dB
IF Sensitivity, Output 1.5 V_{pp} Input 45.75 MHz, 30% AM @ 1.0 kHz Differential Pins 2, 3		—	80	—	μV_{rms}
AGC Range, Input CW for Output Change of ±0.25 Vdc		—	48	—	dB
Intercarrier Sound Output (Beat), Input 45.75 MHz, 7.0 mV_{rms}; 41.25 MHz, 2.2 mV_{rms}		100	200	400	mV_{rms}
IF Bandwidth (3.0 dB)	f_{max}	—	80	—	MHz
Preamplifier Input Resistance Preamplifier Input Capacitance	R_{in} C_{in}	— —	1.5 11.5	— —	kΩ pF
IF Input Resistance IF Input Capacitance	R_{in} C_{in}	— —	2.2 4.0	— —	kΩ pF
Preamplifier Max Input Signal (Single Ended)	V_{in}	—	50	—	mV_{rms}
IF Max Input Signal (Differential)	V_{in}	—	50	—	mV_{rms}
Noise Figure IF, Max Gain Noise Figure Preamplifier		— —	6.0 5.0	— —	dB
AFT Center-Frequency Slope		—	4.0	—	μA/kHz
AFT Output Max, 1.0 MHz Detuning		—	±300	—	μA

FIGURE 2 — TEST CIRCUIT



to be part of a high performance color television system. Its primary function is to provide a complete separate IF amplifier for sound, leaving the normal IF to be concerned only with video. Secondary functions include an AFT detector and a SAW preamp.

In most present day color television receivers, sound and video are processed by the same IF amplifier and, in many cases, the same synchronous or pseudosynchronous detector. This imposes undesirable compromises in video and sound performance. Particularly in the U.S., the avoidance of a color/sound beat product (920 kHz) can only be achieved at the expense of sound quieting and sensitivity. Earlier solutions involved a single IF amplifier driving two detectors, with numerous interstage alignments required.

A method of solving these problems is to process the sound and video separately, directly from the tuner output. The MC13010 provides the second complete IF channel, with its own wideband detector and AGC. This permits both video IF and sound IF to be free of tuned elements, except at their inputs. (See Figure 3.)

4. The intercarrier sound output (Pin 11) is typically about 200 mV_{rms}, which easily overcomes a lossy intercarrier filter and meets the input needs of even the least sensitive FM sound IF ICs.

AFT

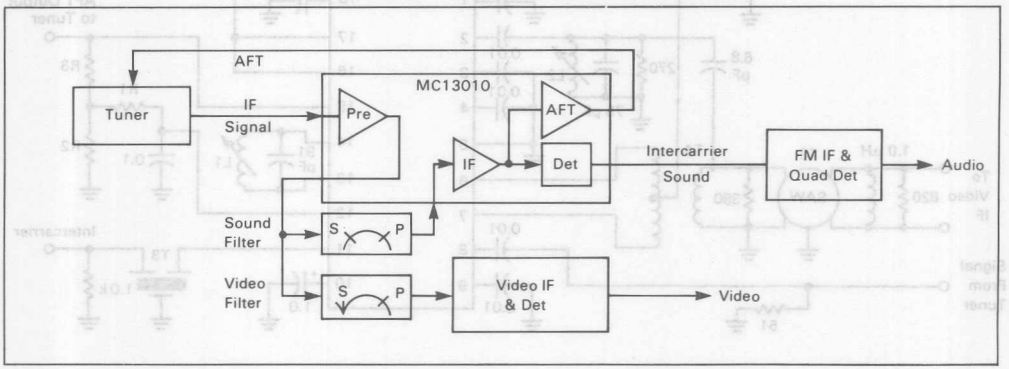
The AFT detector is a quadrature type operating at the picture IF frequency, with only one external L-C to be aligned. The polarity of the AFT output may be changed by taking the mode control (Pin 16) high or low. If the control pin is left open, the AFT is defeated.

ADDITIONAL APPLICATIONS

The MC13010 is an ideal part for stand-alone AFT. It contains the entire active system to provide a tuner with "self control". (See Figure 6.)

This device performs AM detection at the intercarrier sound output. Therefore, AM modulated digital data may be recovered. This function may be useful in cable systems where digital coding is employed.

FIGURE 3 — BLOCK DIAGRAM OF T.V. APPLICATION OF MC13010



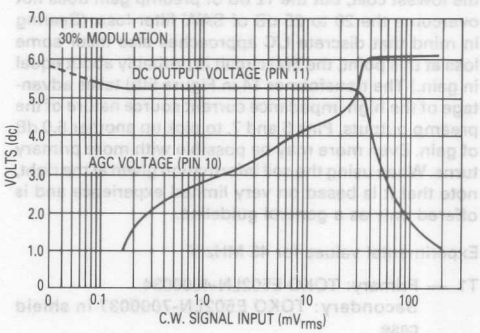
PREAMPLIFIER

The preamp is included to compensate for the high insertion loss of a Surface Acoustic Wave filter. This SAW filter may have two outputs with different responses, or it may serve only the video signal path. The preamp is optional if an LC filter is used. In any case, the selectivity ahead of the video IF must provide deep trapping of the sound carrier, while the sound bandpass is relatively broad and flat between the picture and sound carriers.

THE SOUND IF

The overall gain of 80 dB and gain control range of 48 dB equals the video IF's of earlier designs. This allows the full improvement of the system architecture to be realized. The AGC in the MC13010 is a peak-detecting type, driven internally from the sound detector, and re-

FIGURE 4 — GAIN AND AGC CHARACTERISTICS



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FIGURE 5(A) — TYPICAL TV APPLICATION

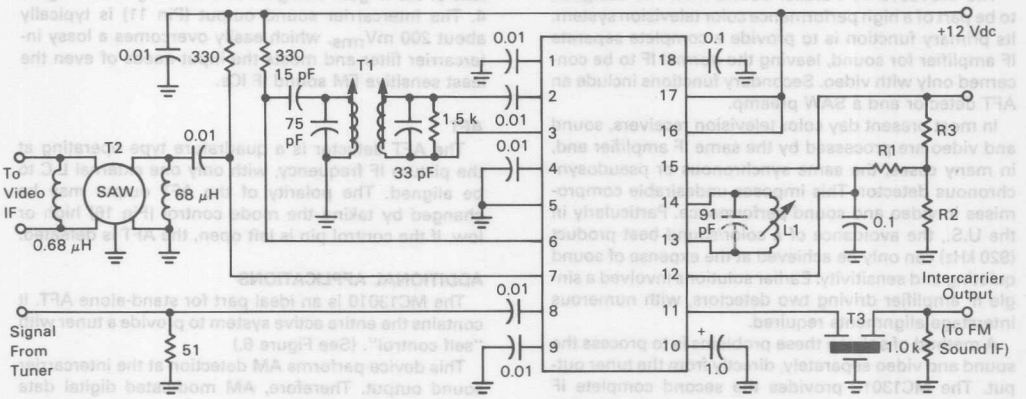
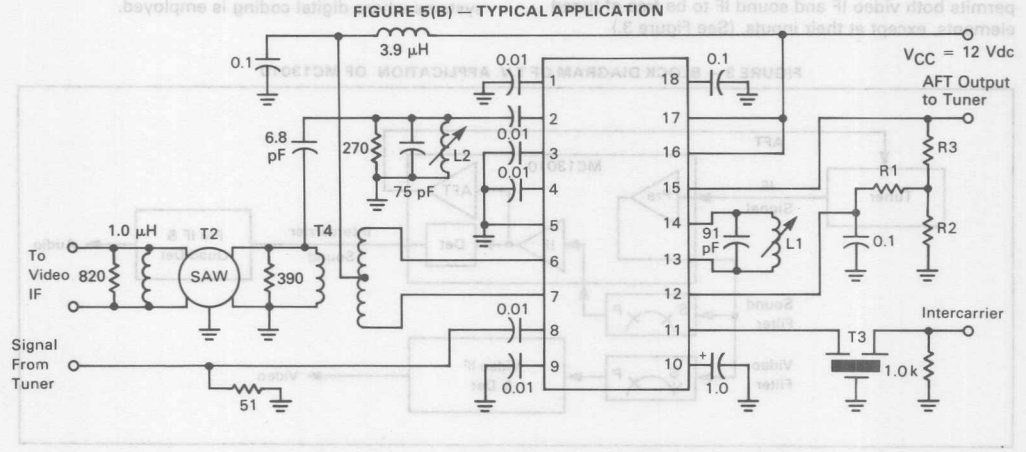


FIGURE 5(B) — TYPICAL APPLICATION



Shown above are two approaches to using the MC13010 in TV designs. The simpler circuit 5(a) offers the lowest cost, but the 12 dB of preamp gain does not overcome the 20 to 25 dB of SAW filter loss. (Bearing in mind that discrete L/C approaches also incur some loss at this point, the 5(a) circuit is probably about equal in gain.) The transformer T4 in Figure 5(b) takes advantage of the high impedance current source nature of the preamp outputs, Pins 6 and 7, to pick up another 6.0 dB of gain. Even more may be possible with more primary turns. When using the coil information given at the right, note that it is based on very limited experience and is offered only as a general guideline.

Experimental values for 45 MHz IF:

T1 — Primary: TOKO E502LN-4000034
Secondary: TOKO E502LN-7000037 in shield case

T2 — Video IF Surface Acoustic Wave (SAW) Filter: muRata, SAF 45MC02Z

T3 — Ceramic Intercarrier Output Filter: muRata SFE 4.5 MB

T4 — TOKO KANAS-K7060EK

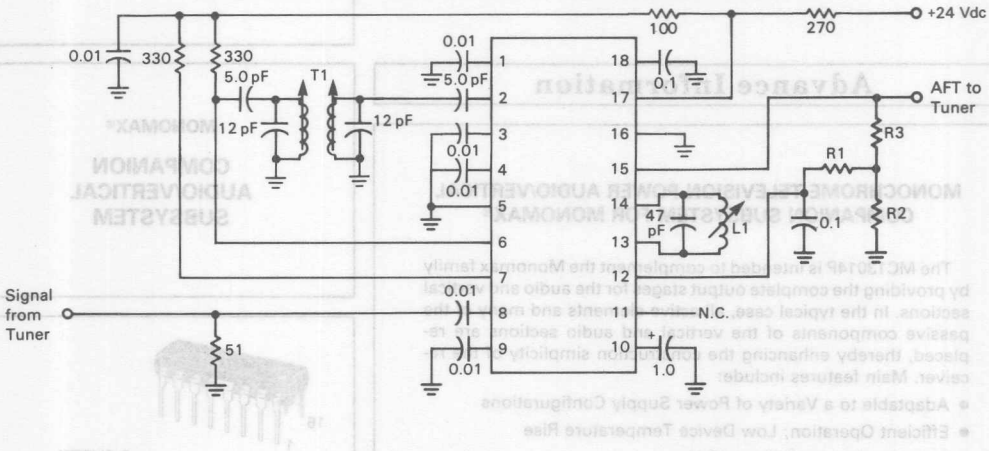
L1 — TOKO E502LN-4000034 J.W. Miller 48A147MPC with shield case, tuned to 45.75, L ≈ 0.12 μH.

L2 — Same part as L1, except tuned to 44 MHz and loaded with 270 Ω

R1 and R2 — Adjust for nominal tuning voltage

R3 — Chosen for tuning voltage swing required. Note that Pin 15 can source or sink 300 μA (typ) at the extremes of control range

FIGURE 6 — "STAND-ALONE" AUTOMATIC FINE TUNING (AFT) APPLICATION



Channel 3 Component Values

T1 — Made from two coils positioned side by side, without shields, on 0.38" centers. Coils are COILCRAFT part no. T7-142 (violet 7-1/2 turns), each with its own slug, Carbonal E, adjusted to 63 MHz (≈0.4 μH). This should give a slightly overcoupled response. A sheild to surround the coils may be required.

L1 — COILCRAFT UNI-7/150 (blue 6-1/2 turns) or UNI-10/144 (green 5-1/2 turns) shielded, adjusted to 61.25 MHz (≈ 0.14 μH)

R1 and R2 — Adjust for nominal tuning voltage

R3 — Chosen for tuning voltage swing required. Note that Pin 15 can source or sink 300 μA (typ) at the extremes of control range

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MC13014P

Advance Information

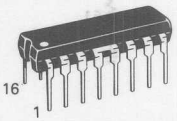
MONOMAX®

COMPANION AUDIO/VERTICAL SUBSYSTEM

MONOCHROME TELEVISION POWER AUDIO/VERTICAL COMPANION SUBSYSTEM FOR MONOMAX®

The MC13014P is intended to complement the Monomax family by providing the complete output stages for the audio and vertical sections. In the typical case, all active elements and many of the passive components of the vertical and audio sections are replaced, thereby enhancing the construction simplicity of the receiver. Main features include:

- Adaptable to a Variety of Power Supply Configurations
- Efficient Operation; Low Device Temperature Rise
- High Breakdown Voltage, 40 V
- Can Deliver 600 mA p-p Yoke Current
- Up to 750 mW of Audio Output
- Operates over a Wide Supply Voltage Range, 6–40 Vdc



P SUFFIX
PLASTIC PACKAGE
CASE 648C-02

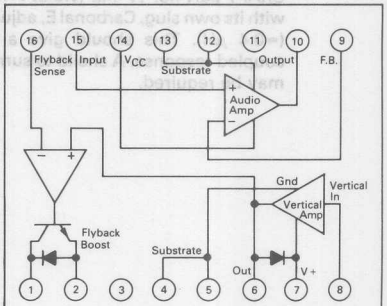
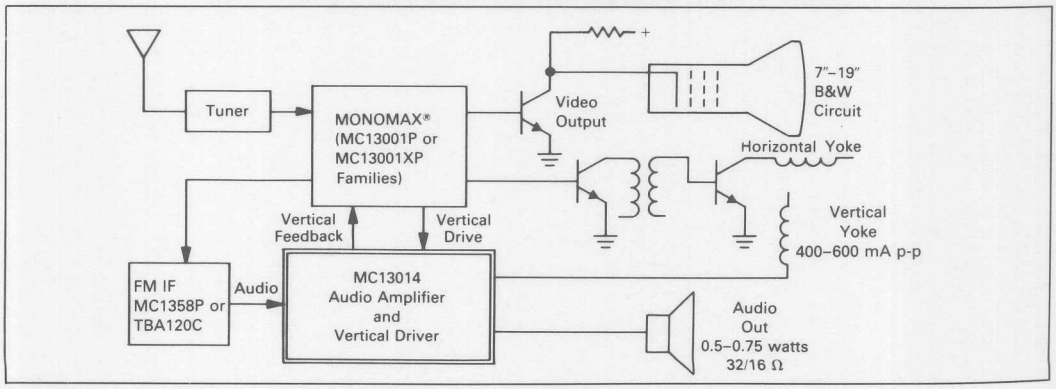


FIGURE 1 — BLOCK DIAGRAM, TYPICAL APPLICATION, MONOCHROME TV RECEIVER



This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (Pins 1, 7, 16)	V_{CC}, V_{boost}	+40	V
Power Supply Voltage, Audio Section (Pin 14)	V_{CC}'	+35	V
Audio Input	V_{IS}	1.0	V p-p
Thermal Resistance, Junction to Air	$R_{\theta JA}$	80	°C/W
Junction Temperature	T_J	150	°C
Operating Temperature Range	T_{op}	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS — AUDIO SECTION (T_A = 25°C, Circuit of Figure 2)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Current, No Signal, Pin 14	I_{CC}	—	11	19	mAdc
Gain	A_o	—	50	—	V/V
Distortion at 50 mW Output 1.0 kHz	V_{out} THD	—	0.1	1.0	%
Distortion at 750 mW Output 1.0 kHz	V_{out} THD	—	0.5	—	%
Quiescent Output Voltage, No Signal	$V_{Pin\ 10}$	—	8.0	—	Vdc
Input Bias	$V_{Pin\ 9}$, $V_{Pin\ 15}$	—	0.7	—	Vdc
Input Resistance	R_{in} Pin 15	—	28	—	kΩ
Output Noise (50 Hz–15 kHz) Input 50 Ω	V_{out}	—	0.5	4.0	mV_{RMS}

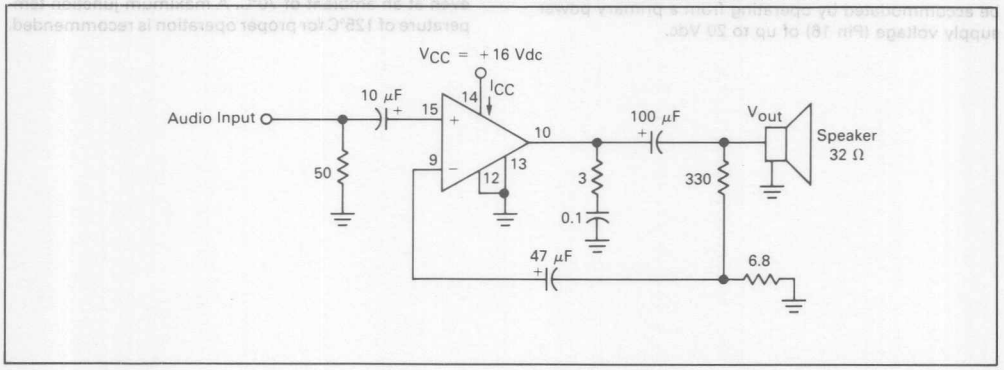
ELECTRICAL CHARACTERISTICS — VERTICAL SECTION (T_A = 25°C, Circuit of Figure 3)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Current, Max Height Control	I_{yoke}	—	500	—	mApp
Power Supply Current	I_{CC}	—	75	—	mAdc
Flyback Voltage, Pin 6	$V_{Pin\ 6}$	—	30	—	Vpk
Pull-Up Current, Max Height Control	$V_{Pin\ 2}$	—	250	—	mApk

ELECTRICAL CHARACTERISTICS — COMBINATION (T_A = 25°C, Circuits of Figures 2 and 3)

Characteristic	Symbol	Min	Typ	Max	Unit
Residual Vertical Buzz-In Audio Output, Vertical Set at 400 mA p-p Output	—	—	6.0	—	mV_{RMS}

FIGURE 2 — TEST CIRCUIT AND TYPICAL APPLICATION, AUDIO SECTION



CIRCUIT DESCRIPTION AND APPLICATION

AUDIO SECTION

The audio amplifier is a rather conventional IC implementation capable of over 1.0 watt output if applied to a 16 Ω speaker at 16 V. However, since the chip is also required to do the vertical output task, it is recommended that the audio section be used with 32 Ω speakers and 16 V, or 16 Ω and 12 V. Either condition will keep power output to about 750 mW at 10% THD. The output (Pin 10) should have the usual 3.0 Ω/0.1 μF snubber located close to the IC for prevention of high frequency oscillation. Voltage gain is set by the resistor divider feeding back to Pin 9. Both the input (Pin 15) and feedback (Pin 9) are internally biased to 0.7 Vdc, and should never be driven below ground.

The designer should keep in mind that this is a Class B audio section, and although it can be operated from supply voltages from 6.0 Vdc to 35 Vdc, there is no escaping the direct relationship of power supply ripple current to output current. The effect of this ripple on power supplies throughout the TV receiver must be minimized by normal external choices. If the TV is totally operated from a very solidly regulated source, the problems are minimal. If it is a low cost line-operated set, as illustrated in Figure 6, then good isolation can be more difficult. One suggestion is illustrated in Figure 6, where a horizontally derived +30 V supply is used to provide the vertical circuit with a vertical pulse clamping voltage and then is considerably decoupled (160 Ω and 50 μF) to provide the audio supply. This offers a good bit of protection from loading effects, and for the most common low audio duty cycles, will given a good supply voltage. It will, of course, sag badly at a steady high output, and is offered for consideration. It is more viable here than in most cases, due to the wide power supply tolerance of this IC.

VERTICAL SECTION

The vertical amplifier takes the approximately 1.5 Vp-p sawtooth output from Pin 22 of MONOMAX and converts it to an output sawtooth of up to 600 mA p-p in the vertical yoke. Yoke impedances of up to 40 Ω can be accommodated by operating from a primary power supply voltage (Pin 16) of up to 20 Vdc.

The MC13014P uses a boost switch to "step up" the operating voltage during retrace. This offers the benefits of keeping IC dissipation low, by allowing minimum V_{CC} during forward scan and permitting rapid retrace by having a highly effective clamp voltage. A comparator senses when the output at Pin 6 rises 0.7 V above the V_{CC} on Pin 16, and turns the boost transistor on, which quickly pulls up the operating voltage at Pin 7. The boost voltage can be provided either of two ways: a higher (than V_{CC}) supply, up to 40 V, can be connected to Pin 1 as shown in Figure 4, or the self boost configuration of Figure 3. In this application the 50 μF (Pin 7 to Pin 2) charges the V_{CC} during forward scan, through the 150 Ω. When retrace triggers the boost switch, this voltage is added to the V_{CC}, nearly doubling the operating voltage at Pin 7 during retrace. The 50 μF is selected to prevent excessive voltage change during retrace.

The vertical output, Pin 6, can source or sink 300 mA, and the boost switch has 300 mA pull-up capability. Supply voltage of 8–20 Vdc is recommended for V_{CC} in both Figures 3 and 4. Boost voltage for Figure 4 should be 25–40 V. There must be a good ground for Pins 4, 5, 12 and 13, which are both substrate and circuit ground, to avoid adding a vertical signal to the audio.

DISSIPATION AND THERMAL CONSIDERATIONS

The 16-pin copper lead frame has excellent thermal characteristics, but these are two big jobs, so attention to P_D is in order. The vertical application of Figure 3 at 400 mA p-p has a vertical section (IC) dissipation of about 300 mW. If the audio section Figure 2, is at a comparatively high output of 500 mW, the dissipation in that section is about 600 mW. Note that the rated $R_{\theta JA}$ of 80°C/W is for a worst case situation, with no help from a PC board, or any conducted heat from the pins. In a practical PC board effort, the $R_{\theta JA}$ can be reduced to approximately 50°C/W. With less than 1.0 watt dissipation, there is considerable safety margin, even at an ambient of 70°C. A maximum junction temperature of 125°C for proper operation is recommended.

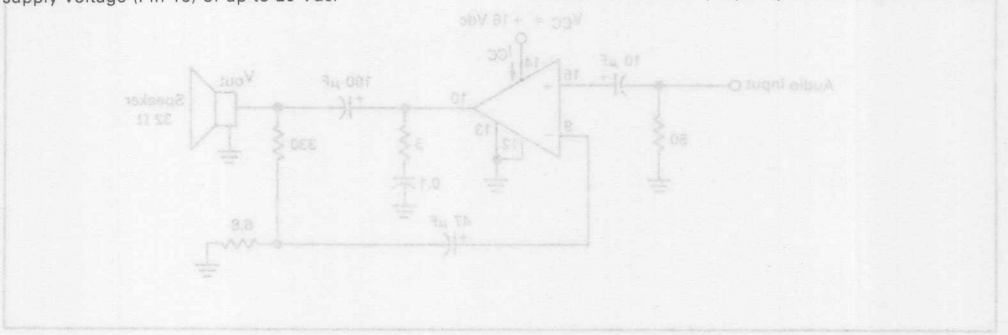


FIGURE 3 — TEST CIRCUIT VERTICAL SECTION AND TYPICAL APPLICATION — SELF BOOST

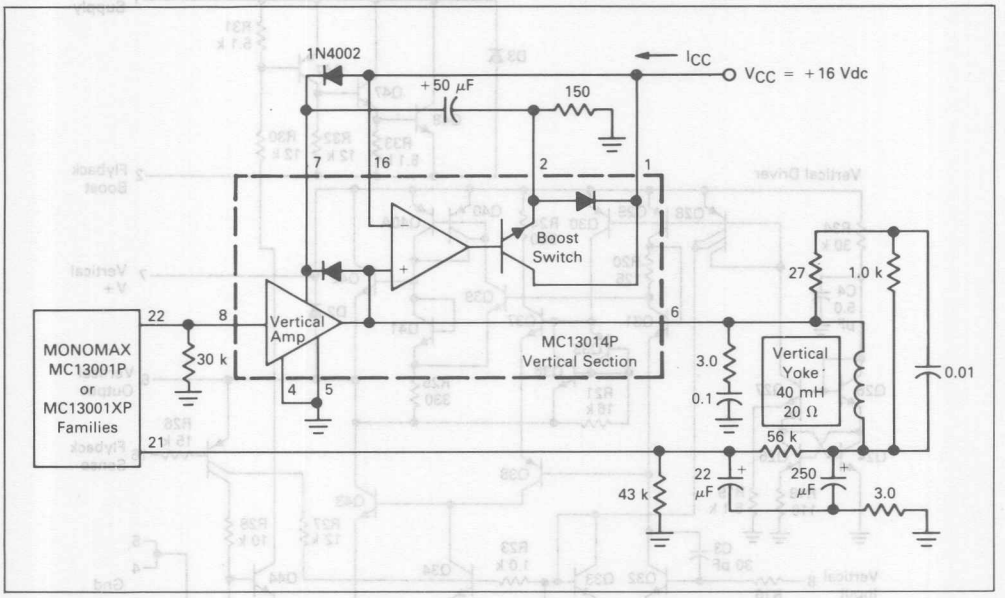
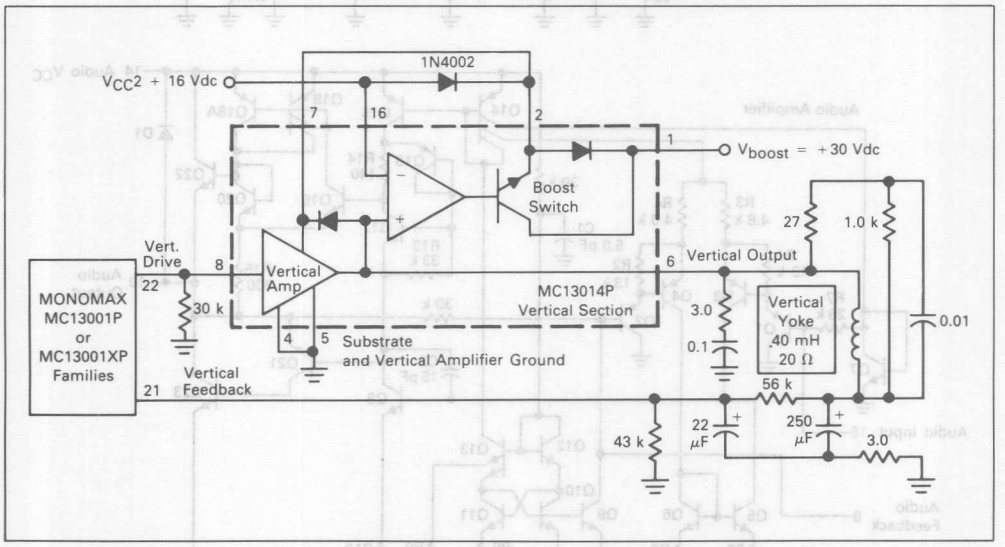
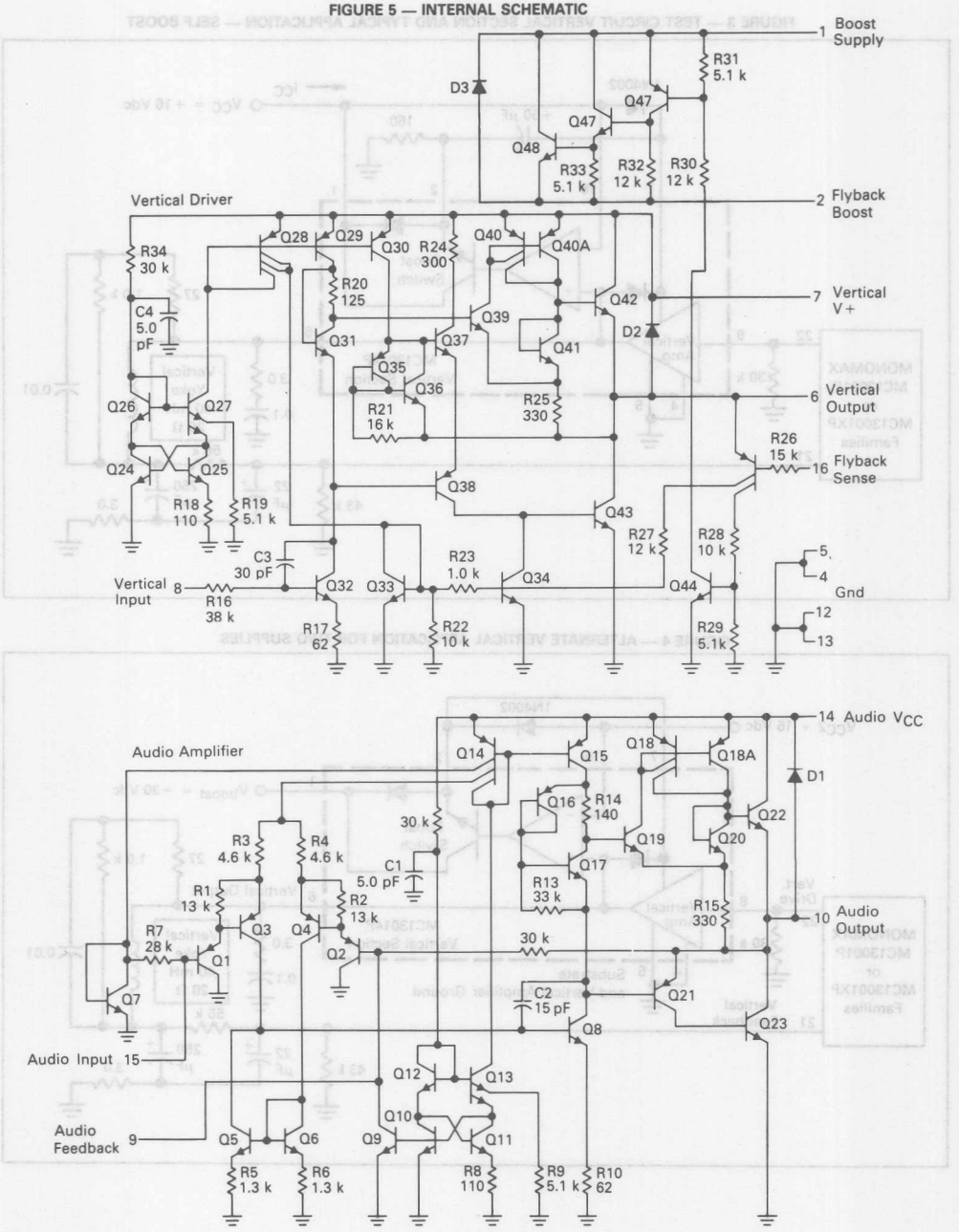


FIGURE 4 — ALTERNATE VERTICAL APPLICATION FOR TWO SUPPLIES



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FIGURE 5 — INTERNAL SCHEMATIC



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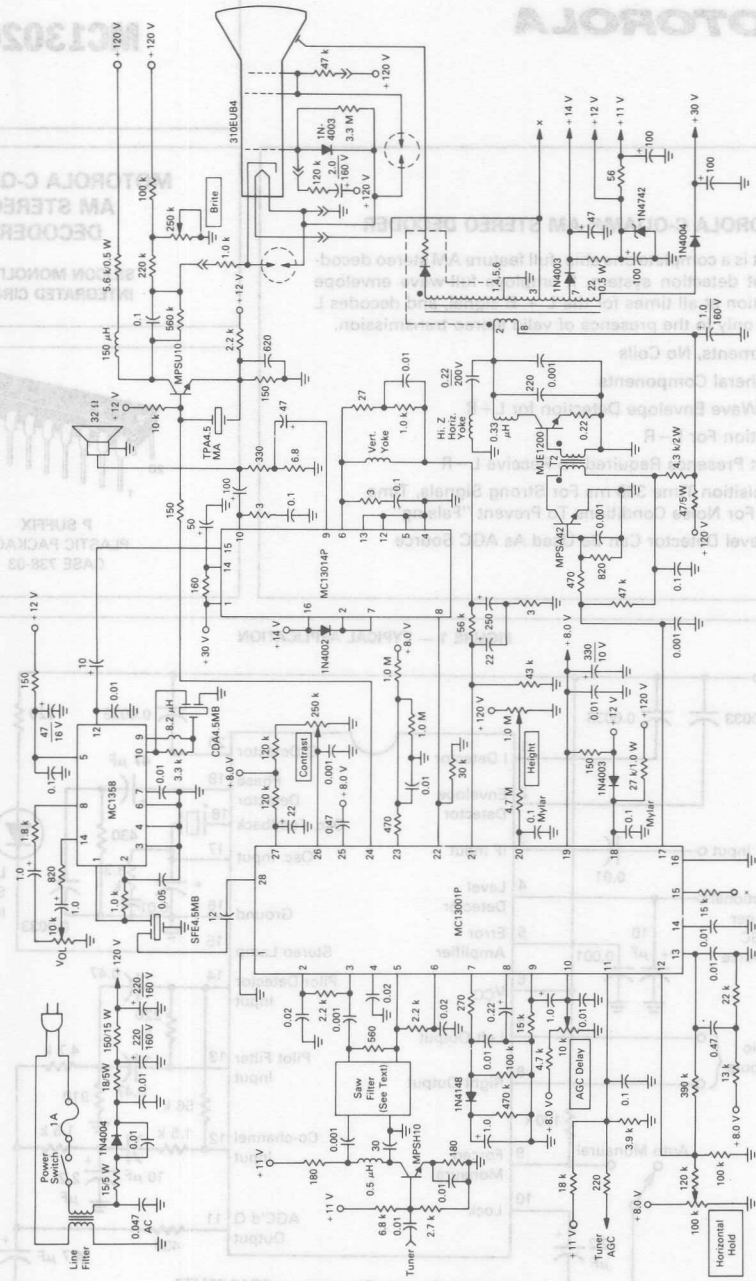


FIGURE 6 — LINE OPERATED RECEIVER SCHEMATIC

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MOTOROLA

MC13020P

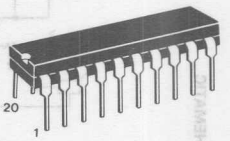
MOTOROLA C-QUAM® AM STEREO DECODER

SILICON MONOLITHIC INTEGRATED CIRCUIT

MOTOROLA C-QUAM® AM STEREO DECODER

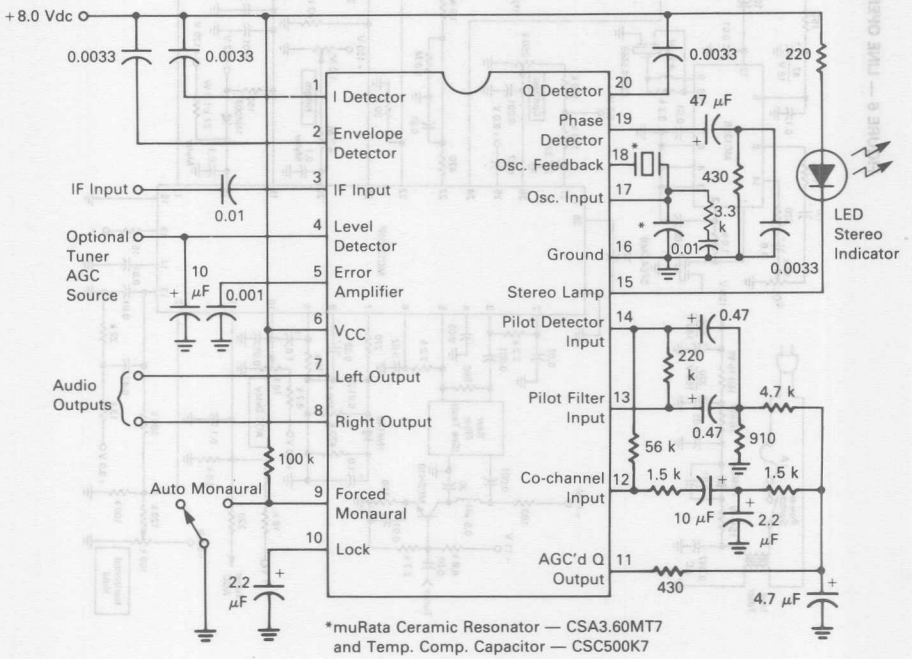
This circuit is a complete one chip, full feature AM stereo decoding and pilot detection system. It employs full-wave envelope signal detection at all times for the L + R signal, and decodes L − R signals only in the presence of valid stereo transmission.

- No Adjustments, No Coils
- Few Peripheral Components
- True Full Wave Envelope Detection for L+R
- PLL Detection For L−R
- 25 Hz Pilot Presence Required To Receive L−R
- Pilot Acquisition Time 300 ms For Strong Signals, Time Extended For Noise Conditions To Prevent "Falsing"
- Internal Level Detector Can Be Used As AGC Source



P SUFFIX
PLASTIC PACKAGE
CASE 738-03

FIGURE 1 — TYPICAL APPLICATION



*muRata Ceramic Resonator — CSA3.60MT7 and Temp. Comp. Capacitor — CSC500K7

The purchase of the Motorola C-QUAM® AM Stereo Decoder does not carry with such purchase any license by implication, estoppel or otherwise, under any patent rights of Motorola or others covering any combination of this decoder with other elements including use in a radio receiver. Upon application by an interested party, licenses are available from Motorola on its patents applicable to AM Stereo radio receivers.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	14	Vdc
Pilot Lamp Current, Pin 15		50	mAdc
Operating Temperature	T_A	−40 to +85	°C
Storage Temperature	T_{stg}	−65 to +150	°C
Junction Temperature	$T_{J(max)}$	150	°C
Power Dissipation Derate above 25°C	P_D	1.25 10	W mW/°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 8.0 Vdc, T_A = 25°C, Input Signal = 200 mVRMS (Unmodulated Carrier, Circuit Of Figure 1 Unless Otherwise Noted.)

Characteristic		Min	Typ	Max	Unit
Power Supply Operating Range		—	6.0 to 10	—	Vdc
Supply Line Current Drain, Pin 6		20	30	40	mAdc
Input Signal Level, Unmodulated, Pin 3, for Full Operation		100	200	357	mVRMS
Audio Output Level, 50% Modulation, L only or R only		160	220	280	mVRMS
Audio Output Level, 50% Modulation, Monaural		80	110	140	mVRMS
Output THD, 50% Modulation	Monaural Stereo	— —	0.5 1.0	— —	%
Channel Separation, L only or R only, 50% Modulation		—	30	—	dB
Pilot Acquisition Time, VCO locked, after release of forced monaural		—	300	—	ms
Input Impedance	R_{in} C_{in}	20 —	27 6.0	— —	kΩ pF
Output Impedance		—	100	150	Ω
Level Detector Filter Voltage, Pin 4,	0 signal 200 mVRMS Signal	1.4 —	1.7 2.5	2.0 —	Vdc
Lock Detector Filter Voltage, Pin 10	In Lock Out of Lock	— —	7.8 0.8	— —	Vdc
Force to Monaural, Pin 9, Pull Down for Monaural Mode		2.0 —	2.5 0.15	— 1.0	Vdc μA
Force to Monaural, Pin 9, Pull Up for Automatic Mode		— —	3.5 <0.001	3.7 1.0	Vdc μA

FIGURE 2 — BASIC QUADRATURE AM (QUAM)

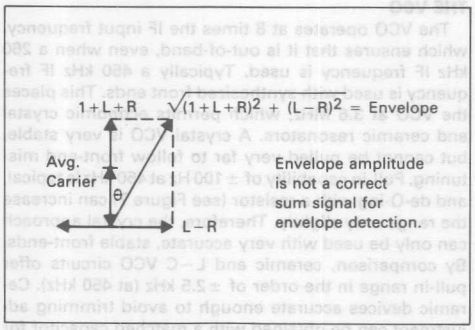
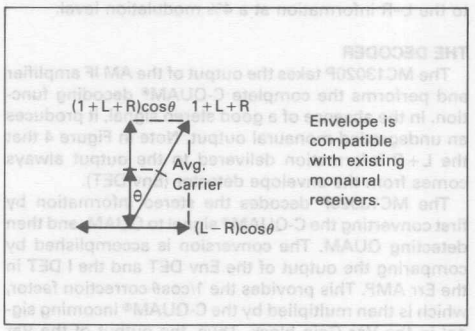
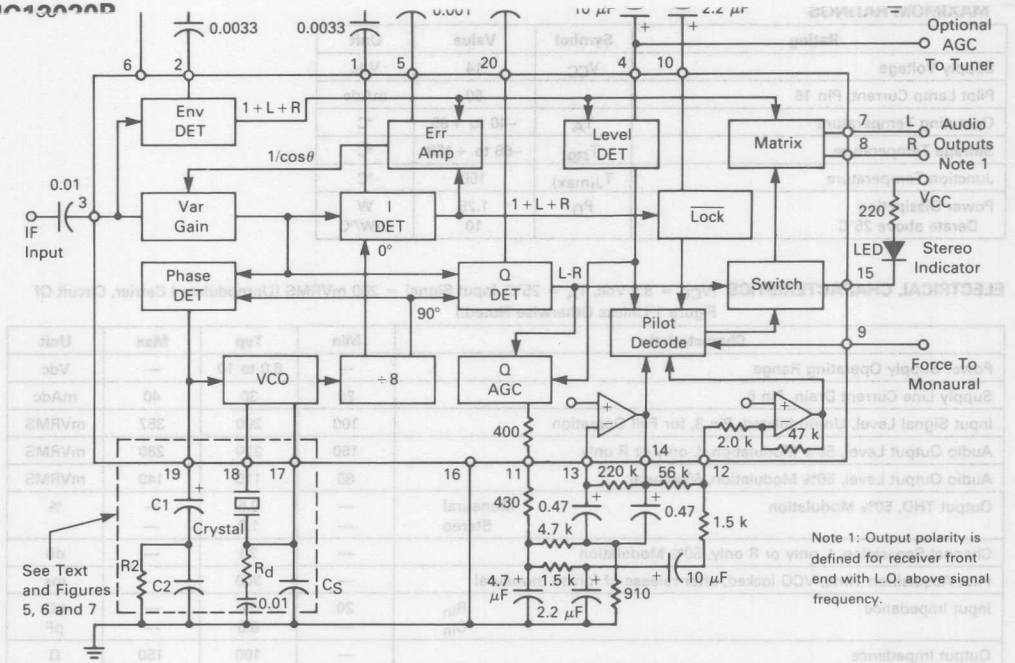


FIGURE 3 — MOTOROLA C-QUAM®



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MOTOROLA C-QUAM® — COMPATIBLE QUADRATURE AM STEREO

9

INTRODUCTION

In C-QUAM®, conventional quadrature amplitude modulation has been modified by multiplying each axis by cosθ as shown in Figures 2 and 3. The resulting carrier envelope is 1+L+R, i.e., a correct sum signal for monaural receivers and for stereo receivers operating in monaural mode. A 25 Hz pilot signal is added to the L–R information at a 4% modulation level.

THE DECODER

The MC13020P takes the output of the AM IF amplifier and performs the complete C-QUAM® decoding function. In the absence of a good stereo signal, it produces an undegraded monaural output. Note in Figure 4 that the L+R information delivered to the output always comes from the envelope detector (Env DET).

The MC13020P decodes the stereo information by first converting the C-QUAM® signal to QUAM, and then detecting QUAM. The conversion is accomplished by comparing the output of the Env DET and the I DET in the Err AMP. This provides the 1/cosθ correction factor, which is then multiplied by the C-QUAM® incoming signal in the Var Gain block. Thus, the output of the Var Gain block is a QUAM signal, which can then be synchronously detected by conventional means. The I and Q detectors are held at 0° and 90° relative demodulation angles by reference signals from the phase-locked, divided-down VCO. The output of the I DET is 1+L+R, with the added benefit (over the Env DET) of being able to produce a negative output on strong co-channel or noise interference. This is used to tell the Lock circuit to go to monaural operation. The output of the Q DET is the L−R and pilot information.

THE VCO

The VCO operates at 8 times the IF input frequency, which ensures that it is out-of-band, even when a 260 kHz IF frequency is used. Typically a 450 kHz IF frequency is used with synthesized front ends. This places the VCO at 3.6 MHz, which permits economic crystal and ceramic resonators. A crystal VCO is very stable, but cannot be pulled very far to follow front-end mistuning. Pull-in capability of ± 100 Hz at 450 kHz is typical, and de-Q-ing with a resistor (see Figure 7) can increase the range only slightly. Therefore, the crystal approach can only be used with very accurate, stable front-ends. By comparison, ceramic and L−C VCO circuits offer pull-in range in the order of ±2.5 kHz (at 450 kHz). Ceramic devices accurate enough to avoid trimming adjustment can be obtained with a matched capacitor for Cs (see Figures 1 and 5).

In the PLL filter circuit on Pin 19, C1 is the primary factor in setting a loop corner frequency of 8–10 Hz, in-lock. An internally controlled fast pull-in is provided. R2 is selected to slightly overdamp the control loop, and C2 prevents high frequency instability.

The Level DET block senses carrier level and provides an optional tuner AGC source. It also operates on the Q AGC block to provide a constant amplitude of 25 Hz pilot at Pin 11, and it delivers information to the pilot decoder regarding signal strength.

PILOT AND CO-CHANNEL FILTERS

The Q AGC output drives a low pass filter, made up of 400 Ω internal, and 430 Ω and 5 μF external. From this point, an active 25 Hz band-pass filter is coupled to the Pilot Decoder, Pin 14, and another low-pass filter is connected to the Co-channel Input, Pin 12. A 2:1 reduction of 25 Hz pilot level to the Pilot Decode circuit will cause the system to go monaural, with the components shown. Refer to Figure 8 for the formulas governing the active band-pass filter. The co-channel input signal contains any low frequency intercarrier beat notes, and, at the selected level, prevents the Pilot Decode circuit from going into stereo. The co-channel input, Pin 12, gain can be adjusted by changing the external 1.5 k resistor. The values shown set the "trip" level at about 7% modulation. The 25 Hz pilot signal at the output of the active filter is opposite in phase to the pilot signal coming from the second low-pass filter. The 56 k resistor from Pin 14 to Pin 12 causes the pilot to be cancelled at the co-channel input. This allows a more sensitive setting of the co-channel trip level.

THE PILOT DECODER

The Pilot Decoder has two modes of operation. When signal conditions are good, the decoder will switch to stereo after 7 consecutive cycles of the 25 Hz pilot tone. When signal conditions are bad, the detected interference changes the pilot counter so as to require 37 consecutive cycles of pilot to go to stereo. In a frequency synthesized radio, the logic that mutes the audio when tuning can be connected to Pin 9. When this pin is held low it holds the decoder in monaural mode and switches it to the short count. This pin should be held low until the synthesizer and decoder have both locked onto a new station. A 300 ms delay should be sufficient. If the synthesizer logic does not provide sufficient delay, the circuit shown in Figure 9 may be added. Once Pin 9 goes high, the Pilot Decoder starts counting. If no pilot is detected for seven consecutive counts, it is assumed to be a good monaural station and the decoder is switched to the long count. This reduces the possibility of false stereo triggering due to signal level fluctuation or noise. If the PLL goes out of lock, or interference is detected by the co-channel protection circuit before seven cycles are counted, the decoder goes into the long count mode. Each disturbance will reset the counter to zero. The Level Detector will keep the decoder from going into stereo if the IF input level drops 10 dB, but will not change the operation of the pilot counter.

Once the decoder has gone into the stereo mode, it will go instantly back to monaural if either the lock detector on Pin 10 goes low, or if the carrier level drops below the preset threshold. Seven consecutive counts of no pilot will also put the decoder in monaural. In stereo, the co-channel input is disabled, and co-channel or other noise is detected by negative excursions of the I DET, as mentioned earlier. When these excursions reach a level caused by approximately 20% modulation of co-channel, the lock detector puts the system in monaural, even though the PLL may still actually be locked. This higher level of co-channel tolerance provides the hysteresis to prevent chattering in and out of stereo on a marginal signal.

When all inputs to the Pilot Decode block are correct, and it has completed its count, it turns on the Switch, sending the L – R to the Matrix, and switches the pilot lamp pin to a low impedance to ground.

SUMMARY

It should be noted that in C-QUAM®, with both channels AM modulated, the noise increase in stereo is a maximum of 3.0 dB, less on program material. Therefore, this is not the major concern in the choice of monaural to stereo switching point as it was in FM, and blend is not needed.

PIN DESCRIPTIONS

Pin 1, 2 — Detector Filters, R_{out} = 4.3 k, recommend 0.0033 μF to V_{CC} to filter 450 kHz components.
Pin 3 — IF Signal Input
Pin 4 — Level Detector filter pin, R_{out} = 8.2 k, 10 μF to ground sets the AGC time constant. High impedance output, needs buffer.
Pin 5 — Error Amp compensation to stabilize the Var Gain feedback loop
Pin 6 — V_{CC}, 6-10 Vdc, suitable for low V_{batt} automotive operation, but must be protected from "high line" condition.
Pin 7, 8 — Left and Right Outputs, NPN emitter followers
Pin 9 — Forced Monaural, MOS or TTL controllable
Pin 10 — Lock detector filter, R_{out} = 27 k, recommend 2.2 μF to ground.
Pin 11 — AGC'd Q output, NPN emitter follower with 400 Ω from emitter to Pin 11
Pin 12 — Co-channel Input, 2.0 k series in and 47 k feedback
Pin 13 — Pilot Filter Input to op amp, see Figure 8
Pin 14 — Pilot Decode Input (op amp output) emitter follower, R_{out} = 100 Ω
Pin 15 — Stereo Lamp, open-collector of an NPN common emitter stage, can sink 50 mA, V_{sat} = 0.3 V at 5.0 mA
Pin 16 — Ground
Pin 17 — Oscillator input, R_{in} = 10 k, do not dc connect to Pin 18 or ground
Pin 18 — Oscillator feedback, NPN emitter, R_{out} = 100 Ω
Pin 19 — Phase Detector Output, current source to filter
Pin 20 — Detector Filter, R_{out} = 4.3 k, recommend 0.0033 μF to V_{CC} to filter 450 kHz

FIGURE 5 — CERAMIC VCO

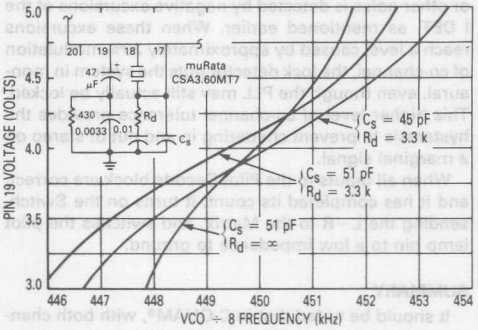


FIGURE 6 — L – C VCO

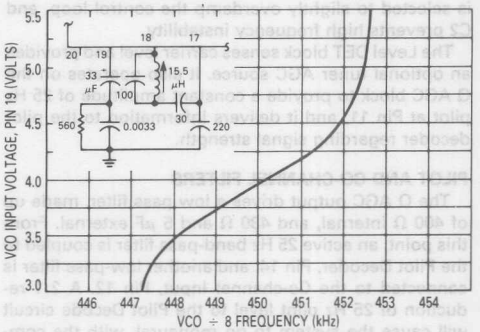


FIGURE 7 — CRYSTAL VCO

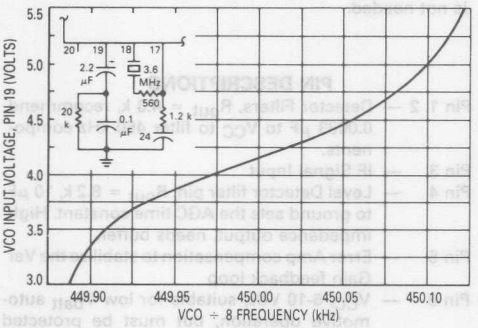
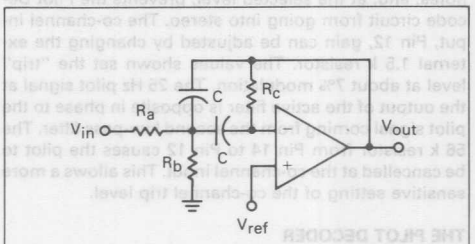


FIGURE 8 — ACTIVE BAND-PASS FILTER



$$R_c = \frac{Q}{\pi f_o C}$$

$$R_a = \frac{R_c}{2 A_o}$$

$$R_b = \frac{R_a R_c}{4Q^2 R_a - R_c}$$

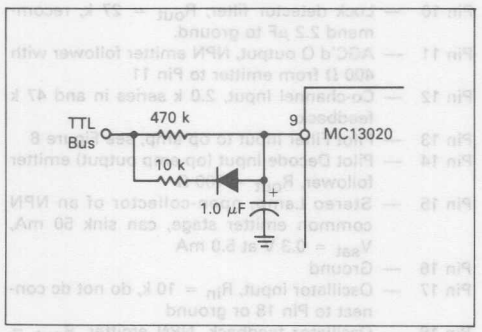
where, in this application:
f_o = center frequency = 25 Hz
A_o = gain at $f_o \leq 25$
$Q \leq 10$

Choose values for f_o, A_o, Q, and convenient C, solve for resistors

C ± 5%	R_a ± 5%	R_b ± 1%	R_c ± 1%
0.47 µF	4.7 k	910	220 k
0.33 µF	8.2 k	1.3 k	330 k

Note: Capacitor C should be a good grade, low ESR.

FIGURE 9 — FORCED MONAURAL OPTIONAL DELAY CIRCUIT



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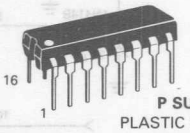
MOTOROLA

MC13021

Product Preview

MOTOROLA C-QUAM® AM STEREO TUNING STABILIZER

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 648-06

AM STEREO TUNING STABILIZER

AM stereo systems are basically microphonic. They require a high degree of local oscillator stability in the receiver front end, particularly with respect to mechanical vibration in the audible range. Motion of physical components which affect oscillator frequency can generate significant audio output via the L-R or stereo information channel. To date, this has meant that most quality AM stereo implementations were done with PLL synthesized tuners. The MC13021 offers a low cost means of obtaining PLL stability in conventional mechanically tuned radios.

- Provides AFC for Tuning Accuracy and Ease
- Eliminates Microphonic Responses
- Provides Tuning Lock Indication
- Uses Existing Mechanical Tuning Elements

The MC13021 is appropriate at both ends of the cost spectrum, from low priced mechanical auto radios to high end component hi-fi receivers using non-varactor tuning. The oscillator drive comes out at two levels to accommodate inductively or capacitively tuned systems. It is designed to work with the MC13020 C-QUAM decoder and any discrete or IC AM front end, such as the MC13041 (ULN3841).

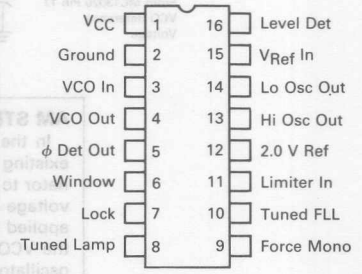


FIGURE 1 — TUNING MODE

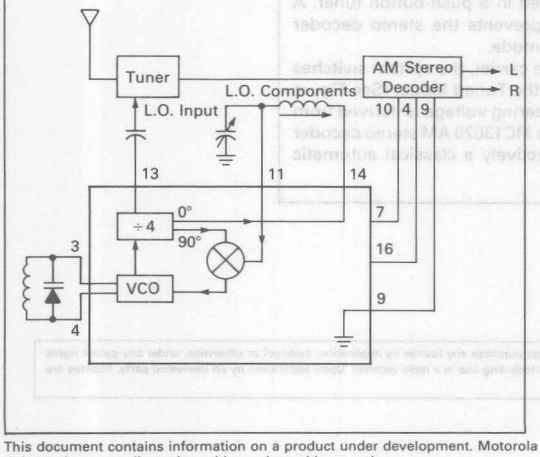
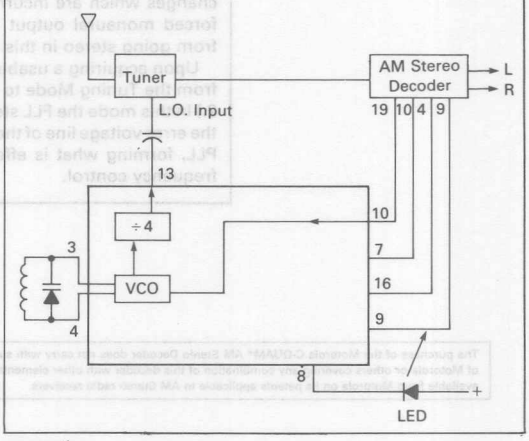
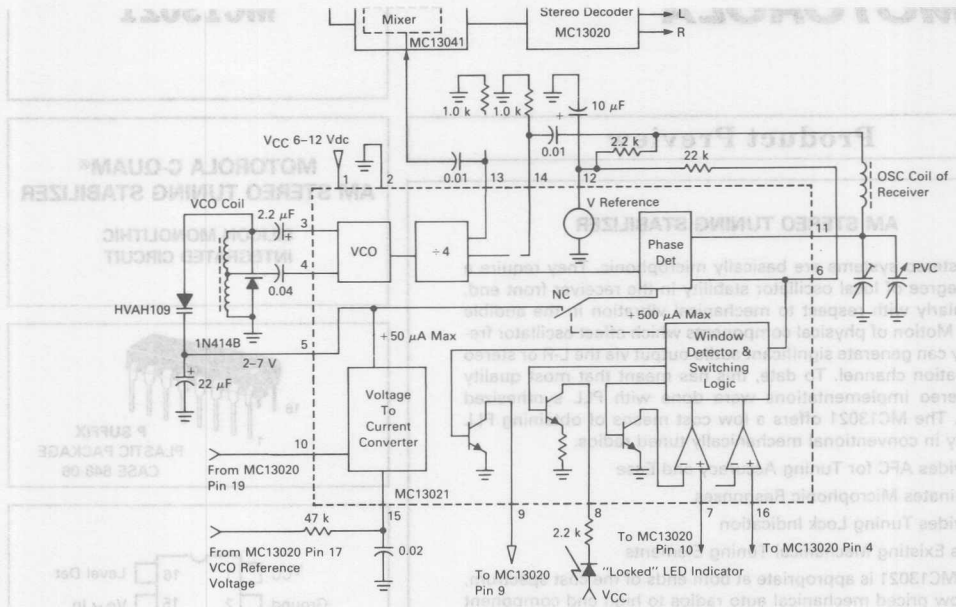


FIGURE 2 — TUNED MODE



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AM STEREO TUNING STABILIZER

In the Tuning Mode (Figure 1) the loop utilizes the existing tuner oscillator coil as a frequency discriminator to generate a dc voltage which is used to steer a voltage controlled oscillator (VCO). The VCO output is applied to the discriminator to close the loop, forcing the VCO to track the resonant frequency of the tuner oscillator coil.

The output of the VCO is used as the receiver local oscillator. In this mode the amount of the noise reduction is limited by the need to track the manual tuning control without producing a delay that is perceptible to the user, and it must be able to follow the rapid tuning changes which are incurred in a push-button tuner. A forced monaural output prevents the stereo decoder from going stereo in this mode.

Upon acquiring a usable carrier, the system switches from the Tuning Mode to the Tuned Mode. (See Figure 2.) In this mode the FLL steering voltage is derived from the error voltage line of the MC13020 AM stereo decoder PLL, forming what is effectively a classical automatic frequency control.

The purchase of the Motorola C-QUAM® AM Stereo Decoder does not carry with such purchase any license by implication, estoppel or otherwise, under any patent rights of Motorola or others covering any combination of this decoder with other elements including use in a radio receiver. Upon application by an interested party, licenses are available from Motorola on its patents applicable to AM Stereo radio receivers.

MOTOROLA

MC13022

Product Preview

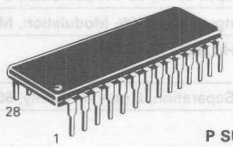
ADVANCED, MEDIUM VOLTAGE AM STEREO DECODER

The MC13022 is designed for home, portable, and automotive AM stereo radio applications. The circuits and functions included in the design allow implementation of a full-featured C-QUAM AM stereo radio with relatively few, inexpensive external parts. It is available in either 28-lead DIP or EIAJ compatible wide-bodied 28-lead SOIC.

- Operation from 4.0 V to 10 V Supply with Current Drain of 18 mA Typ
- IF Amplifier with Two Speed AGC
- Post Detection Filters with 10 kHz Notch that Allow User or Automatic Adjustable Audio Bandwidth Control
- Signal Quality Controlled Stereo Blend and Noise Reduction
- Noise and Co-Channel Discriminating Stop-On-Station
- Signal Strength Indicator Output for RF AGC and/or Meter Drive
- Signal Strength Controlled IF Bandwidth
- Noise Immune Pilot Detector Needs no Precision Filter Components

C-QUAM® ADVANCED, MEDIUM VOLTAGE AM STEREO DECODER

SILICON MONOLITHIC INTEGRATED CIRCUIT



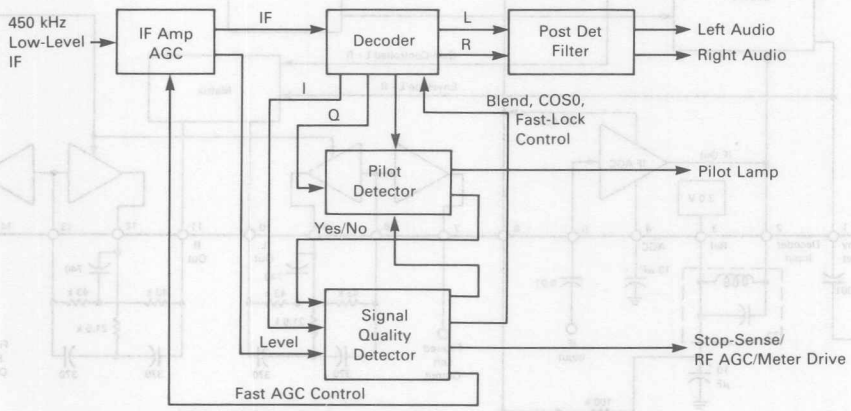
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CASE 710-02



DW SUFFIX
PLASTIC PACKAGE
CASE 751F-02

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FIGURE 1 — BASIC ELEMENTS OF THE SYSTEM



The purchase of the Motorola C-QUAM® AM Stereo Decoder does not carry with such purchase any license by implication, estoppel or otherwise, under any patent rights of Motorola or others covering any combination of this decoder with other elements including use in a radio receiver. Upon application by an interested party, licenses are available from Motorola on its patents applicable to AM Stereo radio receivers.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	12	Vdc
Pilot Lamp Current, Pin 21		30	mAdc
Operating Temperature	T_A	−40 to +85	°C
Storage Temperature	T_{stg}	−65 to +150	°C
Junction Temperature	$T_{J(max)}$	150	°C
Power Dissipation Derate above 25°C	P_D	1.25 10	W mW/°C

ELECTRICAL CHARACTERISTICS

Characteristic		Min	Typ	Max	Unit
Power Supply Operating Range		—	4.0 to 10	—	Vdc
Supply Line Current Drain, Pin 25		—	18	—	mAdc
Input Signal Level, Unmodulated, Pin 5, for Full Operation		—	5.0	—	mVrms
Audio Output Level, 50% Modulation, L only or R only		—	120	—	mVrms
Audio Output Level, 50% Modulation, Monaural		—	60	—	mVrms
Output THD, 50% Modulation	Monaural	—	0.2	—	%
	Stereo	—	0.5	—	
Channel Separation, L only or R only, 50% Modulation		—	32	—	dB

FIGURE 2 — BLOCK DIAGRAM

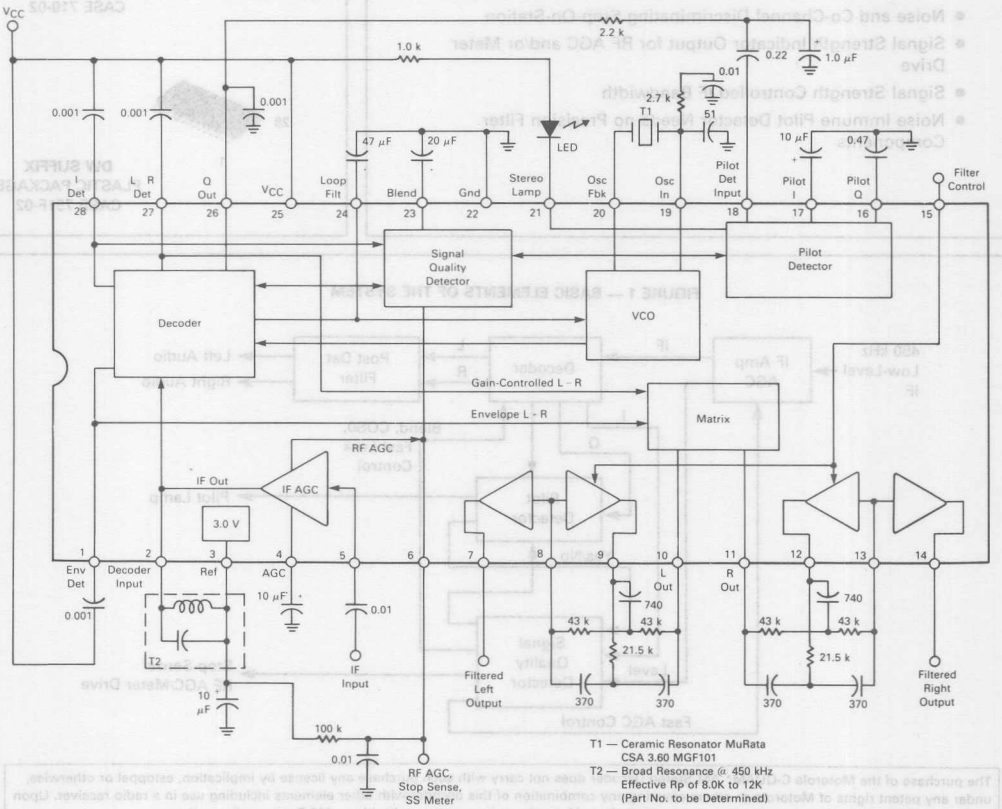


FIGURE 3 — OVERALL SELECTIVITY OF A TYPICAL RECEIVER versus FILTER CONTROL VOLTAGE

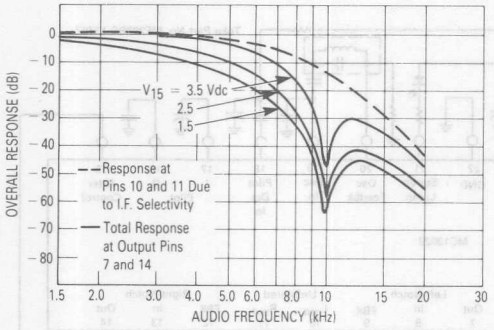
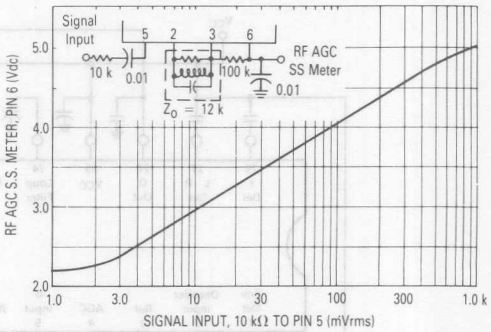


FIGURE 4 — RF AGC/SIGNAL STRENGTH OUTPUT versus INPUT SIGNAL



EXPLANATION OF FEATURES

BLEND AND NOISE REDUCTION

Although AM stereo does not have the extreme difference in S/N between mono and stereo that FM does (typically less than 3.0 dB versus greater than 20 dB for FM), sudden switching between mono and stereo is quite apparent. Some forms of interference such as co-channel have a large L – R component that makes them more annoying than would ordinarily be expected for the measured level. The MC13022 measures the interference level and reduces L – R as interference increases, blending smoothly to mono. The pilot indicator remains on as long as a pilot signal is detected, even when interference is severe, to minimize annoying pilot light flickering.

RF AGC/METER DRIVE

A dc voltage proportional to the log of signal strength is provided at Pin 6. This can be used for RF AGC, signal strength indication, and/or control of the post detection filter. Normal operation is above 2.2 V as shown in Figure 4.

STOP SENSE

Multiplexed with the signal strength information is the stop sense signal. The stop sense is activated when scanning by externally pulling the blend capacitor on Pin 23 below 0.5 V. This would typically be done from the mute line in a frequency synthesizer.

If at any time Pin 23 is low and there is either no signal in the IF or a noisy signal of a predetermined interference level, Pin 6 will go low. This low can be used to tell the frequency synthesizer to immediately scan to the next channel. The interference detection prevents stopping on many unlistenable stations, a feature particularly useful at night when many frequencies may have strong signals from multiple co-channel stations.

IF BANDWIDTH CONTROL

IF AGC attenuates the signal by shunting the signal at the IF input. This widens the IF bandwidth by decreasing the loaded Q of the input coupling coil as signal strength increases.

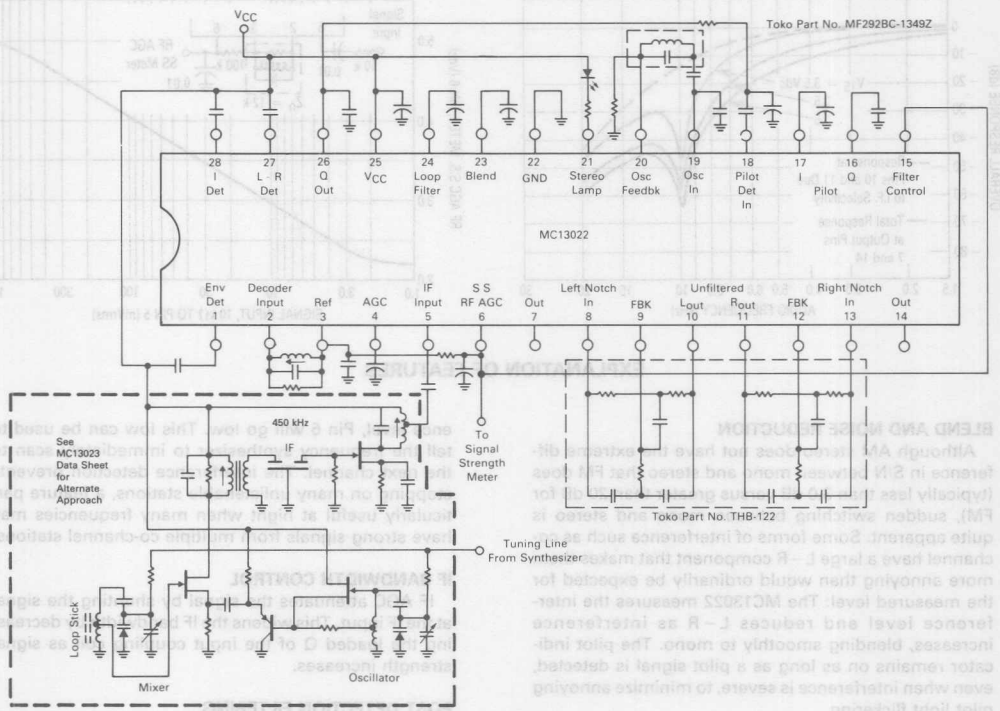
POST DETECTION FILTERING

With weak, noisy signals, high frequency rolloff greatly improves the sound. Conventional tone controls do not attenuate the highs sufficiently to control noise without also significantly affecting the mid-range. Also, notch filters are necessary with any wide-band AM radio to eliminate the 10 kHz whistle from adjacent stations.

By using a twin-T filter with variable feedback to the normally grounded center leg, a variable Q notch filter is formed that provides both the 10 kHz notch and variable high frequency rolloff functions. Typical range of response is shown in Figure 3. Response is controlled by the dc voltage on Pin 15.

Pin 15 could interface with a dc operated tone control such as the TDA1524, or could be tied to Pin 6 for automatic audio bandwidth control as a function of signal strength.

FIGURE 5 — HIGH PERFORMANCE HOME TYPE AM STEREO RECEIVER



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MOTOROLA

MC13023

Product Preview

AM STEREO FRONT END AND TUNER STABILIZER

The MC13023 is a companion part to the MC13022 C-QUAM AM STEREO DECODER. It provides the mixer, local oscillator, and IF amplifier to make a complete AM stereo tuner system. Also included is all circuitry needed to provide the tuning function for high performance manually tuned radios, and a wideband RF AGC circuit for very wide dynamic range systems. The wideband AGC can be disabled to save current in battery powered applications where it is not needed.

For Manual and Electronically Tuned Radios:

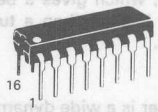
- Operation from 4.0 V to 10 V Supply
- Complete "Front End" for Home and Portable Radios
- Wideband AGC for External RF Amplifier in Automotive Type Radios
- Local Oscillator Unaffected by RF Signal Variations

For Manually Tuned Radios:

- Provides AFC for Tuning Ease and Accuracy
- Eliminates Microphonic Responses
- Provides Tuned Lock Indication
- Uses Existing Mechanical Tuning Elements
- Narrows Audio Bandwidth in MC13022 While Tuning to Reduce Interstation Noise

MOTOROLA C-QUAM® AM RECEIVER FRONT END AND TUNER STABILIZER

SILICON MONOLITHIC INTEGRATED CIRCUIT



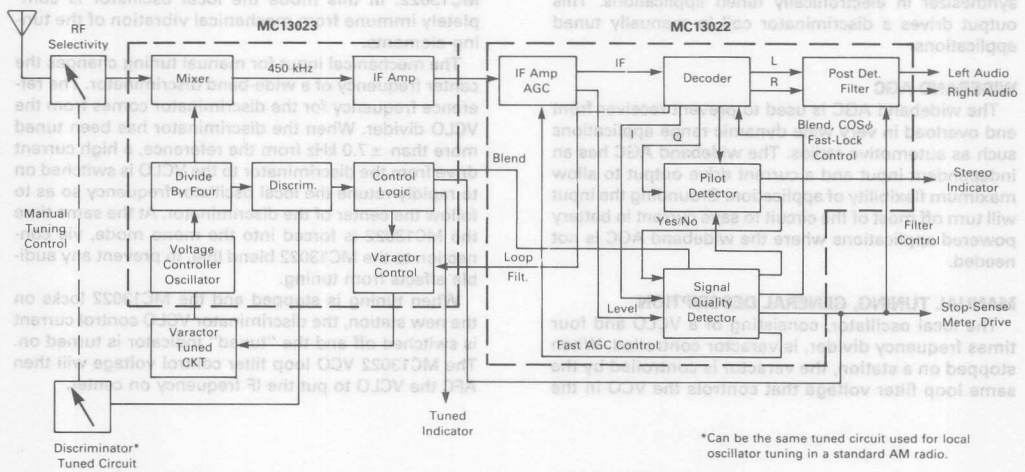
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CASE 648-06



D SUFFIX
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SO-16

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FIGURE 1 — MANUALLY TUNED SYSTEM



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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	12	Vdc
Pilot Lamp Current, Pin 9		20	mAdc
Operating Temperature	T_A	−40 to +85	°C
Storage Temperature	T_{stg}	−65 to +150	°C
Junction Temperature	$T_{J(max)}$	150	°C
Power Dissipation Derate above 25°C	P_D	1.25 10	W mW/°C

CIRCUIT DESCRIPTION

MIXER

The mixer is doubly balanced and has an extended dynamic range. The output is single ended and works into a resistive load, which gives a better impedance match to a ceramic IF filter than a tuned circuit and simplifies alignment.

IF AMPLIFIER

The first IF amplifier is a wide dynamic range design that needs no AGC. All IF AGC is done in the MC13022 by a shunt attenuator preceding the second IF stage. The shunt attenuator has the additional benefit of providing a variable load on the IF coupling coil, which reduces the bandwidth at low signal amplitudes.

OSCILLATOR

The single pin oscillator runs at four times the local oscillator mixer injection frequency. The VCLO is varactor tuned by the frequency synthesizer in electronically tuned applications and by internal varactor drive control in manually tuned applications. The frequency divider isolates the VCLO from any load changes caused by varying incoming RF signal strength. There is also a local oscillator buffered output for driving a frequency synthesizer in electronically tuned applications. This output drives a discriminator coil in manually tuned applications.

WIDEBAND AGC

The wideband AGC is used to prevent receiver front end overload in very wide dynamic range applications such as automotive radios. The wideband AGC has an independent input and a current drive output to allow maximum flexibility of application. Grounding the input will turn off most of the circuit to save current in battery powered applications where the wideband AGC is not needed.

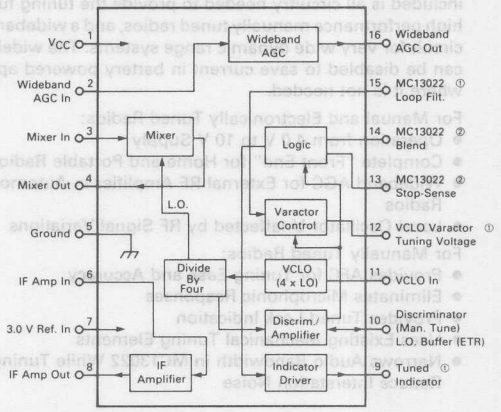
MANUAL TUNING, GENERAL DESCRIPTION

The local oscillator, consisting of a VCLO and four times frequency divider, is varactor controlled. When stopped on a station, the varactor is controlled by the same loop filter voltage that controls the VCO in the MC13022. In this mode the local oscillator is completely immune from mechanical vibration of the tuning elements.

The mechanical input for manual tuning changes the center frequency of a wide-band discriminator. The reference frequency for the discriminator comes from the VCLO divider. When the discriminator has been tuned more than ±7.0 kHz from the reference, a high current drive from the discriminator to the VCLO is switched on to rapidly retune the local oscillator frequency so as to follow the center of the discriminator. At the same time the MC13022 is forced into the mono mode, via connection to the MC13022 blend line, to prevent any audible effects from tuning.

When tuning is stopped and the MC13022 locks on the new station, the discriminator VCLO control current is switched off and the "tuned" indicator is turned on. The MC13022 VCO loop filter control voltage will then AFC the VCLO to put the IF frequency on center.

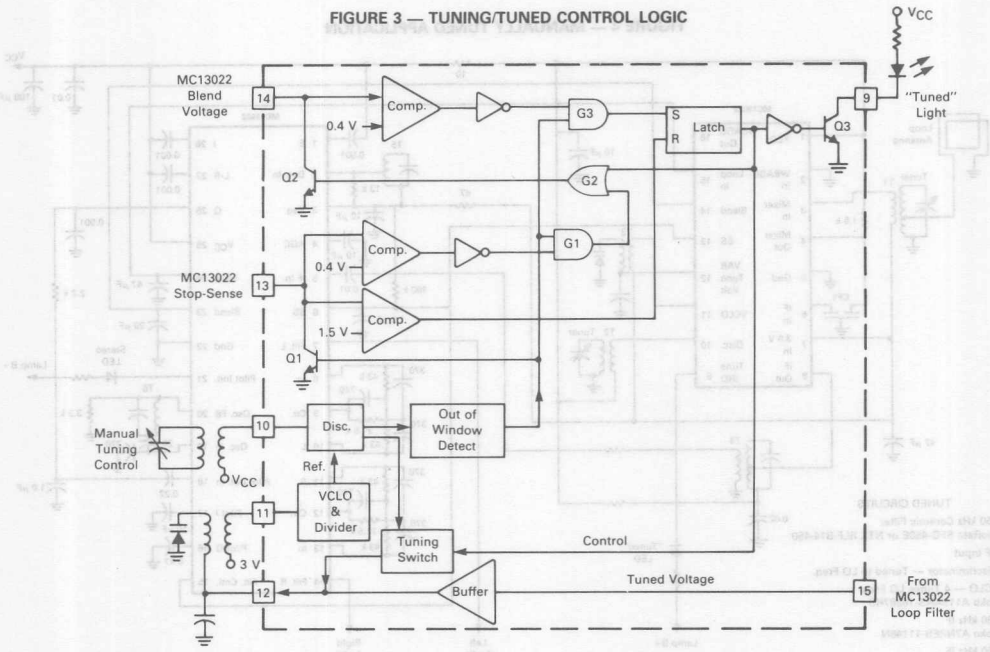
FIGURE 2 — PIN DESCRIPTION



① Manually Tuned Application only — not used for ETR
② Manually Tuned Application only — disabled by 100K Ohm to 3.0 V for ETR

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FIGURE 3 — TUNING/TUNED CONTROL LOGIC



MANUAL TUNING, DESCRIPTION OF CONTROL SEQUENCE

Assuming that the radio has been tuned to a stereo station, the MC13022 blend voltage would be at 3.6 V and the stop-sense voltage greater than 2.3 V. The MC13023 VCLO, see Figure 3, would have the varactor controlled through a buffer from the MC13022 VCO control. Q1 and Q2 are off and the "tuned" light is on, the latch being in the reset condition from the high on the stop-sense line. When the mechanical tuning control is moved to change to a new station the discriminator is tuned to a new frequency. The out-of-window detector immediately turns on Q1 to pull down the stop-sense/meter drive line of the MC13022. Where this line is also used to provide automatic audio bandwidth control, the pull-down reduces the bandwidth to approximately 2.0 kHz, thereby minimizing the annoying interstation noise.

As the stop-sense goes below 0.4 V, the blend line of the MC13022 is pulled down by Q2, controlled by the signal through gates G1 and G2. Between 2.2 V and 1.5 V on the blend line, the MC13022 blends the audio from stereo to mono. Below 0.7 V the pilot detector is turned off.

When the blend line goes below 0.4 V, the latch is set through Gate 3, the "tuned" light is turned off, and the control of the VCLO is switched to the discriminator.

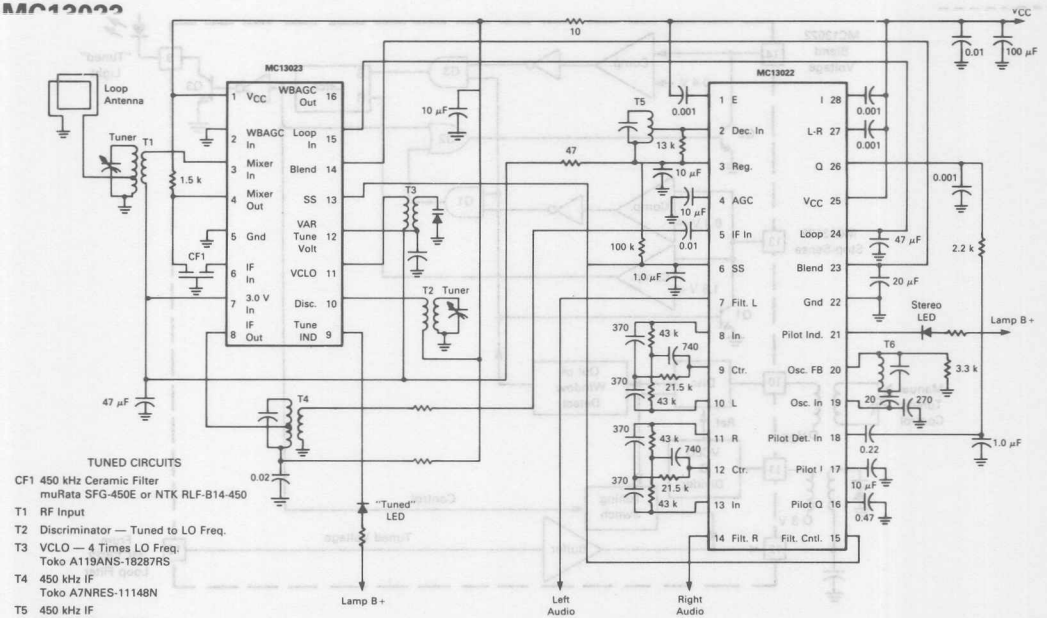
In the MC13022 the low blend voltage activates the fast AGC on the 2nd IF amplifier, sets a latch that will allow fast acquisition of stereo when pilot is detected, and activates the stop-sense. With the blend held low the stop-sense will act as a lock detector, staying low until the MC13022 VCO locks.

With the discriminator in control, the VCLO will be pulled to center the local oscillator frequency in the discriminator. Once within the tuned window, the window detector will release the pull-down on the stop-sense line. If the discriminator was not tuned on a station the MC13022 will not lock and will hold the stop-sense low, preventing any further action.

Assuming that the MC13022 does lock on to a station, the stop-sense will rise. At 1.5 V the latch will be reset, turning on the "tuned" light, releasing the pull-down on the blend line, and switching off the discriminator control of the VCLO.

The MC13022 decoder PLL will AFC the VCLO to put the IF frequency in the center of the IF as determined by the tuning of the VCO coil of the MC13022. The tuning control can now be adjusted within the ±7.0 kHz tuned window to fine tune the RF selectivity.

9



TUNED CIRCUITS

CF1 450 kHz Ceramic Filter
muRata SFG-450E or NTK RLF-B14-450

T1 RF Input

T2 Discriminator — Tuned to LO Freq.

T3 VCLO — 4 Times LO Freq.
Toko A119ANS-18287RS

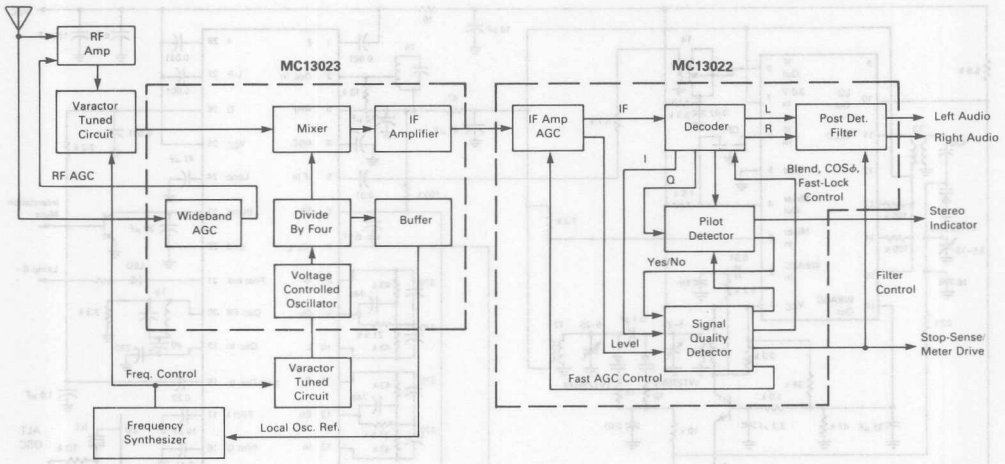
T4 450 kHz IF
Toko A7NRES-11148N

T5 450 kHz IF
Toko 7NRES-T1370Y

T6 Decoder VCO, 3.6 MHz
Toko 1349Z

9

FIGURE 5 — ELECTRONICALLY TUNED SYSTEM



ELECTRONICALLY TUNED RECEIVERS

Figure 5 is a block diagram showing the MC13023 in an electronically tuned system. Except for the four times oscillator and divider, it is similar to most standard AM radio systems. The RF stage and wideband AGC would typically be used in automobile radios. A home type receiver with loop antenna would not normally require the RF stage.

TYPICAL ETR APPLICATION

The performance of AM radios is limited primarily by overload problems such as desensitization, cross-modulation and intermodulation. Problems are caused by nonlinearities in the front end of the radio.

The most severe signal environment is seen by automotive radios as they pass through strong RF fields of nearby stations, and, for this reason, most applications use some form of front end AGC. A typical front end design is shown in Figure 6. This system uses a FET RF stage with AGC applied to a cascode transistor in series with the FET. The wideband AGC turns down the RF gain any time there is a strong signal present in a wide band of frequencies determined only by the selectivity of the first RF coil.

A HIGH PERFORMANCE ETR TUNER

Improvement in overload performance requires multiple solutions, since when one element of the circuit is improved, another part of the circuit will overload a few dB higher.

In the MC13023, the mixer, which is normally the first element to overload and become nonlinear on nearby signals, has been degenerated to give 8.0 to 10 dB improvement over a normal mixer. The mixer is protected by the total amount of RF selectivity for signals further out in frequency.

The next most vulnerable element is usually the tuning varactor on the first RF coil, followed by the wideband AGC elements and RF stage. Figure 7 shows a high performance front end circuit that is much better for overload than the circuit of Figure 6. The circuitry around the MC13022 remains the same.

A light dependent resistor (LDR) is used in front of the RF amplifier for attenuation. The LDR is much more linear and has a greater dynamic range than diodes or transistors that are sometimes used for RF AGC. The current through the LED, which in turn controls the resistance of the LDR, is varied by the wideband AGC.

The first RF coil is tuned with two back-to-back varactors, as is typically done in FM receivers, to make the circuit more linear. The second RF coil varactor is sufficiently protected by the first coil so that two varactors are not needed.

With the above improvements, the wideband AGC input can be taken after the second RF coil. This will prevent strong signals distant in frequency from a weak desired station from causing unnecessary attenuation or drop-out of the desired station.

The performance with the above improvements is now limited by overload in the FET RF amplifier. Slight degeneration with unbypassed source resistance greatly improves the overload performance with only a slight reduction in sensitivity.

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FIGURE 6 — ELECTRONICALLY TUNED APPLICATION

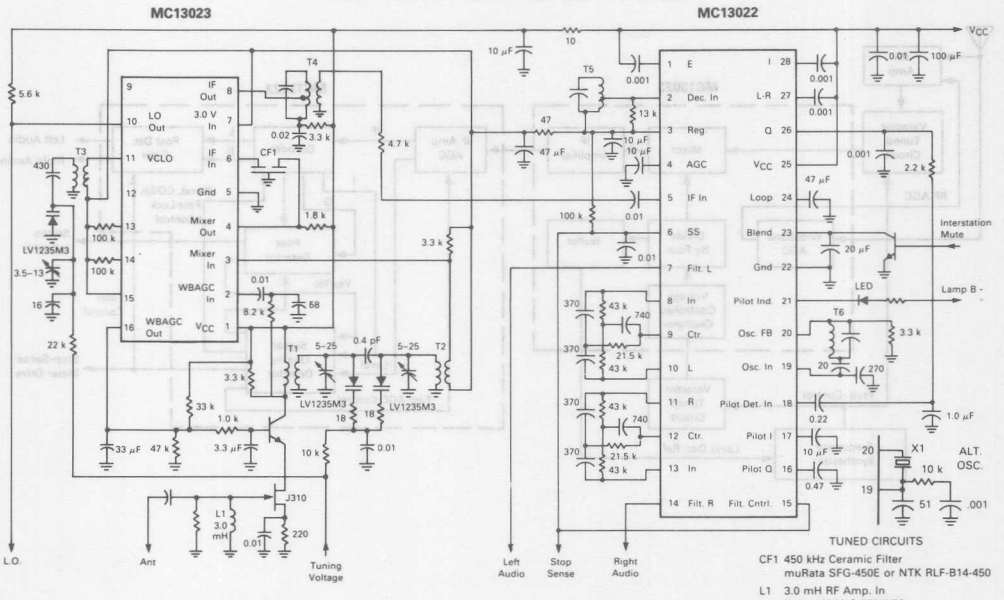
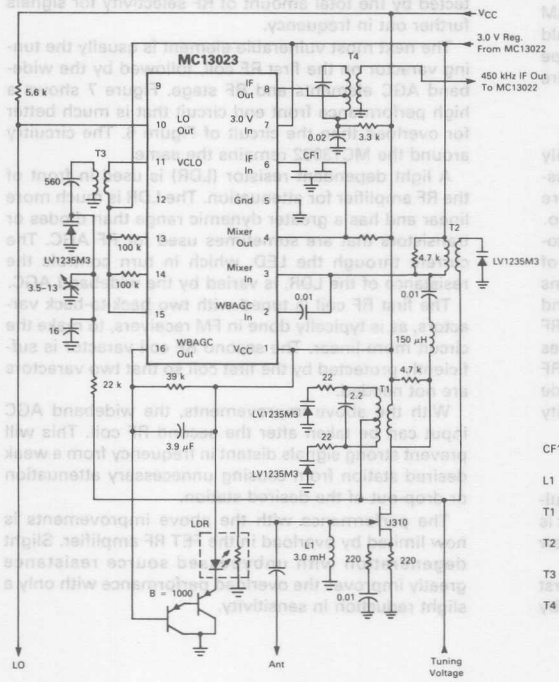


FIGURE 7 — HIGH PERFORMANCE ETR TUNER



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MOTOROLA

MC13024

Product Preview

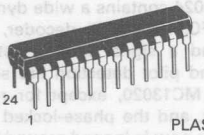
LOW VOLTAGE MOTOROLA C-QUAM® AM STEREO RECEIVER

LOW VOLTAGE MOTOROLA C-QUAM® AM STEREO RECEIVER

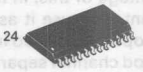
SILICON MONOLITHIC INTEGRATED CIRCUIT

The MC13024 is intended to serve the manually tuned portable and pocket radio mass market. This part includes all receiver and stereo decoding functions, from antenna to Left and Right audio outputs.

- Full Operation from 1.8 V to 8.0 Vdc Supply
- Low Power, Current Drain (typ) 5.0 mA
- Typical Distortion <1% at 90% L+R or 50% Single Channel
- Typical Channel Separation >25 dB
- Pilot Tone Detector
- Combined Tuning and Stereo Indicator
- "Blend On" Stereo Mode and Lamp Drive
- High Accuracy, Fast Locking VCLO
- Controlled Return to Monaural Under Adverse Conditions
- Minimized "Tweets and Birdies"
- Minimized Tuning Transients

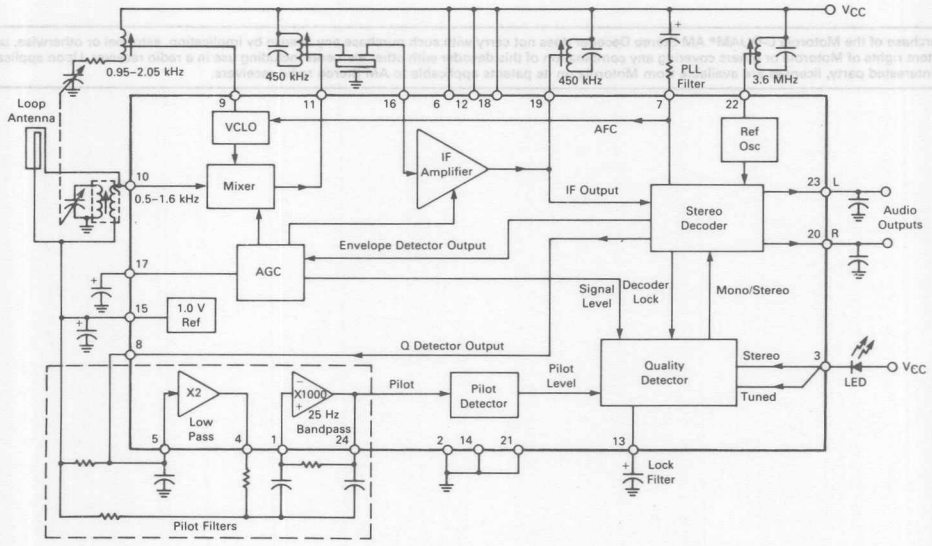


P SUFFIX
PLASTIC PACKAGE
CASE 724-03



DW SUFFIX
PLASTIC PACKAGE
CASE 751E-02
SO-24

FIGURE 1 — FUNCTIONAL BLOCK DIAGRAM



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This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

The MC13024 is a complete C-QUAM® AM stereo receiver, from the antenna to low level audio. All that is needed make a complete AM stereo radio is the addition of the appropriate audio output amplifier. The MC13024 is intended for use in most types of manually tuned receivers: pocket portables, "boom boxes," table radios, etc. It will operate from 1.8 Vdc to 8.0 Vdc and requires typically 5.0 mA (not including LED). This broad supply voltage tolerance and low power consumption makes it ideal for portables using as few as 2 battery cells. The radios which can be built using this part can be quite low in cost, while still benefiting from a high degree of functional sophistication.

FEATURES

The MC13024 contains a wide dynamic range mixer, IF, AGC, AFC, C-QUAM® decoder, stereo pilot tone detector, and a signal quality detector. The stereo decoding and pilot detection are similar to the well-established MC13020, except for reduced peripheral components, and the phase-locked loop used for the L-R detection now is looped around the entire receiver. In other words, the PLL controls the tuner local oscillator (VCLO) rather than a detector loop after the IF. The advantage of this, in manually tuned AM stereo, is significant, because it assures that the signal will always be properly centered in the IF bandpass, which is critical to good channel separation. This architecture also gives the radio an AFC tuning behavior which makes it easy to tune. The PLL has two "speeds," provided by current ratios of 50:1, which give fast lock and low distortion, respectively.

A signal quality detector circuit monitors lock condition, excess in-phase modulation due to interference, pilot presence and amplitude, and the movement of the tuning element by the user. A proper level of pilot must be present for several cycles before stereo mode will be enabled. When all conditions are correct, the transition from monaural to stereo is done gradually to prevent a transient "pop." Under aberrated conditions, the audio may either blend to mono or make an immediate change to mono, depending on the detected condition. The LED pin drives a dual purpose indicator: low current for PLL lock, and full current for stereo mode. Again, the switching is done "softly" to prevent transient loading of a weak battery.

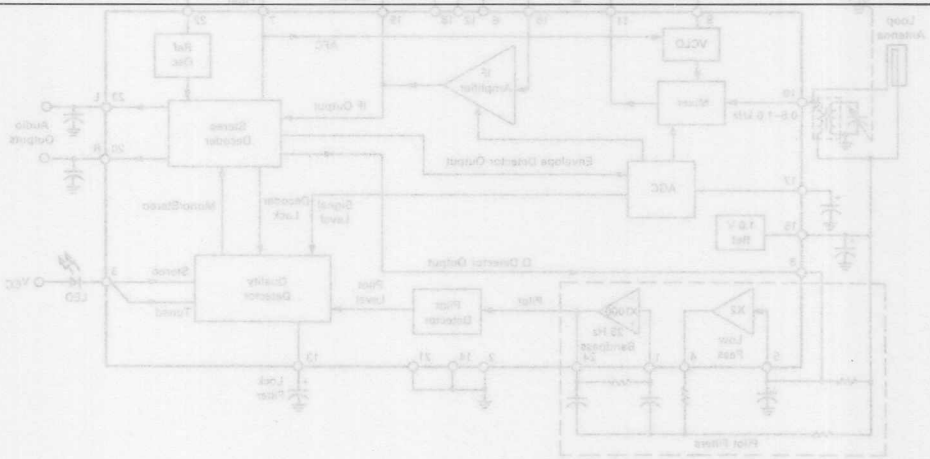
The IF gain and the mixer RF gain are each reduced, in turn, as signal strength increases, to optimize S/N and prevent overload. The receiver is capable of 20 dB S/N at 2.5 μV/50 ohm input. At weak signals, the reference oscillator and quadrature divider are shut off to minimize "tweets and birdies."

RADIO CONSTRUCTION

Layout is not much more critical than any high performance AM receiver. Care must be taken to provide a good ground plane and short leads on signal paths. Take special care to keep the reference oscillator components close to Pin 22 and protected from coupling from the pilot bandpass output, Pin 24. Also take care with the ever present threat of RF radiation from the audio output back into the antenna. This can be controlled by proper component location and good (close) RF bypass on the amplifier V_{CC} and good snubbers on the audio outputs. Keeping in mind that this is a phase-detecting receiver, it is important to mount coils securely and avoid movable wires in tuned circuits. A lot of individual preference will go into each implementation; the components shown here are only intended to provide a good working start.

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The purchase of the Motorola C-QUAM® AM Stereo Decoder does not carry with such purchase any license by implication, estoppel or otherwise, under any patent rights of Motorola or others covering any combination of this decoder with other elements including use in a radio receiver. Upon application by an interested party, licenses are available from Motorola on its patents applicable to AM Stereo radio receivers.



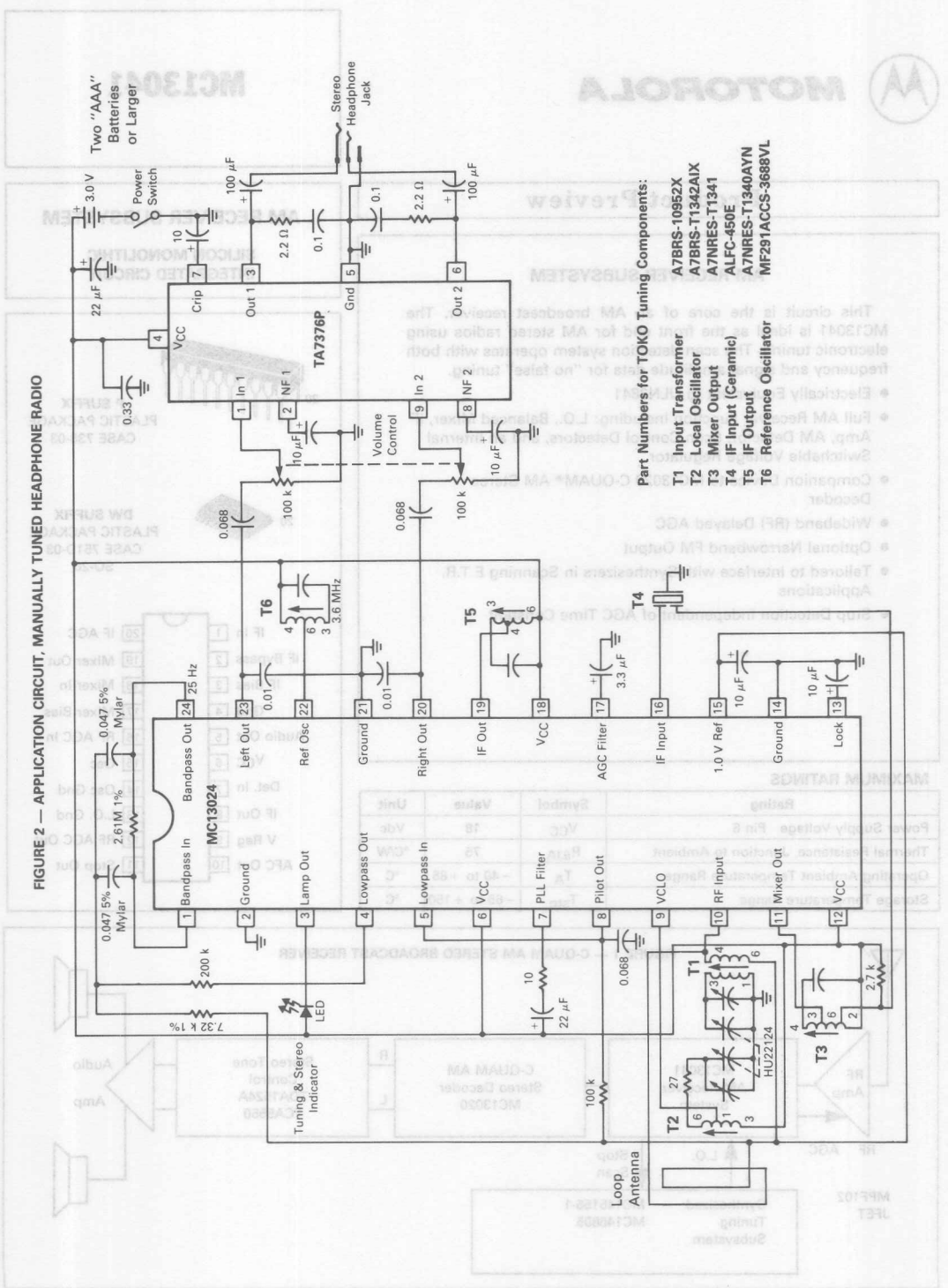


FIGURE 2 — APPLICATION CIRCUIT, MANUALLY TUNED HEADPHONE RADIO

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MOTOROLA

MC13041

Product Preview

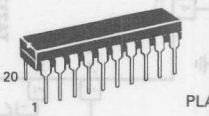
AM RECEIVER SUBSYSTEM

AM RECEIVER SUBSYSTEM

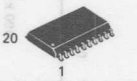
SILICON MONOLITHIC
INTEGRATED CIRCUIT

This circuit is the core of an AM broadcast receiver. The MC13041 is ideal as the front end for AM stereo radios using electronic tuning. The scan detection system operates with both frequency and signal amplitude data for "no false" tuning.

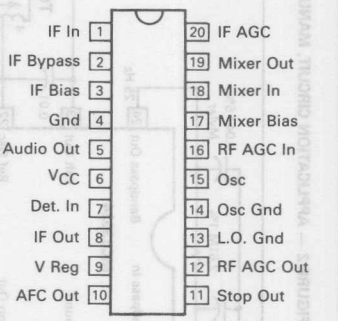
- Electrically Equivalent to ULN3841
- Full AM Receiver Function Including: L.O., Balanced Mixer, IF Amp, AM Detector, Scan Control Detectors, and an Internal Switchable Voltage Regulator
- Companion Device to MC13020 C-QUAM® AM Stereo Decoder
- Wideband (RF) Delayed AGC
- Optional Narrowband FM Output
- Tailored to Interface with Synthesizers in Scanning E.T.R. Applications
- Stop Detection Independent of AGC Time Constant



P SUFFIX
PLASTIC PACKAGE
CASE 738-03



DW SUFFIX
PLASTIC PACKAGE
CASE 751D-03
SO-20

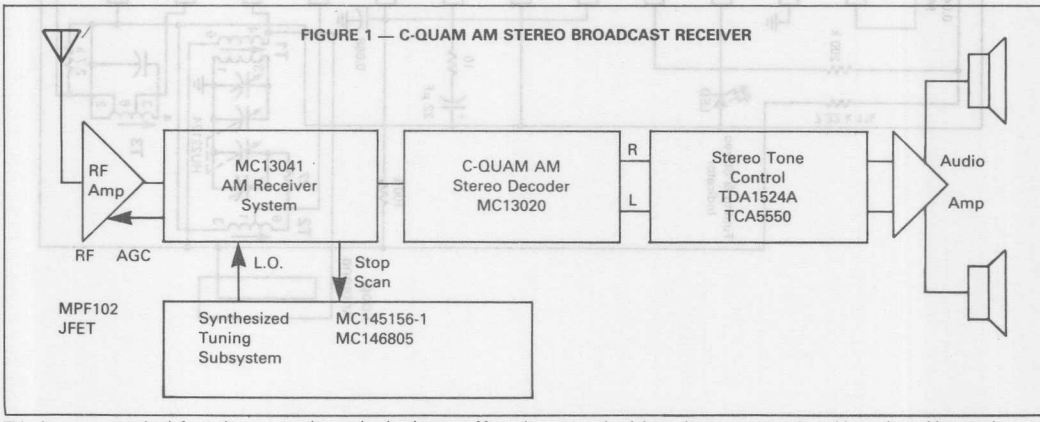


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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage Pin 6	V_{CC}	18	Vdc
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	°C/W
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

FIGURE 1 — C-QUAM AM STEREO BROADCAST RECEIVER



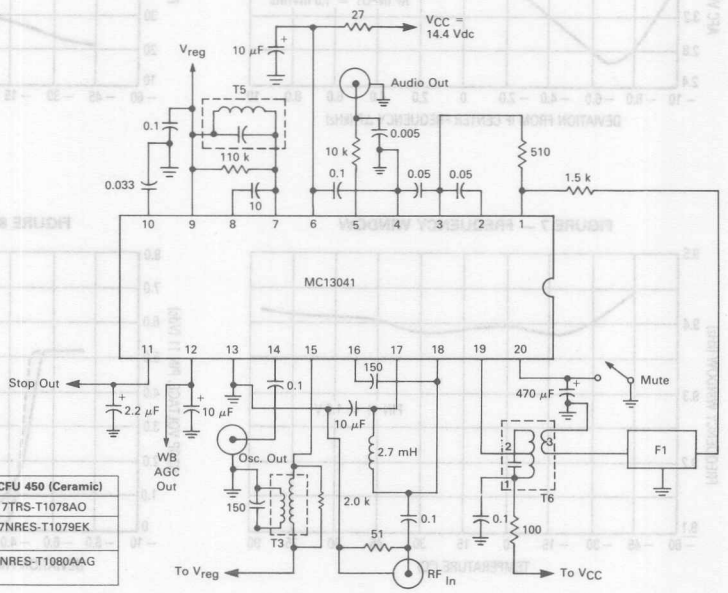
This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

ELECTRICAL CHARACTERISTICS (V_{CC} = 14.4 Vdc, T_A = +25°C, RF Input Frequency = 1.0 MHz, I_F = 450 kHz, FMOD = 1.0 kHz, Modulation = 30%, Test Circuit of Figure 2, unless otherwise noted.)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage Range	V_{CC}		—	6.5–16.5	—	Vdc
Supply Current	I_{CC}	No Input Signal	—	25	33	mAdc
RF Sensitivity	RF_{In} to Pin 18	Pin 5 Audio Out Equals 50 mV	—	2.6	10	μVrms
Usable Sensitivity	RF_{In} to Pin 18	At Pin 5 $\frac{S+N}{N}$ = 20 dB	—	5.6	10	μVrms
Recovered Audio	Audio Out at Pin 5	1.0 mV RF_{In} at Pin 18	173	240	346	mVrms
Total Harmonic Distortion	THD at Pin 5	1.0 mV RF_{In} 80% modulation at Pin 5	—	0.5	3.0	%
Oscillator Output	V_{OSC}	RF_{Out} at Pin 14	—	330	—	mVrms
Stop Voltage	V_{STOP} Pin 11	No Input at Pin 18	4.3	5.2	—	Vdc
Stop Sensitivity	$V_{STP\ SEN}$ Pin 18 RF	Pin 11 Equals 1.5 Vdc	27	40	80	μVrms
Stop Bandwidth	$V_{STOP\ BW}$	Pin 18 = 1.0 mVrms Pin 11 = 1.5 Vdc	—	±4.7	—	kHz
RF AGC	V_{AGC} Pin 12	RF Pin 16 = 0 mVrms	—	—	0.15	Vdc
		RF Pin 16 = 20 mVrms	0.8	—	—	
Overload	THD at Pin 5 Audio Out	RF_{In} at Pin 18 = 25 mVrms Modulation = 80%	—	1.2	—	%
AGC Figure of Merit	Pin 5 Audio Drop to 10 dB Below Ref	RF_{In} at Pin 18 dB Below 30 mV	—	75	—	dB

NOTE: Pin 9 voltage regulator output for local oscillator only.

FIGURE 2 — TEST CIRCUIT



F1	Filter		muRata CFU 450 (Ceramic)
T3	Osc.	5:1	Toko 7TRS-T1078AO
T6	Mixer	N1:N2 = 2.63 N1:N3 = 11.7	Toko 7NRES-T1079EK
T5	Detector	Q = 100 Ct = 100 pF	Toko 7NRES-T1080AAG

TAKEN IN TEST CIRCUIT OF FIGURE 2

FIGURE 3 — RECOVERED AUDIO

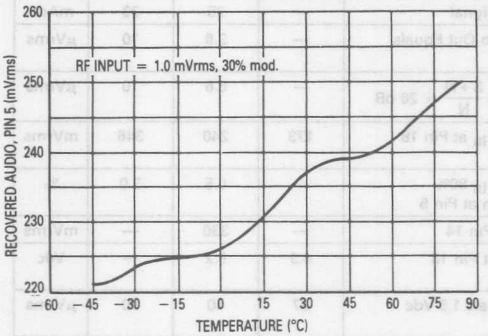


FIGURE 4 — RF INPUT AT AUDIO OUTPUT = 50 mVrms

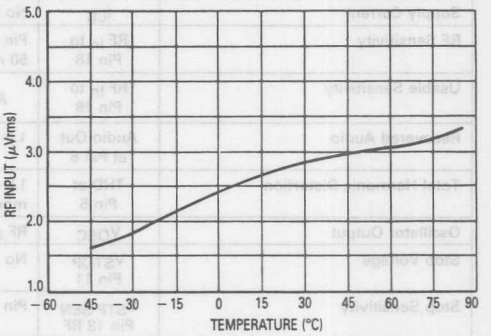


FIGURE 5 — AM AFC

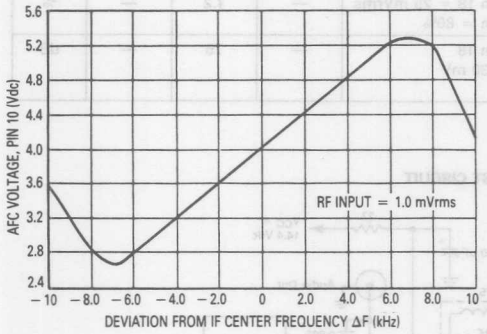


FIGURE 6 — STOP LEVEL

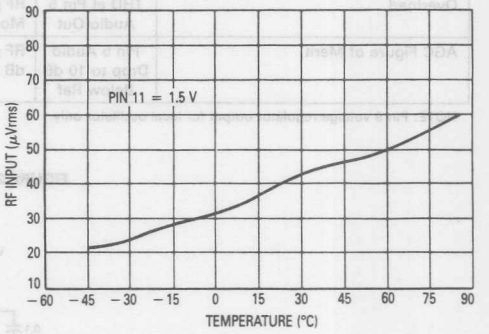


FIGURE 7 — FREQUENCY WINDOW

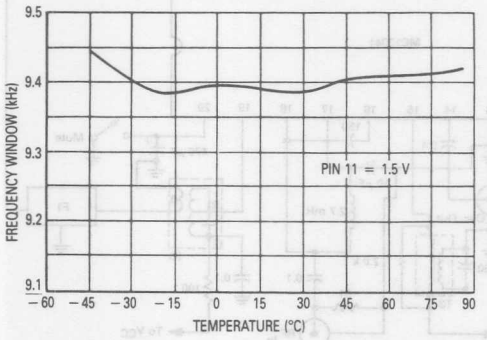
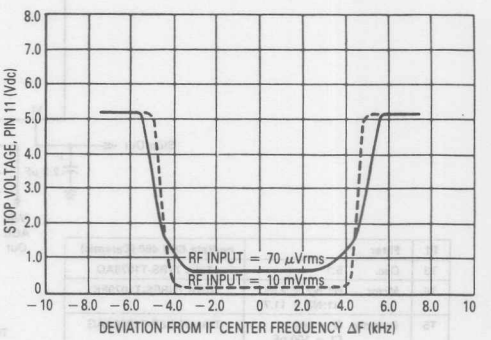
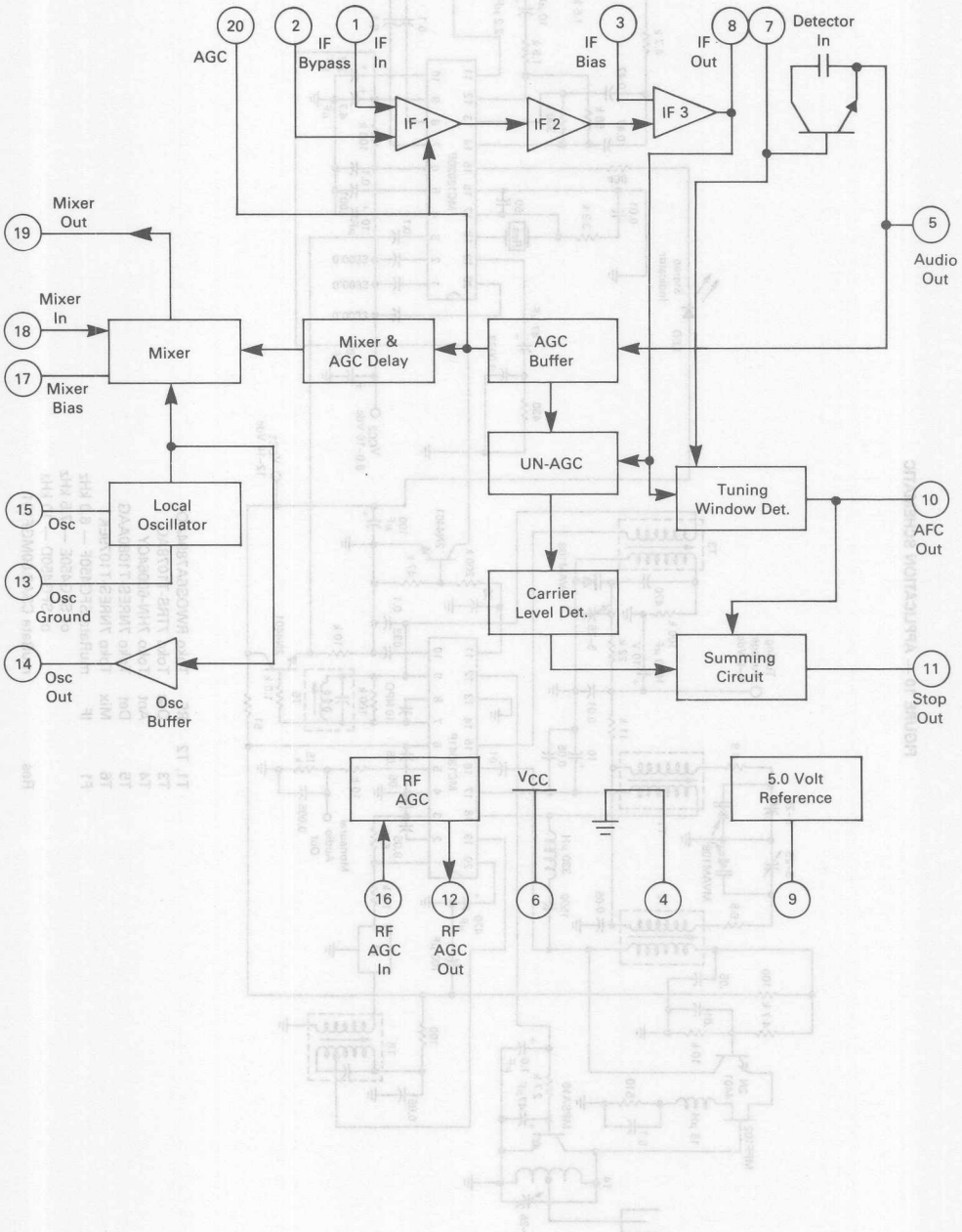


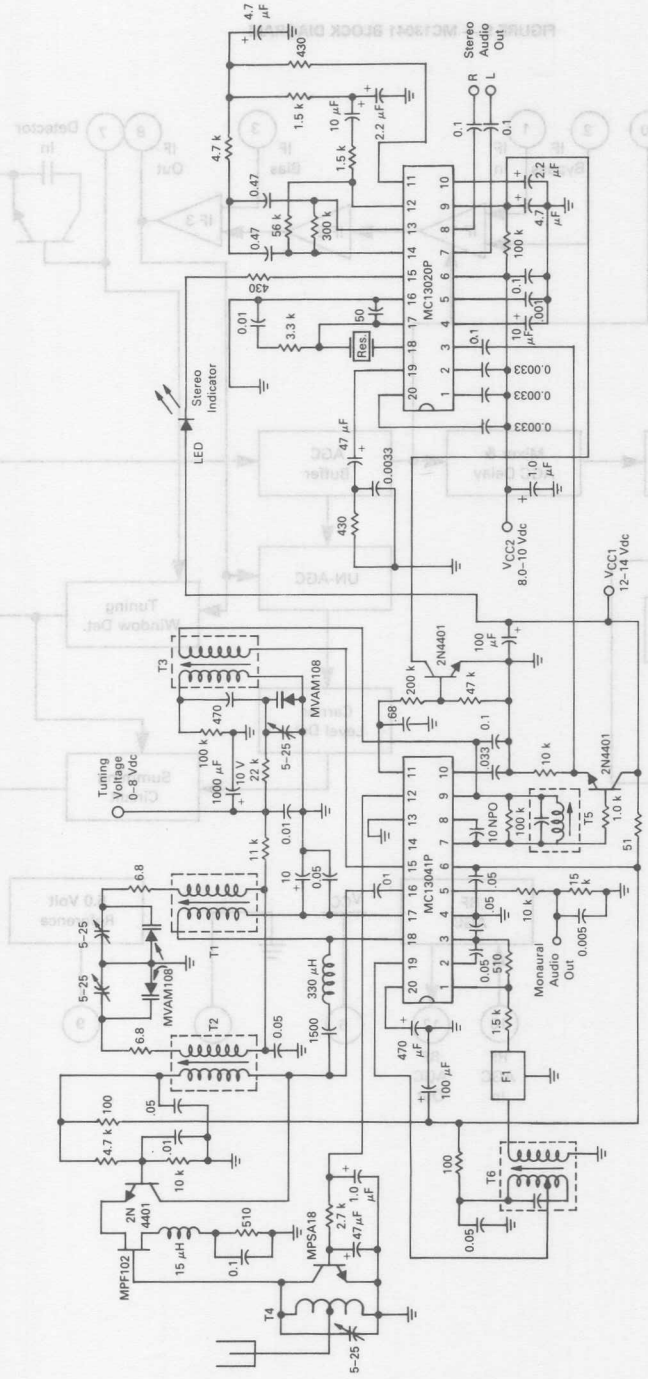
FIGURE 8 — FREQUENCY WINDOW



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FIGURE 9 — MC13041 BLOCK DIAGRAM





T1, T2 RF Toko RWOS6A7894AO
T3 Osc Toko 7TRS-T1078AO
T4 Ant Toko 7HN-60064CY
T5 Det Toko 7NRES-T1080AAG
T6 Mix Toko 7NRES-T1079EK
F1 IF muRata SFG450F — 6.0 kHz
or SFG450E — 7.5 kHz
or SFG450D — 10 kHz
Res muRata CSA3.60MGF101

FIGURE 10 — APPLICATION SCHEMATIC

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FIGURE 11 — RECEIVER GAIN-REDUCTION VOLTAGES

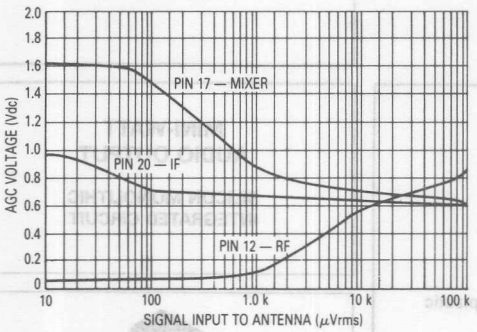
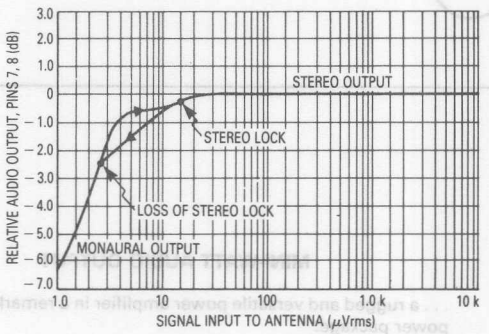


FIGURE 12 — RECEIVER RECOVERED AUDIO



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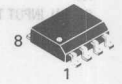
MINI-WATT AUDIO OUTPUT

. . . a rugged and versatile power amplifier in a remarkable plastic power package.

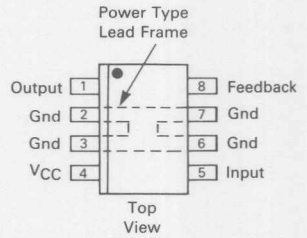
- Supply Voltages from 6–35 Vdc
- 2.0 Watts Output @ 70°C Ambient on PC Board with Good Copper Ground Plane
- Self Protecting Thermal Shutdown
- Easy to Apply, Few Components
- Gain Externally Determined
- Output is Independent of Supply Voltage Over a Wide Range

MINI-WATT AUDIO OUTPUT

SILICON MONOLITHIC INTEGRATED CIRCUIT



D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SOP-8



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FIGURE 1 — TYPICAL APPLICATION

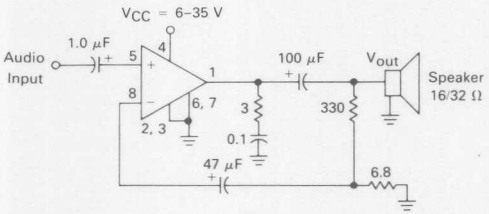
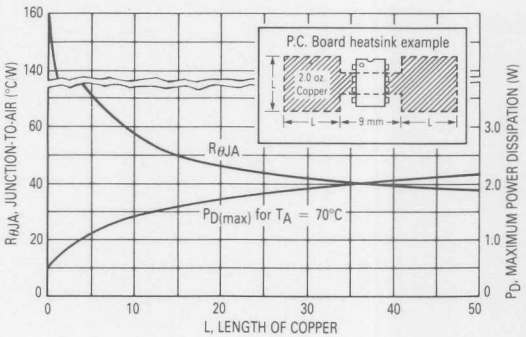


FIGURE 2 — THERMAL RESISTANCE AND MAXIMUM POWER DISSIPATION versus P.C. BOARD COPPER



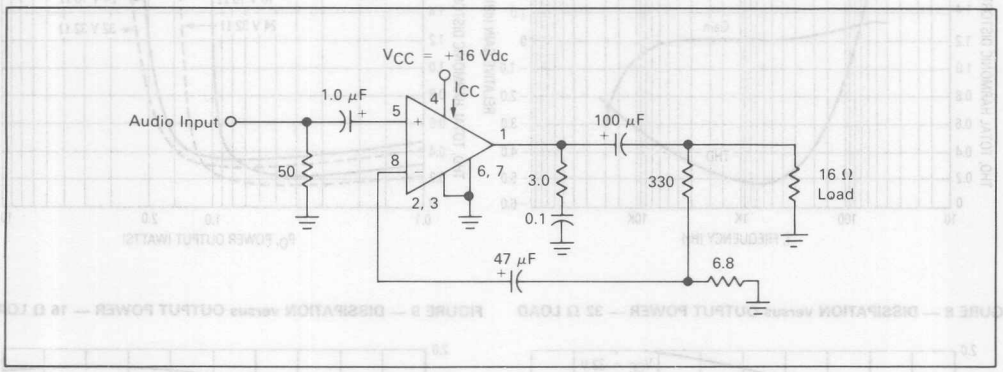
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	35	V
Audio Input, Pin 5		1.0	V_{p-p}
Thermal Resistance, Junction to Air	$R_{\theta JA}$	160	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	25	°C/W
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS — AUDIO SECTION (T_A = 25°C, Circuit of Figure 3 unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Current, No Signal	I_{CC}	—	13	—	mAdc
Gain	A_o	—	50	—	V/V
Distortion at 62.5 mW Output, 1.0 kHz	THD	—	0.2	1.0	%
Distortion at 900 mW Output, 1.0 kHz	THD	—	0.5	3.0	%
Quiescent Output Voltage, No Signal	$V_{Pin\ 1}$	—	8.4	—	Vdc
Input Bias	$V_{Pin\ 5}$, $V_{Pin\ 8}$	—	0.7	—	Vdc
Input Resistance	R_{in}, Pin 5	—	28	—	kΩ
Output Noise (50 Hz–15 kHz) Input 50 Ω	V_{out}	—	0.5	4.0	mVrms

FIGURE 3 — TEST CIRCUIT



DESCRIPTION

The MC13060 is a quasi-complementary audio power amplifier, mounted in the SOP 8 (power SOIC package). It is well suited to a variety of 1.0 and 2.0 watt applications in radio, TV, intercoms, and other speaker driving tasks. It requires the usual external components for high frequency stability and for gain adjustment.

The output signal voltage and the power supply drain current are very linearly related, as shown in Figure 5. Both are quite constant over wide variation of the power supply voltage (above min V_{CC} for clipping, of course). The amplifier can best be described as a voltage source with about 1.0 A_{p-p} capability. On a good heat sink, it can deliver over 2.0 watts at 70°C ambient.

The MC13060 will automatically go into shut-down at a die temperature of about 150°C, effectively protecting itself, even on fairly stiff power supplies. This eliminates the need for decoupling the power supply, which degrades performance and requires extra components.

Input Pins 5 and 8 are internally biased at 0.7 Vdc and should not be driven below ground.

ALL CURVES TAKEN IN THE TEST CIRCUIT OF FIGURE 3 UNLESS OTHERWISE NOTED

FIGURE 4 — QUIESCENT SUPPLY CURRENT AND OUTPUT VOLTAGE versus SUPPLY VOLTAGE

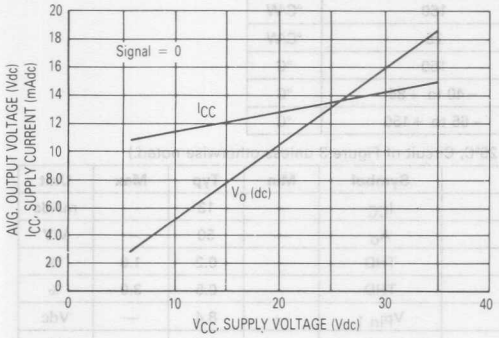


FIGURE 5 — SUPPLY CURRENT versus OUTPUT

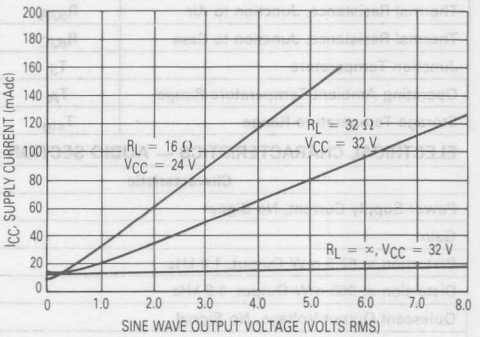


FIGURE 6 — DISTORTION AND GAIN versus FREQUENCY

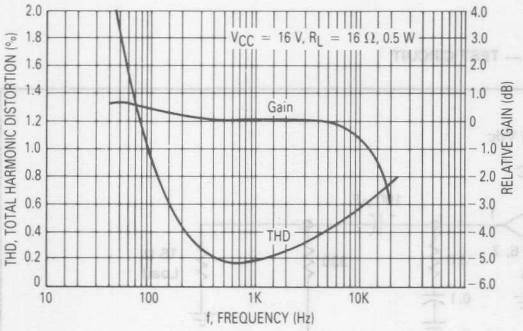


FIGURE 7 — DISTORTION versus POWER OUTPUT

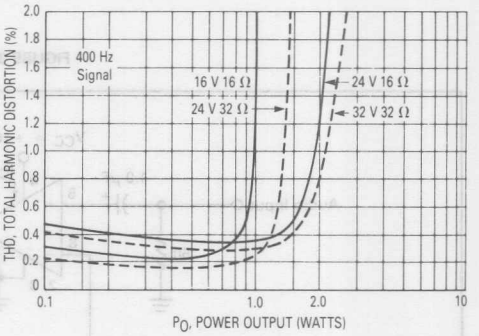


FIGURE 8 — DISSIPATION versus OUTPUT POWER — 32 Ω LOAD

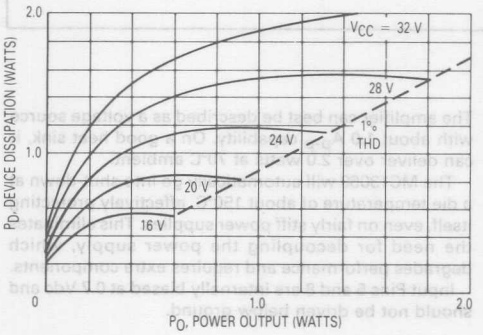
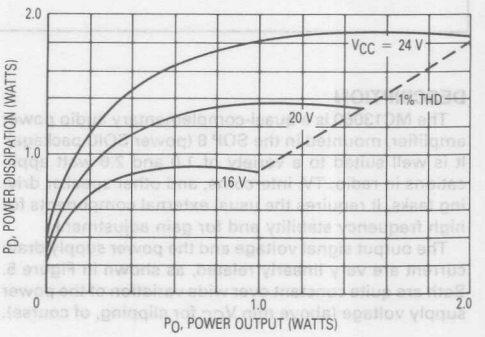
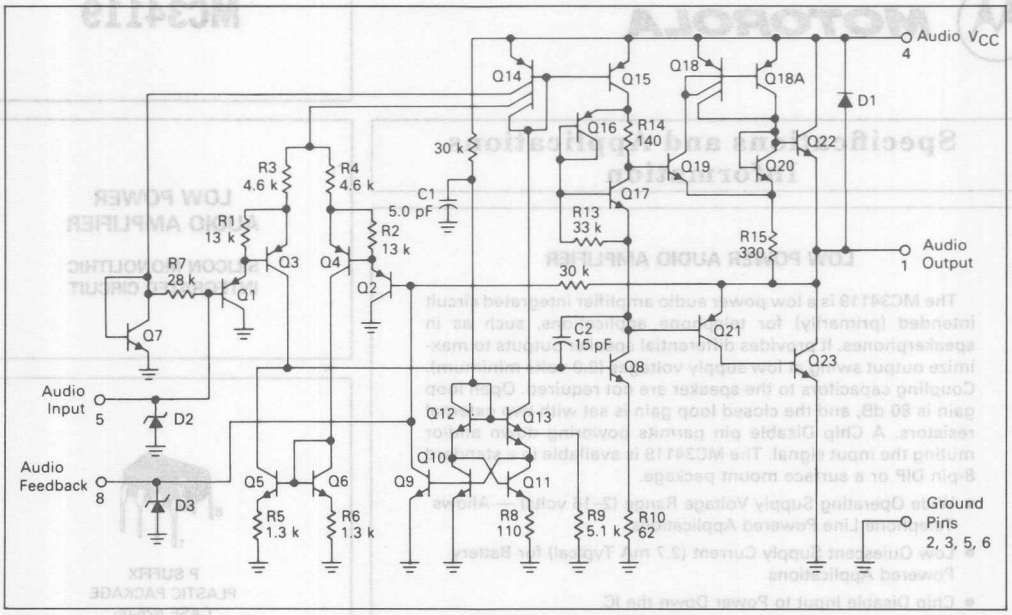


FIGURE 9 — DISSIPATION versus OUTPUT POWER — 16 Ω LOAD



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FIGURE 10 — INTERNAL SCHEMATIC



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Specifications and Applications Information

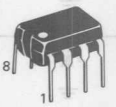
LOW POWER AUDIO AMPLIFIER

The MC34119 is a low power audio amplifier integrated circuit intended (primarily) for telephone applications, such as in speakerphones. It provides differential speaker outputs to maximize output swing at low supply voltages (2.0 volts minimum). Coupling capacitors to the speaker are not required. Open loop gain is 80 dB, and the closed loop gain is set with two external resistors. A Chip Disable pin permits powering down and/or muting the input signal. The MC34119 is available in a standard 8-pin DIP or a surface mount package.

- Wide Operating Supply Voltage Range (2–16 volts) — Allows Telephone Line Powered Applications
- Low Quiescent Supply Current (2.7 mA Typical) for Battery Powered Applications
- Chip Disable Input to Power Down the IC
- Low Power-Down Quiescent Current (65 μA Typical)
- Drives a Wide Range of Speaker Loads (8 Ohms and Up)
- Output Power Exceeds 250 mW with 32 Ohm Speaker
- Low Total Harmonic Distortion (0.5% Typical)
- Gain Adjustable from <0 dB to >46 dB for Voice Band
- Requires Few External Components

LOW POWER AUDIO AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

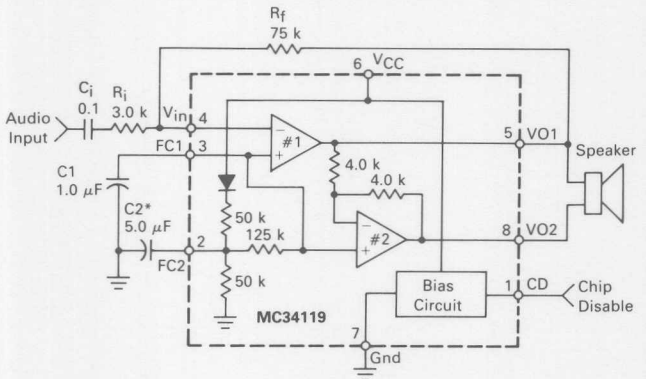


P SUFFIX
PLASTIC PACKAGE
CASE 626-05



D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SO-8

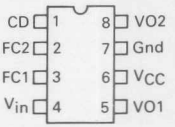
BLOCK DIAGRAM AND TYPICAL APPLICATION CIRCUIT



* = Optional

Differential Gain = $2 \times \frac{R_f}{R_i}$

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC34119P	−20°C to +70°C	Plastic DIP
MC34119D		Plastic SOIC

ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Units
Supply Voltage	−1.0 to +18	Vdc
Maximum Output Current at VO1, VO2	±250	mA
Maximum Voltage @ V_{in}, FC1, FC2, CD	−1.0, V_{CC} +1.0	Vdc
Applied Output Voltage to VO1, VO2 when disabled	−1.0, V_{CC} +1.0	Vdc
Junction Temperature	−55, +140	°C

Devices should not be operated at these values. The "Recommended Operating Limits" provide for actual device operation.

RECOMMENDED OPERATING LIMITS

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	V_{CC}	+2.0	—	+16	Vdc
Load Impedance	R_L	8.0	—	100	Ω
Peak Load Current	I_L	—	—	±200	mA
Differential Gain (5.0 kHz bandwidth)	AVD	0	—	46	dB
Voltage @ CD (Pin 1)	VCD	0	—	V_{CC}	Vdc
Ambient Temperature	T_A	−20	—	+70	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Characteristics	Symbol	Min	Typ	Max	Units
AMPLIFIERS (AC CHARACTERISTICS)					
AC Input Resistance (@ V_{in})	r_i	—	>30	—	MΩ
Open Loop Gain (Amplifier #1, f < 100 Hz)	A_{VOL1}	80	—	—	dB
Closed Loop Gain (Amplifier #2) (V_{CC} = 6.0 V, f = 1.0 kHz, R_L = 32 Ω)	A_{V2}	−0.35	0	+0.35	dB
Gain Bandwidth Product	GBW	—	1.5	—	MHz
Output Power, V_{CC} = 3.0 V, R_L = 16 Ω, THD ≤ 10% V_{CC} = 6.0 V, R_L = 32 Ω, THD ≤ 10% V_{CC} = 12 V, R_L = 100 Ω, THD ≤ 10%	P_{out3} P_{out6} P_{out12}	55 250 400	— — —	— — —	mW
Total Harmonic Distortion (f = 1.0 kHz) (V_{CC} = 6.0 V, R_L = 32 Ω, P_{out} = 125 mW) (V_{CC} ≥ 3.0 V, R_L = 8.0 Ω, P_{out} = 20 mW) (V_{CC} ≥ 12 V, R_L = 32 Ω, P_{out} = 200 mW)	THD	— — —	0.5 0.5 0.6	1.0 — —	%
Power Supply Rejection (V_{CC} = 6.0 V, ΔV_{CC} = 3.0 V) (C1 = ∞, C2 = 0.01 μF) (C1 = 0.1 μF, C2 = 0, f = 1.0 kHz) (C1 = 1.0 μF, C2 = 5.0 μF, f = 1.0 kHz)	PSRR	50 — —	— 12 52	— — —	dB
Muting (V_{CC} = 6.0 V, 1.0 kHz ≤ f ≤ 20 kHz, CD = 2.0 V)	GMT	—	>70	—	dB
AMPLIFIERS (DC CHARACTERISTICS)					
Output DC Level @ VO1, VO2, V_{CC} = 3.0 V, R_L = 16 Ω (R_f = 75 k) V_{CC} = 6.0 V V_{CC} = 12 V	VO(3) VO(6) VO(12)	1.0 — —	1.15 2.65 5.65	1.25 — —	Vdc
Output High Level (I_{out} = −75 mA, 2.0 V ≤ V_{CC} ≤ 16 V)	V_{OH}	—	V_{CC} − 1.0	—	Vdc
Output Low Level (I_{out} = 75 mA, 2.0 V ≤ V_{CC} ≤ 16 V)	V_{OL}	—	0.16	—	Vdc
Output DC Offset Voltage (VO1–VO2) (V_{CC} = 6.0 V, R_f = 75 kΩ, R_L = 32 Ω)	ΔV_O	−30	0	+30	mV
Input Bias Current @ V_{in} (V_{CC} = 6.0 V)	I_{IB}	—	−100	−200	nA
Equivalent Resistance @ FC1 (V_{CC} = 6.0 V)	R_{FC1}	100	150	220	kΩ
Equivalent Resistance @ FC2 (V_{CC} = 6.0 V)	R_{FC2}	18	25	40	kΩ
CHIP DISABLE (Pin 1)					
Input Voltage — Low	V_{IL}	—	—	0.8	Vdc
Input Voltage — High	V_{IH}	2.0	—	—	Vdc
Input Resistance (V_{CC} = V_{CD} = 16 V)	R_{CD}	50	90	175	kΩ
POWER SUPPLY					
Power Supply Current (V_{CC} = 3.0 V, R_L = ∞, CD = 0.8 V) (V_{CC} = 16 V, R_L = ∞, CD = 0.8 V) (V_{CC} = 3.0 V, R_L = ∞, CD = 2.0 V)	I_{CC3} I_{CC16} I_{CCD}	— — —	2.7 3.3 65	4.0 5.0 100	mA μA

Note: Currents into a pin are positive, currents out of a pin are negative.

9

PIN DESCRIPTION

Symbol	Pin	Description
CD	1	Chip Disable — Digital input. A Logic "0" (<0.8 V) sets normal operation. A Logic "1" (≥2.0 V) sets the power down mode. Input impedance is nominally 90 kΩ.
FC2	2	A capacitor at this pin increases power supply rejection, and affects turn-on time. This pin can be left open if the capacitor at FC1 is sufficient.
FC1	3	Analog Ground for the amplifiers. A 1.0 μF capacitor at this pin (with a 5.0 μF capacitor at Pin 2) provides (typically) 52 dB of power supply rejection. Turn-on time of the circuit is affected by the capacitor on this pin. This pin can be used as an alternate input.
V_{in}	4	Amplifier input. The input capacitor and resistor set low frequency rolloff and input impedance. The feedback resistor is connected to this pin and VO1.
VO1	5	Amplifier Output #1. The dc level is ≈ (V_{CC} − 0.7 V)/2.
V_{CC}	6	DC supply voltage (+2.0 to +16 volts) is applied to this pin.
GND	7	Ground pin for the entire circuit.
VO2	8	Amplifier Output #2. This signal is equal in amplitude, but 180° out of phase with that at VO1. The dc level is ≈ (V_{CC} − 0.7 V)/2.

TYPICAL TEMPERATURE PERFORMANCE (−20° < T_A < +70°C)

Function	Typical Change	Units
Input Bias Current (@ V_{in})	±40	pA/°C
Total Harmonic Distortion (V_{CC} = 6.0 V, R_L = 32 Ω, P_{out} = 125 mW, f = 1.0 kHz)	+0.003	%/°C
Power Supply Current (V_{CC} = 3.0 V, R_L = ∞, CD = 0 V)	−2.5	μA/°C
(V_{CC} = 3.0 V, R_L = ∞, CD = 2.0 V)	−0.03	

DESIGN GUIDELINES

GENERAL

The MC34119 is a low power audio amplifier capable of low voltage operation (V_{CC} = 2.0 V minimum) such as that encountered in line-powered speakerphones. The circuit provides a differential output (VO1–VO2) to the speaker to maximize the available voltage swing at low voltages. The differential gain is set by two external resistors. Pins FC1 and FC2 allow controlling the amount of power supply and noise rejection, as well as providing alternate inputs to the amplifiers. The CD pin permits powering down the IC for muting purposes and to conserve power.

AMPLIFIERS

Referring to the block diagram, the internal configuration consists of two identical operational amplifiers. Amplifier #1 has an open loop gain of ≥80 dB (at f ≤ 100 Hz), and the closed loop gain is set by external resistors R_f and R_i. The amplifier is unity gain stable, and has a unity gain frequency of approximately 1.5 MHz. In order to adequately cover the telephone voice band (300–3400 Hz), a maximum closed loop gain of 46 dB is recommended. Amplifier #2 is internally set to a gain of −1.0 (0 dB).

The outputs of both amplifiers are capable of sourcing and sinking a peak current of 200 mA. The outputs can typically swing to within ≈0.4 volts above ground, and to within ≈1.3 volts below V_{CC}, at the maximum current. See Figures 18 and 19 for V_{OH} and V_{OL} curves.

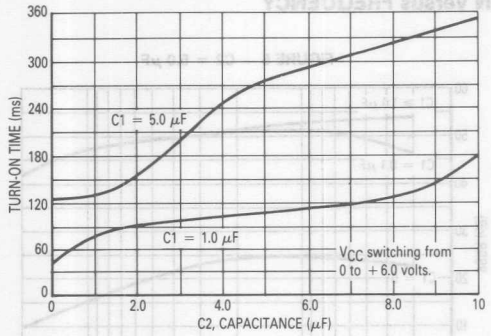
The output dc offset voltage (VO1–VO2) is primarily a function of the feedback resistor (R_f), and secondarily due to the amplifiers' input offset voltages. The input offset voltage of the two amplifiers will generally be similar for a particular IC, and therefore nearly cancel each other at the outputs. Amplifier #1's bias current, however, flows out of V_{in} (Pin 4) and through R_f, forcing VO1 to shift negative by an amount equal to [R_f x I_{IB}]. VO2 is shifted positive an equal amount. The output offset voltage specified in the Electrical Characteristics is measured with the feedback resistor shown in the Typical Application Circuit, and therefore takes into account the bias current as well as internal offset voltages of the amplifiers. The bias current is constant with respect to V_{CC}.

FC1 and FC2

Power supply rejection is provided by the capacitors (C1 and C2 in the Typical Application Circuit) at FC1 and FC2. C2 is somewhat dominant at low frequencies, while C1 is dominant at high frequencies, as shown in the graphs of Figures 4–7. The required values of C1 and C2 depend on the conditions of each application. A line powered speakerphone, for example, will require more filtering than a circuit powered by a well regulated power supply. The amount of rejection is a function of the capacitors, and the equivalent impedance looking into FC1 and FC2 (listed in the Electrical Characteristics as R_{FC1} and R_{FC2}).

In addition to providing filtering, C1 and C2 also affect the turn-on time of the circuit at power-up, since the two capacitors must charge up through the internal 50 k and 125 kΩ resistors. The graph of Figure 1 indicates the turn-on time upon application of V_{CC} of +6.0 volts. The turn-on time is ≈60% longer for V_{CC} = 3.0 volts, and ≈20% less for V_{CC} = 9.0 volts. Turn-off time is <10 μs upon removal of V_{CC}.

FIGURE 1 — TURN-ON TIME versus C1, C2 AT POWER-ON



CHIP DISABLE

The Chip Disable (Pin 1) can be used to power down the IC to conserve power, or for muting, or both. When at a Logic "0" (0 to 0.8 volts), the MC34119 is enabled for normal operation. When Pin 1 is at a Logic "1" (2.0 to V_{CC} volts), the IC is disabled. If Pin 1 is open, that is equivalent to a Logic "0," although good design practice dictates that an input should never be left open. Input impedance at Pin 1 is a nominal 90 kΩ. The power supply current (when disabled) is shown in Figure 15.

Muting, defined as the change in differential gain from normal operation to muted operation, is in excess of 70 dB. The turn-off time of the audio output, from the application of the CD signal, is <2.0 μs, and turn on-time is 12–15 ms. Both times are independent of C1, C2, and V_{CC}.

When the MC34119 is disabled, the voltages at FC1 and FC2 do not change as they are powered from V_{CC}. The outputs, VO1 and VO2, change to a high impedance condition, removing the signal from the speaker. If signals from other sources are to be applied to the outputs (while disabled), they must be within the range of V_{CC} and Ground.

POWER DISSIPATION

Figures 8–10 indicate the device dissipation (within the IC) for various combinations of V_{CC}, R_L, and load power. The maximum power which can safely be dissipated within the MC34119 is found from the following equation:

$$P_D = (140°C - T_A)/\theta_{JA}$$

where T_A is the ambient temperature;
and θ_{JA} is the package thermal resistance (100°C/W for the standard DIP package, and 180°C/W for the surface mount package.)

The power dissipated within the MC34119, in a given application, is found from the following equation:

$$P_D = (V_{CC} \times I_{CC}) + (I_{RMS} \times V_{CC}) - (R_L \times I_{RMS}^2)$$

where I_{CC} is obtained from Figure 15;
and I_{RMS} is the RMS current at the load;
and R_L is the load resistance.

Figures 8–10, along with Figures 11–13 (distortion curves), and a peak working load current of ±200 mA, define the operating range for the MC34119. The operating range is further defined in terms of allowable load power in Figure 14 for loads of 8.0 Ω, 16 Ω, and 32 Ω. The left (ascending) portion of each of the three curves is defined by the power level at which 10% distortion occurs. The center flat portion of each curve is defined by the maximum output current capability of the MC34119. The right (descending) portion of each curve is defined by the maximum internal power dissipation of the IC at 25°C. At higher ambient temperatures, the maximum load power must be reduced according to the above equations. Operating the device beyond the current and junction temperature limits will degrade long term reliability.

LAYOUT CONSIDERATIONS

Normally a snubber is not needed at the output of the MC34119, unlike many other audio amplifiers. However, the PC board layout, stray capacitances, and the manner in which the speaker wires are configured, may dictate otherwise. Generally the speaker wires should be twisted tightly, and be not more than a few inches in length.

9

TYPICAL CHARACTERISTICS

FIGURE 2 — AMPLIFIER #1 OPEN LOOP GAIN AND PHASE

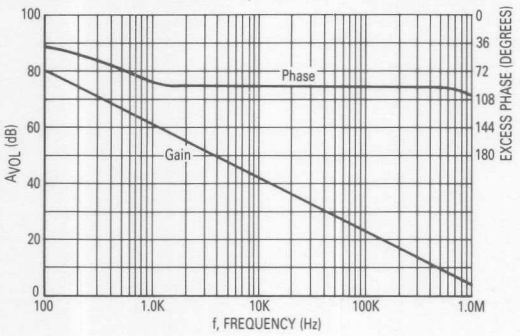


FIGURE 3 — DIFFERENTIAL GAIN versus FREQUENCY

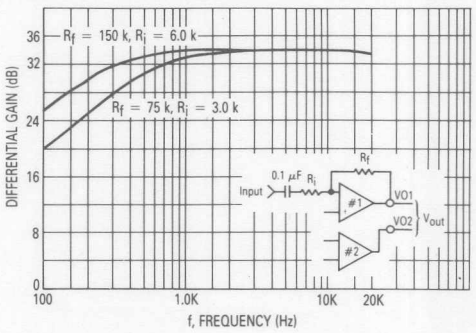


FIGURE 4 — C2 = 10 μF

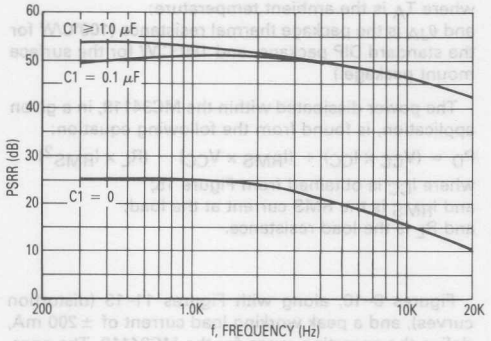


FIGURE 5 — C2 = 5.0 μF

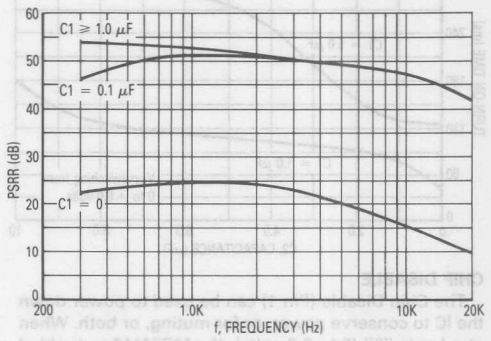


FIGURE 6 — C2 = 1.0 μF

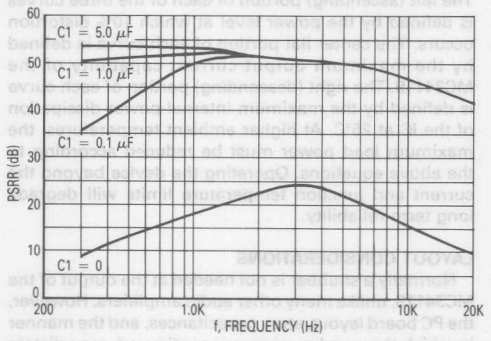
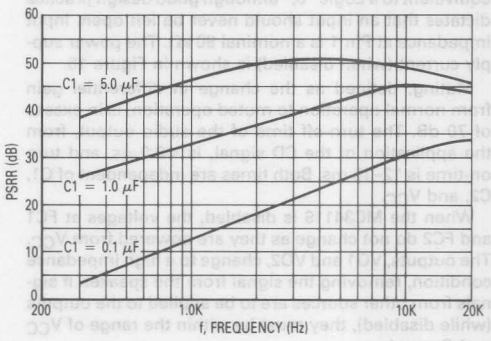


FIGURE 7 — C2 = 0



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FIGURE 8 — DEVICE DISSIPATION
8.0 Ω LOAD

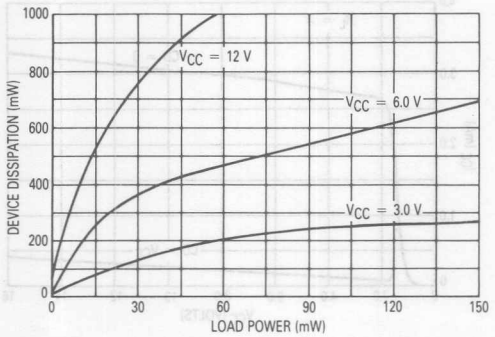


FIGURE 9 — DEVICE DISSIPATION
16 Ω LOAD

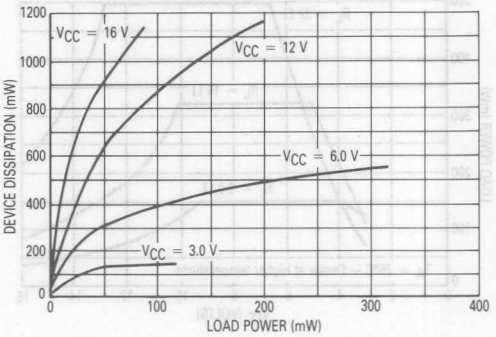


FIGURE 10 — DEVICE DISSIPATION
32 Ω LOAD

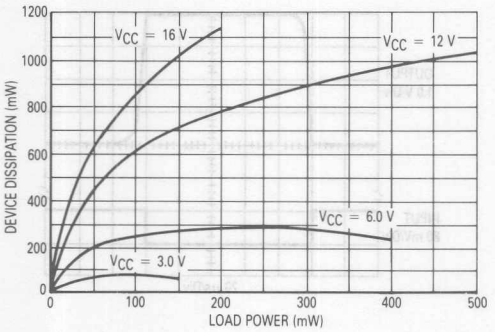


FIGURE 11 — DISTORTION versus POWER
f = 1.0 kHz, AVD = 34 dB

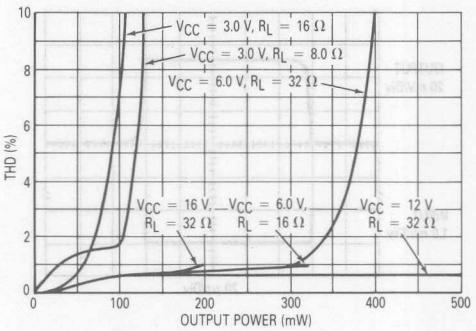


FIGURE 12 — DISTORTION versus POWER
f = 3.0 kHz, AVD = 34 dB

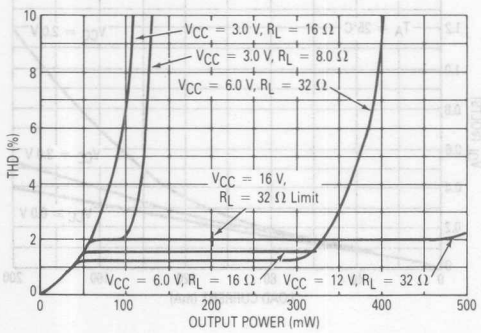
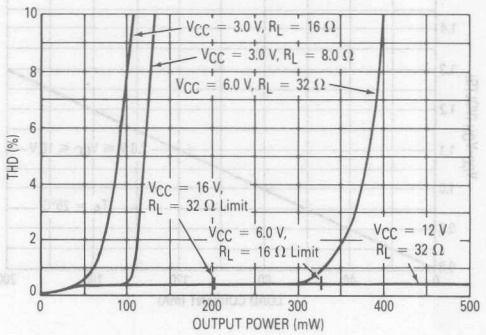


FIGURE 13 — DISTORTION versus POWER
f = 1, 3.0 kHz, AVD = 12 dB



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FIGURE 14 — MAXIMUM ALLOWABLE LOAD POWER

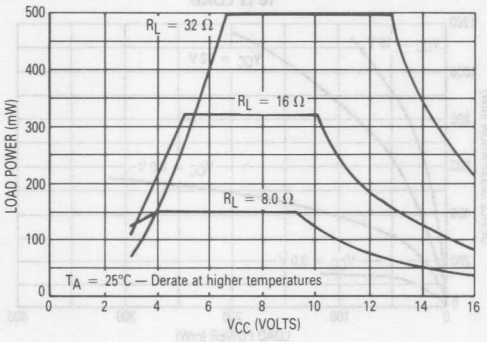


FIGURE 15 — POWER SUPPLY CURRENT

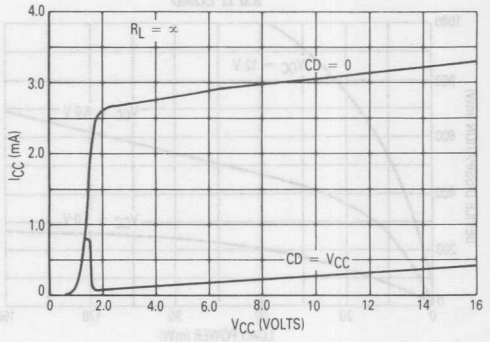


FIGURE 16 — SMALL SIGNAL RESPONSE

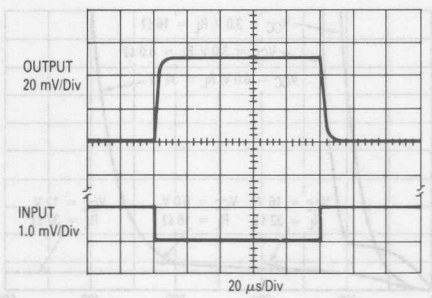
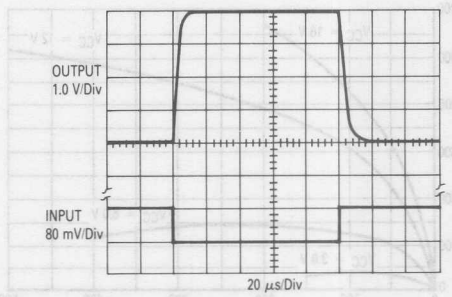


FIGURE 17 — LARGE SIGNAL RESPONSE



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FIGURE 18 — V_{CC}–V_{OH} @ VO1, VO2 versus LOAD CURRENT

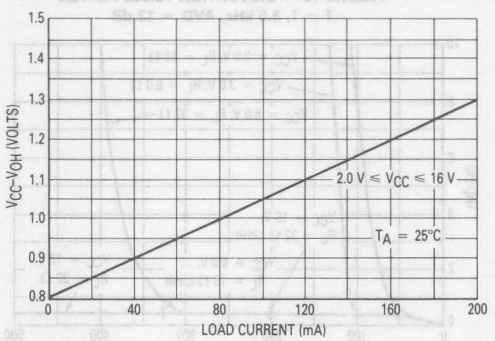


FIGURE 19 — V_{OL} @ VO1, VO2 versus LOAD CURRENT

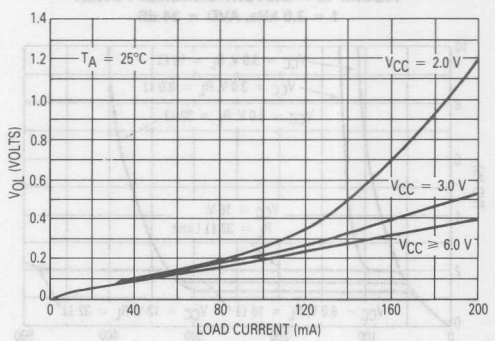


FIGURE 20 — INPUT CHARACTERISTICS @ CD (PIN 1)

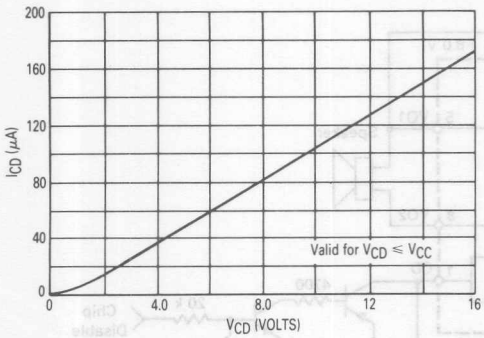
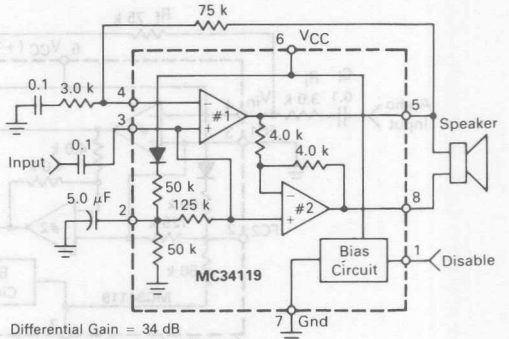


FIGURE 21 — AUDIO AMPLIFIER WITH HIGH INPUT IMPEDANCE



Differential Gain = 34 dB
Frequency Response: See Figure 3
Input Impedance ≈ 125 kΩ
PSRR ≈ 50 dB

FIGURE 22 — AUDIO AMPLIFIER WITH BASS SUPPRESSION

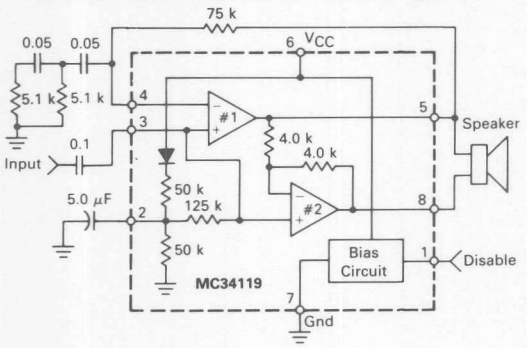


FIGURE 23 — FREQUENCY RESPONSE OF FIGURE 22

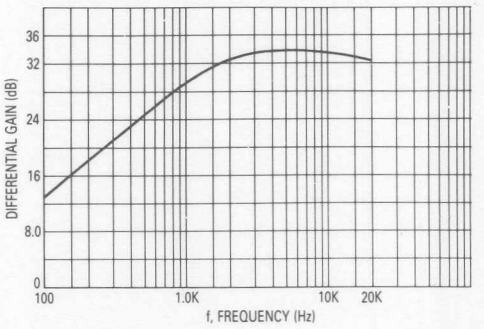


FIGURE 24 — AUDIO AMPLIFIER WITH BANDPASS

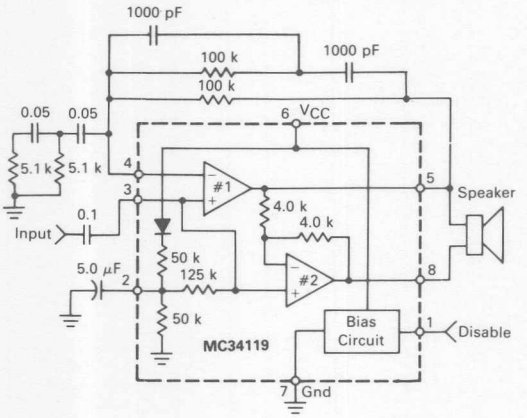
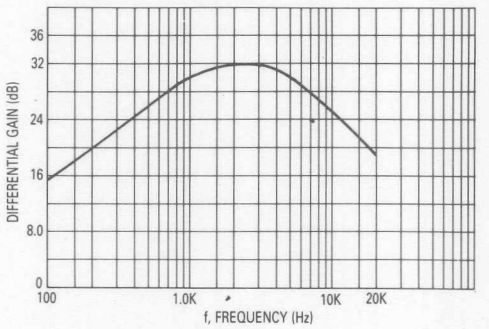
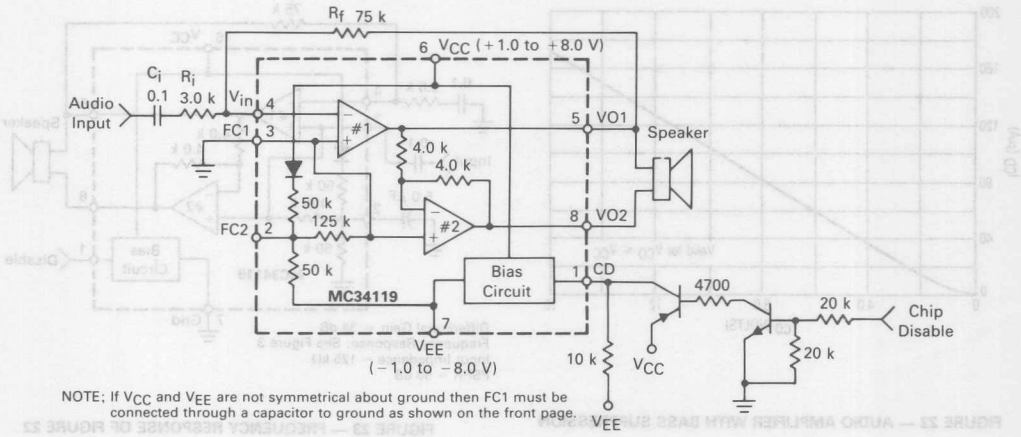


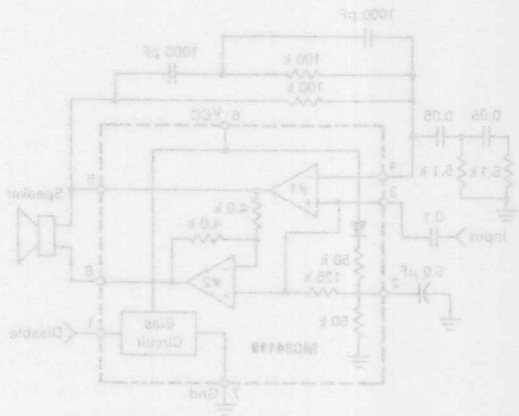
FIGURE 25 — FREQUENCY RESPONSE OF FIGURE 24



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NOTE; If V_{CC} and V_{EE} are not symmetrical about ground then FC1 must be connected through a capacitor to ground as shown on the front page.



MOTOROLA

MC44301
(Formerly MC13011)

Product Preview

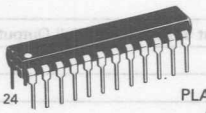
SYSTEM 4
HIGH PERFORMANCE COLOR TV IF

The MC44301 is a single channel TV IF and PLL detector system for all standard transmission systems. This device enables the designer to produce a high quality IF system with white spot inversion, AFT and AGC. The MC44301 was designed with an emphasis on linearity to minimize sound/picture intermodulation.

- Single Coil Adjustment for AFT and PLL
- VCO at 1/2 IF for Minimum Beats
- Simple Circuitry for Low System Cost
- White Spot Inversion
- Symmetrical ± 2.0 MHz Pull-In
- Detects Positive or Negative Modulation
- Auxiliary AM Detector for AM Sound
- Simple Alignment Procedure

SYSTEM 4
HIGH PERFORMANCE
COLOR TV IF

SILICON MONOLITHIC INTEGRATED CIRCUIT

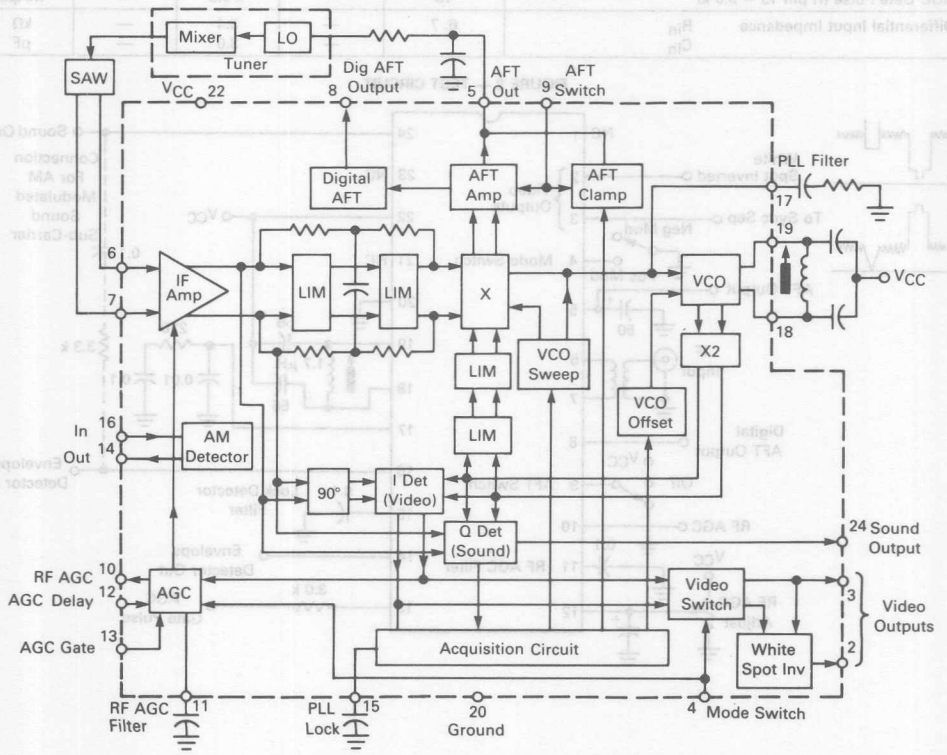


P SUFFIX
PLASTIC PACKAGE
CASE 724-03



DW SUFFIX
PLASTIC PACKAGE
CASE 751E-02
SO-24

FIGURE 1 — BLOCK DIAGRAM



This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

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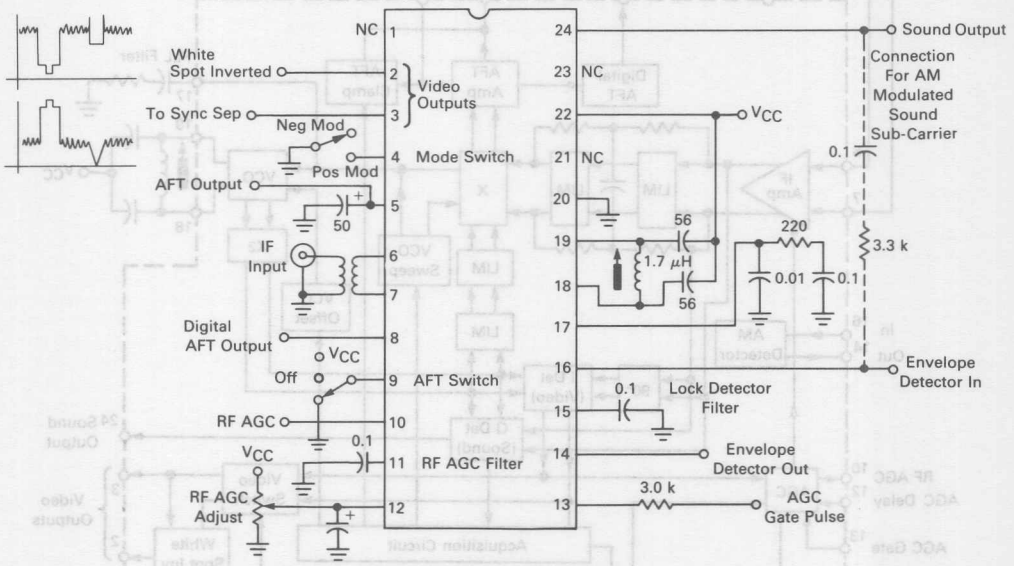
MAXIMUM RATINGS

Rating	Symbol	Value	Units
Power Supply Voltage — Pin 22	V_{CC}	7.0	Vdc
Gating Pulse Amplitude	V_{13}	±500	mApk
Operating Temperature	T_A	−40 to +85	°C
Storage Temperature	T_{stg}	−65 to +150	°C
Junction Temperature	T_J Max	150	°C
Power Dissipation Derate above 25°C	P_D	1.25 10	W mW/°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, T_A = 25°C unless noted)

Characteristic	Pins	Min	Typ	Max	Units
Operating Supply Voltage Range	22	4.5	—	5.5	Vdc
Supply Current	22	—	50	—	mAdc
Differential Input Sensitivity for Full Output	6, 7	—	20	—	μV_{rms}
Bandwidth	—	—	120	—	MHz
AGC Range	—	—	80	—	dB
Noise Figure	—	—	7.0	—	dB
Lock-Up Time	—	—	5.0	—	ms
Video Amplitude (100% mod depth)	2, 3	—	2.4	—	V_{PP}
Tuner AGC Current	10	5.0	—	—	mAdc
Differential Gain Distortion	2	—	—	5.0	%
Differential Phase Distortion	2	—	—	2.0	degrees
Video Bandwidth	2, 3	—	8.0	—	MHz
Sound Subcarrier Output (−20 dB to PIX)	24	—	0.1	—	V_{rms}
AGC Gate Pulse (R pin 13 ≈ 5.0 k)	13	—	±0.3	—	mApk
Differential Input Impedance R_{in} C_{in}	6, 7	— —	3.4 3.0	— —	kΩ pF

FIGURE 2 — TEST CIRCUIT



CIRCUIT DESCRIPTION

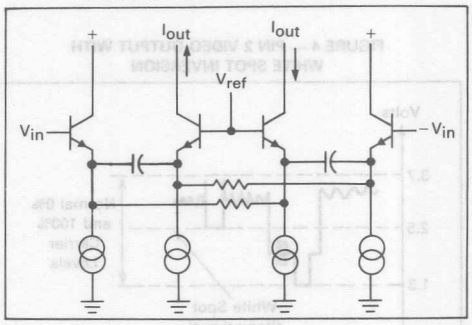
Design Aims

The MC44301 performs the functions of IF amplification, AGC, AFT and demodulation of a TV IF signal for both positive and negative modulation systems. In this respect it is similar to other circuits already on the market. However, in the means of obtaining these functions the MC44301 is very different compared to traditional designs. A unique approach was needed for several reasons. Tuned circuits associated with the IF amplifier output had to be eliminated to enable the part to be easy to use with the minimum of adjustments and external components. With this approach a high degree of IF stability could be obtained with a reduction in cost. Secondly, new techniques were required to improve performance in certain critical areas (differential phase and gain, etc.). This was especially so in view of the removal of the above mentioned tuned circuits. The basic idea therefore, was to produce an advanced, high performance multistandard IF system which would be economical and easy to use. Such a device can successfully compete with the already established IF amplifiers now available.

System Description

Despite the extra complications compared to pseudo synchronous demodulation, true synchronous demodulation seemed to be the only way in which enhanced performance could be achieved. The basic system is shown in Figure 1 in block diagram form. The IF amplifier is a four stage, AC coupled design having a sensitivity of about 20 μV. With a low loss SAW filter and 3.0 to 6.0 dB extra gain in the tuner, there is no need for a SAW preamp. The TV set signal to noise performance is acceptable, while the net savings in cost is considerable. The AGC is a conventional gated system with the usual RF AGC output and RF AGC adjustment. Three stages of the amplifier are gain controlled to give an extended AGC range of 80 dB with improved intermodulation, signal handling, and differential phase and gain performance. The AGC reference is switched when positive modulation is selected, via the mode switch, to ensure the video level remains constant. Under these circumstances the AGC must be gated by a pulse which will sample the back porch, as opposed to negative modulation where flyback can be used. In both cases a positive or negative-going pulse may be used. To ensure that the improvements in performance mentioned above were not lost elsewhere, great care was taken in the design of the video demodulator and video amplifiers. An example of this care is the placing of the phase shift required by the video demodulator on the signal side instead of on the oscillator side of the demodulator as is common practice. The 90° phase shift is produced by replacing the usual emitter resistors by capacitors in the differential amplifier (Figure 3) feeding the video demodulator. The output currents are 90° with respect to the input voltage over a wide band of frequencies and the small phase errors caused by the transistor small signal emitter resistances (re) are corrected by the cross-coupled resistors. This arrangement leads to a simpler design, the ability to adjust the demodulation angle, and lower distortion than is normal at the IF amplifier/demodulator interface. The dynamic emitter resistances, which can give rise to distortion, are now in quadrature with the capacitive reactance and, therefore, contribute very little to the resultant output.

FIGURE 3 — 90° PHASE SHIFT AMPLIFIER



Following the IF amplifier and preceding the PLL phase detector is a two stage limiter with a gain of 100 and overall dc feedback. This contrasts with the usual single stage of limiting with no dc feedback and a tuned circuit with diodes at it's output. With two stages of limiting, the minimum gain required to remove signal amplitude modulation can be designed-in without the large voltage swings of a single stage with the same gain. Large voltage swings lead to poor differential phase and gain performance, hence the need for a tuned circuit and diodes as used in previous designs. The dc feedback removes the effects of input offsets which are another source of differential phase and gain problems. The combination of low swing per stage and dc feedback removes the need for having a tuned circuit at the output of the limiter and reduces the danger of IF instability and radiation. The only problem in using this technique is the potential for extra static phase shift and resultant errors in the demodulating angles at the video and sound demodulators. However, by putting a similar two stage limiter, with matching phase shift, on the oscillator side of the phase detector, the demodulating angles can be restored to the correct phases (0, 90°). Having processed the signal in this way, the VCO is then phase locked at 90° to the nonlimited signal. The only unusual feature of the loop just described is that the VCO runs at half frequency, and is frequency doubled on-chip. This means radiation from the external frequency determining components will be at "half IF" and so will not desensitize the system even if picked up by the amplifier input leads (this could cause what is known as PLL push-off). Running the oscillator at twice IF frequency and dividing down, which is another way of

solving this problem has several disadvantages. First and foremost, radiation into the antenna at twice IF produces channel 6 and channel 8 problems in the USA. Secondly, it is easier to produce a stable VCO at half IF.

After attaining phase lock, demodulation of the video is achieved by multiplying the signal (nonlimited) with the regenerated vision carrier (VCO) in a double balanced multiplier, the phase relationship between the two waveforms being zero degrees. Both positive and negative sync video outputs are produced.

FIGURE 4 — PIN 2 VIDEO OUTPUT WITH WHITE SPOT INVERSION

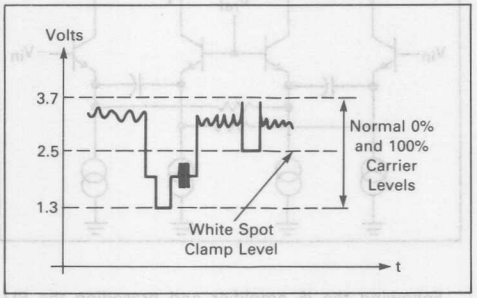
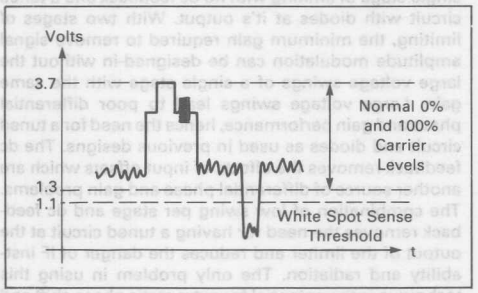


FIGURE 5 — PIN 3 VIDEO OUTPUT FOR DRIVE TO A SYNC SEPARATOR



The negative sync output is intended to be used as the actual video and is acted upon by the white spot noise inverter. This effectively removes the "whiter than white" noise produced by a true synchronous demodulator and prevents the CRT from being over driven and defocused. The positive sync video output is not acted on by a white spot noise inverter and of course the noise output from a synchronous detector does not contain a dc component. Hence, this drive should be used as the sync separator drive because a simple preseparator low pass noise filter will produce optimum sync performance. Note the sense of the video signals at the outputs remain the same whether positive or negative modulation is being received. Positive or negative modulation is selected externally by the mode switch pin. The sound intercarrier is recovered by another demodulator similar to the video, except that the phase relationship between the signal and the VCO is 90° instead of 0°. A consequence of this phase relationship is that video interference of the intercarrier signal at the detector output is minimized by suppression of the lower frequency video components. Should the sound carrier contain amplitude information, as in the French TV system or as in some scrambled cable signals, this information can be recovered by feeding the sound intercarrier output back into the circuit through a bandpass filter if so desired, to the amplitude detector provided on chip.

The AFT portion of the circuit is the most unconventional in form. Essentially, AFT is derived by amplifying the error signal driving the VCO after phase lock, and applying this to the local oscillator in the tuner, thus eliminating a coil and a potential IF instability problem. After acquisition, and when the circuit has settled down, due to the much higher gain in the LO loop, the VCO will have moved a small amount (Δfv) from it's nominal frequency, and almost all the original error frequency (Δfe) between LO and VCO will have been corrected by the change in LO frequency (Δfl). In this way, provided the PLL can be initially locked to the incoming IF signal, the VCO can be used as the frequency reference for the AFT system. It follows from the above therefore, because the system is phase locked, that $\Delta fe = (\Delta fl + \Delta fv)$. The combination of the local VCO loop and the loop produced by feedback to the LO forms a double loop PLL. Analysis shows that overall system stability can be assured by treating the VCO loop as a stand alone PLL, provided its bandwidth is much wider than the LO loop. The VCO loop therefore is a low gain wideband loop which guarantees initial capture, while the LO loop is basically a high gain dc loop used to keep frequency and phase offsets to a minimum. Large phase offsets can also be caused by dc offsets in the phase detector and AFT amplifier. These are removed by the use of commutation on both the phase and AFT outputs. This eliminates the need for external phase adjustment, while at the same time minimizing distortion by maintaining the correct phase angles at the demodulators.

The AFT system has been designed to acquire the vision carrier, without false locking to the sound or adjacent sound carriers, with an initial LO frequency error of ± 2.0 MHz, reducing this initial error to 3.0 to 10 kHz when locked. This contrasts to the discriminator type of AFT's which have highly asymmetric lock characteristics (−2.0 MHz + 1.0 MHz), because of the effects of the IF filter, and large frequency errors caused by limited loop gain. To achieve this level of performance without encountering the normal AFT problems associated with high loop gain, a novel approach has been taken to locking up to the PLL. In the absence of an IF signal, the acquisition circuitry examines the state of the video (I) and sound (Q) demodulators and detects the lack of a signal. It then clamps the LO drive to a reference dc level and applies a −2.0 MHz offset to the VCO. This is done so that the nominal IF (should a signal appear), and the VCO, are sitting in the center of the IF filter passband. Therefore, even if the LO drifts high by +2.0

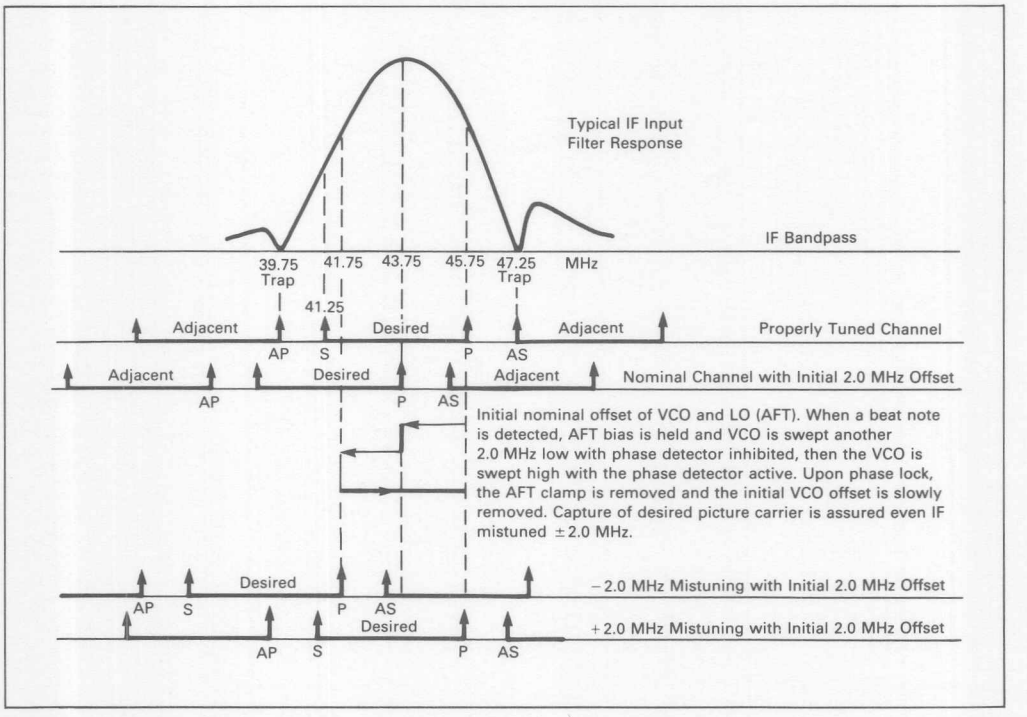
MHz, the signal will not be significantly attenuated by the filter. When the acquisition circuit detects the appearance of a signal, beat notes are produced at the output of the demodulators, a sweep generator is switched on, and immediately sweeps the VCO an additional −2.0 MHz from it's out of lock nominal frequency.

During this negative sweep, the PLL phase detector is switched off so phase lock cannot be obtained. The VCO is then swept positive from −2.0 MHz to +2.0 MHz of nominal with the phase detector switched on. The PLL will therefore lock to the first carrier it encounters. This in fact must be the vision carrier because the sound carrier is more negative than −2.0 MHz from nominal and the adjacent sound carrier is higher than the vision carrier. On achieving phase lock, the AFT clamp is released, the VCO offset is slowly removed, the sweep is inhibited and the phase detector remains enabled. With the AFT clamp removed, a large error voltage appears at the AFT output, driving the system back towards the correct frequency. Since the LO loop is slow and the VCO is fast, the IF changes slowly and the VCO tracks it, maintaining phase lock until the final static conditions are reached. For large frequency errors during this period the slew rate of the LO loop is increased, but not to the extent where it would cause any VCO tracking problems. This technique allows the acquisition time of the circuit to be considerably shortened while still using a larger than normal time constant in the LO loop. To accommodate all types of tuners and LO's, positive or negative LO drive can be selected externally by operation of the AFT switch. The AFT switch also has a third position which disconnects the drive to the tuner. Under this condition the TV set can be tuned in the normal manner and so appears to have a conventional type of AFT. Other PLL AFT systems cannot be manually tuned in this way having an abrupt capture characteristic when tuned, and because of this, have not gained general acceptance in industry.

ALIGNMENT

The alignment is very simple and inexpensive compared to other IF amplifier circuits, especially those using a PLL. With a CW input signal of correct picture carrier frequency, the LO side of the 22 k resistor in series with the loop is connected to a dc supply. The dc supply (approximately 2.5 V) is adjusted until the output of the tuner is 45.75 MHz. The VCO coil is adjusted until lock is obtained and the voltage across the 22 k resistor

FIGURE 6 — THE AFT SYSTEM IN ACTION



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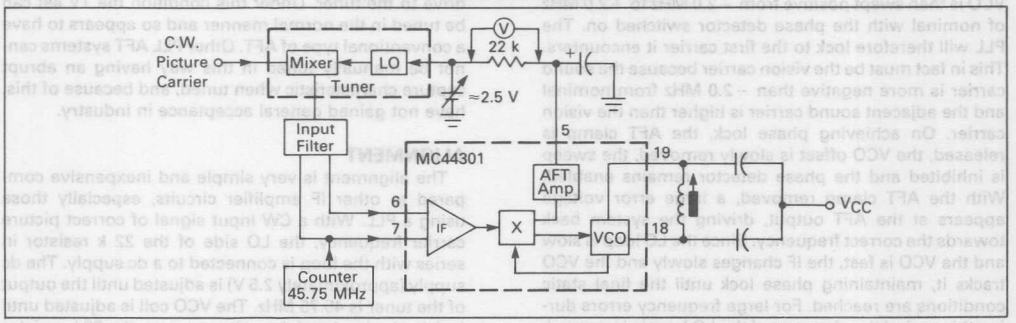
is zero. The dc supply is then removed.

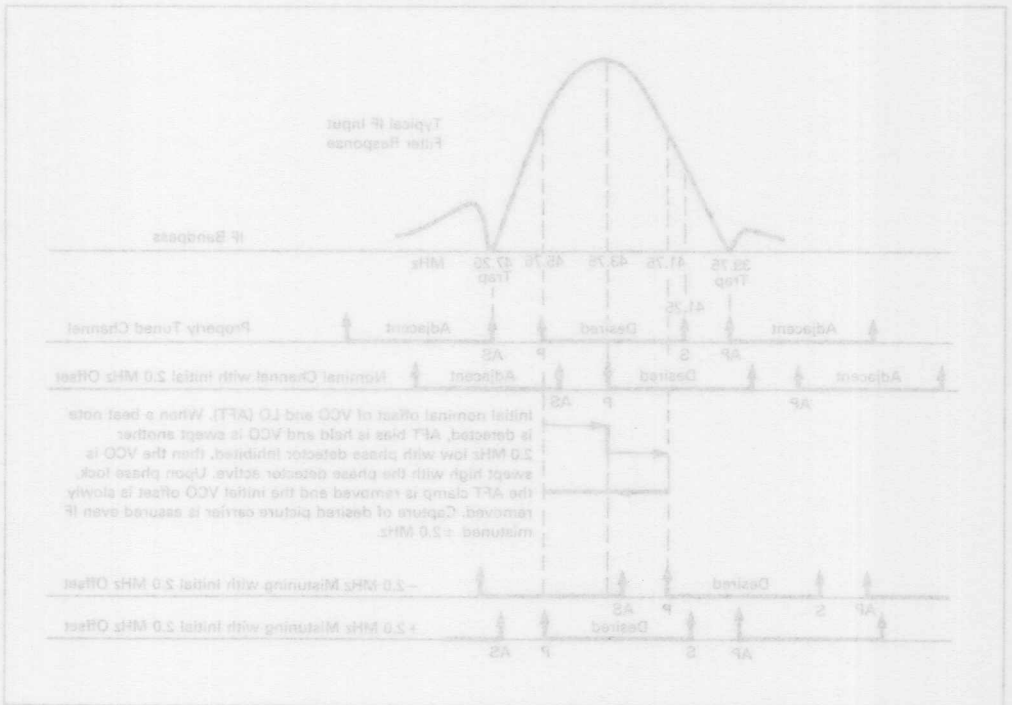
A digital AFT up/down output having a ± 30 kHz dead zone is also provided by the circuit. Again, as in the case of the analog output, the digital output polarity can be controlled externally by the AFT switch.

Note:

Most pins on the IC have electrostatic protection diodes to V_{CC} and ground. It is therefore imperative that no pin is taken below ground or above V_{CC} by more than one diode drop without current limiting.

FIGURE 7 — ALIGNMENT CONFIGURATION





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MOTOROLA

MC44802

Product Preview

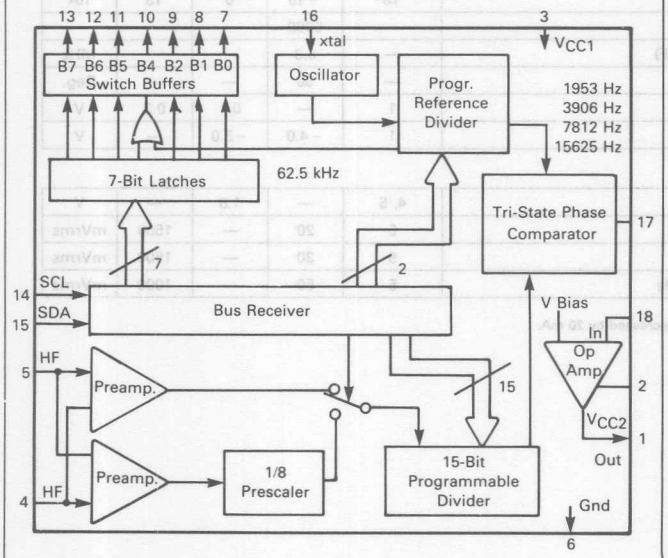
PLL TUNING CIRCUIT WITH 1.3 GHz PRESCALER

The MC44802 is a tuning circuit for TV applications. It contains on one chip all the functions required for PLL control of a VCO. This integrated circuit also contains a high frequency prescaler (which can be bypassed by software control) and thus can handle frequencies up to 1.3 GHz.

The MC44802 is manufactured on a single silicon chip using Motorola's high density bipolar process, MOSAIC (Motorola Oxide Self Aligned Implanted Circuits).

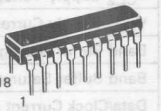
- Complete Single Chip System for MPU Control (IIC Bus)
- Selectable Divide-by-8 Prescaler Accepts Frequencies >1.0 GHz
- 15-Bit Programmable Divider Accepts Input Frequencies >125 MHz
- Programmable Reference Divider
- Tri-State Phase/Frequency Comparator
- Op Amp for Direct Tuning Voltage Output (33 V)
- Seven High Current Output Buffers (10 mA)
- Output Options for 62.5 kHz, Reference Frequency and the Programmable Divider
- Software Compatible with MC44810

SIMPLIFIED BLOCK DIAGRAM



This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

PLL TUNING CIRCUIT WITH 1.3 GHz PRESCALER

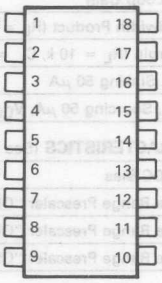


CASE 707-02
PLASTIC PACKAGE



DW SUFFIX
CASE 751C-03
PLASTIC PACKAGE
SO-18L

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC44802P	0°C to 70°C	18-Pin DIP
MC44802DW		18-Pin SOIC

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MAXIMUM RATINGS (T_A = 25°C unless otherwise specified)

Ratings	Pin	Value	Unit
Power Supply Voltage V_{CC1}	3	6.0	V
Band Buffer "OFF" Voltage	7 to 13	15	V
Band Buffer "ON" Current	7 to 13	15	mA
Op Amp Power Supply Voltage V_{CC2}	2	36	V
Op Amp Short Circuit Duration (0 to V_{CC2})	1	Continuous	V
Storage Temperature		−65 to +150	°C
Operating Temperature Range		0 to +70	°C

ELECTRICAL CHARACTERISTICS (V_{CC1} = 5.0 V, V_{CC2} = 32 V, T_A = 25°C unless otherwise specified)

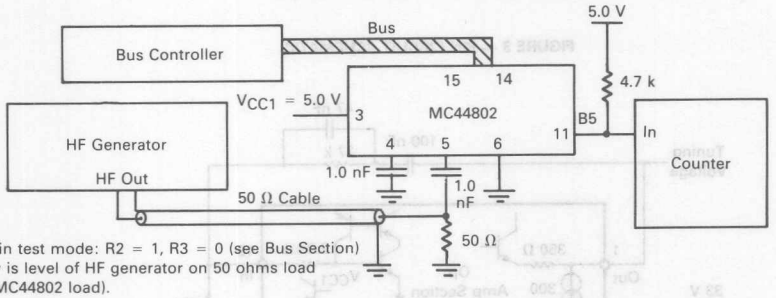
Characteristic	Pin	Min	Typ	Max	Unit
V_{CC1} Supply Voltage Range	3	4.5	5.0	5.5	V
V_{CC1} Supply Current (V_{CC1} = 5.0 V) (Note 1)	3	—	60	90	mA
V_{CC2} Supply Voltage Range	2	25	30	35	V
V_{CC2} Supply Current (Output Open)	2	—	0.8	2.0	mA
Band Buffer Leakage Current When "OFF" at 12 V	7 to 13	—	0.01	1.0	μA
Band Buffer Saturation Voltage When "ON" at 10 mA	7 to 13	—	0.6	1.0	V
Data/Clock Current at 0 V	14, 15	−10	—	0	μA
Clock Current at 5.0 V	14	0	—	1.0	μA
Data Current at 5.0 V Acknowledge "OFF"	15	0	—	1.0	μA
Data Saturation Voltage at 15 mA Acknowledge "ON"	15	—	—	1.0	V
Data/Clock Input Voltage Low	14, 15	—	—	1.5	V
Data/Clock Input Voltage High	14, 15	3.0	—	—	V
Clock Frequency Range	14	0	—	100	kHz
Phase Detector Tri-State Current	17	−15	0	15	nA
Phase Detector High-State Source Current (@ 1.5 V)	17	−3.0	−2.2	−1.5	mA
Phase Detector Low-State Sink Current (@ 3.5 V)	17	2.0	3.0	4.0	mA
Op Amp Internal Reference Voltage	—	2.0	—	3.0	V
Op Amp Input Current	18	−15	0	15	nA
DC Open Loop Gain	—	5000	—	—	
Gain Bandwidth Product (R_L = 10 k, C_L = 20 pF)	—	0.3	—	—	MHz
Phase Margin (R_L = 10 k, C_L = 20 pF)	—	50	—	—	Deg.
V_{out} Low, Sinking 50 μA	1	—	0.1	0.3	V
V_{out} High, Sourcing 50 μA, V_{CC2}	1	−4.0	−3.0	—	V

HF CHARACTERISTICS (See Figure 1)

HF In/Ref DC Bias	4, 5	—	1.6	—	V
HF Voltage Range Prescaler "OFF" 10–150 MHz	5	20	—	1500	mVrms
HF Voltage Range Prescaler "ON" 50–950 MHz	5	30	—	1500	mVrms
HF Voltage Range Prescaler "ON" 950–1300 MHz	5	50	—	1000	mVrms

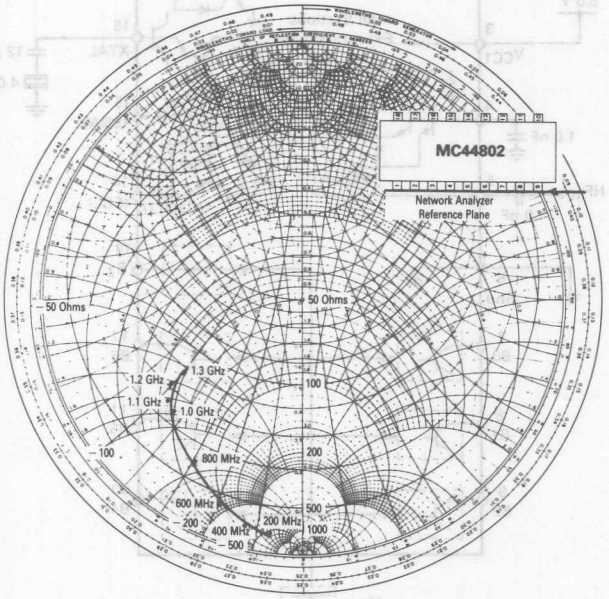
NOTE
1. When prescaler "OFF," typical supply current is decreased by 20 mA.

FIGURE 1 — HF SENSITIVITY TEST CIRCUIT



Device is in test mode: R2 = 1, R3 = 0 (see Bus Section)
sensitivity is level of HF generator on 50 ohms load
(without MC44802 load).

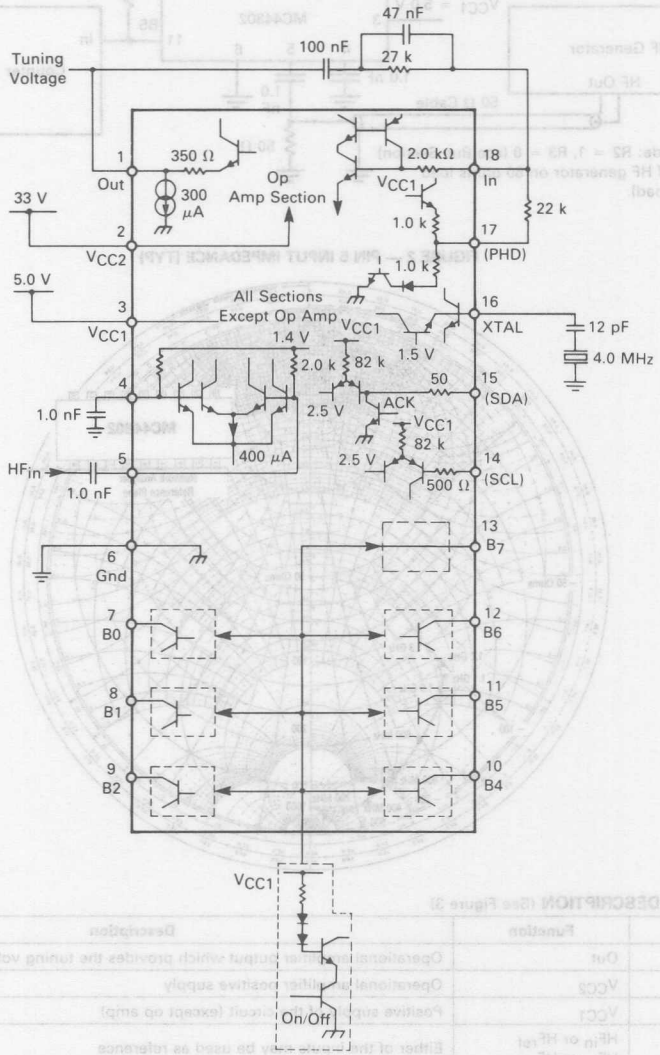
FIGURE 2 — PIN 5 INPUT IMPEDANCE (TYP)



PIN FUNCTION DESCRIPTION (See Figure 3)

Pin	Function	Description
1	Out	Operational amplifier output which provides the tuning voltage
2	V_{CC2}	Operational amplifier positive supply
3	V_{CC1}	Positive supply of the circuit (except op amp)
4 5	HF_{in} or HF_{ref} HF_{in} or HF_{ref}	Either of the inputs may be used as reference
6	Gnd	Ground
7, 8, 9, 10, 11, 12, 13	B0, B1,.....B7	Band buffer output can drive up to 10 mA
14	SCL	Clock Input (supplied by the microprocessor via IIC bus)
15	SDA	Data Input
16	XTAL	Crystal Input (4.0 MHz)
17	PHD	Phase Comparator Output
18	In	Negative Operational Amplifier Input

FIGURE 3 — PIN CIRCUIT SCHEMATIC



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FUNCTIONAL DESCRIPTION

A representative block diagram and a typical system application are shown in Figures 4 and 5. A discussion of the features and function of each of the internal blocks is given below.

FIGURE 4 — BLOCK DIAGRAM

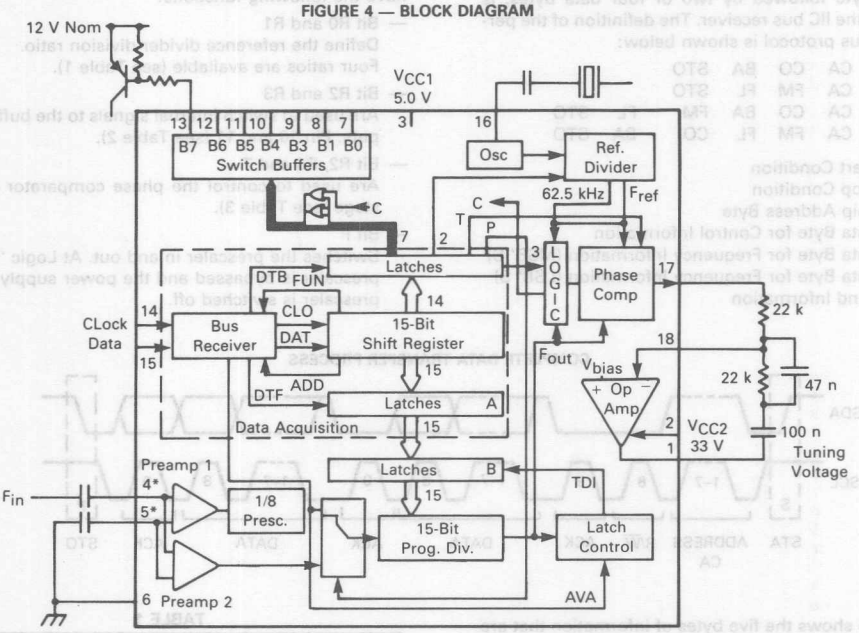
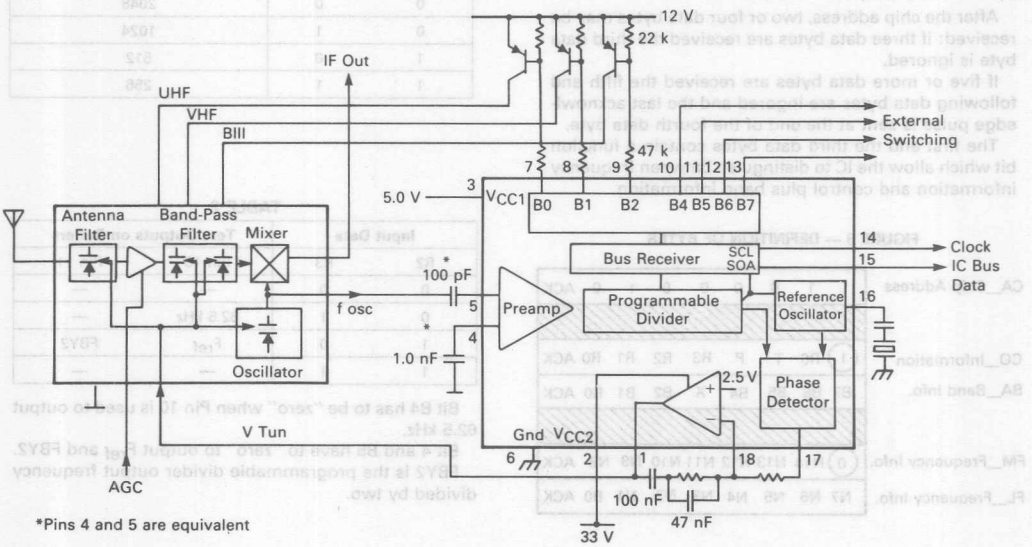


FIGURE 5 — TYPICAL TUNER APPLICATION



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DATA FORMAT AND BUS RECEIVER

The circuit receives the information for tuning and control via a two-wire bus (Motorola Bus, IIC compatible). The incoming information consisting of a chip address byte followed by two or four data bytes, is treated in the IIC bus receiver. The definition of the permissible bus protocol is shown below:

1_STA	CA	CO	BA	STO		
2_STA	CA	FM	FL	STO		
3_STA	CA	CO	BA	FM	FL	STO
4_STA	CA	FM	FL	CO	BA	STO

STA = Start Condition
STO = Stop Condition
CA = Chip Address Byte
CO = Data Byte for Control Information
FM = Data Byte for Frequency Information (MSB' S)
FL = Data Byte for Frequency Information (LSB' S)
BA = Band Information

Frequency information is preceeded by a Logic "0." If the function bit is Logic "1" the two following bytes contain control and band information where the bits have the following functions:

— Bit R0 and R1
Define the reference divider division ratio.
Four ratios are available (see Table 1).

— Bit R2 and R3
Are used to switch internal signals to the buffer outputs. Pin 10 and 11 (see Table 2).

— Bit R2, R6 and T
Are used to control the phase comparator output stage (see Table 3).

— Bit P
Switches the prescaler in and out. At Logic "1" the prescaler is bypassed and the power supply of the prescaler is switched off.

COMPLETE DATA TRANSFER PROCESS

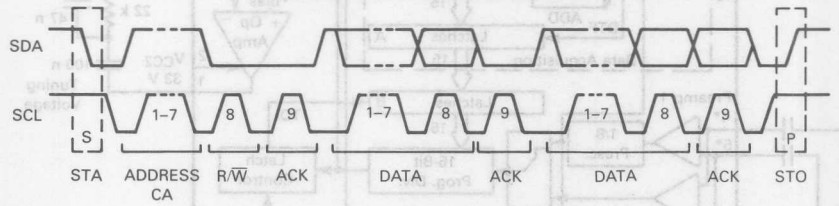


Figure 6 shows the five bytes of information that are needed for circuit operation: there is the chip address, two bytes of control and band information and two bytes of frequency information.

After the chip address, two or four data bytes may be received: if three data bytes are received the third data byte is ignored.

If five or more data bytes are received the fifth and following data bytes are ingored and the last acknowledge pulse is sent at the end of the fourth data byte.

The first and the third data bytes contain a function bit which allow the IC to distinguish between frequency information and control plus band information.

FIGURE 6 — DEFINITION OF BYTES

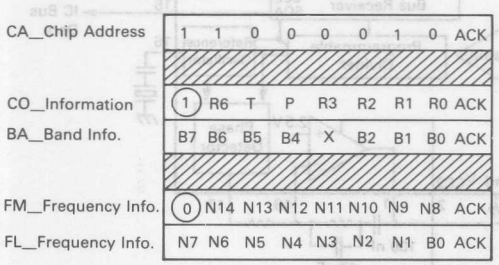


TABLE 1

Input Data		Reference Divider
R1	R0	Division Ratio
0	0	2048
0	1	1024
1	0	512
1	1	256

TABLE 2

Input Data		Test Outputs on Buffers	
R2	R3	Pin 10	Pin 11
0	0	—	—
0	1	62.5 kHz	—
1	0	F_{ref}	FBY2
1	1	—	—

Bit B4 has to be "zero" when Pin 10 is used to output 62.5 kHz.

Bit 4 and B5 have to "zero" to output F_{ref} and FBY2.

FBY2 is the programmable divider output frequency divided by two.

TABLE 3

Input Data			Output State of the Phase Comparator
R2	R6	T	
0	0	0	Normal Operation
0	0	1	Off (High Impedance)
0	1	0	High
0	1	1	Low
1	0	0	Normal Operation
1	0	1	Off
1	1	0	Normal Operation
1	1	1	Off

THE BAND BUFFERS

BA_Band Information	B7	B6	B5	B4	X	B2	B1	B0	ACK

The band buffers are open collector transistors and are active "low" at Bn = 1. They are designed for 10 mA with a typical on-resistance of 70 ohms. These buffers are designed to withstand relative high output voltage in the off-state.

B4 and B5 buffers (Pins 10 and 11) may also be used to output internal IC signals (reference frequency and programmable divider output frequency divided by 2) for tests purposes.

Buffer B4 may also be used to output a 62.5 kHz frequency for an intermediate stage of the reference divider. The bit B4 and/or B5 have to be zero if the buffers are used for these additional functions.

THE PROGRAMMABLE DIVIDER

The programmable divider is a presettable down counter. When it has counted to zero it takes its required division ratio out of the latches B. Latches B are loaded from latches A by means of signal TDI which is synchronous to the programmable divider output signal.

Since latches A receive the data asynchronously with the programmable divider, this double latch scheme is needed to assure correct data transfer to the counter.

The division ratio definition is given by:

$N = 16384 \times N14 + 8132 \times N13 + ... + 4 \times N2 + 2 \times N1 + N0$

Max Ratio 32767
Min Ratio 17

Where N0.....N14 are the different bits for frequency information.

The counter may be used for any ratio between 17 and 32767 and reloads correctly as long as its output frequency does not exceed 1.0 MHz.

The data transfer between latches A and B (signal TDI) is also initiated by any start condition on the IIC bus.

At power-on the whole bus receiver is reset and the programmable divider is set to a counting ratio of N = 256 or higher.

THE PRESCALER

The prescaler has a preamplifier which guarantees high input sensitivity. The prescaler may be by-passed (Bit P) and the signal then passes through preamp 2.

THE PHASE COMPARATOR

The phase comparator is phase and frequency sensitive and has very low output leakage current in the high impedance state.

THE OPERATIONAL AMPLIFIER

The operational amplifier is designed for very low noise, low input bias current and high power supply rejection. The positive input is biased internally. The op amp needs 31 V supply (V_{CC2}) as minimum voltage for a guaranteed maximum tuning voltage of 28 V.

Figure 1 shows a possible filter arrangement. The component values depend very much on the application (tuner characteristic, reference frequency, etc.);

As a starting point for optimization, the components values in Figure 1 may be used for 7.8125 kHz reference frequency in a multiband TV tuner.

THE OSCILLATOR

The oscillator uses a 4.0 MHz crystal tied to ground or V_{CC1} through a capacitor, used in the series resonance mode.

The voltage at Pin 16, "crystal," has low amplitude and low harmonic distortion.

SYSTEM APPLICATION

Table 4 is a summary of the circuit applications using a 4.0 MHz crystal.

TABLE 4

Input Data R1	Input Data R0	Ref. Divider Div. Ratio	Reference Frequency Hz (1)	With Int. Prescaler P = 0 Frequency Steps kHz	With Int. Prescaler P = 0 Max. Input Frequency MHz	Without Prescaler P = 1 Frequency Steps kHz	Without Prescaler P = 1 Max. Input Frequency MHz
0	0	2048	1953.125	15.625	512	1.953125	64
0	1	1024	3906.25	31.25	1024	3.90625	128
1	0	512	7812.5	62.5	1300(2)	7.8125	165(3)
1	1	256	15625.0	125	1300(2)	15.625	165(3)

(1) With 4.0 MHz Crystal (2) Limit of Prescaler (3) Limit of Programmable Divider

9

MOTOROLA

TBA120C

FM IF AMPLIFIER, LIMITER AND DETECTOR

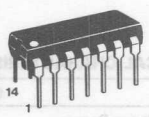
An integrated circuit specifically designed for use in the sound section of TV receivers and the FM/IF portion of radio receivers.

The TBA120C is pin for pin and function compatible with the proelectron type TBA120S but includes an improved dc volume control, which makes "grouping" or selection unnecessary.

- Excellent 3.0 dB Limiting
- High A.M. Rejection
- Wide Supply Voltage Range
- Auxiliary Zener Diode and Transistor
- Minimum Number of External Components Required

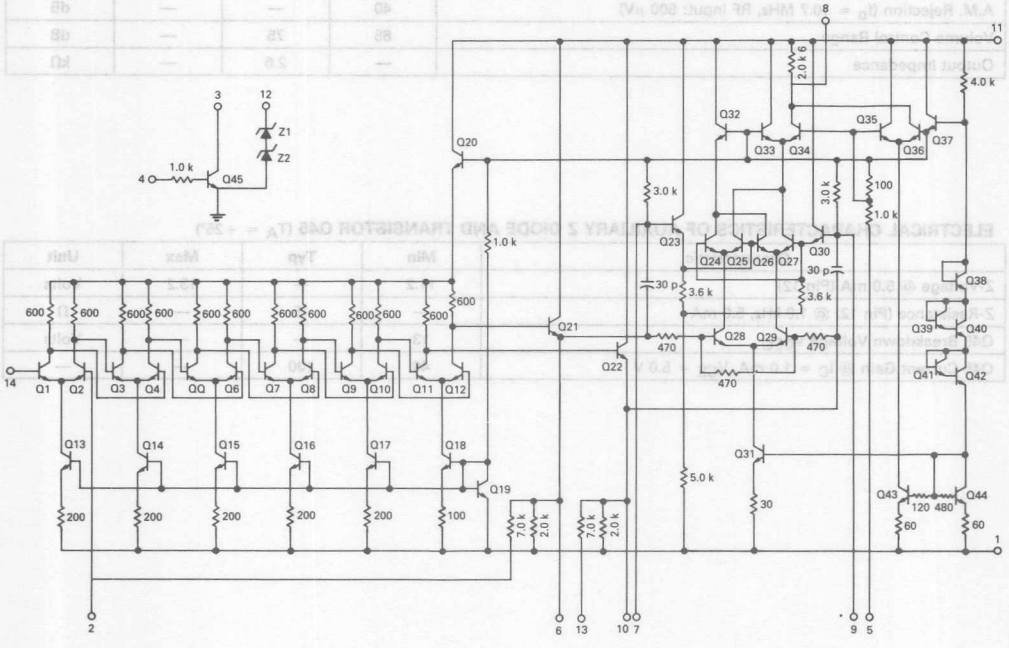
FM IF AMPLIFIER, LIMITER, FM DETECTOR AND AUDIO PREAMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 646-06

CIRCUIT SCHEMATIC



9

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Value	Unit
Power Supply Voltage	+18	Vdc
Power Dissipation (Package Limitation) Plastic Package Derate above T_A = +25°C	 625 5.0	 mW mW/°C
Operating Temperature Range	0 to +75	°C
Storage Temperature Range	−65 to +150	°C

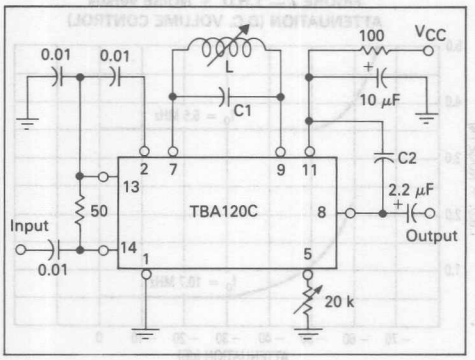
ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = 12 V, R = 20 k, Test circuit: Figure 1)

Characteristic	Min	Typ	Max	Unit
Supply Voltage Range	6.0	—	18	Volts
Supply Current	10	14	18	mA
Audio Output (f_o = 5.5 MHz, Δf = 50 kHz, Q = 45)	—	1.0	—	Volts RMS
Audio Output (f_o = 10.7 MHz, Δf = 75 kHz, Q = 35)	—	0.38	—	Volts RMS
3.0 dB Limiting (f_o = 5.5 MHz, Δf = 50 kHz, Q = 45)	—	30	60	μVRMS
3.0 dB Limiting (f_o = 10.7 MHz, Δf = 75 kHz, Q = 35)	—	40	—	μVRMS
A.M. Rejection (f_o = 5.5 MHz, RF Input: 500 μV)	45	—	—	dB
A.M. Rejection (f_o = 10.7 MHz, RF Input: 500 μV)	40	—	—	dB
Volume Control Range	65	75	—	dB
Output Impedance	—	2.6	—	kΩ

ELECTRICAL CHARACTERISTICS OF AUXILIARY Z DIODE AND TRANSISTOR Q45 (T_A = +25°)

Characteristic	Min	Typ	Max	Unit
Z-Voltage @ 5.0 mA (Pin 12)	11.2	—	13.2	Volts
Z-Resistance (Pin 12) @ 1.0 kHz, 5.0 mA	—	15	—	Ω
Q45 Breakdown Voltage V_{CEO}	13	—	—	Volts
Q45 Current Gain @ I_C = 1.0 mA, V_{CE} = 5.0 V	40	100	—	—

FIGURE 1 — TEST CIRCUIT



COMPONENT VALUES:

	L	C_1	Q
5.5 MHz	0.55 µH	1.5 nF	45
6.0 MHz	0.55 µH	1.2 nF	45
10.7 MHz	2.2 µH	100 pF	35

C2 = 0.022 µF, together with the integrated resistor of 2.6 kΩ (Pin 8) gives the deemphasis and can be reduced if required. For stereo 470 pF should be used to provide H.F. decoupling.

FIGURE 2 — AUDIO OUTPUT AND S/N versus INPUT SIGNAL LEVEL AT 5.5 AND 6.0 MHz

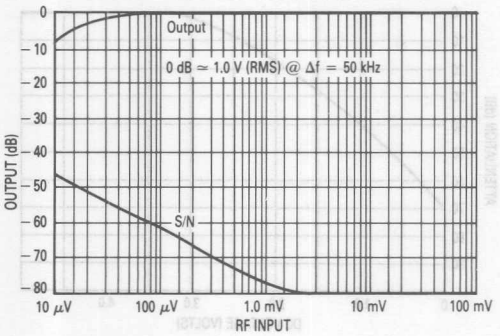


FIGURE 3 — AUDIO OUTPUT AND S/N versus INPUT SIGNAL LEVEL AT 10.7 MHz

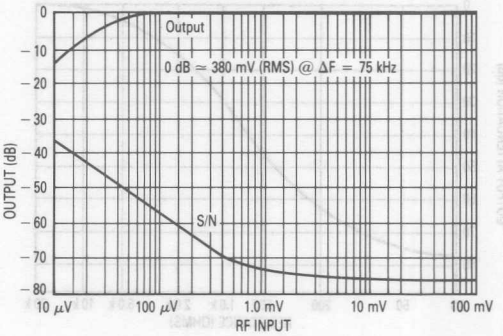


FIGURE 4 — A.M. REJECTION versus INPUT SIGNAL LEVEL AT 5.5 AND 6.0 MHz (30% A.M., 50 kHz F.M.)

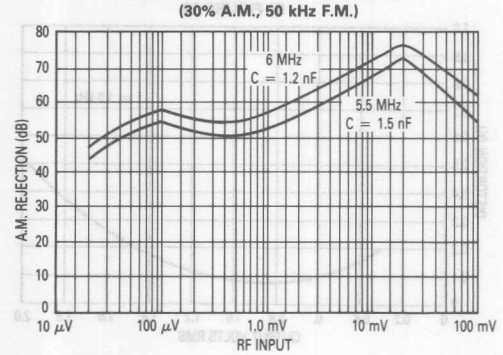
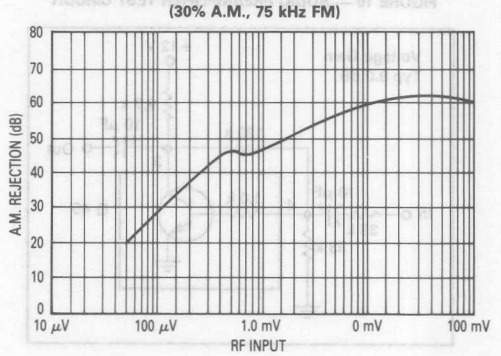


FIGURE 5 — A.M. REJECTION versus INPUT SIGNAL LEVEL AT 10.7 MHz (30% A.M., 75 kHz FM)



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FIGURE 6 — OUTPUT VOLTAGE versus SUPPLY VOLTAGE

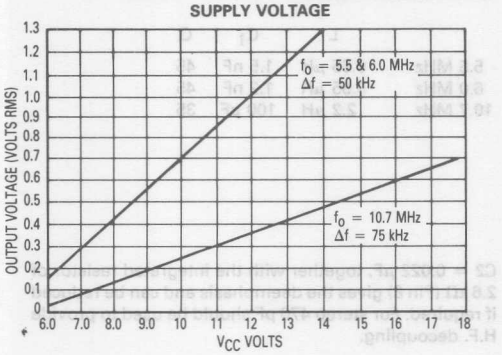


FIGURE 7 — T.H.D. + NOISE versus ATTENUATION (D.C. VOLUME CONTROL)

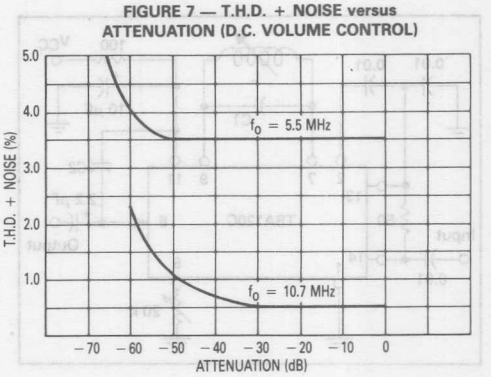


FIGURE 8 — OUTPUT SIGNAL ATTENUATION versus VOLUME CONTROL RESISTANCE

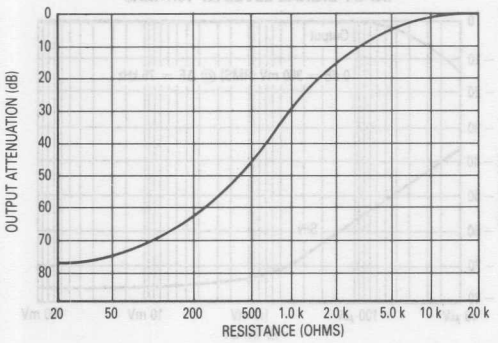


FIGURE 9 — OUTPUT SIGNAL ATTENUATION versus D.C. VOLTAGE AT PIN 5

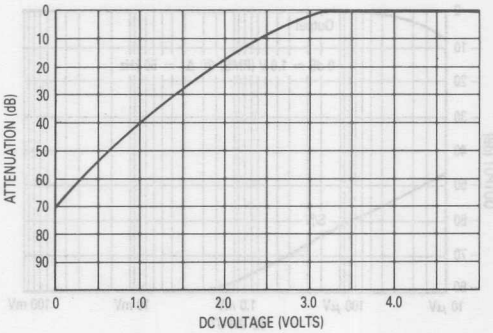


FIGURE 10 — AUDIO PREAMPLIFIER TEST CIRCUIT

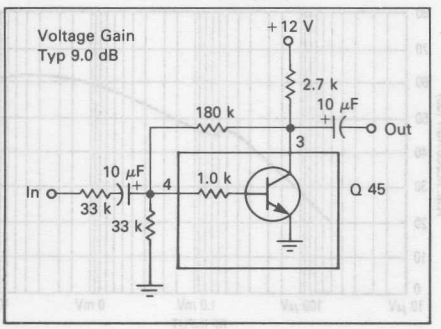
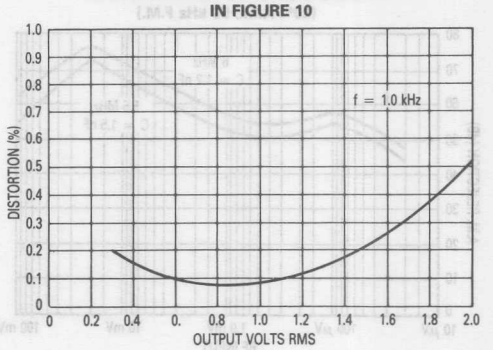


FIGURE 11 — T.H.D. versus OUTPUT VOLTAGE FOR AUDIO PREAMPLIFIER SHOWN IN FIGURE 10



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FIGURE 12 — TYPICAL APPLICATION FOR 5.5 MHz WITH L-C INPUT FILTER

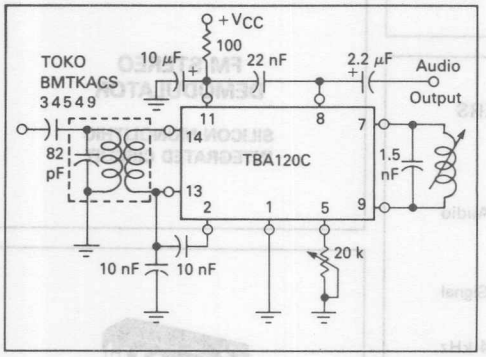


FIGURE 13 — TYPICAL APPLICATION FOR 5.5 MHz WITH CERAMIC INPUT FILTER

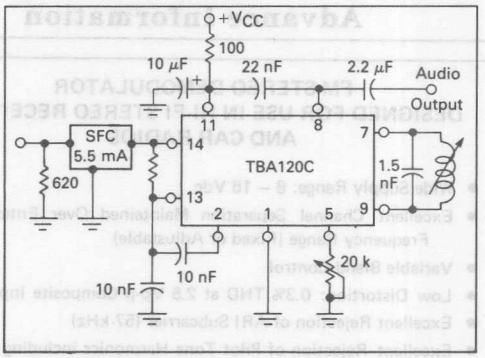
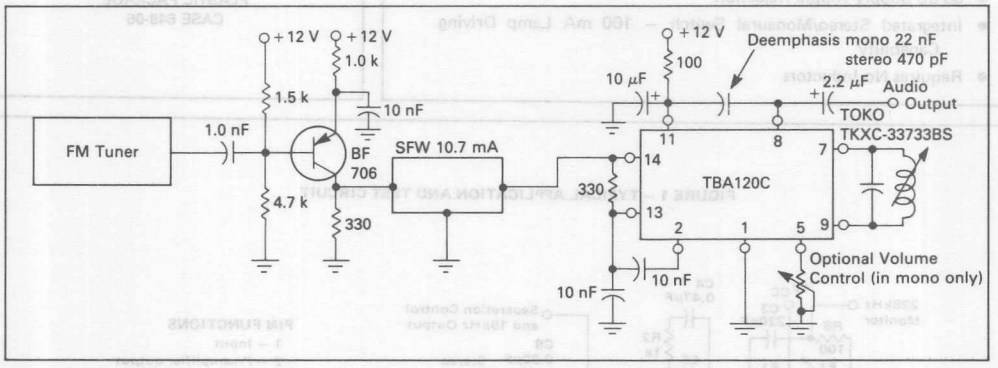


FIGURE 14 — TYPICAL APPLICATION FOR 10.7 MHz WITH CERAMIC FILTER



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TCA4500A

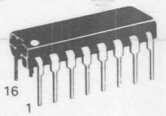
Advance Information

FM STEREO DEMODULATOR DESIGNED FOR USE IN HI-FI STEREO RECEIVERS AND CAR RADIOS

- Wide Supply Range: 8 – 16 Vdc
- Excellent Channel Separation Maintained Over Entire Audio Frequency Range (Fixed or Adjustable)
- Variable Blend Control
- Low Distortion: 0.3% THD at 2.5 Vp-p Composite Input Signal
- Excellent Rejection of ARI Subcarrier (57 kHz)
- Excellent Rejection of Pilot Tone Harmonics including 114 kHz
- Wide Dynamic Range: 0.5 – 2.5 Vp-p Composite Input Signal
- Up to 6 dB Gain (Monaural)
- Low Output Impedance
- Transient-free Mono/Stereo Switching
- 50 dB Supply Ripple Rejection
- Integrated Stereo/Monaural Switch – 100 mA Lamp Driving Capability
- Requires No Inductors

FM STEREO DEMODULATOR

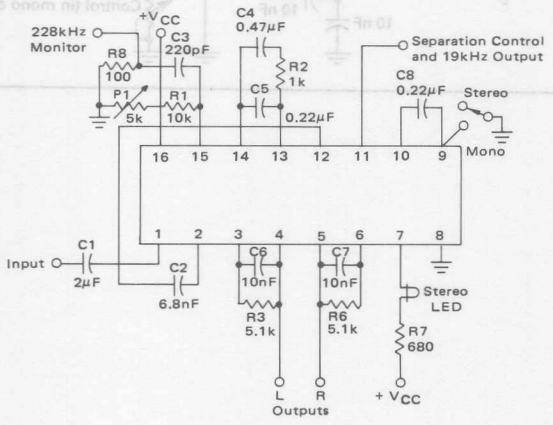
SILICON MONOLITHIC INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 648-06

9

FIGURE 1 – TYPICAL APPLICATION AND TEST CIRCUIT



PIN FUNCTIONS

1 – Input
2 – Preamplifier output
3 – Left amplifier input
4 – Left channel output
5 – Right channel output
6 – Right amplifier input
7 – Stereo indicator Lamp
8 – Ground
9 – Stereo switch filter
10 – Stereo switch filter
11 – 19 kHz output/blend
12 – Modulator input
13 – Loop filter
14 – Loop filter
15 – Oscillator RC network
16 – V_{CC}

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Value	Unit
Power Supply Voltage	16	Volts
Power Dissipation (Package limitation) Derate above T_A = +25°C	1800 15	mW mW/°C
Operating Temperature Range (Ambient)	-40 to +85	°C
Storage Temperature Range	-65 to +150	°C
Lamp Drive Voltage (Max. voltage at Pin 7 with lamp "off")	30	Volts
Lamp Current	100	mA
Blend Control Input Voltage (Pin 11)	10	Volts

ELECTRICAL CHARACTERISTICS Unless otherwise noted: V_{CC} = +12 Vdc, T_A = 25°C, 2.5 Vp-p standard multiplex composite signal with L or R channel only modulated at 1.0 kHz and with 10% pilot level, using circuit of Figure 1.

Characteristic	Min.	Typ.	Max.	Unit
Stereo Channel Separation: Unadjusted Optimised on other channel[1]	30 40	– –	– –	dB
Monaural Voltage Gain[1]	0.8	1.0	1.2	
THD at 2.5 Vp-p Composite Input Signal at 1.5 Vp-p Composite Input Signal	– –	– 0.2	0.3 –	%
Signal/Noise Ratio RMS 20 Hz - 15 kHz	–	90	–	dB
Ultrasonic Frequency Rejection 19 kHz 38 kHz	– –	31 50	– –	dB
Stereo Switch Level (19 kHz input level for lamp "on") Hysteresis	12 –	16 6.0	20 –	mVrms dB
Quiescent Output Voltage Change with Mono/Stereo Switching	–	5.0	20	mVdc
Stereo Blend Control Voltage (Pin 11) 3 dB Separation (see Figure 2) 30 dB Separation	– –	0.7 1.7	– –	V V
Minimum Separation (Pin 11 at 0 V)	–	–	1.0	dB
Monaural Channel Imbalance (pilot tone off)	–	–	0.3	dB
ARI 57 kHz Pilot Tone Influence on THD[2]	–	–	0.5	%
Sub-carrier Harmonic Rejection 76 kHz 114 kHz 152 kHz	– – –	45 50 50	– – –	dB
Supply Ripple Rejection	–	50	–	dB
Input Impedance	–	50	–	KΩ
Output Impedance	–	100	–	Ω
Blend Control Current[1]	–	–	-300	μA
Capture Range	–	±5.0	–	%
Operating Supply Voltage	8.0	–	16	V
Current Drain (lamp off)	–	35	–	mA

Notes: [1] See Applications Information and Circuit Description
[2] ARI Test – Input signal: 1.5 Vp-p standard composite signal, 1 kHz modulation added to a CW 50 mVrms signal at 57.3 kHz.

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TYPICAL CHARACTERISTICS

Unless otherwise noted V_{CC} = +12 V, T_A = +25°C, Input Signal is Modulated L or R with 10% Pilot Level. (See Fig. 16.)

——— : High Loop Gain Circuit

– – – : Normal Circuit

FIGURE 2 – CHANNEL SEPARATION versus COMPOSITE INPUT LEVEL

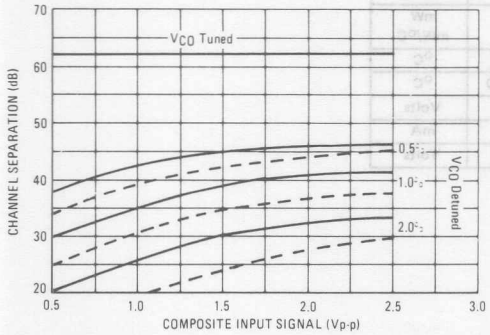


FIGURE 3 – V_{CO} FREE-RUNNING FREQUENCY versus TEMPERATURE

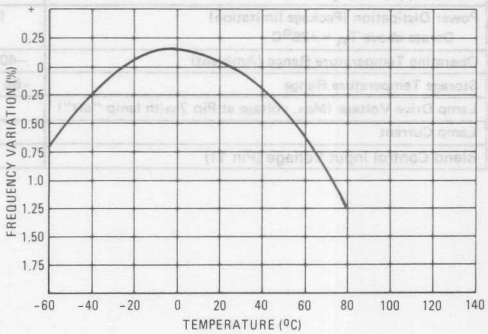


FIGURE 4 – STEREO SWITCH LEVEL versus V_{CO} FREE-RUNNING FREQUENCY

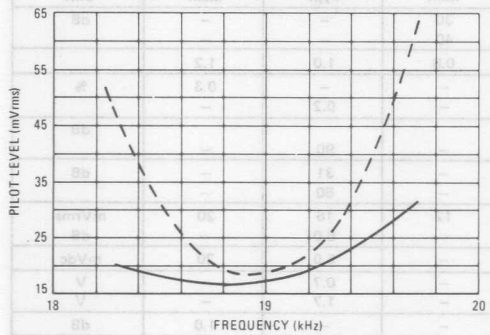


FIGURE 5 – SUPPLY RIPPLE REJECTION versus SUPPLY VOLTAGE

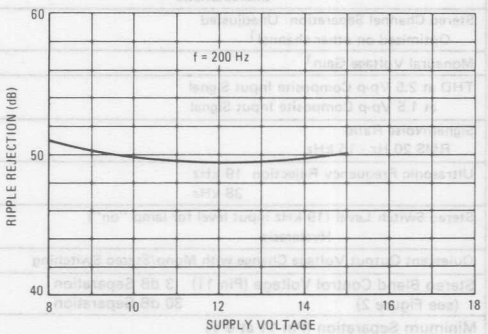


FIGURE 6 – THD versus COMPOSITE INPUT LEVEL

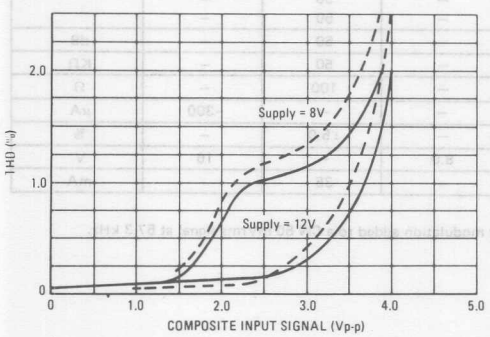
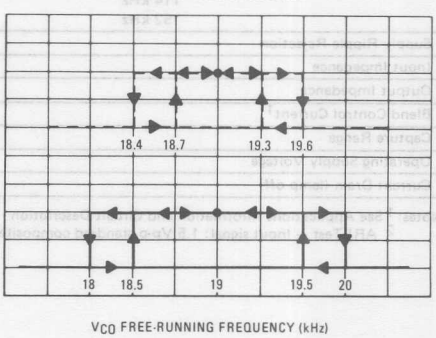


FIGURE 7 – CAPTURE and HOLDING RANGE WITH 20 mV PILOT LEVEL



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FIGURE 8 – CHANNEL SEPARATION versus FREQUENCY

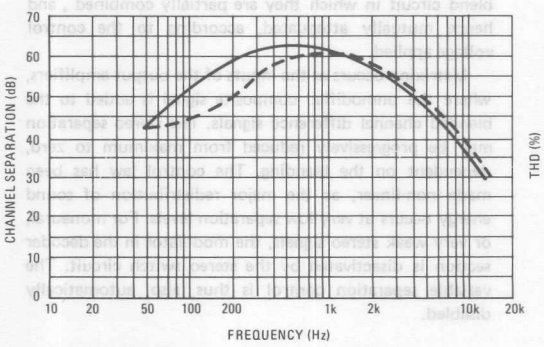


FIGURE 9 – THD versus FREQUENCY

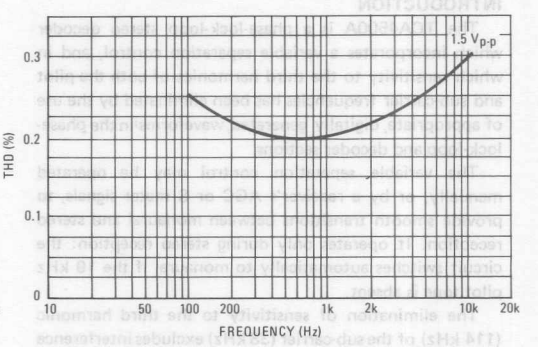
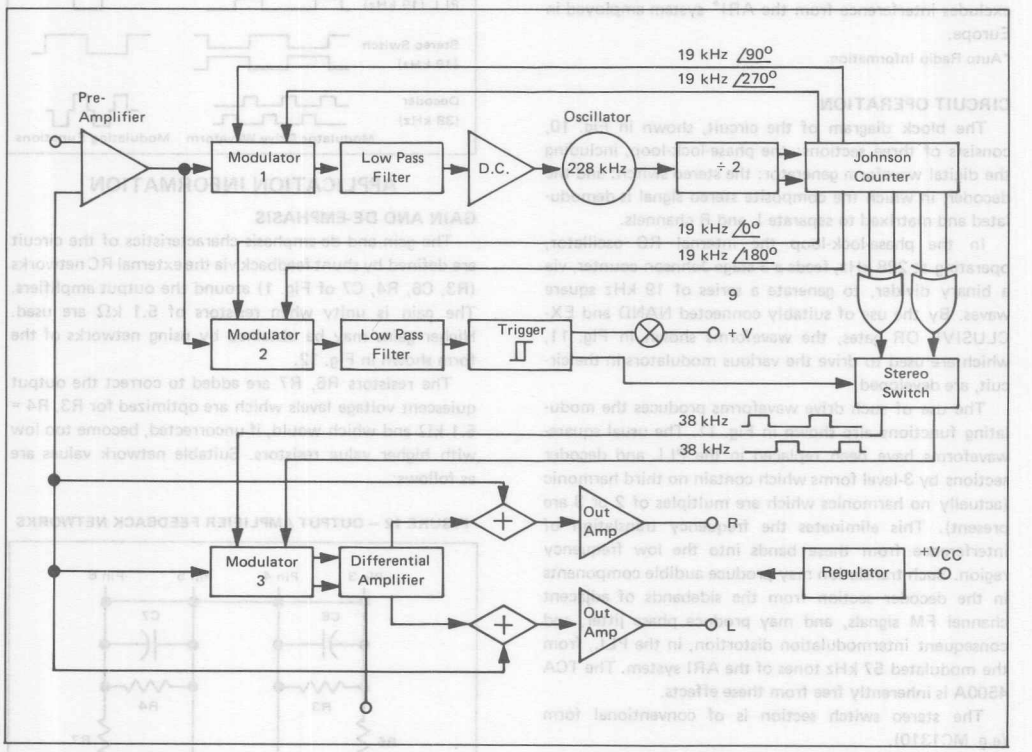


FIGURE 10 – SYSTEM BLOCK DIAGRAM



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CIRCUIT DESCRIPTION

INTRODUCTION

The TCA4500A is a phase-lock-loop stereo decoder which incorporates a variable separation control, and in which sensitivity to the third harmonics of both the pilot and sub-carrier frequencies has been eliminated by the use of appropriate, digitally generated, waveforms in the phase-lock-loop and decoder sections.

The variable separation control may be operated manually, or by a receiver's AGC or S meter signals, to provide smooth transitions between monaural and stereo reception. It operates only during stereo reception: the circuit switches automatically to monaural if the 19 kHz pilot tone is absent.

The elimination of sensitivity to the third harmonic (114 kHz) of the sub-carrier (38 kHz) excludes interference from the 100 kHz (European Spacing) spaced side bands of adjacent transmitters, while elimination of sensitivity to the third harmonic (57 kHz) of the pilot tone (19 kHz) excludes interference from the ARI* system employed in Europe.

*Auto Radio Information.

CIRCUIT OPERATION

The block diagram of the circuit, shown in Fig. 10, consists of three sections: the phase-lock-loop, including the digital waveform generator: the stereo switch: and the decoder, in which the composite stereo signal is demodulated and matrixed to separate L and R channels.

In the phase-lock-loop the internal RC oscillator, operating at 228 kHz, feeds a 3 stage Johnson counter, via a binary divider, to generate a series of 19 kHz square waves. By the use of suitably connected NAND and EX-CLUSIVE OR gates, the waveforms shown in Fig. 11, which are used to drive the various modulators in the circuit, are developed.

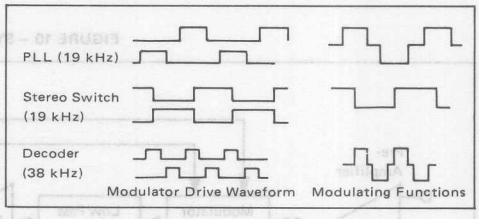
The use of such drive waveforms produces the modulating functions also shown in Fig. 11. The usual square-waveforms have been replaced in the PLL and decoder sections by 3-level forms which contain no third harmonic (actually no harmonics which are multiples of 2 or 3 are present). This eliminates the frequency translation of interference from these bands into the low frequency region. Such translation may produce audible components in the decoder section from the sidebands of adjacent channel FM signals, and may produce phase jitter, and consequent intermodulation distortion, in the PLL, from the modulated 57 kHz tones of the ARI system. The TCA 4500A is inherently free from these effects.

The stereo switch section is of conventional form (e.g. MC1310).

The decoder section consists of a modulator (driven by the waveforms shown in Fig. 11) whose outputs are the inverted and non-inverted channel difference signals. These signals pass to the output amplifiers via the variable blend circuit in which they are partially combined , and hence mutually attenuated, according to the control voltage applied.

Matrixing occurs at the inputs of the output amplifiers, where the unmodified composite signal is added to the blended channel difference signals. The stereo separation may be progressively reduced from maximum to zero, dependent on the blending. The control law has been made non-linear, as the major redistribution of sound energy occurs at very low separation levels. For monaural, or very weak stereo signals, the modulator in the decoder section is disactivated by the stereo switch circuit. The variable separation control is thus, also, automatically disabled.

FIGURE 11 – DIGITAL WAVEFORM



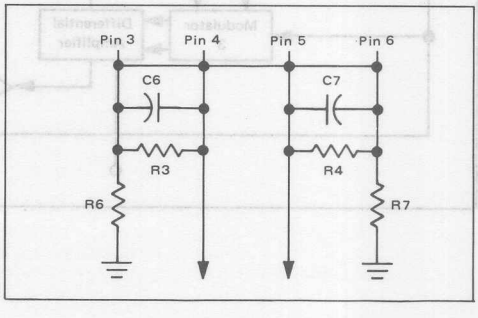
APPLICATION INFORMATION

GAIN AND DE-EMPHASIS

The gain and de-emphasis characteristics of the circuit are defined by shunt feedback via the external RC networks (R3, C6, R4, C7 of Fig. 1) around the output amplifiers. The gain is unity when resistors of 5.1 kΩ are used. Higher gains may be obtained by using networks of the form shown in Fig. 12.

The resistors R6, R7 are added to correct the output quiescent voltage levels which are optimized for R3, R4 = 5.1 kΩ and which would, if uncorrected, become too low with higher value resistors. Suitable network values are as follows:

FIGURE 12 – OUTPUT AMPLIFIER FEEDBACK NETWORKS



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APPLICATION INFORMATION (continued)

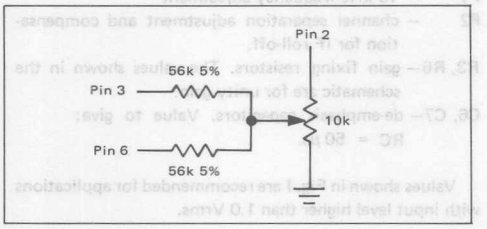
Gain (dB)	R3, R4	C6, C7		R6, R7
		50 μs	75 μs	
0	5.1kΩ	10 nF	15 nF	
3	6.8kΩ	6.8 nF	10 nF	47k ±10%
6	10k	4.7 nF	6.8 nF	27k ±10%

The maximum output level is 1 Vrms; consequently the max. input is limited to 1.4 Vp-p if the gain is set to 6 dB.

SEPARATION ADJUSTMENT

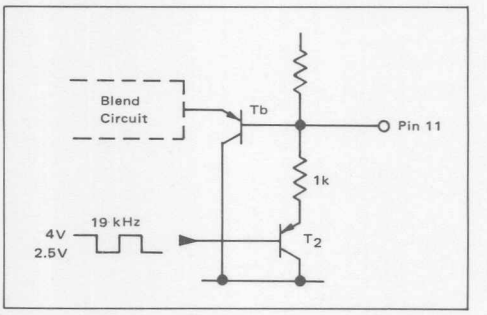
A separation adjustment may be added, as shown below, (Fig. 13), to compensate for the receiver's IF characteristics.

FIGURE 13 – NETWORK PROVIDING ADJUSTABLE SEPARATION



This network reduces the amplification of the channel sum signal in the decoder, to compensate the attenuation of the channel difference signal in the receiver's IF section. The network shown will compensate for up to 2 dB attenuation at 38 kHz. The decoder gain is, obviously, reduced by an amount equal to the compensation required. When used as described, the adjustment also corrects the inherent separation of the decoder, which may be optimized on one channel. Optimization of both channels is possible if separate potentiometers are used to feed each output amplifier.

FIGURE 14 – BLEND CONTROL INPUT CIRCUIT



VARIABLE SEPARATION (BLEND) CONTROL AND 19 kHz OUTPUT

To retain the 16-pin package, the blend control has been combined with the 19 kHz output on pin 11. The internal circuit providing this combination is shown in Fig.14.

If pin 11 is left open-circuit, the 19 kHz signal appears at a mean dc level of 4 V. The blend circuit is inoperative at this level and the decoder provides full separation. The 19 kHz signal can be used to tune the internal oscillator.

To reduce the separation, the voltage on pin 11 is lowered. At 3.2 V, T2 ceases conduction and the 19 kHz signal disappears.

At 2.3 V, the blend circuit comes into operation and the separation decreases according to the curve shown in Fig. 15.

FIGURE 15 – SEPARATION CONTROL VOLTAGE

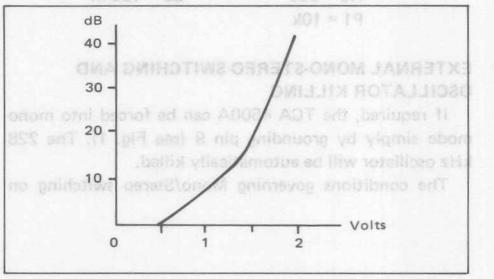
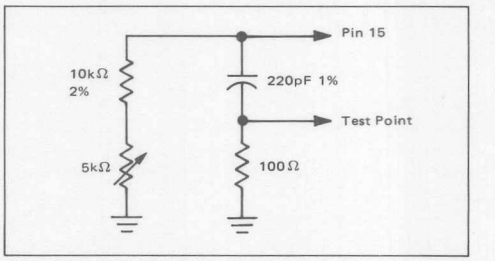


FIGURE 16 – OSCILLATOR NETWORK FOR DIRECT FREQUENCY MEASUREMENT



OSCILLATOR TUNING

If the variable separation facility is not required, pin 11 is left open-circuit and the 19 kHz signal which then appears may be used to indicate the oscillator frequency. If the variable separation is used, and the drive circuit prevents access to the 19 kHz signal, then the oscillator frequency must be measured directly. A test point should be obtained by modifying the oscillator RC network as shown in Fig. 16.

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The output is a pulse train of approximately 1.5 Volts amplitude. Connecting frequency counters of up to 300 pF input capacitance produces less than 0.3% change of the oscillator frequency, which should be set to 228 kHz.

HIGH LOOP GAIN COMPONENTS

For applications demanding operation under low pilot level (e.g., car radio) the following component changes to Fig. 1 are recommended.

R1 = 12k	C3 = 150 pF
R2 = 1.5k	C4 = 330 nF
R8 = 330	C5 = 150 nF
P1 = 10k	

EXTERNAL MONO-STEREO SWITCHING AND OSCILLATOR KILLING

If required, the TCA 4500A can be forced into mono mode simply by grounding pin 9 (see Fig. 1). The 228 kHz oscillator will be automatically killed.

The conditions governing Mono/Stereo switching on pin 9 are the following:

- Quiescent voltage: +2.3 Vdc
- Current required to ensure mono operaton (with 100 mVrms pilot level): 10 μA (from pin 9 to ground) Hysteresis: 0.7μA
- Stereo/mono switching and oscillator killing: less than +500 mV
- Maximum stray capacitance between pin 9 and ground: 100 pF

EXTERNAL COMPONENT FUNCTIONS

P1 – 19 kHz frequency adjustment

P2 – channel separation adjustment and compensation for IF roll-off.

R3, R6 – gain fixing resistors. The values shown in the schematic are for unity gain.

C6, C7 – de-emphasis capacitors. Value to give: RC = 50 μs.

Values shown in Fig. 1 are recommended for applications with input level higher than 1.0 Vrms.

MOTOROLA

TCA5550

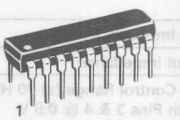
STEREO SOUND CONTROL SYSTEM

STEREO SOUND CONTROL SYSTEM

SILICON MONOLITHIC INTEGRATED CIRCUIT

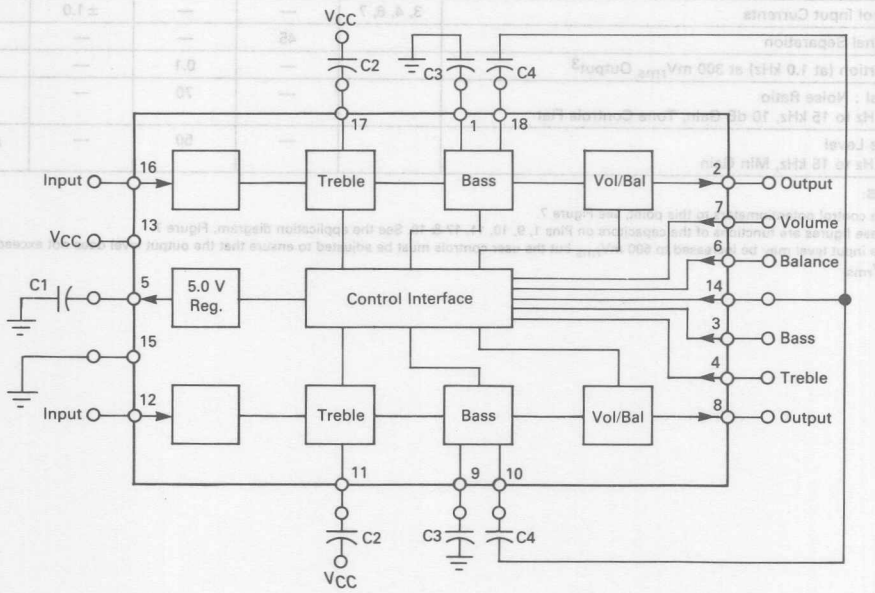
The TCA5550 is a single chip stereo balance, volume, bass and treble control circuit designed for use in car radios, TV, and audio systems. Simple dc inputs allow the control to be effected by four inexpensive potentiometers or a remote control system. The bass and treble responses are defined by a single capacitor per control per channel.

- Four High Impedance dc Controls — Vol, Bass, Treble, Balance
- A Single External Capacitor Defines Each Tone Control Characteristic
- Low Distortion, 0.1% at Nominal Input Level, Unity Gain with the Tone Controls Flat
- Channel Separation Better Than 45 dB
- Wide Power Supply Tolerance, 10 to 16 Vdc
- ± 14 dB of Tone Control
- More Than 75 dB of Volume Control
- Wide Dynamic Range: 100 mV to 500 mV_{rms} Input Signal
- Low Output Impedance



P SUFFIX
PLASTIC PACKAGE
CASE 707-02

FIGURE 1 — BLOCK DIAGRAM



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MAXIMUM RATINGS (T_A = +25°C)

Rating	Value	Unit
Power Supply Voltage	18	Volts
Power Dissipation (Package Limitation) Derate above T_A = +25°C	1250 10	mW mW/°C
Operating Temperature Range (Ambient)	−40 to +85	°C
Storage Temperature Range	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 12 Vdc)

Characteristic		Pin	Min	Typ	Max	Unit
Supply Voltage		13	10	—	16	Vdc
Supply Current	Min Gain		—	30	—	mA
	Max Gain		—	15	—	
Regulated Output		5				
Voltage[1]			—	5.0	—	V
Current			—	—	3.0	mA
Input Levels	Max Gain	12, 16	—	100	—	mV_{rms}
	With Reduced Gain[3]		—	—	500	
Input Impedance		12, 16	—	100	—	kΩ
Output Impedance		2, 8	—	300	—	Ω
Tone Control Range (at 70 Hz & 10 kHz)[2]		3,4				dB
With Pins 3 & 4 @ 0.5 V			—	−14	—	
With Pins 3 & 4 @ 2.3 V			—	0	—	
With Pins 3 & 4 @ 4.1 V			—	+14	—	
Balance Control Range	Min Gain	6	—	−35	—	dB
(Constant Power Law)	Max Gain		—	+3.0	—	dB
Voltage on Pin 6 for Balanced Gain			—	2.3	—	V
Volume Control Range		7	—	80	—	dB
With Pin 7 @ 0 V			—	+10	—	
With Pin 7 @ 3.1 V			—	−20	—	
With Pin 7 @ $V_{PIN\ 5}$			—	−70	—	
Control Input Currents		3, 4, 6, 7	—	—	±1.0	μA
Channel Separation			45	—	—	dB
Distortion (at 1.0 kHz) at 300 mV_{rms} Output[3]			—	0.1	—	%
Signal : Noise Ratio 50 Hz to 15 kHz, 10 dB Gain, Tone Controls Flat			—	70	—	dB
Noise Level 50 Hz to 15 kHz, Min Gain			—	50	—	μV_{rms}

NOTES:

1. The control potentiometers to this point, see Figure 7.
2. These figures are functions of the capacitors on Pins 1, 9, 10, 11, 17 & 18. See the application diagram, Figure 7.
3. The input level may be increased to 500 mV_{rms} but the user controls must be adjusted to ensure that the output level does not exceed 300 mV_{rms}.

PERFORMANCE CHARACTERISTICS, FIGURES 2–7, TAKEN IN CIRCUIT OF FIGURE 8, V_{CC} = 12 V

FIGURE 2 — MIDBAND DISTORTION

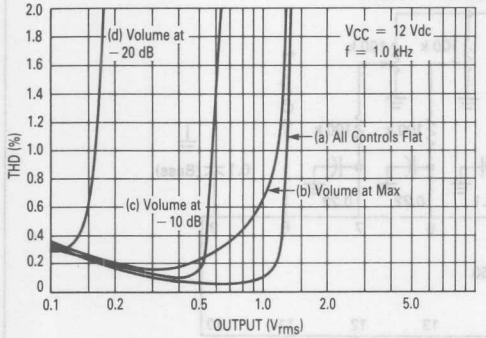


FIGURE 3 — VOLUME CONTROL CHARACTERISTICS

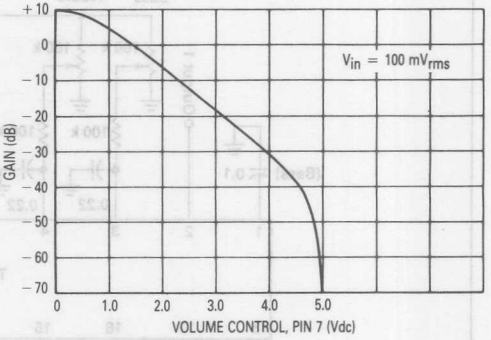


FIGURE 4 — TONE CONTROL CHARACTERISTICS

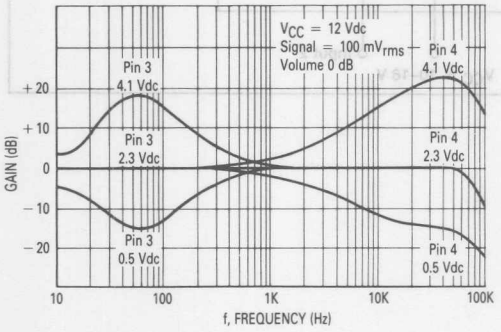


FIGURE 5 — HIGH FREQUENCY DISTORTION

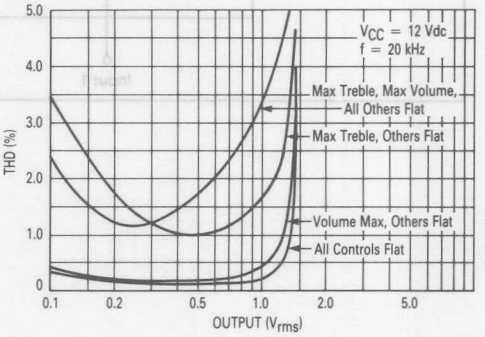


FIGURE 6 — LOW FREQUENCY DISTORTION

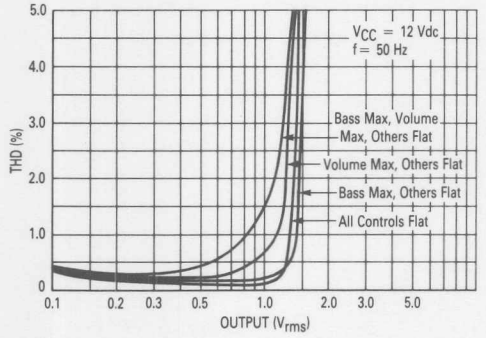
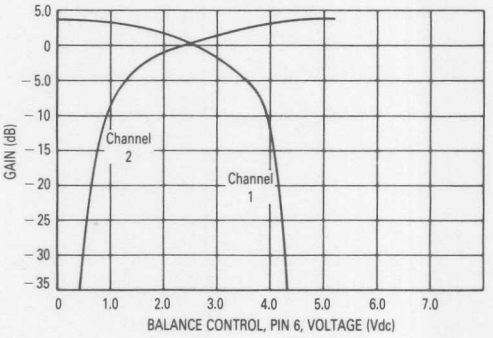
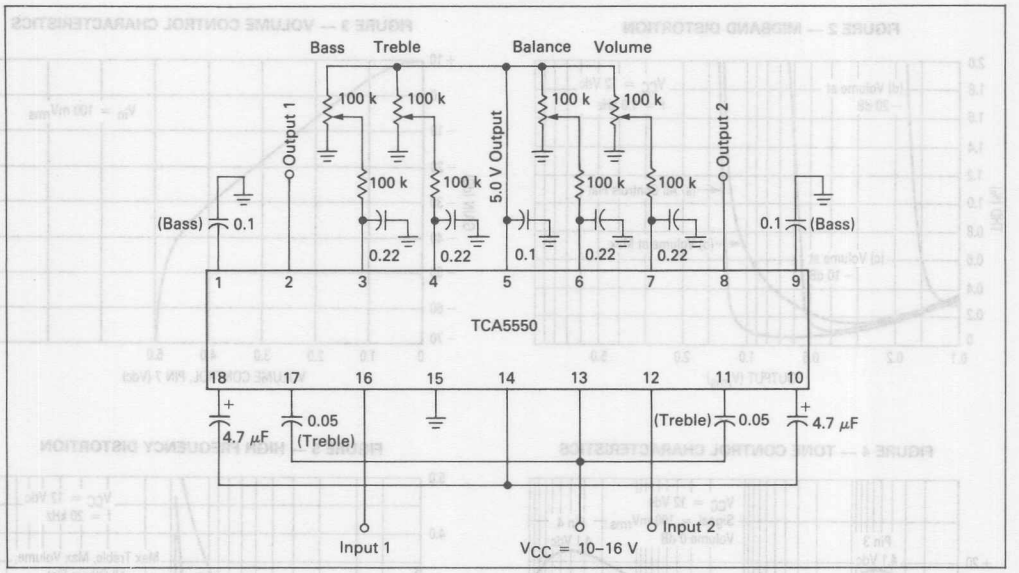


FIGURE 7 — BALANCE CONTROL CHARACTERISTIC



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FIGURE 8 — APPLICATION CIRCUIT



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MOTOROLA

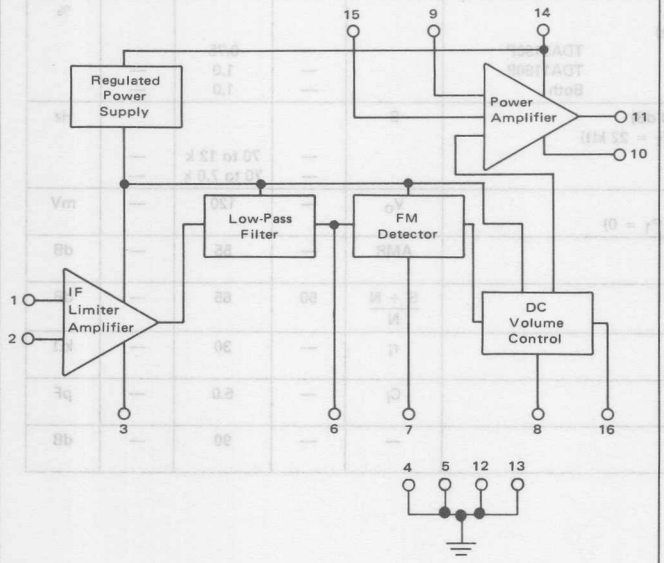
TDA1190P
TDA3190P

TV SOUND SYSTEM

The TDA3190P 4.2-watt sound system is designed for television and related applications. The TDA1190P is a low-power version. Functions performed by these devices include: IF Limiting, IF amplifier, low pass filter, FM detector, DC volume control, audio preamplifier, and audio power amplifier.

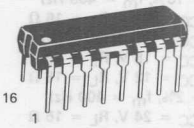
- 4.2 Watts Output Power — TDA3190P (V_{CC} = 24 V, R_L = 16 Ω)
- 1.3 Watts Output Power — TDA1190P (V_{CC} = 18 V, R_L = 32 Ω)
- Linear Volume Control
- High AM Rejection
- Low Harmonic Distortion
- High Sensitivity

BLOCK DIAGRAM

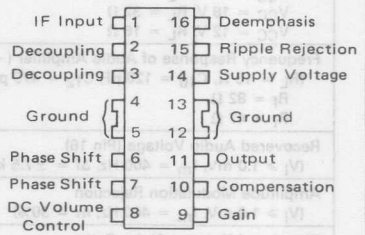


TV SOUND SYSTEM

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 648C-02



ORDERING INFORMATION

Device	Temperature Range	Package
Both Devices	0 to +75°C	Plastic

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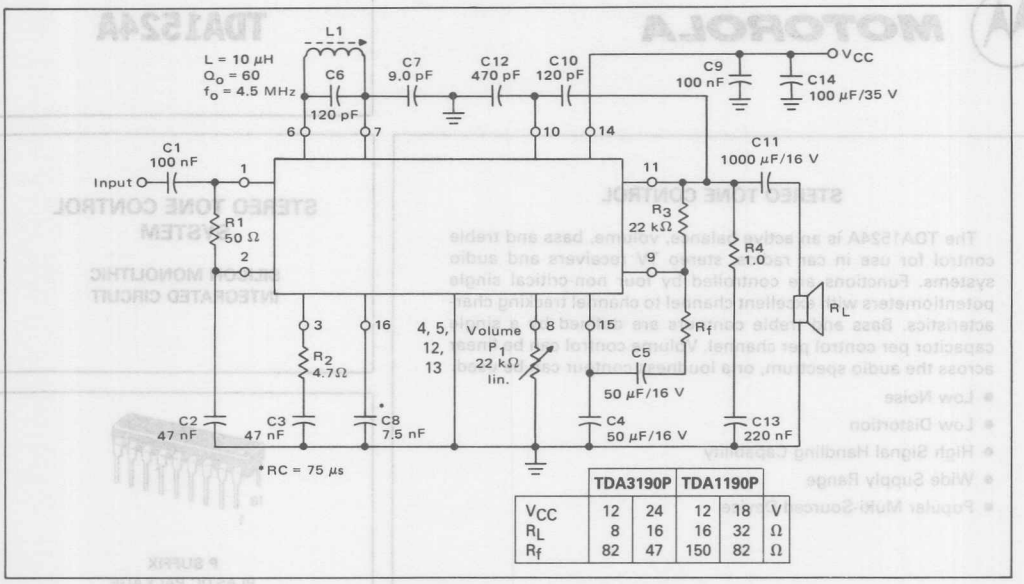
MAXIMUM RATINGS

Rating	Symbol	TDA3190P	TDA1190P	Unit
Supply Voltage Range	V_{CC}	9.0 to 28	9.0 to 22	V
Output Peak Current (Nonrepetitive) (Repetitive)	I_o	2.0 1.5	1.5 1.0	A
Input Signal Voltage	V_I	1.0		V
Operating Temperature Range	T_A	0 to +75		°C
Junction Temperature	T_J	150		°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 V, f_o = 4.5 MHz, Δf = ±25 kHz, T_A = 25°C unless otherwise noted.)

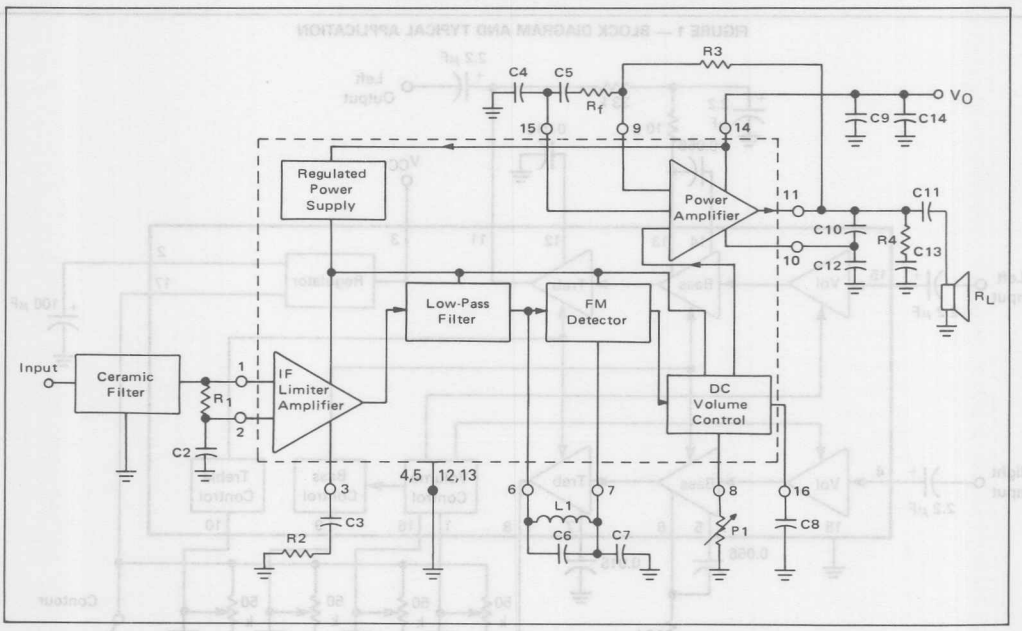
Characteristic		Symbol	Min	Typ	Max	Unit
Quiescent Output Voltage (Pin 11)		V_O				V
V_{CC} = 24 V	TDA3190P		11	12	13	
V_{CC} = 18 V	TDA1190P		8.0	9.0	10	
V_{CC} = 12 V	Both		5.1	6.0	6.9	
Quiescent Drain Current		I_D				mA
(P1 = 22 kΩ)						
V_{CC} = 24 V	TDA3190P		11	22	35	
V_{CC} = 18 V	TDA1190P		11	22	35	
V_{CC} = 12 V	Both		—	19	—	
Output Power		P_O				W
(d = 10%, f_m = 400 Hz)						
V_{CC} = 24 V, R_L = 16 Ω	TDA3190P		—	4.2	—	
V_{CC} = 12 V, R_L = 8.0 Ω	TDA3190P		—	1.5	—	
V_{CC} = 18 V, R_L = 32 Ω	TDA1190P		1.0	1.3	—	
V_{CC} = 12 V, R_L = 16 Ω	TDA1190P		0.7	0.9	—	
(d = 2%, f_m = 400 Hz)						
V_{CC} = 24 V, R_L = 16 Ω	TDA3190P		—	3.5	—	
V_{CC} = 12 V, R_L = 8.0 Ω	TDA3190P		—	1.4	—	
V_{CC} = 18 V, R_L = 32 Ω	TDA1190P		—	1.0	—	
V_{CC} = 12 V, R_L = 16 Ω	TDA1190P		—	0.7	—	
Input Limiting Threshold Volts (−3.0 dB) at Pin 1		V_I				μV
Δf = ±7.5 kHz, f_m = 400 Hz, Set P1 for 2.0 Vrms on Pin 11						
	TDA3190P		—	40	100	
	TDA1190P		—	60	100	
Distortion						%
(P_O = 50 mW, f_m = 400 Hz, Δf = ±7.5 kHz)						
V_{CC} = 24 V, R_L = 16 Ω	TDA3190P		—	0.75	—	
V_{CC} = 18 V, R_L = 32 Ω	TDA1190P		—	1.0	—	
V_{CC} = 12 V, R_L = 16 Ω	Both		—	1.0		
Frequency Response of Audio Amplifier (−3.0 dB)		B				Hz
(R_L = 16 Ω, C_{10} = 120 pF, C_{12} = 470 pF, P_1 = 22 kΩ)						
R_f = 82 Ω			—	70 to 12 k	—	
R_f = 47 Ω			—	70 to 7.0 k	—	
Recovered Audio Voltage (Pin 16)		V_o	—	120	—	mV
(V_I ≥ 1.0 mV, f_m = 400 Hz, Δf = ±7.5 kHz, P_1 = 0)						
Amplitude Modulation Rejection		AMR	—	55	—	dB
(V_I ≥ 1.0 mV, f_m = 400 Hz, m = 30%)						
Signal and Noise to Noise Ratio		$\frac{S+N}{N}$	50	65	—	dB
(V_I ≥ 1.0 mV, V_o = 4.0 V, f_m = 400 Hz)						
Input Resistance (Pin 1)		r_i	—	30	—	kΩ
(V_I = 1.0 mV)						
Input Capacitance (Pin 1)		C_i	—	5.0	—	pF
(V_I = 1.0 mV)						
DC Volume Control Attenuation		—	—	90	—	dB
(P1 = 12 kΩ)						

TEST CIRCUIT



	TDA3190P		TDA1190P		
V_{CC}	12	24	12	18	V
R_L	8	16	16	32	Ω
R_f	82	47	150	82	Ω

TYPICAL CIRCUIT CONFIGURATION



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MOTOROLA

TDA1524A

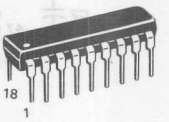
STEREO TONE CONTROL

The TDA1524A is an active balance, volume, bass and treble control for use in car radios, stereo TV receivers and audio systems. Functions are controlled by four non-critical single potentiometers with excellent channel to channel tracking characteristics. Bass and treble contours are defined by a single capacitor per control per channel. Volume control can be linear across the audio spectrum, or a loudness contour can be used.

- Low Noise
- Low Distortion
- High Signal Handling Capability
- Wide Supply Range
- Popular Multi-Sourced Device

STEREO TONE CONTROL SYSTEM

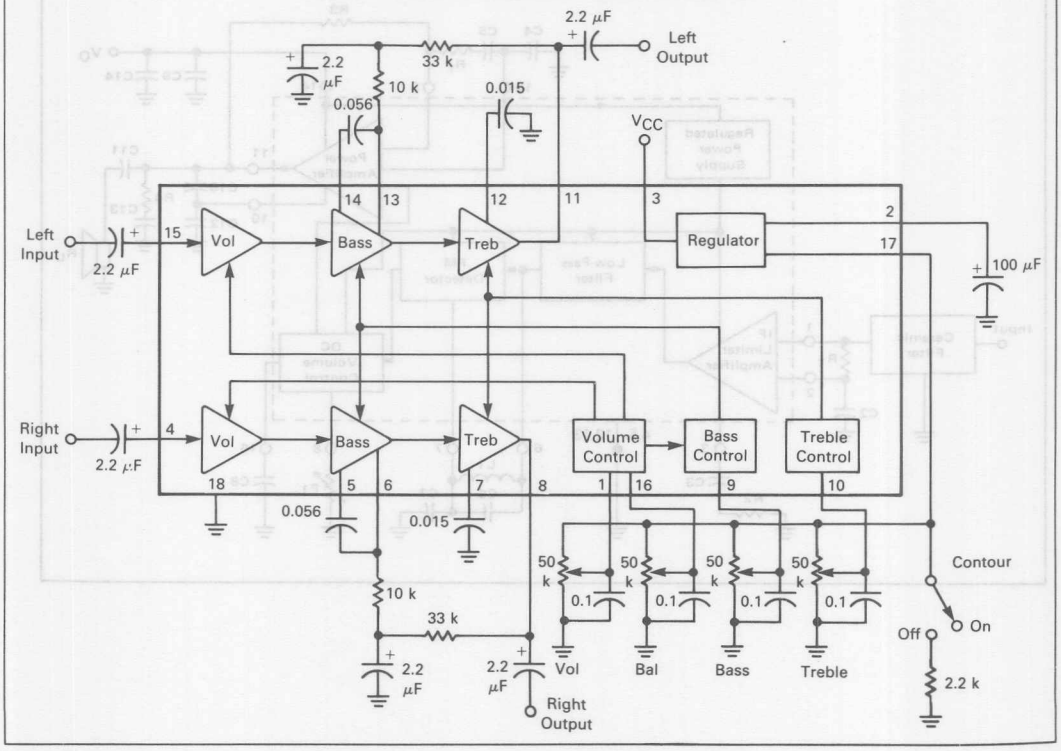
SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 707-02

9

FIGURE 1 — BLOCK DIAGRAM AND TYPICAL APPLICATION



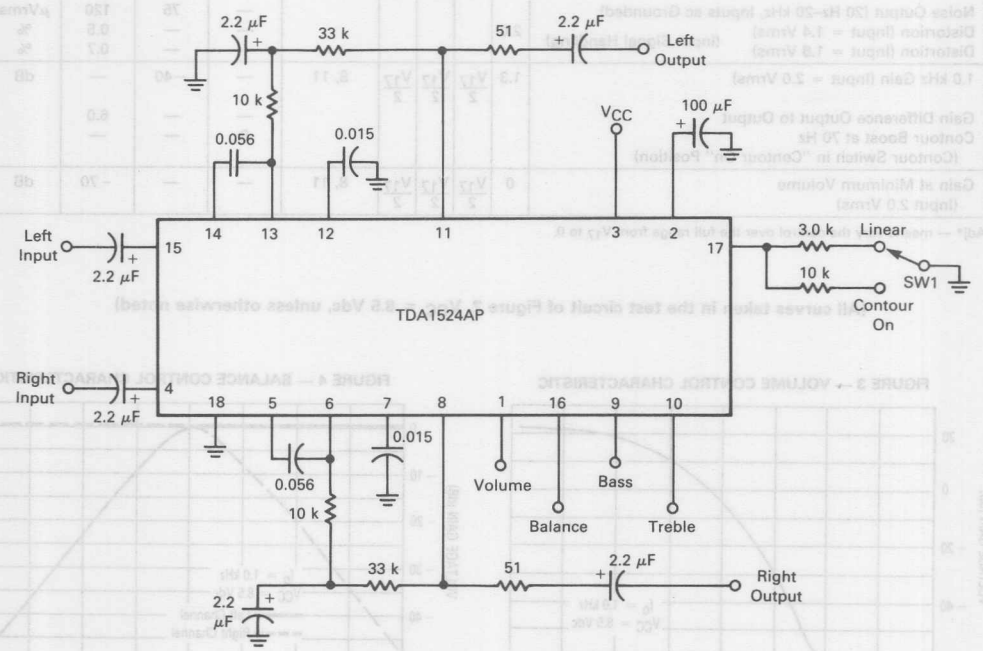
MAXIMUM RATINGS (T_A = +25°C)

Rating	Value	Units
Power Supply Voltage	20	V
Power Dissipation Derate above 25°C	1250 10	mW mW/°C
Operating Temperature Range	−40 to +85	°C
Storage Temperature Range	−65 to +150	°C

DC CHARACTERISTICS (T_A = 25°C, circuit of Figure 2, SW1 at "contour on", V_1, V_9, V_{10}, V_{16} = 1.9 V, unless otherwise noted)

Characteristic	Pin	V_{CC} (Vdc)	Min	Typ	Max	Units
Supply Voltage, V_{CC}	3	—	7.5	—	16.5	Vdc
Supply Current	3	8.5 12 15	19 — —	27 35 43	35 — —	mA
DC Input Level	4, 15	8.5 12 15	3.8 — —	4.25 5.9 7.3	4.7 — —	Vdc
DC Output Level	8, 11	8.5 12 15	3.3 — —	4.25 6.0 7.5	5.2 — —	Vdc
Regulator Output Voltage	17	8.5 12 15	3.5 — —	3.75 3.8 3.85	4.0 — —	Vdc
Regulator Output Voltage, SW1 in "Linear" Position	17	8.5	3.5	3.75	4.0	Vdc

FIGURE 2 — TEST CIRCUIT



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frequency 1.0 kHz, gains expressed as 20 log [voltage ratio] unless otherwise noted)

Characteristic	V_1	V_9	V_{10}	V_{16}	Measure Pin(s)	Min	Typ	Max	Units
Gain at Max Volume Control (Input = 50 mVrms)	V_{17}	$\frac{V_{17}}{2}$	$\frac{V_{17}}{2}$	$\frac{V_{17}}{2}$	8, 11	20	20	24	dB
Distortion at 1.8 Vrms Output (Output signal handling)					8, 11	—	—	0.5	%
AC Input Resistance					4, 15	10	—	—	kΩ
Output to Output Separation, One Input Driven (100 mVrms)					8, 11	60	—	—	dB
Noise Output (20 Hz–20 kHz, Inputs are Grounded)					8, 11	—	250	400	μVrms
Gain at Mid Volume, Left Channel (Input = 100 mVrms)	$\frac{V_{17}}{2}$	$\frac{V_{17}}{2}$	$\frac{V_{17}}{2}$	$\frac{V_{17}}{2}$	8, 11	−12	−9.0	−6.0	dB
Gain Difference Left to Right						—	—	1.5	
70 Hz Gain Difference Output to Output (Input = 100 mVrms)	2.1	$\frac{V_{17}}{2}$	$\frac{V_{17}}{2}$	$\frac{V_{17}}{2}$	8, 11	—	—	2.5	dB
70 Hz Gain at Mid Bass Setting (Input = 100 mVrms)						—	0	—	
70 Hz Bass Control — Boost		V_{17}				10	—	—	
— Cut		0				10	—	—	
16 kHz Gain at Mid Treble Setting (Input = 100 mVrms)	2.1	$\frac{V_{17}}{2}$	$\frac{V_{17}}{2}$	$\frac{V_{17}}{2}$	8, 11	—	0	—	dB
16 kHz Gain Difference Output to Output						—	—	2.5	
16 kHz Treble Control — Boost			V_{17}			12	—	—	
— Cut			0			12	—	—	
Balance Control Range of Right Channel				Adj*	8	35	—	—	dB
Balance Control Range of Left Channel	2.1	$\frac{V_{17}}{2}$	$\frac{V_{17}}{2}$	Adj*	11	35	—	—	dB
Output Ripple (No Signal, 200 mVrms @ 120 Hz Added to V_{CC})				$\frac{V_{17}}{2}$	8, 11	—	—	3.5	mVrms
1.0 kHz Gain (Input = 1.8 Vrms)	1.6	$\frac{V_{17}}{2}$	$\frac{V_{17}}{2}$	$\frac{V_{17}}{2}$	8, 11	—	−20	—	dB
Noise Output (20 Hz–20 kHz, Inputs ac Grounded)						—	75	120	μVrms
Distortion (Input = 1.4 Vrms) (Input Signal Handling)	2.0					—	—	0.5	%
Distortion (Input = 1.8 Vrms)						—	—	0.7	%
1.0 kHz Gain (Input = 2.0 Vrms)	1.3	$\frac{V_{17}}{2}$	$\frac{V_{17}}{2}$	$\frac{V_{17}}{2}$	8, 11	—	−40	—	dB
Gain Difference Output to Output						—	—	6.0	
Contour Boost at 70 Hz (Contour Switch in "Contour On" Position)						8	—	—	
Gain at Minimum Volume (Input 2.0 Vrms)	0	$\frac{V_{17}}{2}$	$\frac{V_{17}}{2}$	$\frac{V_{17}}{2}$	8, 11	—	—	−70	dB

Adj* — means vary the control over the full range from V_{17} to 0.

(All curves taken in the test circuit of Figure 2, V_{CC} = 8.5 Vdc, unless otherwise noted)

FIGURE 3 — VOLUME CONTROL CHARACTERISTIC

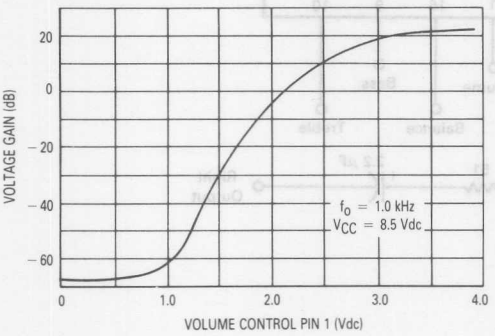


FIGURE 4 — BALANCE CONTROL CHARACTERISTIC

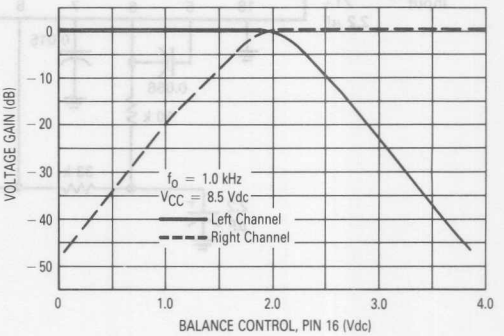


FIGURE 5 — BASS CONTROL CHARACTERISTIC

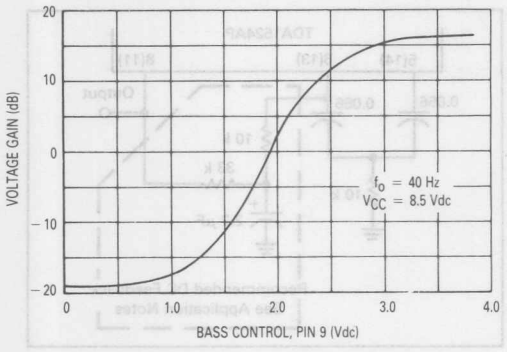


FIGURE 6 — TREBLE CONTROL CHARACTERISTIC

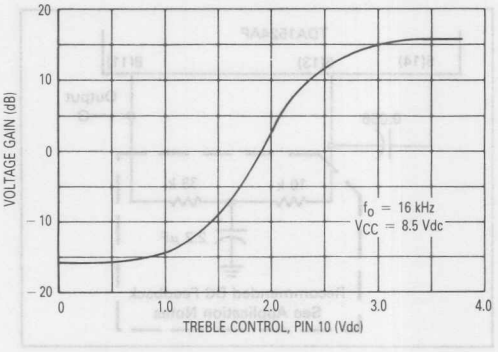


FIGURE 7 — TOTAL HARMONIC DISTORTION versus FREQUENCY

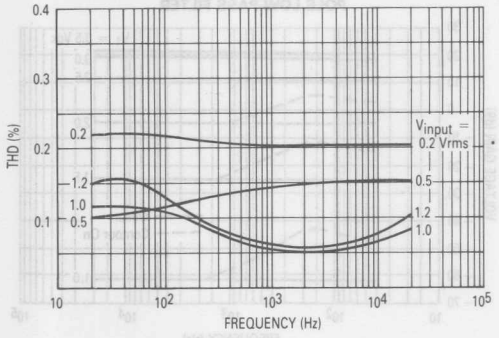


FIGURE 8 — TOTAL HARMONIC DISTORTION versus OUTPUT

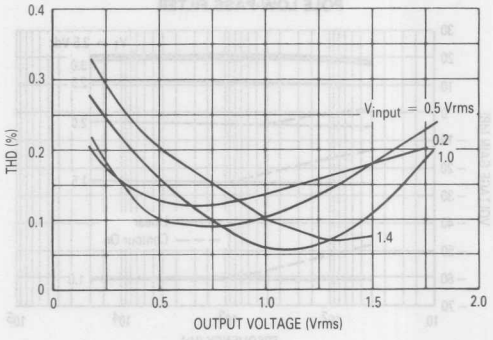


FIGURE 9 — TONE CONTROL RESPONSE WITH SINGLE POLE LOW-PASS FILTER

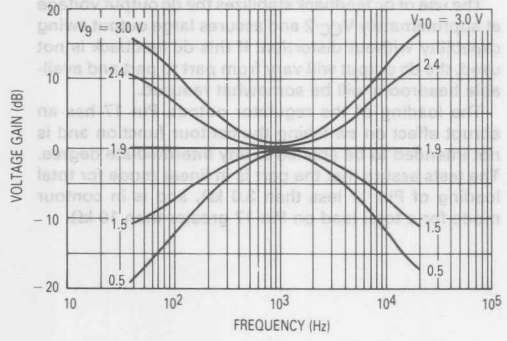
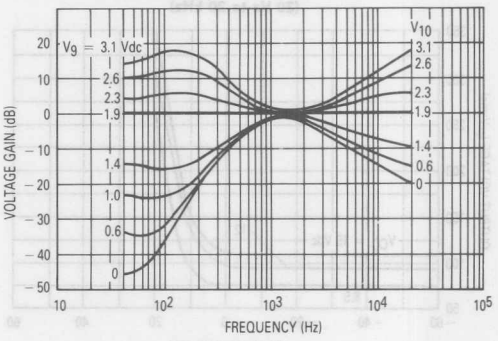


FIGURE 10 — TONE CONTROL RESPONSE WITH DOUBLE POLE LOW-PASS FILTER



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FIGURE 11 — SINGLE POLE LOW-PASS FILTER

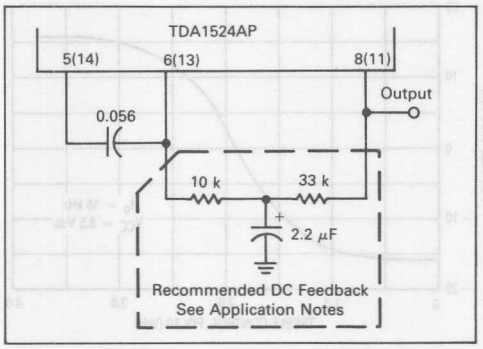


FIGURE 12 — DOUBLE POLE LOW-PASS FILTER

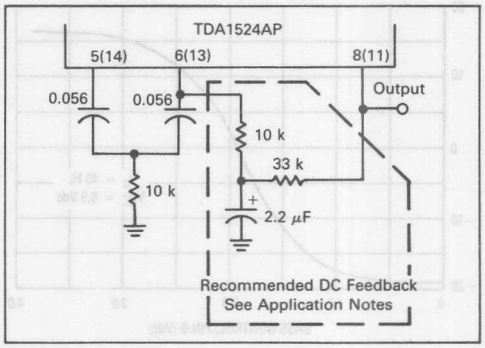


FIGURE 13 — VOLUME CONTROL RESPONSE WITH SINGLE POLE LOW-PASS FILTER

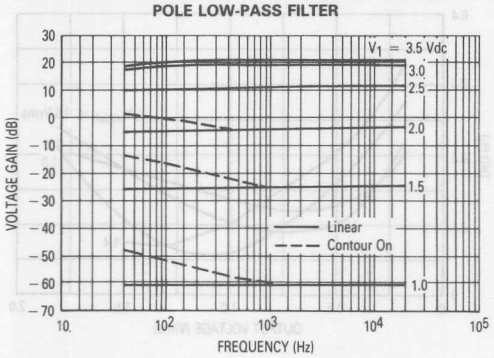
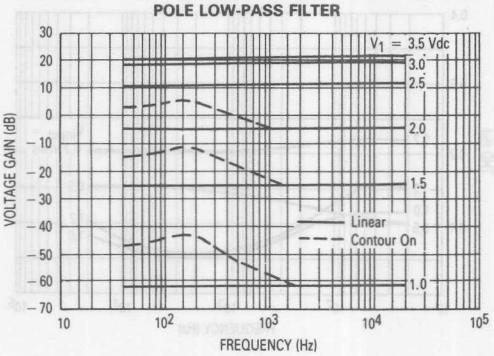
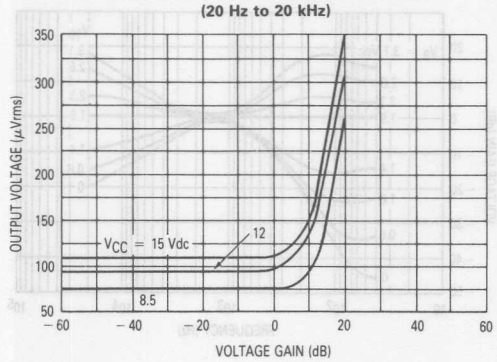


FIGURE 14 — VOLUME CONTROL RESPONSE WITH DOUBLE POLE LOW-PASS FILTER



9

FIGURE 15 — NOISE OUTPUT VOLTAGE (20 Hz to 20 kHz)



APPLICATION NOTES

The use of dc feedback stabilizes the dc output voltage at approximately $V_{CC}/2$ and assures large output swing capability without distortion. If this dc feedback is not used, the dc output will vary from part to part and available headroom will be somewhat reduced.

The loading of the regulator output, Pin 17 has an abrupt effect on switching the contour function and is not intended to be applied in any intermediate degree. The tests assure that the part is in linear mode for total loading of Pin 17 less than 3.0 kΩ, and is in contour mode for a total load on Pin 17 greater than 10 kΩ.

MOTOROLA

TDA3301
TDA3303

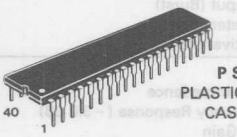
TV COLOR PROCESSOR

These devices will accept a PAL or NTSC composite video signal and output the three color signals, needing only a simple driver amplifier to interface to the picture tube. The provision of high bandwidth on-screen display inputs makes them suitable for text display, TV games, cameras, etc. The TDA3301 differs from the TDA3303 in its user control laws, and also a phase shift control which operates in PAL, as well as NTSC.

- Automatic Black Level Setup
- Beam Current Limiting
- Uses Inexpensive 4.43/3.58 MHz Crystal
- No Oscillator Adjustment Required
- Three OSD Inputs Plus Fast Blanking Input
- Four DC, High Impedance User Controls
- Interfaces with TDA3030B SECAM Adaptor
- Single 12 V Supply
- Low Dissipation, Typically 600 mW

TV COLOR PROCESSOR

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 711-03



FN SUFFIX
PLASTIC PACKAGE
CASE 777-02
PLCC-44

FIGURE 1 — PIN ASSIGNMENT

Chroma Input	1 (1)	(44) 40	Hue Control/NTSC Switch
ACC Capacitor	2 (2)	(43) 39	+12 V
Chroma DL Driver, Emitter	3 (3)	(42) 38	Ground
Chroma DL Driver, Collector	4 (4)	(41) 37	1.0 V Composite Video Input
Saturation Control	5 (5)	(40) 36	Delayed Luma Input
Identification Capacitor	6 (6)	(39) 35	Luma DL Drive and 3.0 Inverted Output
V Input	7 (10)	(38) 34	Luma Emitter Load
U Input	8 (11)	(37) 33	Luma Collector Load
90° Loop Capacitor	9 (12)	(36) 32	Contrast Control
Oscillator Loop Filter	10 (13)	(35) 31	Black Level Clamp
Crystal Drive	11 (14)	(34) 30	Brightness Control
Crystal Feedback	12 (15)	(33) 29	Peak Beam Limit Adjust
Ground	13 (16)	(32) 28	Frame Pulse Input
Blue Output	14 (18)	(31) 27	Sandcastle Pulse Input
Blue Output Clamp Capacitor	15 (19)	(30) 26	OSD Input Green
Blue Output Feedback	16 (20)	(29) 25	OSD Input Red
Green Output	17 (21)	(28) 24	OSD Input Blue
Green Output Clamp Capacitor	18 (22)	(27) 23	OSD Input Fast Blanking
Green Output Feedback	19 (23)	(26) 22	Red Output Feedback
Red Output	20 (24)	(25) 21	Red Output Clamp Capacitor

*( ) PLCC Pin Assignment

9

MAXIMUM RATINGS (T_A = +25°C unless otherwise stated)

Rating	Pin	Value	Unit
Supply Voltage	39	14	Vdc
Operating Temperature Range		0 to +70	°C
Storage Temperature Range		−65 to +150	°C

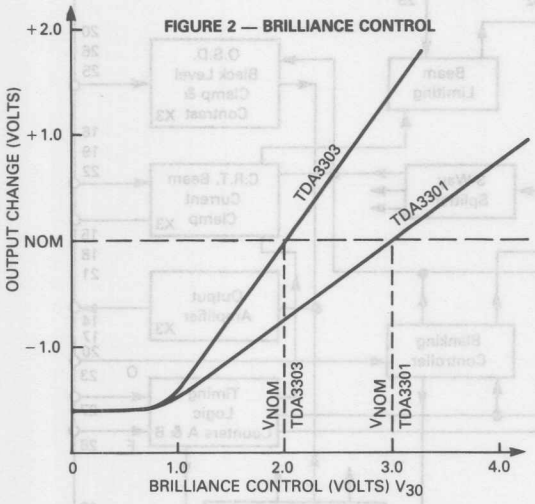
ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 12 V)

Characteristic	Pin	Min	Typ	Max	Unit
Supply Voltage	39	10.8	12	13.2	V
Supply Current		—	45	60	mA
Composite Video Input	37	—	1.0	—	Vp-p
Video Input Resistance		13	18	23	kΩ
Video Gain to Pin 35		2.7	3.2	3.6	Vp-p
Input Window		0.8–3	0.7–3.2	—	V
Chroma Input (Burst)	1	10	100	200	mVp-p
Input Resistance	1	—	5.0	—	kΩ
ACC Effectiveness	4	—	1.2	3.0	dB
OSD Input	24,25,26	0.5	0.7	1.0	V
OSD Drive Impedance		—	—	180	Ω
OSD Frequency Response (−3.0 dB)		9.0	—	—	MHz
OSD Max Gain		—	7.2	—	MHz
Gain Difference Between Any Two		—	—	15	%
Beam Current Ref. Threshold	16,19,22	1.7	2.0	2.3	V
Differential Voltage		—	—	20	mV
Beam Current Ref. Input Current		—	—	+1.5/−0.5	μA
Differential Current		—	—	1.0	μA
Luminance Gain Between Pin 36 and Outputs (depends on R_{33} and R_{34})		—	4.7	—	
Luminance Bandwidth (−3.0 dB)	14,17,20	9.0	—	—	MHz
Output Resistance		120	170	300	Ω
Residual Carrier (4.43 Mc/s)		—	30	150	mVp-p
PAL Offset (H/2)		—	—	50	mVp-p
Difference in Gain Between Y Input and any RGB o/p		—	5.0	—	%
U Input Sensitivity for 5.0 V Blue Output	8	—	340	—	mVp-p
Matrix Error	14,17,20	—	—	10	%
Oscillator Capture Range		350	—	—	Hz
U Ref. Phase Error		—	—	5.0	°
V Ref. Phase Error		—	—	5.0	°
Color Kill Attenuation	14,17,20	50	—	—	dB
Contrast Tracking OSD/Luma/Chroma	14,17,20	—	—	—	dB
OSD Contrast Tracking	14,17,20	—	—	±2.0	dB
OSD Enable Slice Level	23	—	0.7	—	V
Sandcastle Slice Level	27				
Burst Gate		6.5	7.2	8.0	V
Line Blanking		2.0	2.6	3.0	V
R Input V_{27} > 7.0 V		—	5.0	—	kΩ
V_{27} < 7.0 V		—	22	—	kΩ
Frame Slice Level	28	2	2.8	3.6	V
R Input			15	—	kΩ
Peak Beam Limiter Threshold (I_{29} Min = 250 μA)		3.4 x I_{29}	4 x I_{29}	4.6 x I_{29}	
Pin 29 Input Resistance	29	—	5.0	—	kΩ
Pin 29 Open Circuit Voltage	29	—	10.6	—	V

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INPUT/OUTPUT FUNCTIONS

FIGURE 2 — BRILLIANCE CONTROL

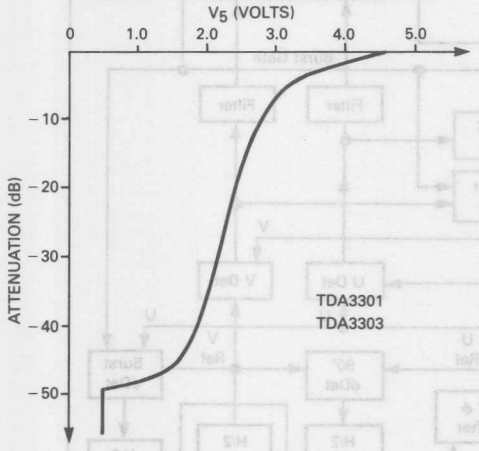


The brilliance control operates by adding a pedestal to the output signals. The amplitude of the pedestal is controlled by Pin 30.

During CRT beam current sampling a standard pedestal is substituted, its value being equivalent to the value given by V_{30} Nom. Brightness at black level with V_{30} Nom is given by the sum of three gun currents at the sampling level, i.e. 3 x 20 μA with 100 k reference resistors on Pins 16, 19, and 22.

During picture blanking the brilliance pedestal is zero; therefore the output voltage during blanking is always the minimum brilliance black level (Note: Signal channels are also gain blanked).

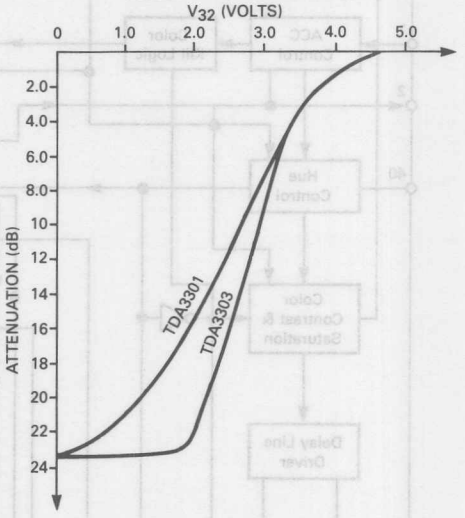
FIGURE 3 — SATURATION CONTROL VOLTAGE



Pin 5 is automatically pulled to ground with a misidentified PAL signal.

Note: Nominal 100% saturation point is given by choice of R_2 which sets ACC operating point.

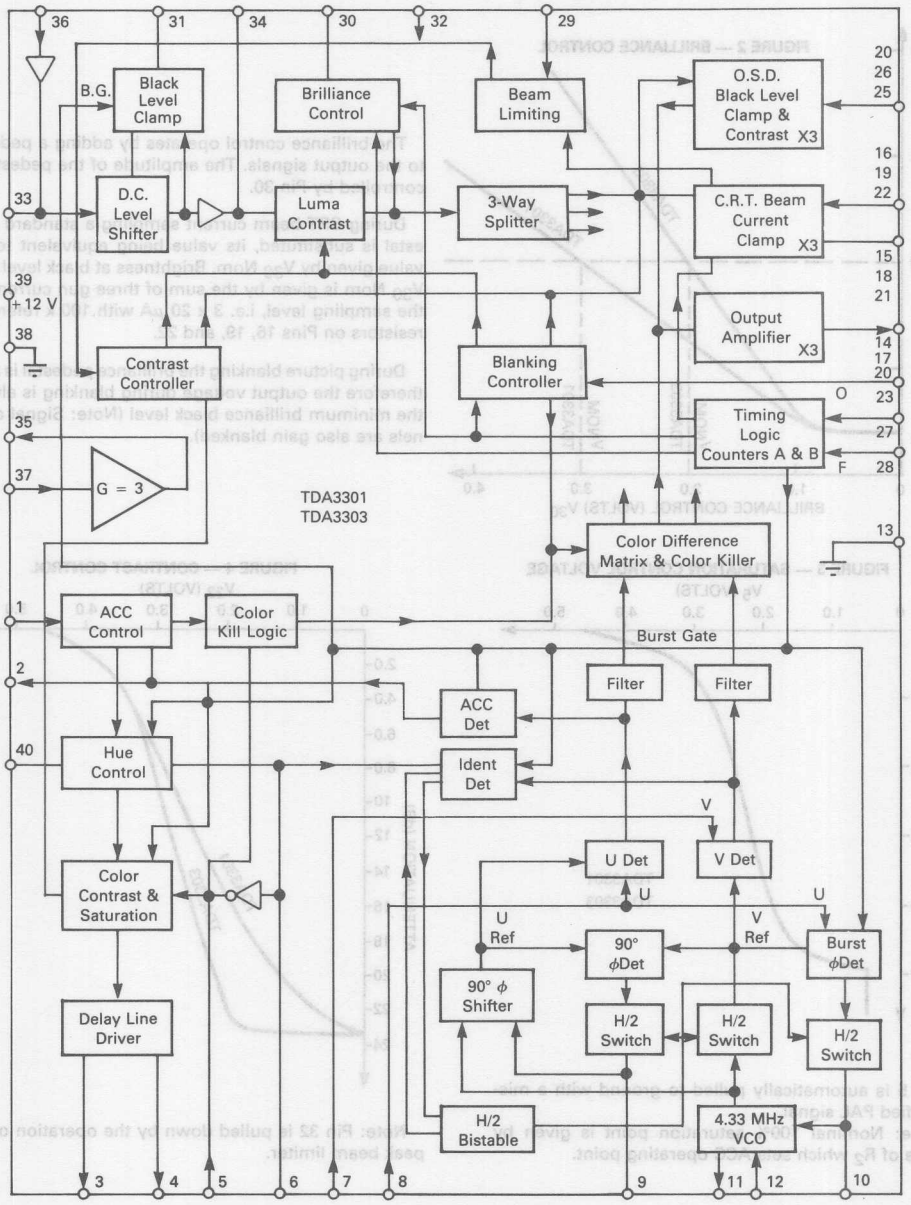
FIGURE 4 — CONTRAST CONTROL



Note: Pin 32 is pulled down by the operation of the peak beam limiter.

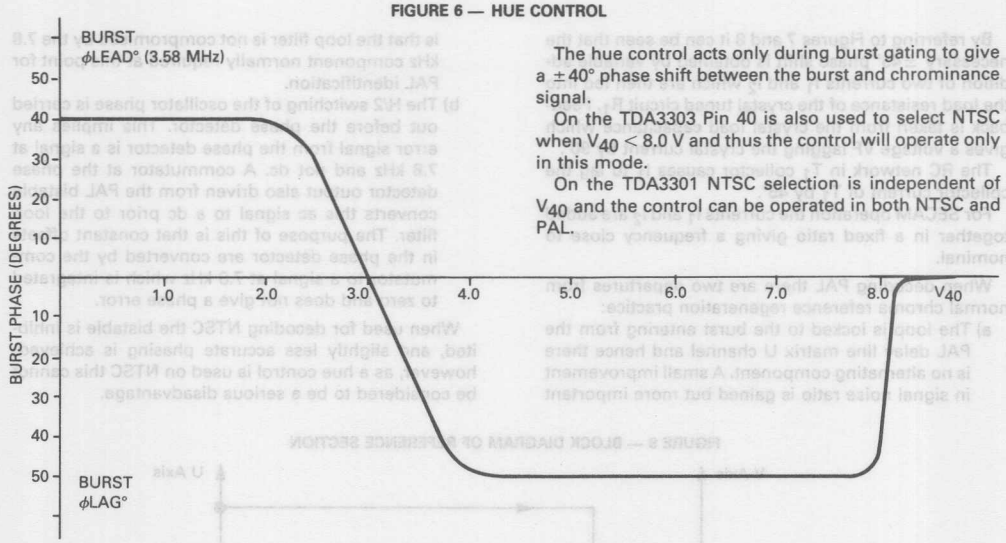
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FIGURE 5 — BLOCK DIAGRAM



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FIGURE 6 — HUE CONTROL



The hue control acts only during burst gating to give a ±40° phase shift between the burst and chrominance signal.

On the TDA3303 Pin 40 is also used to select NTSC when $V_{40} < 8.0$ V and thus the control will operate only in this mode.

On the TDA3301 NTSC selection is independent of V_{40} and the control can be operated in both NTSC and PAL.

CIRCUIT OPERATION

CHROMINANCE DECODER SECTION

The chrominance decoder section of the TDA3301 consists of the following blocks:

Phase-locked reference oscillator — Figures 7, 8 and 9
Phase-locked 90 degree servo loop — Figures 9 and 10
U and V axis decoders
ACC detector and identification detector — Figure 11
Identification circuits and PAL bistable — Figure 12
Color difference filters and matrixes with fast blanking circuits.

The major design considerations apart from optimum performance were:

— a minimum number of factory adjustments
— a minimum number of external components
— compatibility with the SECAM adapter TDA3030B
— low dissipation
— use of a standard 4.433618 MHz Crystal rather than a 2.0 fc Crystal with divider.

REFERENCE REGENERATION

The crystal VCO is of the phase shift variety in which the frequency is controlled by varying the phase of the feedback. A great deal of care was taken to ensure that the oscillator loop gain and the crystal loading impedance were held constant in order to ensure that the circuit functions well with low grade crystal (crystals having high magnitude spurious responses can cause bad phase jitter). It is also necessary to ensure that the gain at third harmonic is low enough to ensure absence of oscillation at this frequency.

FIGURE 7 — VOLTAGE CONTROLLED OSCILLATOR (VCO)

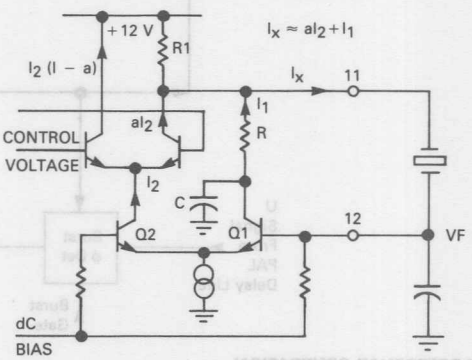
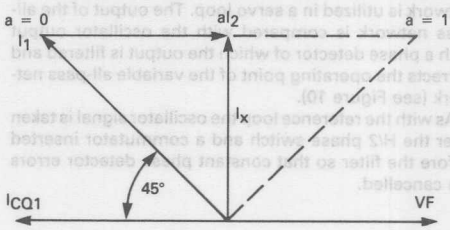


FIGURE 8 — VECTOR DIAGRAM FOR VCO



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By referring to Figures 7 and 8 it can be seen that the necessary ±45° phase shift is obtained by variable addition of two currents I_1 and I_2 which are then fed into the load resistance of the crystal tuned circuit R_1. Feedback is taken from the crystal load capacitance which gives a voltage VF lagging the crystal current by 90°.

The RC network in T_1 collector causes I_1 to lag the collector current of T_1 by 45°.

For SECAM operation the currents I_1 and I_2 are added together in a fixed ratio giving a frequency close to nominal.

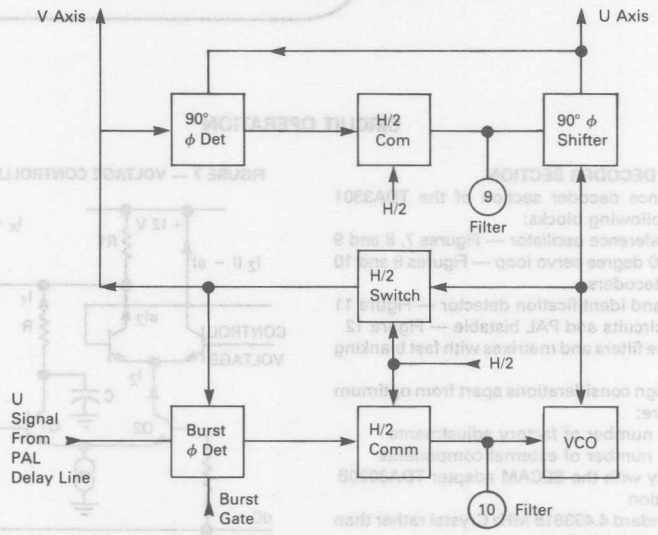
When decoding PAL there are two departures from normal chroma reference regeneration practice:

a) The loop is locked to the burst entering from the PAL delay line matrix U channel and hence there is no alternating component. A small improvement in signal noise ratio is gained but more important is that the loop filter is not compromised by the 7.8 kHz component normally required at this point for PAL identification.

b) The H/2 switching of the oscillator phase is carried out before the phase detector. This implies any error signal from the phase detector is a signal at 7.8 kHz and not dc. A commutator at the phase detector output also driven from the PAL bistable converts this ac signal to a dc prior to the loop filter. The purpose of this is that constant offsets in the phase detector are converted by the commutator to a signal at 7.8 kHz which is integrated to zero and does not give a phase error.

When used for decoding NTSC the bistable is inhibited, and slightly less accurate phasing is achieved; however, as a hue control is used on NTSC this cannot be considered to be a serious disadvantage.

FIGURE 9 — BLOCK DIAGRAM OF REFERENCE SECTION



90° REFERENCE GENERATION

To generate the U axis reference a variable all-pass network is utilized in a servo loop. The output of the all-pass network is compared with the oscillator output with a phase detector of which the output is filtered and corrects the operating point of the variable all-pass network (see Figure 10).

As with the reference loop the oscillator signal is taken after the H/2 phase switch and a commutator inserted before the filter so that constant phase detector errors are cancelled.

For SECAM operation the loop filter is grounded causing near zero phase shift so that the two synchronous detectors work in phase and not in quadrature.

The use of a 4.4 MHz oscillator and a servo loop to generate the required 90° reference signal allows the use of a standard, high volume, low cost crystal and gives an extremely accurate 90° which may be easily switched to 0° for decoding AM SECAM generated by the TDA3030B adapter.

FIGURE 10 — VARIABLE ALL-PASS NETWORK

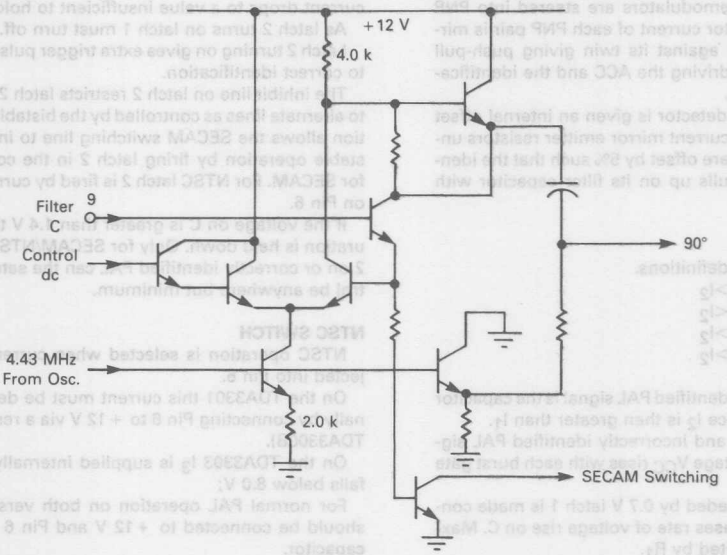
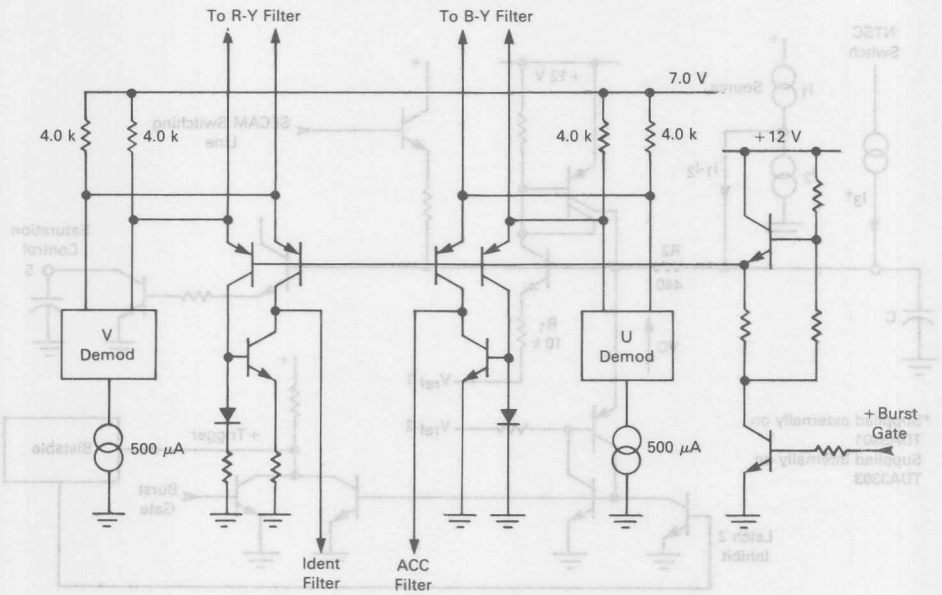


FIGURE 11 — ACC AND IDENTIFICATION DETECTORS



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ACC AND IDENTIFICATION DETECTORS

During burst gate time the output components of the U and also the V demodulators are steered into PNP emitters. One collector current of each PNP pair is mirrored and balanced against its twin giving push-pull current sources for driving the ACC and the identification filter capacitors.

The identification detector is given an internal offset by making the NPN current mirror emitter resistors unequal. The resistors are offset by 5% such that the identification detector pulls up on its filter capacitor with zero signal.

IDENTIFICATION

See Figure 12 for definitions.

Monochrome	$I_1 > I_2$
PAL ident. OK	$I_1 < I_2$
PAL ident. X	$I_1 > I_2$
NTSC	$I_3 > I_2$

Only for correctly identified PAL signal is the capacitor voltage held low since I_2 is then greater than I_1.

For monochrome and incorrectly identified PAL signals $I_1 > I_2$ hence voltage V_{CC} rises with each burst gate pulse.

When V_{ref} is exceeded by 0.7 V latch 1 is made conducting which increases rate of voltage rise on C. Maximum current is limited by R_1.

When V_{ref} 2 is exceeded by 0.7 V then latch 2 is made conducting until C is completely discharged and the current drops to a value insufficient to hold on latch 2.

As latch 2 turns on latch 1 must turn off.

Latch 2 turning on gives extra trigger pulse to bistable to correct identification.

The inhibit line on latch 2 restricts latch 2 conduction to alternate lines as controlled by the bistable. This function allows the SECAM switching line to inhibit the bistable operation by firing latch 2 in the correct phase for SECAM. For NTSC latch 2 is fired by current injected on Pin 6.

If the voltage on C is greater than 1.4 V then the saturation is held down. Only for SECAM/NTSC with latch 2 on or correctly identified PAL can the saturation control be anywhere but minimum.

NTSC SWITCH

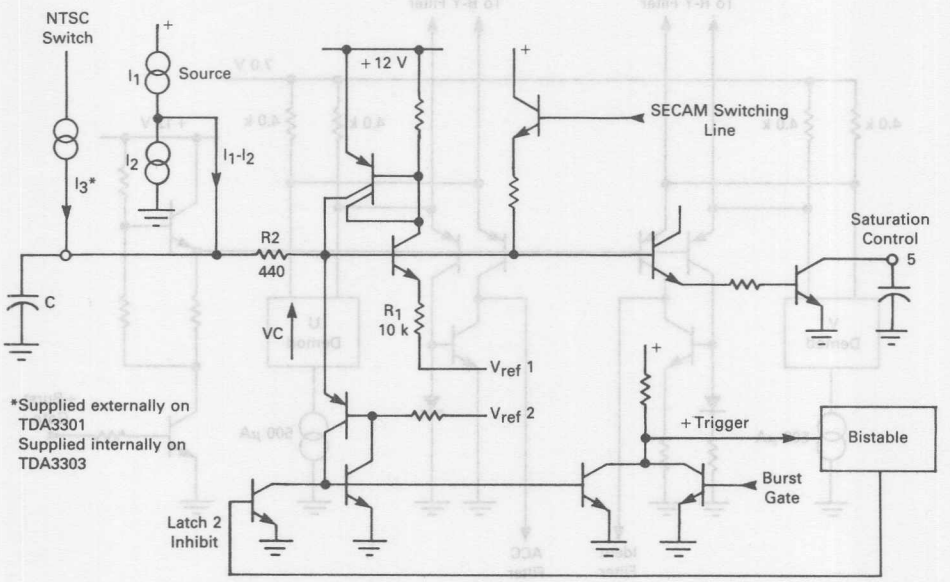
NTSC operation is selected when current (I_3) is injected into Pin 6.

On the TDA3301 this current must be derived externally by connecting Pin 6 to +12 V via a resistor (as on TDA3300B).

On the TDA3303 I_3 is supplied internally when V_{40} falls below 8.0 V;

For normal PAL operation on both versions Pin 40 should be connected to +12 V and Pin 6 to the filter capacitor.

FIGURE 12 — IDENTIFICATION CIRCUIT



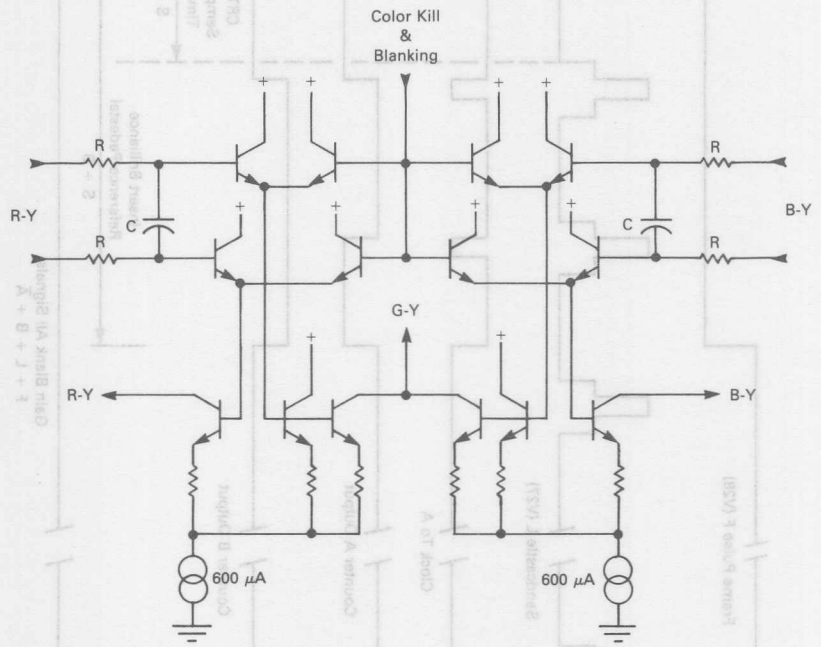
COLOR DIFFERENCE MATRIXING, COLOR KILLING, AND CHROMA BLANKING

During picture time the two demodulators feed simple RC filters with emitter follower outputs. Color killing and blanking is performed by lifting these outputs to a voltage above the maximum value that the color difference signal could supply.

The color difference matrixing is performed by 2 differential amplifiers each with one side split to give the correct values of the −(B-Y) and −(R-Y) signals. These are added to give the (G-Y) signal.

The 3 color difference signals are then taken to the virtual earths of the video output stages together with luminance signal.

FIGURE 13 — COLOR DIFFERENCE STAGES



SANDCASTLE SELECTION

The TDA3301/3303 may be used with a two level sandcastle and a separate frame pulse to Pin 28, or with only a 3 level (super) sandcastle. In the latter case a resistor of 1 MΩ is necessary from +12 volts to Pin 28 and a 470 pF capacitor from Pin 28 to ground.

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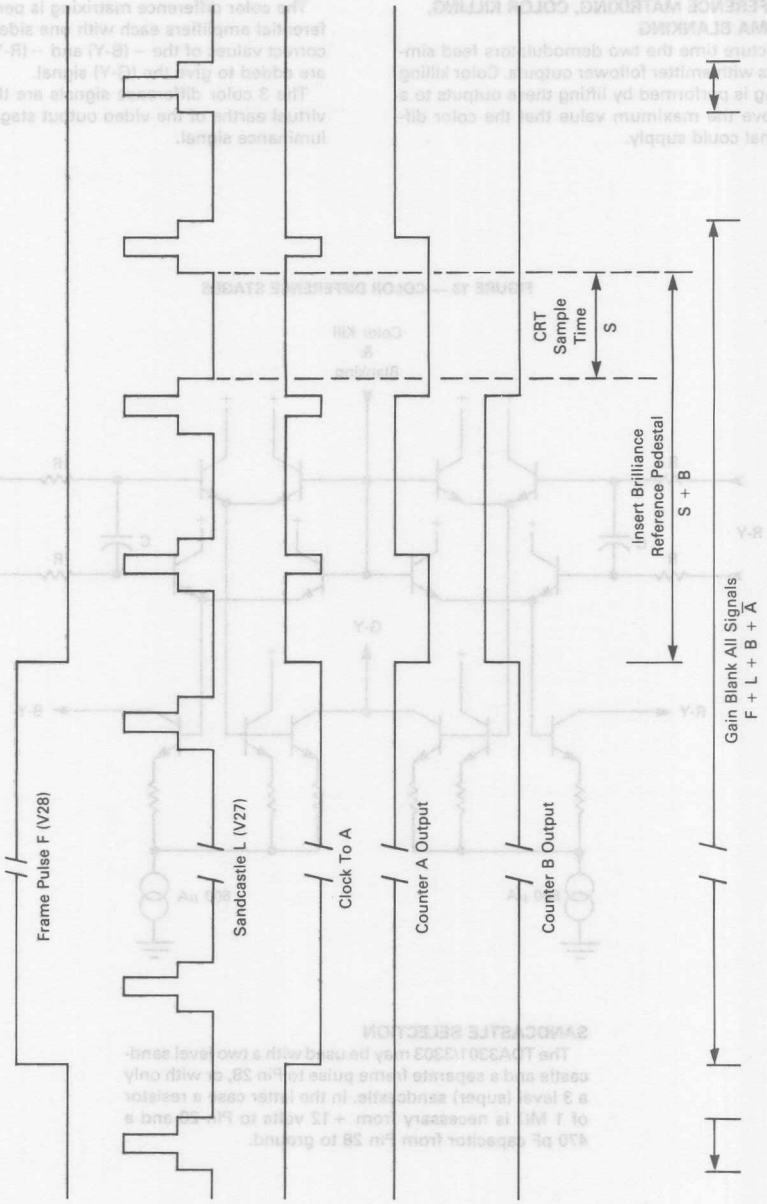


FIGURE 14 — TIMING DIAGRAM

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TIMING COUNTER FOR SAMPLE CONTROL

In order to control the beam current sampling at the beginning of each frame scan two edge triggered flip-flops are used.

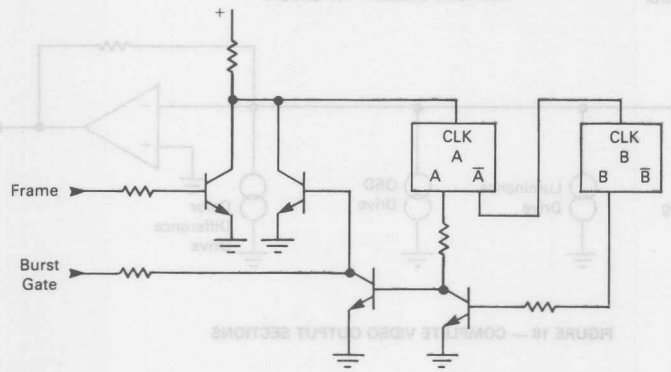
The output $\overline{A}$ of the first flip-flop A is used to clock the second flip-flop B. Clocking of A by the burst gate is inhibited by a count of $A.\overline{B}$.

The count sequence can only by initiated by the trailing edge of the frame pulse. In order to provide control signals for:

Luma/Chroma blanking,
Beam current sampling,
On-screen display blanking,
Brilliance control.

The appropriate flip-flop outputs are matrixed with sandcastle and frame signals by an emitter follower matrix.

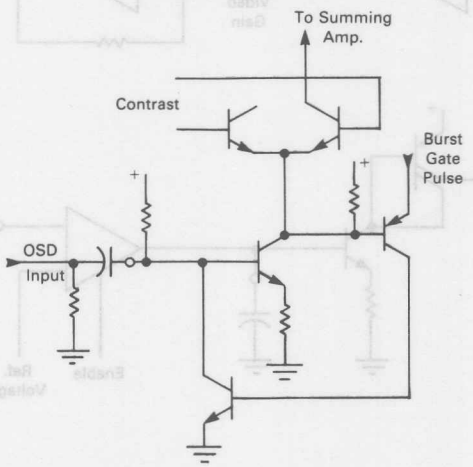
FIGURE 15 — TIMING COUNTER



ON-SCREEN DISPLAY INPUTS

Each section of the OSD stages consists of a common emitter input stage feeding a diversion gate controlled by the contrast control. During burst gate time a feedback loop is activated which clamps the signal at the input coupling capacitor. This ensures that the current in the diversion gate is zero at black level and makes the OSD black level insensitive to contrast control, also the inputs ignore signals below black, e.g. sync, pulses.

FIGURE 16 — OSD STAGE



9

FIGURE 17 — VIDEO OUTPUT SECTION

Each video output stage consists of a feedback amplifier in which the input signal is a current drive to the virtual earth from the luminance, color difference and on-screen display stages.

A further drive current is used to control the dc operating point; this is derived from the sample and hold stage which samples the beam current after frame flyback.

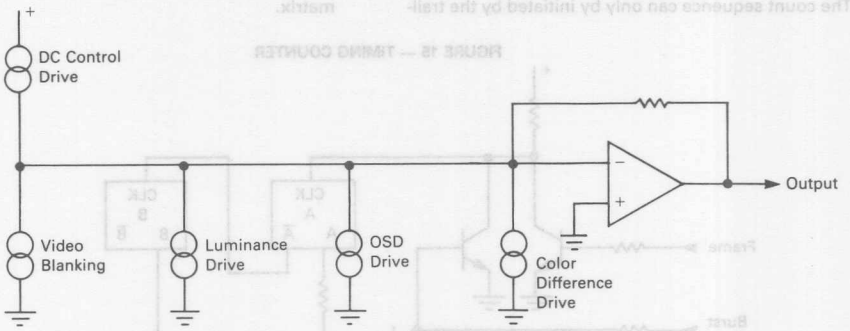
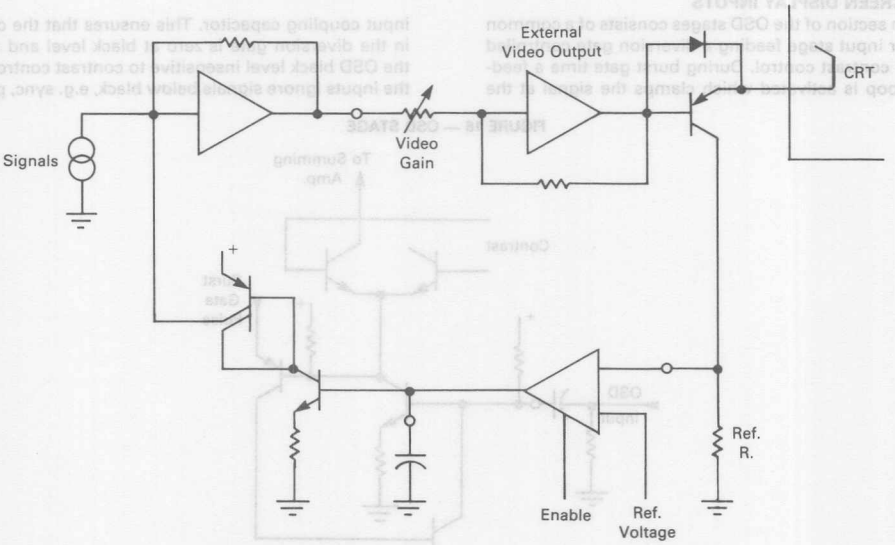


FIGURE 18 — COMPLETE VIDEO OUTPUT SECTIONS



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FIGURE 19 — TYPICAL VIDEO OUTPUT STAGE

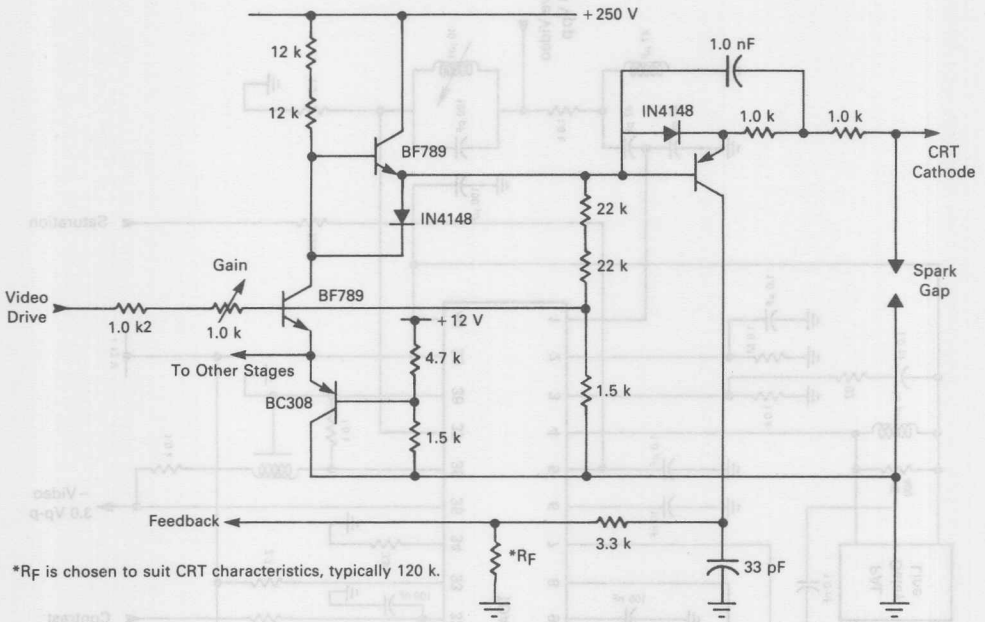
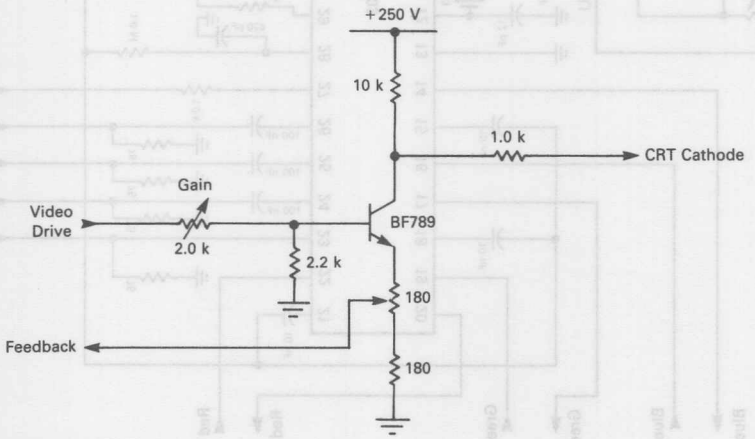
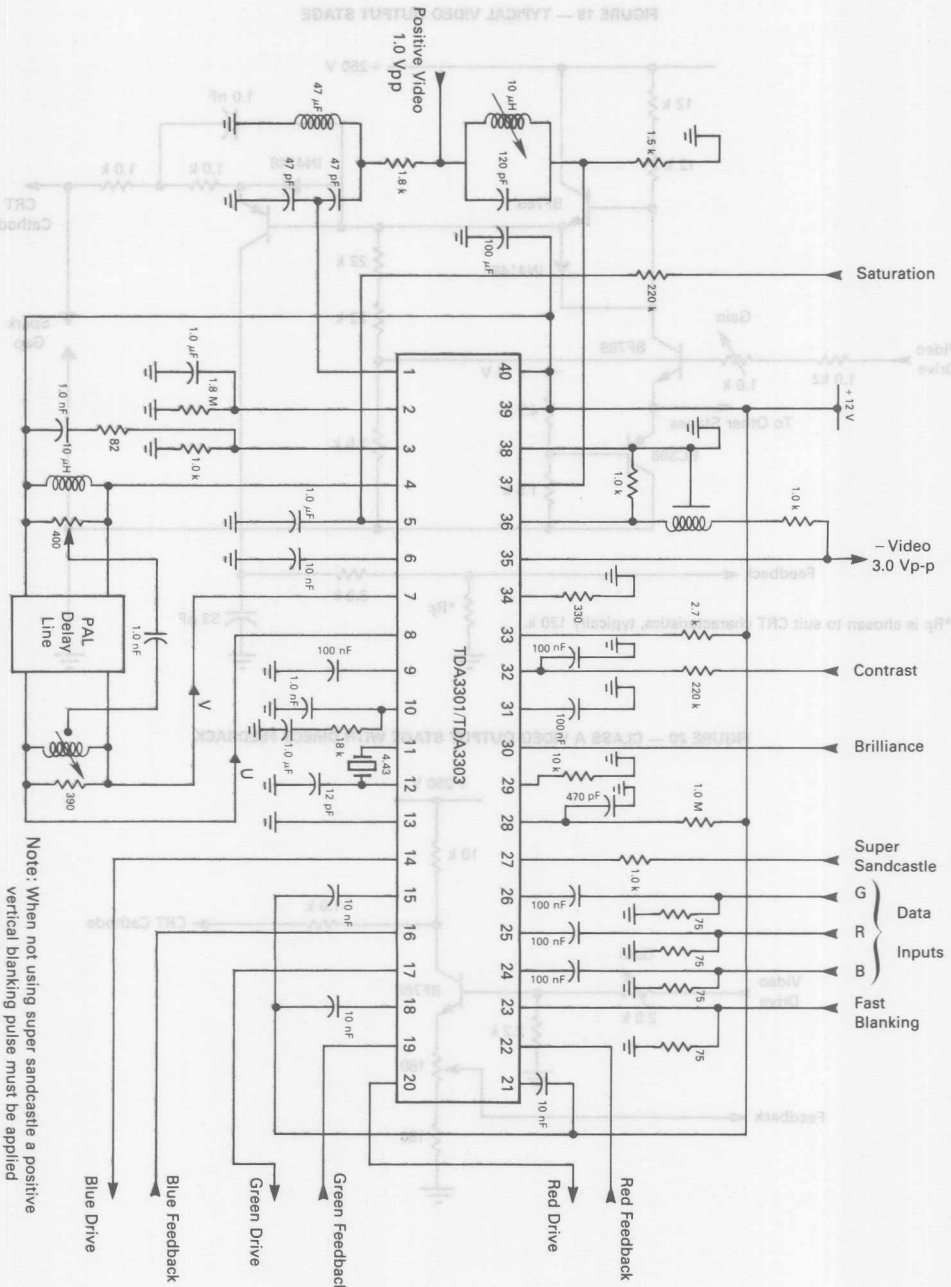


FIGURE 20 — CLASS A VIDEO OUTPUT STAGE WITH DIRECT FEEDBACK



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Note: When not using super sandcastle a positive vertical blanking pulse must be applied to Pin 28.

MOTOROLA

TDA3330

TV COLOR PROCESSOR

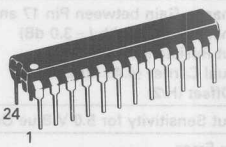
This device will accept a PAL or NTSC composite video signal and output the three color signals, needing only a simple driver amplifier to interface to the picture tube.

Its simplified approach makes it particularly suitable for low cost CTV systems.

- No Oscillator Adjustment Required
- Four dc High Impedance User Controls
- Uses Inexpensive 4.43/3.58 MHz Crystals
- Interfaces With TDA3030B SECAM Adaptor
- Uses Horizontal Flyback or Super Sandcastle Pulse
- Single 12 V Supply
- Low Dissipation

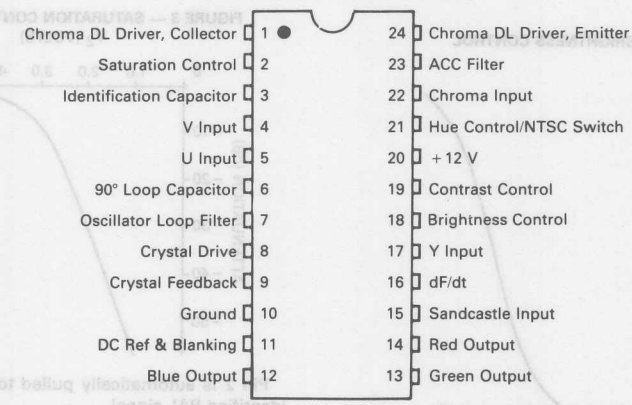
TV COLOR PROCESSOR

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 724-03

FIGURE 1 — PIN ASSIGNMENT



9

MAXIMUM RATINGS (T_A = +25°C unless otherwise stated)

Rating	Pin	Value	Unit
Supply Voltage	20	14	Vdc
Operating Temperature Range		0 to +70	°C
Storage Temperature Range		−65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 12 V)

Characteristic	Pin	Min	Typ	Max	Unit
Supply Voltage	20	10.8	12	13.2	V
Supply Current		—	—	50	mA
Composite Video Input	17	—	1.0	—	Vp-p
Video Input Resistance					
Burst Gate On		—	5.0	—	kΩ
Burst Gate Off		—	1.5	—	MΩ
Chroma Input (Burst)	22	10	100	200	mVp-p
Input Resistance	22	—	5.0	—	kΩ
ACC Effectiveness	1	−1.5	0	+1.5	dB
Luminance Gain between Pin 17 and Outputs (Contrast max)		—	8.0	—	
Luminance Bandwidth (−3.0 dB)	12, 13, 14	—	5.0	—	MHz
Output Resistance		—	170	—	Ω
Residual Carrier (4.43 MHz)		—	—	200	mVp-p
PAL Offset (H/2)		—	—	50	mVp-p
U Input Sensitivity for 5.0 V Blue Output	5	—	340	—	mVp-p
Matrix Error	12, 13, 14	—	—	10	%
Oscillator Capture Range		300	500	—	Hz
U Reference Phase Error		—	—	5.0	°
V Reference Phase Error		—	—	5.0	°
Color Kill Attenuation	12, 13, 14	50	—	—	dB
Contrast Tracking Luma/Chroma	12, 13, 14	—	0	2.0	dB
Sandcastle Slice Level	15				
Burst Gate		—	7.2	8.0	V
Line Blanking		0.5	1.5	2.5	V
R Input $V_{15} > 7.0$ V		—	5.0	—	kΩ
$V_{15} < 7.0$ V		—	10	—	kΩ

9

INPUT/OUTPUT FUNCTIONS

FIGURE 2 — BRIGHTNESS CONTROL

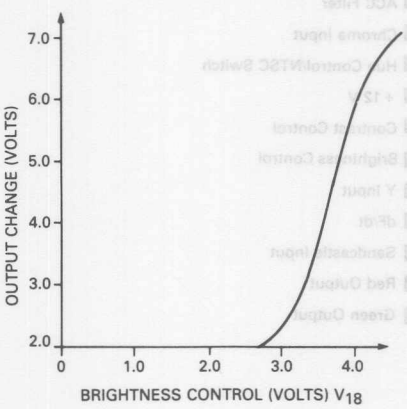
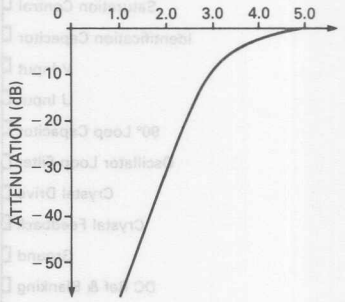


FIGURE 3 — SATURATION CONTROL VOLTAGE



Pin 2 is automatically pulled to ground with a misidentified PAL signal.

Note: Nominal 100% saturation point is given by choice of $R_{pin\ 23}$ which sets ACC operating point.

FIGURE 4 — CONTRAST CONTROL

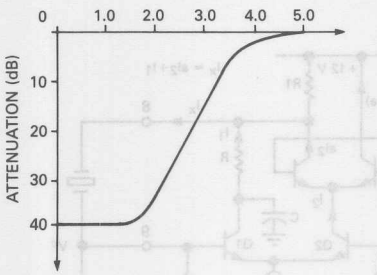
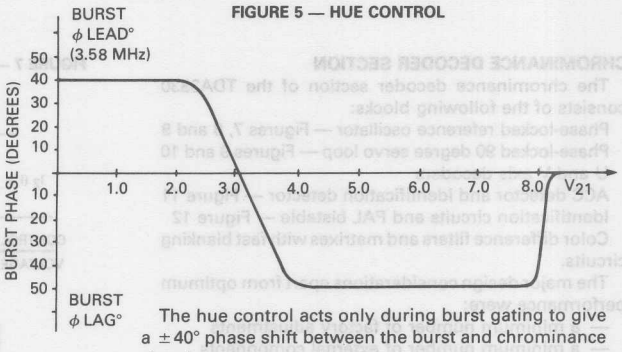


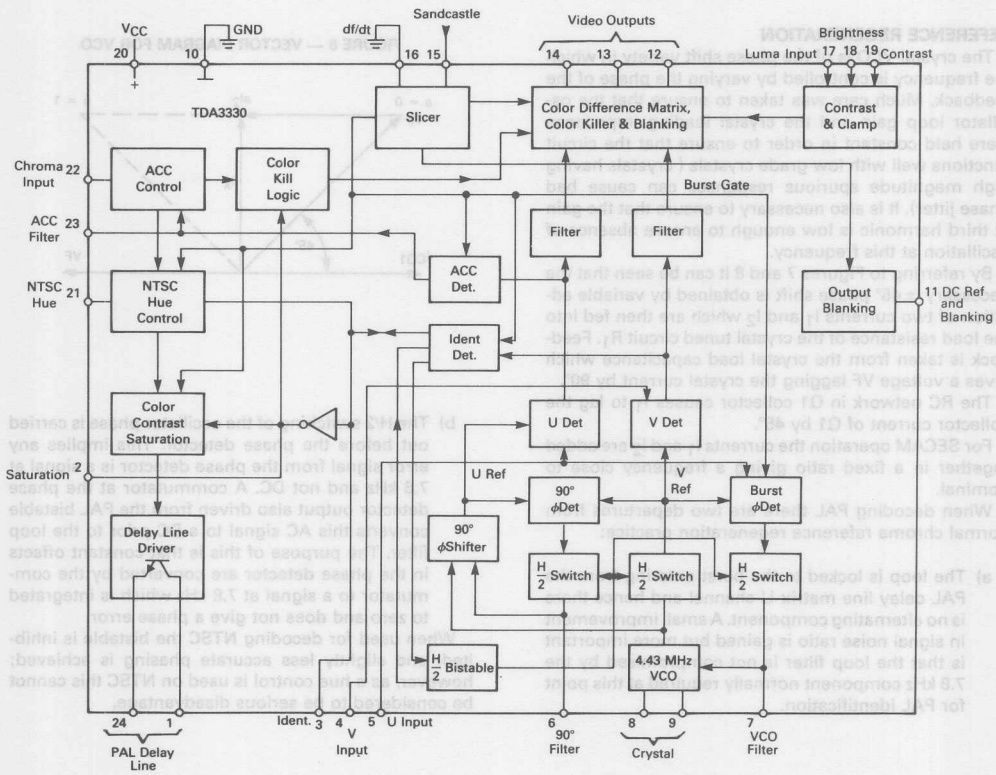
FIGURE 5 — HUE CONTROL



The hue control acts only during burst gating to give a ±40° phase shift between the burst and chrominance signal.

Pin 21 is also used to select NTSC when $V_{21} < 8.0$ V and thus the control will operate only in this mode. NTSC selection means the PAL phase switching is turned off. Delay-line and filter switching must be implemented externally.

FIGURE 6 — BLOCK DIAGRAM



CHROMINANCE DECODER SECTION

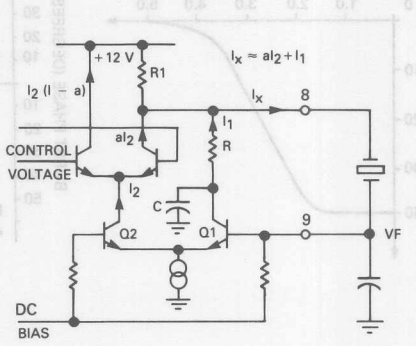
The chrominance decoder section of the TDA3330 consists of the following blocks:

Phase-locked reference oscillator — Figures 7, 8 and 9
Phase-locked 90 degree servo loop — Figures 9 and 10
U and V axis decoders
ACC detector and identification detector — Figure 11
Identification circuits and PAL bistable — Figure 12
Color difference filters and matrixes with fast blanking circuits.

The major design considerations apart from optimum performance were:

— a minimum number of factory adjustments
— a minimum number of external components
— compatibility with the SECAM adapter TDA3030B
— low dissipation
— use of a standard 4.433618 MHz crystal rather than a 2.0 fc crystal with divider, (or standard 3.579545 MHz for NTSC).

FIGURE 7 — VOLTAGE CONTROLLED OSCILLATOR (VCO)



REFERENCE REGENERATION

The crystal VCO is of the phase shift variety in which the frequency is controlled by varying the phase of the feedback. Much care was taken to ensure that the oscillator loop gain and the crystal loading impedance were held constant in order to ensure that the circuit functions well with low grade crystals (crystals having high magnitude spurious responses can cause bad phase jitter). It is also necessary to ensure that the gain at third harmonic is low enough to ensure absence of oscillation at this frequency.

By referring to Figures 7 and 8 it can be seen that the necessary ±45° phase shift is obtained by variable addition of two currents I_1 and I_2 which are then fed into the load resistance of the crystal tuned circuit R_1. Feedback is taken from the crystal load capacitance which gives a voltage VF lagging the crystal current by 90°.

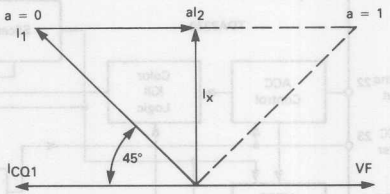
The RC network in Q1 collector causes I_1 to lag the collector current of Q1 by 45°.

For SECAM operation the currents I_1 and I_2 are added together in a fixed ratio giving a frequency close to nominal.

When decoding PAL there are two departures from normal chroma reference regeneration practice:

a) The loop is locked to the burst entering from the PAL delay line matrix U channel and hence there is no alternating component. A small improvement in signal noise ratio is gained but more important is that the loop filter is not compromised by the 7.8 kHz component normally required at this point for PAL identification.

FIGURE 8 — VECTOR DIAGRAM FOR VCO



b) The H/2 switching of the oscillator phase is carried out before the phase detector. This implies any error signal from the phase detector is a signal at 7.8 kHz and not DC. A commutator at the phase detector output also driven from the PAL bistable converts this AC signal to a DC prior to the loop filter. The purpose of this is that constant offsets in the phase detector are converted by the commutator to a signal at 7.8 kHz which is integrated to zero and does not give a phase error.

When used for decoding NTSC the bistable is inhibited, and slightly less accurate phasing is achieved; however, as a hue control is used on NTSC this cannot be considered to be serious disadvantage.

9

90° REFERENCE GENERATION

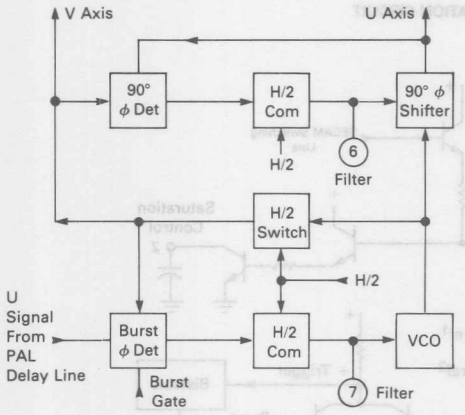
To generate the U axis reference a variable all-pass network is utilized in a servo loop. The output of the all-pass network is compared with the oscillator output with a phase detector of which the output is filtered and corrects the operating point of the variable all-pass network. (See Figure 10.)

As with the reference loop the oscillator signal is taken after the H/2 phase switch and a commutator inserted before the filter so that constant phase detector errors are cancelled.

For SECAM operation with TDA3030B the loop filter is grounded causing near zero phase shift so that the two synchronous detectors work in phase and not in quadrature.

The use of a 4.4 MHz oscillator and a servo loop to generate the required 90° reference signal allows the use of a standard, high volume, low cost crystal and gives an extremely accurate 90° which may be easily switched to 0° for decoding AM SECAM generated by the TDA3030B adapter.

FIGURE 9 — BLOCK DIAGRAM OF REFERENCE SECTION



ACC AND IDENTIFICATION DETECTORS

During burst gate time the output components of the U and also the V demodulators are steered into PNP emitters. One collector current of each PNP pair is mirrored and balanced against its twin giving push pull current sources for driving the ACC and the identification filter capacitors.

The identification detector is given an internal offset by making the NPN current mirror emitter resistors unequal. The resistors are offset by 5% such that the identification detector pulls up on its filter capacitor with zero signal.

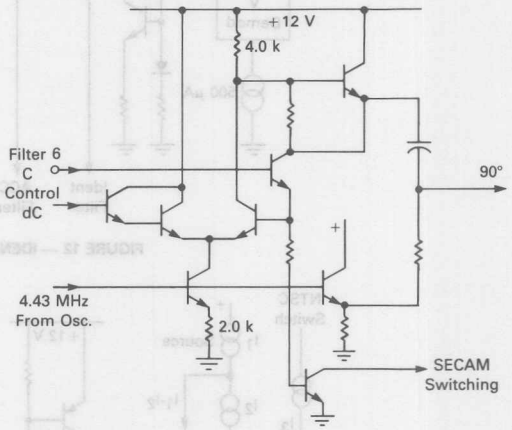
IDENTIFICATION

See Figure 12 for definitions.

Monochrome	$I_1 > I_2$
PAL ident. OK	$I_1 < I_2$
PAL ident. X	$I_1 > I_2$
NTSC	$I_3 > I_2$

Only for correctly identified PAL signal is the capacitor voltage held low since I_2 is then greater than I_1.

FIGURE 10 — VARIABLE ALL-PASS NETWORK



For monochrome and incorrectly identified PAL signals $I_1 > I_2$ hence voltage V_C rises with each burst gate pulse.

When $V_{ref}1$ is exceeded by 0.7 V latch 1 is made conducting which increases rate of voltage rise on C. Maximum current is limited by R_1.

When $V_{ref}2$ is exceeded by 0.7 V then latch 2 is made conducting until C is completely discharged and the current drops to a value insufficient to hold on latch 2.

As latch 2 turns on latch 1 must turn off.

Latch 2 turning on gives extra trigger pulse to bistable to correct identification.

The inhibit line on latch 2 restricts latch 2 conduction to alternate lines as controlled by the bistable. This function allows the SECAM switching line to inhibit the bistable operation by firing latch 2 in the correct phase for SECAM. For NTSC latch 2 is fired by current (I_3) injected into Pin 3 by the NTSC switch. This is supplied internally when V_{21} falls below 8.0 V.

If the voltage on C is greater than 1.4 V then the saturation is held down. Only for SECAM/NTSC with latch 2 on or correctly identified PAL can the saturation control be anywhere but minimum.

9

FIGURE 11 — ACC AND IDENTIFICATION DETECTORS

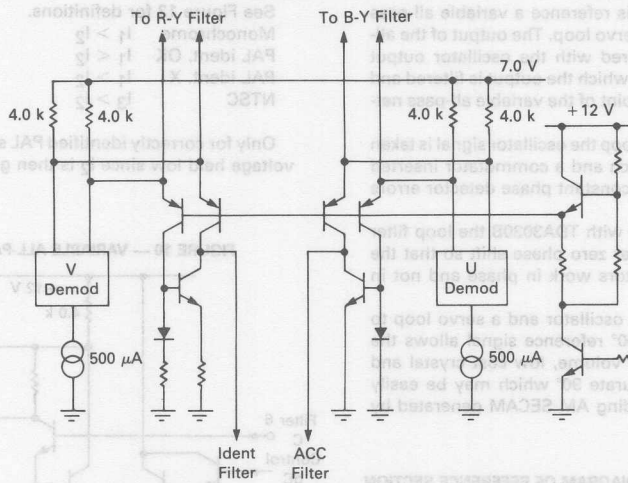
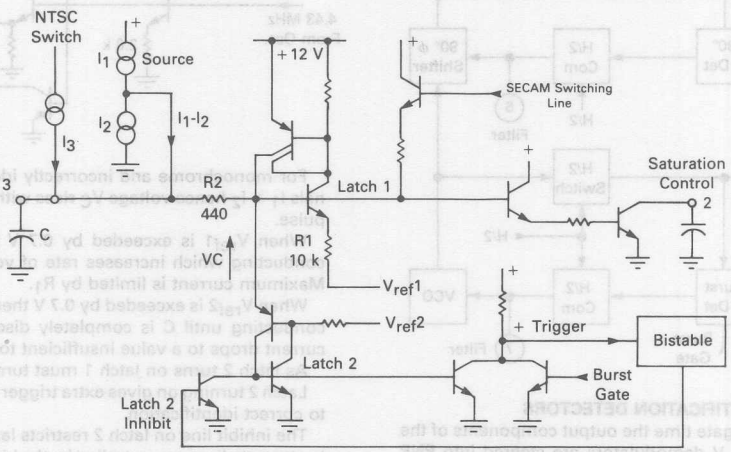


FIGURE 12 — IDENTIFICATION CIRCUIT



COLOR DIFFERENCE MATRIXING, COLOR KILLING, AND CHROMA BLANKING

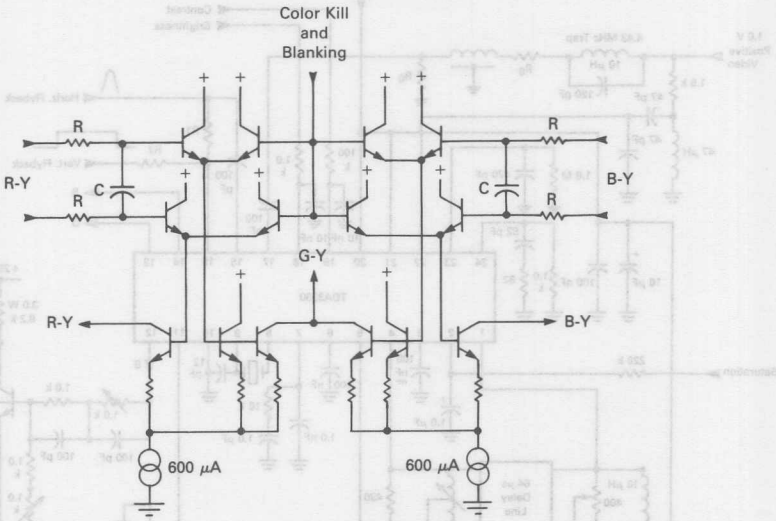
During picture time the two demodulators feed simple RC filters with emitter follower outputs. Color killing and blanking is performed by lifting these outputs to a voltage above the maximum value that the color difference signal could supply.

The color difference matrixing is performed by 2 differential amplifiers each with one side split to give the correct values of the −(B-Y) and −(R-Y) signals. These are added to give the (G-Y) signal.

The 3 color difference signals are then taken to the virtual earths of the video output stages together with luminance signal.

9

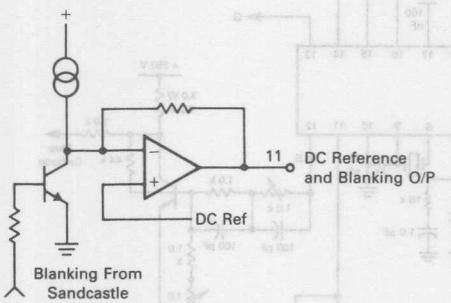
FIGURE 13 — COLOR DIFFERENCE STAGES



SANDCASTLE SECTION

The input signal is sliced at 2 levels, 1.5 V and 7.2 V. Above 1.5 V is used for blanking, above 7.2 V for burst gating provided level on Pin 16 is below 0.7 V. If a normal Sandcastle is used, it is recommended to ground the Pin 16. This input is used to inhibit the burst gate. This is used if a true Sandcastle is not available; in this case horizontal flyback may be used instead and differentiated flyback applied to the $\frac{df}{dt}$ pin (input resistance 1.0 kΩ).

FIGURE 14 — DC REFERENCE AND BLANKING SECTION



The DC Reference and Blanking section is used to bias the Video output stages. The temperature coefficient is arranged to be a V_{BE} drift less than the Red, Green and Blue outputs.

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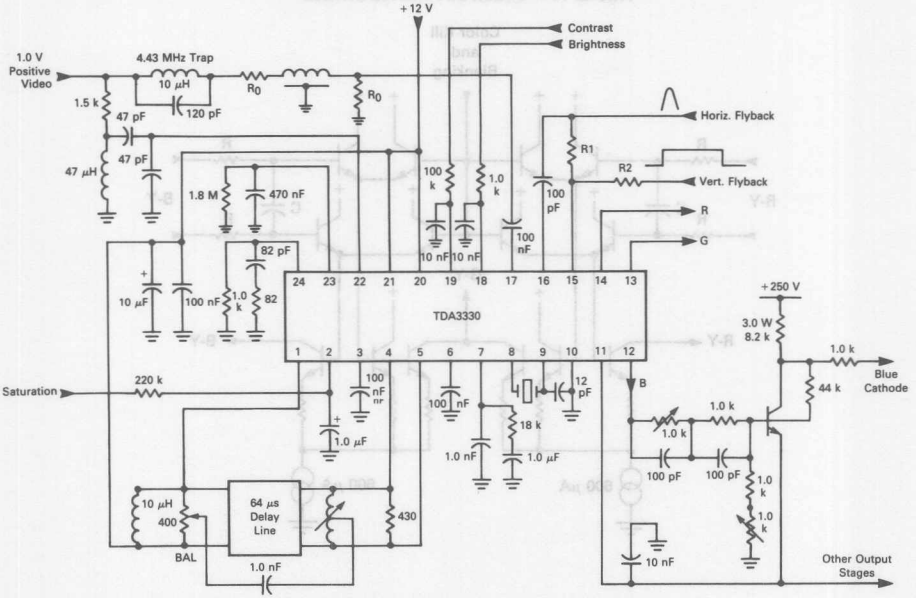
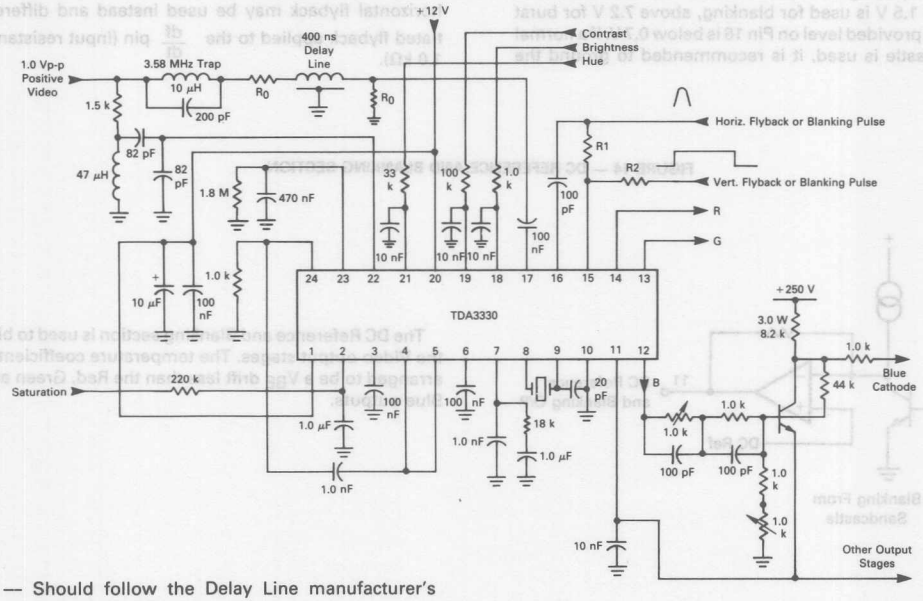


FIGURE 16 — TYPICAL NTSC APPLICATION



R_0 — Should follow the Delay Line manufacturer's recommendations.

R_1 — Should be selected to give approximately 10–12 V pulse at Pin 15 (approximately 5.0 k internal resistance).

R_2 — Should be selected to give approximately 4.0 to 5.0 V pulse at Pin 15 (approximately 10 k internal resistance).

MOTOROLA

TDA3333

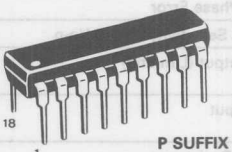
TV COLOR DIFFERENCE DEMODULATOR

This device is designed to demodulate a typical chroma input signal and output the two color difference signals, R – Y and B – Y.

- Decodes PAL or NTSC
- Uses Inexpensive 4.43/3.58 MHz Crystal
- No Oscillator Adjustment Required
- On-Chip Hue Control for NTSC
- Interfaces with TDA3030B SECAM Adaptor
- Single 12 V Supply
- Low Dissipation

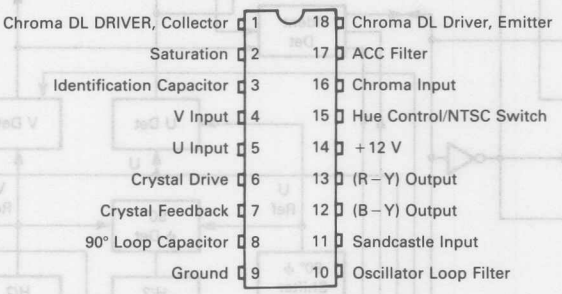
TV COLOR DIFFERENCE DEMODULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 707-02

FIGURE 1 — PIN ASSIGNMENT



9

MAXIMUM RATINGS (T_A = +25°C unless otherwise stated)

Rating	Pin	Value	Unit
Supply Voltage	39	14	Vdc
Operating Temperature Range		0 to +70	°C
Storage Temperature Range		−65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 12 V)

Characteristic		Pin	Min	Typ	Max	Unit
Supply Voltage		14	10.8	12	13.2	V
Chroma Input		16	10	100	200	mVp-p (burst)
ACC Effectiveness		1	—	1.2	3.0	dB
Matrix Error			—	—	10	%
Oscillator Capture Range			350	—	—	Hz
U Ref. Phase Error			—	—	5.0	°
V Ref. Phase Error			—	—	5.0	°
U Input Sensitivity for 1.0 Vp-p	(B-Y) Output	5	—	70	—	mVp-p
Max Output (Limiting)	B-Y R-Y	12 13	— —	4.2 2.4	— —	Vp-p Vp-p
DC Output	B-Y R-Y	12 13	— —	9.2 10.1	— —	V V
Output Resistance	B-Y R-Y	12 13	— —	100 80	— —	Ω Ω

FIGURE 2 — BLOCK DIAGRAM

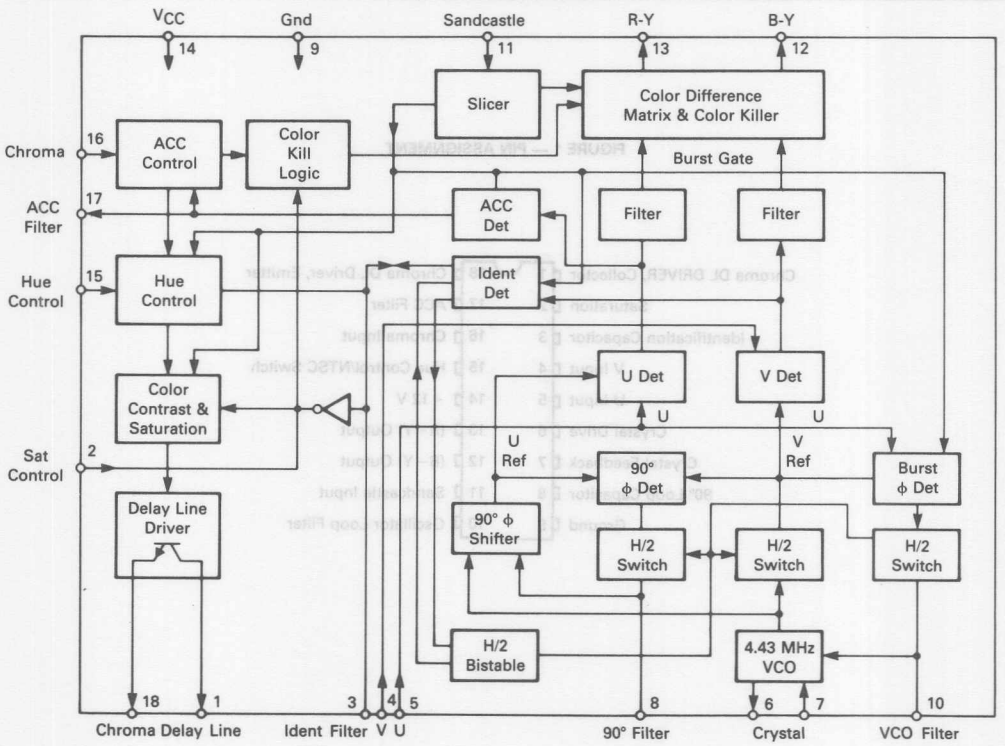
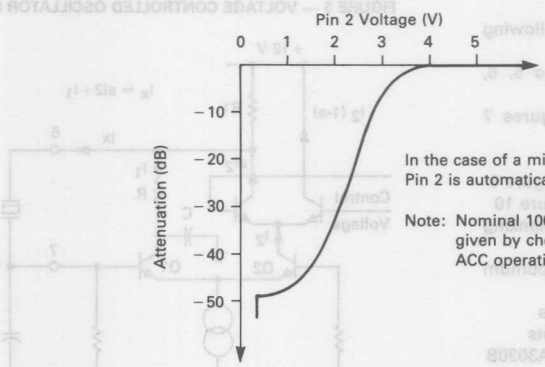


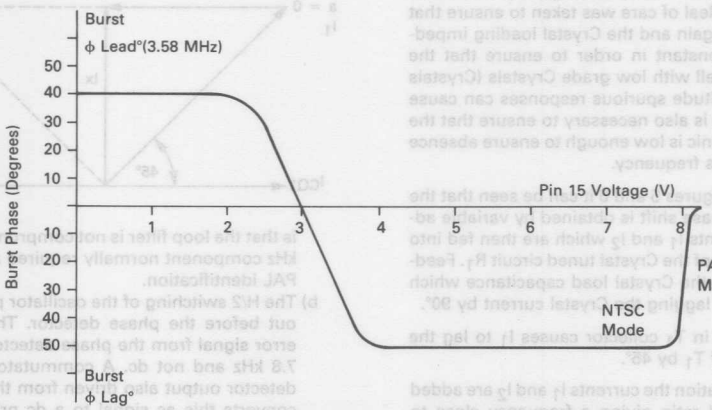
FIGURE 3 — SATURATION CONTROL VOLTAGE



In the case of a misidentified PAL signal Pin 2 is automatically pulled to ground.

Note: Nominal 100% saturation point is given by choice of R_{17} which sets ACC operating point.

FIGURE 4 — HUE CONTROL



Note: Hue control acts only during burst gating with V_{15}<8 Volts.

This condition also selects NTSC mode

9

CHROMINANCE DECODER SECTION

The chrominance decoder consists of the following blocks:

Phase-locked reference oscillator — Figures 5, 6, and 7

Phase-locked 90 degree servo loop — Figures 7 and 8

U and V axis decoders

ACC detector and identification detector — Figure 9

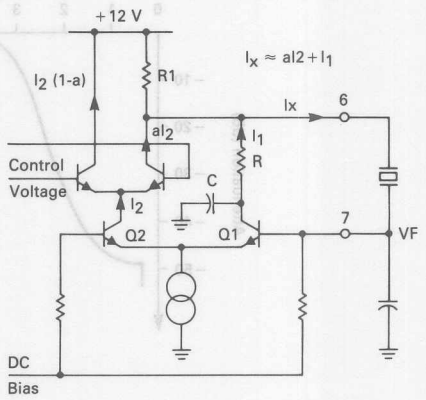
Identification circuits and PAL bistable — Figure 10

Color difference filters and matrixes with fast blanking circuits.

The major design considerations apart from optimum performance were:

— a minimum number of factory adjustments
— a minimum number of external components
— compatibility with the SECAM adapter TDA3030B
— low dissipation
— use of a standard 4.433618 MHz Crystal rather than a 2.0 fc Crystal with divider.

FIGURE 5 — VOLTAGE CONTROLLED OSCILLATOR (VCO)



REFERENCE REGENERATION

The Crystal VCO is of the phase shift variety in which the frequency is controlled by varying the phase of the feedback. A great deal of care was taken to ensure that the oscillator loop gain and the Crystal loading impedance were held constant in order to ensure that the circuit functions well with low grade Crystals (Crystals having high magnitude spurious responses can cause bad phase jitter). It is also necessary to ensure that the gain at third harmonic is low enough to ensure absence of oscillation at this frequency.

By referring to Figures 5 and 6 it can be seen that the necessary ±45° phase shift is obtained by variable addition of two currents I_1 and I_2 which are then fed into the load resistance of the Crystal tuned circuit R_1. Feedback is taken from the Crystal load capacitance which gives a voltage VF lagging the Crystal current by 90°.

The RC network in T_1 collector causes I_1 to lag the collector current of T_1 by 45°.

For SECAM operation the currents I_1 and I_2 are added together in a fixed ratio giving a frequency close to nominal.

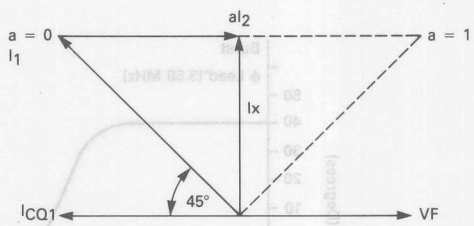
When decoding PAL there are two departures from normal chroma reference regeneration practice:

a) The loop is locked to the burst entering from the PAL delay line matrix U channel and hence there is no alternating component. A small improvement in signal/noise ratio is gained but more important is that the loop filter is not compromised by the 7.8 kHz component normally required at this point for PAL identification.

b) The H/2 switching of the oscillator phase is carried out before the phase detector. This implies any error signal from the phase detector is a signal at 7.8 kHz and not dc. A commutator at the phase detector output also driven from the PAL bistable converts this ac signal to a dc prior to the loop filter. The purpose of this is that constant offsets in the phase detector are converted by the commutator to a signal at 7.8 kHz which is integrated to zero and does not give a phase error.

When used for decoding NTSC the bistable is inhibited, and slightly less accurate phasing is achieved; however, as a hue control is used on NTSC, this cannot be considered to be a serious disadvantage.

FIGURE 6 — VECTOR DIAGRAM FOR VCO



90° REFERENCE GENERATION

FIGURE 7 — BLOCK DIAGRAM OF REFERENCE SECTION

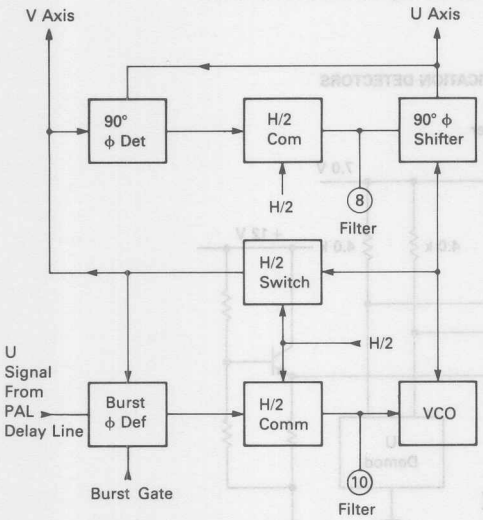
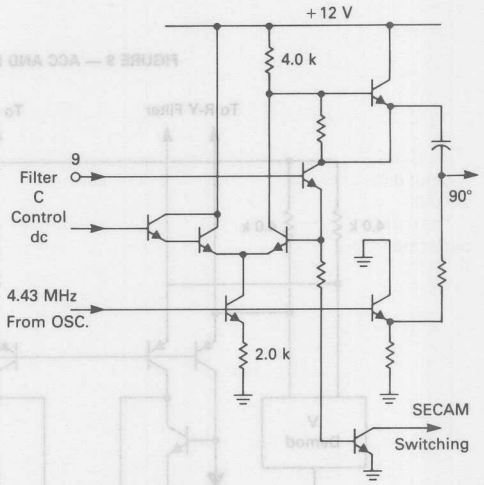


FIGURE 8 — VARIABLE ALL-PASS NETWORK



To generate the U axis reference a variable all-pass network is utilized in a servo loop. The output of the all-pass network is compared with the oscillator output with a phase detector of which the output is filtered and corrects the operating point of the varible all-pass network (see Figure 8).

As with the reference loop the oscillator signal is taken after the H/2 phase switch and a commutator inserted before the filter so that constant phase detector errors are cancelled.

For SECAM operation the loop filter is grounded causing near zero phase shift so that the two synchronous detectors work in phase and not in quadrature.

The use of a 4.4 MHz oscillator and a servo loop to generate the required 90° reference signal allows the use of a standard, high volume, low cost crystal and gives an extremely accurate 90° which may be easily switched to 0° for decoding AM SECAM generated by the TDA3030B Adapter.

ACC AND IDENTIFICATION DETECTORS

During burst gate time the output components of the U and also the V demodulators are steered into PNP emitters. One collector current of each PNP pair is mirrored and balanced against its twin giving push-pull current sources for driving the ACC and the identification filter capacitors.

The identification detector is given an internal offset by making the NPN current mirror emitter resistors unequal. The resistors are offset by 5% such that the identification detector pulls up on its filter capacitor with zero signal.

IDENTIFICATION

Monochrome	$I_1 > I_2$	PAL ident. X	$I_1 > I_2$
PAL ident. OK	$I_1 < I_2$	NTSC	$I_3 > I_2$

Only for correctly identified PAL signal is the capacitor voltage held low since I_2 is then greater than I_1.

For monochrome and incorrectly identified PAL signals $I_1 > I_2$ hence voltage V_C rises with each burst gate pulse.

When V_{ref} is exceeded by 0.7 V latch 1 is made conducting which increases rate of voltage rise on C. Maximum current is limited by R_1.

When V_{ref} is exceeded by 0.7 V then latch 2 is made conducting until C is completely discharged and the current drops to a value insufficient to hold on latch 2.

As latch 2 turns on latch 1 must turn off.

Latch 2 turning on gives extra trigger pulse to bistable to correct identification.

9

The inhibit line on latch 2 restricts latch 2 conduction to alternate lines as controlled by the bistable. This function allows the SECAM switching line to inhibit the bistable operation by firing latch 2 in the correct phase for SECAM. For NTSC latch 2 is fired by current injected externally on the filter capacitor.

If the voltage on C is greater than 1.4 V then the saturation is held down. Only for SECAM/NTSC with latch 2 on or correctly identified PAL can the saturation control be anywhere but minimum.

FIGURE 9 — ACC AND IDENTIFICATION DETECTORS

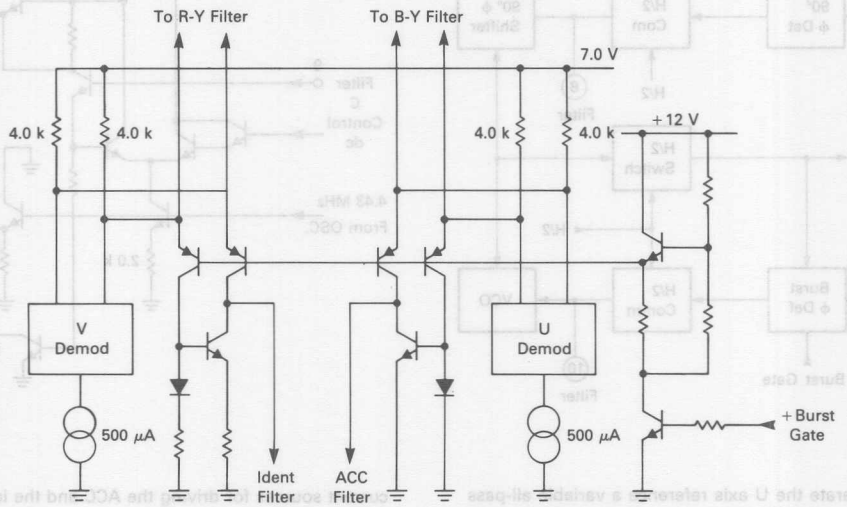
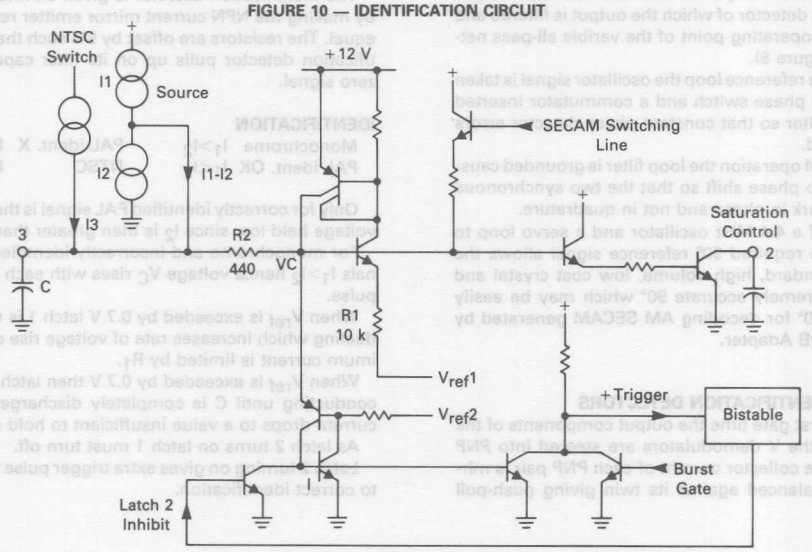


FIGURE 10 — IDENTIFICATION CIRCUIT



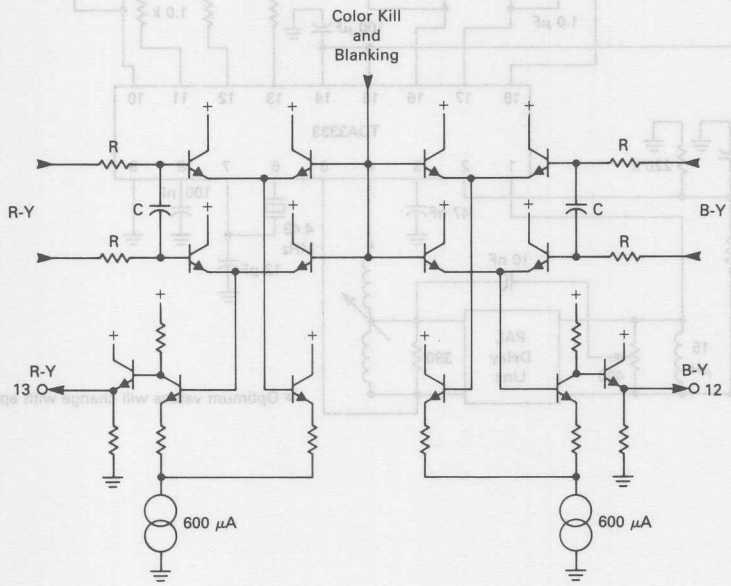
NTSC switch operates when V_{15}<8.0 V.

COLOR DIFFERENCE MATRIXING, COLOR KILLING, AND CHROMA BLANKING

During picture time the two demodulators feed simple RC filters with emitter follower outputs. Color killing and blanking is performed by lifting these outputs to a voltage above the maximum value that the color difference signal could supply.

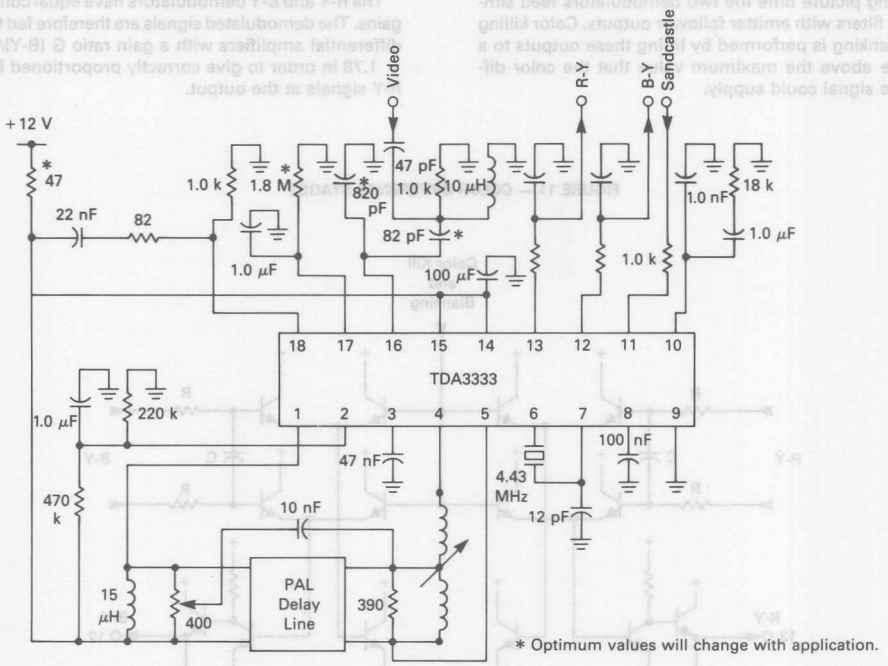
The R-Y and B-Y demodulators have equal conversion gains. The demodulated signals are therefore fed through differential amplifiers with a gain ratio G (B-Y)/G (R-Y) = 1.78 in order to give correctly proportioned B-Y and R-Y signals at the output.

FIGURE 11 — COLOR DIFFERENCE STAGES

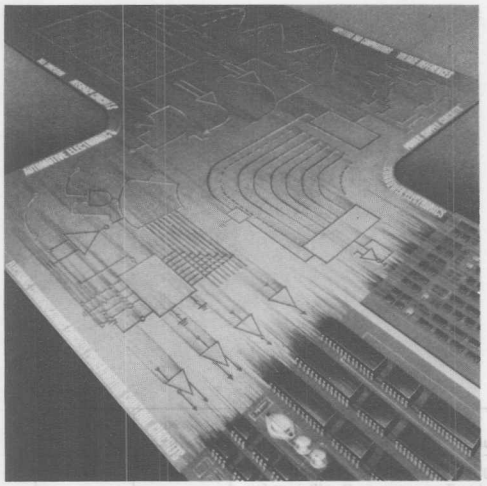


9

FIGURE 12 — TYPICAL PAL APPLICATION



9



Automotive Electronic Circuits

10

In Brief . . .

Motorola Linear has established itself as the leader in custom bipolar integrated circuits in the American and European automotive markets. These products are key elements in the rapidly growing engine control and body electronics portions of modern automobiles. Today, based on this new technology, Motorola offers a wide array of standard products to serve the broad base of manufacturers who support this industry. These products range from rugged high current "smart" fuel injector drivers which control and protect the fuel management system, through the rigors of the underhood environment, to the latest in BiMOS switches and series transient protectors. Several devices are targeted to support microprocessor housekeeping and data line protection. A wide range of packaging is available, from die and SOICs for high density layouts, to low thermal resistance multi-pin, single-in-line types for high power control ICs.

Selector Guide

Voltage Regulators 10-2
Electronic Ignition 10-2
Special Functions 10-2

Alphanumeric Index 10-4

Related Application Notes 10-4

Data Sheets 10-5

Automotive Electronic Circuits

Voltage Regulators 10-2
Electronic Ignition 10-2
Special Functions 10-2
Automotive High-Side Driver Switch. 10-3
Universal Microprocessor Power Supply Controller . . 10-3
Automotive Direction Indicator 10-3

Voltage Regulators

Function	Features	Case Suffix	Device
Automotive Voltage Regulator	Designed for use with NPN Darlington, Overvoltage Protection; "Open Sense" Shut Down; Selectable Temperature Coefficient for Use in a Floating Field Alternator Charging System	P/646	MC3325
Low Dropout Voltage Regulator	Positive fixed and adjustable output voltage regulators which maintain regulation with very low input to output voltage differential.	Z/29, T/221A, T/314D	LM2931,C
Low Dropout Dual Regulator	Positive low voltage differential regulator which features dual 5 V outputs, with currents in excess of 750 mA and 10 mA standby, and a low quiescent current of 3 mA or less.	T/314D	LM2935

Electronic Ignition

Electronic Ignition Circuit	Designed for Use in High Energy Variable Dwell Electronic Ignition Systems with Variable Reluctance Sensors. Dwell and Spark Energy are Externally Adjustable	P/626, D/751	MC3334
Flip-Chip Electronic Ignition Circuit	Same as MC3334 — Mirror Image Die for Inverted "Bumped" Mounting to Substrate	—	MCCF3334

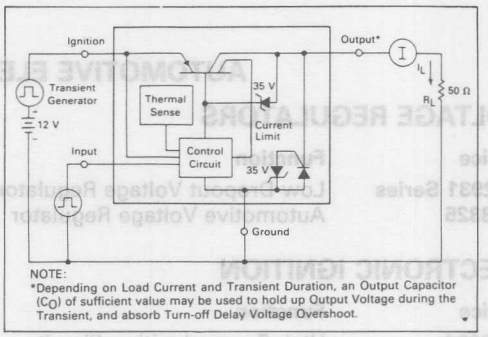
Special Functions

Injector Driver	Power Driver for Automotive Fuel Injection Systems, Reduced Hold Current MC3484S2 — 2 Amps MC3484S4 — 4 Amps	S/314D	MC3484
Transient Suppressor	Series Transient, opens circuit to protect	T/221A,	MC3397T
High Side Driver Switch	Drives loads from positive side of power supply and protects against high-voltage transients.	T/314D	MC3399T
Automotive Direction Indicator	Detects defective lamps and protects against overvoltage and short circuit hazards.	P/626	UAA1041
Peripheral Clamping Array	Protects up to six MPU I/O lines against voltage transients.	626	TCF6000
Pressure Transducer Amplifier	Consists of 2 Low Power Operational amplifiers with identical characteristics, except for the outputs.	626, D/751	TCF7000

Automotive High-Side Driver Switch

MC3399T — T_J = −40° to +150°C, Case 314D

The MC3399T is a High-Side Driver Switch that is designed to drive loads from the positive side of the power supply. The output is controlled by a TTL compatible Enable pin. In the ON state, the device exhibits very low saturation voltages for load currents in excess of 750 mA. The device also protects the load from positive or negative going high voltage transients by becoming an open circuit and isolating the transient for its duration from the load.



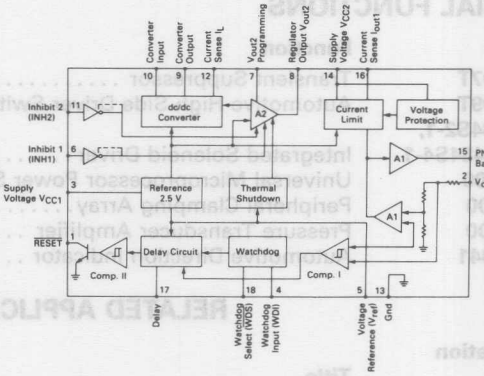
NOTE:
*Depending on Load Current and Transient Duration, an Output Capacitor (C_O) of sufficient value may be used to hold up Output Voltage during the Transient, and absorb Turn-off Delay Voltage Overshoot.

Universal Microprocessor Power Supply Controller

TCA5600 — T_A = −40° to +75°C, Case 707

This device is a versatile power supply control circuit for microprocessor based systems and mainly intended for automotive applications and battery powered instruments. To cover a wide range of applications, the device offers high circuit flexibility with minimum of external components.

Functions included in this IC are a temperature compensated voltage reference, on-chip dc/dc converter, programmable and remote controlled voltage regulator, fixed 5.0 V supply voltage regulator with external PNP power device, undervoltage detection circuit, power-on RESET delay and watchdog feature for orderly microprocessor operations.

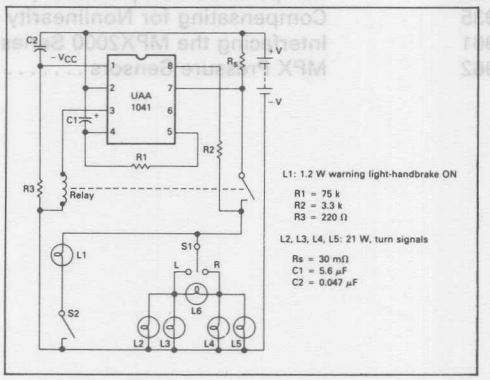


Automotive Direction Indicator

UAA1041,D — T_A = −40° to +100°C, Case 626, 751

. . . designed for use in conjunction with a relay in automotive applications. It is also applicable for other warning lamps like "handbrake on" etc.

- Defective Lamp Detection
- Overvoltage Protection
- Short Circuit Detection and Relay Shutdown to Prevent Risk of Fire
- Reverse Battery Connection Protection
- Integrated Suppression Clamp Diode



10

AUTOMOTIVE ELECTRONIC CIRCUITS

VOLTAGE REGULATORS

Device	Function	Page
LM2931 Series	Low Dropout Voltage Regulator	See Chapter 3
MC3325	Automotive Voltage Regulator	10-5

ELECTRONIC IGNITION

Device	Function	Page
MC3334	High Energy Ignition Circuit	10-9
MCC3334	High Energy Ignition Circuit	10-9
MCCF3334	High Energy Ignition Circuit	10-9

SPECIAL FUNCTIONS

Device	Function	Page
MC3397T	Transient Suppressor	10-13
MC3399T	Automotive High Side Driver Switch	10-16
MC3484S2-1, MC3484S4-1	Integrated Solenoid Driver	10-19
TCA5600	Universal Microprocessor Power Supply Controller	See Chapter 3
TCF6000	Peripheral Clamping Array	See Chapter 7
TCF7000	Pressure Transducer Amplifier	10-25
UAA1041	Automotive Direction Indicator	10-27

RELATED APPLICATION NOTES

Application Note	Title	Related Device
AN840	Temperature Compensation Methods for the Motorola X-Ducer Pressure Sensor Element	TCF7000
AN922	Temperature Compensation, Calibration	TCF7000
AN935	Compensating for Nonlinearity in the	TCF7000
AN961	Interfacing the MPX2000 Series Silicon Pressure Sensors	TCF7000
AN962	MPX Pressure Sensors	TCF7000

MOTOROLA

MC3325

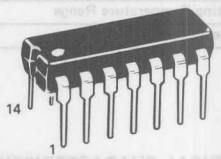
AUTOMOTIVE VOLTAGE REGULATOR

AUTOMOTIVE VOLTAGE REGULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

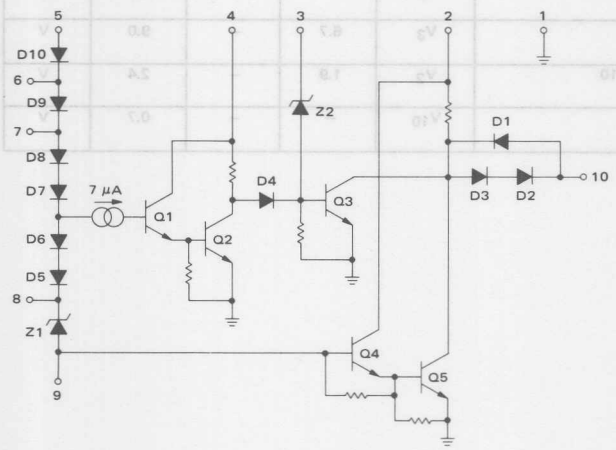
. . . designed for use in conjunction with an NPN Darlington transistor in a floating field alternator charging system.

- Overvoltage Protection
- Shut-Down on Loss of Battery Sense
- Selectable Temperature Coefficient
- Available in Chip Form for Hybrid Assembly

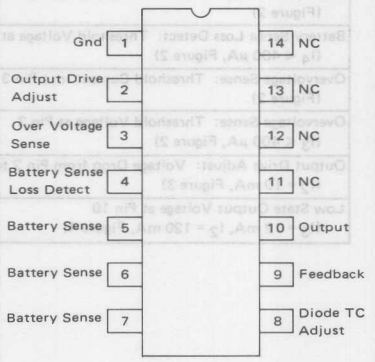


P SUFFIX
PLASTIC PACKAGE
CASE 646-06

CIRCUIT SCHEMATIC



PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
MC3325P	-40 to +85°C	Plastic DIP

10

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Current Into Pins 5, 6, and 7	$I_{5, 6, or 7}$	50	mA
Current Into Pin 3	I_3	20	mA
Current Into Pin 4	I_4	20	mA
Current Into Pin 2	I_2	120	mA
Current Into Pin 8	I_8	50	mA
Current Into Pin 9	I_9	50	mA
Current Into Pin 10	I_{10}	50	mA
Junction Temperature	T_J	150	°C
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit
Diode TC Adjust: Threshold Voltage on Pin 8 (Figure 1)	V_8	7.9	–	8.95	V
Battery Sense: Threshold Voltage on Pin 5 (Figure 1)	V_5	11.8	–	13.45	V
Battery Sense: Threshold Voltage on Pin 6 (Figure 1)	V_6	11.1	–	12.75	V
Battery Sense: Threshold Voltage on Pin 7 (Figure 1)	V_7	10.5	–	11.9	V
Battery Sense Loss Detect: Threshold Current Into Pin 4 (Figure 2)	I_4	–	–	600	μA
Battery Sense Loss Detect: Threshold Voltage at Pin 4 ($I_4 \leq 400$ μA, Figure 2)	V_4	1.3	–	1.7	V
Overvoltage Sense: Threshold Current Into Pin 3 (Figure 2)	I_3	–	–	600	μA
Overvoltage Sense: Threshold Voltage at Pin 3 ($I_3 \leq 400$ μA, Figure 2)	V_3	6.7	–	9.0	V
Output Drive Adjust: Voltage Drop from Pin 2 to Pin 10 (I_2 = 10 mA, Figure 3)	V_2	1.9	–	2.4	V
Low State Output Voltage at Pin 10 (I_3 = 12 mA, I_2 = 120 mA, Figure 4)	V_{10}	–	–	0.7	V

10

TEST CIRCUITS

FIGURE 1

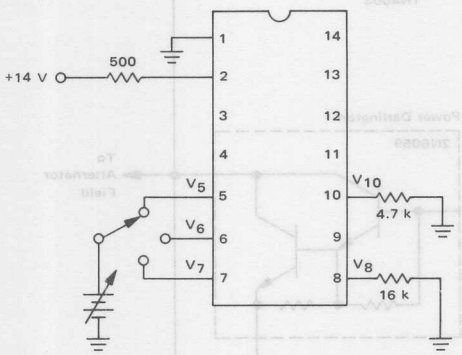


FIGURE 2

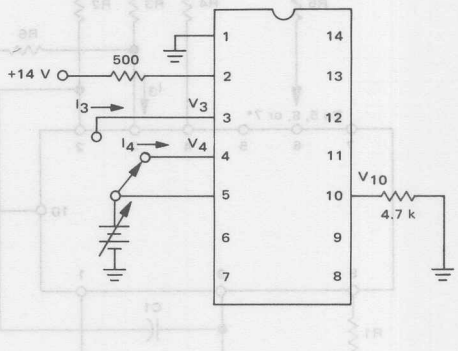


FIGURE 3

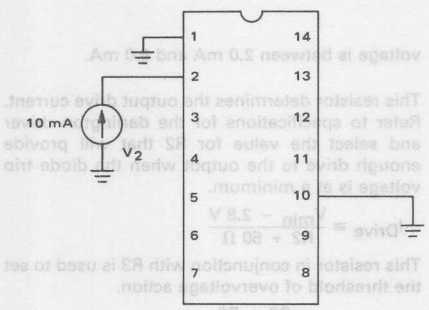
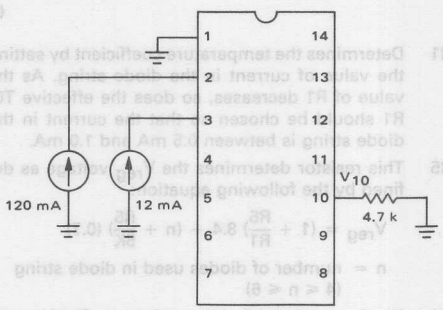
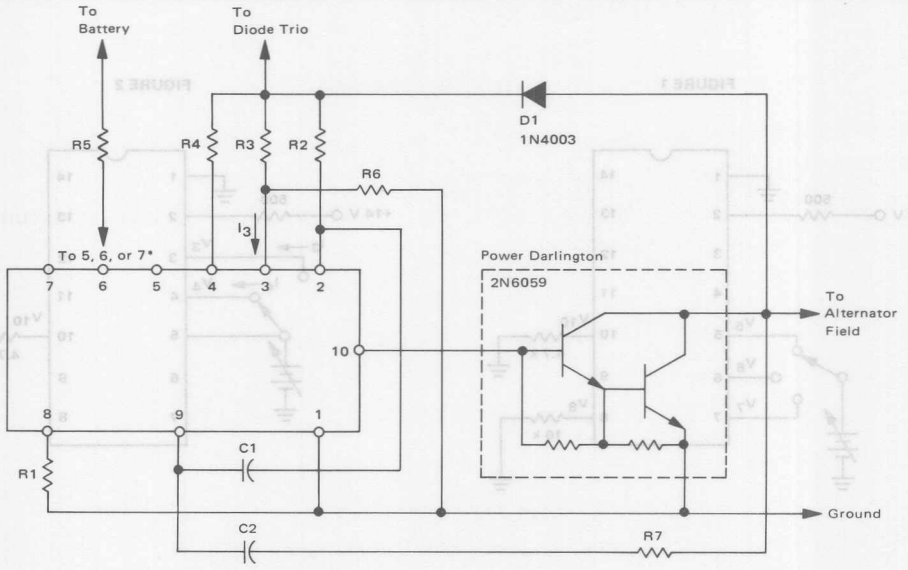


FIGURE 4



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FIGURE 5 – APPLICATION CIRCUIT



*Note: The temperature coefficient of the battery voltage sense terminal is determined by the number of diodes used in the diode string (i.e., whether Pin 5, 6, or 7 is used). The approximate temperature coefficient for a diode at 1.0 mA is -2.0 mV/°C, and for a zener diode it is +3.0 mV/°C. Counting from ground (see circuit schematic) we have -2.0 mV for Q5, -2.0 mV for Q4, +3.0 mV for Z1, -8.0 mV for D5 thru D8, and an additional -2.0 mV each for D9 and D10 if used. The total temperature coefficient can be varied from approximately -9.0 mV/°C to -13 mV/°C depending on the number of the diodes in the diode string that are utilized.

10

APPLICATIONS CIRCUIT INFORMATION

(See Figure 5)

R1 Determines the temperature coefficient by setting the value of current in the diode string. As the value of R1 decreases, so does the effective TC. R1 should be chosen so that the current in the diode string is between 0.5 mA and 1.0 mA.

R5 This resistor determines the V_{reg} voltage as defined by the following equation:

$$V_{reg} = (1 + \frac{R5}{R1})\,8.4 + (n + \frac{R5}{5K})\,(0.7)$$

n = number of diodes used in diode string ($4 \leq n \leq 6$)

R4 Used as a current limiting resistor on Pin 4 in case of an open battery voltage sense lead.

R3 Used as a current limiting resistor on Pin 3 in case of overvoltage at the diode trio. Voltage at Pin 3 will run approximately 7.5 volts. R3 should be chosen so that the current (I_3) at maximum overvoltage is between 2.0 mA and 6.0 mA.

R2 This resistor determines the output drive current. Refer to specifications for the darlington driver and select the value for R2 that will provide enough drive to the output when the diode trio voltage is at a minimum.

$$I_{Drive} \cong \frac{V_{min} - 2.8\ V}{R2 + 50\ \Omega}$$

R6 This resistor in conjunction with R3 is used to set the threshold of overvoltage action.

$$\text{Threshold} \cong \frac{R3 + R6}{R6}\,(7.5)$$

R7 Used for compensation (Approximately 3.0 kΩ)

C1, C2 Used for compensation (Approximately 0.01 μF)

MOTOROLA

MC3334P
MCC3334
MCCF3334

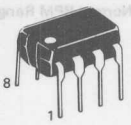
HIGH ENERGY IGNITION CIRCUIT

. . . designed to use the signal from a reluctor type ignition pickup to produce a well controlled output from a power Darlington output transistor.

- Very Low Peripheral Component Count
- No Critical System Resistors
- Wide Supply Voltage Operating Range (4.0–24 V)
- Overvoltage Shutdown (30 V)
- Dwell Automatically Adjusts To Produce Optimum Stored Energy Without Waste
- Externally Adjustable Peak Current
- Available in Chip and Flip Chip Form
- Transient Protected Inputs and Outputs

HIGH ENERGY IGNITION CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 626-05

MAXIMUM RATINGS

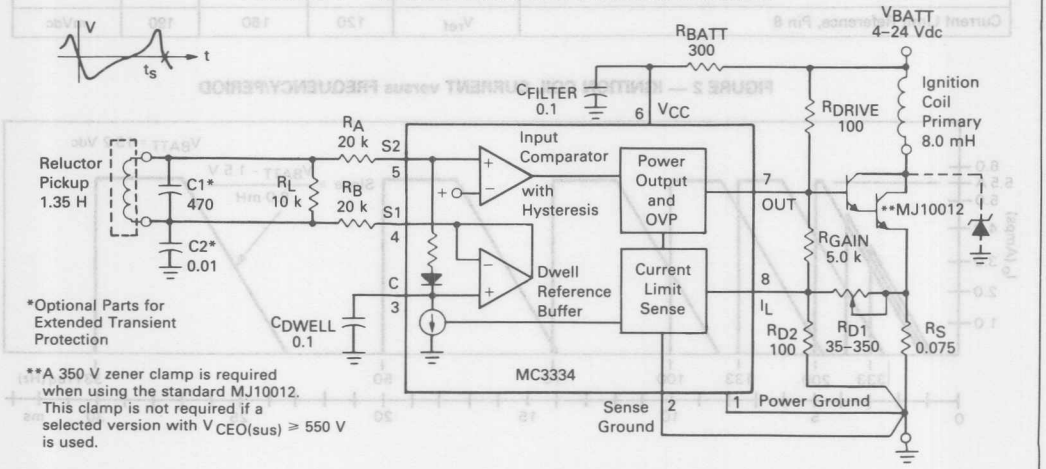
Rating	Symbol	Value	Unit
Power Supply Voltage — Steady State Transient 300 ms or less	V_{BATT}	24 90	Volts
Output Sink Current — Steady State Transient 300 ms or less	I_{out}	300 1.0	mA Amps
Junction Temperature	$T_{J(max)}$	150	°C
Operating Temperature Range	T_A	−40 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Power Dissipation, Package Derate above 25°C	P_D	1.25 10	Watts mW/°C

ORDERING INFORMATION

Device	Temperature Range	Package
MC3334P	−40 to +125	Plastic DIP
MCC3334	−40 to +125	Chip
MCCF3334	−40 to +125	Flip-Chip

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FIGURE 1 — BLOCK DIAGRAM AND TYPICAL APPLICATION



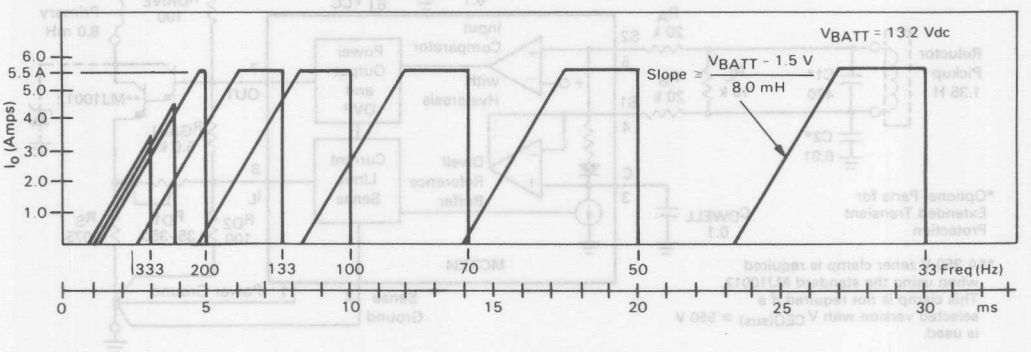
**A 350 V zener clamp is required when using the standard MJ10012. This clamp is not required if a selected version with $V_{CEO(sus)} \geq 550$ V is used.

ELECTRICAL CHARACTERISTICS (T_A = −40 to +125°C, V_{BATT} = 13.2 Vdc, circuit of Figure 1, unless noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Internal Supply Voltage, Pin 6	V_{CC}				Vdc
V_{BATT} = 4.0 Vdc		—	3.5	—	
8.0 Vdc		—	7.2	—	
12.0		—	10.4	—	
14.0		—	11.8	—	
Ignition Coil Current Peak, Cranking RPM 2.0 - 27 Hz	$I_{o(pk)}$				A pk
V_{BATT} = 4.0 Vdc		3.0	3.4	—	
6.0		4.0	5.2	—	
8.0		4.6	5.3	—	
10.0		5.1	5.4	—	
Ignition Coil Current Peak, Normal RPM	$I_{o(pk)}$				A pk
Freq. = 33 Hz		5.1	5.5	—	
133 Hz		5.1	5.5	—	
200 Hz		4.2	5.4	—	
267 Hz		3.4	4.4	—	
333 Hz		2.7	3.4	—	
Ignition Coil On-Time, Normal RPM Range	t_{on}				ms
Freq. = 33 Hz		—	7.5	14.0	
133 Hz		—	5.0	5.9	
200 Hz		—	4.0	4.6	
267 Hz		—	3.0	3.6	
333 Hz		—	2.3	2.8	
Shutdown Voltage	V_{BATT}	25	30	35	Vdc
Input Threshold (Static Test)	V_{S2}-V_{S1}				mVdc
Turn-on		—	360	—	
Turn-off		—	90	—	
Input Threshold Hysteresis	V_{S2}-V_{S1}	75	—	—	mVdc
Input Threshold (Active Operation)	V_{S2}				Vdc
Turn-on		—	1.8	—	
Turn-off		—	1.5	—	
Total Circuit Lag from t_s (Figure 1) until Ignition Coil Current Falls to 10%		—	60	120	μs
Ignition Coil Current Fall Time (90%-10%)		—	4.0	—	μs
Saturation Voltage I.C. Output (Pin 7) (R_{DRIVE} = 100 Ω)	$V_{CE(sat)}$				mVdc
V_{BATT} = 10 Vdc		—	120	—	
30 Vdc		—	280	—	
50 Vdc		—	540	—	
Current Limit Reference, Pin 8	V_{ref}	120	160	190	mVdc

10

FIGURE 2 — IGNITION COIL CURRENT versus FREQUENCY/PERIOD



The MC3334 high energy ignition circuit was designed to serve aftermarket Delco five terminal ignition applications. This device, driving a high voltage Darlington transistor, offers an ignition system which optimizes spark energy at minimum power dissipation. The IC is pinned out to permit thick film or printed circuit module design without any crossovers.

CIRCUIT DESCRIPTION

The basic function of an ignition circuit is to permit build-up of current in the primary of a spark coil, and then to interrupt the flow at the proper firing time. The resulting flyback action in the ignition coil induces the required high secondary voltage needed for the spark. In the simplest systems, fixed dwell angle produces a fixed duty cycle, which can result in too little stored energy at high RPM, and/or wasted power at low RPM. The MC3334 uses a variable dc voltage reference, stored on C_{DWELL}, and buffered to the bottom end of the reluctor pickup (S1) to vary the duty cycle at the spark coil. At high RPM, the MC3334 holds the output "off" for approximately 1.0 ms to permit full energy discharge from the previous spark; then it switches the output Darlington transistor into full saturation. The current ramps up at a slope dictated by V_{BATT} and the coil L. At very high RPM the peak current may be less than desired, but it is limited by the coil itself.

As the RPM decreases, the ignition coil current builds up and would be limited only by series resistance losses. The MC3334 provides adjustable peak current regulation sensed by R_S and set by R_{D1}, in this case at 5.5 A, as shown in Figure 2. As the RPM decreases further, the coil current is held at 5.5 A for a short period. This provides a reserve for sudden acceleration, when discharge may suddenly occur earlier than expected. The peak hold period is about 20% at medium RPM, decreasing to about 10% at very low RPM. (Note: 333 Hz = 5000 RPM for an eight cylinder four stroke engine.) At lower V_{BATT}, the "on" period automatically stretches to accommodate the slower current build-up. At very low V_{BATT} and low RPM, a common condition during cold starting, the "on" period is nearly the full cycle to permit as much coil current as possible.

The output stage of the IC is designed with an OVP circuit which turns it on at $V_{BATT} \approx 30$ V ($V_{CC} \approx 22$ V), holding the output Darlington off. This protects the IC and the Darlington from damage due to load dump or other causes of excessive V_{BATT}.

COMPONENT VALUES

PICKUP — series resistance = 800 Ω ± 10% @ 25°C
inductance = 1.35 H @ 1.0 kHz @ 15 Vrms.

COIL — leakage L = 0.6 mH
primary R = 0.43 Ω ± 5% @ 25°C
primary L = 7.5 to 8.5 mH @ 5.0 A

R_L — load resistor for pick-up = 10 kΩ ± 20%

R_A, R_B — input buffer resistors, provide additional transient protection to the already clamped inputs = 20 k ± 20%

C1, C2 — for reduction of high frequency noise and spark transients induced in pick-up and leads; optional and non-critical

R_{BATT} — provides load dump protection (but small enough to allow operation at V_{BATT} = 4.0 V) = 300 Ω ± 20%

C_{FILTER} — transient filter on V_{CC}, non-critical

C_{DWELL} — stores reference, circuit designed for 0.1 μF ± 20%

R_{GAIN} — R_{GAIN}/R_{D1} sets the dc gain of the current regulator = 5.0 k ± 20%

R_{D2} — R_{D2}/R_{D1} set up voltage feedback from R_S

R_S — sense resistor (PdAg in thick film techniques) = 0.075 Ω ± 30%

R_{DRIVE} — low enough to supply drive to the output Darlington, high enough to keep $V_{CE(sat)}$ of the IC below Darlington turn-on during load dump = 100 Ω ± 20%, 5.0 W

R_{D1} — starting with 35 Ω assures less than 5.5 A, increasing as required to set 5.5 A

$$R_{D1} = \frac{I_{o(pk)} R_S - V_{ref}}{\frac{V_{ref}}{R_{D2}} - \frac{1.4}{R_{GAIN}}} \approx 100\ \Omega\ (nom)$$

GENERAL LAYOUT NOTES

The major concern in the substrate design should be to reduce ground resistance problems. The first area of concern is the metallization resistance in the power ground to module ground and the output to the R_{DRIVE} resistor. This resistance directly adds to the $V_{CE(sat)}$ of the IC power device and if not minimized could cause failure in load dump. The second concern is to reference the sense ground as close to the ground end of the sense resistor as possible in order to further remove the sensitivity of ignition coil current to ground I.R. drops.

All versions were designed to provide the same pinout order viewed from the top (component side) of the board or substrate. This was done to eliminate conductor cross-overs. The standard MC3334 plastic device is numbered in the industry convention, counter-clockwise viewed from the top. The MCC3334 chip version is made from the same die artwork, so it is also counter-clockwise viewed from the top, or bonding pad side. The MCCF3334 "flip" or "bump" chip is made from reversed artwork, so it is numbered clockwise viewed from its bump side. Since this chip is mounted face down, the resulting assembly still has the same counter-clockwise order viewed from above the component surface. All chips have the same size and bonding pad spacing. See Figure 4 for dimensions.

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FIGURE 3 — INTERNAL SCHEMATIC

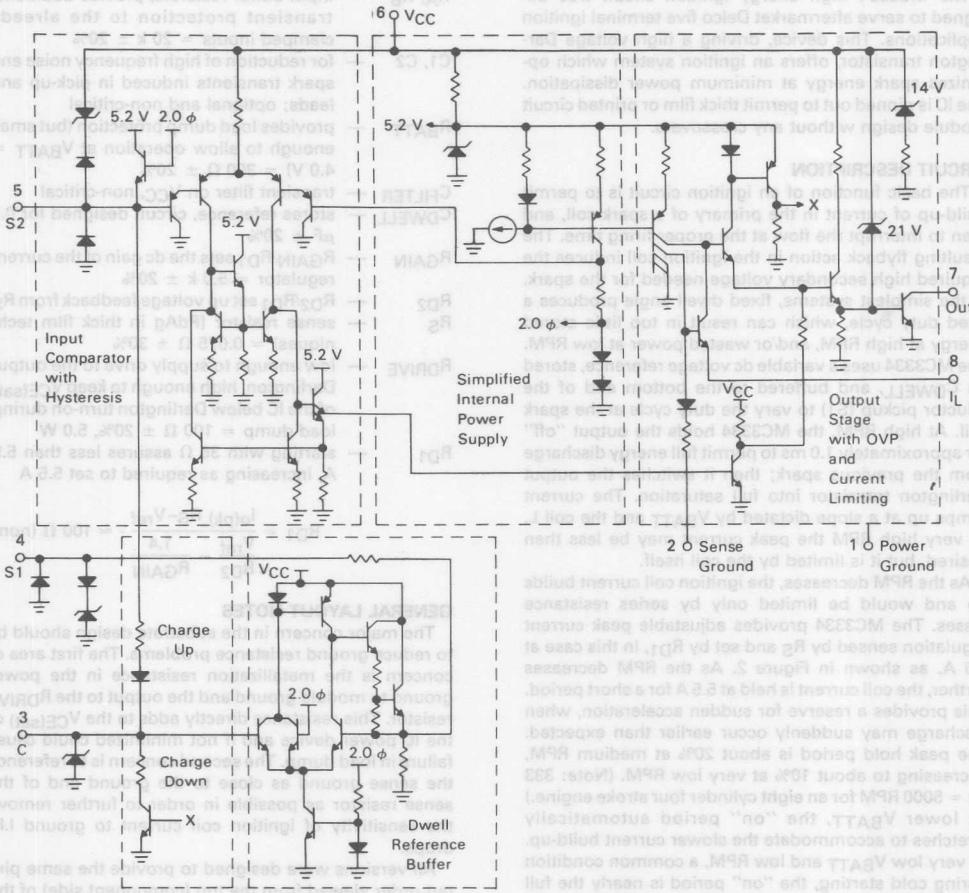
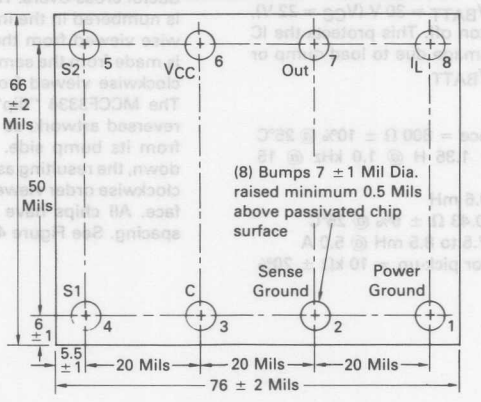


FIGURE 4 — MCCF3334 IGNITION CIRCUIT BUMP SIDE VIEW



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MOTOROLA

MC3397T

Product Preview

SERIES SWITCH TRANSIENT PROTECTION CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT

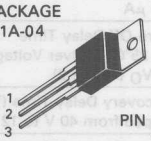
The MC3397T is a Series Switch Transient Protection Circuit. Under normal operating voltage conditions, the device acts as a saturated series pass element with a very low voltage drop for load currents in excess of 750 mA. In the event of an over voltage condition (≥ 17.5 V typ) or high voltage transient of either positive or negative polarity, the MC3397T instantaneously switches to an open circuit (OFF) state, interrupting power to the load and protecting the load during this potentially destructive condition. The device will immediately recover to an ON state when supply voltages fall within the normal operating range.

The MC3397T is fabricated on a power BiMOS process which combines the best features of Bipolar and MOS technologies. The mixed technology provides higher gain PNP output devices and results in Power Integrated Circuits with reduced quiescent current.

The device operates in its ON state over a wide power supply voltage range of 4.0 V to 16 V and can withstand voltage transients (positive or negative) of ±125 V. A rugged PNP output stage along with active clamp circuitry, current limit and thermal shutdown permits driving of all types of loads including inductive. The MC3397T is specified over a wide junction temperature of −40°C to +125°C and is ideally suited for industrial and automotive applications where harsh environments exist.

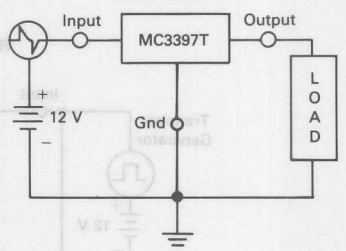
- Transient Protection Up to ±125 V
- Load Currents in Excess of 750 mA
- Low Switch Voltage Drop
- Low Quiescent Current
- Fast Shutdown and Recovery Response to Transients
- On-Chip Current Limit and Thermal Shutdown Circuitry
- Capacitor May Be Used to Support Load During Transient

T SUFFIX
PLASTIC PACKAGE
CASE 221A-04

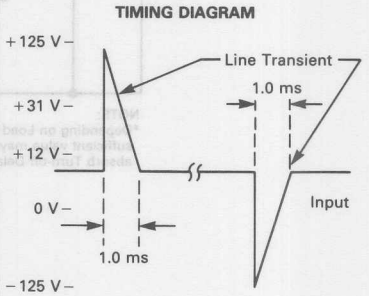


PIN 1. INPUT
2. OUTPUT
3. GROUND

BLOCK DIAGRAM



TIMING DIAGRAM



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage — Continuous	V_{in}	±85	Vdc
Input Voltage — Transient (t = 100 ms) (t = 1.0 ms)	$V_{in(t)}$	±125	V
Output Current	I_O	Internally Limited	A
Power Dissipation and Thermal Characteristics T_A = +25°C Derate above T_A = +25°C Thermal Resistance Junction to Ambient T_C = +25°C Derate above T_C = +25°C Thermal Resistance Junction to Case	 P_D $1/\theta JA$ θJA P_D $1/\theta JA$ θJA	 2.0 16 62.5 25 200 5.0	 Watts mW/°C °C/W Watts mW/°C °C/W
Operating Junction Temperature Range	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

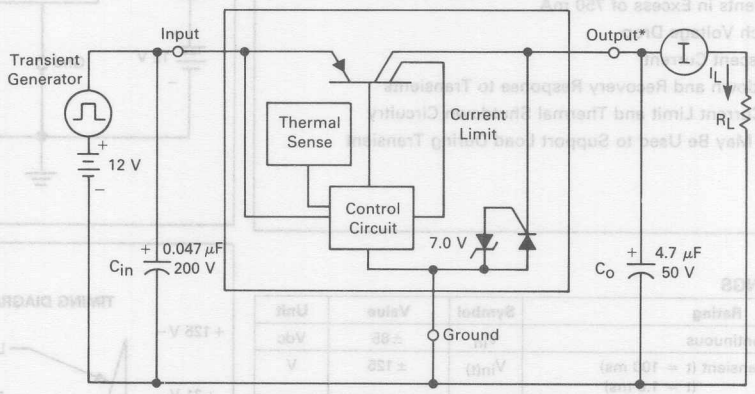
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ELECTRICAL CHARACTERISTICS (V_{in} = +12 V, I_L = 150 mA, −40°C ≤ T_J ≤ +125°C unless otherwise noted)*

Characteristic	Symbol	Min	Typ	Max	Unit
Minimum Operating Voltage	$V_{in(min)}$	—	2.5	4.5	V
Quiescent Current	I_B				mA
I_L = 150 mA, V_{in} = +4.5 V		—	3.0	10	
I_L = 500 mA, V_{in} = +12 V		—	8.0	30	
I_L = 750 mA, V_{in} = +16 V		—	15	50	
Switch Voltage Drop	$V_{in}-V_O$				mV
I_L = 150 mA, V_{in} = +4.5 V		—	175	300	
I_L = 500 mA, V_{in} = +12 V		—	300	500	
I_L = 750 mA, V_{in} = +16 V		—	425	750	
Output Current Limit V_O = 0 V	I_{SC}	0.8	1.5	2.5	A
Output Leakage Current 36 V < V_{in} ≤ 55 V, V_O = 0 V	I_{Leak}	—	10	—	mA
Over Voltage Shutdown Threshold I_L ≤ 100 μA	$V_{in(OV)}$	16	17.25	18.5	V
Output Turn-Off Delay Time (T_J = +25°C) to Over Voltage Condition, V_{in} stepped from 12 V to 40 V V ≤ 0.9 V_O (Figure 2)	$t_{DLY(OV)}$	—	14	—	μs
Output Recovery Delay Time (T_J = +25°C) V_{in} stepped from 40 V to 12 V, V ≥ 0.9 V_O (Figure 2)	t_{RCVY}	—	7.0	—	μs

*Typical Values Represent Characteristics of Operation at T_J = +25°C.

FIGURE 1 — TRANSIENT RESPONSE TEST CIRCUIT



NOTE:
*Depending on Load Current and Transient Duration, an Output Capacitor (C_O) of sufficient value may be used to hold up Output Voltage during the Transient, and absorb Turn-off Delay Voltage Overshoot.

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FIGURE 2 — RESPONSE TIME DIAGRAM

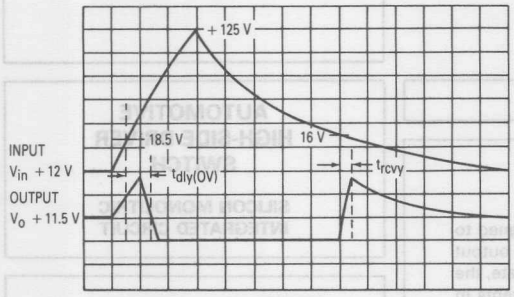


FIGURE 3 — SWITCH DROP versus LOAD CURRENT

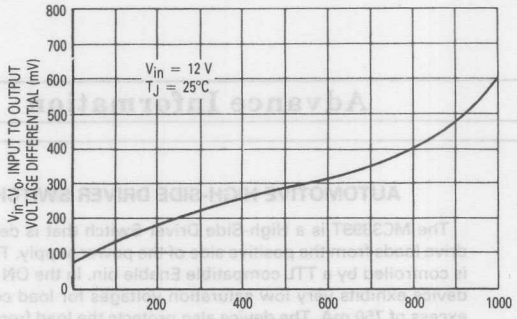
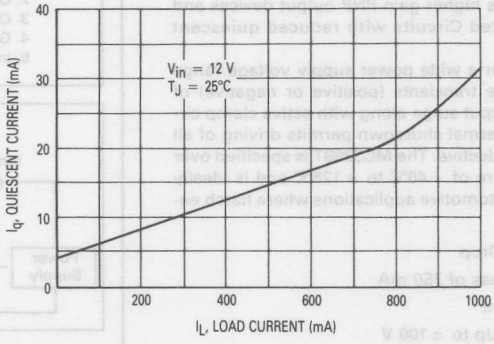


FIGURE 4 — QUIESCENT CURRENT versus LOAD CURRENT



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MC3399T

Advance Information

AUTOMOTIVE HIGH-SIDE DRIVER SWITCH

AUTOMOTIVE HIGH-SIDE DRIVER SWITCH

SILICON MONOLITHIC INTEGRATED CIRCUIT

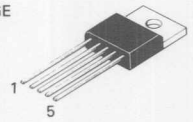
The MC3399T is a High-Side Driver Switch that is designed to drive loads from the positive side of the power supply. The output is controlled by a TTL compatible Enable pin. In the ON state, the device exhibits very low saturation voltages for load currents in excess of 750 mA. The device also protects the load from positive or negative going high voltage transients by becoming an open circuit and isolating the transient for its duration from the load.

The MC3399T is fabricated on a power BIMOS process which combines the best features of Bipolar and MOS technologies. The mixed technology provides higher gain PNP output devices and results in Power Integrated Circuits with reduced quiescent current.

The device operates over a wide power supply voltage range and can withstand voltage transients (positive or negative) of ±100 V. A rugged PNP output stage along with active clamp circuitry, current limit and thermal shutdown permits driving of all types of loads including inductive. The MC3399T is specified over a wide junction temperature of −40°C to +125°C and is ideally suited for industrial and automotive applications where harsh environments exist.

- Low Switch Voltage Drop
- Load Currents in Excess of 750 mA
- Low Quiescent Current
- Transient Protection Up to ±100 V
- TTL Compatible Enable Input
- On-Chip Current Limit and Thermal Shutdown Circuitry

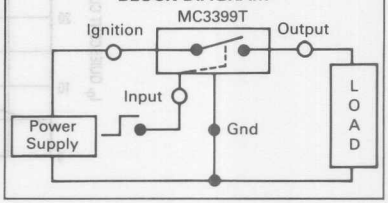
T SUFFIX
PLASTIC PACKAGE
CASE 314D-01



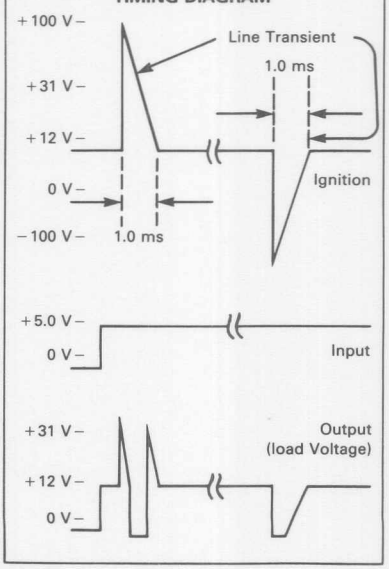
Pin 1. Ignition
2. Output
3. Output
4. Ground
5. Input

(Heatsink surface connected to Pin 2)

BLOCK DIAGRAM



TIMING DIAGRAM



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Ignition Input Voltage — Continuous	V_{IGN}	+25 −12	Vdc
Ignition Input Voltage — Transient t = 100 ms t = 1.0 ms	V_{IGN}	 ±60 ±100	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Output Current	I_O	Internally Limited	A
Power Dissipation and Thermal Characteristics T_A = +25°C Derate above T_A = +25°C	 P_D $1/\theta_{JA}$	 2.0 16	 Watts mW/°C
Thermal Resistance Junction to Ambient T_C = +25°C Derate above T_C = +25°C Thermal Resistance Junction to Case	θ_{JA} P_D $1/\theta_{JA}$ θ_{JA}	65 25 200 5.0	°C/W Watts mW/°C °C/W
Operating Junction Temperature Range	T_J	−40 to +150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

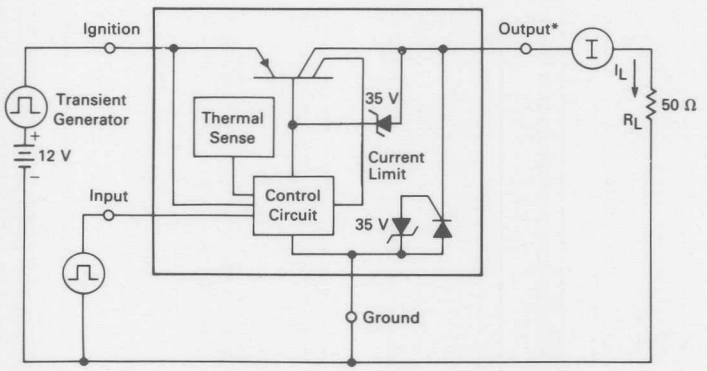
This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS (V_{IGN} = +12 V, I_L = 150 mA, −40°C ≤ T_J = +125°C, V Input = "1" unless noted)*

Characteristic	Symbol	Min	Typ	Max	Unit
Operating Voltage	$V_{IGN(min)}$	4.5	—	—	V
Switch Voltage Drop (Saturation)	V_{IGN}-V_O				V
V_{IGN} = 4.5 V I_O = 150 mA T_J = 25°C		—	0.2	0.5	
I_O = 200 mA T_J = −40°C		—	0.3	0.5	
I_O = 125 mA T_J = 125°C		—	0.3	0.5	
V_{IGN} = 12 V I_O = 425 mA T_J = 25°C		—	0.3	0.7	
I_O = 550 mA T_J = −40°C		—	0.3	0.7	
V_{IGN} = 16 V I_O = 375 mA T_J = 125°C		—	0.4	0.7	
Quiescent Current	I_{GND}				mA
V_{IGN} = 12 V I_O = 150 mA T_J = 25°C		—	12	50	
I_O = 550 mA T_J = −40°C		—	25	100	
I_O = 300 mA T_J = 125°C		—	10	50	
Output Current Limit V_O = 0 V	I_{SC}	—	1.6	2.5	A
Output Leakage Current V_{IGN} = 12 V, Input = "0"	I_{Leak}	—	10	150	μA
Input Voltage					V
High Logic State	V_{IH}	2.0	—	—	
Low Logic State	V_{IL}	—	—	0.8	
Input Current					μA
High Logic State (V_{IH} = 5.5 V)	I_{IH}	—	120	—	
Low Logic State (V_{IL} = 0.4 V)	I_{IL}	—	20	—	
Output Turn-On Delay Time Input = "0" → "1," T_J = +25°C (Figures 1 and 2)	$t_{DLY(on)}$	—	50	—	μs
Output Turn-Off Delay Time Input = "1" → "0," T_J = +25°C (Figures 1 and 2)	$t_{DLY(off)}$	—	5.0	—	μs
Over Voltage Shutdown Threshold	$V_{in(OV)}$	26	31	36	V
Output Turn-Off Delay Time (T_J = +25°C) to Over Voltage Condition, V_{in} stepped from 12 V to 40 V, V ≤ 0.9 V_O (Figures 1 and 2)	t_{DLY}	—	2.0	—	μs
Output Recovery Delay Time (T_J = +25°C) V_{IGN} stepped from 40 V to 12 V, V ≥ 0.9 V_O (Figures 1 and 2)	t_{RCVY}	—	5.0	—	μs

NOTE:
*Typical Values Represent Characteristics of Operation at T_J = +25°C.

FIGURE 1 — TRANSIENT RESPONSE TEST CIRCUIT



NOTE:
*Depending on Load Current and Transient Duration, an Output Capacitor (C_O) of sufficient value may be used to hold up Output Voltage during the Transient, and absorb Turn-off Delay Voltage Overshoot.

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FIGURE 2 — RESPONSE TIME DIAGRAM

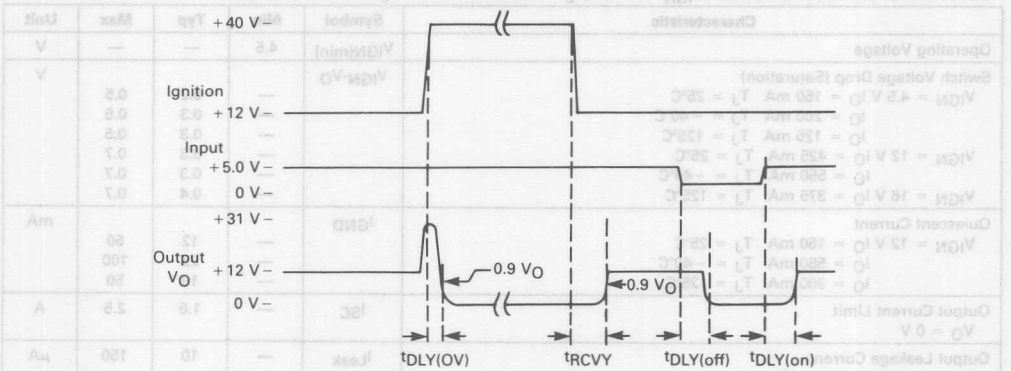


FIGURE 3 — SWITCH VOLTAGE DROP versus LOAD CURRENT

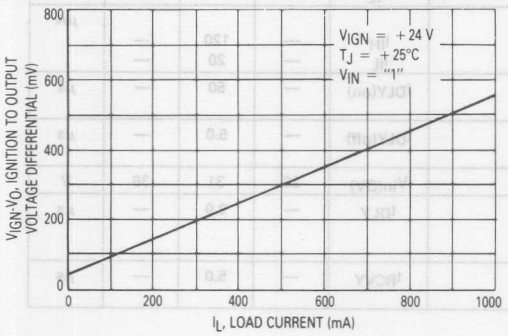
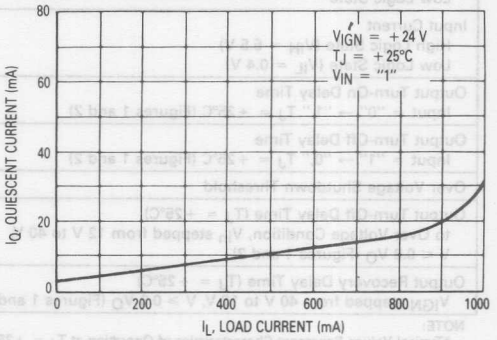


FIGURE 4 — QUIESCENT CURRENT versus LOAD CURRENT



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MOTOROLA

MC3484S2-1
MC3484S4-1

INTEGRATED SOLENOID DRIVER

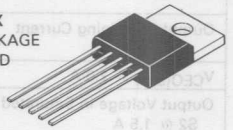
The MC3484 is an integrated monolithic solenoid driver. Its typical function is to apply full battery voltage to fuel injector(s) for rapid current rise, in order to produce positive injector opening. When load current reaches a preset level (4.0 A in MC3484S4 or 2.4 A in MC3484S2) the injector driver reduces the load current by a 4-to-1 ratio and operates as a constant current supply. This condition holds the injector open and reduces system dissipation. Other solenoid or relay applications could be served by the MC3484. Two high impedance inputs are provided which permit a variety of control options and can be driven by TTL or CMOS logic.

- Microprocessor Compatible Inputs
- On-Chip Power Device
  - MC3484S2-1 2.4 A Peak 0.6 A Sustain
  - MC3484S4-1 4.0 A Peak 1.0 A Sustain
- Low Thermal Resistance to Grounded Tab — $R_{\theta JC}$ = 2.5°C/W
- Overvoltage Protection Cutoff
- Low Saturation Voltage — $V_{CE(sat)}$ = 1.6 V Typ @ 4.0 A
- Uncompromised Performance −40°C to +85°C Junction Temperature
- Fully Functional from V_{bat} = 4.0 V to 24 V
- High $V_{CEO(sus)}$ = 42 V min @ $I_{SUSTAIN}$
- Alternate Lead Forms are Available

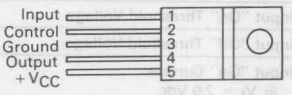
SOLENOID DRIVER
2.4 A — S2
4.0 A — S4

SILICON MONOLITHIC INTEGRATED CIRCUIT

S SUFFIX
PLASTIC PACKAGE
CASE 314D



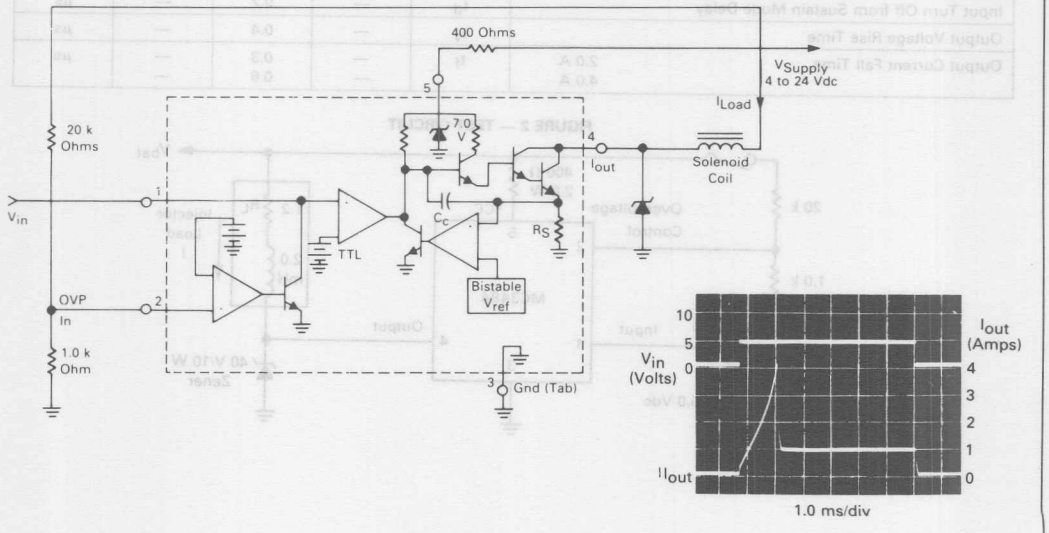
PIN CONNECTIONS
UNFORMED PACKAGE



ORDERING INFORMATION

Device	Tested Ambient Temperature Range	Peak Current
MC3484S2-1	−40 to +85°C	2.4 A
MC3484S4-1	−40 to +85°C	4.0 A

FIGURE 1 — TYPICAL APPLICATION
Single Injector with Overvoltage Protection at 30 V (V_{bat})



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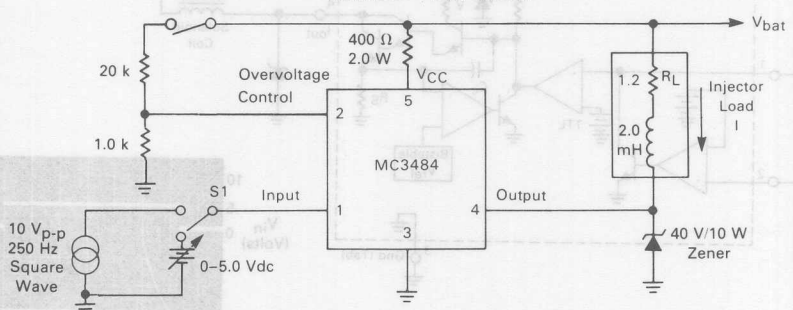
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{bat})	V_{bat}	24	Volts
Input (Pin 1)	V_{in}	−6.0 to +24	V
Control (Pin 2)	V_{cont}	0 to +5.0	V
Internal Regulator (Pin 5)	—	50	mA
Junction Temperature	T_J	150	°C
Operating Temperature (Tab Temperature)	T_A	−40 to +105	°C
Storage Temperature	T_{stg}	−65 to +150	°C
Thermal Resistance, Junction to Case	θ_{JC}	2.5	°C/W

ELECTRICAL CHARACTERISTICS (V_{bat} = 12 Vdc, T_C = −40° to +85°C, test circuit of Figure 2, unless noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Output Peak Current	S4-1 S2-1	$I_{pk(sense)}$	3.6 1.7	4.0 2.4	5.2 2.9	A
Output Sustaining Current		I_{sus}	0.95 0.50	1.0 0.6	1.3 0.7	A
$V_{CEO(sus)}$ @ 2.0 A		—	42	50	—	V
Output Voltage in Saturated Mode S2 @ 1.5 A S4 @ 3.0 A		V_{out}	 — —	 1.2 1.6	 — —	V
Internal Regulated Voltage (V_{CC}, Figure 2)		V_{reg}	—	7.1	—	V
Input "On" Threshold Voltage		V_{on}	—	1.4	2.0	V
Input "Off" Threshold Voltage		V_{off}	0.7	1.3	—	V
Input "On" Current @ V_I = 2.0 Vdc @ V_I = 5.0 Vdc		I_{in}	 — —	 50 220	 — —	μA
Control "On" Threshold Voltage (Pin 2)		V_{cont}	—	1.5	—	V
Control "On" Current		I_{in2}	—	75	—	μA
Control Pin Impedance		V_1 Low	—	10	—	kΩ
Input Turn On Delay		t_i	—	0.5	—	μs
I_{pk} sense to I_{sus} delay		t_p	—	60	—	μs
Control Signal Delay		t_t	—	15	—	μs
Input Turn Off from Saturated Mode Delay		t_s	—	1.0	—	μs
Input Turn Off from Sustain Mode Delay		t_d	—	0.2	—	μs
Output Voltage Rise Time		t_v	—	0.4	—	μs
Output Current Fall Time	2.0 A 4.0 A	t_f	— —	0.3 0.6	— —	μs

FIGURE 2 — TEST CIRCUIT



GENERAL INFORMATION

Inductive actuators such as automotive electronic fuel injectors, relays, solenoids and hammer drivers can be powered more efficiently by providing a high current drive until actuation (pull-in) occurs and then decreasing the drive current to a level which will sustain actuation. Pull-in and especially drop-out times of the actuators are also improved.

The fundamental output characteristic of the MC3484 provides a low impedance saturated power switch until the load current reaches a predetermined high-current level and then changes to a current source of lower magnitude until the device is turned off. This output characteristic allows the inductive load to control its actuation time during turn-on while minimizing power and stored energy during the sustain period, thereby promoting a fast turn-off time.

Automotive injectors at present come in two types. The large throttle body injectors have an impedance of about 2.0 mH and 1.2 Ω and require the MC3484S4 driver. The smaller type, popular world-wide, has an impedance of 4.0 mH and 2.4 Ω and needs about a 2.0 A pulse for good results. Some designs are planned which employ two of the smaller types in parallel. The inductance of an injector is much larger at low current, decreasing due to armature movement and core saturation to the values above at rated current.

Operating frequencies range from 5.0 Hz to 250 Hz depending on the injector location and engine type. Duty cycle in some designs reaches 80%.

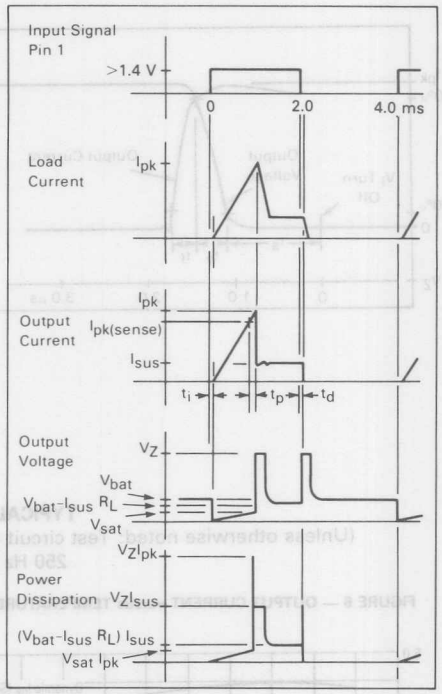
APPLICATIONS INFORMATION

The MC3484 is provided with an input pin (Pin 1) which turns the injector driver "on" and "off." This pin has a nominal trip level of 1.4 V and an input impedance of 20 kΩ. It is internally protected against negative voltages and is compatible with TTL and most other logic.

There is also a control pin (Pin 2) which may be used as an overvoltage, load dump, shutdown. When a nominal 1.5 V is applied to Pin 2, via a 20:1 voltage divider the driver and circuit are set in a safe off state at 30 V (V_{bat}).

Figure 3 shows the operating waveforms for the simplest mode; i.e., with control Pin 2 grounded. When the driver is turned on, the current ramps up to the peak current sense level, where some overshoot occurs because of internal delay. The MC3484 then reduces its output to I_{sus}. The fall time of the device is very rapid (≤1.0 μs), but the decay of the load current takes 150 to 220 μs, while dumping the load energy into the protection zener clamp. It is essential that the zener voltage

FIGURE 3 — OPERATING WAVEFORMS (Max Frequency 250 Hz, Pin 2 Grounded)



be lower than the $V_{CEO(sus)}$, but not so low as to greatly stretch the load current decay time. Without the zener, the discharge of the load energy would be totally into the MC3484, which, for the high current applications, could cause the device to fail. (See SOA, Figure 11.)

Also in Figure 3 is the graphically derived instantaneous power dissipation of the MC3484. It shows that, for practical purposes, the worst case dissipation is less than (I_{sus}) (V_{bat}) (duty cycle).

Provided in Figures 3 and 4 are definitions of the switching intervals specified in the Electrical Characteristics. Figure 5 shows that the critical switching parameters stay under control at elevated temperatures.

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FIGURE 4 — SWITCHING WAVEFORMS
(Expanded Time Scale)

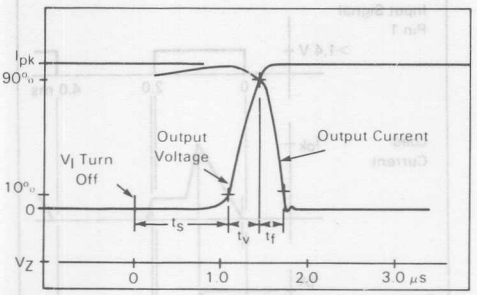
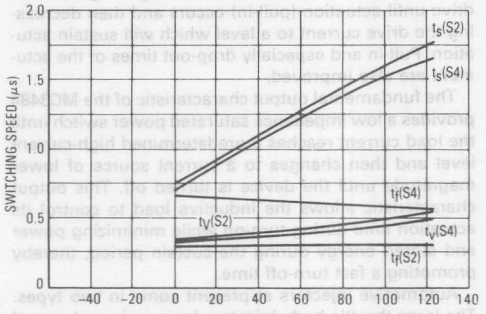


FIGURE 5 — SWITCHING SPEED versus TEMPERATURE



TYPICAL CHARACTERISTICS

(Unless otherwise noted: Test circuit of Figure 2, V_{bat} = 12 Vdc, T_C = −40° to +85°C, 250 Hz square wave input)

FIGURE 6 — OUTPUT CURRENT versus TEMPERATURE

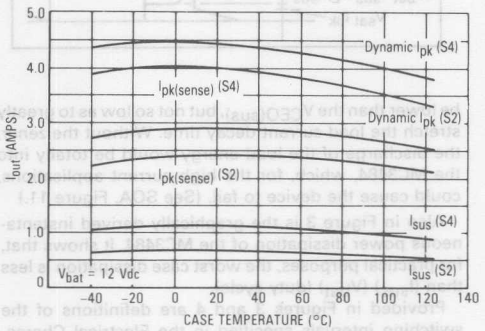
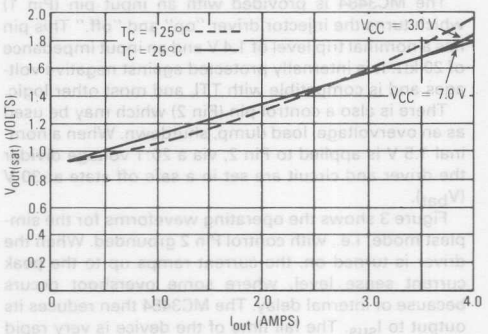


FIGURE 7 — SATURATION VOLTAGE



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TYPICAL CHARACTERISTICS

(Unless otherwise noted: Test circuit of Figure 2, V_{bat} = 12 Vdc, T_C = −40° to +85°C, 250 Hz square wave input)

FIGURE 8 — OUTPUT CURRENT versus SUPPLY VOLTAGE

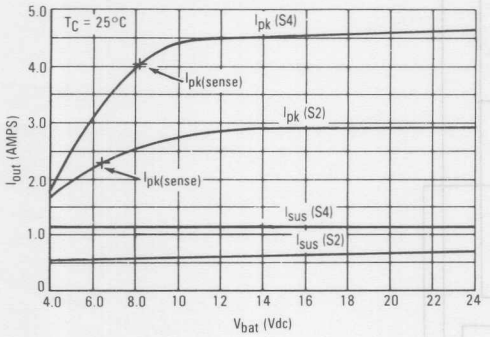


FIGURE 9 — OPERATING VOLTAGES

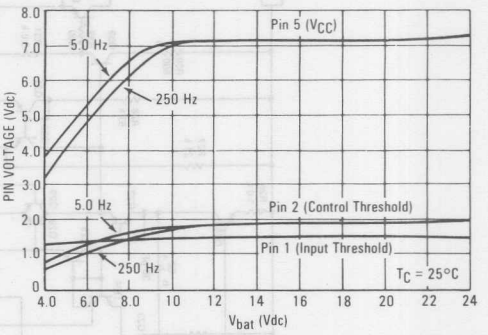


FIGURE 10 — BREAKDOWN VOLTAGE versus TEMPERATURE

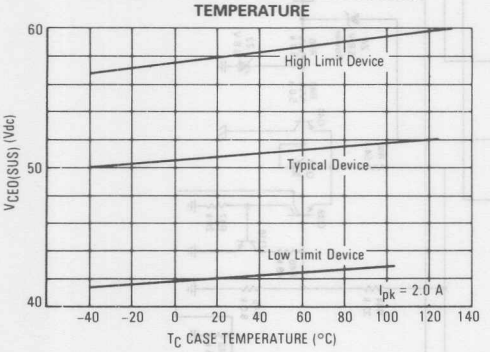
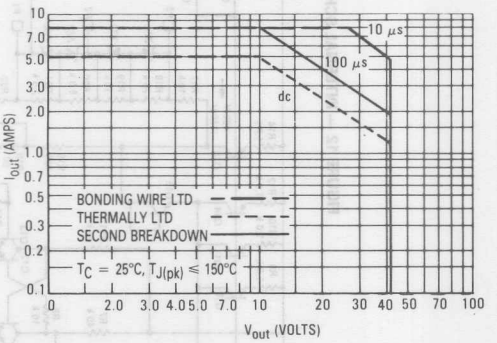
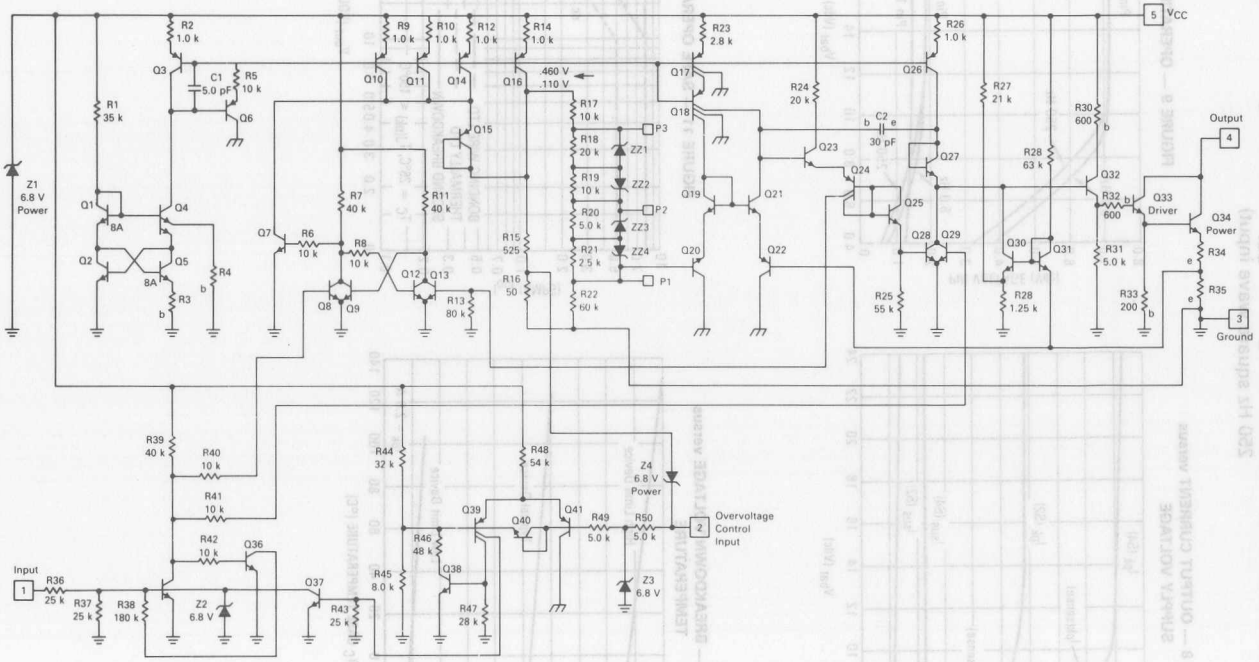


FIGURE 11 — SAFE OPERATING AREA



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FIGURE 12 — INTERNAL SCHEMATIC



MOTOROLA

TCF7000

Advance Information

PRESSURE TRANSDUCER AMPLIFIER

This circuit is ideal for automotive and industrial applications and consists of two low power operational amplifiers with identical characteristics except the outputs which have the following configurations:

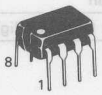
AMPLIFIER A — NPN Transistor driving an on-chip current source

AMPLIFIER B — NPN Transistor with pull-up resistor

- Short Circuit Protected Outputs
- True Differential Input Stage
- Single Supply Operation 4 to 20 Volts
- Low Input Bias Currents
- Internally Compensated
- Common Mode Range Extends to Negative Supply
- Large Output Voltage Swing from Gnd to V_{CC}
- Large Current Drive Capability
- Very Low Input Offset Voltage
- Operating Ambient Temperature Range of −40°C to +125°C

PRESSURE TRANSDUCER AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 626-05

D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SO-08



PIN ASSIGNMENTS
(Top View)

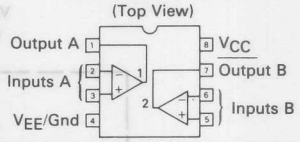
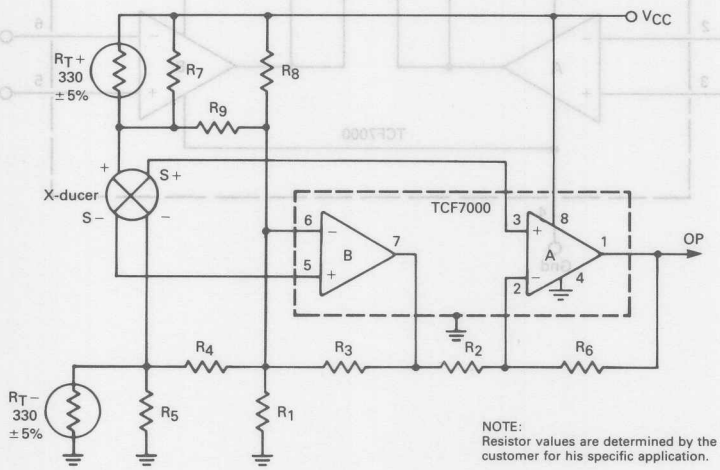


FIGURE 1 — TYPICAL APPLICATION



NOTE:
Resistor values are determined by the customer for his specific application.

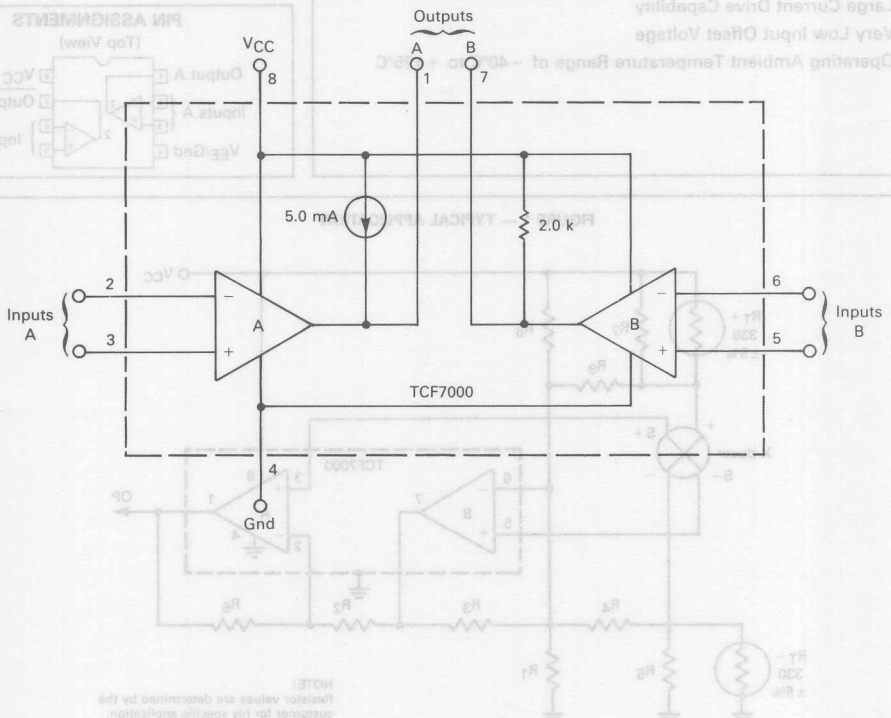
This document contains information on a new product. Specifications and information herein are subject to change without notice.

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ELECTRICAL CHARACTERISTICS (at T_A = 25°C and V_{CC} = 5.0 V)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Output	V_{CC}	4.0	—	20	V
Short Circuit Duration			Continuous		
Source Current (Amp. A)	I_L	3.0	5.0	—	mA
Sink Current		—	50	—	mA
High Voltage at I_L = −5.0 mA (Amp. A)	V_{OH1}	—	V_{CC} − 0.12	—	V
Low Voltage at I_L = 5.0 mA	V_{OL}	—	0.12	—	V
Pull Up Resistor (Amp. B)		—	2.0	3.0	KOhm
Input					
Common Mode Voltage Range		1.0	—	V_{CC} − 1	
Offset Voltage		—	1.0	3.0	mV
Temperature Coefficient of Offset Voltage		—	2.0	—	μV/°C
Offset Current		—	3.0	—	nA
Bias Current		—	30	—	nA
Large Signal Open Loop Gain		—	100	—	V/mV
Bandwidth Unity Gain		—	100	—	kHz
Common Mode Rejection		50	100	—	dB
Power Supply Rejection		50	80	—	dB
Power Supply Current (Outputs High State)		—	2.2	—	mA

FIGURE 2 — OUTPUT CONFIGURATION



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MOTOROLA

UAA1041

AUTOMOTIVE DIRECTION INDICATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

AUTOMOTIVE DIRECTION INDICATOR

. . . designed for use in conjunction with a relay in automotive applications. It is also applicable for other warning lamps such as "handbrake ON," etc.

- Defective Lamp Detection
- Overvoltage Protection
- Short Circuit Detection and Relay Shutdown to Prevent Risk of Fire
- Reverse Battery Connection Protection
- Integrated Suppression Clamp Diode

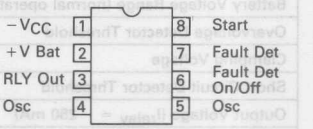
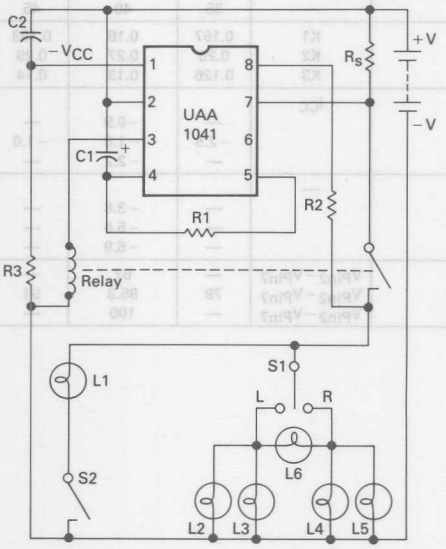
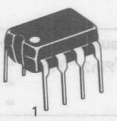


FIGURE 1 — TYPICAL AUTOMOTIVE SYSTEM



L1: 1.2 W warning light handbrake ON L2, L3, L4, L5: 21 W, turn signals

R1 = 75 k
R2 = 3.3 k
R3 = 220 Ω
Rs = 30 mΩ
C1 = 5.6 μF
C2 = 0.047 μF



P SUFFIX
PLASTIC PACKAGE
CASE 626-05



D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SO-8

10

MAXIMUM RATINGS

Rating	Pin	Value	Unit
Current: Continuous/Pulse*	1	+150/+500 −35/−500	mA
	2	+/−350/1900	
	3	+/−300/1400	
	8	+/−25/50	
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	−40 to +100	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

*One pulse with an exponential decay and with a time constant of 500 ms.

ELECTRICAL CHARACTERISTICS (T_1 = 25°C)

Characteristics		Symbol	Min	Typ	Max	Unit
Battery Voltage Range (normal operation)		V_B	8.0	—	18	V
Overvoltage Detector Threshold	($V_{Pin2}-V_{Pin1}$)	$D_{th(OV)}$	19	20.2	21.5	V
Clamping Voltage	($V_{Pin2}-V_{Pin1}$)	V_{IK}	29	31.5	34	V
Short Circuit Detector Threshold	($V_{Pin2}-V_{Pin7}$)	$D_{th(SC)}$	0.63	0.7	0.77	V
Output Voltage (I_{relay} = −250 mA)	($V_{Pin2}-V_{Pin3}$)	V_O	—	—	1.5	V
Starter Resistance $R_{st} = R_2 + R_{Lamp}$		R_{st}	—	—	3.6	kΩ†
Oscillator Constant (normal operation)		Kn	1.4	1.5	1.6	—
Temperature Coefficient of Kn		kn	—	-1.5×10^{-3}	—	1/°C
Duty Cycle (normal operation)		—	45	50	55	%
Oscillator Constant — (1 lamp defect of 21 W)		KF	0.63	0.68	0.73	—
Duty Cycle (1 lamp defect of 21 W)		—	35	40	45	%
Oscillator Constant		K1 K2 K3	0.167 0.25 0.126	0.18 0.27 0.13	0.193 0.29 0.14	—
Current Consumption (relay off) Pin 1; at $V_{Pin2}-V_{Pin1}$ = 8.0 V = 13.5 V = 18 V		I_{CC}	 — −2.5 —	 −0.9 −1.6 −2.2	 — −1.0 —	mA
Current Consumption (relay on) Pin 1; at $V_{Pin2}-V_{Pin1}$ = 8.0 V = 13.5 V = 18 V		—	 — — —	 −3.8 −5.6 −6.9	 — — —	mA
Defect Lamp Detector Threshold at V_{Pin2} to − V_B = 8.0 V and R_3 = 220 Ω = 13.5 V = 18 V		$V_{Pin2}-V_{Pin7}$ $V_{Pin2}-V_{Pin7}$ $V_{Pin2}-V_{Pin7}$	— 79 —	67 85.3 100	— 91 —	mV

†See Note 1 of Application Information

10

flasher relay. Figure 2 shows the typical system configuration with the external components. It consists of a network (R1, C1) to determine the oscillator frequency, shunt resistor (R_S) to detect defective bulbs and short circuits in the system, and two current limiting resistors (R_2/R_3) to protect the IC against load dump transients. The circuit can be used either with or without short-circuit detection.

The lightbulbs L2, L3, L4, L5 are the turn signal indicators with the dashboard-light L6. When switch S1 is closed, after a time delay of t_1 (in our example t_1 = 75 ms), the relay will be actuated. The corresponding lightbulbs L2, L3 (or L4, L5) will flash at the oscillator frequency, independent of the battery voltage of 8.0 V to 18 V. The flashing cycle stops and the circuit is reset to the initial position when the switch S1 is open.

The circuit features overvoltage, defective lamp and short circuit detection.

Overvoltage detection:
Senses the battery voltage. When this voltage exceeds 20.2 V (this is the case when two batteries are connected in series), the relay will be turned off to protect the lightbulbs.

Lightbulb defect detector:
Senses the current through the shunt resistor R_S. When one of the lightbulbs is defective, the failure is indicated by doubling the flashing frequency.

Short circuit detector:
Detects excessive current (I_{sh} > 25 A) flowing in the shunt resistor R_S. The detection takes place after a time delay of t_3 (t_3 = 55 ms). In this case, the relay will be turned off. The circuit is reset by switching S1 to the off position.

Operation with short circuit detection:
Pin 6 has to be left open and a capacitor C_2 has to be connected between Pin 1 and Pin 2.

Operation without short circuit detection:
Pin 6 has to be connected to Pin 2 and the use of capacitor C_2 is not necessary.

The circuit can also be used for other warning flashers. In our example, handbrake engaged is signaled by the light L1.

APPLICATION INFORMATION

1. The flashing cycle is started by closing S1.
   The switch position is sensed across resistor R_2 and R_{Lamp} by input 8.
   $R_{st} = R_2 + R_{Lamp}$.
   The condition for the start is: $R_{st} < 3.6\ k\Omega$
   For correct operation leakage resistance from Pin 8 to ground must be greater than 5.6 kΩ.
3. f_F: Flashing frequency in the case of one defective lightbulb of 21 W
   $$f_F = \frac{1}{R_1 C_1 K_F} K_n = 2{,}2 K_F$$
4. t_1: delay at the moment when S1 is closed and first flash $t_1 = K_1 R_1 C$
5. t_2: defective lightbulb detection delay $t_2 = K_2 R_1 C_1$
6. t_3: short circuit detection delay $t_3 = K_1 R_1 C_1$
   In the case of short circuit:
   — it is assumed that the voltage $V_{Pin2} - V_{Pin1} \geq 8.0$ V.
   — The relay will be turned off after delay t_3.
   — The circuit is reset by switching S1 to the off position.
7. The capacitor C2 is not obligatory when the short circuit detector is not used. In this case Pin 6 has to be connected to Pin 2.
8. When overvoltage is sensed ($V_{Pin2} - V_{Pin1}$) the relay is turned off to protect the relay and the lightbulbs against excessive currents.

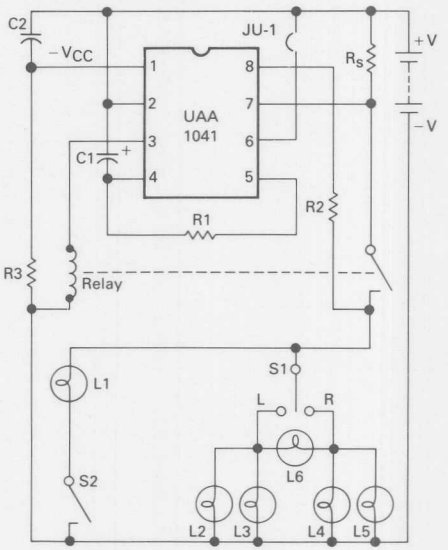


FIGURE 2

PARTS LIST

R1 = 75 kΩ
R2 = 3.3 kΩ
R3 = 220 Ω
R_S = 30 mΩ
Wire Resistor
C1 = 5.6 μF
C2 = 0.047 μF

Relay — Coil Resistance
Range 60 to 800 Ω

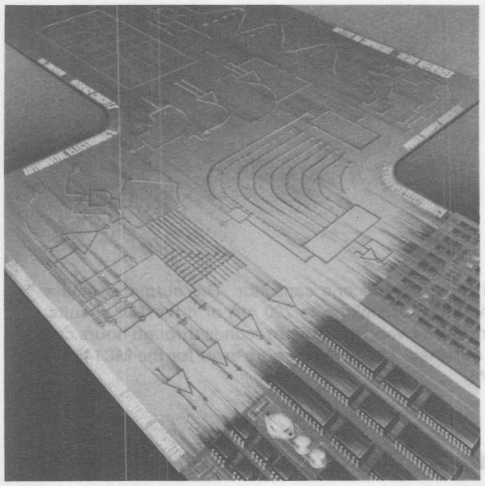
Note: Per text connect jumper JU-1 to bypass short circuit detector. C2 may be deleted also.

10

FIGURE 2

PARTS LIST

R1 = 75 kΩ	Relay — Coil Resistance
R2 = 3.3 kΩ	Range 80 to 800 Ω
R3 = 220 Ω	
R_S = 30 mΩ	Note: Per test connect
Wire Resistor	Jumper JU-1 to bypass
C1 = 5.6 µF	short circuit detector.
C2 = 0.047 µF	C2 may be deleted also.



In Brief . . .

A variety of other analog circuits are provided for special applications with both bipolar and CMOS technologies. These circuits range from the industry-standard analog timing circuits and multipliers.

Selector Guide
- Timing Circuits 11-2
- Multipliers 11-2

Alphanumeric Listing 11-3

Related Application Notes 11-3

Data Sheets 11-4

Other Linear Circuits

11

Other Linear Circuits

Timing Circuits

These highly stable timers are capable of producing accurate time delays or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The output structure can source or sink up to 200 mA or drive TTL circuits. Timing intervals from microseconds through hours can be obtained. The typical timing error for the MC1455 is 1.0%.

Singles

MC1455G,P1,U T_A = 0° to +70°C, Case 601, 626, 693
MC1455BP1 T_A = −40° to +85°C, Case 626

Duals

MC3556L T_A = −55° to +125°C, Case 632
MC3456L,P T_A = 0° to +70°C, Case 632, 646

Multipliers

Linear Four-Quadrant Multipliers

Multipliers are designed for use where the output voltage is a linear product of two input voltages. Typical applications include: multiply, divide, square, root-mean-square, phase detector, frequency doubler, balanced modulator/demodulator, electronic gain control.

MC1594L T_A = −55° to +125°C, Case 620
MC1494L T_A = 0° to +70°C, Case 620

The MC1594/MC1494 is a Variable Transconductance Multiplier with internal level-shift circuitry and voltage regulator. Scale factor, input offsets and output offset are completely adjustable with the use of four external potentiometers. Two complementary regulated voltages are provided to simplify offset adjustment and improve power-supply rejection.

MC1595L T_A = −55° to +125°C, Case 632
MC1495L T_A = 0° to +70°C, Case 632

. . . designed for uses where the output is a linear product of two input voltages. Maximum versatility is assured by allowing the user to select the level shift method. Typical applications include: multiply, divide*, square root,* mean square*, phase detector, frequency doubler, balanced modulator/demodulator, electronic gain control.

*When used with an operational amplifier.

OTHER LINEAR CIRCUITS

TIMING CIRCUITS

Device	Function	Page
MC1455	Timing Circuit	11-4
MC3456	Dual Timing Circuit	11-40
MC3556	Dual Timing Circuit	11-40

MULTIPLIERS

Device	Function	Page
MC1494L	Four-Quadrant Multiplier	11-11
MC1495L	Four-Quadrant Multiplier	11-25
MC1496	Balanced Modulator-Demodulator	See Chapter 8
MC1594L	Four-Quadrant Multiplier	11-11
MC1595L	Four-Quadrant Multiplier	11-25
MC1596	Balanced Modulator-Demodulator	See Chapter 8

RELATED APPLICATION NOTES

Application Note	Title	Related Device
AN489	Analysis and Basic Operation of the MC1595	MC1595L
AN531	MC1596 Balanced Modulator	MC1596

MOTOROLA

MC1455

Specifications and Applications Information

TIMING CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT

TIMING CIRCUIT

The MC1455 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200 mA or drive MTTL circuits.

- Direct Replacement for NE555 Timers
- Timing From Microseconds Through Hours
- Operates in Both Astable and Monostable Modes
- Adjustable Duty Cycle
- High Current Output Can Source or Sink 200 mA
- Output Can Drive MTTL
- Temperature Stability of 0.005% per °C
- Normally "On" or Normally "Off" Output

FIGURE 1 — 22-SECOND SOLID-STATE TIME DELAY RELAY CIRCUIT

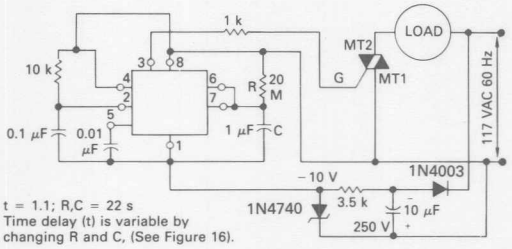
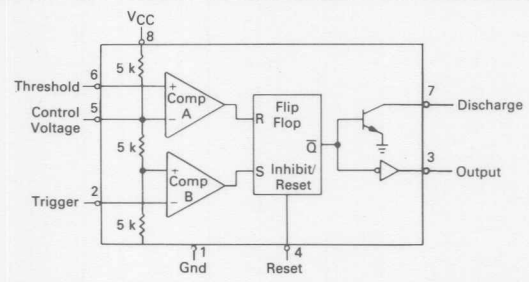


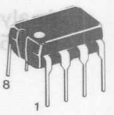
FIGURE 2 — BLOCK DIAGRAM





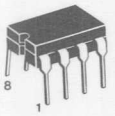
G SUFFIX
METAL PACKAGE
CASE 601-04

1. Ground
2. Trigger
3. Output
4. Reset
5. Control Voltage
6. Threshold
7. Discharge
8. V_{CC}



P1 SUFFIX
PLASTIC PACKAGE
CASE 626-05

U SUFFIX
CERAMIC PACKAGE
CASE 693-02



D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SO-8



ORDERING INFORMATION

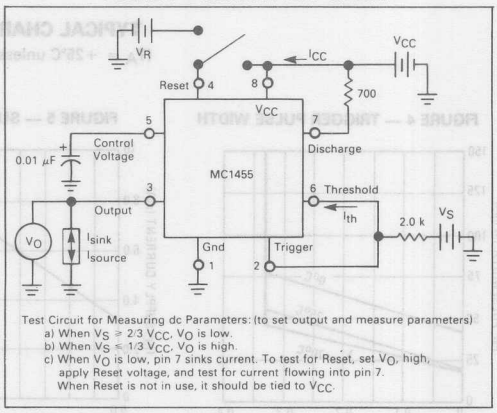
Device	Alternate	Temperature Range	Package
MC1455G	—	0°C to +70°C	Metal Can
MC1455P1	NE555V	0°C to +70°C	Plastic DIP
MC1455D	—	0°C to +70°C	SO-8
MC1455U	—	0°C to +70°C	Ceramic DIP
MC1455BP1	—	−40°C to +85°C	Plastic DIP

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MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+18	Vdc
Discharge Current (Pin 7)	I_7	200	mA
Power Dissipation (Package Limitation) Metal Can Derate above T_A = +25°C Plastic Dual In-Line Package Derate above T_A = +25°C	P_D	 680 4.6 625 5.0	 mW mW/°C mW mW/°C
Operating Temperature Range (Ambient) MC1455B MC1455	T_A	 −40 to +85 0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

FIGURE 3 — GENERAL TEST CIRCUIT



Test Circuit for Measuring dc Parameters: (to set output and measure parameters)
a) When $V_S \geq 2/3\ V_{CC}$, V_O is low.
b) When $V_S \leq 1/3\ V_{CC}$, V_O is high.
c) When V_O is low, pin 7 sinks current. To test for Reset, set V_O high, apply Reset voltage, and test for current flowing into pin 7. When Reset is not in use, it should be tied to V_{CC}.

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = +5.0 V to +15 V unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Operating Supply Voltage Range	V_{CC}	4.5	—	16	V
Supply Current V_{CC} = 5.0 V, R_L = ∞ V_{CC} = 15 V, R_L = ∞ Low State, (Note 1)	I_{CC}	 — —	 3.0 10	 6.0 15	mA
Timing Error (Note 2) R = 1.0 kΩ to 100 kΩ Initial Accuracy C = 0.1 μF Drift with Temperature Drift with Supply Voltage		 — — —	 1.0 50 0.1	 — — —	 % PPM/°C %/Volt
Threshold Voltage	V_{th}	—	2/3	—	xV_{CC}
Trigger Voltage V_{CC} = 15 V V_{CC} = 5.0 V	V_T	 — —	 5.0 1.67	 — —	V
Trigger Current	I_T	—	0.5	—	μA
Reset Voltage	V_R	0.4	0.7	1.0	V
Reset Current	I_R	—	0.1	—	mA
Threshold Current (Note 3)	I_{th}	—	0.1	0.25	μA
Discharge Leakage Current (Pin 7)	I_{dis}	—	—	100	nA
Control Voltage Level V_{CC} = 15 V V_{CC} = 5.0 V	V_{CL}	 9.0 2.6	 10 3.33	 11 4.0	V
Output Voltage Low (V_{CC} = 15 V) I_{sink} = 10 mA I_{sink} = 50 mA I_{sink} = 100 mA I_{sink} = 200 mA (V_{CC} = 5.0 V) I_{sink} = 8.0 mA I_{sink} = 5.0 mA	V_{OL}	 — — — — — —	 0.1 0.4 2.0 2.5 — 0.25	 0.25 0.75 2.5 — — 0.35	V
Output Voltage High (I_{source} = 200 mA) V_{CC} = 15 V (I_{source} = 100 mA) V_{CC} = 15 V V_{CC} = 5.0 V	V_{OH}	 — 12.75 2.75	 12.5 13.3 3.3	 — — —	V
Rise Time of Output	t_{OLH}	—	100	—	ns
Fall Time of Output	t_{OHL}	—	100	—	ns

NOTES:
1. Supply current when output is high is typically 1.0 mA less.
2. Tested at V_{CC} = 5.0 V and V_{CC} = 15 V.
   Monostable mode
3. This will determine the maximum value of $R_A + R_B$ for 15 V operation. The maximum total R = 20 megohms.

(T_A = +25°C unless otherwise noted.)

FIGURE 4 — TRIGGER PULSE WIDTH

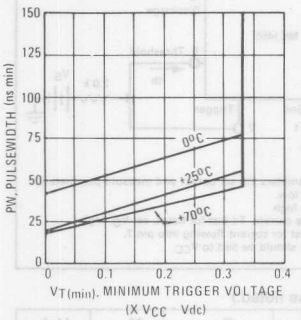


FIGURE 5 — SUPPLY CURRENT

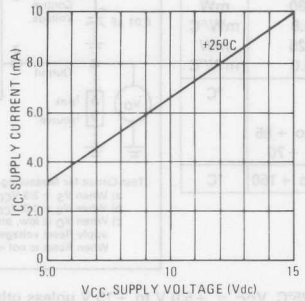


FIGURE 6 — HIGH OUTPUT VOLTAGE

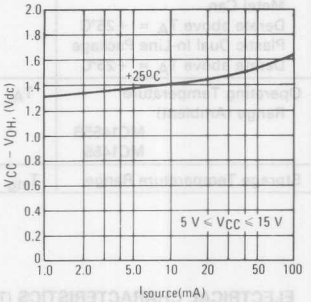


FIGURE 7 — LOW OUTPUT VOLTAGE @ V_{CC} = 5.0 Vdc

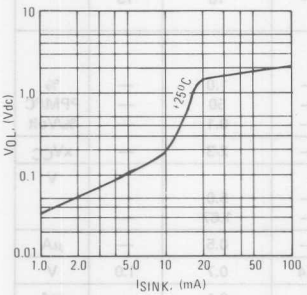


FIGURE 8 — LOW OUTPUT VOLTAGE @ V_{CC} = 10 Vdc

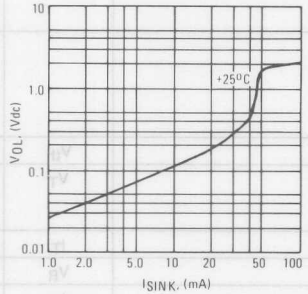


FIGURE 9 — LOW OUTPUT VOLTAGE @ V_{CC} = 15 Vdc

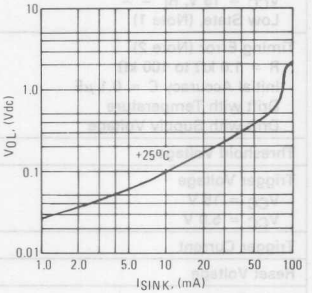


FIGURE 10 — DELAY TIME versus SUPPLY VOLTAGE

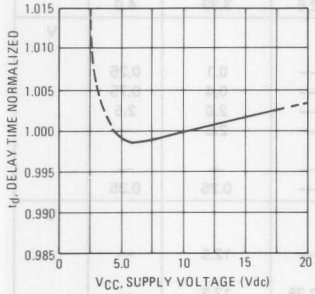


FIGURE 11 — DELAY TIME versus TEMPERATURE

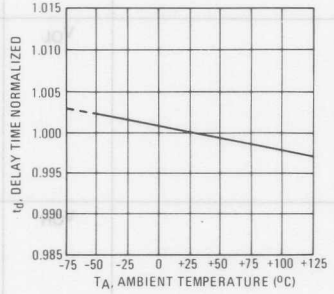
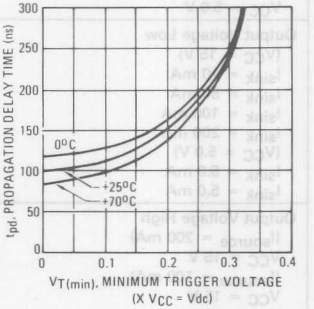
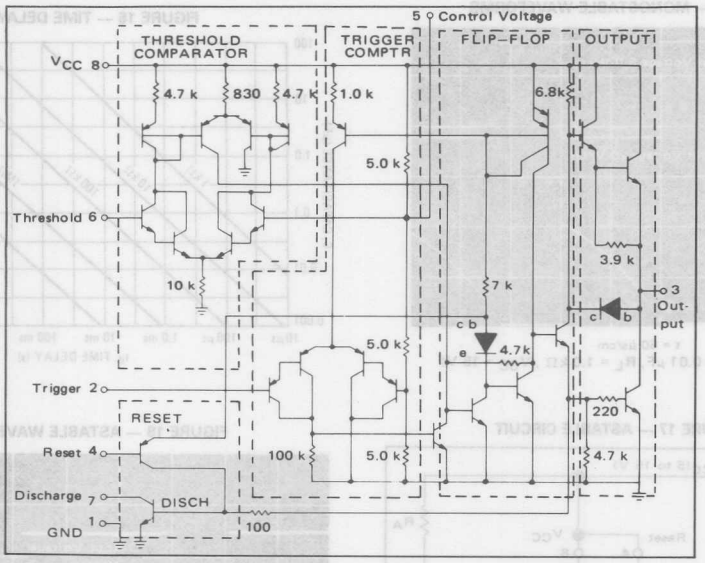


FIGURE 12 — PROPAGATION DELAY versus TRIGGER VOLTAGE



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FIGURE 13 — REPRESENTATIVE CIRCUIT SCHEMATIC



GENERAL OPERATION

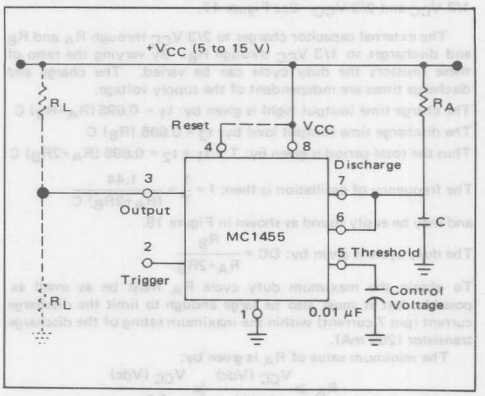
The MC1455 is a monolithic timing circuit which uses as its timing elements an external resistor — capacitor network. It can be used in both the monostable (one-shot) and astable modes with frequency and duty cycle controlled by the capacitor and resistor values. While the timing is dependent upon the external passive components, the monolithic circuit provides the starting circuit, voltage comparison and other functions needed for a complete timing circuit. Internal to the integrated circuit are two comparators, one for the input signal and the other for capacitor voltage; also a flip-flop and digital output are included. The comparator reference voltages are always a fixed ratio of the supply voltage thus providing output timing independent of supply voltage.

Monostable Mode

In the monostable mode, a capacitor and a single resistor are used for the timing network. Both the threshold terminal and the discharge transistor terminal are connected together in this mode, refer to circuit Figure 14. When the input voltage to the trigger comparator falls below 1/3 V_{CC} the comparator output triggers the flip-flop so that it's output sets low. This turns the capacitor discharge transistor "off" and drives the digital output to the high state. This condition allows the capacitor to charge at an exponential rate which is set by the RC time constant. When the capacitor voltage reaches 2/3 V_{CC} the threshold comparator resets the flip-flop. This action discharges the timing capacitor and returns the digital output to the low state. Once the flip-flop has been triggered by an input signal, it cannot be retriggered until the present timing period has been completed. The time that the output is high is given by the equation $t = 1.1\ R_A\ C$. Various combinations of R and C and their associated times are shown in Figure 16. The trigger pulse width must be less than the timing period.

A reset pin is provided to discharge the capacitor thus interrupting the timing cycle. As long as the reset pins is low, the capacitor discharge transistor is turned "on" and prevents the capacitor from charging. While the reset voltage is applied the digital output will remain the same. The reset pin should be tied to the supply voltage when not in use.

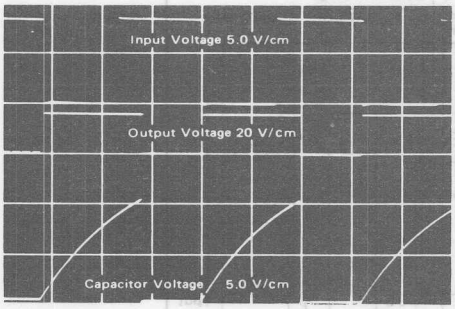
FIGURE 14 — MONOSTABLE CIRCUIT



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GENERAL OPERATION (continued)

FIGURE 15 — MONOSTABLE WAVEFORMS



t = 50 μs/cm
(R_A = 10 kΩ, C = 0.01 μF, R_L = 1.0 kΩ , V_{CC} = 15 V)

FIGURE 16 — TIME DELAY

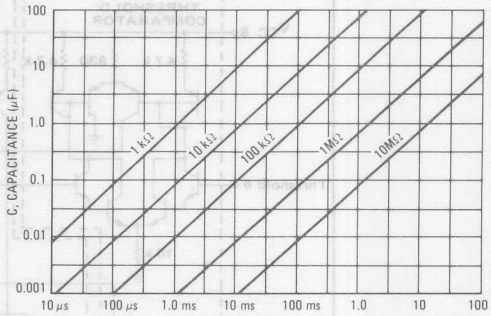


FIGURE 17 — ASTABLE CIRCUIT

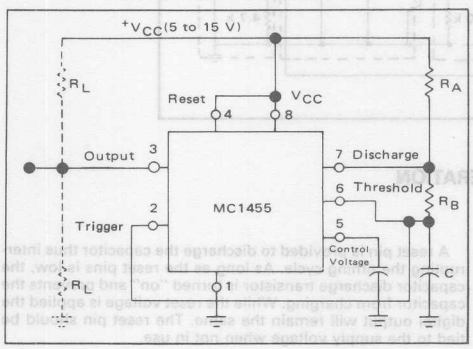
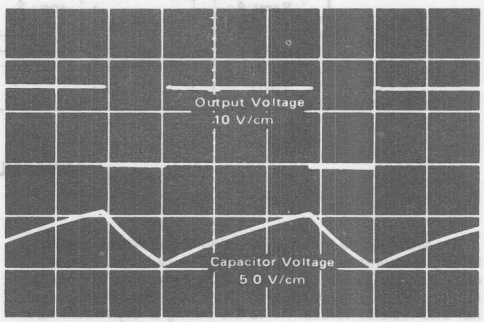


FIGURE 18 — ASTABLE WAVEFORMS



t = 20 μs/cm
(R_A = 5.1 kΩ, C = 0.01 μF, R_L = 1.0 kΩ;
R_B = 3.9 kΩ, V_{CC} = 15 V)

Astable Mode

In the astable mode the timer is connected so that it will retrigger itself and cause the capacitor voltage to oscillate between 1/3 V_{CC} and 2/3 V_{CC}. See Figure 17.

The external capacitor charges to 2/3 V_{CC} through R_A and R_B and discharges to 1/3 V_{CC} through R_B. By varying the ratio of these resistors the duty cycle can be varied. The charge and discharge times are independent of the supply voltage.

The charge time (output high) is given by: $t_1 = 0.695\,(R_A+R_B)\,C$

The discharge time (output low) by: $t_2 = 0.695\,(R_B)\,C$

Thus the total period is given by: $T = t_1 + t_2 = 0.695\,(R_A+2R_B)\,C$

The frequency of oscillation is then: $f = \frac{1}{T} = \frac{1.44}{(R_A+2R_B)\,C}$

and may be easily found as shown in Figure 19.

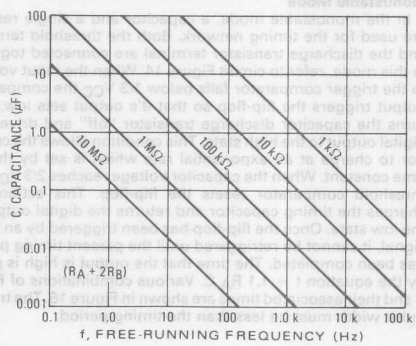
The duty cycle is given by: $DC = \frac{R_B}{R_A+2R_B}$

To obtain the maximum duty cycle R_A must be as small as possible; but it must also be large enough to limit the discharge current (pin 7 current) within the maximum rating of the discharge transistor (200 mA).

The minimum value of R_A is given by:

$$R_A \geq \frac{V_{CC}\,(Vdc)}{I_7\,(A)} \geq \frac{V_{CC}\,(Vdc)}{0.2}$$

FIGURE 19 — FREE-RUNNING FREQUENCY



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APPLICATIONS INFORMATION

Linear Voltage Ramp

In the monostable mode, the resistor can be replaced by a constant current source to provide a linear ramp voltage. The capacitor still charges from 0 to 2/3 V_{CC}. The linear ramp time is given by $t = \frac{2}{3}\frac{V_{CC}}{I}$

where $I = \frac{V_{CC} - V_B - V_{BE}}{R_E}$. If V_B is much larger than V_{BE}, then t can be made independent of V_{CC}.

FIGURE 20 — LINEAR VOLTAGE SWEEP CIRCUIT

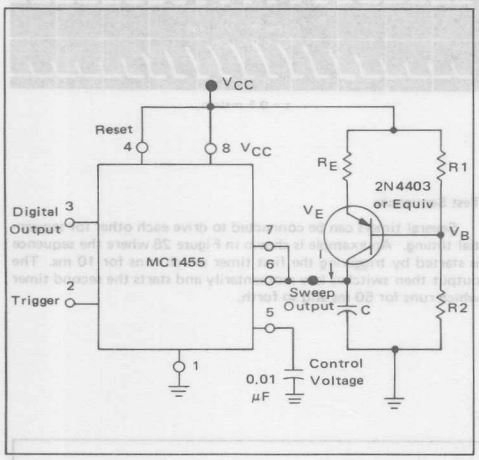
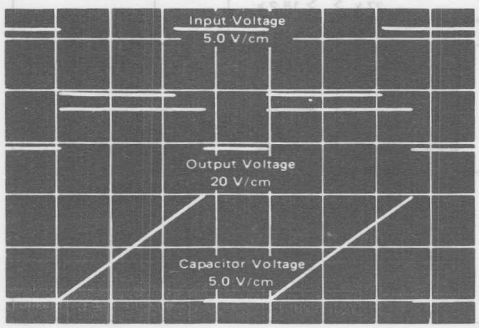


FIGURE 21 — LINEAR VOLTAGE RAMP WAVEFORMS
(R_E = 10 kΩ, R2 = 100 kΩ, R1 = 39 kΩ, C = 0.01 μF, V_{CC} = 15 V)



t = 100 μs/cm

Missing Pulse Detector

The timer can be used to produce an output when an input pulse fails to occur within the delay of the timer. To accomplish this, set the time delay to be slightly longer than the time between successive input pulses. The timing cycle is then continuously reset by the input pulse train until a change in frequency or a missing pulse allows completion of the timing cycle, causing a change in the output level.

FIGURE 22

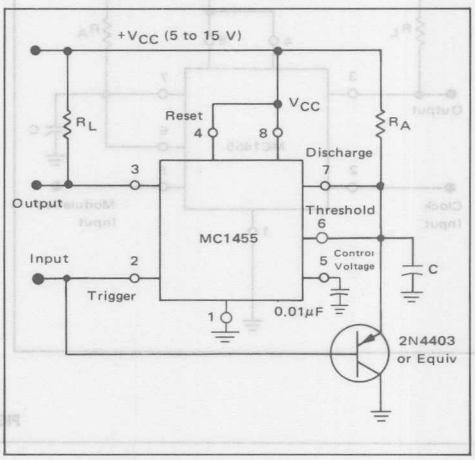
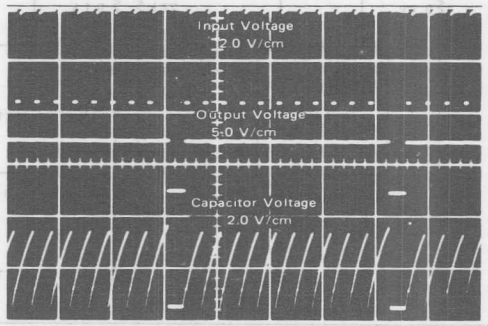


FIGURE 23 — MISSING PULSE DETECTOR WAVEFORMS
(R_A = 2.0 kΩ, R_L = 1.0 kΩ, C = 0.1 μF, V_{CC} = 15 V)



t = 500 μs/cm

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Pulse Width Modulation

If the timer is triggered with a continuous pulse train in the monostable mode of operation, the charge time of the capacitor can be varied by changing the control voltage at pin 5. In this manner, the output pulse width can be modulated by applying a modulating signal that controls the threshold voltage.

FIGURE 24

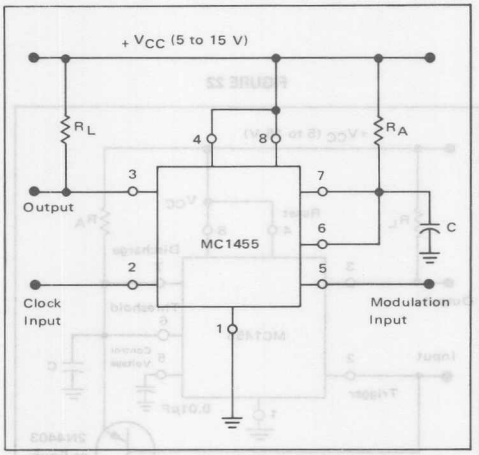
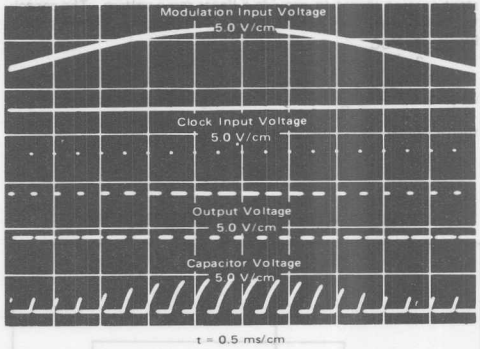


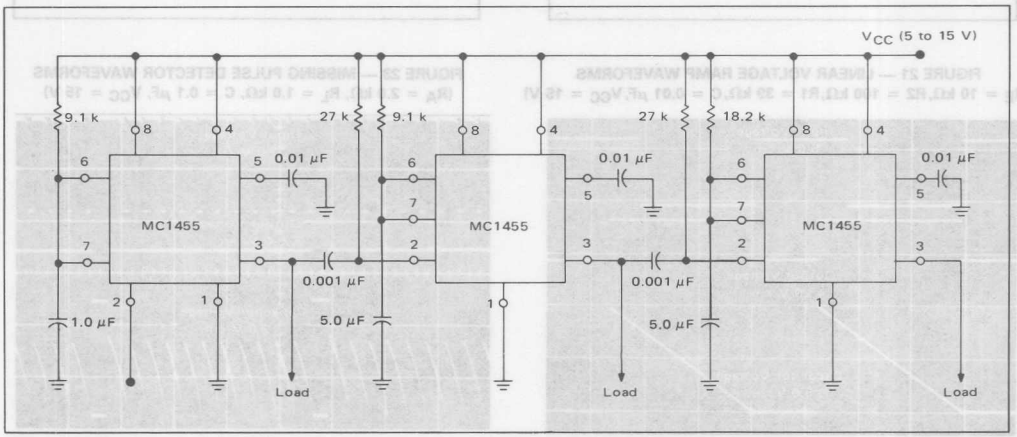
FIGURE 25 — PULSE WIDTH MODULATION WAVEFORMS (R_A = 10 kΩ, C = 0.02 μF, V_{CC} = 15 V)



Test Sequences

Several timers can be connected to drive each other for sequential timing. An example is shown in Figure 26 where the sequence is started by triggering the first timer which runs for 10 ms. The output then switches low momentarily and starts the second timer which runs for 50 ms and so forth.

FIGURE 26



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MOTOROLA

MC1494L
MC1594L

Specifications and Applications Information

LINEAR FOUR-QUADRANT MULTIPLIER INTEGRATED CIRCUIT

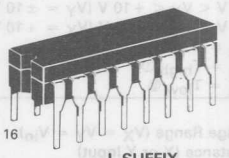
SILICON MONOLITHIC EPITAXIAL PASSIVATED

MONOLITHIC FOUR-QUADRANT MULTIPLIER

. . . designed for use where the output voltage is a linear product of two input voltages. Typical applications include: multiply, divide, square root, mean square, phase detector, frequency doubler, balanced modulator/demodulator, electronic gain control.

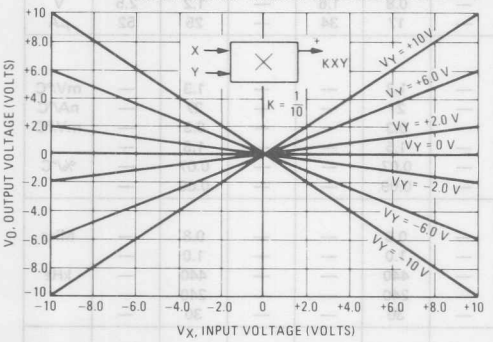
The MC1594/1494 is a variable transconductance multiplier with internal level-shift circuitry and voltage regulator. Scale factor, input offsets and output offset are completely adjustable with the use of four external potentiometers. Two complementary regulated voltages are provided to simplify offset adjustment and improve power-supply rejection.

- Operates With ±15 V Supplies
- Excellent Linearity – Maximum Error (X or Y): ± 0.5% (MC1594)
  ± 1.0% (MC1494)
- Wide Input Voltage Range – ±10 volts
- Adjustable Scale Factor, K (0.1 nominal)
- Single-Ended Output Referenced to Ground
- Simplified Offset Adjust Circuitry
- Frequency Response (3 dB Small-Signal) – 1.0 MHz
- Power Supply Sensitivity – 30 mV/V typical

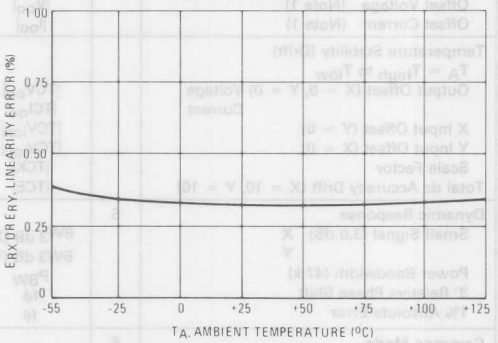


L SUFFIX
CERAMIC PACKAGE
CASE 620-10

FOUR-QUADRANT
MULTIPLIER TRANSFER CHARACTERISTIC



TYPICAL LINEARITY ERROR
versus TEMPERATURE



11

CONTENTS

Subject Sequence	Specification Page No.	Subject Sequence	Specification Page No.
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Electrical Characteristics	2	DC Applications	9
Test Circuits	3	AC Applications	11
Characteristic Curves	4	**Definitions**	13
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Circuit Schematic	5		
DC Operation	6		

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+18 −18	Vdc
Differential Input Signal	V_9-V_6 $V_{10}-V_{13}$	$\pm\lvert 6+I_1R_Y\rvert<30$ $\pm\lvert 6+I_1R_X\rvert<30$	Vdc
Common-Mode Input Voltage $V_{CMY} = V_9 = V_6$ $V_{CMX} = V_{10} = V_{13}$	 V_{CMY} V_{CMX}	 ±11.5 ±11.5	Vdc
Power Dissipation (Package Limitation) T_A = +25°C Derate above T_A = +25°C	 P_D $1/\theta_{JA}$	 750 5.0	 mW mW/°C
Operating Temperature Range MC1594 MC1494	T_A	−55 to +125 0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V^+ = +15 V, V^- = −15 V, T_A = +25°C, R1 = 16 kΩ, R_X = 30 kΩ, R_Y = 62 kΩ, R_L = 47 kΩ, unless otherwise noted)

Characteristic	Fig.	Symbol	MC1594 Min	MC1594 Typ	MC1594 Max	MC1494 Min	MC1494 Typ	MC1494 Max	Unit
Linearity Output error in Percent of full scale −10 V < V_X < +10 V (V_Y = ±10 V) −10 V < V_Y < +10 V (V_X = +10 V) T_A = +25°C $T_A = T_{high}$ ① $T_A = T_{low}$ ②	1	E_{RX} or E_{RY}	 — — —	 ±0.3 — —	 ±0.5 ±0.8 ±0.8	 — — —	 ±0.5 — —	 ±1.0 ±1.3 ±1.3	%
Input Voltage Range ($V_X = V_Y = V_{in}$) Resistance (X or Y Input) Offset Voltage (X Input) (Note 1) (Y Input) (Note 1) Bias Current (X or Y Input) Offset Current (X or Y Input)	2,3,4	 V_{in} R_{in} $\lvert V_{iox}\rvert$ $\lvert V_{ioy}\rvert$ I_b $\lvert I_{io}\rvert$	 ±10 — — — — —	 — 300 0.1 0.4 0.5 28	 — — 1.6 1.6 1.5 150	 ±10 — — — — —	 — 300 0.2 0.8 1.0 50	 — — 2.5 2.5 2.5 400	 V_{pk} MΩ V μA nA
Output Voltage Swing Capability Impedance Offset Voltage (Note 1) Offset Current (Note 1)	3,4	 V_o R_o $\lvert V_{oo}\rvert$ $\lvert I_{oo}\rvert$	 ±10 — — —	 — 850 0.8 17	 — — 1.6 34	 ±10 — — —	 — 850 1.2 25	 — — 2.5 52	 V_{pk} kΩ V μA
Temperature Stability (Drift) $T_A = T_{high}$ to T_{low} Output Offset (X = 0, Y = 0) Voltage Current X Input Offset (Y = 0) Y Input Offset (X = 0) Scale Factor Total dc Accuracy Drift (X = 10, Y = 10)		 $\lvert TCV_{oo}\rvert$ $\lvert TCI_{oo}\rvert$ $\lvert TCV_{iox}\rvert$ $\lvert TCV_{ioy}\rvert$ $\lvert TCK\rvert$ $\lvert TCE\rvert$	 — — — — — —	 1.3 27 0.3 1.5 0.07 0.09	 — — — — — —	 — — — — — —	 1.3 27 0.3 1.5 0.07 0.09	 — — — — — —	 mV/°C nA/°C mV/°C %/°C
Dynamic Response Small Signal (3.0 dB) X Y Power Bandwidth (47 k) 3° Relative Phase Shift 1% Absolute Error	5	 $BW_{3\ dB}$ (X) BW3 dB (Y) P_{BW} $f\phi$ $f\theta$	 — — — — —	 0.8 1.0 440 240 30	 — — — — —	 — — — — —	 0.8 1.0 440 240 30	 — — — — —	 MHz kHz
Common Mode Input Swing (X or Y) Gain (X or Y)	6	 CMV A_{CM}	 ±10.5 —	 — −65	 — —	 ±10.5 —	 — −65	 — —	 V_{pk} dB
Power Supply Current Quiescent Power Dissipation Sensitivity	7	 I_d+ I_d- P_d S^+ $S-$	 — — — — —	 6.0 6.5 185 13 30	 9.0 9.0 260 50 100	 — — — — —	 6.0 6.5 185 13 30	 12 12 350 100 200	 mAdc mW mV/V
Regulated Offset Adjust Voltages Positive Negative Temperature Coefficient (V_R+ or V_R-) Power Supply Sensitivity (V_R+ or V_R-)	7	 V_R+ V_R- TCV_R S_R+, S_R-	 +3.5 −3.5 — —	 +4.3 −4.3 0.03 0.6	 +5.0 −5.0 — —	 +3.5 −3.5 — —	 +4.3 −4.3 0.03 0.6	 +5.0 −5.0 — —	 Vdc mV/°C mV/V

Note 1: Offsets can be adjusted to zero with external potentiomers. ① T_{high} = +125°C for MC1594, +70°C for MC1494 ② T_{low} = −55°C for MC1594, 0°C for MC1494

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TEST CIRCUITS

FIGURE 1 – LINEARITY

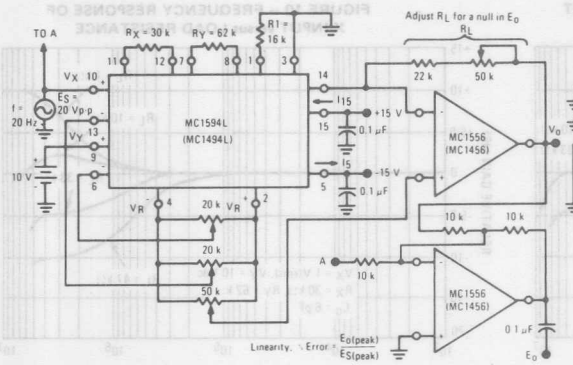


FIGURE 2 – INPUT RESISTANCE

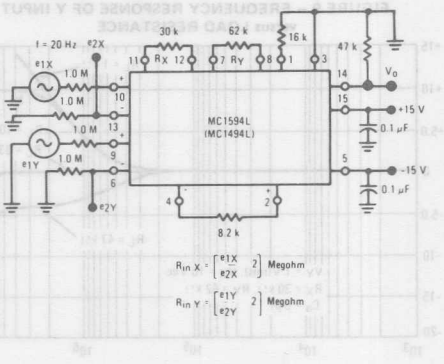


FIGURE 3 – OFFSET VOLTAGES, GAIN

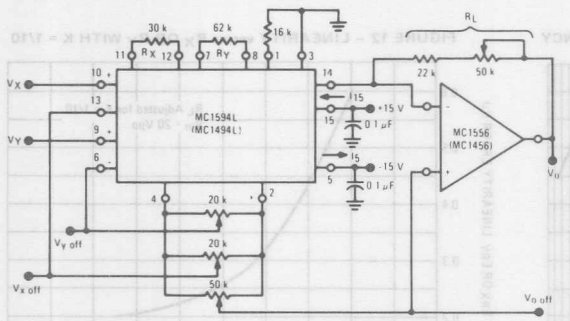


FIGURE 4 – INPUT BIAS CURRENT/INPUT OFFSET CURRENT, OUTPUT RESISTANCE

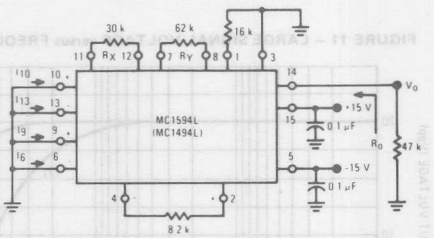


FIGURE 5 – FREQUENCY RESPONSE

FIGURE 6 – COMMON MODE

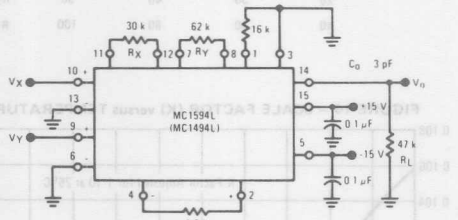


FIGURE 7 – POWER-SUPPLY SENSITIVITY

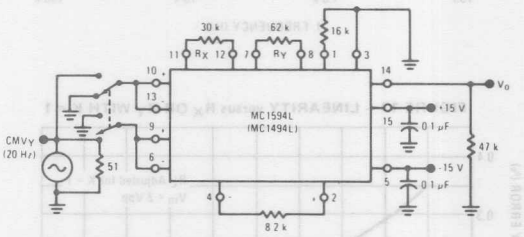
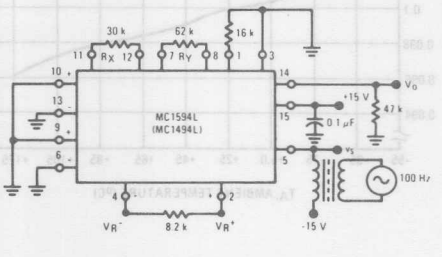
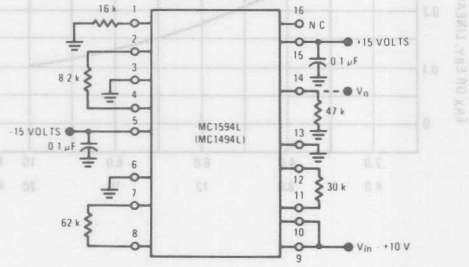


FIGURE 8 – BURN-IN





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FIGURE 9 – FREQUENCY RESPONSE OF Y INPUT versus LOAD RESISTANCE

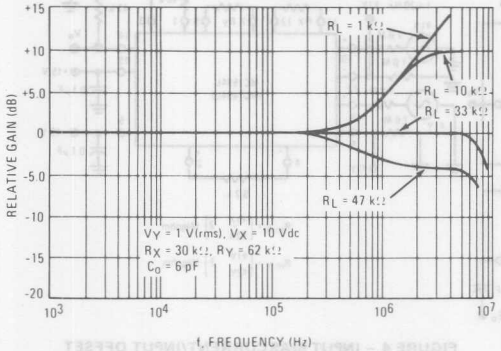


FIGURE 10 – FREQUENCY RESPONSE OF X INPUT versus LOAD RESISTANCE

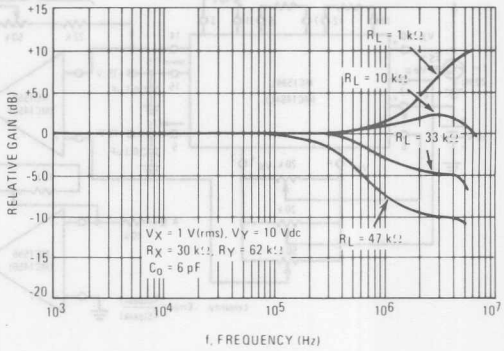


FIGURE 11 – LARGE SIGNAL VOLTAGE versus FREQUENCY

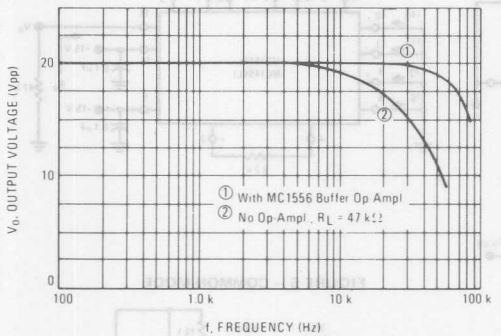


FIGURE 12 – LINEARITY versus R_X OR R_Y WITH K = 1/10

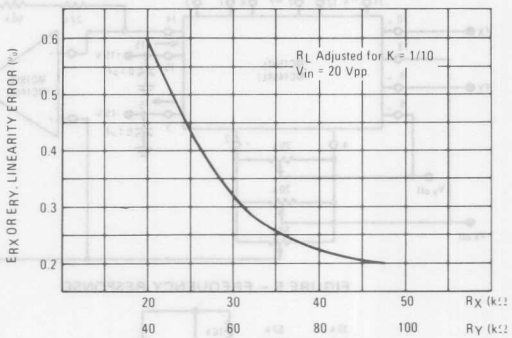


FIGURE 13 – LINEARITY versus R_X OR R_Y WITH K = 1

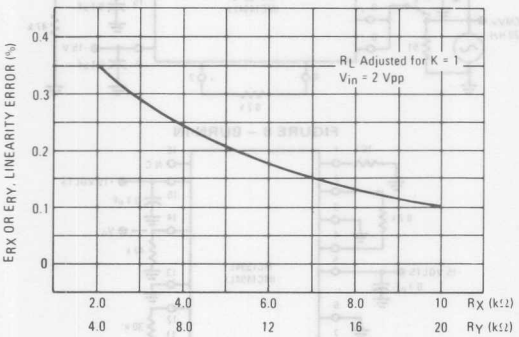
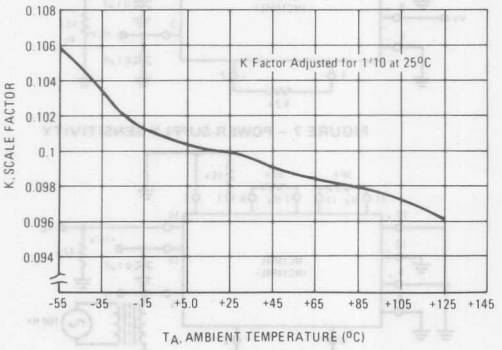


FIGURE 14 – SCALE FACTOR (K) versus TEMPERATURE



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GENERAL INFORMATION

1. CIRCUIT DESCRIPTION

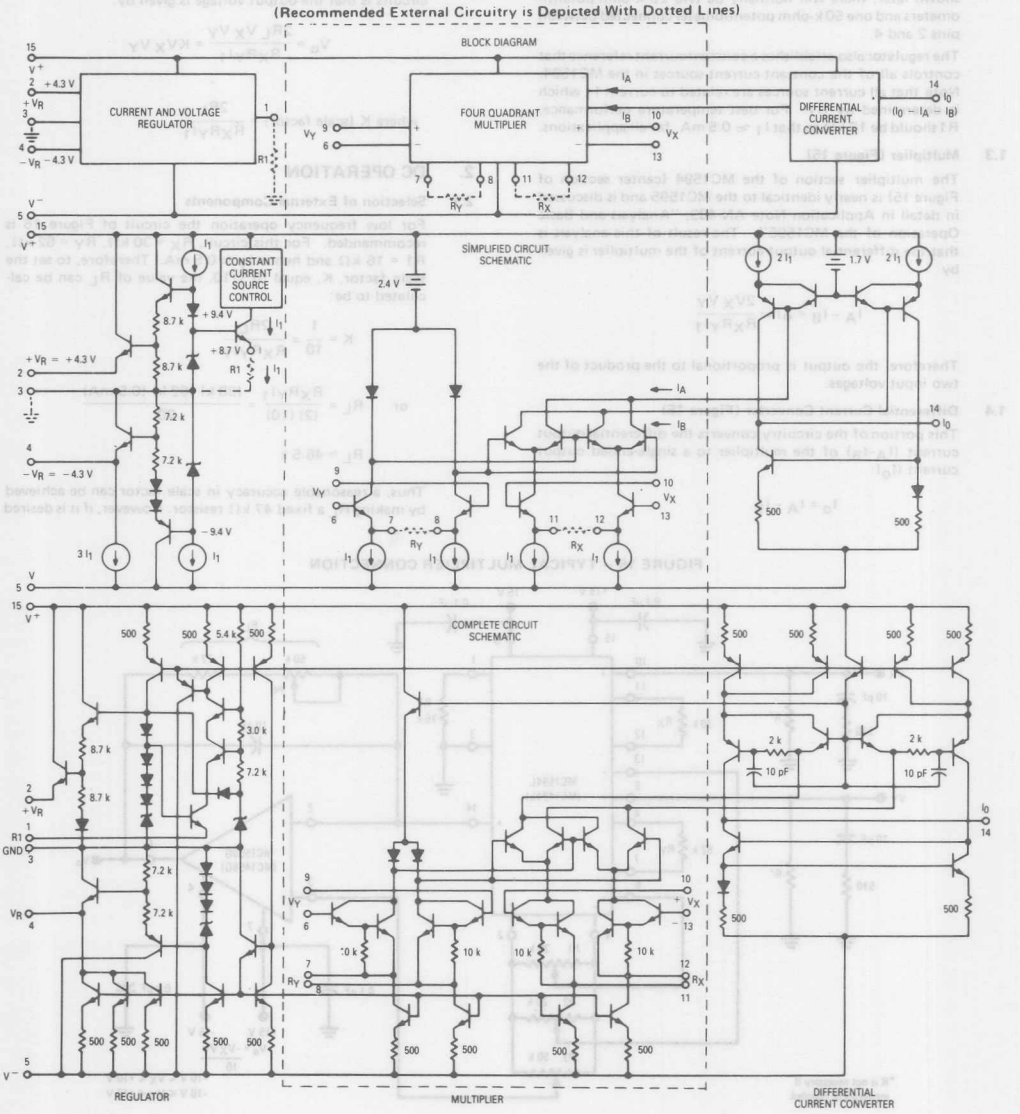
1.1 Introduction

The MC1594 is a monolithic, four-quadrant multiplier that operates on the principle of variable transconductance. It features a single-ended current output referenced to ground and provides two complementary regulated voltages for use with the offset adjust circuits to virtually eliminate sensitivity of the offset voltage nulls to changes in supply voltage.

As shown in Figure 15, the MC1594 consists of a multiplier proper and associated peripheral circuitry to provide these features.

FIGURE 15

(Recommended External Circuitry is Depicted With Dotted Lines)



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1.2 Regulator (Figure 15)

The regulator biases the entire MC1594 circuit making it essentially independent of supply variation. It also provides two convenient regulated supply voltages which can be used in the offset adjust circuitry. The regulated output voltage at pin 2 is approximately +4.3 V while the regulated voltage at pin 4 is approximately -4.3 V. For optimum temperature stability of these regulated voltages, it is recommended that $|I_2| = |I_4| = 1.0$ mA (equivalent load of 8.6 kΩ). As will be shown later, there will normally be two 20 k-ohm potentiometers and one 50 k-ohm potentiometer connected between pins 2 and 4.

The regulator also establishes a constant current reference that controls all of the constant current sources in the MC1594. Note that all current sources are related to current I_1 which is determined by R1. For best temperature performance, R1 should be 16 kΩ so that $I_1 \approx 0.5$ mA for all applications.

1.3 Multiplier (Figure 15)

The multiplier section of the MC1594 (center section of Figure 15) is nearly identical to the MC1595 and is discussed in detail in Application Note AN-489, "Analysis and Basic Operation of the MC1595". The result of this analysis is that the differential output current of the multiplier is given by:

$$I_A - I_B = \Delta I \approx \frac{2V_X V_Y}{R_X R_Y I_1}$$

Therefore, the output is proportional to the product of the two input voltages.

1.4 Differential Current Converter (Figure 15)

This portion of the circuitry converts the differential output current (I_A-I_B) of the multiplier to a single-ended output current (I_o):

$$I_o = I_A - I_B$$

or

$$I_o = \frac{2V_X V_Y}{R_X R_Y I_1}$$

The output current can be easily converted to an output voltage by placing a load resistor R_L from the output (pin 14) to ground (Figure 17) or by using an op-ampl. as a current-to-voltage converter (Figure 16). The result in both circuits is that the output voltage is given by:

$$V_o = \frac{2R_L V_X V_Y}{R_X R_Y I_1} = KV_X V_Y$$

where K (scale factor) = $\frac{2R_L}{R_X R_Y I_1}$

2. DC OPERATION

2.1 Selection of External Components

For low frequency operation the circuit of Figure 16 is recommended. For this circuit, R_X = 30 kΩ, R_Y = 62 kΩ, R1 = 16 kΩ and hence $I_1 \approx 0.5$ mA. Therefore, to set the scale factor, K, equal to 1/10, the value of R_L can be calculated to be:

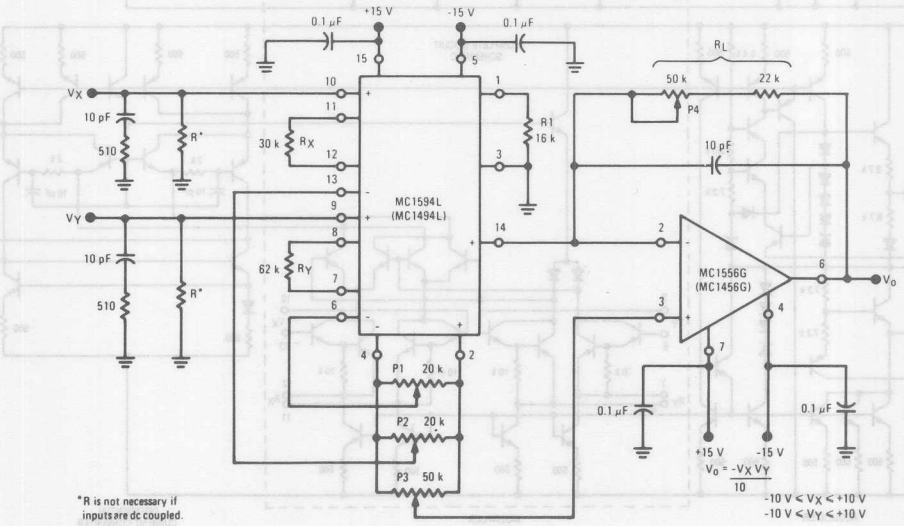
$$K = \frac{1}{10} = \frac{2R_L}{R_X R_Y I_1}$$

or $$R_L = \frac{R_X R_Y I_1}{(2)(10)} = \frac{(30\text{ k})(62\text{ k})(0.5\text{ mA})}{20}$$

$$R_L = 46.5\text{ k}$$

Thus, a reasonable accuracy in scale factor can be achieved by making R_L a fixed 47 kΩ resistor. However, if it is desired

FIGURE 16 – TYPICAL MULTIPLIER CONNECTION



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that the scale factor be exact, R_L can be comprised of a fixed resistor and a potentiometer as shown in Figure 16. It should be pointed out that there is nothing magic about setting the scale factor to 1/10. This is merely a convenient factor to use if the V_X and V_Y input voltages are expected to be large, say ±10 V. Obviously with $V_X = V_Y = 10$ V and a scale factor of unity, the device could not hope to provide a 100 V output, so the scale factor is set to 1/10 and provides an output scaled down by a factor of ten. For many applications it may be desirable to set K = 1/2 or K = 1 or even K = 100. This can be accomplished by adjusting R_X, R_Y and R_L appropriately.

The selection of R_L is arbitrary and can be chosen after resistors R_X and R_Y are found. Note in Figure 16 that R_Y is 62 kΩ while R_X is 30 kΩ. The reason for this is that the "Y" side of the multiplier exhibits a second order non-linearity whereas the "X" side exhibits a simple non-linearity. By making the R_Y resistor approximately twice the value of the R_X resistor, the linearity on both the "X" and "Y" sides are made equal. The selection of the R_X and R_Y resistor values is dependent upon the expected amplitude of V_X and V_Y inputs. To maintain a specified linearity, resistors R_X and R_Y should be selected according to the following equations:

$$R_X \geq 3\ V_X\ (\text{max}) \text{ in k}\Omega \text{ when } V_X \text{ is in volts}$$

$$R_Y \geq 6\ V_Y\ (\text{max}) \text{ in k}\Omega \text{ when } V_Y \text{ is in volts}$$

For example, if the maximum input on the "X" side is ±1 volt, resistor R_X can be selected to be 3 kΩ. If the maximum input on the "Y" side is also ±1 volt, then resistor R_Y can be selected to be 6 kΩ (6.2 kΩ nominal value). If a scale factor of K = 10 is desired, the load resistor is found to be 47 kΩ. In this example, the multiplier provides a gain of 20 dB.

2.2 Operational Amplifier Selection

The operational amplifier connection in Figure 16 is a simple but extremely accurate current-to-voltage converter. The output current of the multiplier flows through the feedback resistor R_L to provide a low impedance output voltage from the op-ampl. Since the offset current and bias currents of the op-ampl. will cause errors in the output voltage, particularly with temperature, one with very low bias and offset currents is recommended. The MC1556/MC1456 or MC1741/MC1741C are excellent choices for this application.

Since the MC1594 is capable of operation at much higher frequencies than the op-ampl., the frequency characteristics of the circuit in Figure 16 will be primarily dependent upon the op-ampl.

2.3 Stability

The current-to-voltage converter mode is a most demanding application for an operational amplifier. Loop gain is at its maximum and the feedback resistor in conjunction with stray or input capacitance at the multiplier output adds additional phase shift. It may therefore be necessary to add (particularly in the case of internally compensated op-ampls.) a small feedback capacitor to reduce loop gain at the higher frequencies. A value of 10 pF in parallel with R_L should be adequate to insure stability over production and temperature variations, etc.

An externally compensated op-ampl. might be employed using slightly heavier compensation than that recommended for unity-gain operation.

2.4 Offset Adjustment

The non-inverting input of the op-ampl. provides a convenient point to adjust the output offset voltage. By connecting this point to the wiper arm of a potentiometer (P3), the output offset voltage can be adjusted to zero (see offset and scale factor adjustment procedure).

The input offset adjustment potentiometers, P1 and P2 will be necessary for most applications where it is desirable to take advantage of the multiplier's excellent linearity characteristics. Depending upon the particular application, some of the potentiometers can be omitted (see Figures 17, 19, 22, 24 and 25).

2.5 Offset and Scale Factor Adjustment Procedure

The adjustment procedure for the circuit of Figure 16 is:

A. X Input Offset
   (a) connect oscillator (1 kHz, 5 Vpp sinewave) to the "Y" input (pin 9)
   (b) connect "X" input (pin 10) to ground
   (c) adjust X-offset potentiometer, P2 for an ac null at the output

B. Y Input Offset
   (a) connect oscillator (1 kHz, 5 Vpp sinewave) to the "X" input (pin 10)
   (b) connect "Y" input (pin 9) to ground
   (c) adjust Y-offset potentiometer, P1 for an ac null at the output

C. Output Offset
   (a) connect both "X" and "Y" inputs to ground
   (b) adjust output offset potentiometer, P3, until the output voltage V_O, is zero volts dc

D. Scale Factor
   (a) apply +10 Vdc to both the "X" and "Y" inputs
   (b) adjust P4 to achieve -10.00 V at the output
   (c) apply -10 Vdc to both "X" and "Y" inputs and check for V_O = -10.00 V

E. Repeat steps A through D as necessary.

The ability to accurately adjust the MC1594 is dependent on the offset adjust potentiometers. Potentiometers should be of the "infinite" resolution type rather than wirewound. Fine adjustments in balanced-modulator applications may require two potentiometers to provide "coarse" and "fine" adjustment. Potentiometers should have low temperature coefficients and be free from backlash.

2.6 Temperature Stability

While the MC1594 provides excellent performance in itself, overall performance depends to a large degree on the quality of the external components. Previous discussion shows the direct dependence on R_X, R_Y, and R_L and indirect dependence on R1 (through I_1). Any circuit subjected to temperature variations should be evaluated with these effects in mind.

2.7 Bias Currents

The MC1594 multiplier, like most linear IC's, requires a dc bias current into its input terminals. The device cannot be capacitively coupled at the input without regard for this bias current. If inputs V_X and V_Y are able to supply the small bias current ($\approx 0.5\ \mu A$) resistors, R (Figure 16) can be omitted. If the MC1594 is used in an ac mode of operation and capacitive coupling is used the value of resistor R can be any reasonable value up to 100 kΩ. For minimum noise and optimum temperature performance, the value of resistor R should be as low as practical.

2.8 Parasitic Oscillation

When long leads are used on the inputs, oscillation may occur. In this event, an RC parasitic suppression network similar to the ones shown in Figure 16 should be connected directly to each input using short leads. The purpose of the network

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the oscillation.

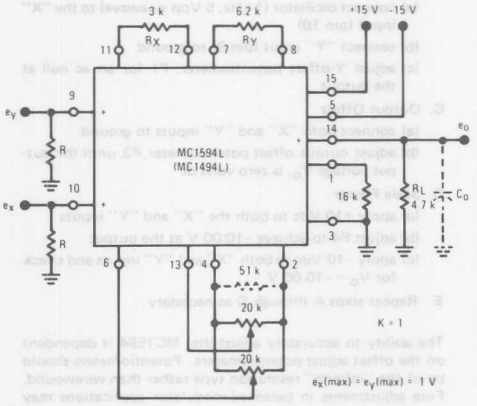
Inability to adjust the circuit to within the specified accuracy may be an indication of oscillation.

3. AC OPERATION

3.1 General

For ac operation, such as balanced modulation, frequency doubler, AGC, etc., the op-ampl. will usually be omitted as well as the output offset adjust potentiometer. The output offset adjust potentiometer is omitted since the output will normally be ac-coupled and the dc voltage at the output is of no concern providing it is close enough to zero volts that it will not cause clipping in the output waveform. Figure 17

FIGURE 17 – WIDEBAND MULTIPLIER



shows a typical ac multiplier circuit with a scale factor $K \approx 1$. Again, resistor R_X and R_Y are chosen as outlined in the previous section, with R_L chosen to provide the required scale factor.

The offset voltage then existing at the output will be equal to the offset current times the load resistance. The output offset current of the MC1594 is typically 17 μA and 35 μA maximum. Thus, the maximum output offset would be about 160 mV.

3.2 Bandwidth

The bandwidth of the MC1594 is primarily determined by two factors. First, the dominant pole will be determined by the load resistor and the stray capacitance at the output terminal. For the circuit shown in Figure 17, assuming a total output capacitance (C_O) of 10 pF, the 3 dB bandwidth would be approximately 3.4 MHz. If the load resistor were 47 kΩ, the bandwidth would be approximately 340 kHz.

Secondly, a "zero" is present in the frequency response characteristic for both the "X" and "Y" inputs which causes the output signal to rise in amplitude at a 6 dB/octave slope at frequencies beyond the breakpoint of the "zero". The "zero" is caused by the parasitic and substrate capacitance which is related to resistors R_X and R_Y and the transistors associated with them. The effect of these transmission increase in gain is due to the bypassing of R_X and R_Y at high frequencies. Since the R_Y resistor is approximately twice the value of the R_X resistor, the zero associated with the "Y" input will occur at approximately one octave below the zero associated with the "X" input. For R_X = 30 kΩ and R_Y = 62 kΩ, the zeros occur at 1.5 MHz for the "X" input and 700 kHz for the "Y" input. These two measured breakpoints correspond to a shunt capacitance of about 3.5 pF. Thus, for the circuit of Figure 17, the "X" input zero and "Y" input zero will be at approximately 15 MHz and 7 MHz respectively.

It should be noted that the MC1594 multiplies in the time domain, hence, its frequency response is found by means of complex convolution in the frequency (Laplace) domain. This means that if the "X" input does not involve a frequency, it is not necessary to consider the "X" side frequency response in the output product. Likewise, for the "Y" side. Thus, for applications such as a wideband linear AGC amplifier which has a dc voltage as one input, the multiplier frequency response has one zero and one pole. For applications which involve an ac voltage on both the "X" and "Y" side, such as a balanced modulator, the product voltage response will have two zeros and one pole, hence, peaking may be present in the output.

From this brief discussion, it is evident that for ac applications; (1) the value of resistors R_X, R_Y and R_L should be kept as small as possible to achieve maximum frequency response, and (2) it is possible to select a load resistor R_L such that the dominant pole (R_L, C_O) cancels the input zero (R_X, 3.5 pF or R_Y, 3.5 pF) to give a flat amplitude characteristic with frequency. This is shown in Figures 9 and 10. Examination of the frequency characteristics of the "X" and "Y" inputs will demonstrate that for wideband amplifier applications, the best tradeoff with frequency response and gain is achieved by using the "Y" input for the ac signal.

For ac applications requiring bandwidths greater than those specified for the MC1594, two other devices are recommended. For modulator-demodulator applications, the MC1596 may be used up to 100 MHz. For wideband multiplier applications, the MC1595 (using small collector loads and ac coupling) can be used.

3.3 Slew-Rate

The MC1594 multiplier is not slew-rate limited in the ordinary sense that an op-ampl. is. Since all the signals in the multiplier are currents and not voltages, there is no charging and discharging of stray capacitors and thus no limitations beyond the normal device limitations. However, it should be noted that the quiescent current in the output transistors is 0.5 mA and thus the maximum rate of change of the output voltage is limited by the output load capacitance by the simple equation:

$$\text{Slew-Rate} \quad \frac{\Delta V_o}{\Delta T} = \frac{I_o}{C}$$

Thus, if C_O is 10 pF, the maximum slew-rate would be:

$$\frac{\Delta V_o}{\Delta T} = \frac{0.5 \times 10^{-3}}{10 \times 10^{-12}} = 50 \text{ V}/\mu\text{s}$$

This can be improved if necessary by addition of an emitter-follower or other type of buffer.

3.4 Phase-Vector Error

All multipliers are subject to an error which is known as the phase-vector error. This error is a phase error only and does not contribute an amplitude error per se. The phase-vector

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error is best explained by an example. If the "X" input is described in vector notation as

$$X = A \angle 0^o$$

and the "Y" input is described as

$$Y = B \angle 0^o$$

then the output product would be expected to be

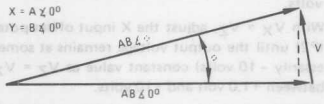
$$V_o = AB \angle 0^o \text{ (see Figure 18)}$$

However, due to a relative phase shift between the "X" and "Y" channels, the output product will be given by

$$V_o = AB \angle \phi$$

Notice that the magnitude is correct but the phase angle of the product is in error. The vector, V, associated with this error is the "phase-vector error". The startling fact about the phase-vector error is that it occurs and accumulates much more rapidly than the amplitude error associated with frequency response. In fact, a relative phase shift of only 0.57^o will result in a 1% phase-vector error. For most applications, this error is meaningless. If phase of the output product is not important, then neither is the phase-vector error. If phase is important, such as in the case of double sideband modulation or demodulation, then a 1% phase-vector error will represent a 1% amplitude error at the phase angle of interest.

FIGURE 18 – PHASE-VECTOR ERROR



3.5 Circuit Layout

If wideband operation is desired, careful circuit layout must be observed. Stray capacitance across R_X and R_Y should be avoided to minimize peaking (caused by a zero created by the parallel RC circuit).

4. DC APPLICATIONS

4.1 Squaring Circuit

If the two inputs are connected together, the resultant function is squaring:

$$V_o = KV^2$$

where K is the scale factor (see Figure 19).

However, a more careful look at the multiplier's defining equation will provide some useful information. The output voltage, without initial offset adjustments is given by:

$$V_o = K(V_x + V_{iox} - V_{x\,off})(V_y + V_{ioy} - V_{y\,off}) + V_{oo}$$

(See "Definitions" for an explanation of terms).

With $V_x = V_y = V$ (squaring) and defining

$$\epsilon_x = V_{iox} - V_{x\,off}$$

$$\epsilon_y = V_{ioy} - V_{y\,off}$$

The output voltage equation becomes

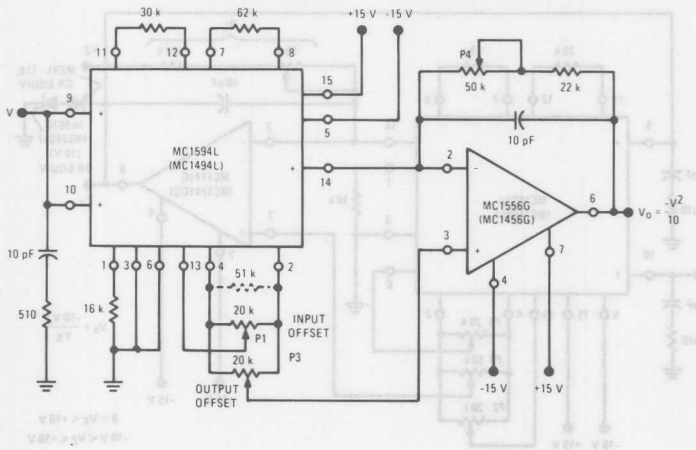
$$V_o = K V_x^2 + KV_x(\epsilon_x + \epsilon_y) + K\epsilon_x\epsilon_y + V_{oo}$$

This shows that all error terms can be eliminated with only three adjustment potentiometers, eliminating one of the input offset adjustments. For instance, if the "X" input offset adjustment is eliminated, ϵ_x is determined by the internal offset, V_{iox}, but ϵ_y is adjustable to the extent that the $(\epsilon_x + \epsilon_y)$ term can be zeroed. Then the output offset adjustment is used to adjust the V_{oo} term and thus zero the remaining error terms. An ac procedure for nulling with three adjustments is:

A. AC Procedure:

1. Connect oscillator (1 kHz, 15 Vpp) to input
2. Monitor output at 2 kHz with tuned voltmeter and adjust P4 for desired gain (Be sure to peak response of voltmeter)
3. Tune voltmeter to 1 kHz and adjust P1 for a minimum output voltage
4. Ground input and adjust P3 (output offset) for zero volts dc out
5. Repeat steps 1 through 4 as necessary.

FIGURE 19 – MC1594 SQUARING CIRCUIT



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B. DC Procedure:

1. Set $V_X = V_Y = 0$ V and adjust P3 (output offset potentiometer) such that $V_o = 0.0$ Vdc
2. Set $V_X = V_Y = 1.0$ V and adjust P1 (Y input offset potentiometer) such that the output voltage is -0.100 volts
3. Set $V_X = V_Y = 10$ Vdc and adjust P4 (load resistor) such that the output voltage is -10.00 volts
4. Set $V_X = V_Y = -10$ Vdc and check that $V_O = -10$V Repeat steps 1 through 4 as necessary.

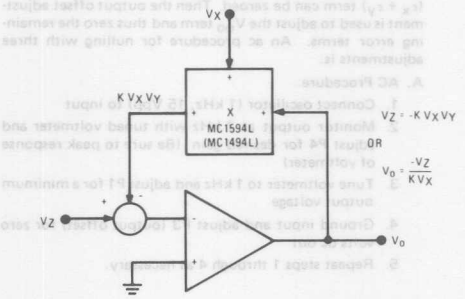
4.2 Divide

Divide circuits warrant a special discussion as a result of their special problems. Classic feedback theory teaches that if a multiplier is used as a feedback element in an operational amplifier circuit, the divide function results. Figure 20 illustrates the theoretical simplicity of such an approach and a practical realization is shown in Figure 21.

The characteristic "failure" mode of the divide circuit is latch-up. One way it can occur is if V_X is allowed to go negative or, in some cases, if V_X approaches zero.

Figure 20 illustrates why this is so. For $V_X > 0$ the transfer function through the multiplier is non-inverting. Its output is fed to the inverting input of the op-ampl. Thus, operation is in the negative feedback mode and the circuit is dc stable.

FIGURE 20 – BASIC DIVIDE CIRCUIT USING MULTIPLIER



Should V_X change polarity, the transfer function through the multiplier becomes inverting, the amplifier has positive feedback and latch-up results. The problem resulting from V_X being near zero is a result of the transfer through the multiplier being near zero. The op-ampl. is then operating with a very high closed loop gain and error voltages can thus become effective in causing latch-up.

The other mode of latch-up results from the output voltage of the op-ampl. exceeding the rated common-mode input voltage of the multiplier. The input stage of the multiplier becomes saturated, phase reversal results, and the circuit is latched up. The circuit of Figure 21 protects against this happening by clamping the output swing of the op-ampl. to approximately ±10.7 volts. Five-percent tolerance, 10-volt zeners are used to assure adequate output swing but still limit the output voltage of the op-ampl. from exceeding the common-mode input range of the MC1594.

Setting up the divide circuit for reasonably accurate operation is somewhat different from the procedure for the multiplier itself. One approach, however, is to break the feedback loop, null out the multiplier circuit, and then close the loop.

A simpler approach, since it does not involve breaking the loop (thus making it more practical on a production basis), is:

1. Set $V_Z = 0$ volts and adjust the output offset potentiometer (P3) until the output voltage (V_o) remains at some (not necessarily zero) constant value as V_X is varied between +1.0 volt and +10 volts.
2. Maintain V_Z at 0 volts, set V_X at +10 volts and adjust the Y input offset potentiometer (P1) until $V_o = 0$ volts.
3. With $V_X = V_Z$, adjust the X input offset potentiometer (P2) until the output voltage remains at some (not necessarily -10 volts) constant value as $V_Z = V_X$ is varied between +1.0 volt and +10 volts.
4. Maintain $V_X = V_Z$ and adjust the scale factor potentiometer (R_L) until the average value of V_o is -10 volts as $V_Z = V_X$ is varied between +1.0 volt and +10 volts.
5. Repeat steps 1 through 4 as necessary to achieve optimum performance.

Users of the divide circuit should be aware that the accuracy to be expected decreases in direct proportion to the denomi-

FIGURE 21 – PRACTICAL DIVIDE CIRCUIT

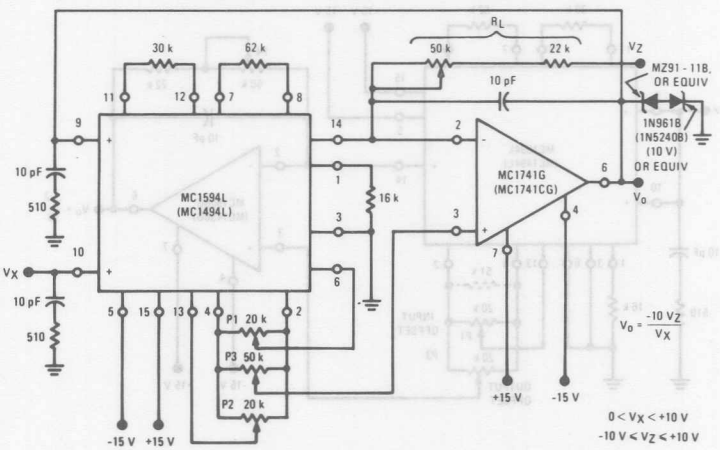
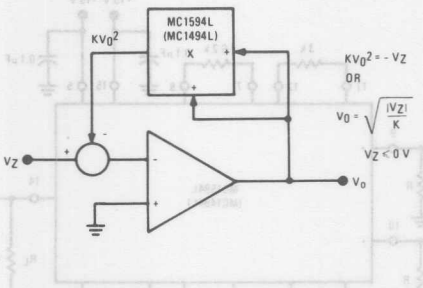


FIGURE 22 – BASIC SQUARE ROOT CIRCUIT



nator voltage. As a result, if V_X is set to 10 volts and 0.5% accuracy is available, then 5% accuracy can be expected when V_X is only 1 volt.

In accordance with an earlier statement, V_X may have only one polarity, positive, while V_Z may be either polarity.

4.3 Square Root

A special case of the divide circuit in which the two inputs to the multiplier are connected together results in the square root function as indicated in Figure 22. This circuit too may suffer from latch-up problems similar to those of the divide circuit. Note that only one polarity of input is allowed and diode clamping (see Figure 23) protects against accidental latch-up.

This circuit too, may be adjusted in the closed-loop mode:

1. Set V_Z = -0.01 Vdc and adjust P3 (output offset) for V_O = 0.316 Vdc.
2. Set V_Z to -0.9 Vdc and adjust P2 ("X" adjust) for V_O = +3 Vdc.
3. Set V_Z to -10 Vdc and adjust P4 (gain adjust) for V_O = +10 Vdc.

Steps 1 through 3 may be repeated as necessary to achieve desired accuracy.

Note: Operation near zero volts input may prove very inaccurate, hence, it may not be possible to adjust V_O to 0 but rather only to within 100 to 400 mV of zero.

5. AC APPLICATIONS

5.1 Wideband Amplifier With Linear AGC

If one input to the MC1594 is a dc voltage and a signal voltage is applied to the other input, the amplitude of the output signal can be controlled in a linear fashion by varying the dc voltage. Hence, the multiplier can function as a dc coupled, wideband amplifier with linear AGC control.

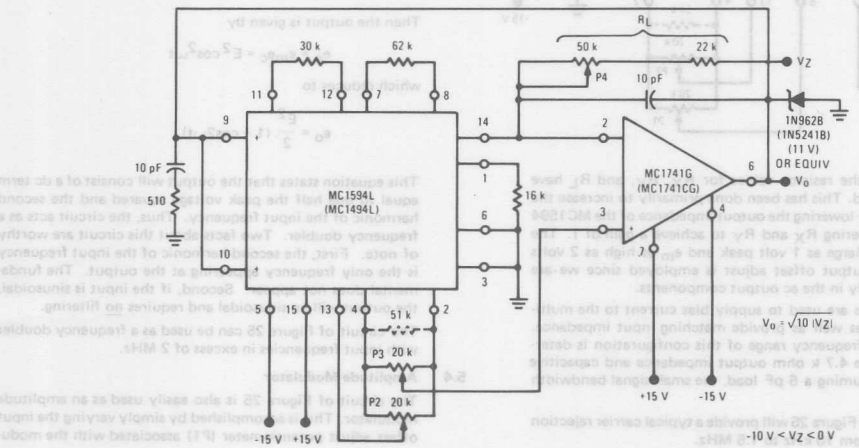
In addition to the advantage of Linear AGC control, the multiplier has three other distinct advantages over most other types of AGC systems. First, the AGC dynamic range is theoretically infinite. This stems from the basic fact that with zero volts dc applied to the AGC, the output will be zero regardless of the input. In practice, the dynamic range is limited by the ability to adjust the input offset adjust potentiometers. By using cermet multi-turn potentiometers, a dynamic range of 80 dB can be obtained. The second advantage of the multiplier is that variation of the AGC voltage has no effect on the signal handling capability of the signal port, nor does it alter the input impedance of the signal port. This feature is particularly important in AGC systems which are phase sensitive. A third advantage of the multiplier is that the output-voltage-swing capability and output impedance are unchanged with variations in AGC voltage.

The circuit of Figure 24 demonstrates the linear AGC amplifier. The amplifier can handle 1 V(rms) and exhibits a gain of approximately 20 dB. It is AGC'd through a 60 dB dynamic range with the application of an AGC voltage from 0 Vdc to 1 Vdc. The bandwidth of the amplifier is determined by the load resistor and output stray capacitance. For this reason, an emitter-follower buffer has been added to extend the bandwidth in excess of 1 MHz.

5.2 Balanced Modulator

When two-time variant signals are used as inputs, the result-

FIGURE 23 – SQUARE ROOT CIRCUIT



In terms of sinusoidal inputs, this can be seen in the following equation:

$$V_o = K(e_1 \cos\omega_m t)(e_2 \cos\omega_c t)$$

where ω_m is the modulation frequency and ω_c is the carrier frequency. This equation can be expanded to show the suppressed carrier or balanced modulation:

$$V_o = \frac{Ke_1e_2}{2}[\cos(\omega_c + \omega_m)t + \cos(\omega_c - \omega_m)t]$$

Unlike many modulation schemes, which are non-linear in nature, the modulation which takes place when using the MC1594 is linear. This means that for two sinusoidal inputs, the output will contain only two frequencies, the sum and difference, as seen in the above equation. There will be no spectrum centered about the second harmonic of the carrier, or any multiple of the carrier. For this reason, the filter requirements of a modulation system are reduced to the minimum. Figure 25 shows the MC1594 configuration to perform this function.

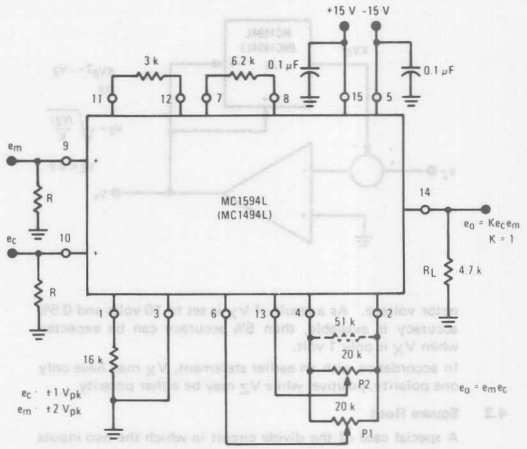
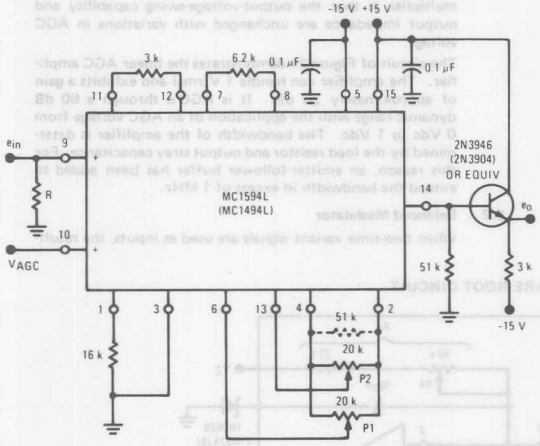


FIGURE 24 – WIDEBAND AMPLIFIER WITH LINEAR AGC



Notice that the resistor values for R_X, R_Y, and R_L have been modified. This has been done primarily to increase the bandwidth by lowering the output impedance of the MC1594 and then lowering R_X and R_Y to achieve a gain of 1. The e_c can be as large as 1 volt peak and e_m as high as 2 volts peak. No output offset adjust is employed since we are interested only in the ac output components.

The input R's are used to supply bias current to the multiplier inputs as well as provide matching input impedance. The output frequency range of this configuration is determined by the 4.7 k ohm output impedance and capacitive loading. Assuming a 6 pF load, the small-signal bandwidth is 5.5 MHz.

The circuit of Figure 25 will provide a typical carrier rejection of ≥70 dB from 10 kHz to 1.5 MHz.

The adjustment procedure for this circuit is quite simple.

(1) Place the carrier signal at pin 10. With no signal applied to pin 9, adjust potentiometer P1 such that an ac null is obtained at the output.

(2) Place a modulation signal at pin 9. With no signal applied to pin 10, adjust potentiometer P2 such that an ac null is obtained at the output.

Again, the ability to make careful adjustment of these offsets will be a function of the type of potentiometers used for P1 and P2. Multiple turn cermet type potentiometers are recommended.

5.3 Frequency Doubler

If for Figure 25 both inputs are identical;

$$e_m = e_c = E\cos\omega t$$

Then the output is given by

$$e_o = e_m e_c = E^2\cos^2\omega t$$

which reduces to

$$e_o = \frac{E^2}{2}(1 + \cos 2\omega t)$$

This equation states that the output will consist of a dc term equal to one half the peak voltage squared and the second harmonic of the input frequency. Thus, the circuit acts as a frequency doubler. Two facts about this circuit are worthy of note. First, the second harmonic of the input frequency is the only frequency appearing at the output. The fundamental does not appear. Second, if the input is sinusoidal, the output will be sinusoidal and requires no filtering.

The circuit of Figure 25 can be used as a frequency doubler with input frequencies in excess of 2 MHz.

5.4 Amplitude Modulator

The circuit of Figure 25 is also easily used as an amplitude modulator. This is accomplished by simply varying the input offset adjust potentiometer (P1) associated with the modu-

lation input. This procedure places a dc offset on the modulation input of the multiplier such that the carrier still passes thru the multiplier when the modulating signal is zero. The result is amplitude modulation. This is easily seen by examining the basic mathematical expression for amplitude modulation given below. For the case under discussion, with K = 1,

$$e_o = (E + E_m \cos\omega_m t)\,(E_c \cos\omega_c t)$$

where E is the dc input offset adjust voltage. This expression can be written as:

$$e_o = E_o\,[1 + M\cos\omega_c t]\,\cos\omega_c t$$

where $E_o = EE_c$

and $M = \dfrac{E_m}{E}$ = modulation index

This is the standard equation for amplitude modulation. From this, it is easy to see that 100% modulation can be achieved by adjusting the input offset adjust voltage to be exactly equal to the peak value of the modulation, E_m. This is done by observing the output waveform and adjusting the input offset potentiometer, P1, until the output exhibits the familiar amplitude modulation waveform.

5.5 Phase Detector

If the circuit of Figure 25 has as its inputs two signals of identical frequency but having a relative phase shift the output will be a dc signal which is directly proportional to the cosine of phase difference as well as the double frequency term.

$$e_c = E_c \cos\omega_c t$$

$$e_m = E_m \cos(\omega_c t + \phi)$$

$$e_o = e_c e_m = E_c E_m \cos\omega_c t \cos(\omega_c t + \phi)$$

or $$e_o = \frac{E_c E_m}{2}\,[\cos\phi + \cos(2\omega_c t + \phi)]$$

The addition of a simple low pass filter to the output (which eliminates the second cosine term) and return of R_L to an offset adjustment potentiometer will result in a dc output voltage which is proportional to the cosine of the phase difference. Hence, the circuit functions as a synchronous detector.

6. DEFINITIONS OF SPECIFICATIONS

Because of the unique nature of a multiplier, i.e., two inputs and one output, operating specifications are difficult to define and interpret. Indeed the same specification may be defined in several completely different ways depending upon which manufacturer is doing the defining. In order to clear up some of this mystery, the following definitions and examples are presented.

6.1 Multiplier Transfer Function

The output of the multiplier may be expressed by this equation:

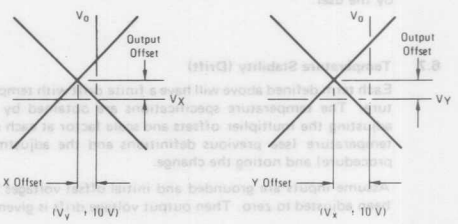
$$V_o = K\,(V_x \pm V_{iox} - V_{x\,off})\,(V_y \pm V_{ioy} - V_{y\,off}) \pm V_{oo} \quad (1)$$

where K = scale factor (see 6.5)

V_x = "x" input voltage
V_y = "y" input voltage
V_{iox} = "x" input offset voltage
V_{ioy} = "y" input offset voltage
$V_{x\,off}$ = "x" input offset adjust voltage
$V_{y\,off}$ = "y" input offset adjust voltage
V_{oo} = output offset voltage

The voltage transfer characteristic below indicates "X", "Y" and output offset voltages.

FIGURE 26



6.2 Linearity

Linearity is defined to be the maximum deviation of output voltage from a straight line transfer function. It is expressed as a percentage of full-scale output and is measured for V_x and V_y separately either using an "X-Y" plotter (and checking the deviation from a straight line) or by using the method shown in Figure 1. The latter method nulls the output signal with the input signal, resulting in distortion components proportional to the linearity.

Example: 0.35% linearity means

$$V_o = \frac{V_x V_y}{10} \pm (0.0035)\ (10\ \text{volts})$$

6.3 Input Offset Voltage

The input offset voltage is defined from Equation (1). It is measured for V_x and V_y separately and is defined to be that dc input offset adjust voltage ("x" or "y") that will result in minimum ac output when ac (5 Vpp, 1 kHz) is applied to the other input ("y" or "x" respectively). From Equation (1) we have:

$$V_{o(ac)} = K\,(0 \pm V_{iox} - V_{x\,off})\,(\sin\omega t)$$

adjust $V_{x\,off}$ so that $(\pm V_{iox} - V_{x\,off}) = 0$.

6.4 Output Offset Current and Voltage

Output offset current (I_{oo}) is the dc current flowing in the output lead when $V_x = V_y = 0$ and "X" and "Y" offset voltages are adjusted to zero.

Output offset voltage (V_{oo}) is:

$$V_{oo} = I_{oo} R_L$$

where R_L is the load resistance.

Note: Output offset voltage is defined by many manufacturers with all inputs at zero but without adjusting "X" and "Y" offset voltages to zero. Thus it includes input offset terms, an output offset term and a scale factor term.

6.5 Scale Factor

Scale factor is the K term in Equation (1). It determines the "gain" of the multiplier and is expressed approximately by the following equation.

$$K = \frac{2R_L}{R_x R_y I_1} \text{ where } R_x \text{ and } R_y >> \frac{kT}{qI_1}$$

and I_1 is the current out of pin 1.

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6.6 Total DC Accuracy

The total dc accuracy of a multiplier is defined as error in multiplier output with dc (±10 Vdc) applied to both inputs. It is expressed as a percent of full scale. Accuracy is not specified for the MC1594 because error terms can be nulled by the user.

6.7 Temperature Stability (Drift)

Each term defined above will have a finite drift with temperature. The temperature specifications are obtained by re-adjusting the multiplier offsets and scale factor at each new temperature (see previous definitions and the adjustment procedure) and noting the change.

Assume inputs are grounded and initial offset voltages have been adjusted to zero. Then output voltage drift is given by:

$$\Delta V_O = \pm[K \pm K\ (TCK)\ (\Delta T)\ ][\ (TCV_{iox})\ (\Delta T)\ ][\ (TCV_{ioy})\ (\Delta T)\ ] \pm (TCV_{oo})\ (\Delta T)$$

6.8 Total DC Accuracy Drift

This is the temperature drift in output voltage with 10 volts applied to each input. The output is adjusted to 10 volts at $T_A = +25^oC$. Assuming initial offset voltages have been adjusted to zero at $T_A = +25^oC$, then:

$$V_O = [K \pm K\ (TCK)\ (\Delta T)\ ][10 \pm (TCV_{iox})\ (\Delta T)\ ][10 \pm (TCV_{ioy})\ (\Delta T)\ ] \pm (TCV_{oo})\ (\Delta T)$$

6.9 Power Supply Rejection

Variation in power supply voltages will cause undesired variation of the output voltage. It is measured by superimposing a 1-volt, 100-Hz signal on each supply (±15 V) with each input grounded. The resulting change in the output is expressed in mV/V.

6.10 Output Voltage Swing

Output voltage swing capability is the maximum output voltage swing (without clipping) into a resistive load (note output offset is adjusted to zero).

If an op-ampl. is used, the multiplier output becomes a virtual ground – the swing is then determined by the scale factor and the op-ampl. selected.

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ORDERING INFORMATION

Device	Temperature Range	Package
MC1495L	0°C to +70°C	Ceramic DIP
MC1595L	−55°C to +125°C	Ceramic DIP

MC1495L
MC1595L

Specifications and Applications Information

WIDEBAND MONOLITHIC FOUR-QUADRANT MULTIPLIER

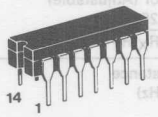
. . . designed for uses where the output is a linear product of two input voltages. Maximum versatility is assured by allowing the user to select the level shift method. Typical applications include: multiply, divide*, square root*, mean square*, phase detector, frequency doubler, balanced modulator/demodulator, electronic gain control.

*When used with an operational amplifier.

- Wide Bandwidth
- Excellent Linearity – 1% max Error on X-Input, 2% max Error on Y-Input – MC1595L
- Excellent Linearity – 2% max Error on X-Input, 4% max Error on Y-Input – MC1495L
- Adjustable Scale Factor, K
- Excellent Temperature Stability
- Wide Input Voltage Range – ± 10 Volts
- ± 15 Volt Operation

LINEAR FOUR-QUADRANT MULTIPLIER

SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 632-08

FIGURE 1 – FOUR-QUADRANT MULTIPLIER TRANSFER CHARACTERISTIC

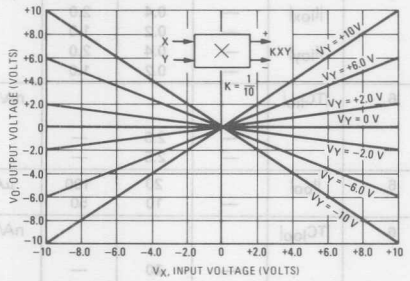


FIGURE 2 – TRANSCONDUCTANCE BANDWIDTH

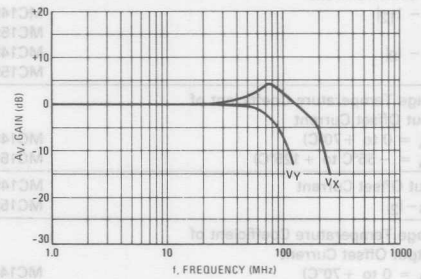
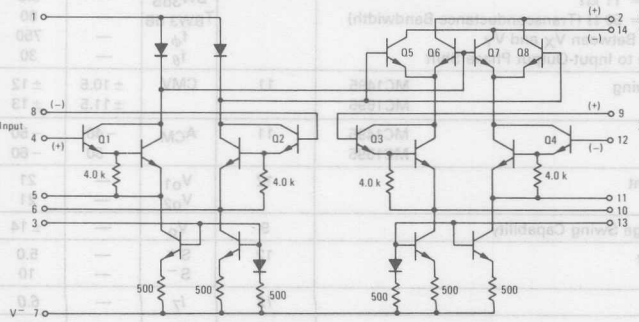


FIGURE 3 – CIRCUIT SCHEMATIC



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ELECTRICAL CHARACTERISTICS ($V^+ = +32$ V, $V^- = -15$ V, $T_A = +25°C$, $I_3 = I_{13} = 1.0$ mA, $R_X = R_Y = 15$ kΩ, $R_L = 11$ kΩ unless otherwise noted)

Characteristic		Figure	Symbol	Min	Typ	Max	Unit
Linearity:		5					%
Output Error in Percent of Full Scale:							
$T_A = +25°C$							
$-10 < V_X < +10$ ($V_Y = \pm 10$ V)	MC1495		E_{RX}	—	±1.0	±2.0	
	MC1595			—	±0.5	±1.0	
$-10 < V_Y < +10$ ($V_X = \pm 10$ V)	MC1495		E_{RY}	—	±2.0	±4.0	
	MC1595			—	±1.0	±2.0	
$T_A = 0$ to $+70°C$	MC1495						
$-10 < V_X < +10$ ($V_Y = \pm 10$ V)			E_{RX}	—	±1.5	—	
$-10 < V_Y < +10$ ($V_X = +10$ V)			E_{RY}	—	±3.0	—	
$T_A = -55°C$ to $+125°C$	MC1595						
$-10 < V_X < +10$ ($V_Y = \pm 10$ V)			E_{RX}	—	±0.75	—	
$-10 < V_Y < +10$ ($V_X = \pm 10$ V)			E_{RY}	—	±1.5	—	
Squaring Mode Error:		5	E_{SQ}				%
Accuracy in Percent of Full Scale After Offset and Scale Factor Adjustment							
$T_A = +25°C$	MC1495			—	±0.75	—	
	MC1595			—	±0.5	—	
$T_A = 0$ to $+70°C$	MC1495			—	±1.0	—	
$T_A = -55°C$ to $+125°C$	MC1595			—	±0.75	—	
Scale Factor (Adjustable) $(K = \frac{2R_L}{I_3 R_X R_Y})$		—	K	—	0.1	—	
Input Resistance	MC1495	7	R_{INX}	—	30	—	MΩ
(f = 20 Hz)	MC1595			—	35	—	
	MC1495		R_{INY}	—	20	—	
	MC1595			—	35	—	
Differential Output Resistance (f = 20 Hz)		8	R_o	—	300	—	kΩ
Input Bias Current		6					μA
$I_{bx} = \frac{(I_9 + I_{12})}{2}$, $I_{by} = \frac{(I_4 + I_8)}{2}$	MC1495		I_{bx}	—	2.0	12	
	MC1595			—	2.0	8.0	
	MC1495		I_{by}	—	2.0	12	
	MC1595			—	2.0	8.0	
Input Offset Current		6					μA
$\lvert I_9 - I_{12} \rvert$	MC1495		$\lvert I_{iox} \rvert$	—	0.4	2.0	
	MC1595			—	0.2	1.0	
$\lvert I_4 - I_8 \rvert$	MC1495		$\lvert I_{ioy} \rvert$	—	0.4	2.0	
	MC1595			—	0.2	1.0	
Average Temperature Coefficient of Input Offset Current		6	$\lvert TC_{Iio} \rvert$				nA/°C
($T_A = 0$ to $+70°C$)	MC1495			—	2.5	—	
($T_A = -55°C$ to $+125°C$)	MC1595			—	2.5	—	
Output Offset Current	MC1495	6	$\lvert I_{oo} \rvert$		20	100	μA
$\lvert I_{14} - I_2 \rvert$	MC1595			—	10	50	
Average Temperature Coefficient of Output Offset Current		6	$\lvert TC_{Ioo} \rvert$				nA/°C
($T_A = 0$ to $+70°C$)	MC1495			—	20	—	
($T_A = -55°C$ to $+125°C$)	MC1595			—	20	—	
Frequency Response		9,10					
3.0 dB Bandwidth, $R_L = 11$ kΩ			BW_{3dB}	—	3.0	—	MHz
3.0 dB Bandwidth, $R_L = 50$ Ω (Transconductance Bandwidth)			$T_{BW3\ dB}$	—	80	—	MHz
3° Relative Phase Shift Between V_X and V_Y			f_ϕ	—	750	—	kHz
1% Absolute Error Due to Input-Output Phase Shift			f_θ	—	30	—	kHz
Common Mode Input Swing	MC1495	11	CMV	±10.5	±12	—	Vdc
(Either Input)	MC1595			±11.5	±13	—	
Common Mode Gain	MC1495	11	A_{CM}	−40	−50	—	dB
(Either Input)	MC1595			−50	−60	—	
Common Mode Quiescent Output Voltage		12	V_{o1}	—	21	—	Vdc
			V_{o2}	—	21	—	
Differential Output Voltage Swing Capability		9	V_o	—	±14	—	V_{peak}
Power Supply Sensitivity		12	S^+	—	5.0	—	mV/V
			S^-	—	10	—	
Power Supply Current		12	I_7	—	6.0	7.0	mA
DC Power Dissipation		12	P_D	—	135	170	mW

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MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Applied Voltage (V_2-V_1, $V_{14}-V_1$, V_1-V_9, V_1-V_{12}, V_1-V_4, V_1-V_8, $V_{12}-V_7$, V_9-V_7, V_8-V_7, V_4-V_7)	ΔV	30	Vdc
Differential Input Signal	$V_{12}-V_9$ V_4-V_8	$\pm(6+I_{13}R_X)$ $\pm(6+I_3R_Y)$	Vdc Vdc
Maximum Bias Current	I_3 I_{13}	10 10	mA
Power Dissipation (Package Limitation) Ceramic Package Derate above T_A = +25°C	P_D	 750 5.0	 mW mW/°C
Operating Temperature Range MC1495 MC1595	T_A	 0 to +70 -55 to +125	°C °C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TEST CIRCUITS

FIGURE 4 – LINEARITY (USING NULL TECHNIQUE)

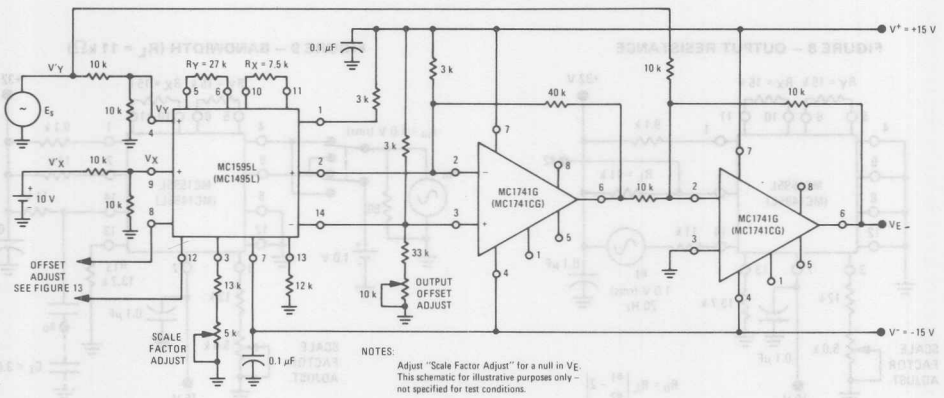
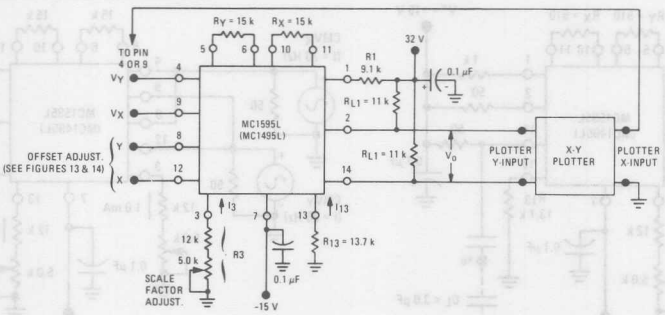


FIGURE 5 – LINEARITY (USING X-Y PLOTTER TECHNIQUE)



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TEST CIRCUITS (continued)

FIGURE 6 – INPUT AND OUTPUT CURRENT

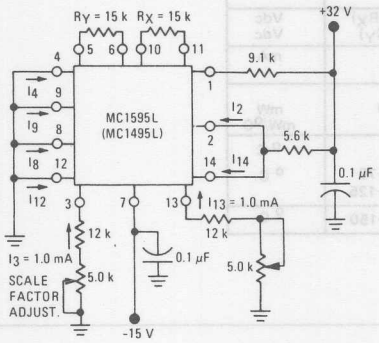


FIGURE 7 – INPUT RESISTANCE

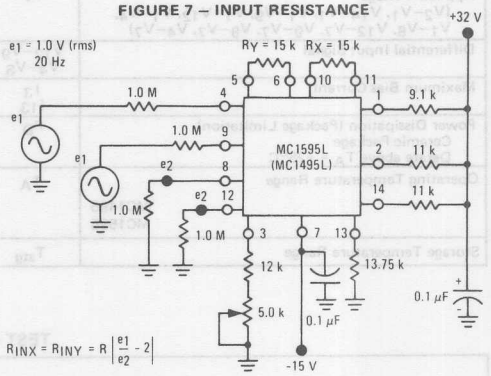


FIGURE 8 – OUTPUT RESISTANCE

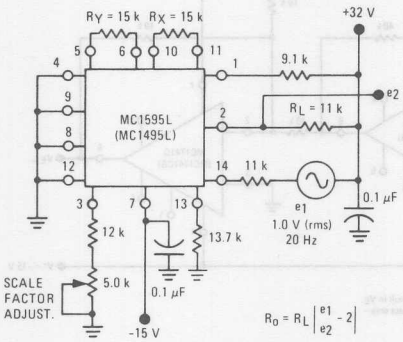


FIGURE 9 – BANDWIDTH (R_L = 11 kΩ)

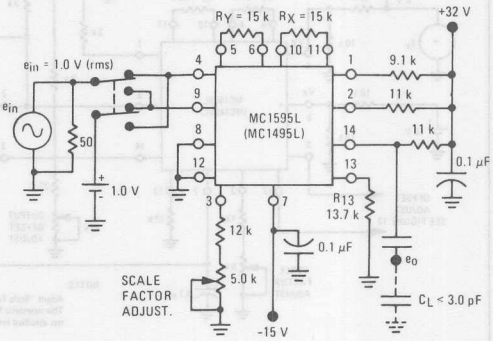


FIGURE 10 – BANDWIDTH (R_L = 50 Ω)

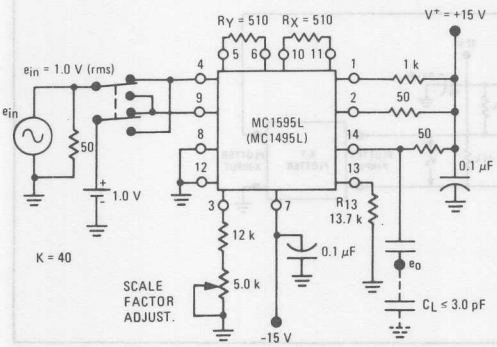
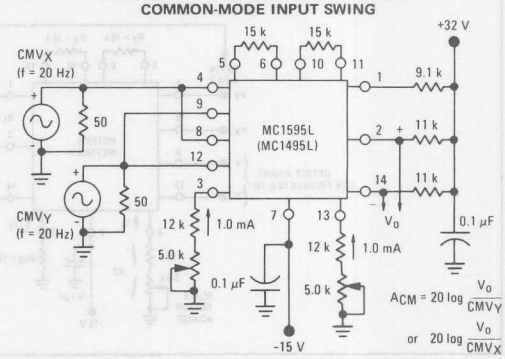


FIGURE 11 – COMMON-MODE GAIN and COMMON-MODE INPUT SWING



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TEST CIRCUITS (continued)

FIGURE 12 – POWER SUPPLY SENSITIVITY

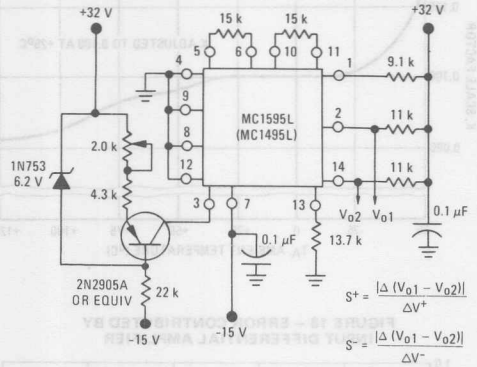
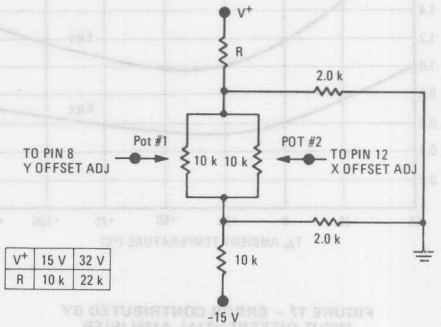
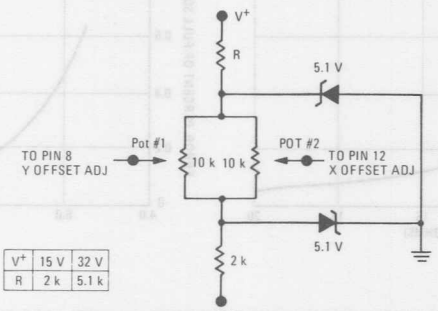


FIGURE 13 – OFFSET ADJUST CIRCUIT



V^+	15 V	32 V
R	10 k	22 k

FIGURE 14 – OFFSET ADJUST CIRCUIT (ALTERNATE)



V^+	15 V	32 V
R	2 k	5.1 k

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FIGURE 15 – LINEARITY versus TEMPERATURE

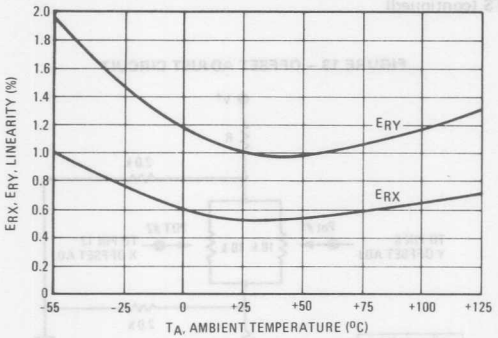


FIGURE 16 – SCALE FACTOR versus TEMPERATURE

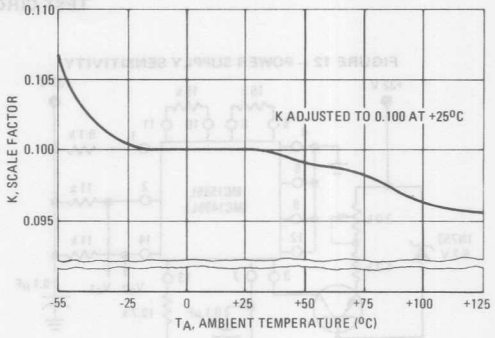


FIGURE 17 – ERROR CONTRIBUTED BY INPUT DIFFERENTIAL AMPLIFIER

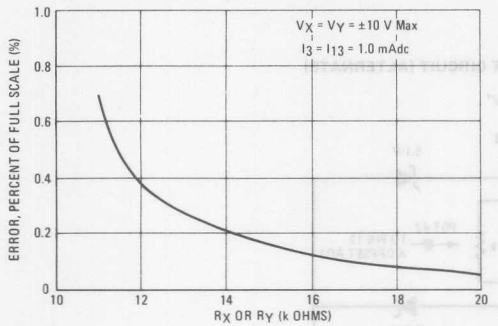


FIGURE 18 – ERROR CONTRIBUTED BY INPUT DIFFERENTIAL AMPLIFIER

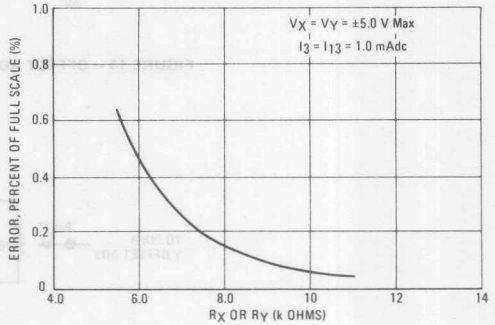
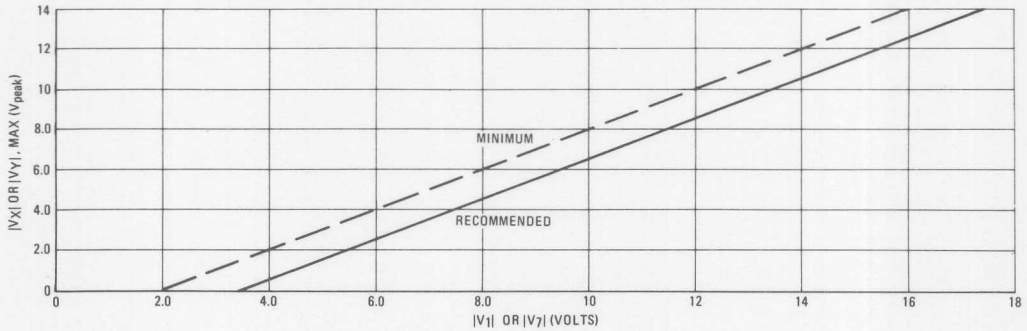


FIGURE 19 – MAXIMUM ALLOWABLE INPUT VOLTAGE versus VOLTAGE AT PIN 1 OR PIN 7



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OPERATION AND APPLICATIONS INFORMATION

1. Theory of Operation

The MC1595 (MC1495) is a monolithic, four-quadrant multiplier which operates on the principle of variable transconductance. The detailed theory of operation is covered in Application Note AN-489, Analysis and Basic Operation of the MC1595. The result of this analysis is that the differential output current of the multiplier is given by

$$I_A - I_B = \Delta I = \frac{2V_X V_Y}{R_X R_Y I_3}$$

where I_A and I_B are the currents into pins 14 and 2, respectively, and V_X and V_Y are the X and Y input voltages at the multiplier input terminals.

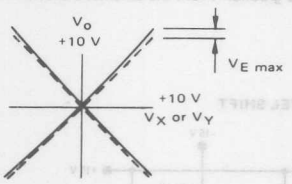
2. Design Considerations

2.1 General

The MC1595 (MC1495) permits the designer to tailor the multiplier to a specific application by proper selection of external components. External components may be selected to optimize a given parameter (e.g. bandwidth) which may in turn restrict another parameter (e.g. maximum output voltage swing). Each important parameter is discussed in detail in the following paragraphs.

2.1.1 Linearity, Output Error, E_{RX} or E_{RY}

Linearity error is defined as the maximum deviation of output voltage from a straight line transfer function. It is expressed as error in percent of full scale (see figure below).



For example, if the maximum deviation, $V_{E(max)}$, is ±100 mV and the full scale output is 10 volts, then the percentage error is

$$E_R = \frac{V_{E(max)}}{V_{o(max)}} \times 100 = \frac{100 \times 10^{-3}}{10} \times 100 = \pm 1.0\%.$$

Linearity error may be measured by either of the following methods:

1. Using an X – Y plotter with the circuit shown in Figure 5, obtain plots for X and Y similar to the one shown above.
2. Use the circuit of Figure 4. This method nulls the level shifted output of the multiplier with the original input. The peak output of the null operational amplifier will be equal to the error voltage, $V_{E(max)}$.

One source of linearity error can arise from large signal nonlinearity in the X and Y-input differential amplifiers. To avoid introducing error from this source, the emitter degeneration resistors R_X and R_Y must be chosen large enough so that nonlinear base-emitter voltage variation can be ignored. Figures 17 and 18 show the error expected from this source as a function of the values of R_X and R_Y with an operating current of 1.0 mA in each side of the differential amplifiers (i.e., $I_3 = I_{13} = 1.0$ mA).

2.1.2 3 dB-Bandwidth and Phase Shift

Bandwidth is primarily determined by the load resistors and the stray multiplier output capacitance and/or the operational amplifier used to level shift the output. If wideband operation is desired, low value load resistors and/or a wideband operational amplifier should be used. Stray output capacitance will depend to a large extent on circuit layout.

Phase shift in the multiplier circuit results from two sources: phase shift common to both X and Y channels (due to the load resistor-output capacitance pole mentioned above) and relative phase shift between X and Y channels (due to differences in transadmittance in the X and Y channels). If the input to output phase shift is only 0.6°, the output product of two sine waves will exhibit a vector error of 1%. A 3° relative phase shift between V_X and V_Y results in a vector error of 5%.

2.1.3 Maximum Input Voltage

$V_{X(max)}$, $V_{Y(max)}$ maximum input voltages must be such that:

$$V_{X(max)} < I_{13} R_Y$$

$$V_{Y(max)} < I_3 R_Y.$$

Exceeding this value will drive one side of the input amplifier to "cutoff" and cause non-linear operation.

Currents I_3 and I_{13} are chosen at a convenient value (observing power dissipation limitation) between 0.5 mA and 2.0 mA, approximately 1.0 mA. Then R_X and R_Y can be determined by considering the input signal handling requirements.

For $V_{X(max)} = V_{Y(max)} = 10$ volts:

$$R_X = R_Y > \frac{10\ V}{1.0\ mA} = 10\ k\Omega.$$

The equation $I_A - I_B = \dfrac{2V_X V_Y}{R_X R_Y I_3}$

is derived from $I_A - I_B = \dfrac{2V_X V_Y}{(R_X + \frac{2kT}{qI_{13}})(R_Y + \frac{2kT}{qI_3}) I_3}$

with the assumption $R_X \gg \dfrac{2kT}{qI_{13}}$ and $R_Y \gg \dfrac{2kT}{qI_3}$

At $T_A = +25°C$ and $I_{13} = I_3 = 1$ mA,

$$\frac{2kT}{qI_{13}} = \frac{2kT}{qI_3} = 52\ \Omega.$$

Therefore, with $R_X = R_Y = 10\ k\Omega$ the above assumption is valid. Reference to Figure 19 will indicate limitations of $V_{X(max)}$ or $V_{Y(max)}$ due to V_1 and V_7. Exceeding these limits will cause saturation or "cutoff" of the input transistors. See Step 4 of Section 3 (General Design Procedure) for further details.

2.1.4 Maximum Output Voltage Swing

The maximum output voltage swing is dependent upon the factors mentioned below and upon the particular circuit being considered.

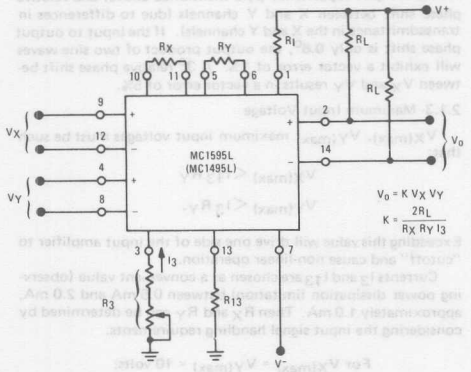
For Figure 20 the maximum output swing is dependent upon V^+ for positive swing and upon the voltage at pin 1 for negative swing. The potential at pin 1 determines the quiescent level for transistors Q_5, Q_6, Q_7, and Q_8. This potential

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OPERATION AND APPLICATIONS INFORMATION (continued)

should be related so that negative swing at pins 2 or 14 does not saturate those transistors. See Section 3 for further information regarding selection of these potentials.

FIGURE 20 – BASIC MULTIPLIER



If an operational amplifier is used for level shift, as shown in Figure 21, the output swing (of the multiplier) is greatly reduced. See Section 3 for further details.

3. General Design Procedure

Selection of component values is best demonstrated by the following example: assume resistive dividers are used at the X and Y inputs to limit the maximum multiplier input to ±5.0 volts ($V_X = V_{Y\,[max]}$) for a ±10-volt input ($V_X' = V_{Y'\,[max]}$). (See Figure 21). If an overall scale factor of 1/10 is desired, then

$$V_o = \frac{V_X' V_Y'}{10} = \frac{(2V_X)(2V_Y)}{10} = 4/10\ V_X V_Y .$$

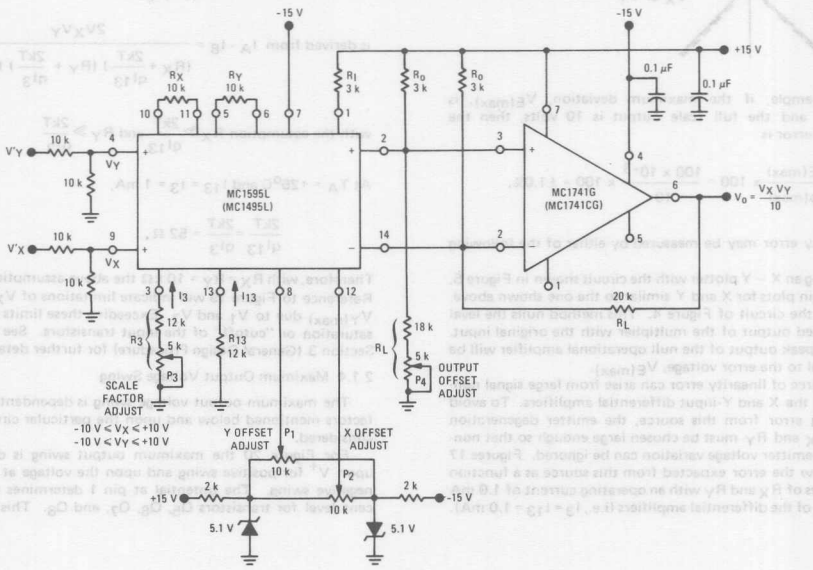
Therefore, K = 4/10 for the multiplier (excluding the divider network).

Step 1. The first step is to select current I_3 and current I_{13}. There are no restrictions on the selection of either of these currents except the power dissipation of the device. I_3 and I_{13} will normally be one or two milliamperes. Further, I_3 does not have to be equal to I_{13}, and there is normally no need to make them different. For this example, let

$$I_3 = I_{13} = 1\ mA.$$

To set currents I_3 and I_{13} to the desired value, it is only necessary to connect a resistor between pin 13 and ground, and between pin 3 and ground. From the schematic shown in Figure 3,

FIGURE 21 – MULTIPLIER WITH OP-AMPL. LEVEL SHIFT



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OPERATION AND APPLICATIONS INFORMATION (continued)

it can be seen that the resistor values necessary are given by:

$$R_{13} + 500\ \Omega = \frac{|V^-| - 0.7\ V}{I_{13}}$$

$$R_3 + 500\ \Omega = \frac{|V^-| - 0.7\ V}{I_3}$$

Let $V^- = -15$ V

Then $R_{13} + 500 = \frac{14.3\ V}{1\ mA}$ or $R_{13} = 13.8\ k\Omega$

Let $R_{13} = 12\ k\Omega$

Similarly, $R_3 = 13.8\ k\Omega$

Let $R_3 = 15\ k\Omega$

However, for applications which require an accurate scale factor, the adjustment of R_3 and consequently, I_3, offers a convenient method of making a final trim of the scale factor. For this reason, as shown in Figure 21, resistor R_3 is shown as a fixed resistor in series with a potentiometer.

For applications not requiring an exact scale factor (balanced modulator, frequency doubler, AGC amplifier, etc.), pins 3 and 13 can be connected together and a single resistor from pin 3 to ground can be used. In this case, the single resistor would have a value of one-half the above calculated value for R_{13}.

Step 2. The next step is to select R_X and R_Y. To insure that the input transistors will always be active, the following conditions should be met:

$$\frac{V_X}{R_X} < I_{13} \qquad \frac{V_Y}{R_Y} < I_3.$$

A good rule of thumb is to make $I_3 R_Y \geq 1.5\ V_{Y(max)}$ and $I_{13} RX \geq 1.5\ V_{X(max)}$.

The larger the $I_3 R_Y$ and $I_{13} R_X$ product in relation to V_Y and V_X respectively, the more accurate the multiplier will be (see Figures 17 and 18).

Let $R_X = R_Y = 10\ k\Omega$

Then $I_3 R_Y = 10$ V

$I_{13} R_X = 10$ V

since $V_{X(max)} = V_{Y(max)} = 5.0$ volts the value of $R_X = R_Y = 10\ k\Omega$ is sufficient.

Step 3. Now that R_X, R_Y and I_3 have been chosen, R_L can be determined:

$$K = \frac{2R_L}{R_X R_Y I_3} = \frac{4}{10}$$

or $$\frac{(2)\ (R_L)}{(10\ k)\ (10\ k)\ (1\ mA)} = \frac{4}{10}$$

Thus $R_L = 20\ k\Omega$.

Step 4. To determine what power-supply voltage is necessary for this application, attention must be given to the circuit schematic shown in Figure 3. From the circuit schematic it can be seen that in order to maintain transistors Q_1, Q_2, Q_3 and Q_4 in an active region when the maximum input voltages are applied ($V_X' = V_Y' = 10$ V or $V_X = 5.0$ V, $V_Y = 5.0$ V), their respective collector voltage should be at least a few tenths of a volt higher than the maximum input voltage. It should also be noticed that the collector voltage of transistors Q_3 and Q_4 are at a potential which is two diode-drops below the voltage at pin 1. Thus, the voltage at pin 1 should be about two volts higher than the maximum input voltage. Therefore, to handle +5.0 volts at the inputs, the voltage at pin 1 must be at least +7.0 volts. Let $V_1 = 9.0$ Vdc.

Since the current following into pin 1 is always equal to $2I_3$, the voltage at pin 1 can be set by placing a resistor, R_1 from pin 1 to the positive supply:

$$R_1 = \frac{V^+ - V_1}{2I_3}$$

Let $V^+ = +15$ V

Then $R_1 = \frac{15\ V - 9\ V}{(2)\ (1\ mA)}$

$R_1 = 3\ k\Omega$.

Note that the voltage at the base of transistors Q_5, Q_6, Q_7 and Q_8 is one diode-drop below the voltage at pin 1. Thus, in order that these transistors stay active, the voltage at pins 2 and 14 should be approximately halfway between the voltage at pin 1 and the positive-supply voltage. For this example, the voltage at pins 2 and 14 should be approximately 11 volts.

Step 5. Level Shifting

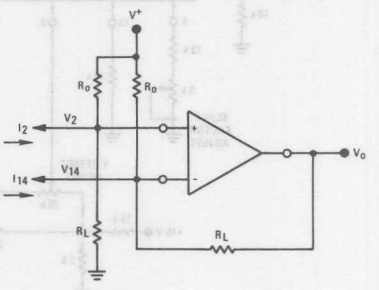
For dc applications, such as the multiply, divide and square-root functions, it is usually desirable to convert the differential output to a single-ended output voltage referenced to ground. The circuit shown in Figure 22 performs this function. It can be shown that the output voltage of this circuit is given by:

$$V_o = (I_2 - I_{14})\ R_L$$

And since $I_A - I_B = I_2 - I_{14} = \frac{2I_X I_Y}{I_3} = \frac{2\ V_X V_Y}{I_3 R_X R_Y}$

Then $V_o = \frac{2R_L V_X' V_Y'}{4R_X R_X I_3}$ where $V_X' V_Y'$ is the voltage at the input to the voltage dividers.

FIGURE 22 – LEVEL SHIFT CIRCUIT



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The choice of an operational amplifier for this application should have low bias currents, low offset current, and a high common-mode input voltage range as well as a high common-mode rejection ratio. The MC1556, and MC1741 operational amplifiers meet these requirements.

Referring to Figure 21, the level shift components will be determined. When $V_X = V_Y = 0$, the currents I_2 and I_{14} will be equal to I_{13}. In Step 3, R_L was found to be 20 kΩ and in Step 4, V_2 and V_{14} were found to be approximately 11 volts. From this information, R_o can be found easily from the following equation (neglecting the operational amplifiers bias current):

$$\frac{V_2}{R_L} + I_{13} = \frac{V^+ - V_2}{R_o}$$

And for this example, $\frac{11\ V}{20\ k\Omega} + 1\ mA = \frac{15\ V - 11\ V}{R_o}$

Solving for R_o, $R_o = 2.6\ k\Omega$

Thus, select $R_o = 3.0\ k\Omega$

For $R_o = 3.0\ k\Omega$, the voltage at pins 2 and 14 is calculated to be

$$V_2 = V_{14} = 10.4 \text{ volts.}$$

The linearity of this circuit (Figure 21) is likely to be as good or better than the circuit of Figure 5. Further improvements are possible as shown in Figure 23 where R_Y has been increased substantially to improve the Y linearity, and R_X decreased somewhat so as not to materially affect the X linearity, this avoids increasing R_L significantly in order to maintain a K of 0.1.

The versatility of the MC1595 (MC1495) allows the user to to optimize its performance for various input and output signal levels.

4. Offset and Scale Factor Adjustment

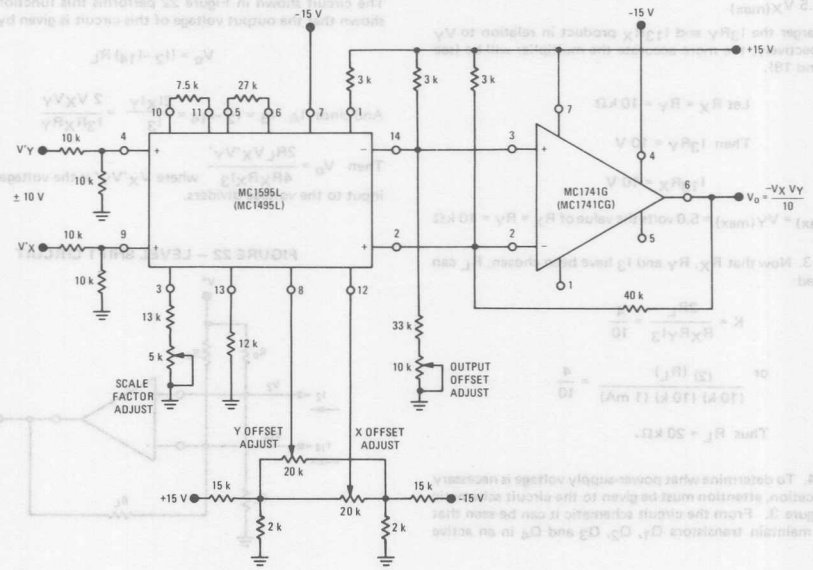
4.1 Offset Voltages

Within the monolithic multiplier (Figure 3) transistor base-emitter junctions are typically matched within 1 mV and resistors are typically matched within 2%. Even with this careful matching, an output error can occur. This output error is comprised of X-input offset voltage, Y-input offset voltage, and output-offset voltage. These errors can be adjusted to zero with the techniques shown in Figure 21. Offset terms can be shown analytically by the transfer function:

$$V_o = K(V_X \pm V_{IOX} \pm V_{X\,off})(V_Y \pm V_{IOY} \pm V_{Y\,off}) \pm V_{oo} \quad (1)$$

Where K = scale factor
V_X = X input voltage
V_Y = Y input voltage
V_{IOX} = X input offset voltage
V_{IOY} = Y input offset voltage
$V_{X\,off}$ = X input offset adjust voltage
$V_{Y\,off}$ = Y input offset adjust voltage
V_{oo} = output offset voltage.

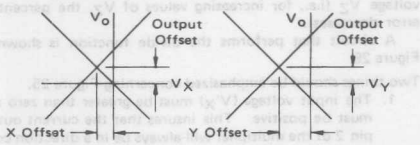
FIGURE 23 – MULTIPLIER WITH IMPROVED LINEARITY



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OPERATION AND APPLICATIONS INFORMATION (continued)

X, Y and Output Offset Voltages



For most dc applications, all three offset adjust potentiometers (P_1, P_2, P_4) will be necessary. One or more offset adjust potentiometers can be eliminated for ac applications (See Figures 28, 29, 30, 31).

If well regulated supply voltages are available, the offset adjust circuit of Figure 13 is recommended. Otherwise, the circuit of Figure 14 will greatly reduce the sensitivity to power supply changes.

4.2 Scale Factor

The scale factor, K, is set by P_3(Figure 21). P_3 varies I_3 which inversely controls the scale factor K. It should be noted that current I_3 is one-half the current through R_1. R_1 sets the bias level for Q_5, Q_6, Q_7, and Q_8 (See Figure 3). Therefore, to be sure that these devices remain active under all conditions of input and output swing, care should be exercised in adjusting P_3 over wide voltage ranges (see Section 3, General Design Procedure).

4.3 Adjustment Procedures

The following adjustment procedure should be used to null the offsets and set the scale factor for the multiply mode of operation. (See Figure 21)

1. X Input Offset
   (a) Connect oscillator (1 kHz, 5 Vpp sinewave) to the "Y" input (pin 4)
   (b) Connect "X" input (pin 9) to ground
   (c) Adjust X offset potentiometer, P_2, for an ac null at the output
2. Y Input Offset
   (a) Connect oscillator (1 kHz, 5 Vpp sinewave) to the "X" input (pin 9)
   (b) Connect "Y" input (pin 4) to ground
   (c) Adjust "Y" offset potentiometer, P_1, for an ac null at the output
3. Output Offset
   (a) Connect both "X" and "Y" inputs to ground
   (b) Adjust output offset potentiometer, P_4, until the output voltage V_o is zero volts dc
4. Scale Factor
   (a) Apply +10 Vdc to both the "X" and "Y" inputs
   (b) Adjust P_3 to achieve + 10.00 V at the output.
5. Repeat steps 1 through 4 as necessary.

The ability to accurately adjust the MC1595 (MC1495) depends upon the characteristics of potentiometers P_1 through P_4. Multi-turn, infinite resolution potentiometers with low-temperature coefficients are recommended.

5. DC Applications

5.1 Multiply

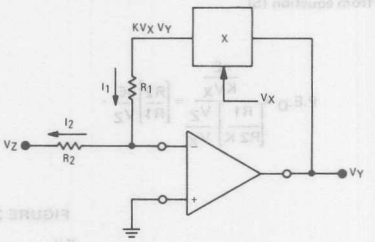
The circuit shown in Figure 21 may be used to multiply signals from dc to 100 kHz. Input levels to the actual multiplier are 5.0 V (max). With resistive voltage dividers the maximum could be very large — however, for this application two-to-one dividers have been used so that the maximum input level is 10 V. The maximum output level has also been designed for 10 V (max).

5.2 Squaring Circuit

If the two inputs are tied together, the resultant function is squaring; that is $V_o = KV^2$ where K is the scale factor. Note that all error terms can be eliminated with only three adjustment potentiometers, thus eliminating one of the input offset adjustments. Procedures for nulling with adjustments are given as follows:

1. AC Procedure:
   (a) Connect oscillator (1 kHz, 15 Vpp) to input
   (b) Monitor output at 2 kHz with tuned voltmeter and adjust P_3 for desired gain (be sure to peak response of the voltmeter)
   (c) Tune voltmeter to 1 kHz and adjust P_1 for a minimum output voltage
   (d) Ground input and adjust P_4 (output offset) for zero volts dc output
   (e) Repeat steps a through d as necessary.
2. DC Procedure:
   (a) Set $V_X = V_Y = 0$ V and adjust P_4 (output offset potentiometer) such that $V_o = 0.0$ Vdc
   (b) Set $V_X = V_Y = 1.0$ V and adjust P_1 (Y input offset potentiometer) such that the output voltage is +0.100 volts
   (c) Set $V_X = V_Y = 10$ Vdc and adjust P_3 such that the output voltage is +10.00 volts
   (d) Set $V_X = V_Y = -10$ Vdc. Repeat steps a through d as necessary.

FIGURE 24 — BASIC DIVIDE CIRCUIT



5.3 Divide Circuit

Consider the circuit shown in Figure 24 in which the multiplier is placed in the feedback path of an operational amplifier. For this configuration, the operational amplifier will maintain a "virtual ground" at the inverting (-) input. Assuming that the bias current of the operational amplifier is negligible, then $I_1 = I_2$ and

$$\frac{KV_XV_Y}{R1} = \frac{-V_Z}{R2} \quad (1)$$

Solving for V_Y,

$$V_Y = \frac{-R1}{R2\,K}\,\frac{V_Z}{V_X}. \quad (2)$$

If $R1 = R2$

$$V_Y = \frac{-V_Z}{KV_X} \quad (3)$$

If $R1 = KR2$

$$V_Y = \frac{-V_Z}{V_X}. \quad (4)$$

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OPERATION AND APPLICATIONS INFORMATION (continued)

Hence, the output voltage is the ratio of V_Z to V_X and provides a divide function. This analysis is, of course, the ideal condition. If the multiplier error is taken into account, the output voltage is found to be

$$V_Y = -\left[\frac{R1}{R2\ K}\right]\frac{V_Z}{V_X} + \frac{\triangle E}{K V_X}, \quad (5)$$

where $\triangle E$ is the error voltage at the output of the multiplier. From this equation, it is seen that divide accuracy is strongly dependent upon the accuracy at which the multiplier can be set, particularly at small values of V_Y. For example, assume that R1 = R2, and K = 1/10. For these conditions the output of the divide circuit is given by:

$$V_Y = \frac{-10\ V_Z}{V_X} + \frac{10\ \triangle E}{V_X}, \quad (6)$$

From equation 6, it is seen that only when V_X = 10 V is the error voltage of the divide circuit as low as the error of the multiply circuit. For example, when V_X is small, (0.1 volt) the error voltage of the divide circuit can be expected to be a hundred times the error of the basic multiplier circuit.

In terms of percentage error,

$$\text{percentage error} = \frac{\text{error}}{\text{actual}} \times 100\%$$

or from equation (5),

$$P.E._D = \frac{\frac{\triangle E}{K V_X}}{\left[\frac{R1}{R2\ K}\right]\frac{V_Z}{V_X}} = \left[\frac{R2}{R1}\right]\frac{\triangle E}{V_Z}. \quad (7)$$

From equation 7, the percentage error is inversely related to voltage V_Z (i.e., for increasing values of V_Z, the percentage error decreases).

A circuit that performs the divide function is shown in Figure 25.

Two things should be emphasized concerning Figure 25.

1. The input voltage (V'_X) must be greater than zero and must be positive. This insures that the current out of pin 2 of the multiplier will always be in a direction compatible with the polarity of V_Z.
2. Pins 2 and 14 of the multiplier have been interchanged in respect to the operational amplifiers input terminals. In this instance, Figure 25 differs from the circuit connection shown in Figure 21; necessitated to insure negative feedback around the loop.

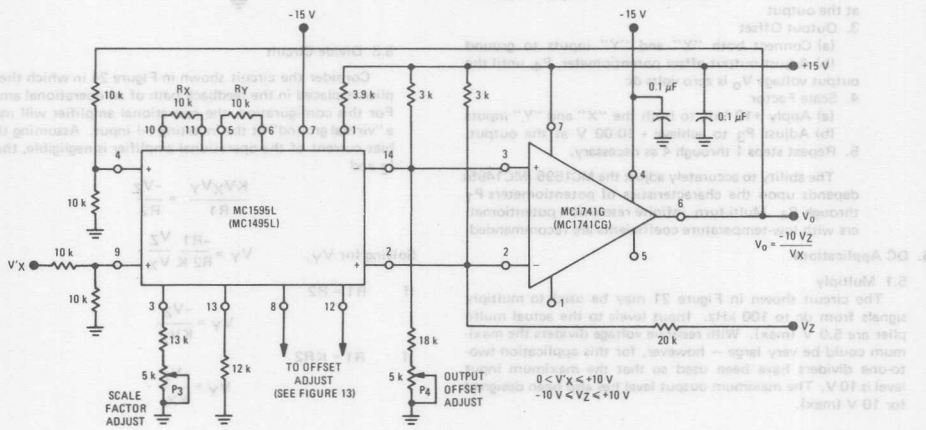
A Suggested Adjustment Procedure for the Divide Circuit

1. Set V_Z = 0 volts and adjust the output offset potentiometer (P_4) until the output voltage (V_o) remains at some (not necessarily zero) constant value as V_X' is varied between +1.0 volt and +10 volts.
2. Keep V_Z at 0 volts, set V_X' at +10 volts and adjust the Y input offset potentiometer (P_1) until V_o = 0 volts.
3. Let $V_X' = V_Z$ and adjust the X input offset potentiometer (P_2) until the output voltage remains at some (not necessarily - 10 volts) constant value as $V_Z = V_X'$ is varied between +1.0 and +10 volts.
4. Keep $V_X' = V_Z$ and adjust the scale factor potentiometer (P_3) until the average value of V_o is - 10 volts as $V_Z = V_X'$ is varied between +1.0 volt and +10 volts.
5. Repeat steps 1 through 4 as necessary to achieve optimum performance.

5.4 Square Root

A special case of the divide circuit in which the two inputs to the multiplier are connected together is the square root function

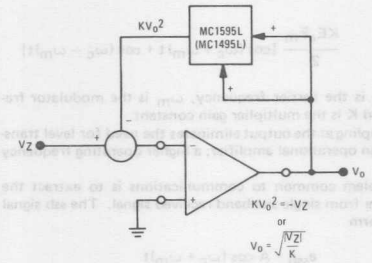
FIGURE 25 – DIVIDE CIRCUIT



11

OPERATION AND APPLICATIONS INFORMATION (continued)

FIGURE 26 – BASIC SQUARE ROOT CIRCUIT



as indicated in Figure 26. This circuit may suffer from latch-up problems similar to those of the divide circuit. Note that only one polarity of input is allowed and diode clamping (see Figure 27) protects against accidental latch-up.

This circuit also may be adjusted in the closed-loop mode as follows:

1. Set V_Z to -0.01 volts and adjust P_4 (output offset) for V_o = +0.316 volts, being careful to approach the output from the positive side to preclude the effect of the output diode clamping.
2. Set V_Z to -0.9 volts and adjust P_2 (X adjust) for V_o = +3.0 volts.
3. Set V_Z to -10 volts and adjust P_3 (scale factor adjust) for V_o = +10 volts.
4. Steps 1 through 3 may be repeated as necessary to achieve desired accuracy.

6. AC Applications

The applications that follow demonstrate the versatility of the monolithic multiplier. If a potted multiplier is used for these cases, the results generally would not be as good because the potted units have circuits that, although they optimize dc multiplication operation, can hinder ac applications.

6.1 Frequency doubling often is done with a diode where the fundamental plus a series of harmonics are generated. However, extensive filtering is required to obtain the desired harmonic, and the second harmonic obtained under this technique usually is small in magnitude and requires amplification.

When a multiplier is used to double frequency the second harmonic is obtained directly, except for a dc term, which can be removed with ac coupling.

$$e_o = KE^2 \cos^2 \omega t$$

$$e_o = \frac{KE^2}{2} (1 + \cos 2\omega t).$$

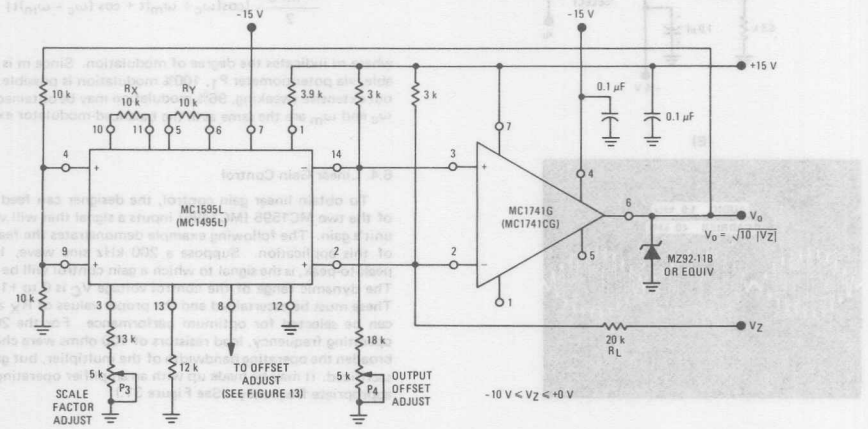
A potted multiplier can be used to obtain the double frequency component, but frequency would be limited by its internal level-shift amplifier. In the monolithic units, the amplifier is omitted.

In a typical doubler circuit, conventional ± 15-volt supplies are used. An input dynamic range of 5.0 volts peak-to-peak is allowed. The circuit generates wave-forms that are double frequency; less than 1% distortion is encountered without filtering. The configuration has been successfully used in excess of 200 kHz; reducing the scale factor by decreasing the load resistors can further expand the bandwidth.

A slightly modified version of the MC1595 (MC1495) – the MC1596 (MC1496) – has been successfully used as a doubler to obtain 400 MHz. (See Figure 28.)

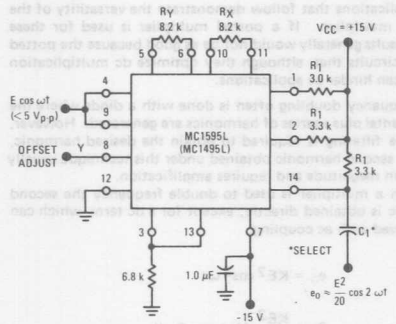
6.2 Figure 29 represents an application for the monolithic multiplier as a balanced modulator. Here, the audio input signal is 1.6 kHz and the carrier is 40 kHz.

FIGURE 27 – SQUARE ROOT CIRCUIT



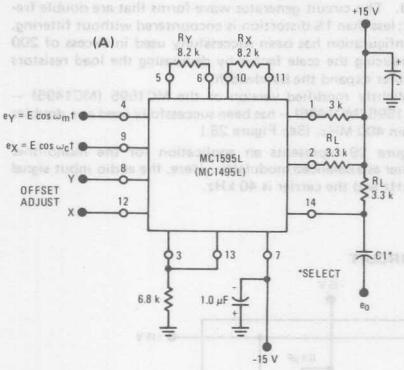
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FIGURE 28 – FREQUENCY DOUBLER

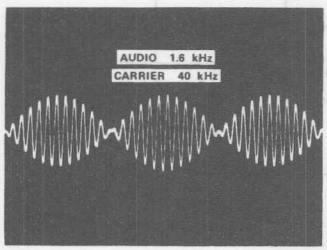


When two equal cosine waves are applied to X and Y, the result is a wave shape of twice the input frequency. For this example the input was a 10 kHz signal, output was 20 kHz.

FIGURE 29 – BALANCED MODULATOR



(B)



The defining equation for balanced modulation is

$$K(E_m \cos \omega_m t)(E_c \cos \omega_c t) =$$

$$\frac{KE_cE_m}{2}[\cos(\omega_c + \omega_m)t + \cos(\omega_c - \omega_m)t]$$

where ω_c is the carrier frequency, ω_m is the modulator frequency and K is the multiplier gain constant.

AC coupling at the output eliminates the need for level translation or an operational amplifier; a higher operating frequency results.

A problem common to communications is to extract the intelligence from single-sideband received signal. The ssb signal is of the form

$$e_{ssb} = A \cos(\omega_c + \omega_m)t$$

and if multiplied by the appropriate carrier waveform, cos $\omega_c t$,

$$e_{ssb}e_{carrier} = \frac{AK}{2}[\cos(2\omega_c + \omega_m)t + \cos(\omega_c)t].$$

If the frequency of the band-limited carrier signal, ω_c, is ascertained in advance the designer can insert a low-pass filter and obtain the (AK/2) (cos $\omega_c t$) term with ease. He also can use an operational amplifier for a combination level shift-active filter, as an external component. But in potted multipliers, even if the frequency range can be covered, the operational amplifier is inside and not accessible, so the user must accept the level shifting provided, and still add a low-pass filter.

6.3 Amplitude Modulation

The multiplier performs amplitude modulation, similar to balanced modulation, when a dc term is added to the modulating signal with the Y offset adjust potentiometer. (See Figure 30.)

Here, the identity is

$$E_m(1 + m \cos \omega_m t)E_c \cos \omega_c t = KE_mE_c \cos \omega_c t +$$

$$\frac{KE_mE_cm}{2}[\cos(\omega_c + \omega_m)t + \cos(\omega_c - \omega_m)t]$$

where m indicates the degree of modulation. Since m is adjustable, via potentiometer P_1, 100% modulation is possible. Without extensive tweaking, 96% modulation may be obtained where ω_c and ω_m are the same as in the balanced-modulator example.

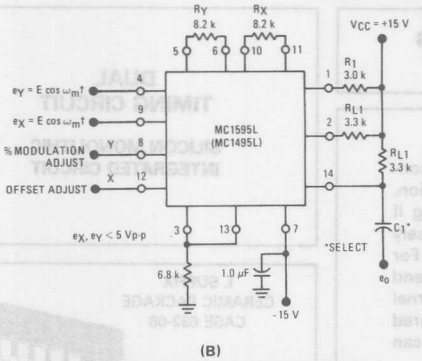
6.4 Linear Gain Control

To obtain linear gain control, the designer can feed to one of the two MC1595 (MC1495) inputs a signal that will vary the unit's gain. The following example demonstrates the feasibility of this application. Suppose a 200 kHz sine wave, 1.0 volt peak-to-peak, is the signal to which a gain control will be added. The dynamic range of the control voltage V_C is 0 to +1.0 volt. These must be ascertained and the proper values of R_X and R_Y can be selected for optimum performance. For the 200-kHz operating frequency, load resistors of 100 ohms were chosen to broaden the operating bandwidth of the multiplier, but gain was sacrificed. It may be made up with an amplifier operating at the appropriate frequency. (See Figure 31.)

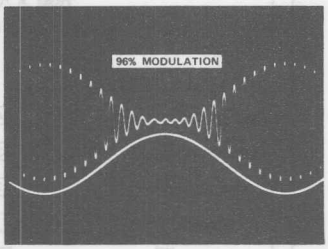
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OPERATION AND APPLICATIONS INFORMATION (continued)

FIGURE 30 – AMPLITUDE MODULATION



(B)



The signal is applied to the unit's Y input. Since the total input range is limited to 1.0 volt p-p, a 2.0-volt swing, a current source of 2.0 mA and an R_Y value of 1.0 kilohm is chosen. This takes best advantage of the dynamic range and insures linear operation in the Y-channel.

Since the X input varies between 0 and +1.0 volt, the current source selected was 1.0 mA and the R_X value chosen was 2.0 kilohms. This also insures linear operation over the X input dynamic range.

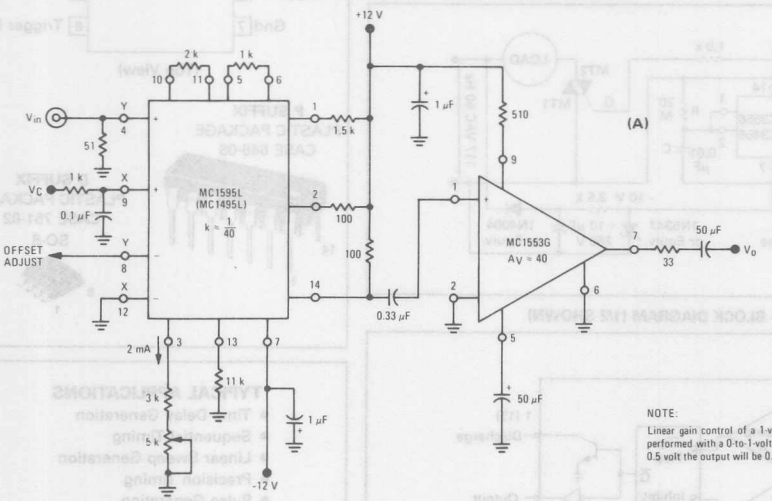
Choosing $R_L = 100$ assures wide-bandwidth operation. Hence, the scale factor for this configuration is

$$K = \frac{R_L}{R_X R_Y I_3} = \frac{100}{(2\text{ k})(1\text{ k})(2 \times 10^{+3})}\ V^{-1} = \frac{1}{40}\ V^{-1}.$$

The 2 in the numerator of the equation is missing in this scale-factor expression because the output is single-ended and ac coupled.

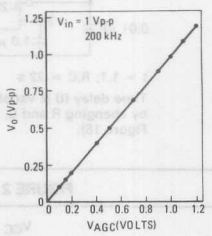
To recover the gain, an MC1552 video amplifier with a gain of 40 is used. An operational amplifier also could have been used with frequency compensation to allow a gain of 40 at 200 kHz. The MC1539 operational amplifier can be tailored for this use; and the MC1520 operational amplifier does it directly.

FIGURE 31 – LINEAR GAIN CONTROL



(A)

(B)



NOTE:
Linear gain control of a 1-volt peak-to-peak signal is performed with a 0-to-1-volt control voltage. If V_C is 0.5 volt the output will be 0.5 volt p-p.

11

ORDERING INFORMATION

Device	Alternate	Temperature Range	Package
MC3456D	—	0°C to +70°C	SO-14
MC3456L	—	0°C to +70°C	Ceramic DIP
MC3456P	NE556A	0°C to +70°C	Plastic DIP
MC3556L	—	−55°C to +125°C	Ceramic DIP
NE556D	—	0°C to +70°C	SO-14

MC3456
MC3556

Specifications and Applications Information

DUAL TIMING CIRCUIT

The MC3556/MC3456 dual timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor per timer. For astable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor per timer. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200 mA or drive MTTL circuits.

- Direct Replacement for NE556/SE556 Timers
- Timing From Microseconds Through Hours
- Operates in Both Astable and Monostable Modes
- Adjustable Duty Cycle
- High Current Output Can Source or Sink 200 mA
- Output Can Drive MTTL
- Temperature Stability of 0.005% per °C
- Normally "On" or Normally "Off" Output
- Dual Version of the Popular MC1455 Timer

FIGURE 1 — 22-SECOND SOLID-STATE TIME DELAY RELAY CIRCUIT

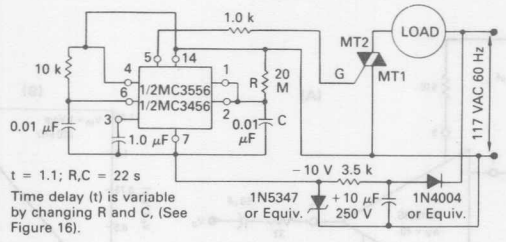
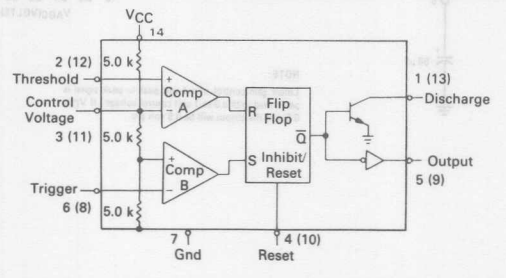


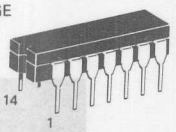
FIGURE 2 — BLOCK DIAGRAM (1/2 SHOWN)

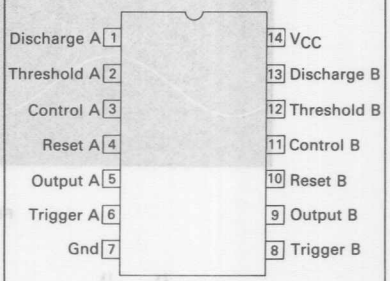


DUAL TIMING CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT

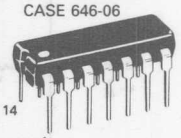
L SUFFIX
CERAMIC PACKAGE
CASE 632-08





(Top View)

P SUFFIX
PLASTIC PACKAGE
CASE 646-06



D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SO-8



TYPICAL APPLICATIONS

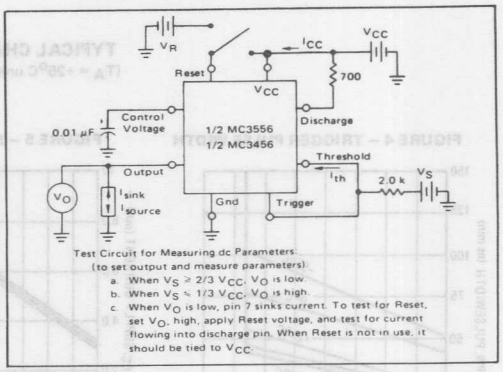
- Time Delay Generation
- Sequential Timing
- Linear Sweep Generation
- Precision Timing
- Pulse Generation
- Pulse Shaping
- Missing Pulse Detection
- Pulse Width Modulation
- Pulse Position Modulation

11

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+18	Vdc
Discharge Current	I_{dis}	200	mA
Power Dissipation (Package Limitation)	P_D		
Ceramic Dual-In-Line Package		1000	mW
Derate above T_A = +25°C		6.6	mW/°C
Plastic Dual In-Line Package		625	mW
Derate above T_A = +25°C		5.0	mW/°C
Operating Ambient Temperature Range MC3556	T_A	-55 to +125	°C
MC3456		0 to +70	
Storage Temperature Range	T_{stg}	-65 to +150	°C

FIGURE 3 – GENERAL TEST CIRCUIT



Test Circuit for Measuring dc Parameters
(to set output and measure parameters)
a. When $V_S \geq 2/3\ V_{CC}$, V_O is low.
b. When $V_S \leq 1/3\ V_{CC}$, V_O is high.
c. When V_O is low, pin 7 sinks current. To test for Reset, set V_O high, apply Reset voltage, and test for current flowing into discharge pin. When Reset is not in use, it should be tied to V_{CC}.

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = +5.0 V to +15 V unless otherwise noted.)

Characteristics	Symbol	MC3556 Min	MC3556 Typ	MC3556 Max	MC3456 Min	MC3456 Typ	MC3456 Max	Unit
Supply Voltage	V_{CC}	4.5	–	18	4.5	–	16	V
Supply Current	I_{CC}							mA
V_{CC} = 5.0 V, R_L = ∞		–	6.0	10	–	6.0	12	
V_{CC} = 15 V, R_L = ∞		–	20	24	–	20	30	
Low State, (Note 1)								
Timing Error (Note 2)								
Monostable Mode								
R_A = 2.0 kΩ to 100 kΩ								
Initial Accuracy C = 0.1 µF		–	0.5	1.5	–	0.75	–	%
Drift with Temperature		–	30	100	–	50	–	PPM/°C
Drift with Supply Voltage		–	0.15	0.2	–	0.1	–	%/Volt
Astable Mode								
R_A = R_B = 2.0 kΩ to 100 kΩ								
C = 0.01 µF								
Initial Accuracy		–	1.5	–	–	2.25	–	%
Drift with Temperature		–	90	–	–	150	–	PPM/°C
Drift with Supply Voltage		–	0.15	–	–	0.3	–	%/Volt
Threshold Voltage	V_{th}	–	2/3	–	–	2/3	–	xV_{CC}
Trigger Voltage	V_T							V
V_{CC} = 15 V		4.8	5.0	5.2	–	5.0	–	
V_{CC} = 5.0 V		1.45	1.67	1.9	–	1.67	–	
Trigger Current	I_T	–	0.5	–	–	0.5	–	µA
Reset Voltage	V_R	0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current	I_R	–	0.1	–	–	0.1	–	mA
Threshold Current (Note 3)	I_{th}	–	0.03	0.1	–	0.03	0.1	µA
Control Voltage Level	V_{CL}							V
V_{CC} = 15 V		9.6	10	10.4	9.0	10	11	
V_{CC} = 5.0 V		2.9	3.33	3.8	2.6	3.33	4.0	
Output Voltage Low	V_{OL}							V
(V_{CC} = 15 V)								
I_{sink} = 10 mA		–	0.1	0.15	–	0.1	0.25	
I_{sink} = 50 mA		–	0.4	0.5	–	0.4	0.75	
I_{sink} = 100 mA		–	2.0	2.25	–	2.0	2.75	
I_{sink} = 200 mA		–	2.5	–	–	2.5	–	
(V_{CC} = 5.0 V)								
I_{sink} = 8.0 mA		–	0.1	0.25	–	–	–	
I_{sink} = 5.0 mA		–	–	–	–	0.25	0.35	
Output Voltage High	V_{OH}							V
(I_{source} = 200 mA)								
V_{CC} = 15 V		–	12.5	–	–	12.5	–	
(I_{source} = 100 mA)								
V_{CC} = 15 V		13	13.3	–	12.75	13.3	–	
V_{CC} = 5.0 V		3.0	3.3	–	2.75	3.3	–	
Toggle Rate (Figures 17, 19)								
R_A = 3.3 kΩ, R_B = 6.8 kΩ, C = 0.003 µF	–	–	100	–	–	100	–	kHz
Discharge Leakage Current	I_{dis}	–	20	100	–	20	100	nA
Rise Time of Output	t_{OLH}	–	100	–	–	100	–	ns
Fall Time of Output	t_{OHL}	–	100	–	–	100	–	ns
Matching Characteristics Between Sections (Monostable)								
Initial Timing Accuracy		–	0.5	1.0	–	1.0	2.0	%
Timing Drift with Temperature		–	±10	–	–	±10	–	ppm/°C
Drift with Supply Voltage		–	0.1	0.2	–	0.2	0.5	%/V

NOTES: 1. Supply current is typically 1.0 mA less for each output which is high.
2. Tested at V_{CC} = 5.0 V and V_{CC} = 15 V.
3. This will determine the maximum value of R_A + R_B for 15 V operation. The maximum total R = 20 megohms.

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(T_A = +25°C unless otherwise noted.)

FIGURE 4 – TRIGGER PULSE WIDTH

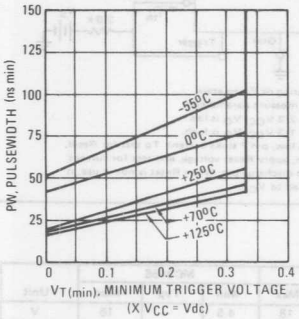


FIGURE 5 – SUPPLY CURRENT

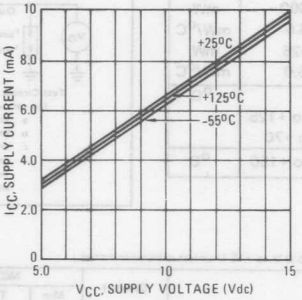


FIGURE 6 – HIGH OUTPUT VOLTAGE

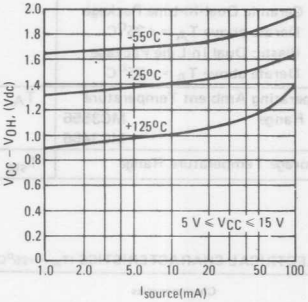


FIGURE 7 – LOW OUTPUT VOLTAGE @ V_{CC} = 5.0 Vdc

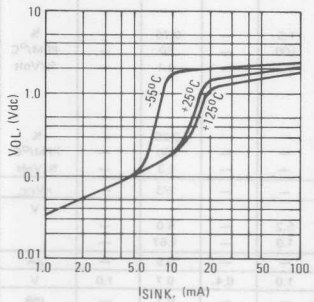


FIGURE 8 – LOW OUTPUT VOLTAGE @ V_{CC} = 10 Vdc

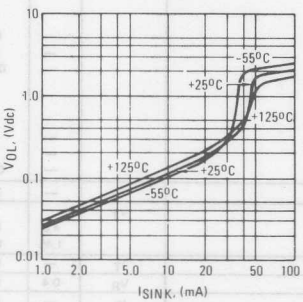


FIGURE 9 – LOW OUTPUT VOLTAGE @ V_{CC} = 15 Vdc

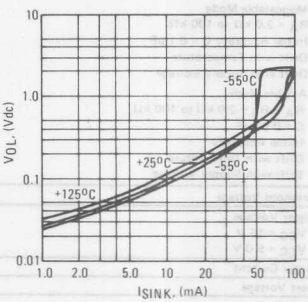


FIGURE 10 – DELAY TIME versus SUPPLY VOLTAGE

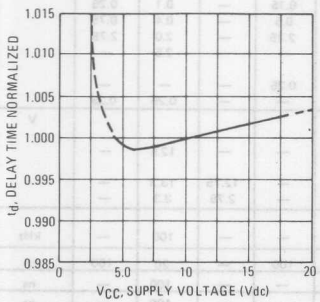


FIGURE 11 – DELAY TIME versus TEMPERATURE

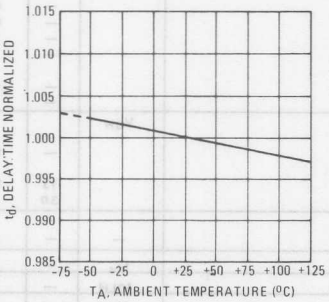
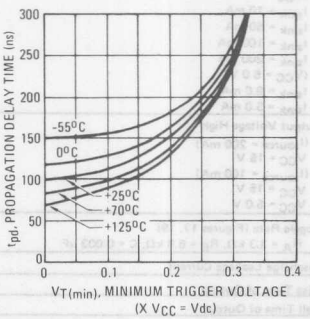
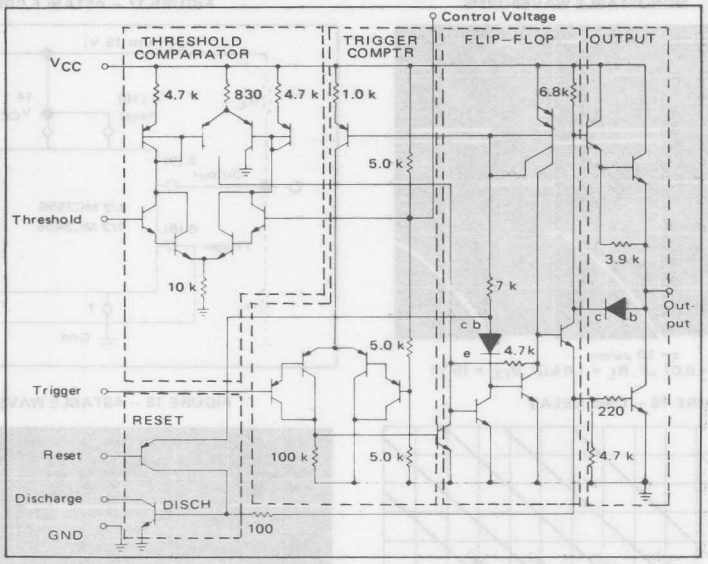


FIGURE 12 – PROPAGATION DELAY versus TRIGGER VOLTAGE



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FIGURE 13 – 1/2 REPRESENTATIVE CIRCUIT SCHEMATIC



GENERAL OPERATION

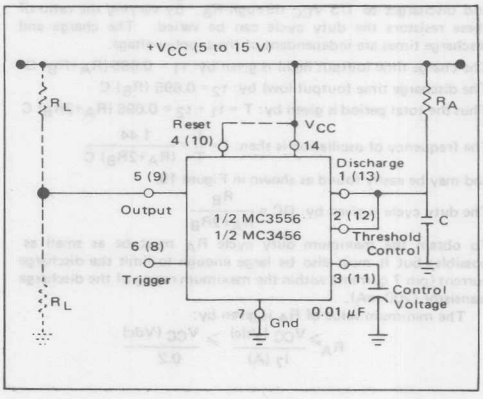
The MC3556 is a dual timing circuit which uses as its timing elements an external resistor – capacitor network. It can be used in both the monostable (one-shot) and astable modes with frequency and duty cycle controlled by the capacitor and resistor values. While the timing is dependent upon the external passive components, the monolithic circuit provides the starting circuit, voltage comparison and other functions needed for a complete timing circuit. Internal to the integrated circuit are two comparators, one for the input signal and the other for capacitor voltage; also a flip-flop and digital output are included. The comparator reference voltages are always a fixed ratio of the supply voltage thus providing output timing independent of supply voltage.

Monostable Mode

In the monostable mode, a capacitor and a single resistor are used for the timing network. Both the threshold terminal and the discharge transistor terminal are connected together in this mode, refer to circuit Figure 14. When the input voltage to the trigger comparator falls below 1/3 V_{CC} the comparator output triggers the flip-flop so that it's output sets low. This turns the capacitor discharge transistor "off" and drives the digital output to the high state. This condition allows the capacitor to charge at an exponential rate which is set by the RC time constant. When the capacitor voltage reaches 2/3 V_{CC} the threshold comparator resets the flip-flop. This action discharges the timing capacitor and returns the digital output to the low state. Once the flip-flop has been triggered by an input signal, it cannot be retriggered until the present timing period has been completed. The time that the output is high is given by the equation $t = 1.1\ R_A\ C$. Various combinations of R and C and their associated times are shown in Figure 16. The trigger pulse width must be less than the timing period.

A reset pin is provided to discharge the capacitor thus interrupting the timing cycle. As long as the reset pin is low, the capacitor discharge transistor is turned "on" and prevents the capacitor from charging. While the reset voltage is applied the digital output will remain the same. The reset pin should be tied to the supply voltage when not in use.

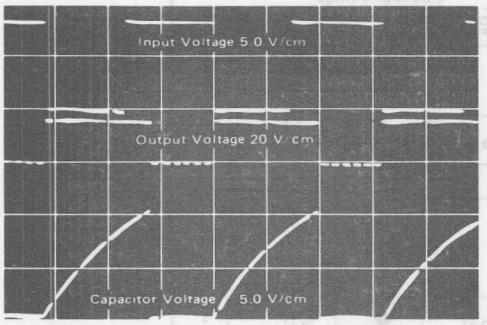
FIGURE 14 – MONOSTABLE CIRCUIT



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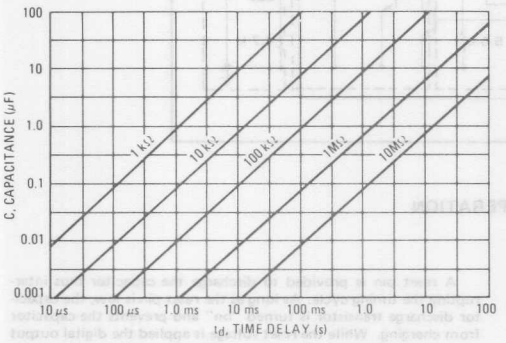
GENERAL OPERATION (continued)

FIGURE 15 – MONOSTABLE WAVEFORMS



t = 50 μs/cm
(R_A = 10 kΩ, C = 0.01 μF, R_L = 1.0 kΩ, V_{CC} = 15 V)

FIGURE 16 – TIME DELAY



Astable Mode

In the astable mode the timer is connected so that it will retrigger itself and cause the capacitor voltage to oscillate between 1/3 V_{CC} and 2/3 V_{CC}. See Figure 17.

The external capacitor charges to 2/3 V_{CC} through R_A and R_B and discharges to 1/3 V_{CC} through R_B. By varying the ratio of these resistors the duty cycle can be varied. The charge and discharge times are independent of the supply voltage.

The charge time (output high) is given by: $t_1 = 0.695 (R_A+R_B) C$

The discharge time (output low) by: $t_2 = 0.695 (R_B) C$

Thus the total period is given by: $T = t_1 + t_2 = 0.695 (R_A+2R_B) C$

The frequency of oscillation is then: $f = \frac{1}{T} = \frac{1.44}{(R_A+2R_B) C}$

and may be easily found as shown in Figure 19.

The duty cycle is given by: $DC = \frac{R_B}{R_A+2R_B}$

To obtain the maximum duty cycle R_A must be as small as possible; but it must also be large enough to limit the discharge current (pin 7 current) within the maximum rating of the discharge transistor (200 mA).

The minimum value of R_A is given by:

$$R_A \geq \frac{V_{CC}\ (Vdc)}{I_7\ (A)} \geq \frac{V_{CC}\ (Vdc)}{0.2}$$

FIGURE 17 – ASTABLE CIRCUIT

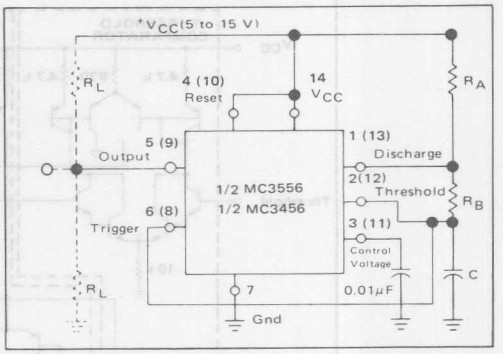
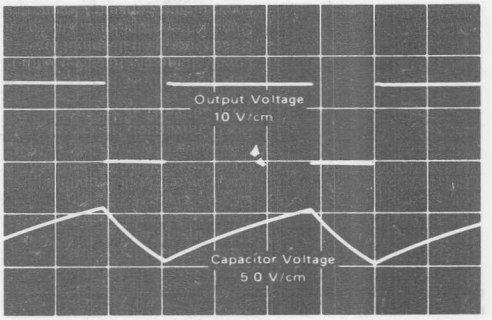
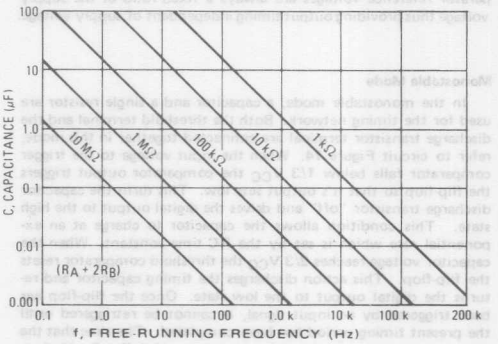


FIGURE 18 – ASTABLE WAVEFORMS



t = 20 μs/cm
(R_A = 5.1 kΩ, C = 0.01 μF, R_L = 1.0 kΩ;
R_B = 3.9 kΩ, V_{CC} = 15 V)

FIGURE 19 – FREE-RUNNING FREQUENCY



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APPLICATIONS INFORMATION

TONE BURST GENERATOR

For a tone burst generator the first timer is used as a monostable and determines the tone duration when triggered by a positive pulse at Pin 6. The second timer is enabled by the high output of the monostable. It is connected as an astable and determines the frequency of the tone.

DUAL ASTABLE MULTIVIBRATOR

This dual astable multivibrator provides versatility not available with single timer circuits. The duty cycle can be adjusted from 5% to 95%. The two outputs provide two phase clock signals often required in digital systems. It can also be inhibited by use of either reset terminal.

FIGURE 20 – TONE BURST GENERATOR

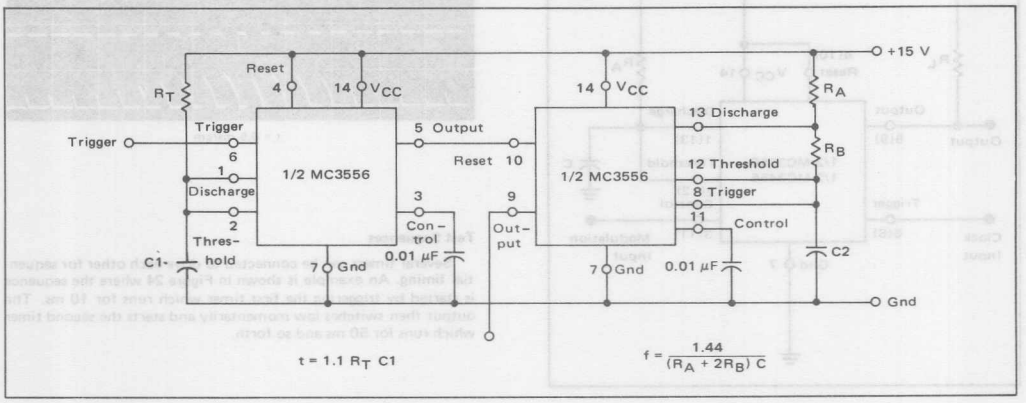
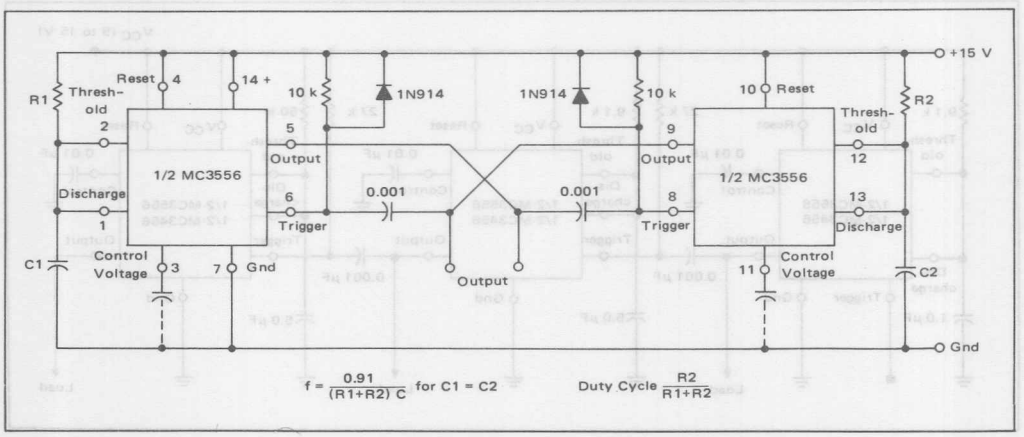


FIGURE 21 – DUAL ASTABLE MULTIVIBRATOR



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Pulse Width Modulation

If the timer is triggered with a continuous pulse train in the monostable mode of operation, the charge time of the capacitor can be varied by changing the control voltage at pin 3. In this manner, the output pulse width can be modulated by applying a modulating signal that controls the threshold voltage.

FIGURE 22

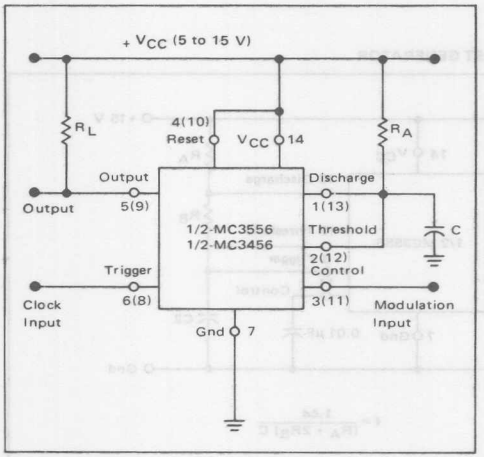
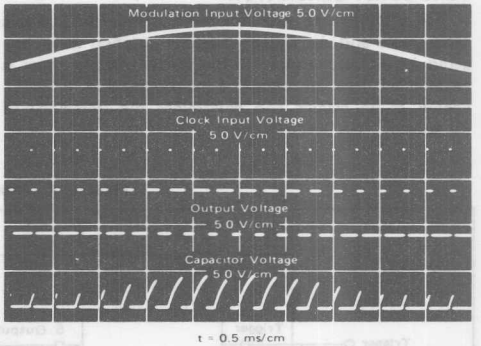


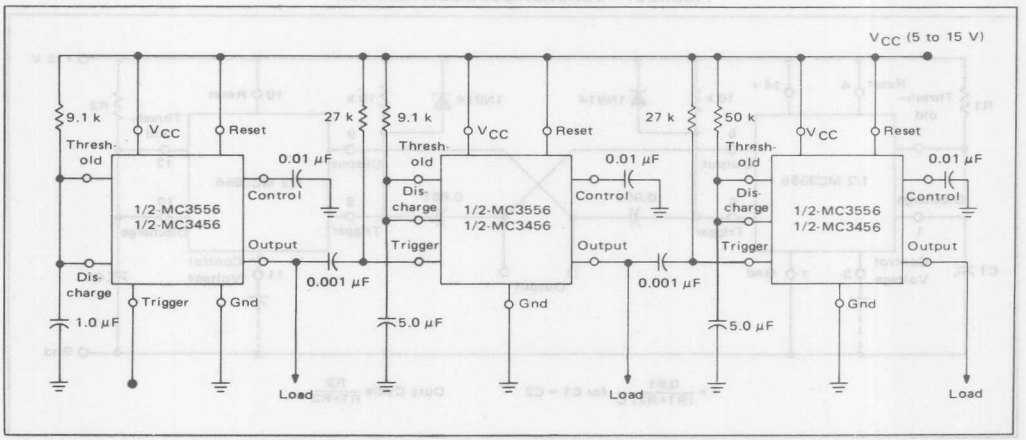
FIGURE 23 – PULSE WIDTH MODULATION WAVEFORMS
(R_A = 10 kΩ, C = 0.02 μF, V_{CC} = 15 V)



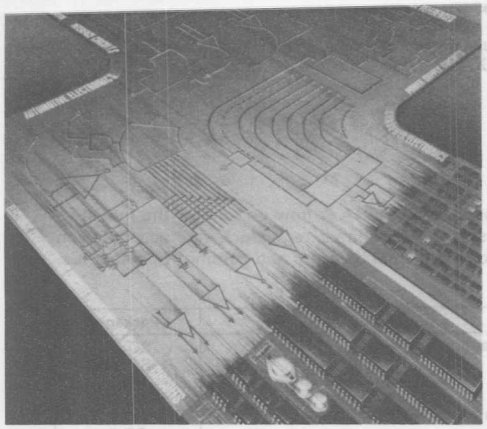
Test Sequences

Several timers can be connected to drive each other for sequential timing. An example is shown in Figure 24 where the sequence is started by triggering the first timer which runs for 10 ms. The output then switches low momentarily and starts the second timer which runs for 50 ms and so forth.

FIGURE 24



11



In Brief . . .

Surface Mount Technology is now being utilized to offer answers to many problems that have been created in the use of insertion technology.

Limitations have been reached with insertion packages and PC board technology. Surface Mount Technology offers the opportunity to continue to advance the State-of-the-Art designs that cannot be accomplished with Insertion Technology.

Surface Mount Packages allow more optimum device performance with the smaller Surface Mount configuration. Internal lead lengths, parasitic capacitance and inductance that placed limitations on chip performance has been reduced.

The lower profile of Surface Mount Packages allows more boards to be utilized in a given amount of space. They are stacked closer together and utilize less total volume than insertion populated PC boards.

Printed circuit costs are lowered with the reduction of the number of board layers required. The elimination or reduction of the number of plated through holes in the board, contribute significantly to lower PC board prices.

Surface Mount assembly does not require the preparation of components that are common on insertion technology lines. Surface Mount components are sent directly to the assembly line, eliminating an intermediate step.

Automatic placement equipment is available that can place Surface Mount components at the rate of a few thousand per hour to hundreds of thousands of components per hour.

Surface Mount Technology is cost effective, allowing the manufacturer the opportunity to produce smaller units and offer increased functions with the same size product.

Linear and Interface Devices. 12-2

Tape and Reel 12-5

Surface Mount Technology

12

Surface Mount Technology

Linear and Interface Devices 12-2
Tape and Reel
Standard Bipolar Logic, Bipolar Analog and
MOS Integrated Circuits 12-5

Linear and Interface

All the major bipolar analog families are now represented in surface mount packaging. Standard SOIC and PLCC packages are augmented by SOP-8 and DPAK for Linear regulators. In addition, tape and reel shipping to the updated EIA-481A is now on line for the industry's largest array of op-amps, regulators, interface, data conversion, consumer, telecom and automotive Linear ICs.

Device	Function	Package
DAC-08CD,ED	High-Speed 8-Bit Multiplying D-to-A Converter	SO-16
LF347D	Quad BIFET Operational Amplifiers	SO-14
LF351D	Single BIFET Operational Amplifier	SO-8
LF353D	Dual BIFET Operational Amplifiers	SO-8
LF412CD	Dual BIFET High Power Operational Amplifiers	SO-8
LF441CD	Single BIFET Low Power Operational Amplifier	SO-8
LF442CD	Dual BIFET Low Power Operational Amplifiers	SO-8
LF444CD	Quad BIFET Low Power Operational Amplifiers	SO-14
LM201AD	General Purpose Adjustable Operational Amplifier	SO-8
LM208D,AD	Precision Operational Amplifier	SO-8
LM211D	High Performance Voltage Comparator	SO-8
LM224D	Quad Low Power Operational Amplifiers	SO-14
LM239D,AD	Quad Single Supply Comparators	SO-14
LM258D	Dual Low Power Operational Amplifiers	SO-8
LM293D	Dual Comparators	SO-8
LM301AD	General Purpose Adjustable Operational Amplifier	SO-8
LM308D,AD	Precision Operational Amplifier	SO-8
LM311D	High Performance Voltage Comparator	SO-8
LM317LD	Positive Adjustable 100 mA Voltage Regulator	SOP-8
LM324D,AD	Quad Low Power Operational Amplifiers	SO-14
LM339D,AD	Quad Single Supply Comparators	SO-14
LM348D	Quad MC1741 Operational Amplifiers	SO-14
LM358D	Dual Low Power Operational Amplifiers	SO-8
LM385D-1.2	Micropower Voltage Reference Diodes	SO-8
LM385D-2.5	Micropower Voltage Reference Diodes	SO-8
LM393D	Dual Comparators	SO-8
LM833D	Dual Audio Amplifiers	SO-8
LM2901D	Quad Single Supply Comparators	SO-14
LM2902D	Quad Low Power Operational Amplifiers	SO-14
LM2903D	Dual Comparators	SO-8
LM2904D	Dual Low Power Operational Amplifiers	SO-8
LM2931AD-5.0,D-5.0	Low Dropout Voltage Regulator	SOP-8
LM2931CD*	Adjustable Low Dropout Voltage Regulator	SOP-8
LM3900D	Quad Single Supply Operational Amplifiers	SO-14
MC1377DW*	Color Television RGB to PAL/NTSC Encoder	SO-20
MC1378FN	Video Overlay Synchronizer	PLCC-44
MC1403D	Precision Low Voltage Reference	SO-8
MC1413D	Peripheral Driver Array	SO-16
MC1436D,CD	High Voltage Operational Amplifier	SO-8
MC1455D	Timing Circuit	SO-8
MC1458D,CD	Dual Operational Amplifiers	SO-8
MC1458SD	High Slew Rate Dual Operational Amplifiers	SO-8
MC1488D	Quad EIA-232C Drivers	SO-14
MC1489D	Quad EIA-232C Receivers	SO-14
MC1496D	Balanced Modulator-Demodulator	SO-14
MC1723CD	Adjustable Positive Or Negative Voltage Regulator	SO-14
MC1733CD	Differential Video Amplifier	SO-14
MC1741CD	General Purpose Operational Amplifier	SO-8
MC1741SCD	High Slew Rate Operational Amplifier	SO-8
MC1747CD	Dual MC1741 Operational Amplifiers	SO-14
MC1776CD	Programmable Operational Amplifier	SO-8
MC26LS31D	Quad EIA-422/3 Drivers	SO-16

*To Be Introduced.

LINEAR AND INTERFACE (continued)

Device	Function	Package
MC26LS32D	Quad EIA-422 Receivers	SO-16
MC2831AD	FM Transmitter	SO-16
MC3346D	General Purpose Transistor Array	SO-14
MC3356FN	FSK Receiver	PLCC-20
MC3357D	Low Power FM IF Amplifier	SO-16
MC3359DW	Low Power Narrowband FM IF Amplifier	SO-20
MC3361D	Low Voltage Narrowband FM IF Amplifier	SO-16
MC3362DW	Dual Conversion Receivers	SO-28
MC3363DW*	Dual Conversion Receivers	SO-28
MC3367DW	Low Voltage VHF Receiver	SO-28
MC3371D*	Low Voltage FM Receiver with RSSI	SO-16
MC3401D	Quad Operational Amplifiers	SO-14
MC3403D	Quad Differential-Input Operational Amplifiers	SO-14
MC3423D	Overvoltage Sensing Circuit	SO-8
MC3448AD	Quad GPIB Transceivers	SO-16
MC3450D	Quad Line Receivers	SO-16
MC3452D	Quad Line Receivers	SO-16
MC3458D	Dual Low Power Operational Amplifiers	SO-8
MC3486D	Quad EIA-422/3 Receivers	SO-16
MC3487D	Quad EIA-422 Drivers	SO-16
MC4558CD	Dual High Frequency Operational Amplifiers	SO-8
MC4741CD	Quad MC1741 Operational Amplifiers	SO-14
MC78L05ACD	Positive Voltage Regulator, 5 V, 100 mA	SOP-8
MC78L08ACD	Positive Voltage Regulator, 8 V, 100 mA	SOP-8
MC78L12ACD	Positive Voltage Regulator, 12 V, 100 mA	SOP-8
MC78L15ACD	Positive Voltage Regulator, 15 V, 100 mA	SOP-8
MC78M05CDT*	Positive Voltage Regulator, 5 V, 500 mA	DPAK
MC78M12CDT*	Positive Voltage Regulator, 12 V, 500 mA	DPAK
MC78M15CDT*	Positive Voltage Regulator, 15 V, 500 mA	DPAK
MC79L05ACD	3-Terminal Negative Fixed Voltage Regulator, −5 V, 100 mA	SOP-8
MC79L12ACD	3-Terminal Negative Fixed Voltage Regulator, −12 V, 100 mA	SOP-8
MC79L15ACD	3-Terminal Negative Fixed Voltage Regulator, −15 V, 100 mA	SOP-8
MC79M05CDT*	3-Terminal Negative Fixed Voltage Regulator, −5 V, 500 mA	DPAK
MC79M12CDT*	3-Terminal Negative Fixed Voltage Regulator, −12 V, 500 mA	DPAK
MC79M15CDT*	3-Terminal Negative Fixed Voltage Regulator, −15 V, 500 mA	DPAK
MC13022DW*	Medium Voltage AM Stereo C-QUAM Decoder	SO-28
MC13024DW*	Low Voltage C-QUAM Receiver	SO-24
MC13041DW*	AM Receiver Subsystem	SO-20
MC13055D	VHF LAN Receiver — FSK	SO-16
MC13060D	1 Watt Audio Amp	SOP-8
MC33077D	Dual, Low Noise High Frequency Operational Amplifiers	SO-8
MC33078D	Dual Audio, Low Noise Operational Amplifiers	SO-8
MC33079D	Low Power, Single Supply Operational Amplifier	SO-14
MC33171D	Single, Low Power, Single Supply Operational Amplifier	SO-8
MC33172D*	Dual, Low Power, Single Supply Operational Amplifiers	SO-8
MC33174D*	Quad, Low Power, Single Supply Operational Amplifiers	SO-14
MC33282D*	Dual Precision Low Input JFET Operational Amplifiers	SO-14
MC33284D*	Quad Precision JFET Operational Amplifiers (Trim-in-the-Package)	SO-14
MC34001D,AD,BD	Single JFET Input Operational Amplifier	SO-8
MC34002D,AD,BD	Dual JFET Input Operational Amplifiers	SO-8
MC34004D,BD	Quad JFET Input Operational Amplifiers	SO-14
MC34011AFN	Electronic Telephone Circuit	PLCC-44
MC34012-1D	Telephone Tone Ringer	SO-8
MC34012-2D	Telephone Tone Ringer	SO-8
MC34012-3D	Telephone Tone Ringer	SO-8
MC34013AFN	Speech Network and Tone Dialer	PLCC-28
MC34014FN	Telephone Speech Network with Dialer Interface	PLCC-20
MC34017-1D	Telephone Tone Dialer	SO-8
MC34017-2D	Telephone Tone Dialer	SO-8
MC34017-3D	Telephone Tone Dialer	SO-8
MC34018DW	Voice Switched Speakerphone Circuit	SO-28

*To Be Introduced.

Device	Function	Package
MC34018FN	Voice Switched Speakerphone Circuit	PLCC-28
MC34060AD*	Switchmode Pulse Width Modulation Control Circuit	SO-14
MC34063AD	Precision DC-to-DC Converter Control Circuit	SO-8
MC34071D	Single, High Speed, Single Supply Operational Amplifier	SO-8
MC34072D*	Dual, High Speed, Single Supply Operational Amplifiers	SO-8
MC34074D*	Quad, High Performance, Single Supply Operational Amplifiers	SO-14
MC34080D	High Speed Decompensated ($A_{VCL} \geq 2$) JFET Input Operational Amplifier	SO-8
MC34081D	High Speed JFET Input Operational Amplifier	SO-8
MC34114DW	Speech Network II	SO-18
MC34118DW	Speakerphone II	SO-28
MC34119D	Telephone Speaker Amplifier	SO-8
MC34129D	Power Supply Controller	SO-14
MC34181D	Single, Low Power, High Speed JFET Operational Amplifier	SO-8
MC34182D	Dual, Low Power, High Speed JFET Operational Amplifiers	SO-8
MC34184D	Quad, Low Power, High Speed JFET Operational Amplifiers	SO-14
MC44301DW*†	High Performance Video IF	SO-28
NE592D	Video Amplifier	SO-14
TL061CD	Single BIFET Low Power Operational Amplifier	SO-8
TL062CD	Dual BIFET Low Power Operational Amplifiers	SO-8
TL064CD	Quad BIFET Low Power Operational Amplifiers	SO-14
TL071CD,ACD,BCD	Single, Low Noise JFET Input Operational Amplifier	SO-8
TL072CD,ACD,BCD	Dual, Low Noise JFET Input Operational Amplifiers	SO-8
TL074CD,ACD,BCD	Quad, Low Noise JFET Input Operational Amplifiers	SO-14
TL081CD,ACD,BCD	Single, JFET Input Operational Amplifier	SO-8
TL082CD,ACD,BCD	Dual, JFET Input Operational Amplifiers	SO-8
TL084CD,ACD,BCD*	Quad, JFET Input Operational Amplifiers	SO-14
TL431CD	Programmable Precision Reference	SOP-8
TYA1350D	IF Amplifier (M1350D)	SO-8
UAA1041D	Automotive Direction Indicator	SO-8
UC2842AD	Off-Line Current Mode PWM Controller	SO-14
UC2843AD	Current Mode PWM Controller	SO-14
UC3842AD	Off-Line Current Mode PWM Controller	SO-14
UC3843AD	Current Mode PWM Controller	SO-14

*To Be Introduced.
†Formerly MC13011DW

12

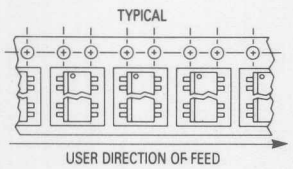
Tape and Reel

Standard Bipolar Logic, Bipolar Analog and MOS Integrated Circuits

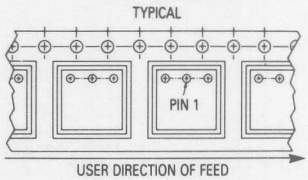
Motorola has now added the convenience of Tape and Reel packaging for our growing family of standard Integrated Circuit products. Two reel sizes are available, for all but the largest types, to support the requirements of both first and second generation pick-and-place equipment. The packaging fully conforms to the latest EIA-481A specification. The anti-static embossed tape provides a secure cavity, sealed with a peel-back cover tape.

Mechanical Polarization

SOIC DEVICES



PLCC DEVICES



Package	Tape Width (mm)	Device per Reel	Reel Size* (inch)	Tape & Reel Lot Size(1) (Min)	Device Suffix
SO-8, SOP-8	12 12	750 2,500	7 13	5,000 5,000	R1 R2
SO-14	16 16	750 2,500	7 13	5,000 5,000	R1 R2
SO-16	16 16	750 2,500	7 13	5,000 5,000	R1 R2
SO-16L (WIDE)	16 16	250 1,000	7 13	5,000 5,000	R1 R2
SO-20L (WIDE)	24 24	250 1,000	7 13	5,000 5,000	R1 R2
SO-24L (WIDE)	24 24	250 1,000	7 13	5,000 5,000	R1 R2
SO-28L (WIDE)	24 24	200 1,000	7 13	3,000 3,000	R1 R2
PLCC-20	16 16	200 1,000	7 13	3,000 3,000	R1 R2
PLCC-28	24 24	200 500	7 13	2,400 2,500	R1 R2
PLCC-44	32 32	200 500	7 13	2,000 2,000	R1 R2
PLCC-52 PLCC-68 PLCC-84	32 44 44	500 250 250	13 13 13	2,000 2,000 2,000	R2 R2 R2
TO-226AA(2)	18	1800	13	10,000	RA, RB or RP only

Notes: 1. Minimum lot size information applies to OEM customers. Distributors may break lots or reels at their option, however broken reels may not be returned.
2. Integrated Circuits in TO-226AA packages are available in Styles A and B only, with optional "Ammo Pack" (Suffix RP).

For ordering information please contact your local Motorola Semiconductor Sales Office.
Distribution minimum order quantity is 1 reel.
*Reel Size: 7"/178 mm, 13"/330 mm.

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Tape and Reel

Standard Bipolar Logic, Bipolar Analog and MOS Integrated Circuits

Motorola has now added the convenience of Tape and Reel packaging for our growing family of standard Integrated Circuits. Two reel sizes are available, for all but the largest types, to support the requirements of both first and second generation pick-and-place equipment. The packaging fully conforms to the latest EIA-481A specification. The anti-static embossed tape provides a secure cavity, sealed with a peel-back cover tape.

Mechanical Polarization

SOIC DEVICES

PLCC DEVICES

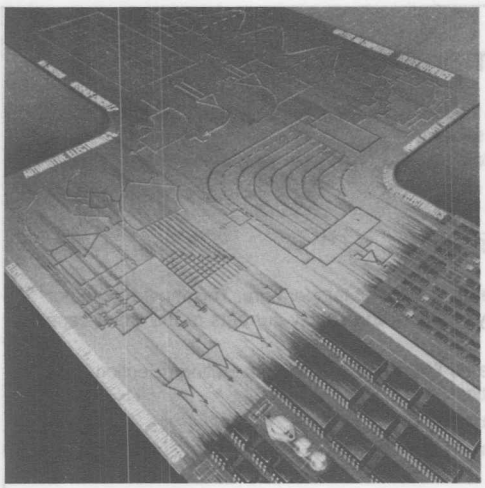
Package	Tape Width (mm)	Device per Reel	Reel Size* (Inch)	Tape & Reel Loc Size(1) (Min)	Device Suffix
SO-8, SOP-8	12 12	750 2,500	7 13	5,000 5,000	R1 R2
SO-14	16 16	750 2,500	7 13	5,000 5,000	R1 R2
SO-16	16 16	750 2,500	7 13	5,000 5,000	R1 R2
SO-16L (WIDE)	16 16	200 1,000	7 13	5,000 5,000	R1 R2
SO-20L (WIDE)	24 24	250 1,000	7 13	5,000 5,000	R1 R2
SO-24L (WIDE)	24 24	200 1,000	7 13	5,000 5,000	R1 R2
SO-28L (WIDE)	24 24	200 1,000	7 13	3,000 3,000	R1 R2
PLCC-20	16 16	200 1,000	7 13	3,000 3,000	R1 R2
PLCC-28	24 24	200 500	7 13	2,400 2,500	R1 R2
PLCC-44	32 32	200 500	7 13	2,000 2,000	R1 R2
PLCC-52 PLCC-68 PLCC-84	32 44 44	200 250 250	13 13 13	2,000 2,000 2,000	R2 R2 R2
TO-226AA(2)	16	1000	13	10,000	RA, RB or RP only

Notes: 1. Minimum lot size information applies to OEM customers. Distributors may break lots or reels at their option, however broken reels may not be returned.

2. Integrated Circuits in TO-226AA packages are available in Styles A and B only, with optional "Ammo Pack" (Suffix RP). For ordering information please contact your local Motorola Semiconductor Sales Office.

Distributors minimum order quantity is 1 reel.

*Reel Size: 7"/178 mm, 13"/330 mm.



Packaging Information

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The packaging availability for each device type is indicated on the individual data sheets and the Selector Guide. All of the outline dimensions for the packages are given in this section.

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}}$$

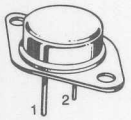
where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

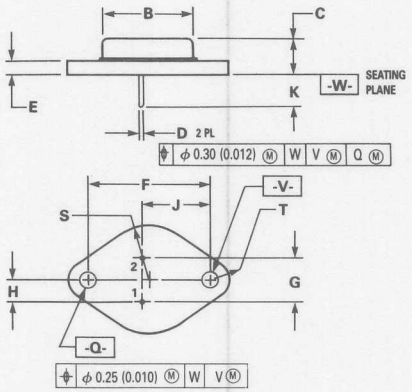
$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section. See individual data sheets for $T_{J(max)}$ information.

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient

K SUFFIX
CASE 1-03
Metal Package
$R_{\theta JA}$ = 45° C/W(Typ)

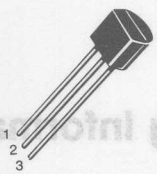


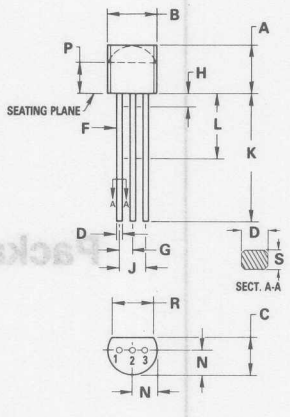


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	—	22.23	—	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	—	3.43	—	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	7.92	—	0.312	—
Q	3.84	4.09	0.151	0.161
S	—	13.34	—	0.525
T	—	4.78	—	0.188
V	3.84	4.09	0.151	0.161

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

LP, P, Z SUFFIX
CASE 29-04
Plastic Package
$R_{\theta JA}$ = 200° C/W





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.45	5.20	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.55	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.15	1.39	0.045	0.055
H	—	2.54	—	0.100
J	2.42	2.66	0.095	0.105
K	12.70	—	0.500	—
L	6.35	—	0.250	—
N	2.04	2.66	0.080	0.105
P	2.93	—	0.115	—
R	3.43	—	0.135	—
S	0.39	0.50	0.015	0.020

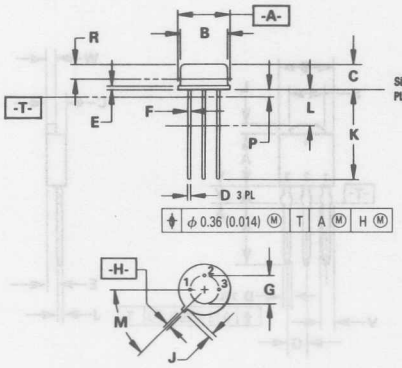
NOTES:
1. CONTOUR OF PACKAGE BEYOND ZONE "P" IS UNCONTROLLED.
2. DIM "F" APPLIES BETWEEN "H" AND "L". DIM "D" & "S" APPLIES BETWEEN "L" & 12.70mm (0.5") FROM SEATING PLANE. LEAD DIM IS UNCONTROLLED IN "H" & BEYOND 12.70mm (0.5") FROM SEATING PLANE.
3. CONTROLLING DIM: INCH.

13

Packaging Information

G, H SUFFIX
CASE 79-05
Metal Package
$R_{\theta JA}$ = 185° C/W(Typ)

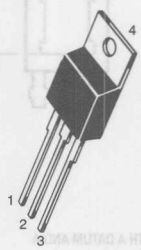


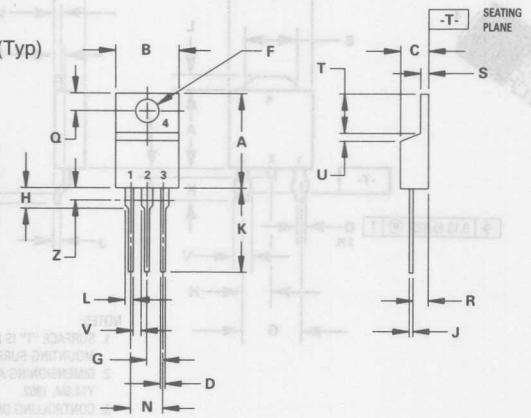


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION J MEASURED FROM DIMENSION A MAXIMUM.
4. DIMENSION B SHALL NOT VARY MORE THAN 0.25 (0.010) IN ZONE R. THIS ZONE CONTROLLED FOR AUTOMATIC HANDLING.
5. DIMENSION F APPLIES BETWEEN DIMENSION P AND L. DIMENSION D APPLIES BETWEEN DIMENSION L AND K MINIMUM. LEAD DIAMETER IS UNCONTROLLED IN DIMENSION P AND BEYOND DIMENSION K MINIMUM.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.02	9.29	0.355	0.366
B	8.01	8.50	0.315	0.335
C	4.20	4.57	0.165	0.180
D	0.44	0.53	0.017	0.021
E	0.44	0.88	0.017	0.035
F	0.41	0.48	0.016	0.019
G	5.08 BSC		0.200 BSC	
H	0.72	0.86	0.028	0.034
J	0.74	1.01	0.029	0.040
K	12.70	19.05	0.500	0.750
L	6.35	—	0.250	—
M	45° BSC		45° BSC	
P	—	1.27	—	0.050
R	2.54	—	0.100	—

KC, T SUFFIX
CASE 221A-04
Plastic Package
$R_{\theta JA}$ = 65° C/W(Typ)

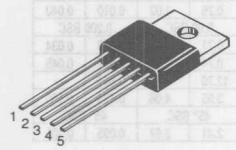


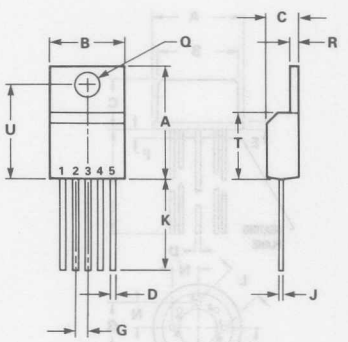


	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

T SUFFIX
CASE 314D-01
Plastic Package
$R_{\theta JA}$ = 65° C/W(Typ)



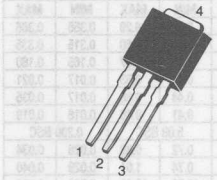


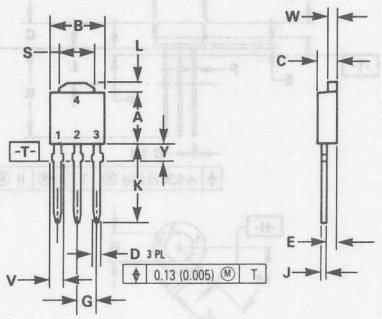
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.49	15.87	0.610	0.625
B	9.91	10.41	0.390	0.410
C	4.32	4.57	0.170	0.180
D	0.51	1.01	0.020	0.040
G	1.45	1.96	0.057	0.077
J	0.38	0.63	0.015	0.025
K	12.70	—	0.500	—
Q	3.53	3.73	0.139	0.147
R	0.89	1.39	0.035	0.055
T	9.02	9.39	0.355	0.370
U	12.70	13.69	0.500	0.539

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

13

DT-1 SUFFIX
CASE 369-03
Plastic Package

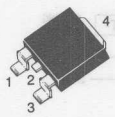


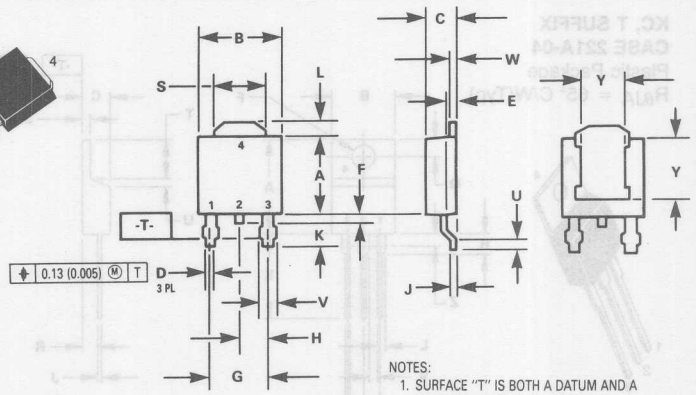


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.64	0.88	0.025	0.035
E	0.97	1.06	0.038	0.042
G	2.29 BSC		0.090 BSC	
J	0.46	0.58	0.018	0.023
K	8.89	9.65	0.350	0.380
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	1.91	2.28	0.075	0.090

NOTES:
1. SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: INCH.

DT SUFFIX
CASE 369A-03
Plastic Package
DPAK



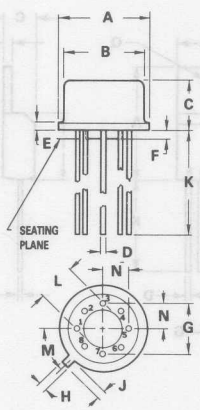


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.69	0.88	0.027	0.035
E	0.97	1.06	0.038	0.042
F	0.64	0.88	0.025	0.035
G	4.58 BSC		0.180 BSC	
H	2.29 BSC		0.090 BSC	
J	6.46	0.58	0.018	0.023
K	2.59	2.89	0.102	0.114
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
U	0.51	—	0.020	—
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	4.32	—	0.170	—

NOTES:
1. SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: INCH.

H, G SUFFIX
CASE 601-04
Metal Package
$R_{\theta JA}$ = 160° C/W(Typ)



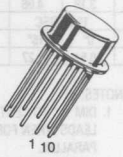


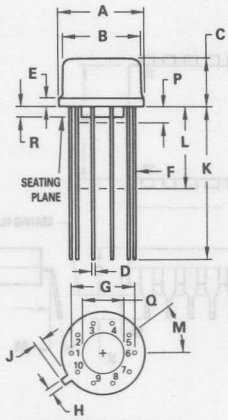
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.51	9.40	0.335	0.370
B	7.75	8.51	0.305	0.335
C	4.19	4.70	0.165	0.185
D	0.41	0.48	0.016	0.019
E	0.25	1.02	0.010	0.040
F	0.25	1.02	0.010	0.040
G	5.08 BSC		0.200 BSC	
H	0.71	0.86	0.028	0.034
J	0.74	1.14	0.029	0.045
K	12.70	—	0.500	—
L	3.05	4.06	0.120	0.160
M	45° BSC		45° BSC	
N	2.41	2.67	0.095	0.105

NOTE:
1. LEADS WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.

13

H, G SUFFIX
CASE 603-04
Metal Can
$R_{\theta JA}$ = 160° C/W





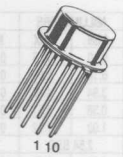
(BOTTOM VIEW)

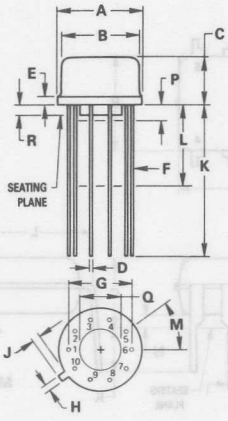
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.51	9.39	0.335	0.370
B	7.75	8.51	0.305	0.335
C	4.19	4.70	0.165	0.185
D	0.407	0.533	0.016	0.021
E	—	1.02	—	0.040
F	0.406	0.483	0.016	0.019
G	5.84 BSC		0.230 BSC	
H	0.712	0.864	0.028	0.034
J	0.737	1.14	0.029	0.045
K	12.70	—	0.500	—
L	6.35	12.70	0.250	0.500
M	36° BSC		36° BSC	
P	—	1.27	—	0.050
Q	3.56	4.06	0.140	0.160
R	0.254	1.02	0.010	0.040

All JEDEC Dimensions and Notes Apply.

NOTE:
LEADS WITHIN 0.18 mm (0.007) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.

G SUFFIX
CASE 603C-01
Metal Can
$R_{\theta JA}$ = 150° C/W(Typ)



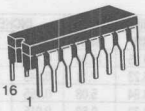


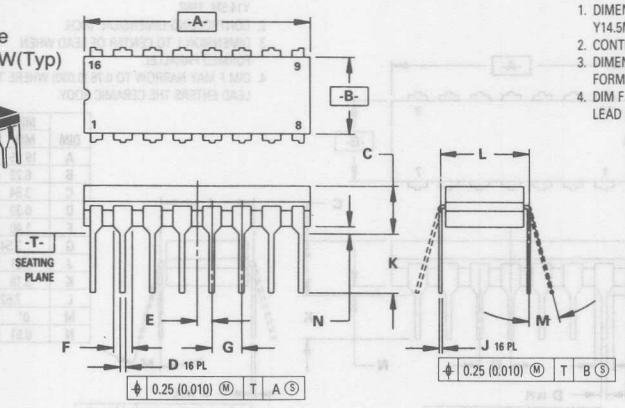
(BOTTOM VIEW)

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.51	9.39	0.335	0.370
B	7.75	8.51	0.305	0.335
C	4.19	6.73	0.165	0.265
D	0.407	0.533	0.016	0.021
E	—	1.02	—	0.040
F	0.406	0.483	0.016	0.019
G	5.84 BSC		0.230 BSC	
H	0.712	0.864	0.028	0.034
J	0.737	1.14	0.029	0.045
K	12.70	—	0.500	—
L	6.35	12.70	0.250	0.500
M	36° BSC		36° BSC	
P	—	1.27	—	0.050
Q	3.56	4.06	0.140	0.160
R	0.254	1.02	0.010	0.040

NOTES:
1. LEADS WITHIN 0.18 mm (0.007) RADIUS OF TRUE POSITION TO DIM. "A" & "H" AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. LEAD DIA UNCONTROLLED BEYOND DIM "K" MIN.

DP2, D, J, N SUFFIX
CASE 620-10
Ceramic Package
$R_{\theta JA}$ = 100° C/W(Typ)



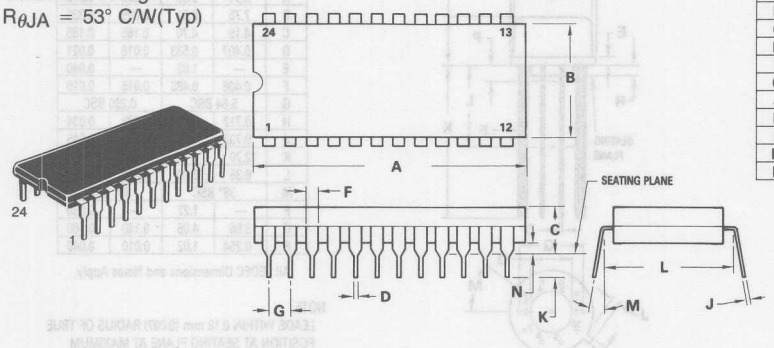


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	19.05	19.93	0.750	0.785
B	6.10	7.49	0.240	0.295
C	—	5.08	—	0.200
D	0.39	0.50	0.015	0.020
E	1.27 BSC		0.050 BSC	
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	3.18	4.31	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

13

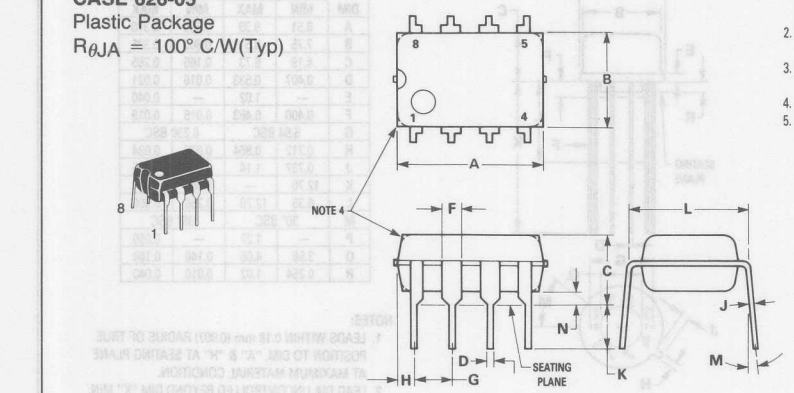
L SUFFIX
CASE 623-05
Ceramic Package
$R_{\theta JA}$ = 53° C/W(Typ)



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	31.24	32.77	1.230	1.290
B	12.70	15.49	0.500	0.610
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

NOTES:
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL).

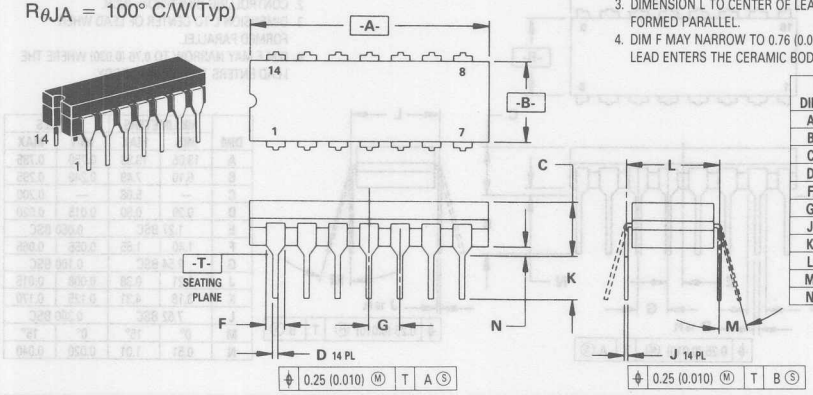
DP1, N, P, P1 SUFFIX
CASE 626-05
Plastic Package
$R_{\theta JA}$ = 100° C/W(Typ)



NOTES:
1. LEAD POSITIONAL TOLERANCE: ⌖ | ⌀ 0.13 (0.005) Ⓜ | T | A Ⓜ | B Ⓜ
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
4. DIMENSIONS A AND B ARE DATUMS.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	—	10°	—	10°
N	0.76	1.01	0.030	0.040

J, F, L SUFFIX
CASE 632-08
Ceramic Package
$R_{\theta JA}$ = 100° C/W(Typ)

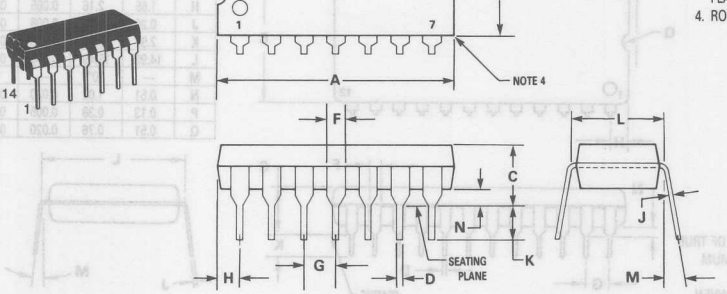


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	19.05	19.94	0.750	0.785
B	6.23	7.11	0.245	0.280
C	3.94	5.08	0.155	0.200
D	0.39	0.50	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	3.18	4.31	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

13

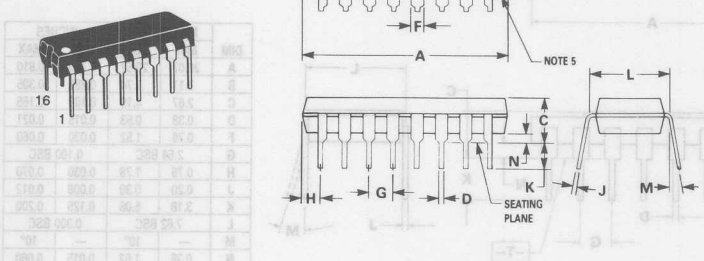
N, P, N-14, P2 SUFFIX
CASE 646-06
Plastic Package
$R_{\theta JA}$ = 100° C/W(Typ)



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.39	1.01	0.015	0.039

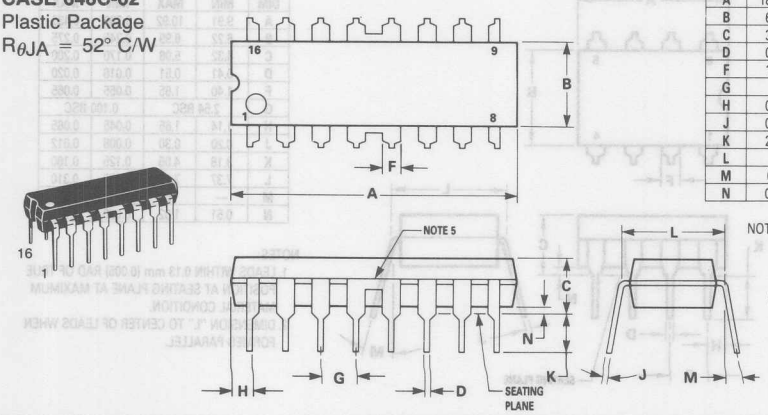
N, P SUFFIX
CASE 648-06
Plastic Package
$R_{\theta JA}$ = 67° C/W(Typ)



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. "F" DIMENSION IS FOR FULL LEADS.
5. ROUNDED CORNERS OPTIONAL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	18.80	21.34	0.740	0.840
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.38	2.41	0.015	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.39	1.01	0.015	0.040

P SUFFIX
CASE 648C-02
Plastic Package
$R_{\theta JA}$ = 52° C/W

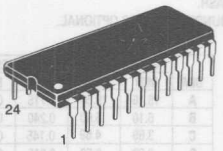


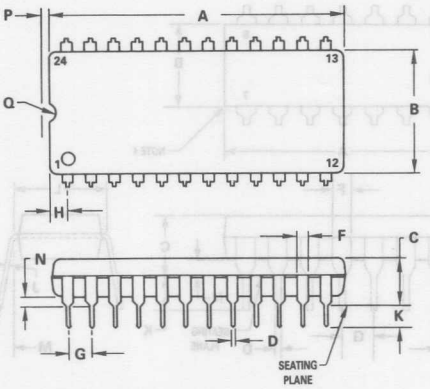
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	18.80	21.34	0.740	0.840
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.38	2.41	0.015	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.39	1.01	0.015	0.040

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITON AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.
5. EXTERNAL LEAD CONNECTION, BETWEEN 4 AND 5, 12 AND 13 AS SHOWN.

13

P SUFFIX
CASE 649-03
Plastic Package
$R_{\theta JA}$ = 90° C/W(Typ)

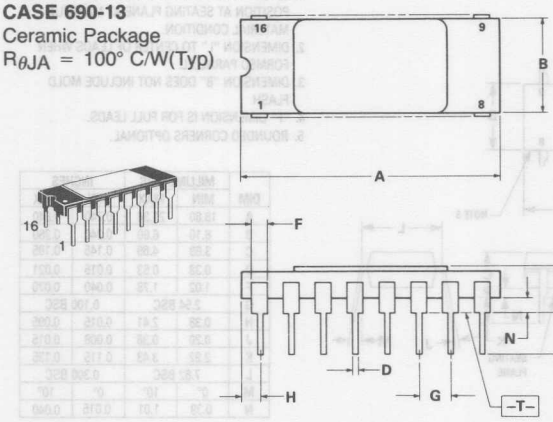




DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	31.50	32.13	1.240	1.265
B	13.21	13.72	0.520	0.540
C	4.70	5.21	0.185	0.205
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	14.99	15.49	0.590	0.610
M	—	10°	—	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

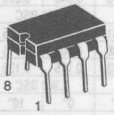
L SUFFIX
CASE 690-13
Ceramic Package
$R_{\theta JA}$ = 100° C/W(Typ)

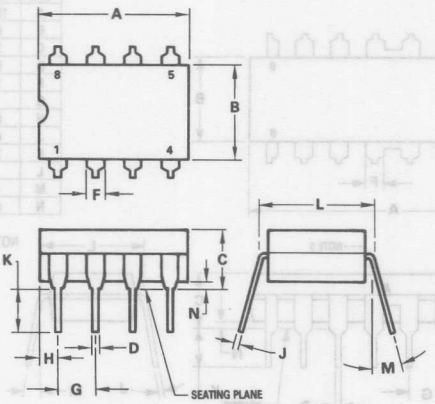


NOTES:
1. -A- AND -B- ARE DATUMS.
2. -T- IS SEATING PLANE
3. POSITIONAL TOLERANCE FOR LEADS (D).
   ⌖ | ϕ 0.25 (0.010) Ⓜ | T | A Ⓜ | B Ⓜ
4. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.07	20.57	0.790	0.810
B	7.11	7.74	0.280	0.305
C	2.67	4.19	0.105	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.52	0.030	0.060
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	3.18	5.08	0.125	0.200
L	7.62 BSC		0.300 BSC	
M	—	10°	—	10°
N	0.38	1.52	0.015	0.060

J-8, J, JG, U, Z SUFFIX
CASE 693-02
Ceramic Package
$R_{\theta JA}$ = 100° C/W(Typ)



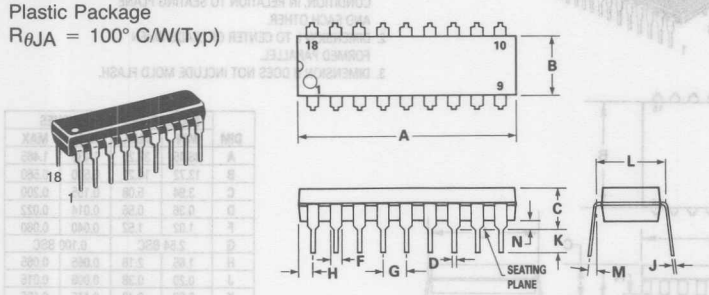


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.91	10.92	0.390	0.430
B	6.22	6.99	0.245	0.275
C	4.32	5.08	0.170	0.200
D	0.41	0.51	0.016	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	1.14	1.65	0.045	0.065
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.37	7.87	0.290	0.310
M	—	15°	—	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RAD OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

13

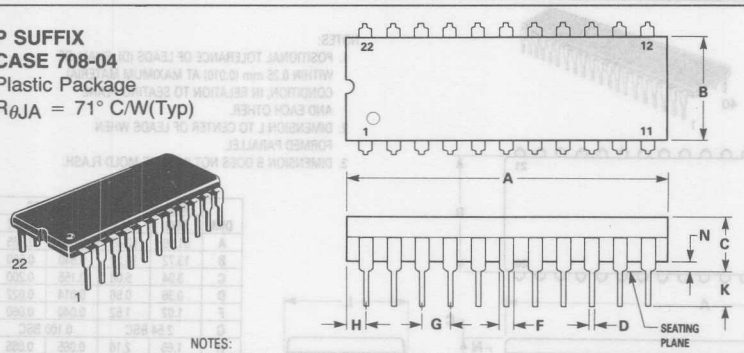
A, B, N, P SUFFIX
CASE 707-02
Plastic Package
$R_{\theta JA}$ = 100° C/W(Typ)



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

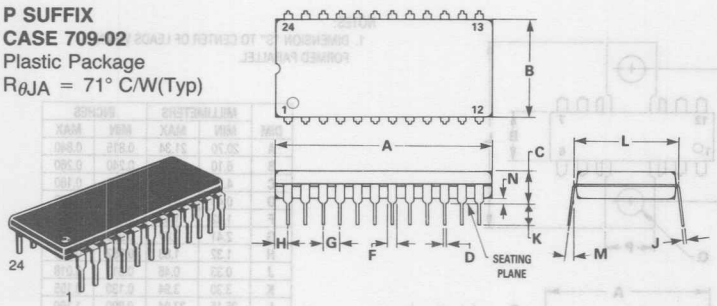
P SUFFIX
CASE 708-04
Plastic Package
$R_{\theta JA}$ = 71° C/W(Typ)



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	27.56	28.32	1.085	1.115
B	8.64	9.14	0.340	0.360
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	10.16 BSC		0.400 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

P SUFFIX
CASE 709-02
Plastic Package
$R_{\theta JA}$ = 71° C/W(Typ)

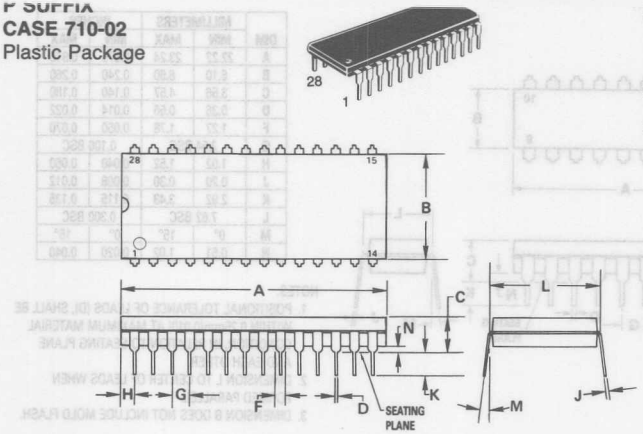


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.03	0.065	0.080
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

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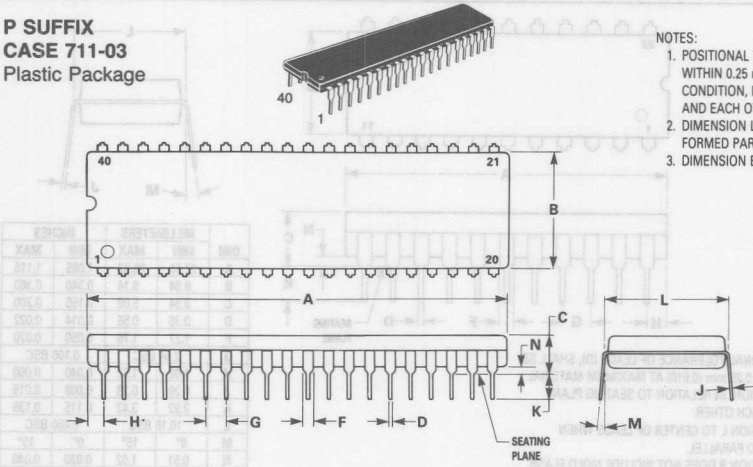
P SUFFIX
CASE 710-02
Plastic Package



1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

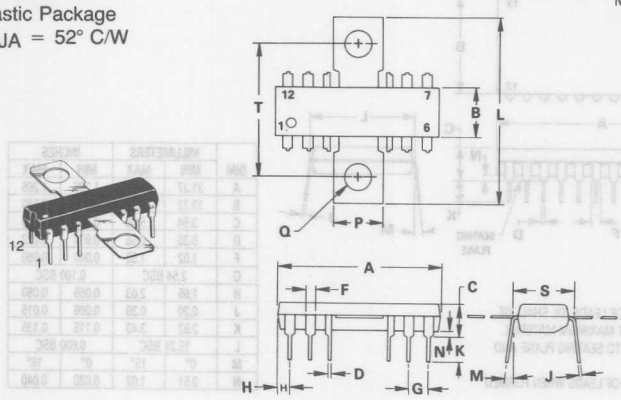
P SUFFIX
CASE 711-03
Plastic Package



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

CASE 721-02
Plastic Package
$R_{\theta JA}$ = 52° C/W

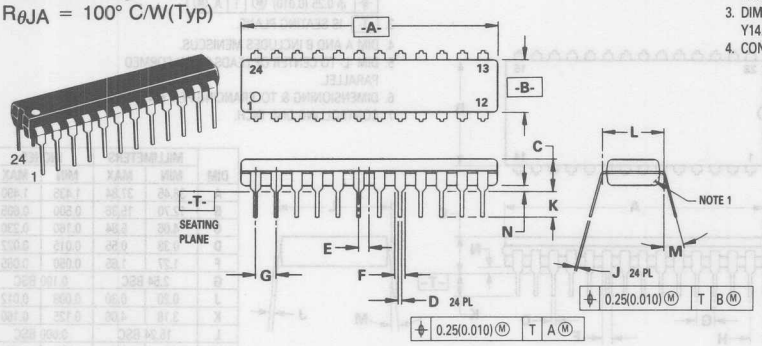


NOTES:
1. DIMENSION "S" TO CENTER OF LEADS WHEN FORMED PARALLEL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	20.70	21.34	0.815	0.840
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.43	0.56	0.017	0.022
F	1.02	1.52	0.040	0.060
G	2.41	2.67	0.095	0.105
H	1.32	1.83	0.052	0.072
J	0.33	0.46	0.013	0.018
K	3.30	3.94	0.130	0.155
L	25.15	27.94	0.990	1.100
M	—	10°	—	10°
N	0.51	1.02	0.020	0.040
P	6.27	6.53	0.247	0.257
Q	3.48	3.73	0.137	0.147
S	7.37	7.87	0.290	0.310
T	16.26	16.76	0.640	0.660

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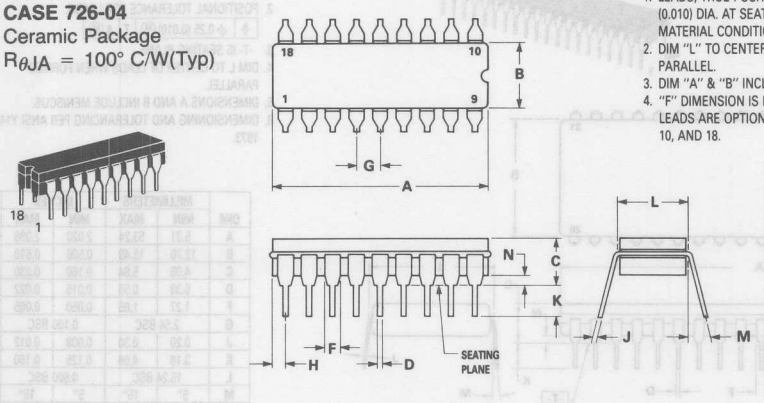
P-3, P-60, P-120 SUFFIX
CASE 724-03
Plastic Package
$R_{\theta JA}$ = 100° C/W(Typ)



NOTES:
1. CHAMFERRED CONTOUR OPTIONAL.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.25	32.13	1.230	1.265
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.38	0.51	0.015	0.020
E	1.27 BSC		0.050 BSC	
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
J	0.18	0.30	0.007	0.012
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

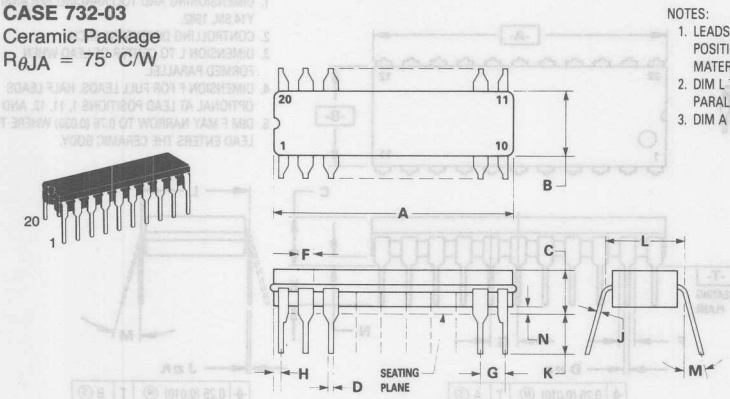
J, L SUFFIX
CASE 726-04
Ceramic Package
$R_{\theta JA}$ = 100° C/W(Typ)



NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA. AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM "A" & "B" INCLUDES MENISCUS.
4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 9, 10, AND 18.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	22.35	23.11	0.880	0.910
B	6.10	7.49	0.240	0.295
C	—	5.08	—	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.32	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

L SUFFIX
CASE 732-03
Ceramic Package
$R_{\theta JA}$ = 75° C/W

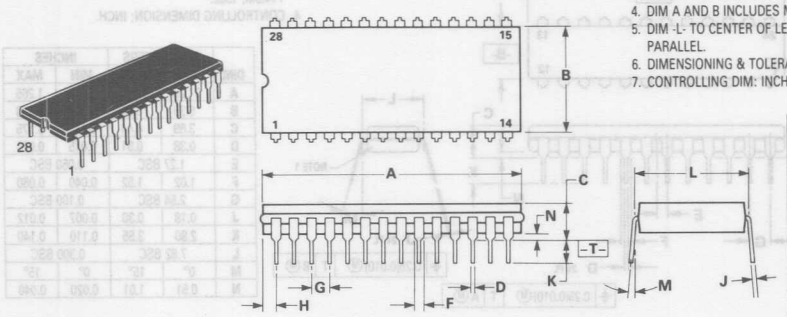


NOTES:
1. LEADS WITHIN 0.25 mm (0.010) DIA., TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM A AND B INCLUDES MENISCUS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	23.88	25.15	0.940	0.990
B	6.60	7.49	0.260	0.295
C	3.81	5.08	0.150	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.25	1.02	0.010	0.040

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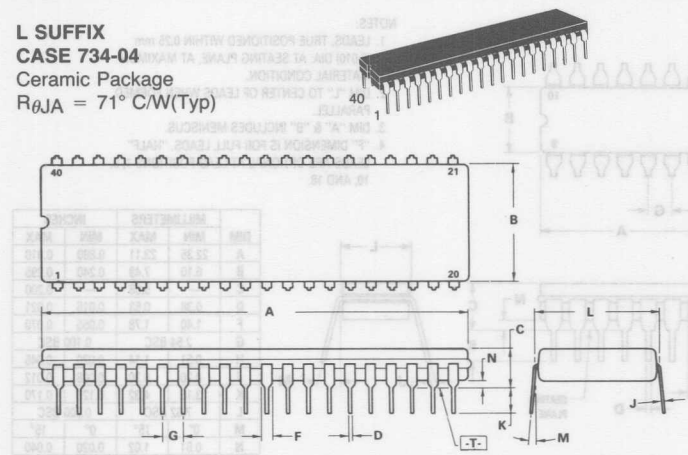
L SUFFIX
CASE 733-04
Ceramic Package



NOTES:
1. DIM -A- IS DATUM.
2. POSITIONAL TOL FOR LEADS: ⌖ ϕ 0.25 (0.010) Ⓜ T A Ⓜ
3. -T- IS SEATING PLANE.
4. DIM A AND B INCLUDES MENISCUS.
5. DIM -L- TO CENTER OF LEADS WHEN FORMED PARALLEL.
6. DIMENSIONING & TOLERANCING PER Y14.5, 1982.
7. CONTROLLING DIM: INCH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	36.45	37.84	1.435	1.490
B	12.70	15.36	0.500	0.605
C	4.06	5.84	0.160	0.230
D	0.38	0.55	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

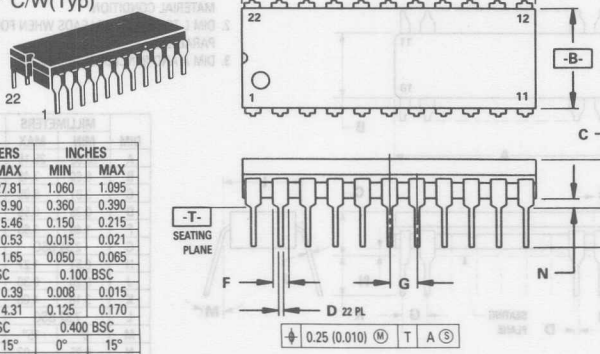
L SUFFIX
CASE 734-04
Ceramic Package
$R_{\theta JA}$ = 71° C/W(Typ)



NOTES:
1. DIM -A- IS A DATUM.
2. POSITIONAL TOLERANCE FOR LEADS: ⌖ ϕ 0.25 (0.010) Ⓜ T A Ⓜ
3. -T- IS SEATING PLANE.
4. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONS A AND B INCLUDE MENISCUS.
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	5.31	53.24	2.020	2.096
B	12.70	15.49	0.500	0.610
C	4.06	5.84	0.160	0.230
D	0.38	0.56	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	5°	15°	5°	15°
N	0.51	1.27	0.020	0.050

L SUFFIX
CASE 736-05
Ceramic Package
$R_{\theta JA}$ = 71° C/W(Typ)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F FOR FULL LEADS. HALF LEADS OPTIONAL AT LEAD POSITIONS 1, 11, 12, AND 22.
5. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

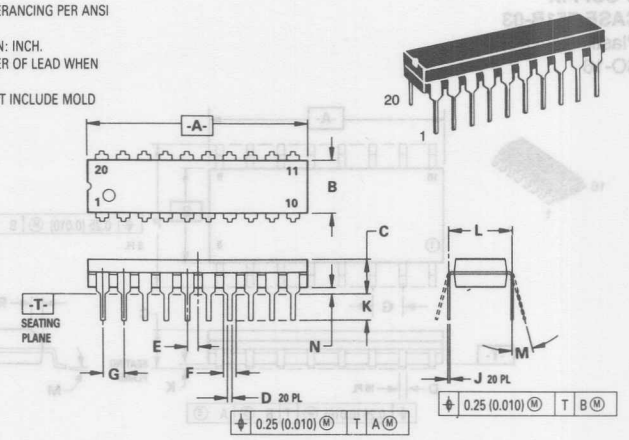
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	26.93	27.81	1.060	1.095
B	9.15	9.90	0.360	0.390
C	3.81	5.46	0.150	0.215
D	0.39	0.53	0.015	0.021
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.39	0.008	0.015
K	3.18	4.31	0.125	0.170
L	10.16 BSC		0.400 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

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P SUFFIX
CASE 738-03
Plastic Package
$R_{\theta JA}$ = 75° C/W

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.

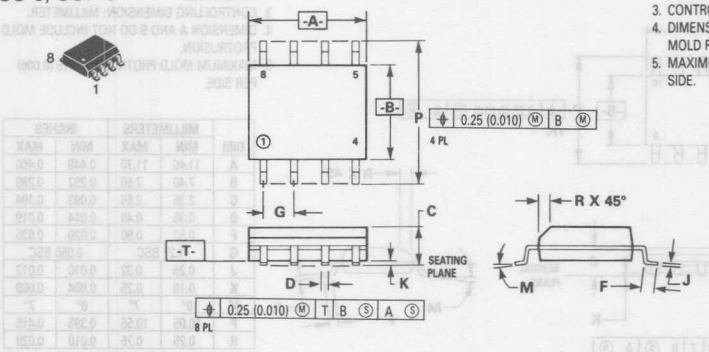
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	25.66	27.17	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.81	4.57	0.150	0.180
D	0.39	0.55	0.015	0.022
E	1.27 BSC		0.050 BSC	
F	1.27	1.77	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040



D SUFFIX
CASE 751-02
Plastic Package
SO-8, SOP-8

NOTES:
1. DIMENSIONS "A" AND "B" ARE DATUMS AND "T" IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIM: MILLIMETER.
4. DIMENSION "A" AND "B" DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

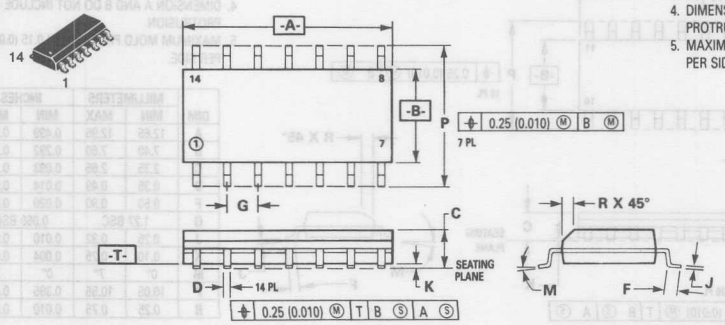
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019



D SUFFIX
CASE 751A-02
Plastic Package
SO-14

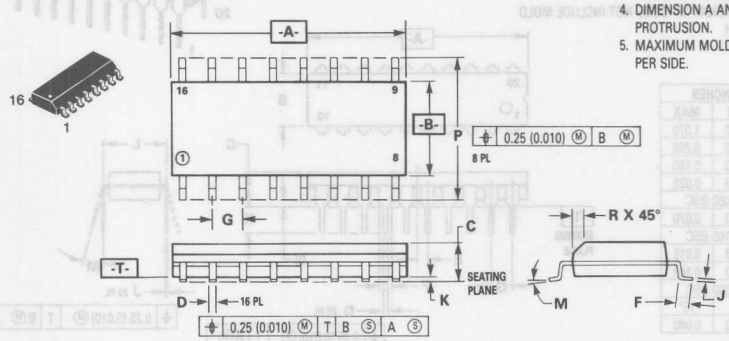
NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019



13

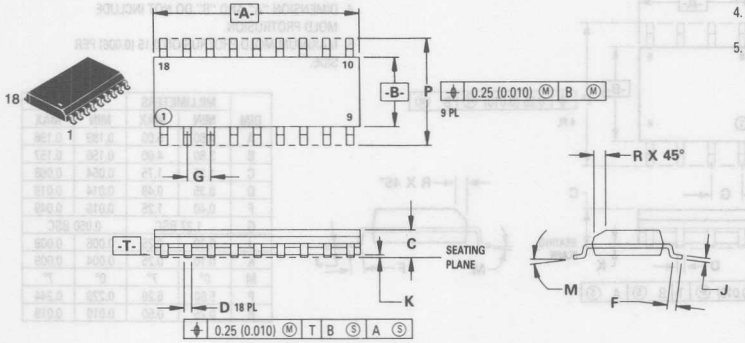
Plastic Package
SO-16



2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

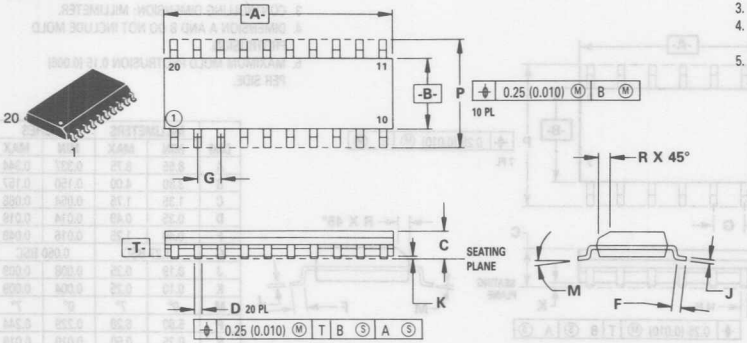
DW SUFFIX
CASE 751C-03
Plastic Package
SO-18



NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	11.40	11.70	0.449	0.460
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

DW SUFFIX
CASE 751D-03
Plastic Package
SO-20L

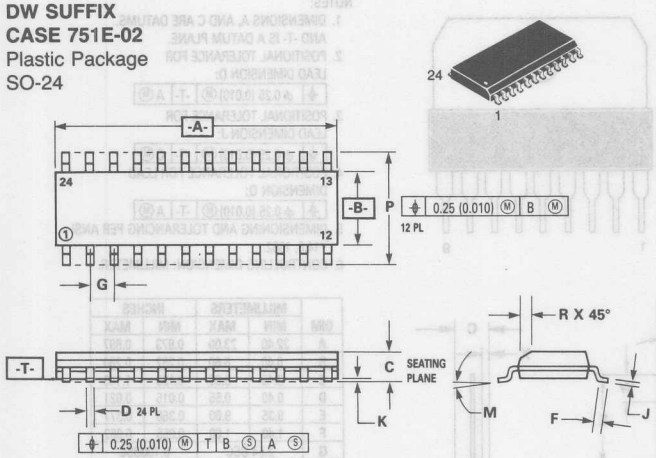


NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

13

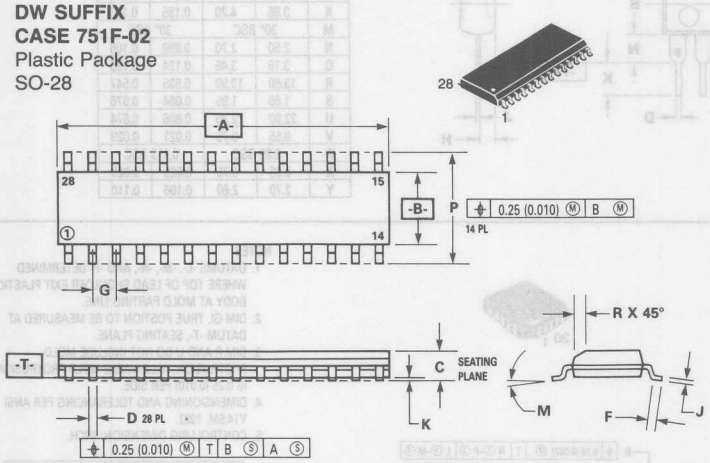
DW SUFFIX
CASE 751E-02
Plastic Package
SO-24



NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.25	15.50	0.601	0.610
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

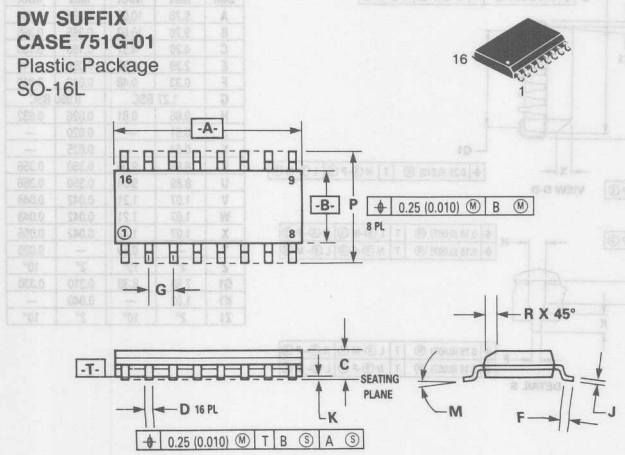
DW SUFFIX
CASE 751F-02
Plastic Package
SO-28



NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	17.80	18.05	0.701	0.710
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

DW SUFFIX
CASE 751G-01
Plastic Package
SO-16L

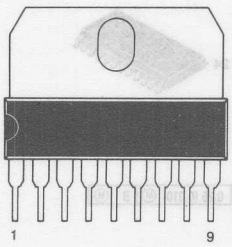


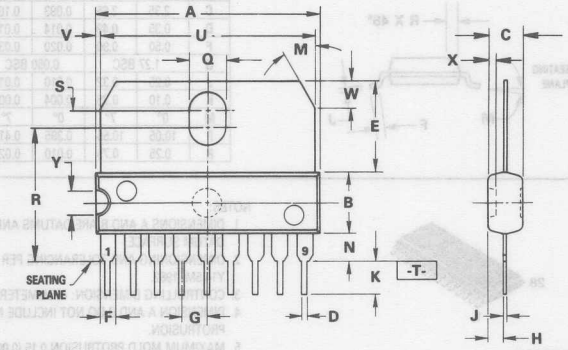
NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
	0.25	0.75	0.010	0.029

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CASE 762-01
Plastic Medium Power Package
SIP 9
$R_{\theta JA}$ = 70° C/W(Typ)
$R_{\theta JC}$ = 15° C/W(Typ)



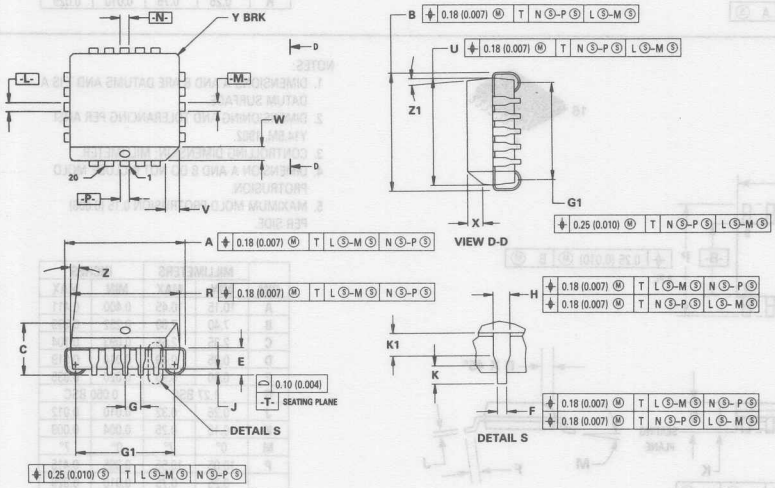


NOTES:
1. DIMENSIONS A, AND C ARE DATUMS. AND -T- IS A DATUM PLANE.
2. POSITIONAL TOLERANCE FOR LEAD DIMENSION D:
   ⌖ ϕ 0.25 (0.010) Ⓜ -T- A Ⓜ
3. POSITIONAL TOLERANCE FOR LEAD DIMENSION J:
   ⌖ ϕ 0.25 (0.010) Ⓜ -T- C Ⓜ
4. POSITIONAL TOLERANCE FOR LEAD DIMENSION Q:
   ⌖ ϕ 0.25 (0.010) Ⓜ -T- A Ⓜ
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1982.
6. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	22.40	23.00	0.873	0.897
B	6.40	6.60	0.252	0.260
C	3.45	3.65	0.135	1.143
D	0.40	0.55	0.015	0.021
E	9.35	9.60	0.368	0.377
F	1.40	1.60	0.055	0.062
G	2.54 BSC		0.100BSC	
H	1.51	1.71	0.059	0.067
J	0.360	0.400	0.014	0.015
K	3.95	4.20	0.155	0.165
M	30° BSC		30° BSC	
N	2.50	2.70	0.099	0.106
Q	3.15	3.45	0.124	0.135
R	13.60	13.90	0.535	0.547
S	1.65	1.95	0.064	0.076
U	22.00	22.20	0.866	0.874
V	0.55	0.75	0.021	0.029
W	2.89 BSC		0.113 BSC	
X	0.65	0.75	0.025	0.029
Y	2.70	2.80	0.106	0.110

FN SUFFIX
CASE 775-02
Plastic Package
PLCC-20
$R_{\theta JA}$ = 72° C/W(Typ)
(5K SQML)





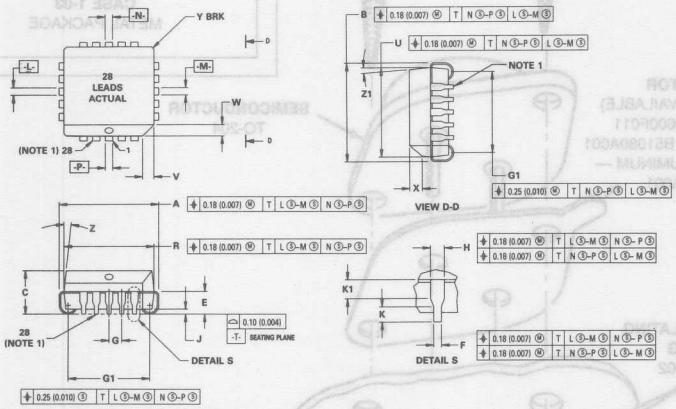
NOTES:
1. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
2. DIM GI, TRUE POSTION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.78	10.03	0.385	0.395
B	9.78	10.03	0.385	0.395
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	—	0.020	—
K	0.64	—	0.025	—
R	8.89	9.04	0.350	0.356
U	8.89	9.04	0.350	0.356
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	—	0.50	—	0.020
Z	2°	10°	2°	10°
G1	7.88	8.38	0.310	0.330
K1	1.02	—	0.040	—
Z1	2°	10°	2°	10°

13

FN SUFFIX
CASE 776-02
Plastic Package
PLCC-28
$R_{\theta JA}$ = 66° C/W(Typ)
(5K SQML)



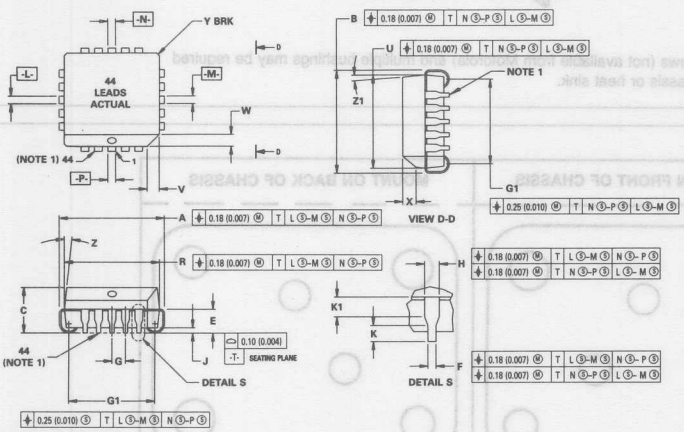


NOTES:
1. **DUE TO SPACE LIMITATION, CASE 776-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 28 LEADS.**
2. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
3. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
4. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: INCH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.32	12.57	0.485	0.495
B	12.32	12.57	0.485	0.495
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	—	0.020	—
K	0.64	—	0.025	—
R	11.43	11.58	0.450	0.456
U	11.43	11.58	0.450	0.456
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	—	0.50	—	0.020
Z	2°	10°	2°	10°
G1	10.42	10.92	0.410	0.430
K1	1.02	—	0.040	—
Z1	2°	10°	2°	10°

FN SUFFIX
CASE 777-02
Plastic Package
PLCC-44
$R_{\theta JA}$ = 55° C/W(Typ)
(10K SQML)



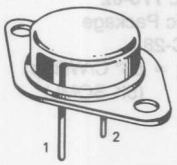


NOTES:
1. **DUE TO SPACE LIMITATION, CASE 777-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 44 LEADS.**
2. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
3. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
4. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: INCH.

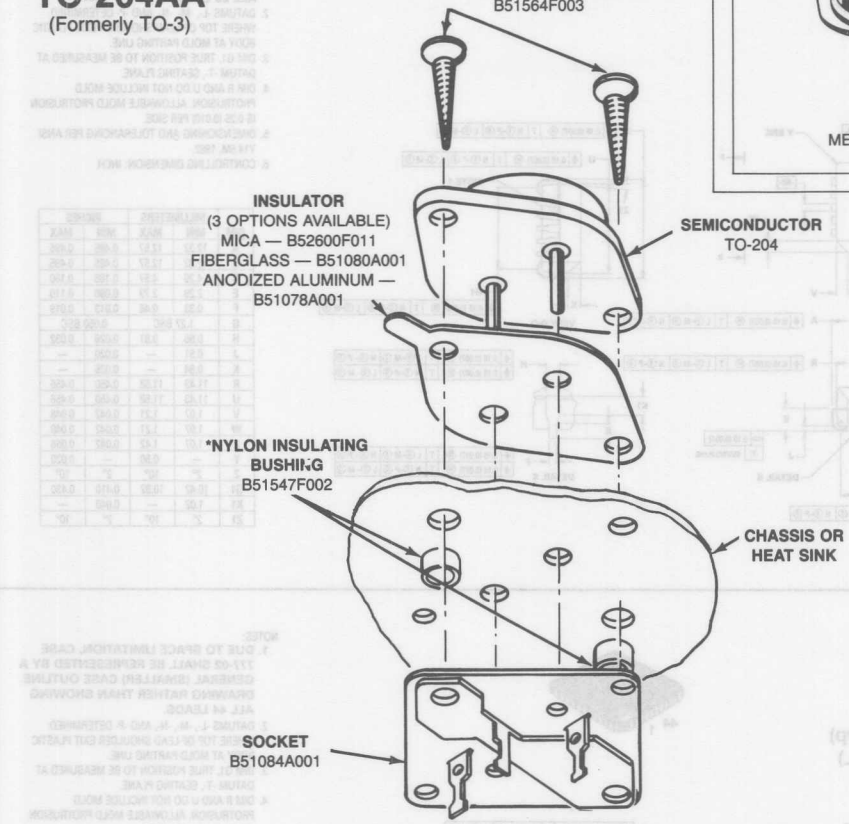
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	17.40	17.65	0.685	0.695
B	17.40	17.65	0.685	0.695
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	—	0.020	—
K	0.64	—	0.025	—
R	16.51	16.66	0.650	0.656
U	16.51	16.66	0.650	0.656
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	—	0.50	—	0.020
Z	2°	10°	2°	10°
G1	15.50	16.00	0.610	0.630
K1	1.02	—	0.040	—
Z1	2°	10°	2°	10°

13

Mounting Hardware TO-204AA
(Formerly TO-3)

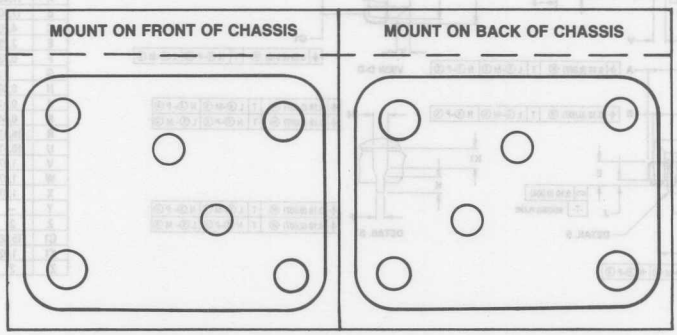


CASE 1-03
METAL PACKAGE



*Longer screws (not available from Motorola) and multiple bushings may be required for thick chassis or heat sink.

DRAWINGS NOT TO SCALE

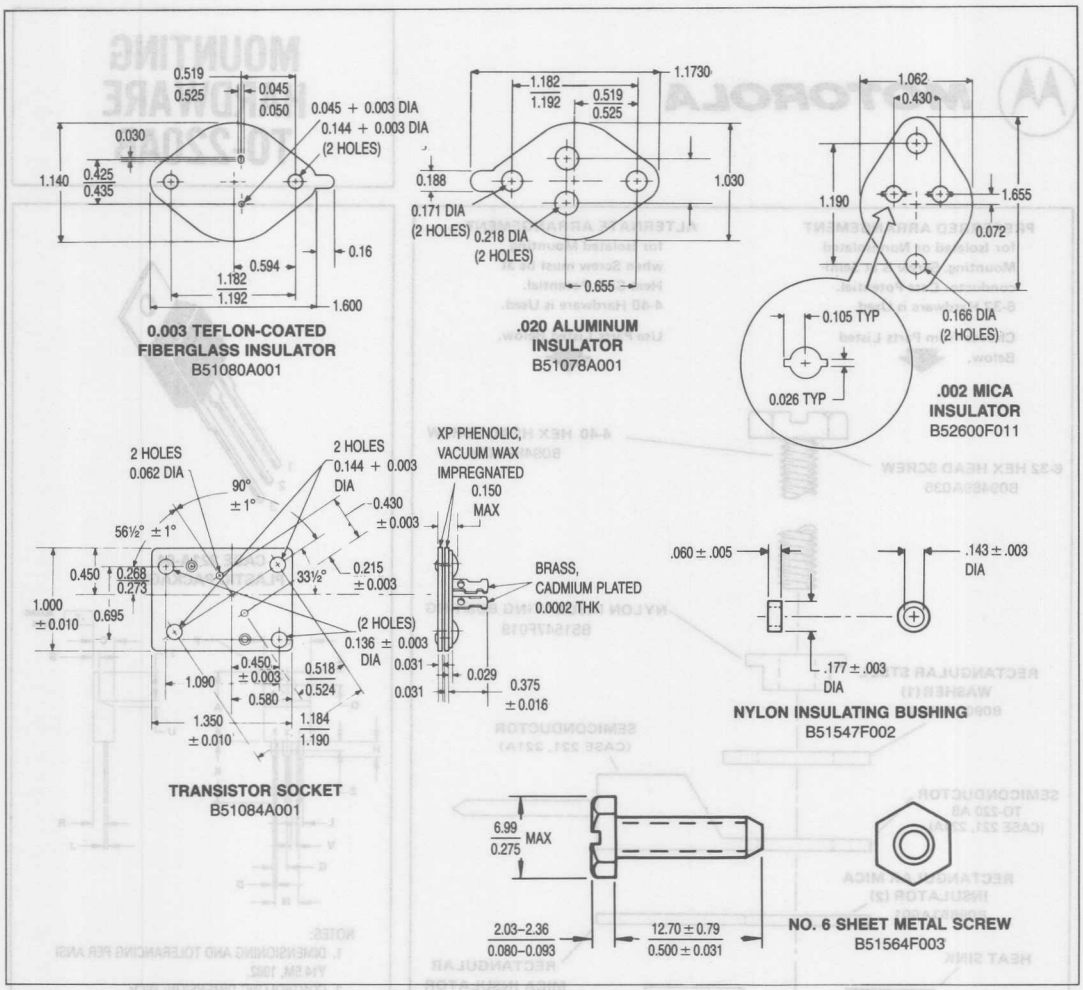


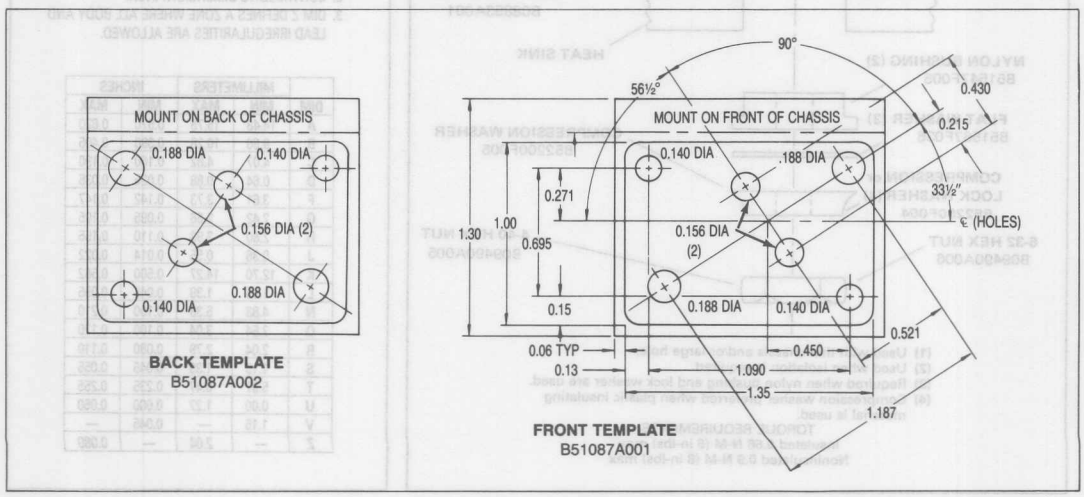
FRONT TEMPLATE
B51087A001

BACK TEMPLATE
B51087A002

13

MOUNTING HARDWARE TO-204AA





13

MOTOROLA

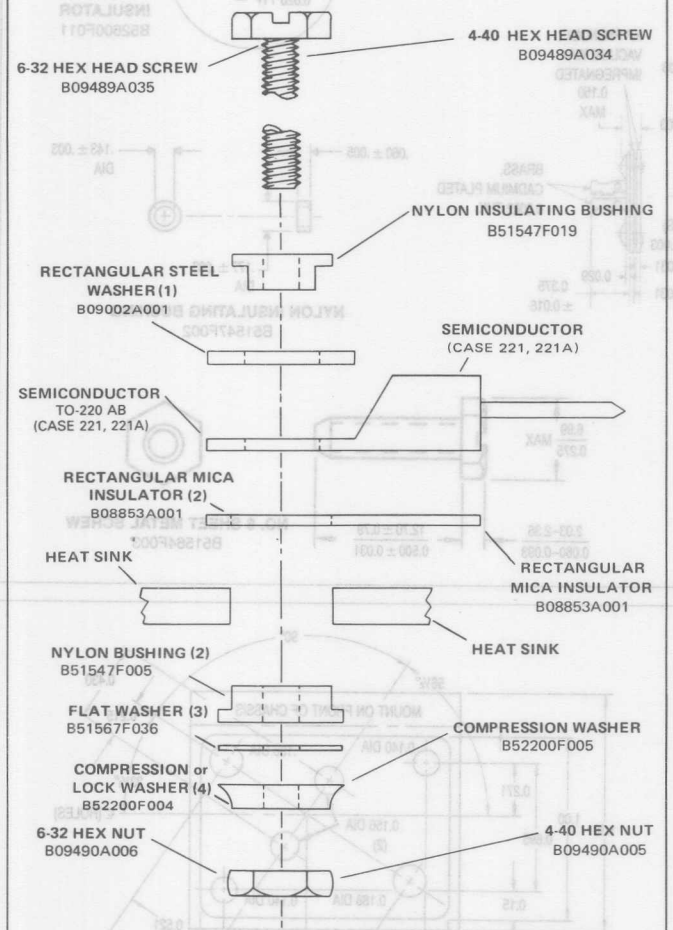
MOUNTING HARDWARE TO-220AB

PREFERRED ARRANGEMENT
for Isolated or Non-isolated Mounting. Screw is at Semiconductor Case Potential. 6-32 Hardware is Used.

Choose from Parts Listed Below.

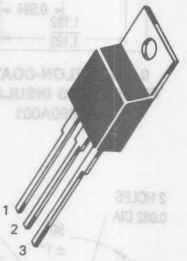
ALTERNATE ARRANGEMENT
for Isolated Mounting when Screw must be at Heat-Sink Potential. 4-40 Hardware is Used.

Use Parts Listed Below.

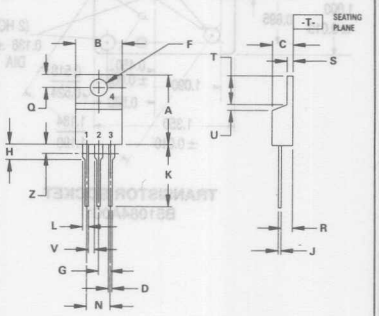


(1) Used with thin chassis and/or large hole.
(2) Used when isolation is required.
(3) Required when nylon bushing and lock washer are used.
(4) Compression washer preferred when plastic insulating material is used.

TORQUE REQUIREMENTS
Insulated 0.68 N-M (6 in-lbs) max
Noninsulated 0.9 N-M (8 in-lbs) max



CASE 221A-04
PLASTIC PACKAGE



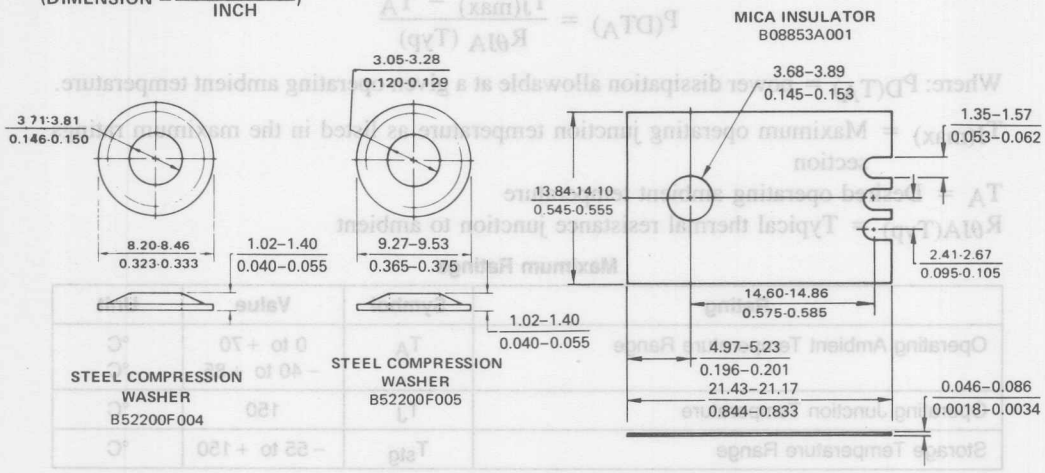
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

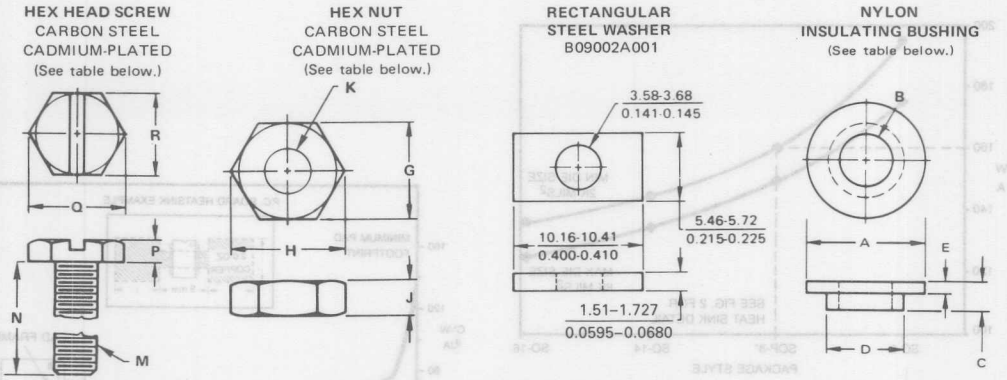
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

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MOUNTING HARDWARE TO-220AB

(DIMENSION — MILLIMETER / INCH)





DIMENSIONS — MILLIMETER (INCH)

NYLON BUSHING

PART NO.	DIM A	DIM B	DIM C	DIM D	DIM E
B51547F005	9.40-9.65 (0.370-0.380)	3.84-4.09 (0.151-0.161)	2.16-2.41 (0.085-0.095)	6.10-6.35 (0.240-0.250)	1.02-1.27 (0.040-0.050)
B51547F019	5.59-6.10 (0.220-0.240)	3.05-3.15 (0.120-0.124)	1.73-1.91 (0.068-0.075)	3.61-3.68 (0.142-0.145)	0.51-0.64 (0.020-0.025)

HEX NUT

TYPE	PART NO.	DIM G	DIM H	DIM J	DIM K
4-40	B09490A005	6.12-6.35 (0.241-0.250)	6.98-7.34 (0.275-0.289)	2.21-2.49 (0.087-0.098)	2.84 NOM (0.112 NOM)
6-32	B09490A006	7.67-7.92 (0.302-0.312)	8.74-9.17 (0.344-0.361)	2.59-2.90 (0.102-0.114)	3.50 NOM (0.138 NOM)

HEX HEAD SCREW

TYPE	PART NO.	DIM M	DIM N	DIM P	DIM Q	DIM R
4-40	B09489A034	0.112-40	1.57 (0.62)	1.24-1.52 (0.049-0.060)	5.13 MIN (0.202 MIN)	4.60-4.75 (0.181-0.187)
6.32	B09489A035	0.138-32	1.57 (0.62)	2.03-2.36 (0.080-0.093)	6.91 MIN (0.272 MIN)	6.20-6.35 (0.244-0.250)

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The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{(DT_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA\ (Typ)}}$$

Where: $P_{D(T_A)}$ = power dissipation allowable at a given operating ambient temperature.

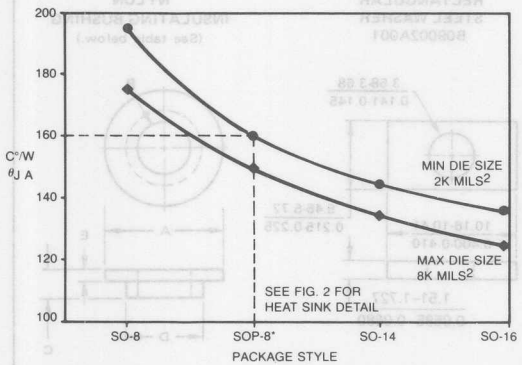
$T_{J(max)}$ = Maximum operating junction temperature as listed in the maximum ratings section

T_A = Desired operating ambient temperature

$R_{\theta JA(Typ)}$ = Typical thermal resistance junction to ambient

Maximum Ratings

Rating	Symbol	Value	Unit
Operating Ambient Temperature Range	T_A	0 to +70 −40 to +85	°C °C
Operating Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C



DATA TAKEN USING PHILIPS SO TEST BOARD #7322-078, 80873
*SOP-8 USING STANDARD SO-8 FOOTPRINT — MIN PAD SIZE

Figure 1. Thermal Resistance, Junction-to-Ambient (°C/W)

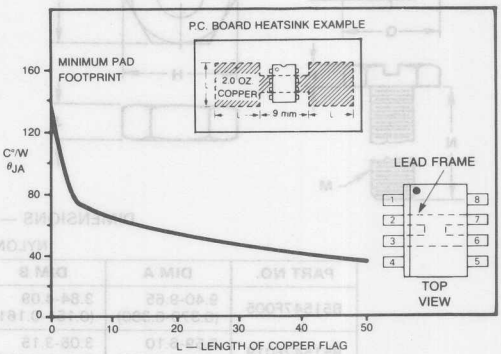
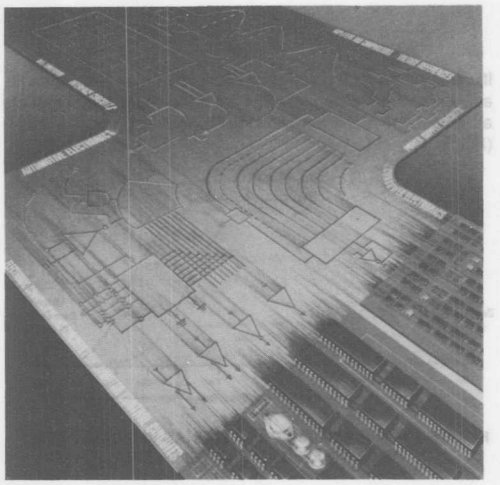


Figure 2. Thermal Resistance for SOP-8 Package Die 2K mils²

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THERMAL RESISTANCE OF SOIC PACKAGES

Measurement specimens are solder mounted on a Philips SO test board #7322-078, 80873 in still air. No auxiliary thermal conduction aids are used. As thermal resistance varies inversely with die area, a given package takes thermal resistance values between the max and min curves shown. These curves represent the smallest (2000 square mils) and largest (8000 square mils) die areas expected to be assembled in the SOIC package.



Quality and Reliability Assurance

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Quality Concepts

The word **Quality** has been used to describe many things, such as fitness for use, customer satisfaction, customer enthusiasm, what the customer says quality is, etc. These descriptions convey important truths, however quality should be described in a way that precipitates immediate action. With that in mind **quality** can be described **as reduction of variability around a target, so that conformance to customer requirements/expectations can be achieved in a cost effective way.** This definition provides direction and potential for immediate action for a person desiring to improve quality. **Quality Improvement** for a task or a process can be quickly described in terms of the target, current status with respect to target (variability), reduction of variability (commitment to never ending improvement), customer requirements (who receives output, what are person's requirements/expectations) and economics (cost of nonconformance; loss function, etc.).

The definition of quality as described above can be applied to a task, process or a whole company. If we are to reap the benefits of quality and obtain a competitive advantage, quality must be applied to the whole company.

Application of quality to the whole company has come to be known by such names as **"Total Quality Control" (TQC); "Company Wide Quality Control" (CWQC); "Total Quality Excellence" (TQE); "Total Quality Involvement" (TQI).** These names attempt to convey the idea that quality is a process (a way of acting continuously) rather than a program (implying a beginning and an end). Nevertheless for this process to be successful it must be able to show measurable results.

Implementation of quality ideas, company, wide requires a quality plan showing: A philosophy (belief) of operation, measurable goals, training of individuals and methods of communicating this philosophy of operation to the whole organization.

Motorola, for example, believes that **quality** and **reliability** are the **responsibility of every person. Participative Management Program (PMP)** is the process by which problem solving and quality improvement are facilitated at all levels of the organization. **Continuous improvement** for the individual is facilitated by a broad educational program covering on-site, university and college courses. The **Motorola Training and Education Center (MTEC)** provides leadership and administers this educational effort on a company wide basis.

Another key belief is that **quality excellence** is accomplished by **people doing things right the first time** and **committed to never ending improvement.** The **Six Sigma (6σ)** challenge is designed to convey and facilitate the idea of continuous improvement at all levels.

"Six Sigma is the required capability level to approach the standard. The **standard** is **zero defects.** Our goal is to be Best-In-Class in product, sales and service." (For a more detailed explanation, contact your Motorola Representative for a pamphlet of the Six Sigma Challenge.)

Quick insight into Six Sigma is obtained if we realize that a Six Sigma process has variability which is one half of the variation allowed (tolerance; spread) by the customer requirements (i.e. natural variation is one half of the customer specification range for a given characteristic). When Six Sigma is achieved, virtually zero defects are observed in the output of a process/product even allowing for potential process shifts (Figure 1).

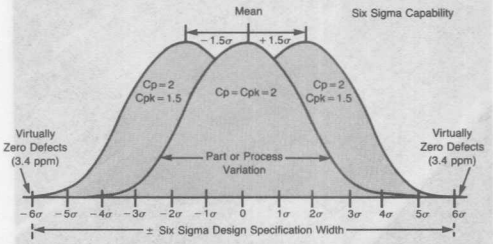


FIGURE 1 — A SIX SIGMA PROCESS HAS VIRTUALLY ZERO DEFECTS ALLOWING FOR 1.5σ SHIFT

Policies, **objectives** and **five year plans** are the mechanisms for communicating the key beliefs and measurable goals to all personnel and continuously keeping them in focus. This is done at the corporate, sector, group, division, and department levels.

The Analog Division, for example, evaluates performance to the corporate goals of **10 Fold Improvement by 1989; 100 Fold Improvement by 1991** and achievement of **Six Sigma capability by 1992** by utilizing indices such as Outgoing Electrical and Visual Mechanical Quality **(AOQ)** in terms of PPM (parts per million or sometimes given in 'parts per billion'); **% of devices with zero PPB; product quality returns** (RMR); number of processes/products with specified **capability indices (cp; cpk); Six Sigma capability roadmaps; failure rates for various reliability tests** (operating life, temperature humidity bias, hast, temperature cycling, etc.); **on time delivery; customer product evaluation and failure analysis turnaround; cost of nonconformance; productivity improvement and personnel development.**

Figure 2 shows the improvement in electrical outgoing quality for bipolar analog products over recent years in a normalized form.

Documentation control is an important part of statistical process control. Process flow charting with documentation identified allows visualization and therefore optimization of the process. Figure 4 shows a portion of a flow chart for Wafer Fabrication. Control plans are an important part of Statistical Process Control, these plans identify in detail critical points where data for process control is taken, parameters measured, frequency of measurements, type of control device used, measuring equipment, responsibilities and reaction plans. Figure 5 shows a portion of a control plan for wafer fabrication. These flow charts and control plans exist for all product flows.

Six Sigma progress is tracked by roadmaps. A portion of a roadmap is shown for example on Figure 6.

On Time Delivery is of great importance, with the current emphasis on just-in-time systems. Tracking is done on an overall basis, and at the device level.

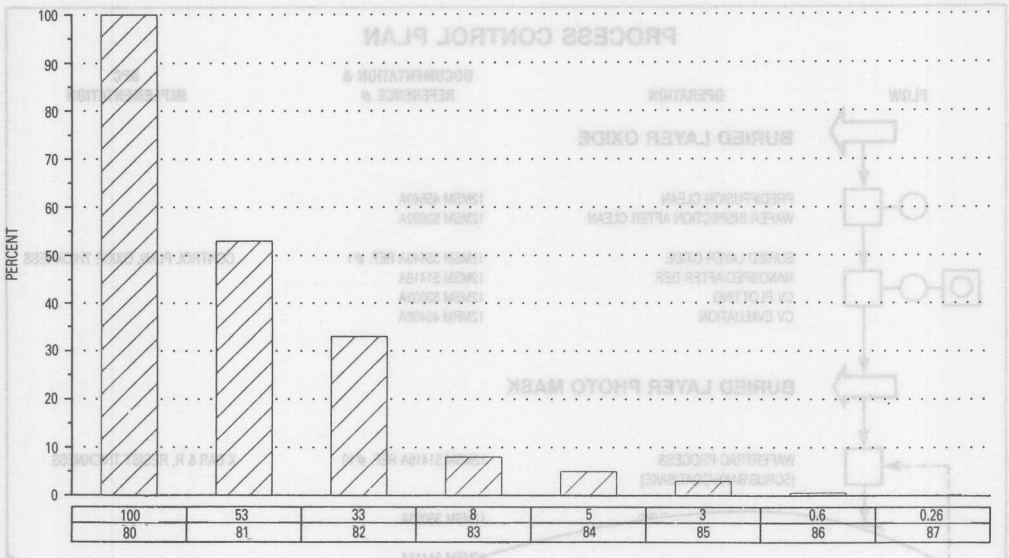


FIGURE 2 — OUTGOING ELECTRICAL QUALITY (AOQ) TREND/NORMALIZED 1980 = 100%

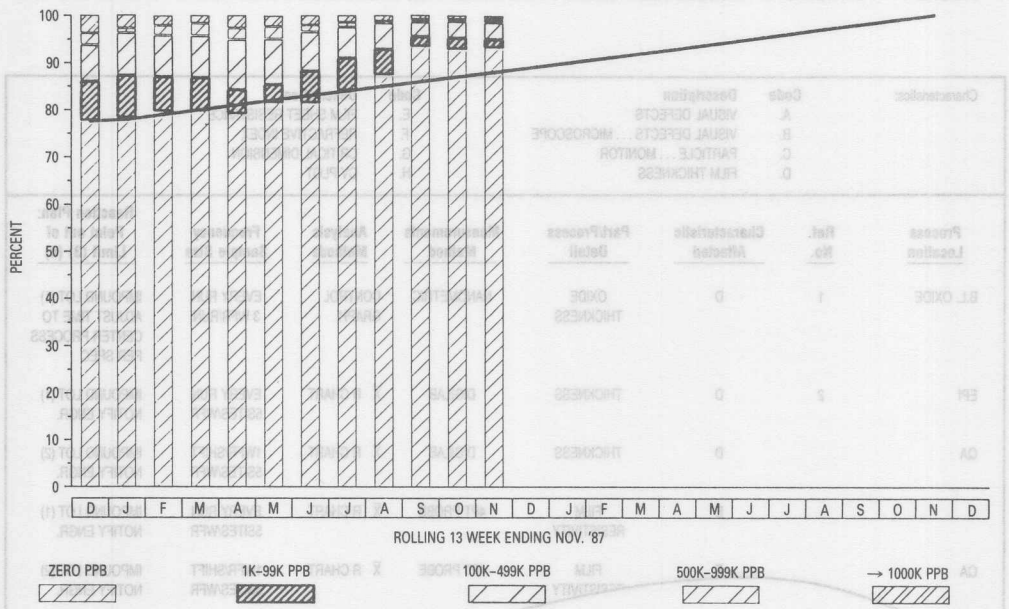


FIGURE 3 — PERCENT (%) OF DEVICES WITH ZERO PARTS PER BILLION (AOQ)

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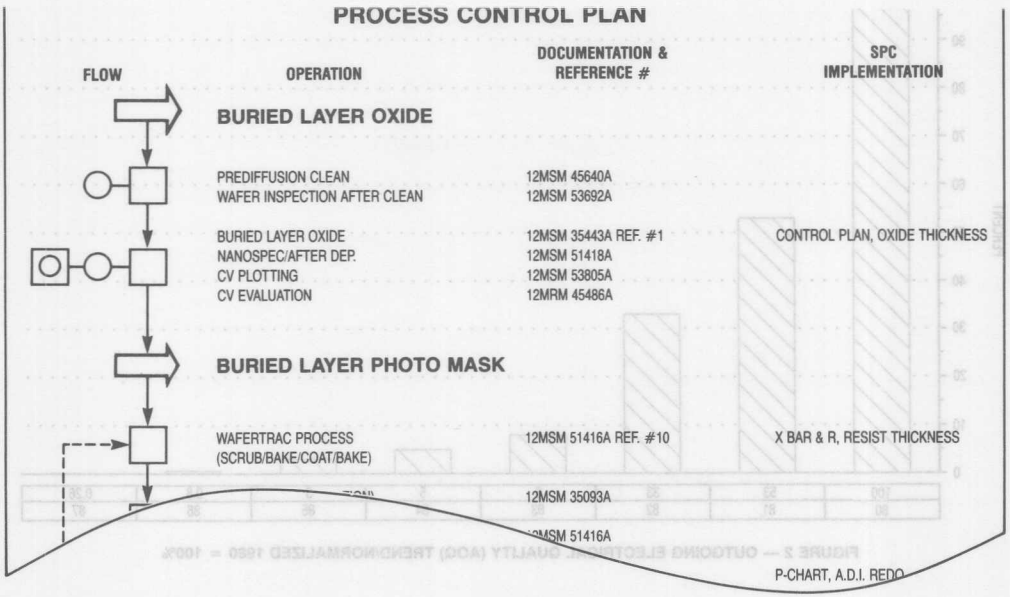


FIGURE 4 — PORTION OF A PROCESS FLOW CHART FROM WAFER FAB, SHOWING DOCUMENTATION CONTROL AND SPC

Characteristics:	Code	Description	Code	Description
	A.	VISUAL DEFECTS	E.	FILM SHEET RESISTANCE
	B.	VISUAL DEFECTS . . . MICROSCOPE	F.	REFRACTIVE INDEX
	C.	PARTICLE . . . MONITOR	G.	CRITICAL DIMENSION
	D.	FILM THICKNESS	H.	CV PLOT

Process Location	Ref. No.	Characteristic Affected	Part/Process Detail	Measurements Method	Analysis Methods	Frequency Sample Size	Reaction Plan: Point out of Limit (3) (4)
B.L. OXIDE	1	D	OXIDE THICKNESS	NANOMETRIC	CONTROL GRAPH	EVERY RUN 3 WFR/RUN	IMPOUND LOT (1) ADJUST TIME TO CENTER PROCESS PER SPEC
EPI	2	D	THICKNESS	DIGILAB	$\bar{X}$ R CHART	EVERY RUN 5SITES/WFR	IMPOUND LOT (1) NOTIFY ENGR.
QA		D	THICKNESS	DIGILAB	$\bar{X}$ R CHART	1WFR/SHIFT 5SITES/WFR	IMPOUND LOT (2) NOTIFY ENGR.
		E	FILM RESISTIVITY	4PT PROBE	$\bar{X}$ R CHART	EVERY RUN 5SITES/WFR	IMPOUND LOT (1) NOTIFY ENGR.
QA		E	FILM [illegible]	4PT PROBE	$\bar{X}$ R CHART	1WFR/SHIFT 5SITES/WFR	IMPOUND LOT (2) NOTIFY ENGR.
DEEP			[illegible]ROBE	MOVING R		EVERY LOT 1 CTRL WFR PER LOT	IMPOUND LOT NOTIFY LPO[illegible]

FIGURE 5 — PART OF A WAFER FAB CONTROL PLAN, SHOWING STATISTICAL PROCESS CONTROL DETAILS

±6σ Summary

Step	
1. Identify critical characteristics	• Product description • Marketing • Industrial Design • R&D/Developmental Engineering • Actual or potential customers
2. Determine specified product elements contributing to critical characteristics	• Critical Characteristics Matrix • Cause-and-effect and Ishikawa diagrams • Success tree/fault tree analysis • Component search or other forms of planned experimentation • FMECA (Failure Mode Effects and Critical Analysis)
3. For each product element, determine the process step or process choice that affects or controls required performance	• Planned experiments • Computer-aided simulation • TOP/process engineering studies • Multi-vari analysis • Comparative experiments
4. Determine maximum (real) allowable tolerance for each [illegible] and proces	• Graphing techniques • Engineering handbooks • Planned experiments • Optimization, especially response surface methodolog[illegible]

FIGURE 6 — PART OF SIX SIGMA (6σ) ROADMAP SHOWING STEPS TO SIX SIGMA CAPABILITY

Reliability Concepts

Reliability is the probability that a Linear integrated circuit will perform its specified function in a given environment for a specified period of time. This is the classical definition of reliability applied to Linear integrated circuits.

Another way of thinking about reliability is in relationship to quality. While quality is a measure of variability (extending to potential nonconformances-rejects) in the population domain, reliability is a measure of variability (extending to potential nonconformances-failures) in the population, time and environmental conditions domain. In brief **reliability** can be thought of as **quality over time and environmental conditions.**

The most frequently used reliability measure for integrated circuits is the **failure rate expressed** in percent per thousand device hours (%/1000 hrs.). If the time interval is small the failure rate is called **"Instantaneous Failure Rate"** [λ (t)] or "Hazard Rate." If the time interval is long (for example total operational time) the failure rate is called **"Cumulative Failure Rate."**

The number of failures observed, taken over the number of device hours accumulated at the end of the observation period and expressed as a percent is called the point estimate failure rate. This however, is a number obtained from observations from a sample of all integrated circuits. If we are to use this number to estimate the failure rate of all integrated circuits (total population), we need to say something about the risk we are taking by using this estimate. A **risk** statement is provided by the **confidence level** expressed together with the failure rate. For example, a 0.1% per 1000 device hours failure rate at 90% confidence level can be thought of as 90% of the integrated circuits will have a failure rate below 0.1%/1000 hours. Mathematically the failure rate at a given confidence level is obtained from the point estimate and the **CHI square** (X^2) distribution. (The X^2 is a statistical distribution used to relate the observed and expected frequencies of an event.) In practice, a reliability calculator rule is used which gives the failure rate at the confidence level desired for the number of failures and device hours under question.

As the number of device hours increases, our confidence in the estimate increases. In integrated circuits, it is preferred to make estimates on the basis of failures per 1,000,000,000 (10^9) device hours **(FITS)** or more. If such large numbers of device hours are not available for a particular device, then the point estimate is obtained by pooling the data from devices that are similar in process, voltage, construction, design, etc., and for which we expect to see the same failure modes in the field.

The environment is specified in terms of the temperature, electric field, relative humidity, etc., by an **Eyring** type equation of the form:

$$\lambda = Ae^{-\frac{\emptyset}{KT}} \ldots e^{-\frac{B}{RH}} \ldots e^{-\frac{C}{E}} \ldots$$

Where A, B, C, Ø & K are constants, T is temperature, RH is relative humidity, E is the electric field, etc.

The most familiar form of this equation deals with the first exponential which shows an **Arrhenious type** relationship of the **failure rate** versus the **junction temperature** of integrated circuits, while the causes of failure generally remain the same. Thus, we can test devices near their maximum junction temperatures, analyze the failures to assure that they are the types that are accelerated by temperature and then applying known acceleration factors, estimate the failure rates for lower junction temperatures. Figure 7 shows an

example of a curve which gives estimates of typical failure rates versus temperature for integrated circuits.

Arrhenious type of equation: $\lambda = Ae - \frac{\emptyset}{KT}$

Where: λ = Failure Rate
A = Constant
e = 2.72
$\emptyset$ = Activation Energy
K = Botzman's Constant
T = Temperature in Degrees Kelvin

$T_J = T_A + \theta_{JA} P_D$ or $T_J = T_C + \theta_{JC} P_D$

Where: T_J = Junction Temperature
T_A = Ambient Temperature
T_C = Case Temperature
θ_{JA} = Junction to Ambient Thermal Resistance
θ_{JC} = Junction to Case Thermal Resistance
P_D = Power Dissipation

Failure rate curves for equipment and devices can be represented by an idealized graph called the **Bathtub Curve** (Figure 8).

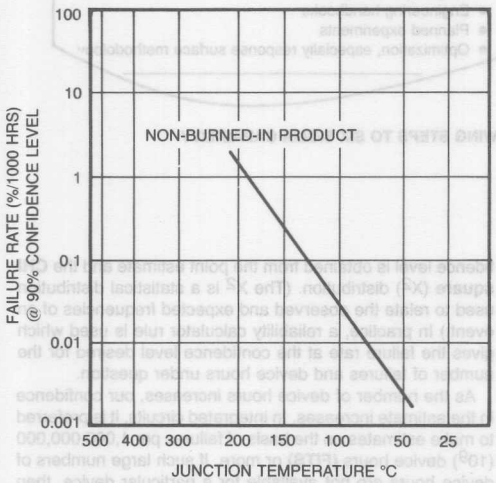


FIGURE 7 — TYPICAL FAILURE RATE versus JUNCTION TEMPERATURE

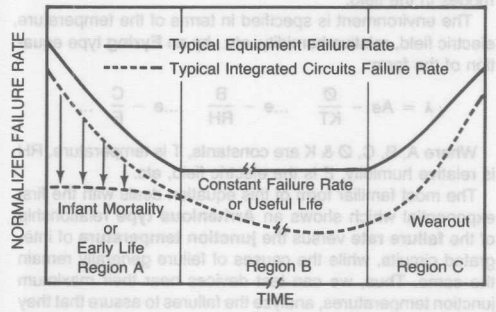


FIGURE 8 — FAILURE RATE versus TIME (BATHTUB CURVE)

There are three important regions identified on this curve. In Region A, the failure rate decreases with time and it is generally called **infant mortality** or early life failure region. In Region B, the failure rate has reached a relatively constant level and it is called **constant failure rate** or **useful life region.** In the third region, the failure rate increases again and it is called wearout region. Modern integrated circuits generally do not reach the wearout portion of the curve when operated under normal use conditions.

The **wearout** portion of the curve can usually be identified by using highly accelerated test conditions. For modern integrated circuits, even the useful life portion of the curve is characterized by so few failures compared to the accumulated device hours, that the **useful life** portion of the curve looks like a continuously decreasing failure rate curve (Figure 8, dotted line).

The **infant mortality** portion of the curve is of most interest to equipment manufacturers because of its impact on customer perception and potential warranty costs. In recent years the infant mortality portion of the curve for integrated circuits, and even equipment, has been drastically reduced (Figure 8, note arrows showing reduction of infant mortality). The reduction was accomplished by improvements in technology, emphasis on statistical process control, reliability modeling in design and reliability in manufacturing (wafer reliability, assembly reliability, etc.). In this respect many integrated circuit families have a continuously decreasing failure rate curve.

Does a user still need to consider burn-in? For this question to be answered properly the IC user must consider the **target failure rate** of the equipment, **apportioned** to the components used, application environment, maturity of equipment and components (new versus mature technology), the impact of a failure (i.e. safety versus casual entertainment), maintenance costs, etc. Therefore, if the IC user is going through these considerations for the first time, the question of burn-in at the component level should be discussed during a user-vendor interface meeting.

A frequently asked question is about the reliability differences between **plastic** versus **hermetic** packaged integrated circuits. In general, for all bipolar integrated circuits including linear, the field removal rates are the same for normal use environments, with many claims of plastic being better because of their "solid block" structure.

The tremendous increase in reliability of plastic packages has been accomplished by the continuous improvements in piece parts, materials and processes. Nevertheless differences can still be observed under highly accelerated environmental conditions. For example, if a bimetallic (gold wire and aluminum metallization) system is used in plastic packages and they are placed on a high temperature operating life test (125°C) then failures in the form of opens will be observed after 10,000 hours of continuous operating life at the gold to aluminum interface. Packages, whether plastic or hermetic, with a monometallic system (aluminum wire to aluminum metallization) will have no opens because of the absence of the gold to aluminum interface. As a result, a difference in failure rates will be observable.

Differences in failure rates between plastics and hermetics could be observed if devices from both packaging systems are placed in an environment of 85°C; 85% RH with bias applied. At some point in time plastic encapsulated ICs should fail since they are considered pervious by moisture, (the failure mechanism being corrosion of the aluminum metallization) while hermetic packages should not fail since they are considered impervious by moisture. The reason the word

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"should" was used is because advances in plastic compounds, package piece parts, encapsulation processes and final chip passivation have made plastic integrated circuits capable of operating more than 5000 hours without failures in an 85°C; 85% RH environment. Differences in failure rates due to internal corrosion between plastic and hermetic packages may not be observable until well after 5000 operating hours.

The aforementioned two examples had environments substantially more accelerated than normal life so these two issues discussed are not even a factor under normal use conditions. In addition, mechanisms inherent in hermetic packages but absent in plastics were not even considered here. Improved reliability of plastic encapsulated ICs has decreased demand of hermetic packages to the point where many devices are offered only in plastic packages. The user then should feel comfortable in using the present plastic packaging systems.

A final question that is asked by the IC users is: how can one be assured that the reliability of standard product does not degrade over time? This is accomplished by our emphasis on statistical process control, in-line reliability assessment and reliability auditing by periodic and strategic sampling and accelerated testing of the various integrated circuit device packaging systems. A description of these audit programs follows below.

Linear Reliability Audit Program

The reliability of a product is a function of design and manufacturing. Inherent reliability is the reliability which a product would have if there were no imperfections in the materials, piece parts and manufacturing processes of the product. The presence of imperfections gives risk to the actual reliability of the product.

Motorola uses on-line and off-line reliability monitoring in an attempt to prevent situations which could degrade reliability. On-line reliability monitoring is at the wafer and assembly levels while off-line reliability monitoring involves reliability assessment of the finished product through the use of accelerated environmental tests.

Continuous monitoring of the reliability of Linear integrated circuits is accompished by the Linear Reliability Audit Program, which is designed to compare the actual reliability to that specified. This objective is accomplished by periodic and strategic sampling of the various integrated circuit device packaging systems. The samples are tested by subjecting them to accelerated environmental conditions and the results are reviewed for unfavorable trends that would indicate a degradation of the reliability or quality of a particular packaging system. This provides the trigger mechanism for initiating an investigation for cause and corrective action. Concurrently, in order to provide a minimum of interruption of product flow and assure that the product is fit for use, a lot by lot sampling or a nondestructive type 100% screen is used to assure that a particular packaging system released for shipment does have the expected reliability. This rigorous surveillance is continued until there is sufficient proof (many consecutive lots) that the problem has been corrected.

The Standard Logic and Analog Integrated Circuits Group has used reliability audits since the late sixties. Such programs have been identified by acronyms such as CRP (Consumer Reliability Program), EPIIC (Environmental Package Indicators for Integrated Circuits), LAPP (Linear Accelerated Punishment Program), and RAP (Reliability Audit Program).

Currently, the Bipolar Analog Reliability Audit Program consists of a Weekly Reliability Audit and a Quarterly Reliability Audit. The Weekly Reliability Audit consists of rapid (short time) types of tests used to monitor the production lines on a real time basis. This type of testing is performed at the assembly/test sites worldwide. It provides data for use as an early warning system for identifying negative trends and triggering investigations for causes and corrective actions.

The Quarterly Reliability Audit consists of long term types of tests and is performed at the U.S. Bipolar Analog Division Center. The data obtained from the Quarterly Reliability Audit is used to assure that the correlation between the short term weekly tests and long term quarterly tests has not changed, and a new failure mechanism has not appeared.

A large data base is established by combining the results from the Weekly Reliability Audit with the results from the Quarterly Reliability Audit. Such a data base is necessary for estimating long term failure rates and evaluating potential process improvement changes. Also, after a process improvement change has been implemented, the Linear Reliability Audit Program provides a system for monitoring the change and the past history data base for evaluating the affect of the change.

Weekly Reliability Audit

The Weekly Reliability Audit is performed by each assembly/test site worldwide. The site must have capability for final electrical and quality assurance testing; reliability testing and first level of failure analysis. The results are reviewed on a continuous basis and corrective action is taken when appropriate. The results are accumulated on a monthly basis and published.

The Reliability Audit test plan is as follows:

Electrical Measurements: Performed initially and after each reliability test, consists of critical parameters and functional testing at 25°C on a go-no-go basis.

High Temperature Operating Life: Performed to detect failure mechanisms that are accelerated by a combination of temperature and electric fields. Procedure and conditions are per the MIL-STD-883, Method 1015 with an ambient temperature of 145°C for 40 hours or equivalent based on a 1.0eV activation energy and the Arrhenious equation.

Approximate Accelerated Factors

	125°C	50°C
145°C	4	4000
125°C	1	1000

Temperature Cycling/Thermal Shock: Performed to detect mechanisms related to thermal expansion and contraction of dissimilar materials, etc. Procedures and conditions are per MIL-STD-883, Methods 1010 or 1011, with ambient temperatures of −65°C to +150°C or −40°C to +125°C (JEDEC-STD-22-A104), minimum of 100 cycles.

Pressure Temperature Humidity (Autoclave): Performed to measure the moisture resistance of plastic encapsulated packages. It detects corrosion type failure mechanisms due to free ionic contaminants that may have entered the package during the manufacturing processes. Conditions are per

environment and 15psig. The duration of the test is 48 hours.

Analysis Procedure: Devices failing to meet the electrical criteria after being subjected to an accelerated environment type test are verified and characterized electrically, then submitted for failure analysis.

Quarterly Reliability Audit

The Quarterly Bipolar Analog Reliability Audit Program is performed at the U.S. Bipolar Analog Division Center. This testing is designed to assure that the correlation between the short term weekly tests and the longer quarterly tests has not changed and that no new failure mechanisms have appeared. It also provides additional long term information for a data base for estimating failure rates and evaluation of potential process improvement changes.

Electrical Measurements: Performed initially and at interim readouts, consist of all standard dc and functional parameters at 25°C, measured on a go-no-go basis.

High Temperature Operating Life Test: Performed to detect failure mechanisms that are accelerated by a combination of temperature and electric fields. Procedure and conditions are per MIL-STD-883, Method 1015, with an ambient temperature of 145°C for 40 and 250 hours or equivalent, based on 1.0eV activation energy and the Arrhenious equation.

Approximate Acceleration Factors

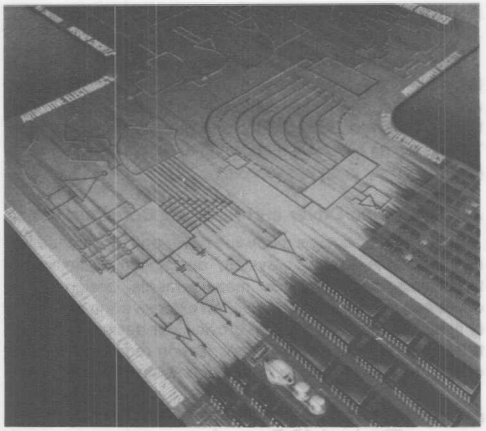
	125°C	50°C
145°C	4	4000
125°C	1	1000

Temperature Cycling/Thermal Shock: Performed to detect mechanisms related to thermal expansion and contraction, mismatch effects, etc. Procedure and conditions are per MIL-STD-883, Methods 1010 or 1011, with ambient temperatures of −65°C to +150°C or −40°C to +125°C (JEDEC-STD-22-A104) for 100 and 1000 cycles. Temperature Cycling and Thermal Shock are used interchangeably.

Pressure Humidity Bias (Biased Autoclave): This test measures the moisture resistance of plastic encapsulated packages. It detects corrosion type failure mechanism due to free and bounded ionic contaminants that may have entered the package during the manufacturing processes, or they may be bound in the materials of the integrated circuit packaging system and activated by the moisture and the applied electric fields. Conditions are per JEDEC-STD-22, Method 102, with bias applied. Temperature is 121°C, steam environment and 15psig. Duration is for 32 hours, with a 16 hour interim readout. This test detects the same type of failures as the Temperature Humidity Bias (85°C, 85% RH, with bias) test, only faster. The acceleration factor between PTHB and THB is between 20 and 40 times, depending on the type of corrosion mechanism, electric field and packaging system.

Temperature, Humidity and Bias (THB): This test measures the moisture resistance of plastic encapsulated packages. It detects corrosion type failure mechanisms due to free and bounded ionic contaminants that may have entered the package during the manufacturing processes, or they may be bound in the materials of the integrated circuit packaging system and activated by moisture and the applied electric fields. Conditions are per JEDEC-STD-22, Method 102 (85°C, 85% RH), with bias applied. The duration is for 1008 hours, with a 504 hour interim readout. The acceleration factor between THB (85°C, 85% RH and bias) and the 30°C, 90% RH is typically 40–50 times, depending on the type of corrosion mechanism, electric field and packaging system.

Analysis Procedure: Devices failing to meet the electrical criteria after being subjected to an accelerated environment type test are verified and characterized electrically, then submitted for failure analysis.



Applications Literature

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Applications Literature

The application literature listed in this section has been prepared to acquaint the circuits and systems engineer with Motorola Linear integrated circuits and their applications.

Application Note Abstracts

AN273A Getting More Value Out of an Integrated Operational Amplifier Data Sheet

The operational amplifier has become a basic building block in present day solid state electronic systems. The purpose of this application note is to provide a better understanding of the open loop characteristics of the amplifier and their significance to overall circuit operation. Also each parameter is defined and reviewed with respect to closed loop considerations. The importance of loop gain stability and bandwidth is discussed at length. Input offset voltage and current and resultant drift effects in the circuit are also reviewed with respect to closed loop operation.

AN489 Analysis and Basic Operation of the MC1595

The MC1595 monolithic linear four-quadrant multiplier is discussed. The equations for the analysis are given along with performance that is characteristic of the device. A few basic applications are given to assist the designer in system design.

AN513 A High Gain Integrated Circuit RF-IF Amplifier with Wide Range AGC

This note describes the operation and application of the MC1590G, a monolithic RF-IF amplifier. Included are several applications for IF amplifiers, a mixer, video amplifiers, single and two-stage RF amplifiers.

AN531 MC1596 Balanced Modulator

The MC1596 monolithic circuit is a highly versatile communications building block. In this note, both theoretical and practical information are given to aid the designer in the use of this part. Applications include modulators/demodulators for AM, SSB, and suppressed carrier AM; frequency doublers and HF/VHF double balanced mixers.

AN545A Television Video IF Amplifier Using Integrated Circuits

This applications note considers the requirements of the video IF amplifier section of a television receiver, and gives working circuit schematics using integrated circuits which have been specifically designed for consumer oriented products. The integrated circuits used are the MC1350, MC1352, and the MC1330.

AN587 Analysis and Design of the Op Amp Current Source

A voltage controlled current source utilizing an operational amplifier is discussed. Expressions for the transfer function and output impedances are developed using both the ideal and non-ideal op amp models. A section on analysis of the effects of op amp parameters and temperature variations on circuit performance is presented.

AN703 Designing Digitally-Controlled Power Supplies

This application note shows two design approaches; a basic low voltage supply using an inexpensive MC1723 voltage regulator and a high current, high voltage, supply using the MC1466 floating regulator with optoelectronic isolation. Various circuit options are shown to allow the designer maximum flexibility in an application.

AN708A Line Driver and Receiver Considerations

This report discusses many line driver and receiver design considerations such as system description, definition of terms, important parameter measurements, design procedures and application examples. An extensive line of devices is available from Motorola to provide the designer with the tools to implement the data transmission requirements necessary for almost every type of transmission system.

AN727 Television Horizontal APC/AFC Loops: The Last 10 Percent

A discussion of some common problems that may be encountered with the design of Horizontal APC/AFC loops and methods to avoid or overcome them.

AN778 Mounting Techniques for Power Semiconductors

For reliable operation, semiconductors must be properly mounted. Discussed are aspects of preparing the mounting surface, using thermal compounds, insulation techniques, fastening techniques, handling of leads and pins, and evaluation methods for the thermal system.

AN781A Revised Data Interface Standards

This application note provides a brief overview and comparison of communication interface standards EIA-232-C, EIA-422A, EIA-423, EIA-449 and EIA-485 for the hardware designer. A listing of the standard's specifications and appropriate Motorola devices are included.

AN829 Application of the MC1374 TV Modulator

The MC1374 was designed for use in applications where separate audio and composite video signals are available, which need converting to a high quality VHF television signal. It's idealy suited as an output device for subscription TV decoders, video disk and video tape players.

AN879 Monomax — Application of the MC13001 Monochrome Television Integrated Circuit

This application note presents a complete 12″ black and white line-operated television receiver, including artwork for the printed circuit board. It is intended to provide a good starting point for the first-time user. Some of the most common pitfalls are overcome, and the significance of component selections and locations are discussed.

AN917 Reading and Writing in Floppy Disk Systems Using Motorola Integrated Circuits

The floppy disk system has become a widely used means for storing and retrieving both programs and data. A floppy disk drive requires precision controls to position and load the head as well as defined read/write signals in order to be a viable system. This application note describes the use of the

APPLICATIONS LITERATURE (continued)

MC3469 and MC3471 Write Control ICs and the MC3470 Read Amplifier which provide the necessary head and erase control, timing functions, and filtering.

AN920A Theory and Applications of the MC34063 and μA78S40 Switching Regulator Control Circuits

This paper describes in detail the principle of operation of the MC34063 and μA78S40 switching regulator subsystems. Several converter design examples and numerous applications circuits with test data are included.

AN926 Techniques for Improving the Settling Time of a DAC & Op Amp Combination

This application note describes some techniques which were tested for the purpose of optimizing settling time of a DAC/op amp combination. The objective of the experimentation was to obtain a settling time of under 1.0 μs for 12 bit (±0.012%) accuracy. Op amps chosen for this exercise are high speed, yet inexpensive monolithic devices.

AN932 Application of the MC1377 Color Encoder

The MC1377 is an economical, high quality, RGB encoder for NTSC or PAL applications. It accepts red, green, blue, and composite sync inputs and delivers IVpp composite NTSC or PAL video output into a 75 ohm load. It can provide its own color oscillator and burst gating, or it can be easily driven from external sources. Performance virtually equal to high cost studio equipment is possible with common color receiver components. The following note is intended to explain the operation of the device and guide the prospective user in selecting the optimum circuit for his needs.

AN933 A Variety of Uses for the MC34012 and MC34017 Tone Ringers

The MC34012 and MC34017 electronic tone ringers were developed to replace the bulky electromechanical bell assembly of a telephone, while providing the same basic function. When used in conjunction with a piezo ceramic transducer, these circuits will output a warbling sound in response to the applied ringing voltage. With some imagination, however, the circuits can be used in a variety of ways, including non-telephone applications, — wherever an alerting sound or indication is required. Applications include appliance buzzers, burglar alarms, safety alerting functions, special sound effects, visual ringing indicators, and others. The circuits in this application note show how a variety of effects can be obtained.

AN937 A Telephone Ringer Which Complies with FCC and EIA Impedance Standards

The MC34012 and MC34017 Tone Ringers are designed to replace the bulky bell assembly of a telephone, while providing the same function and performance under a variety of conditions. The operational requirements spelled out by the FCC and the EIA, simply stated, are that a ringer circuit MUST function when a ringing signal is provided, and MUST NOT ring when other signals (speech, dialing signals, noise) are on the line. This application note discusses how the IC's operate, the specific operational requirements to be met, and how they are met. Only "on-hook" requirements are discussed since off-hook operation is not applicable.

AN954 A Unique Converter Configuration Provides Step-Up/Down Functions

The use of switching regulators in new portable equipment designs is becoming more pronounced over that of linear regulators. This is primarily due to the need for reductions in size and weight which dictate an ever increasing demand for higher power conversion efficiency from a battery pack. When designing at the board level it sometimes becomes necessary to generate a constant output voltage that is less than that of the battery. The step-down circuit will perform this function efficiently. However, as the battery discharges, its terminal voltage will eventually fall below the desired output, and in order to utilize the remaining battery energy, the step-up circuit will be required.

AN957 Interfacing the Speakerphone to the MC34010/11/13 Speech Networks

Interfacing the MC34018 speakerphone circuit to the MC34010 series of telephone circuits is described in this application note. The series includes the MC34010, MC34011, MC34013, and the new "A" version of each of those. The interface is applicable to existing designs, as well as to new designs.

AN958 Transmit Gain Adjustments for the MC34014 Speech Network

The MC34014 telephone speech network provides for direct connection to an electret microphone and to Tip and Ring. In between, the circuit provides gain, drive capability, and determination of the ac impedance for compatability with the telephone lines. Since different microphones have different sensitivity levels, different gain levels are required from the microphone to the Tip and Ring lines. This application note will discuss how to change the gain level to suit a particular microphone while not affecting the other circuit parameters.

AN959 A Speakerphone with Receive Idle Mode

The MC34018 speakerphone system operates on the principle of comparing the transmit and receive signals to determine which is stronger, and then switching the circuit into that mode. Under conditions where noise from the telephone line (in the receive path) exceeds the background noise in the transmit path, the speakerphone will switch easily, or even lock, into the receive mode. Under these conditions the conversation will sound "dead" to the party at the far-end. It will also be more difficult for the near-end party to activate the transmit channel since the transmit detection is at the output of the transmit attenuator, which will be at maximum attenuation during this time. The addition of a receive idle mode can alleviate this problem by ensuring that the transmit and receive gains will be approximately equal when no voice signals are present. This allows the far-end party to hear ambient noises, and also increases the sensitivity to transmit signals.

AN960 Equalization of DTMF Signals Using the MC34014

This application note will describe how to obtain equalization (line length compensation) of the DTMF dialing tones using the MC34014 speech network. While the MC34014 does not have an internal dialer, it has the interface for a dialer so as to provide the means for putting the DTMF tones onto the Tip & Ring lines. The Equalization amplifier, whose gain varies with loop current, was meant primarily to equalize the speech signals. However, by adding one resistor, it can be used to equalize the DTMF signals as well.

AN963 Interfacing the MC6108 A/D to a Microprocessor — It's Easier Than You Think!

This application note will supplement information in the

APPLICATIONS LITERATURE (continued)

MC6108 data sheet by describing the detailed requirements for interfacing the Analog-to-Digital converter to a microprocessor. The hardware requirements, and the programming necessary to execute a conversion and read the data, in several different configurations, will be discussed. The microprocessor used in developing this application note is the MC6802 (operating off a 3.58 MHz crystal), a representative sample of the MC6800 family.

Because of the short conversion time of the MC6108, "Wait" states and "Wait for Interrupt" instructions are generally not needed with most microprocessors. The microprocessor can issue a CONVERT instruction, and immediately thereafter, issue a READ instruction, regardless of whether the MC6108 is read through a port (MC6821), or read off the bus directly.

AN976 A New High Performance Current Mode Controller Teams Up with Current Sensing Power MOSFETs

A new current mode control IC that interfaces directly with current sensing power MOSFETs is described. Its second generation architecture is shown to provide a variety of advantages in current mode power supplies. The most notable of these advantages is a "lossless" current sensing capability that is provided when used with current sensing MOSFETs.

Included in the discussion are subtle factors to watch out for in practical designs, and an applications example.

AN980 Low Power FM Dual Conversion Receivers MC3362/3/4

Motorola has recently developed a series of low power FM dual conversion receivers in monolithic silicon integrated circuits. The MC3362/3/4 series is ideal for application in cordless phones, narrowband voice and data receivers, CB and amateur band radios, RF security devices, and other applications through 150 MHz.

AN983 A Simplified Power Supply Design Using the TL494 Control Circuit

This describes the operation and characteristics of the TL494 Switchmode™ Voltage Regulator and shows its application in a 400-watt off-line power supply.

The TL494 is a fixed-frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply.

AN1002 A Handsfree Featurephone Design Using the MC34114 Speech Network and the MC34018 Speakerphone ICs

This application note describes the procedure for combining the MC34114 speech network with the MC34018 speakerphone circuit into a featurephone which includes the following functions: ten number memory pulse/tone dialer, tone ringer, a "Privacy" (Mike Mute) function, and line length compensation for both handset and speakerphone operation.

Three circuits are developed in this discussion: a line-powered featurephone, a line-powered featurephone with a booster (for using the speakerphone on long lines), and one powered from a power supply. The circuits are nearly identical, except for the Tip/Ring interface. Their performance, however, differs noticeably, particularly in the low loop current range. Initially, the discussion will focus on the line-powered circuit.

ANE002 130 W Ringing Choke Power Supply Using TDA4601

The architecture is based on the fly-back mode working in a free switching mode. Frequency range varies between 20 kHz at full load and 70 kHz in the standby condition (also called sleep-mode). Input power is from the line (220 Vac) and is completely isolated from the output. Control and regulation are achieved by the TDA4601.

The power supply presents a linear foldback characteristic and is short circuit proof. An undervoltage inhibit provides a protection against low line voltage.

The complete system is an excellent compromise between complexity, cost and performance.

AN-HK-07 A High Performance Manually Tuned AM Stereo Receiver for Automotive Application Using MOTOROLA ICs MC13021, MC13020 and MC13041

This application note presents a high performance manually tuned automotive AM stereo receiver design using MOTOROLA AM stereo ICs; MC13021, MC13020 and the MC13041. It is intended to provide radio design engineers with a good start in automotive AM stereo receiver design. The note consists of two parts; the first describes all relative important principles of a manually tuned AM stereo receiver, and the second part details the AM stereo receiver design for automotive application.

Article Reprints

AR115

A bipolar quad op amp having a JFET-like 4.5 MHz bandwidth resolves common mode input voltages and sinks output current close to the ground rail — even with a single +5.0 V supply.

Engineering Bulletin Abstracts

EB20 Multiplier/Op Amp Circuit Detects True RMS

Two op amps and two multipliers are used in the circuit described in EB20 to obtain the true rms of an input voltage ranging from 2.0 to 10 Vpk.

EB51 Successive Approximation BCD A/D Converter

A successive approximation A/D converter in which a digital-to-analog converter in a feedback loop produces a BCD digital output from an analog input is described in EB51.